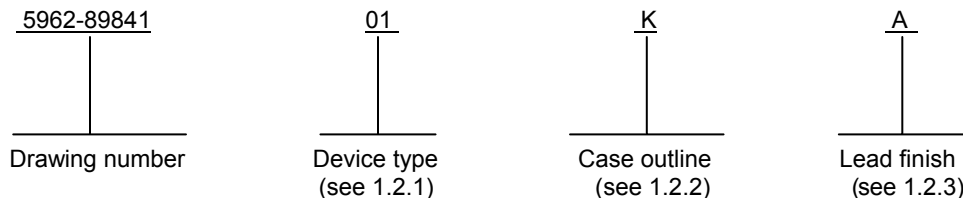


| REVISIONS  |   |    |    |                                       |       |         |   |   |  |                           |                   |   |   |   |                 |                 |    |    |    |
|--|---|----|----|---------------------------------------|-------|---------|---|---|--|---------------------------|-------------------|---|---|---|-----------------|-----------------|----|----|----|
| LTR  | DESCRIPTION   |    |    |                                       |       |         |   |   |  |                           |                   |   |   |   | DATE (YR-MO-DA) | APPROVED        |    |    |    |
| A  | Added K package. Added 04 device, two suppliers and 05 device, one supplier. Added vendor CAGE 34335 for devices 01L, 013, and 02L. Editorial changes throughout. Added vendor CAGE 34335 for devices 01K, 023, and 02K. Redrawn. |    |    |                                       |       |         |   |   |  |                           |                   |   |   |   | 91 - 04 - 19    | M. A. Frye      |    |    |    |
| B  | Added vendor CAGE 65786 for devices 01, 02, 03, 04, and 05LX, KX, and 3X. Added vendor CAGE 18324 for devices 01, 02, 04, and 05LX. IAW NOR 5962-R079-93.   |    |    |                                       |       |         |   |   |  |                           |                   |   |   |   | 93 - 01 - 28    | M. A. Frye      |    |    |    |
| C  | Added 06 device for one supplier. Added test $t_{SU2}$ to table I. Editorial changes throughout. Redrawn.   |    |    |                                       |       |         |   |   |  |                           |                   |   |   |   | 93 - 07 - 30    | M. A. Frye      |    |    |    |
| D  | Added devices 07-14, Added CAGE 1FN41 for devices 13 and 14, added test $I_{CCSB}$ to table I for devices 13 and 14, and updated text to newer boiler plate.  |    |    |                                       |       |         |   |   |  |                           |                   |   |   |   | 97 - 03 - 04    | Raymond Monnin  |    |    |    |
| E  | Changes in accordance with NOR 5962-R263-97   |    |    |                                       |       |         |   |   |  |                           |                   |   |   |   | 97 - 04 - 23    | Raymond Monnin  |    |    |    |
| F  | Changes in accordance with NOR 5962-R341-97   |    |    |                                       |       |         |   |   |  |                           |                   |   |   |   | 97 - 06 - 05    | Raymond Monnin  |    |    |    |
| G  | Added powerup-reset parameters to table I, and the waveform as figure 5. Updated boilerplate. ksr   |    |    |                                       |       |         |   |   |  |                           |                   |   |   |   | 98 - 07 - 10    | Raymond Monnin  |    |    |    |
| H  | Changed minimum IOS value for devices 01 thru 06 on table I. Value was changed from -50 mA to -30 mA. ksr   |    |    |                                       |       |         |   |   |  |                           |                   |   |   |   | 99 - 03 - 19    | Raymond Monnin  |    |    |    |
| J  | Updated boiler plate. ksr   |    |    |                                       |       |         |   |   |  |                           |                   |   |   |   | 02 - 10 - 10    | Raymond Monnin  |    |    |    |
| K  | Boilerplate update, part of 5 year review. ksr  |    |    |                                       |       |         |   |   |  |                           |                   |   |   |   | 08 - 06 - 04    | Robert M. Heber |    |    |    |
| L  | Added devices 15 and 16. Updated Table I, added Figure 6 for devices 15 and 16. ksr   |    |    |                                       |       |         |   |   |  |                           |                   |   |   |   | 08 - 08 - 25    | Robert M. Heber |    |    |    |
|  |   |    |    |                                       |       |         |   |   |  |                           |                   |   |   |   |                 |                 |    |    |    |
| REV  |   |    |    |                                       |       |         |   |   |  |                           |                   |   |   |   |                 |                 |    |    |    |
| SHEET  |   |    |    |                                       |       |         |   |   |  |                           |                   |   |   |   |                 |                 |    |    |    |
| REV  | L   | L  | L  | L                                     | L     |         |   |   |  |                           |                   |   |   |   |                 |                 |    |    |    |
| SHEET  | 15  | 16 | 17 | 18                                    | 19    |         |   |   |  |                           |                   |   |   |   |                 |                 |    |    |    |
| REV STATUS OF SHEETS   |   |    |    | REV                                   |       | L       | L | L | L  | L                         | L                 | L | L | L | L               | L               | L  | L  | L  |
|  |   |    |    | SHEET                                 |       | 1       | 2 | 3 | 4  | 5                         | 6                 | 7 | 8 | 9 | 10              | 11              | 12 | 13 | 14 |
| PMIC N/A   |   |    |    | PREPARED BY<br>Kenneth Rice           |       |         |   |   | <b>DEFENSE SUPPLY CENTER COLUMBUS</b><br><b>COLUMBUS, OHIO 43218-3990</b><br><a href="http://www.dscc.dla.mil">http://www.dscc.dla.mil</a> |                           |                   |   |   |   |                 |                 |    |    |    |
| <b>STANDARD MICROCIRCUIT DRAWING</b><br>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE<br>AMSC N/A |   |    |    | CHECKED BY<br>Charles Reusing         |       |         |   |   |  |                           |                   |   |   |   |                 |                 |    |    |    |
|  |   |    |    | APPROVED BY<br>Michael A. Frye        |       |         |   |   | <b>MICROCIRCUIT, MEMORY, DIGITAL, CMOS, PROGRAMMABLE ARRAY LOGIC (EEPLD), MONOLITHIC SILICON</b>   |                           |                   |   |   |   |                 |                 |    |    |    |
|  |   |    |    | DRAWING APPROVAL DATE<br>89 - 11 - 28 |       |         |   |   |  |                           |                   |   |   |   |                 |                 |    |    |    |
|  |   |    |    | REVISION LEVEL<br>L                   |       |         |   |   | SIZE<br>A  | CAGE CODE<br><b>67268</b> | <b>5962-89841</b> |   |   |   |                 |                 |    |    |    |
|  |   |    |    |                                       | SHEET | 1 OF 19 |   |   |  |                           |                   |   |   |   |                 |                 |    |    |    |

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

| Device type | Generic number | Circuit function  | Access time |
|-------------|----------------|---|-------------|
| 01, 07      | 22V10          | 22-input, 10-output, EECMOS, architecturally generic, programmable AND-OR array                           | 30          |
| 02, 08      | 22V10          | 22-input, 10-output, EECMOS, architecturally generic, programmable AND-OR array                           | 20          |
| 03, 09, 15  | 22V10          | 22-input, 10-output, EECMOS, architecturally generic, programmable AND-OR array                           | 15          |
| 04, 10      | 22V10          | 22-input, 10-output, EECMOS, architecturally generic, programmable AND-OR array                           | 25          |
| 05, 11      | 22V10          | 22-input, 10-output, EECMOS, architecturally generic, programmable AND-OR array (higher tCO, lower fCLK2) | 15          |
| 06, 12, 16  | 22V10          | 22-input, 10-output, EECMOS, architecturally generic, programmable AND-OR array                           | 10          |
| 13          | 22V10L         | 22-input, 10-output, EECMOS, architecturally generic, programmable AND-OR array                           | 25          |
| 14          | 22V10L         | 22-input, 10-output, EECMOS, architecturally generic, programmable AND-OR array                           | 20          |

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style       |
|----------------|------------------------|-----------|---------------------|
| K              | GDFP2-F24 or CDFP3-F24 | 24        | flat pack           |
| L              | GDIP3-T24 or CDIP4-T24 | 24        | dual-in-line        |
| 3              | CQCC1-N28              | 28        | square chip carrier |

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

|  |  |
|--|--|
| Supply voltage range -----   | -0.5 V dc to +7.0 V dc                           |
| Input voltage applied -----  | -0.5 V dc to V <sub>CC</sub> +1.0 V dc <u>1/</u> |
| Off-state output voltage applied -----                             | -0.5 V dc to V <sub>CC</sub> +1.0 V dc <u>1/</u> |
| Storage temperature range (T <sub>STG</sub> ) -----                | -65°C to +150°C                                  |
| Maximum power dissipation (P <sub>D</sub> ) <u>2/</u> -----        | 1.5 W  |
| Lead temperature (soldering, 10 seconds) (T <sub>SOL</sub> ) ----- | +260°C   |
| Thermal resistance, junction-to-case (Θ <sub>JC</sub> ) -----      | See MIL-STD-1835                                 |
| Junction temperature (T <sub>J</sub> ) -----                       | +175°C   |
| Data retention -----   | 10 years (minimum)                               |
| Endurance -----  | 100 erase/write cycles (minimum)                 |

1/ Minimum voltage is -0.5 V which may undershoot to -2.5 V for pulses of less than 20 ns.

2/ Must withstand the added P<sub>D</sub> due to short circuit test; e.g., I<sub>OS</sub>.

|   |                     |                   |
|---|---------------------|-------------------|
| <b>STANDARD<br/>MICROCIRCUIT DRAWING</b>                            | SIZE<br><b>A</b>    | <b>5962-89841</b> |
| <b>DEFENSE SUPPLY CENTER COLUMBUS<br/>COLUMBUS, OHIO 43218-3990</b> | REVISION LEVEL<br>L | SHEET<br>2        |

1.4 Recommended operating conditions.

|   |                                    |
|---|------------------------------------|
| Supply voltage range ( $V_{CC}$ )-----          | 4.5 V dc to 5.5 V dc               |
| High level input voltage ( $V_{IH}$ )-----      | 2.0 V dc to $V_{CC} + 1.0$ V dc    |
| Low level input voltage ( $V_{IL}$ )-----       | $V_{SS} - 0.5$ V dc to $+0.8$ V dc |
| High level output current ( $I_{OH}$ )-----     | -2.0 mA maximum                    |
| Low level output current ( $I_{OL}$ )-----      | 12 mA maximum                      |
| Case operating temperature range ( $T_C$ )----- | -55°C to +125°C                    |

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.  
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.  
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.2.1 Unprogrammed devices. The truth table for unprogrammed devices shall be as specified on figure 2.

3.2.2.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.2.3 Case outlines The case outlines shall be in accordance with 1.2.2 herein.

|   |                  |                     |                   |
|---|------------------|---------------------|-------------------|
| <b>STANDARD<br/>MICROCIRCUIT DRAWING</b><br><br><b>DEFENSE SUPPLY CENTER COLUMBUS</b><br><b>COLUMBUS, OHIO 43218-3990</b> | SIZE<br><b>A</b> |                     | <b>5962-89841</b> |
|   |                  | REVISION LEVEL<br>L | SHEET<br>3        |

Table I. Electrical performance characteristics.

| Test   | Symbol             | Conditions<br>-55°C ≤ T <sub>C</sub> ≤ +125°C<br>V <sub>SS</sub> = 0 V, 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V<br>unless otherwise specified | Group A<br>subgroups | Device<br>type      | Limits |      | Unit |
|--|--------------------|---|----------------------|---------------------|--------|------|------|
|  |                    |   |                      |                     | Min    | Max  |      |
| Input leakage current <u>1/</u>                | I <sub>LX</sub>    | 0.0 V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>   | 1, 2, 3              | 01-06,<br>13,14     | 10     | -150 | μA   |
|  |                    |   |                      | 7-12                | -10    | 10   |      |
|  |                    |   |                      | <u>2/</u><br>15, 16 | -10    | 10   |      |
| Bidirectional pin leakage<br>current <u>1/</u> | I <sub>I/O/Q</sub> | 0.0 V ≤ V <sub>I/O/Q</sub> ≤ V <sub>CC</sub>  | 1, 2, 3              | 01-06,<br>13,14     | 10     | -150 | μA   |
|  |                    |   |                      | 7-12                | -40    | 40   |      |
|  |                    |   |                      | <u>2/</u><br>15, 16 | -10    | 10   |      |
| Output low voltage                             | V <sub>OL</sub>    | V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 12 mA,<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>                             | 1, 2, 3              | All                 |        | 0.5  | V    |
| Output high voltage                            | V <sub>OH</sub>    | V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -2 mA,<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>                             | 1, 2, 3              | All                 | 2.4    |      | V    |
| Input low voltage <u>3/</u>                    | V <sub>IL</sub>    |   | 1, 2, 3              | All                 |        | 0.8  | V    |
| Input high voltage <u>3/</u>                   | V <sub>IH</sub>    |   | 1, 2, 3              | All                 | 2.0    |      | V    |
| Operating power supply<br>current              | I <sub>CC</sub>    | V <sub>IL</sub> = 0.5 V, V <sub>IH</sub> = 3.0 V<br><br>f <sub>tog</sub> = 15 MHz   | 1, 2, 3              | 01-06               |        | 150  | mA   |
|  |                    |   |                      | 07-12               |        | 130  |      |
|  |                    |   |                      | 13,14               |        | 70   |      |
|  |                    |   |                      | 15,16               |        | 160  |      |
| Power supply<br>current standby                | I <sub>CCSB</sub>  | V <sub>IN</sub> 0 V or V <sub>CC</sub><br>f <sub>tog</sub> = 0 MHz  | 1, 2, 3              | 13,14               |        | 15   | mA   |
| Output short circuit<br>current <u>4/</u>      | I <sub>OS</sub>    | V <sub>CC</sub> = 5.0 V, V <sub>OUT</sub> = 0.5 V<br><br>T <sub>A</sub> = 25°C see 4.3.1d   | 1, 2, 3              | 01-06               | -30    | -135 | mA   |
|  |                    |   |                      | 07-12               | -30    | -90  |      |
| Input capacitance                              | C <sub>IN</sub>    | V <sub>CC</sub> = 5.0 V, V <sub>I</sub> = 2.0 V<br>f = 1.0 MHz, T <sub>A</sub> = +25°C,<br>See 4.3.1c                                 | 4                    | All                 |        | 10   | pF   |
| Bidirectional pin<br>capacitance               | C <sub>I/O/Q</sub> | V <sub>CC</sub> = 5.0 V, V <sub>I/O/Q</sub> = 2.0 V<br><br>f = 1.0 MHz, T <sub>A</sub> = +25°C,<br>See 4.3.1c                         | 4                    | All                 |        | 10   | pF   |
| Functional tests                               |                    | See 4.3.1e  | 7, 8A,8B             | All                 |        |      |      |

See footnotes at end of table.

|   |                  |                     |                   |
|---|------------------|---------------------|-------------------|
| <b>STANDARD<br/>MICROCIRCUIT DRAWING</b><br><br><b>DEFENSE SUPPLY CENTER COLUMBUS</b><br><b>COLUMBUS, OHIO 43218-3990</b> | SIZE<br><b>A</b> |                     | <b>5962-89841</b> |
|   |                  | REVISION LEVEL<br>L | SHEET<br>4        |

Table I. Electrical performance characteristics - Continued.

| Test   | Symbol          | Conditions<br>-55°C ≤ T <sub>C</sub> ≤ +125°C<br>V <sub>SS</sub> = 0 V, 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V<br>unless otherwise specified | Group A<br>subgroups | Device<br>type              | Limits |     | Unit |
|--|-----------------|---|----------------------|-----------------------------|--------|-----|------|
|  |                 |   |                      |                             | Min    | Max |      |
| Input or feedback to<br>nonregistered output | t <sub>PD</sub> | V <sub>CC</sub> = 4.5 V, see figures<br>3 and 4 5/  | 9, 10, 11            | 01                          |        | 30  | ns   |
|  |                 |   |                      | 02                          |        | 20  |      |
|  |                 |   |                      | 03, 05,<br>15               |        | 15  |      |
|  |                 |   |                      | 08, 09,<br>11               | 3      | 15  |      |
|  |                 |   |                      | 04                          |        | 25  |      |
|  |                 |   |                      | 06, 16                      |        | 10  |      |
|  |                 |   |                      | 12                          | 3      | 10  |      |
|  |                 |   |                      | 07, 10,<br>13               | 3      | 25  |      |
| Clock to output delay 6/                     | t <sub>CO</sub> |   | 9, 10, 11            | 01,04                       |        | 20  | ns   |
|  |                 |   |                      | 02                          |        | 15  |      |
|  |                 |   |                      | 07, 10,<br>14               | 2      | 15  |      |
|  |                 |   |                      | 03, 15                      |        | 8   |      |
|  |                 |   |                      | 08, 09,<br>11               | 2      | 8   |      |
|  |                 |   |                      | 05                          |        | 12  |      |
|  |                 |   |                      | 06, 16                      |        | 7   |      |
|  |                 |   |                      | 12                          | 2      | 7   |      |
| Input to output enable                       | t <sub>EA</sub> |   | 9, 10, 11            | 01,04,<br>07,10,<br>13      |        | 25  | ns   |
|  |                 |   |                      | 02, 14                      |        | 20  |      |
|  |                 |   |                      | 03, 05,<br>08,09,<br>11, 15 |        | 15  |      |
|  |                 |   |                      | 06, 12,<br>16               |        | 10  |      |
| Input to output disable 7/                   | t <sub>ER</sub> |   | 9, 10, 11            | 01,04,<br>07,10,<br>13,     |        | 25  | ns   |
|  |                 |   |                      | 02, 14                      |        | 20  |      |
|  |                 |   |                      | 03, 05,<br>08,09,<br>11,15  |        | 15  |      |
|  |                 |   |                      | 06, 16                      |        | 12  |      |
|  |                 |   |                      | 12                          |        | 10  |      |

See footnotes at end of table.

|   |                  |                     |                   |
|---|------------------|---------------------|-------------------|
| <b>STANDARD<br/>MICROCIRCUIT DRAWING</b><br><br><b>DEFENSE SUPPLY CENTER COLUMBUS</b><br><b>COLUMBUS, OHIO 43218-3990</b> | SIZE<br><b>A</b> |                     | <b>5962-89841</b> |
|   |                  | REVISION LEVEL<br>L | SHEET<br>5        |

Table I. Electrical performance characteristics – Continued.

| Test   | Symbol            | Conditions<br>-55°C ≤ T <sub>C</sub> ≤ +125°C<br>V <sub>SS</sub> = 0 V, 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V<br>unless otherwise specified | Group A<br>subgroups | Device<br>type             | Limits |       | Unit |
|--|-------------------|---|----------------------|----------------------------|--------|-------|------|
|  |                   |   |                      |                            | Min    | Max   |      |
| Asynchronous register<br>reset <u>6/</u>   | t <sub>RES</sub>  | V <sub>CC</sub> = 4.5 V, see figures<br>3 and 4 <u>5/</u>   | 9, 10, 11            | 01,04,<br>13               |        | 30    | ns   |
|  |                   |   |                      | 02,07,<br>10,14            |        | 25    |      |
|  |                   |   |                      | 03,05,<br>08,09,<br>11, 15 |        | 20    |      |
|  |                   |   |                      | 06,12,<br>16               |        | 12    |      |
| Clock frequency without<br>feedback <u>6/ 8/</u><br>1/(t <sub>PWH</sub> + t <sub>PWL</sub> ) | f <sub>CLK1</sub> |   | 9, 10, 11            | 01                         | 0      | 25.0  | MHz  |
|  |                   |   |                      | 02,14,<br>07,10            | 0      | 33.3  |      |
|  |                   |   |                      | 03, 05                     | 0      | 35.7  |      |
|  |                   |   |                      | 08, 09,<br>11              | 0      | 62.5  |      |
|  |                   |   |                      | 04, 13                     | 0      | 83.3  |      |
|  |                   |   |                      | 15                         | 0      | 33.0  |      |
|  |                   |   |                      | 12                         | 0      | 100.0 |      |
|  |                   |   |                      | 16                         | 0      | 142.0 |      |
|  |                   |   |                      | 06                         | 0      | 143.0 |      |
| Clock frequency with<br>feedback <u>6/ 8/</u><br>1/(t <sub>CO</sub> + t <sub>SU1</sub> )     | f <sub>CLK2</sub> |   | 9, 10, 11            | 01                         | 0.0    | 22.0  | MHz  |
|  |                   |   |                      | 07,10                      | 0.0    | 30.3  |      |
|  |                   |   |                      | 02,14                      | 0.0    | 31.2  |      |
|  |                   |   |                      | 03,08,<br>09,11            | 0.0    | 50.0  |      |
|  |                   |   |                      | 04, 13                     | 0.0    | 26.3  |      |
|  |                   |   |                      | 05                         | 0.0    | 42.0  |      |
|  |                   |   |                      | 15                         | 0.0    | 62.5  |      |
|  |                   |   |                      | 16                         | 0.0    | 83.3  |      |
|  |                   |   |                      | 06,12                      | 0.0    | 76.9  |      |
| Input or feedback setup<br>time before rising clock<br><u>6/</u>                             | t <sub>SU1</sub>  |   | 9, 10, 11            | 01                         | 25     |       | ns   |
|  |                   |   |                      | 02, 14                     | 17     |       |      |
|  |                   |   |                      | 03,05                      | 12     |       |      |
|  |                   |   |                      | 08, 09,<br>11              | 10     |       |      |
|  |                   |   |                      | 04, 07,<br>10, 13          | 18     |       |      |
|  |                   |   |                      | 15                         | 8      |       |      |
|  |                   |   |                      | 06, 12                     | 6      |       |      |
|  |                   |   |                      | 16                         | 5      |       |      |

See footnotes at end of table.

|   |                  |                     |                   |
|---|------------------|---------------------|-------------------|
| <b>STANDARD<br/>MICROCIRCUIT DRAWING</b><br><br><b>DEFENSE SUPPLY CENTER COLUMBUS</b><br><b>COLUMBUS, OHIO 43218-3990</b> | SIZE<br><b>A</b> |                     | <b>5962-89841</b> |
|   |                  | REVISION LEVEL<br>L | SHEET<br>6        |

Table I. Electrical performance characteristics - Continued.

| Test   | Symbol           | Conditions<br>-55°C ≤ T <sub>C</sub> ≤ +125°C<br>V <sub>SS</sub> = 0 V, 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V<br>unless otherwise specified | Group A<br>subgroups | Device<br>type      | Limits |     | Unit |
|--|------------------|---|----------------------|---------------------|--------|-----|------|
|  |                  |   |                      |                     | Min    | Max |      |
| Synchronous Preset<br>setup time                               | t <sub>SU2</sub> | V <sub>CC</sub> = 4.5 V, see figures<br>3 and 4 <u>5/</u>   | 9, 10, 11            | 01                  | 25     |     | ns   |
|  |                  |   |                      | 02, 14              | 17     |     |      |
|  |                  |   |                      | 08, 09,<br>11       | 10     |     |      |
|  |                  |   |                      | 03, 05,<br>15       | 12     |     |      |
|  |                  |   |                      | 04, 07,<br>10, 13   | 18     |     |      |
|  |                  |   |                      | 06, 12,<br>16       | 7      |     |      |
| Input or feedback hold<br>time after rising<br>clock <u>6/</u> | t <sub>h</sub>   |   | 9, 10, 11            | All                 | 0      |     | ns   |
| Clock pulse width, high<br><u>6/</u>                           | t <sub>PWH</sub> |   | 9, 10, 11            | 01                  | 20     |     | ns   |
|  |                  |   |                      | 02, 14              | 15     |     |      |
|  |                  |   |                      | 03, 05              | 8      |     |      |
|  |                  |   |                      | 04, 13              | 15     |     |      |
|  |                  |   |                      | 07, 10              | 14     |     |      |
|  |                  |   |                      | 08, 09,<br>11       | 6      |     |      |
|  |                  |   |                      | 15                  | 5      |     |      |
|  |                  |   |                      | 06, 12<br><u>7/</u> | 3      |     |      |
| Clock pulse width, low<br><u>6/</u>                            | t <sub>PWL</sub> |   | 9, 10, 11            | 01                  | 20     |     | ns   |
|  |                  |   |                      | 02, 14              | 15     |     |      |
|  |                  |   |                      | 03, 05              | 8      |     |      |
|  |                  |   |                      | 04, 13              | 15     |     |      |
|  |                  |   |                      | 07, 10              | 14     |     |      |
|  |                  |   |                      | 08, 09,<br>11       | 6      |     |      |
|  |                  |   |                      | 15                  | 5      |     |      |
|  |                  |   |                      | 06, 12<br><u>7/</u> | 3      |     |      |
|  | 16               | 3.5   |                      |                     |        |     |      |

|   |                         |                                   |                          |
|---|-------------------------|-----------------------------------|--------------------------|
| <b>STANDARD<br/>MICROCIRCUIT DRAWING</b><br><br><b>DEFENSE SUPPLY CENTER COLUMBUS</b><br><b>COLUMBUS, OHIO 43218-3990</b> | <b>SIZE</b><br><b>A</b> |                                   | <b>5962-89841</b>        |
|   |                         | <b>REVISION LEVEL</b><br><b>L</b> | <b>SHEET</b><br><b>7</b> |

Table I. Electrical performance characteristics - Continued.

| Test  | Symbol           | Conditions<br>-55°C ≤ T <sub>C</sub> ≤ +125°C<br>V <sub>SS</sub> = 0 V, 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V<br>unless otherwise specified | Group A<br>subgroups | Device<br>type               | Limits |     | Unit |
|---|------------------|---|----------------------|------------------------------|--------|-----|------|
|   |                  |   |                      |                              | Min    | Max |      |
| Asynchronous reset pulse<br>width                   | t <sub>PWR</sub> | V <sub>CC</sub> = 4.5 V, see figures<br>3 and 4 <u>5/</u>   | 9, 10, 11            | 01                           | 30     |     | ns   |
|   |                  |   |                      | 02, 14                       | 20     |     |      |
|   |                  |   |                      | 03, 05,<br>08, 09,<br>11, 15 | 15     |     |      |
|   |                  |   |                      | 04, 07,<br>10, 13            | 25     |     |      |
|   |                  |   |                      | 06, 12,<br>16                | 10     |     |      |
| Asynchronous reset to<br>rising clock recovery time | t <sub>REC</sub> |   | 9, 10, 11            | 01                           | 30     |     | ns   |
|   |                  |   |                      | 02, 14                       | 20     |     |      |
|   |                  |   |                      | 03, 05                       | 15     |     |      |
|   |                  |   |                      | 08, 09,<br>11, 15            | 12     |     |      |
|   |                  |   |                      | 04, 07,<br>10, 13            | 25     |     |      |
| Clock pulse width<br><u>6/</u> <u>8/</u>            | t <sub>w</sub>   | See figure 5  | 9, 10, 11            | 01, 07                       | 20     |     | ns   |
|   |                  |   |                      | 04, 10,<br>13                | 15     |     |      |
|   |                  |   |                      | 02, 08,<br>14                | 15     |     |      |
|   |                  |   |                      | 03, 05,<br>09, 11,<br>15     | 8      |     |      |
|   |                  |   |                      | 06, 12,<br>16                | 3.5    |     |      |
| Setup time<br><u>6/</u> <u>8/</u>                   | t <sub>s</sub>   |   | 9, 10, 11            | 01, 07                       | 25     |     | ns   |
|   |                  |   |                      | 04, 10,<br>13                | 18     |     |      |
|   |                  |   |                      | 02, 08,<br>14                | 17     |     |      |
|   |                  |   |                      | 03, 05,<br>09, 11,<br>15     | 12     |     |      |
|   |                  |   |                      | 06, 12,<br>16                | 6      |     |      |
| Power up reset time <u>8/</u>                       | t <sub>PR</sub>  |   | 9, 10, 11            | All                          |        | 1.0 | μs   |

See footnotes at end of table.

|   |                  |                     |                   |
|---|------------------|---------------------|-------------------|
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|   |                  | REVISION LEVEL<br>L | SHEET<br>8        |



Table I. Electrical performance characteristics - Continued.

- 1/ The maximum leakage current is due to the internal pull-up resistor on all pins.
- 2/ See figure 6 for the I/V curve for ppk (bus friendly pin keeper).
- 3/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
- 4/ Not more than one output at a time should be shorted. Short circuit test duration should not exceed 1 second (see 4.3.1d).
- 5/ AC tests are performed with input rise and fall times (10 percent to 90 percent) of 3.0 ns, timing reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V and the output load of figure 3. Input pulse levels are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
- 6/ Test applies only to registered outputs.
- 7/ Transition is measured at steady-state high level -500 mV or steady-state low level +500 mV on the output from the 1.5 V level on the input.
- 8/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.

TABLE II. Electrical test requirements.

|  |   |
|--|---|
| MIL-STD-883 test requirements                                      | Subgroups<br>(in accordance with<br>MIL-STD-883, method 5005,<br>table I) |
| Interim electrical parameters<br>(method 5004)                     | ---   |
| Final electrical test parameters<br>(method 5004)                  | 1*, 2,3, 7*, 8A,<br>8B, 9, 10, 11   |
| Group A test requirements<br>(method 5005)                         | 1, 2,3, 4**, 7, 8A,<br>8B, 9, 10, 11                                      |
| Groups C and D end-point<br>Electrical parameters<br>(method 5005) | 2, 3, 7, 8A, 8B   |

\* PDA applies to subgroups 1 and 7

\*\* See 4.3.1c

|   |                  |                     |                   |
|---|------------------|---------------------|-------------------|
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|   |                  | REVISION LEVEL<br>L | SHEET<br>9        |

| Device Types    | All Devices     |                 |
|-----------------|-----------------|-----------------|
| Case outlines   | K and L         | 3               |
| Terminal number | Terminal symbol |                 |
| 1               | I/CLK           | NC              |
| 2               | I               | I/CLK           |
| 3               | I               | I               |
| 4               | I               | I               |
| 5               | I               | I               |
| 6               | I               | I               |
| 7               | I               | I               |
| 8               | I               | NC              |
| 9               | I               | I               |
| 10              | I               | I               |
| 11              | I               | I               |
| 12              | GND             | I               |
| 13              | I               | I               |
| 14              | I/O/Q           | GND             |
| 15              | I/O/Q           | NC              |
| 16              | I/O/Q           | I               |
| 17              | I/O/Q           | I/O/Q           |
| 18              | I/O/Q           | I/O/Q           |
| 19              | I/O/Q           | I/O/Q           |
| 20              | I/O/Q           | I/O/Q           |
| 21              | I/O/Q           | I/O/Q           |
| 22              | I/O/Q           | NC              |
| 23              | I/O/Q           | I/O/Q           |
| 24              | V <sub>CC</sub> | I/O/Q           |
| 25              | ---             | I/O/Q           |
| 26              | ---             | I/O/Q           |
| 27              | ---             | I/O/Q           |
| 28              | ---             | V <sub>CC</sub> |

FIGURE 1. Terminal connections.

|   |                  |                     |                   |
|---|------------------|---------------------|-------------------|
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|   |                  | REVISION LEVEL<br>L | SHEET<br>10       |

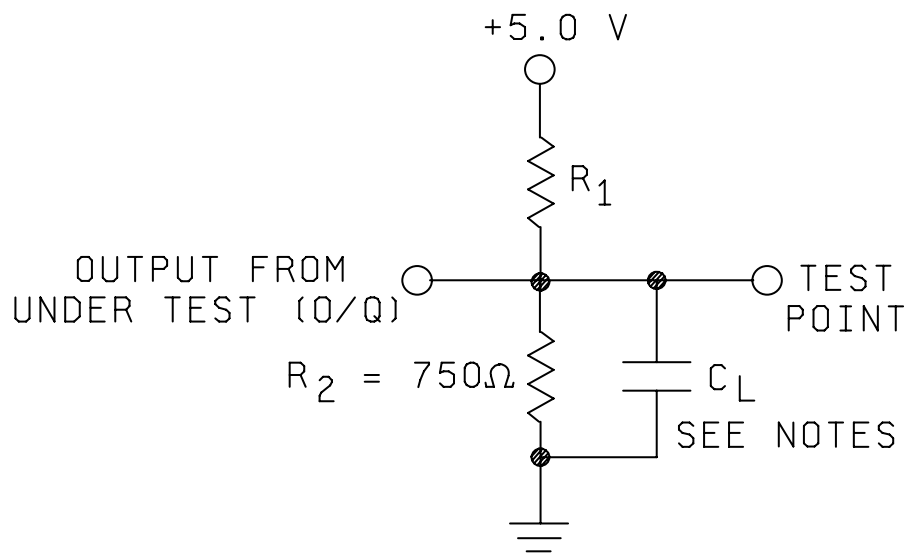
| Inputs |   |   |   |   |   |   |   |   |   |   |   |
|--------|---|---|---|---|---|---|---|---|---|---|---|
| I/CLK  | I | I | I | I | I | I | I | I | I | I | I |
| X      | X | X | X | X | X | X | X | X | X | X | X |

| Outputs |       |       |       |       |       |       |       |       |       |       |       |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| I/O/Q   | I/O/Q | I/O/Q | I/O/Q | I/O/Q | I/O/Q | I/O/Q | I/O/Q | I/O/Q | I/O/Q | I/O/Q | I/O/Q |
| Z       | Z     | Z     | Z     | Z     | Z     | Z     | Z     | Z     | Z     | Z     | Z     |

X = don't care state  
Z = high impedance state

FIGURE 2. Truth table (unprogrammed).

|  |                         |                                   |                           |
|--|-------------------------|-----------------------------------|---------------------------|
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|  |                         | <b>REVISION LEVEL</b><br><b>L</b> | <b>SHEET</b><br><b>11</b> |



| Test   | $R_1$   | $C_L$<br>(minimum) |
|--|---|--------------------|
| $t_{PD}$ , $t_{CO}$ , $t_{RES}$ ,<br>$f_{CLK1}$ , $f_{CLK2}$ | 390 $\Omega$  | 50 pF              |
| $t_{EA}$   | Active high = infinity<br>Active low = 390 $\Omega$ | 50 pF              |
| $t_{ER}$   | Active high = infinity<br>Active low = 390 $\Omega$ | 5 pF               |

NOTES:

1.  $C_L$  = load capacitance and includes jig and probe capacitance.
2. A different output load circuit may be utilized, but table I electricals shall be guaranteed with figure 3 output load circuit.

FIGURE 3. Output load circuit.

|   |                  |                     |                   |
|---|------------------|---------------------|-------------------|
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|   |                  | REVISION LEVEL<br>L | SHEET<br>12       |

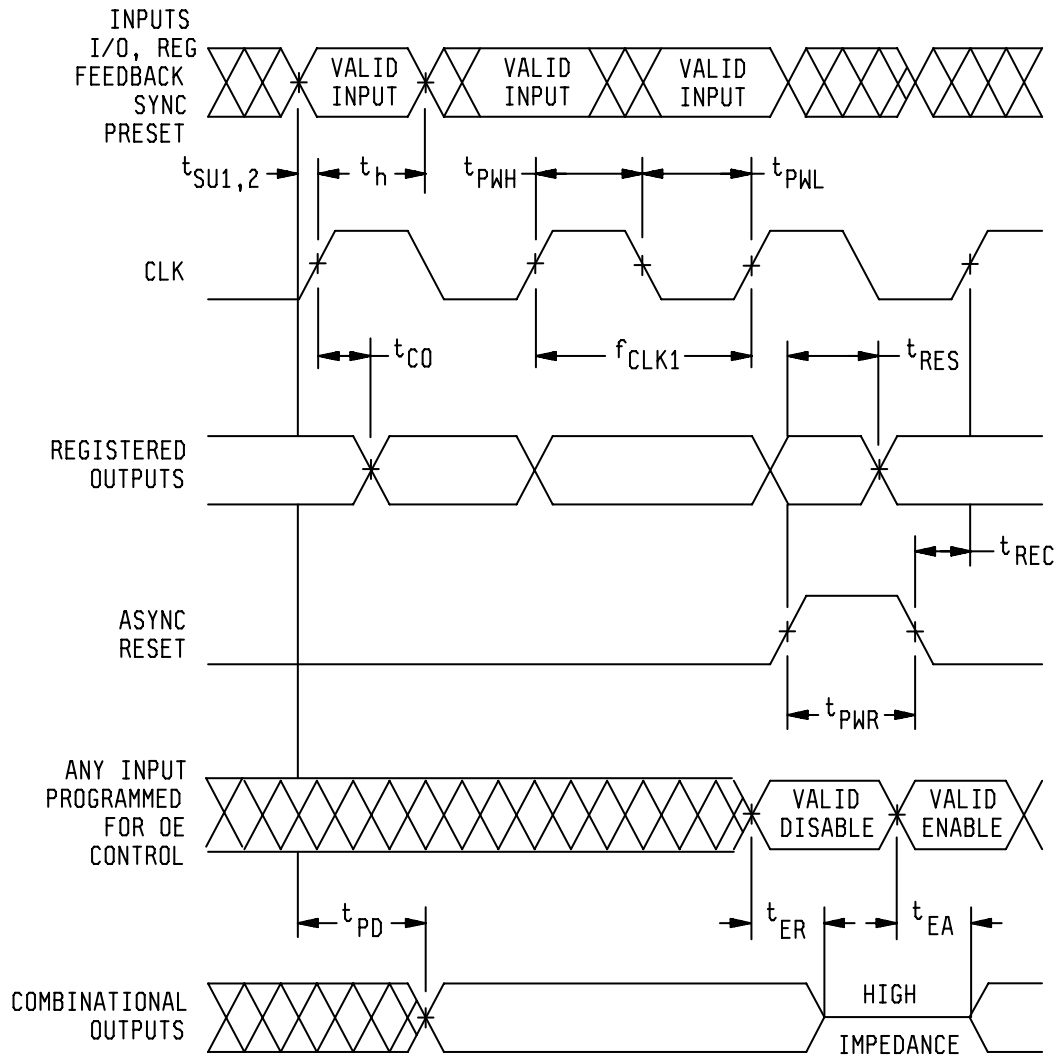
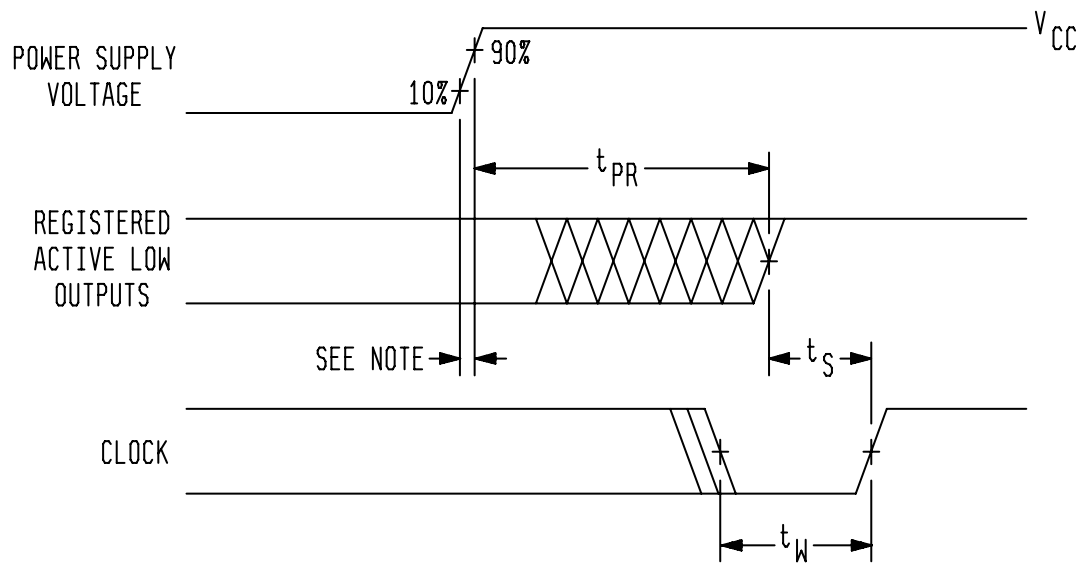


FIGURE 4. Switching waveforms.

|   |                  |                     |                   |
|---|------------------|---------------------|-------------------|
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|   |                  | REVISION LEVEL<br>L | SHEET<br>13       |



Note: The power-up reset feature ensures that all flip-flops will be reset to low after the device has been powered up. The following conditions are required:

- The  $V_{CC}$  rise must be monotonic.
- After reset occurs, all applicable input and feedback setup times must be met before driving the clock pin high.
- The clock signal must remain stable beginning prior to the occurrence of the 10% level and continuing until the end of  $t_{PR}$ .

FIGURE 5. Power-up Reset waveform.

|   |                  |                     |                   |
|---|------------------|---------------------|-------------------|
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|   |                  | REVISION LEVEL<br>L | SHEET<br>14       |

For devices 15 and 16 only.

22V10 INPUT CURRENT VS INPUT VOLTAGE  
( $V_{CC}=5\text{ V}$ ,  $T=25\text{C}$ )

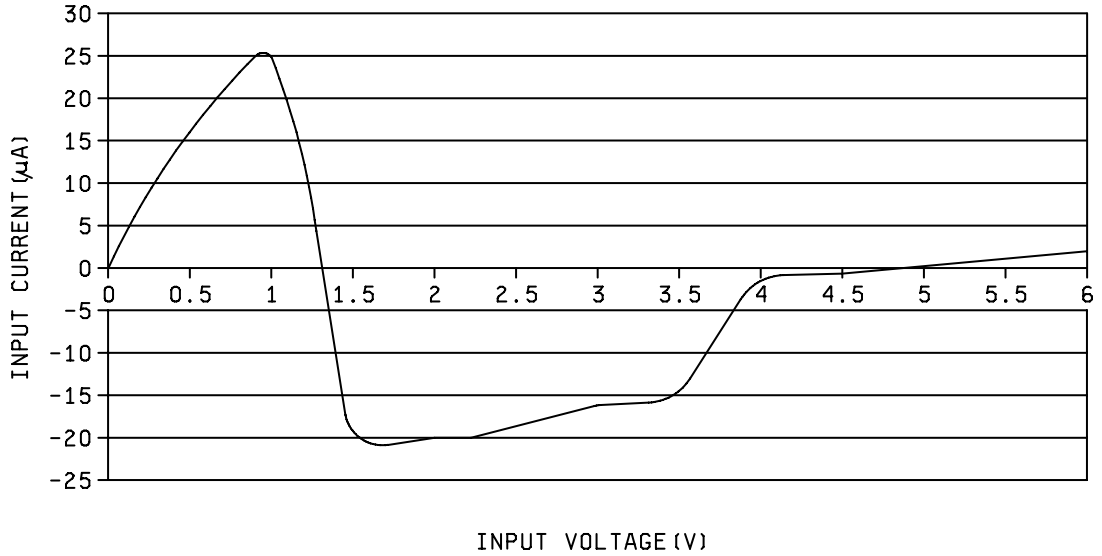


FIGURE 6. IV Curve.

|   |                         |                            |                    |
|---|-------------------------|----------------------------|--------------------|
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|   |                         | <b>REVISION LEVEL</b><br>L | <b>SHEET</b><br>15 |

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

#### 4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

- (1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- (2)  $T_A = +125^{\circ}\text{C}$ , minimum.
- (3) Devices shall be burned-in containing a pattern that assures all inputs and I/O's are dynamically switched. This pattern must have all cells programmed in a high or low state (not neutralized).
- (4) The burn-in pattern shall be read before and after burn-in. Devices having any logic array bits not in the proper state shall constitute a device failure and shall be added as failures for PDA calculation.

b. Interim and final electrical parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

|   |                  |                     |                   |
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| <b>STANDARD<br/>MICROCIRCUIT DRAWING</b><br><br><b>DEFENSE SUPPLY CENTER COLUMBUS</b><br><b>COLUMBUS, OHIO 43218-3990</b> | SIZE<br><b>A</b> |                     | <b>5962-89841</b> |
|   |                  | REVISION LEVEL<br>L | SHEET<br>16       |



c. An endurance/retention test prior to burn-in (may be performed at wafer level), in accordance with method 1033 of MIL-STD-883, shall be included as part of the screening procedure with the following conditions:

- (1) Cycling may be at equipment room ambient temperature and shall cycle all bit locations for a minimum of 100 cycles. After cycling, devices containing bits which fail to verify shall be considered device failures.
- (2) The retention pattern must have a minimum of 50 percent of the logic array programmed.
- (3) After cycling, perform a high temperature unbiased bake for a minimum of 48 hours at +150°C. The bake time may be accelerated by using higher temperature in accordance with the Arrhenius Relationship:

$$A_F = e^{-\frac{E_A}{K} \left[ \frac{1}{T_1} - \frac{1}{T_2} \right]}$$

$A_F$  = Acceleration factor (unit less quantity) =  $t_1/t_2$ .

$T$  = Temperature in Kelvin (i.e., °C + 273 = K).

$t_1$  = Time (hrs) at temperature  $T_1$ .

$t_2$  = Time (hrs) at temperature  $T_2$ .

$K$  = Boltzmann's constant =  $8.62 \times 10^{-5}$  eV/°K using an apparent activation energy ( $E_A$ ) of 0.6 eV.

The maximum bake temperature shall not exceed +250°C.

- (4) After cycling and bake, and prior to burn-in, read the data retention pattern. Test using subgroups 1 and 7 (at the manufacturer's option, high temperature equivalent subgroups 2 and 8A or low temperature equivalent subgroups 3 and 8B may be used in lieu of subgroups 1 and 7). Devices having any logic array bits not in the proper state after storage shall constitute device failure.
- (5) At the manufacturer's option, the testing specified in 4.2c(4) may be deleted if the devices are put into burn-in with no reprogramming allowed between the start of data retention bake and the end of burn-in. Exercising this option will result in data retention bake failures being caught and included in post burn-in PDA calculations.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 ( $C_{IN}$  and  $C_{I/O/Q}$  measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.
- d.  $I_{OS}$  measurements in subgroup 1 shall be measured only for the initial test and after process or design changes which may affect  $I_{OS}$ . Sample size is 15 devices with no failures, and all output terminals tested.
- e. Subgroups 7, 8A, and 8B shall be sufficient to verify the truth table.

|   |                   |                     |                   |
|---|-------------------|---------------------|-------------------|
| <b>STANDARD<br/>MICROCIRCUIT DRAWING<br/>DEFENSE SUPPLY CENTER COLUMBUS<br/>COLUMBUS, OHIO 43218-3990</b> | <b>SIZE<br/>A</b> |                     | <b>5962-89841</b> |
|   |                   | REVISION LEVEL<br>L | SHEET<br>17       |

4.3.2 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
  - (1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
  - (2) TA = +125°C, minimum.
  - (3) Test duration: 1,000 hours except as permitted by method 1005 of MIL-STD-883.
  - (4) All devices shall be programmed with a pattern that assures all inputs and I/O's are dynamically switched.
- c. An extended data retention test shall be added. A new sample shall be selected, and the sample size, accept number and frequency of testing shall be the same as that required for group C inspection. Extended data retention shall also consist of the following:
  - (1) All devices shall have a minimum of 50 percent of the logic array programmed with a charge on all cells, such that the cell will not be in a neutral state.
  - (2) Unbiased bake for 1,000 hours (minimum) at +150°C (minimum). The unbiased bake time may be accelerated by using a higher temperature in accordance with the Arrhenius Relationship:

$$A_F = e^{-\frac{E_A}{K} \left[ \frac{1}{T_1} - \frac{1}{T_2} \right]}$$

A<sub>F</sub> = Acceleration factor (unitless quantity) = t<sub>1</sub>/t<sub>2</sub>.  
 T = Temperature in Kelvin (i.e., °C + 273 = K).  
 t<sub>1</sub> = Time (hrs) at temperature T<sub>1</sub>.  
 t<sub>2</sub> = Time (hrs) at temperature T<sub>2</sub>.  
 K = Boltzmann's constant = 8.62 x 10<sup>-5</sup> eV/°K using an apparent activation energy (EA) of 0.6 eV.

The maximum bake temperature shall not exceed +200°C.

- (3) Read the pattern after bake and perform end-point electrical tests in accordance with table II herein for group C.

4.3.3 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical parameters shall be as specified in table II herein.

4.4 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available to the user on request.

4.5 Erasing procedures. The erasing procedures shall be as specified by the device manufacturer and shall be made available to the user on request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

|   |                  |                     |                   |
|---|------------------|---------------------|-------------------|
| <b>STANDARD<br/>MICROCIRCUIT DRAWING<br/>DEFENSE SUPPLY CENTER COLUMBUS<br/>COLUMBUS, OHIO 43218-3990</b> | SIZE<br><b>A</b> |                     | <b>5962-89841</b> |
|   |                  | REVISION LEVEL<br>L | SHEET<br>18       |

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

|   |                   |                             |                     |
|---|-------------------|-----------------------------|---------------------|
| <b>STANDARD<br/>MICROCIRCUIT DRAWING<br/>DEFENSE SUPPLY CENTER COLUMBUS<br/>COLUMBUS, OHIO 43218-3990</b> | <b>SIZE<br/>A</b> |                             | <b>5962-89841</b>   |
|   |                   | <b>REVISION LEVEL<br/>L</b> | <b>SHEET<br/>19</b> |

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 25 AUG 2008

Approved sources of supply for SMD 5962-89841 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at <http://www.dscclia.mil/Programs/Smcr/>.

| Standard microcircuit drawing<br>PIN <u>1</u> / | Vendor<br>CAGE<br>number                                     | Vendor<br>similar<br>PIN <u>2</u> /   |
|---|--|---|
| 5962-8984101LA                                  | 0C7V7<br>0C7V7<br><u>3</u> /<br>66675<br>66675<br><u>3</u> / | PALC22V10D-30DMB<br>PALCE22V10-30DMB<br>PALCE22V10H-30E4/BLA<br>GAL22V10C-30LD/883C<br>GAL22V10D-30LD/883C<br>QPC22V10-30/BLA |
| 5962-8984101KA                                  | 0C7V7<br>0C7V7<br><u>3</u> /<br>0C7V7                        | PALC22V10D-30KMB<br>PALCE22V10-30KMB<br>PALCE22V10H-30E4/BKA<br>QPC22V10-30/BKA   |
| 5962-89841013A                                  | 0C7V7<br>0C7V7<br><u>3</u> /<br><u>3</u> /                   | PALC22V10D-30LMB<br>PALCE22V10-30LMB<br>PALCE22V10H-30E4/B3A<br>QPC22V10-30/B3A   |
| 5962-8984102LA                                  | 0C7V7<br>0C7V7<br><u>3</u> /<br>66675<br>66675<br><u>3</u> / | PALC22V10D-20DMB<br>PALCE22V10-20DMB<br>PALCE22V10H-20E4/BLA<br>GAL22V10C-20LD/883C<br>GAL22V10D-20LD/883C<br>QPC22V10-20/BLA |
| 5962-8984102KA                                  | 0C7V7<br>0C7V7<br>0C7V7<br><u>3</u> /                        | PALC22V10D-20KMB<br>PALCE22V10-20KMB<br>QPC22V10-20/BKA<br>PALCE22V10H-20E4/BKA   |
| 5962-89841023A                                  | 66675<br>66675<br>0C7V7<br>0C7V7<br><u>3</u> /<br><u>3</u> / | GAL22V10C-20LR/883C<br>GAL22V10D-20LR/883C<br>PALC22V10D-20LMB<br>PALCE22V10-20LMB<br>PALCE22V10H-20E4/B3A<br>QPC22V10-20/B3A |
| 5962-8984103LA                                  | 66675<br>66675<br>0C7V7<br>0C7V7<br>1FN41                    | GAL22V10C-15LD/883C<br>GAL22V10D-15LD/883C<br>PALC22V10D-15DMB<br>PALCE22V10-15DMB<br>ATF22V10B-15GM/883                      |
| 5962-8984103LC                                  | 6S055  | DPA22V10-15LC   |
| 5962-8984103KA                                  | 0C7V7<br>0C7V7<br>0C7V7                                      | PALC22V10D-15KMB<br>PALCE22V10-15KMB<br>QPC22V10-15/BKA   |

See footnote at end of table.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN – Continued.

| Standard microcircuit drawing<br>PIN 1/ | Vendor<br>CAGE<br>number  | Vendor<br>similar<br>PIN 2/   |
|---|---|---|
| 5962-89841033A                          | 66675<br>66675<br>0C7V7<br>0C7V7<br>1FN41                               | GAL22V10C-15LR/883C<br>GAL22V10D-15LR/883C<br>PALC22V10D-15LMB<br>PALCE22V10-15LMB<br>ATF22V10B-15NM/883  |
| 5962-8984104LA                          | 0C7V7<br>0C7V7<br><u>3/</u><br>66675<br>66675<br><u>3/</u><br><u>3/</u> | PALC22V10D-25DMB<br>PALCE22V10-25DMB<br>ATF22V10B-25GM/883<br>GAL22V10C-25LD/883C<br>GAL22V10D-25LD/883C<br>PALCE22V10H-25E4/BLA<br>QPC22V10-25/BLA |
| 5962-8984104KA                          | 0C7V7<br>0C7V7<br><u>3/</u><br>0C7V7                                    | PALC22V10D-25KMB<br>PALCE22V10-25KMB<br>PALCE22V10H-25E4/BKA<br>QPC22V10-25/BKA   |
| 5962-89841043A                          | 0C7V7<br>0C7V7<br><u>3/</u><br><u>3/</u>                                | PALC22V10D-25LMB<br>PALCE22V10-25LMB<br>ATF22V10B-25NM/883<br>PALCE22V10H-25E4/B3A  |
| 5962-8984105LA                          | 0C7V7<br>0C7V7<br>1FN41<br><u>3/</u><br><u>3/</u>                       | PALC22V10D-15DMB<br>PALCE22V10-15DMB<br>ATF22V10B-15GM/883<br>PALCE22V10H-15E4/BLA<br>QPC22V10-15/BLA   |
| 5962-8984105KA                          | 0C7V7<br>0C7V7<br><u>3/</u><br>0C7V7                                    | PALC22V10D-15KMB<br>PALCE22V10-15KMB<br>PALCE22V10H-15E4/BKA<br>QPC22V10-15/BKA   |
| 5962-89841053A                          | 0C7V7<br>0C7V7<br>1FN41<br><u>3/</u>                                    | PALC22V10D-15LMB<br>PALCE22V10-15LMB<br>ATF22V10B-15NM/883<br>PALCE22V10H-15E4/B3A  |
| 5962-8984106LA                          | 0C7V7<br>0C7V7<br>66675<br>66675<br>1FN41                               | PALC22V10D-10DMB<br>PALCE22V10-10DMB<br>GAL22V10C-10LD/883C<br>GAL22V10D-10LD/883C<br>ATF22V10B-10GM/883  |
| 5962-8984106KA                          | 0C7V7<br>0C7V7<br>0C7V7   | PALC22V10D-10KMB<br>PALCE22V10-10KMB<br>QPC22V10-10/BKA   |
| 5962-89841063A                          | 0C7V7<br>0C7V7<br>66675<br>66675<br>1FN41                               | PALC22V10D-10LMB<br>PALCE22V10-10LMB<br>GAL22V10C-10LR/883C<br>GAL22V10D-10LR/883C<br>ATF22V10B-10NM/883  |

See footnote at end of table.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN – Continued.

| Standard microcircuit drawing<br>PIN <u>1</u> / | Vendor<br>CAGE<br>number                       | Vendor<br>similar<br>PIN <u>2</u> /   |
|---|--|---|
| 5962-8984107LA                                  | 0C7V7<br>0C7V7<br><u>3</u> /                   | PALC22V10D-30DMB<br>PALCE22V10-30DMB<br>QPC22V10-30/BLA   |
| 5962-8984107KA                                  | 0C7V7<br>0C7V7<br><u>3</u> /                   | PALC22V10D-30KMB<br>PALCE22V10-30KMB<br>QPC22V10-30/BKA   |
| 5962-89841073A                                  | 0C7V7<br>0C7V7<br><u>3</u> /                   | PALC22V10D-30LMB<br>PALCE22V10-30LMB<br>QPC22V10-30/B3A   |
| 5962-8984108LA                                  | 65786<br>65786<br><u>3</u> /<br>0C7V7<br>0C7V7 | PALC22V10D-20DMB<br>PALCE22V10-20DMB<br>QPC22V10-20/BLA<br>PALCE22V10-20DMB<br>PALC22V10D-20DMB |
| 5962-8984108KA                                  | 65786<br>65786<br>0C7V7<br>0C7V7<br><u>3</u> / | PALC22V10D-20KMB<br>PALCE22V10-20KMB<br>PALCE22V10-20KMB<br>PALC22V10D-20KMB<br>QPC22V10-20/BKA |
| 5962-89841083A                                  | 65786<br>65786<br>0C7V7<br>0C7V7<br><u>3</u> / | PALC22V10D-20LMB<br>PALCE22V10-20LMB<br>PALCE22V10-20LMB<br>PALC22V10D-20LMB<br>QPC22V10-20/B3A |
| 5962-8984109LA                                  | 0C7V7<br>0C7V7<br><u>3</u> /                   | PALC22V10D-15DMB<br>PALCE22V10-15DMB<br>QPC22V10-15/BLA   |
| 5962-8984109KA                                  | 0C7V7<br>0C7V7<br><u>3</u> /                   | PALC22V10D-15KMB<br>PALCE22V10-15KMB<br>QPC22V10-15/BKA   |
| 5962-89841093A                                  | 0C7V7<br>0C7V7<br><u>3</u> /                   | PALC22V10D-15LMB<br>PALCE22V10-15LMB<br>QPC22V10-15/B3A   |
| 5962-8984110LA                                  | 65786<br>65786<br>0C7V7<br>0C7V7<br><u>3</u> / | PALC22V10D-25DMB<br>PALCE22V10-25DMB<br>PALCE22V10-25DMB<br>PALC22V10D-25DMB<br>QPC22V10-25/BLA |
| 5962-8984110KA                                  | 65786<br>65786<br>0C7V7<br>0C7V7<br><u>3</u> / | PALC22V10D-25KMB<br>PALCE22V10-25KMB<br>PALCE22V10-25KMB<br>PALC22V10D-25KMB<br>QPC22V10-25/BKA |
| 5962-89841103A                                  | 65786<br>65786<br>0C7V7<br>0C7V7<br><u>3</u> / | PALC22V10D-25LMB<br>PALCE22V10-25LMB<br>PALCE22V10-25LMB<br>PALC22V10D-25LMB<br>QPC22V10-25/B3A |
| 5962-8984111LA                                  | 0C7V7<br>0C7V7<br><u>3</u> /                   | PALC22V10D-15DMB<br>PALCE22V10-15DMB<br>QPC22V10-15/BLA   |

See footnote at end of table.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN – Continued.

| Standard microcircuit drawing<br>PIN <u>1/</u> | Vendor<br>CAGE<br>number    | Vendor<br>similar<br>PIN <u>2/</u>                      |
|--|-----------------------------|---|
| 5962-8984111KA                                 | 0C7V7<br>0C7V7<br><u>3/</u> | PALC22V10D-15KMB<br>PALCE22V10-15KMB<br>QPC22V10-15/BKA |
| 5962-89841113A                                 | 0C7V7<br>0C7V7<br><u>3/</u> | PALC22V10D-15LMB<br>PALCE22V10-15LMB<br>QPC22V10-15/B3A |
| 5962-8984112LA                                 | 0C7V7<br>0C7V7<br><u>3/</u> | PALC22V10D-10DMB<br>PALCE22V10-10DMB<br>QPC22V10-10/BLA |
| 5962-8984112KA                                 | 0C7V7<br>0C7V7<br><u>3/</u> | PALC22V10D-10KMB<br>PALCE22V10-10KMB<br>QPC22V10-10/BKA |
| 5962-89841123A                                 | 0C7V7<br>0C7V7<br><u>3/</u> | PALC22V10D-10LMB<br>PALCE22V10-10LMB<br>QPC22V10-10/B3A |
| 5962-8984113LA                                 | <u>3/</u>                   | ATF22V10BQL-25GM/883                                    |
| 5962-89841133A                                 | <u>3/</u>                   | ATF22V10BQL-25NM/883                                    |
| 5962-8984114LA                                 | <u>3/</u>                   | ATF22V10BQL-20GM/883                                    |
| 5962-89841143A                                 | <u>3/</u>                   | ATF22V10BQL-20NM/883                                    |
| 5962-8984115LA                                 | 1FN41                       | ATF22V10C-15GM/883                                      |
| 5962-89841153A                                 | 1FN41                       | ATF22V10C-15NM/883                                      |
| 5962-8984116LA                                 | 1FN41                       | ATF22V10C-10GM/883                                      |
| 5962-89841163A                                 | 1FN41                       | ATF22V10C-10NM/883                                      |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ **Caution.** Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ No longer available from an approved source of supply.

| <u>Vendor CAGE<br/>number</u> | <u>Vendor name<br/>and address</u>   |
|-------------------------------|--|
| 66675                         | Lattice Semiconductor Corporation<br>5555 NE Moore Court<br>Hillsboro, OR 97124-6421 |
| 65786                         | Cypress Semiconductor Corporation<br>3901 North First Street<br>San Jose, CA 95134   |
| 1FN41                         | Atmel Corporation<br>2325 Orchard Parkway<br>San Jose, CA 95131                      |
| 6S055                         | DPA Laboratories<br>2251 Ward Ave.<br>Simi Valley, CA 93065                          |
| 0C7V7                         | QP Semiconductor<br>2945 Oakmead Village Court<br>Santa Clara, CA 95051              |

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