

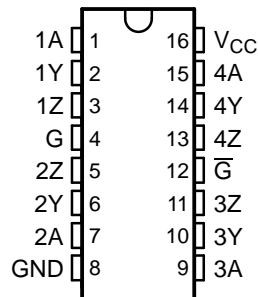
FEATURES

- Meets or Exceeds the Requirements of ANSI TIA/EIA-422-B and ITU
- Operates From a Single 5-V Supply
- TTL Compatible
- Complementary Outputs
- High Output Impedance in Power-Off Conditions
- Complementary Output-Enable Inputs

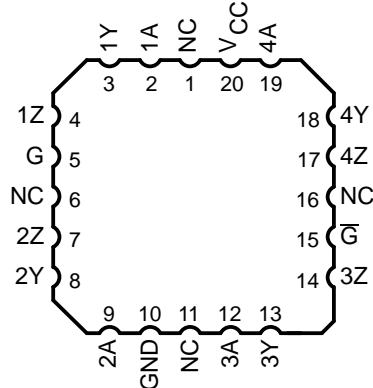
DESCRIPTION/ORDERING INFORMATION

The AM26LS31 is a quadruple complementary-output line driver designed to meet the requirements of ANSI TIA/EIA-422-B and ITU (formerly CCITT) Recommendation V.11. The 3-state outputs have high-current capability for driving balanced lines such as twisted-pair or parallel-wire transmission lines, and they are in the high-impedance state in the power-off condition. The enable function is common to all four drivers and offers the choice of an active-high or active-low enable (G, \bar{G}) input. Low-power Schottky circuitry reduces power consumption without sacrificing speed.

D, DB, N, NS, J, OR W PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

| T _A | PACKAGE (1) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|---------------|---------------|-----------------------|------------------|
| 0°C to 70°C | PDIP – N | Tube | AM26LS31CN | AM26LS31CN |
| | SOIC – D | Tube | AM26LS31CD | AM26LS31C |
| | | Tape and reel | AM26LS31CDR | |
| | SOP – NS | Tape and reel | AM26LS31CNSR | 26LS31 |
| SSOP – DB | Tape and reel | AM26LS31CDBR | SA31C | |
| –55°C to 125°C | CDIP – J | Tube | AM26LS31MJB | AM26LS31MJB |
| | LCCC – FK | Tube | AM26LS31MFKB | AM26LS31MFKB |
| | CFP – W | Tube | AM26LS31MWB | AM26LS31MWB |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



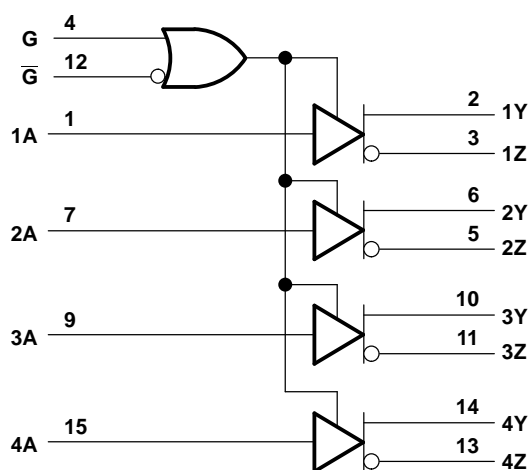
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FUNCTION TABLE⁽¹⁾
 (EACH DRIVER)

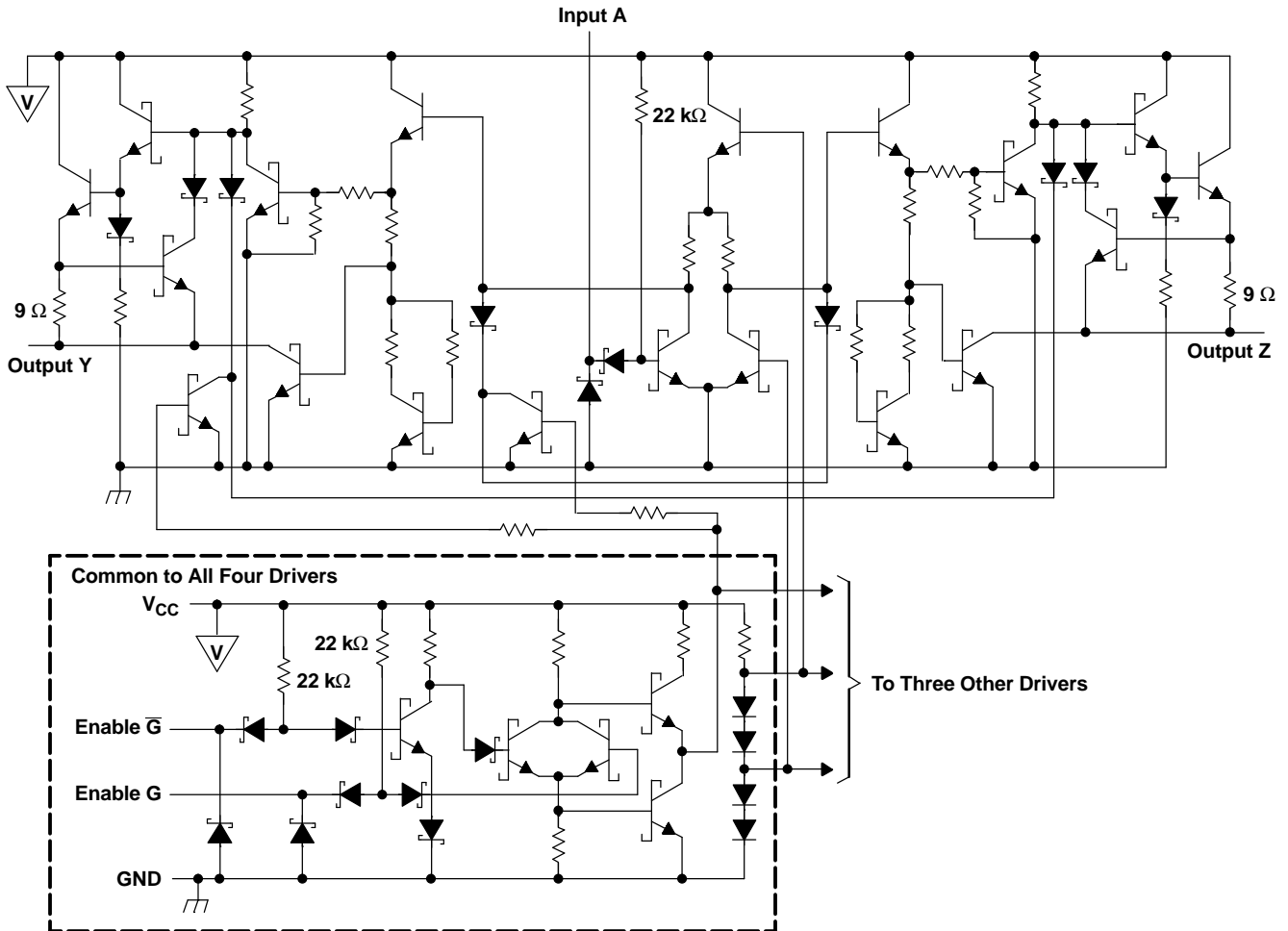
| INPUT A | ENABLES | | OUTPUTS | |
|------------|---------|-----------|---------|---|
| | G | \bar{G} | Y | Z |
| H | H | X | H | L |
| L | H | X | L | H |
| H | X | L | H | L |
| L | X | L | L | H |
| X | L | H | Z | Z |

(1) H = high level, L = low level,
 X = irrelevant,
 Z = high impedance (off)

LOGIC DIAGRAM (POSITIVE LOGIC)



SCHEMATIC (EACH DRIVER)



All resistor values are nominal.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------|--|------------|-----|------|
| V_{CC} | Supply voltage ⁽²⁾ | | 7 | V |
| V_I | Input voltage | | 7 | V |
| | Output off-state voltage | | 5.5 | V |
| θ_{JA} | Package thermal impedance ⁽³⁾ | D package | 73 | °C/W |
| | | DB package | 82 | |
| | | N package | 67 | |
| | | NS package | 64 | |
| | Lead temperature 1,6 mm (1/16 in) from case for 10 s | | 260 | °C |
| | Lead temperature 1,6 mm (1/16 in) from case for 60 s | J package | 300 | °C |
| T_{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential output voltage V_{OD} , are with respect to network GND.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

AM26LS31C, AM26LS31M QUADRUPLE DIFFERENTIAL LINE DRIVER

SLLS114I–JANUARY 1979–REVISED FEBRUARY 2006

Recommended Operating Conditions

| | | | MIN | NOM | MAX | UNIT |
|-----------------|--------------------------------|-----------|------|-----|------|------|
| V _{CC} | Supply voltage | AM26LS31C | 4.75 | 5 | 5.25 | V |
| | | AM26LS31M | 4.5 | 5 | 5.5 | |
| V _{IH} | High-level input voltage | | 2 | | | V |
| V _{IL} | Low-level input voltage | | | | 0.8 | V |
| I _{OH} | High-level output current | | | | -20 | mA |
| I _{OL} | Low-level output current | | | | 20 | mA |
| T _A | Operating free-air temperature | AM26LS31C | 0 | | 70 | °C |
| | | AM26LS31M | -55 | | 125 | |

Electrical Characteristics⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP ⁽²⁾ | MAX | UNIT |
|-----------------|---|------------------------|--------------------|-------|------|
| V _{IK} | Input clamp voltage V _{CC} = MIN, I _I = -18 mA | | | -1.5 | V |
| V _{OH} | High-level output voltage V _{CC} = MIN, I _{OH} = -20 mA | 2.5 | | | V |
| V _{OL} | Low-level output voltage V _{CC} = MIN, I _{OL} = 20 mA | | | 0.5 | V |
| I _{OZ} | Off-state (high-impedance-state) output current V _{CC} = MIN, | | | -20 | μA |
| | | V _O = 0.5 V | | 20 | |
| I _I | Input current at maximum input voltage V _{CC} = MAX, V _I = 7 V | | | 0.1 | mA |
| I _{IH} | High-level input current V _{CC} = MAX, V _I = 2.7 V | | | 20 | μA |
| I _{IL} | Low-level input current V _{CC} = MAX, V _I = 0.4 V | | | -0.36 | mA |
| I _{OS} | Short-circuit output current ⁽³⁾ V _{CC} = MAX | -30 | | -150 | mA |
| I _{CC} | Supply current V _{CC} = MAX, All outputs disabled | | 32 | 80 | mA |

(1) For C-suffix devices, V_{CC} min = 4.75 V and V_{CC} max = 5.25 V. For M-suffix devices, V_{CC} min = 4.5 V and V_{CC} max = 5.5 V.

(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.

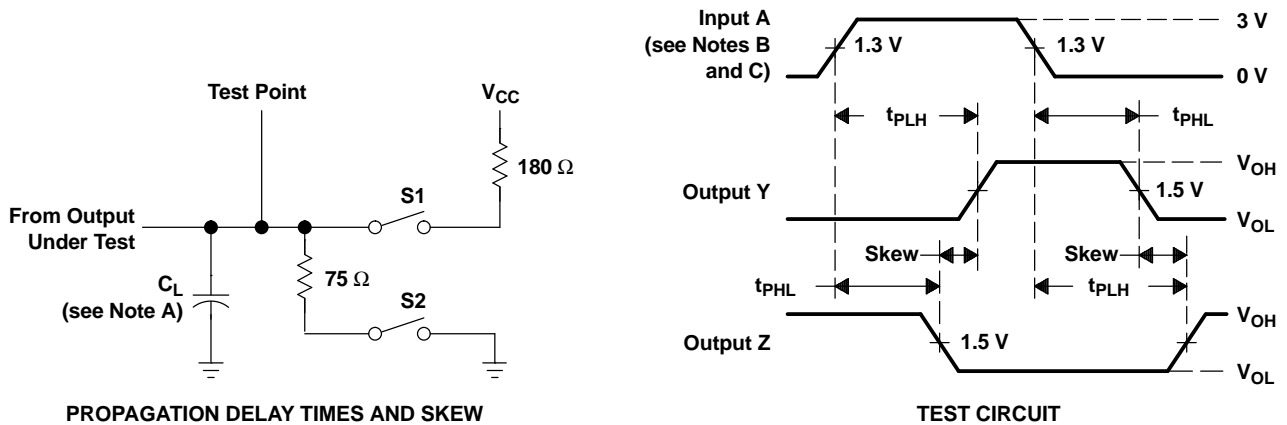
(3) Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

Switching Characteristics

V_{CC} = 5 V (see Figure 1)

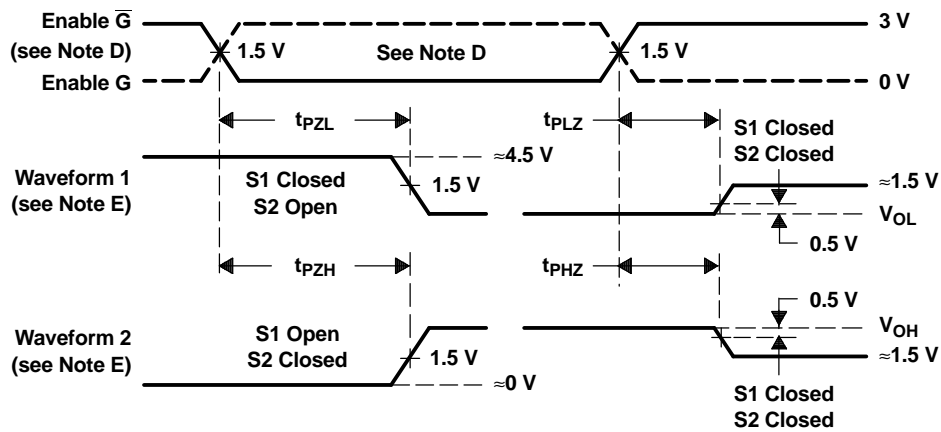
| PARAMETER | TEST CONDITIONS | T _A = 25°C | | | AM26LS31M | | UNIT |
|-------------------|---|--|------------------------|-----|-----------|-----|------|
| | | MIN | TYP | MAX | MIN | MAX | |
| t _{PLH} | Propagation delay time, low- to high-level output | C _L = 30 pF, S1 and S2 open | | 14 | 20 | | ns |
| t _{PHL} | Propagation delay time, high- to low-level output | | | 14 | 20 | 30 | |
| t _{PZH} | Output enable time to high level | C _L = 30 pF | R _L = 75 Ω | 25 | 40 | 60 | ns |
| t _{PZL} | Output enable time to low level | | R _L = 180 Ω | 37 | 45 | 68 | |
| t _{PHZ} | Output disable time from high level | C _L = 10 pF, S1 and S2 closed | | 21 | 30 | 45 | ns |
| t _{PLZ} | Output disable time from low level | | | 23 | 35 | 53 | |
| t _{SKEW} | Output-to-output skew | C _L = 30 pF, S1 and S2 open | | 1 | 6 | 9 | ns |

PARAMETER MEASUREMENT INFORMATION



PROPAGATION DELAY TIMES AND SKEW

TEST CIRCUIT



ENABLE AND DISABLE TIME WAVEFORMS

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O \approx 50 \Omega$, $t_r \leq 15$ ns, $t_f \leq 6$ ns.
 C. When measuring propagation delay times and skew, switches S1 and S2 are open.
 D. Each enable is tested separately.
 E. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

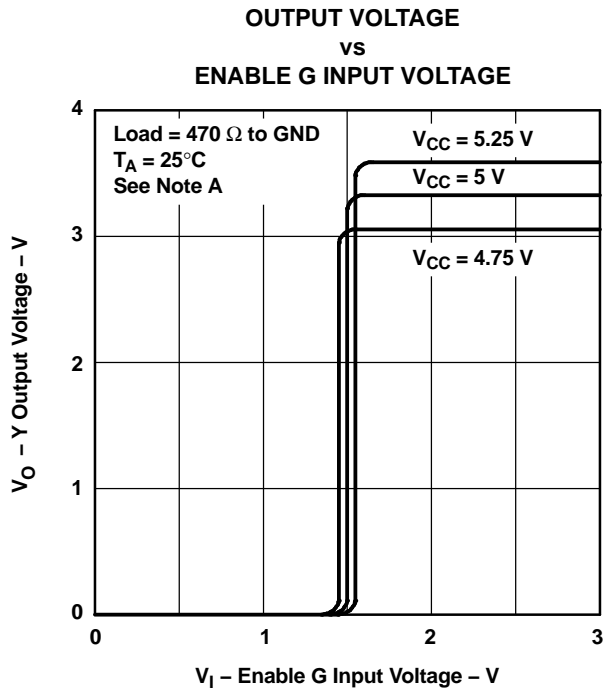


Figure 2.

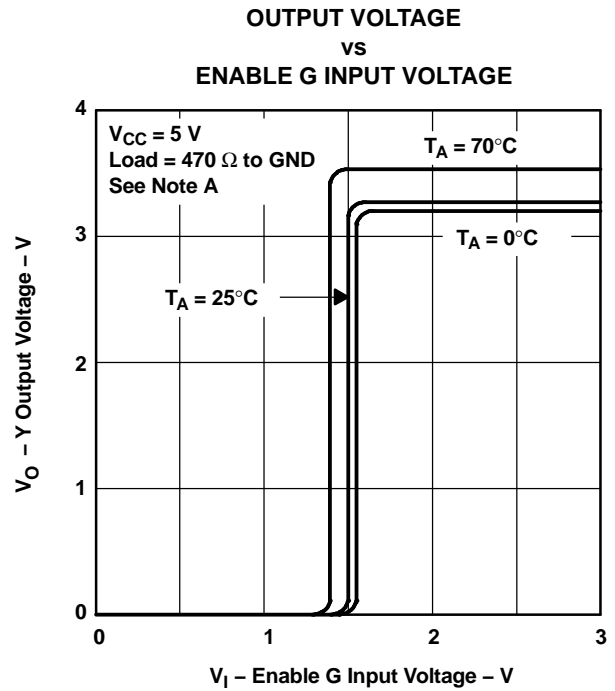


Figure 3.

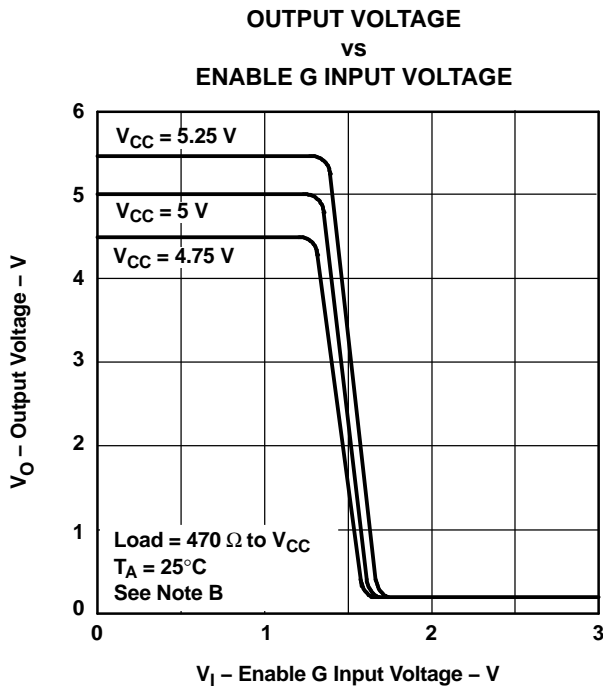


Figure 4.

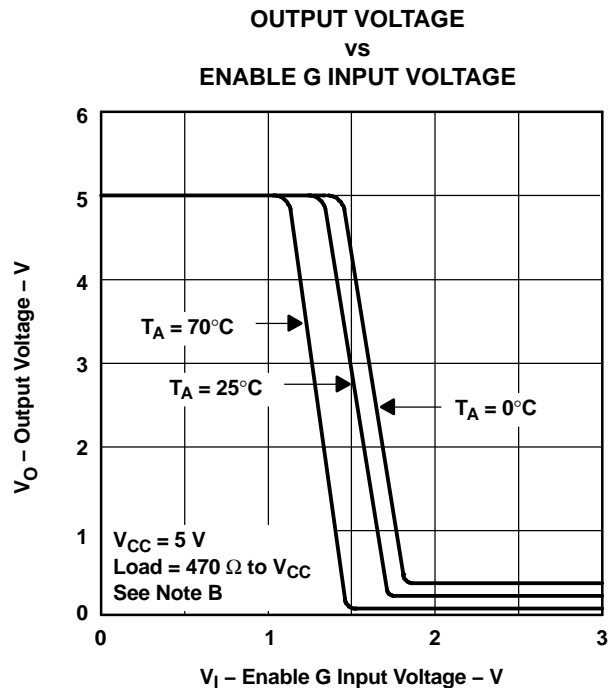


Figure 5.

- A. The A input is connected to V_{CC} during testing of the Y outputs and to ground during testing of the Z outputs.
- B. The A input is connected to ground during testing of the Y outputs and to V_{CC} during testing of the Z outputs.

TYPICAL CHARACTERISTICS (continued)



Figure 6.



Figure 7.



Figure 8.

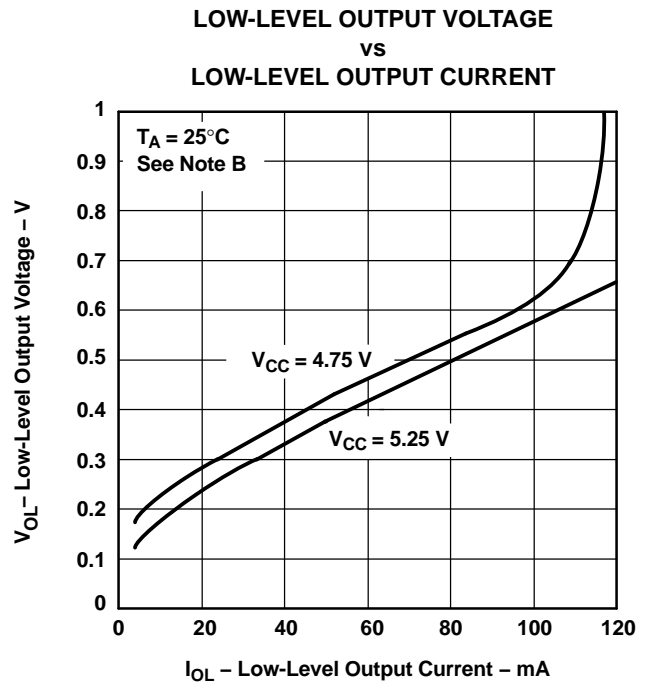


Figure 9.

- A. The A input is connected to V_{CC} during testing of the Y outputs and to ground during testing of the Z outputs.
- B. The A input is connected to ground during testing of the Y outputs and to V_{CC} during testing of the Z outputs.

TYPICAL CHARACTERISTICS (continued)



Figure 10.

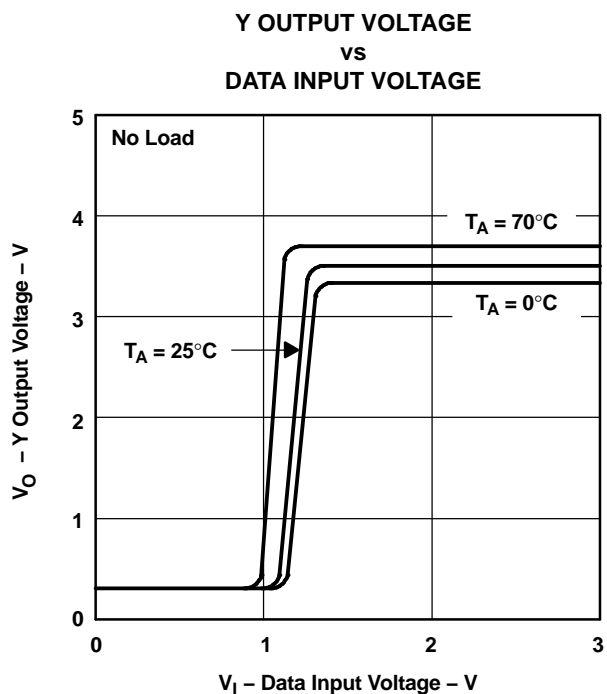


Figure 11.

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 5962-7802301M2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| 5962-7802301MEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| 5962-7802301MFA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| AM26LS31CD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LS31CDBR | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LS31CDBRE4 | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LS31CDBRG4 | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LS31CDE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LS31CDG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LS31CDR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LS31CDRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LS31CDRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LS31CN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| AM26LS31CNE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| AM26LS31CNSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LS31CNSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LS31MFKB | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| AM26LS31MJB | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| AM26LS31MWB | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| AM26LS31CDBR | SSOP | DB | 16 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| AM26LS31CDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| AM26LS31CDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| AM26LS31CNSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| AM26LS31CDBR | SSOP | DB | 16 | 2000 | 346.0 | 346.0 | 33.0 |
| AM26LS31CDR | SOIC | D | 16 | 2500 | 346.0 | 346.0 | 33.0 |
| AM26LS31CDR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| AM26LS31CNSR | SO | NS | 16 | 2000 | 346.0 | 346.0 | 33.0 |

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK

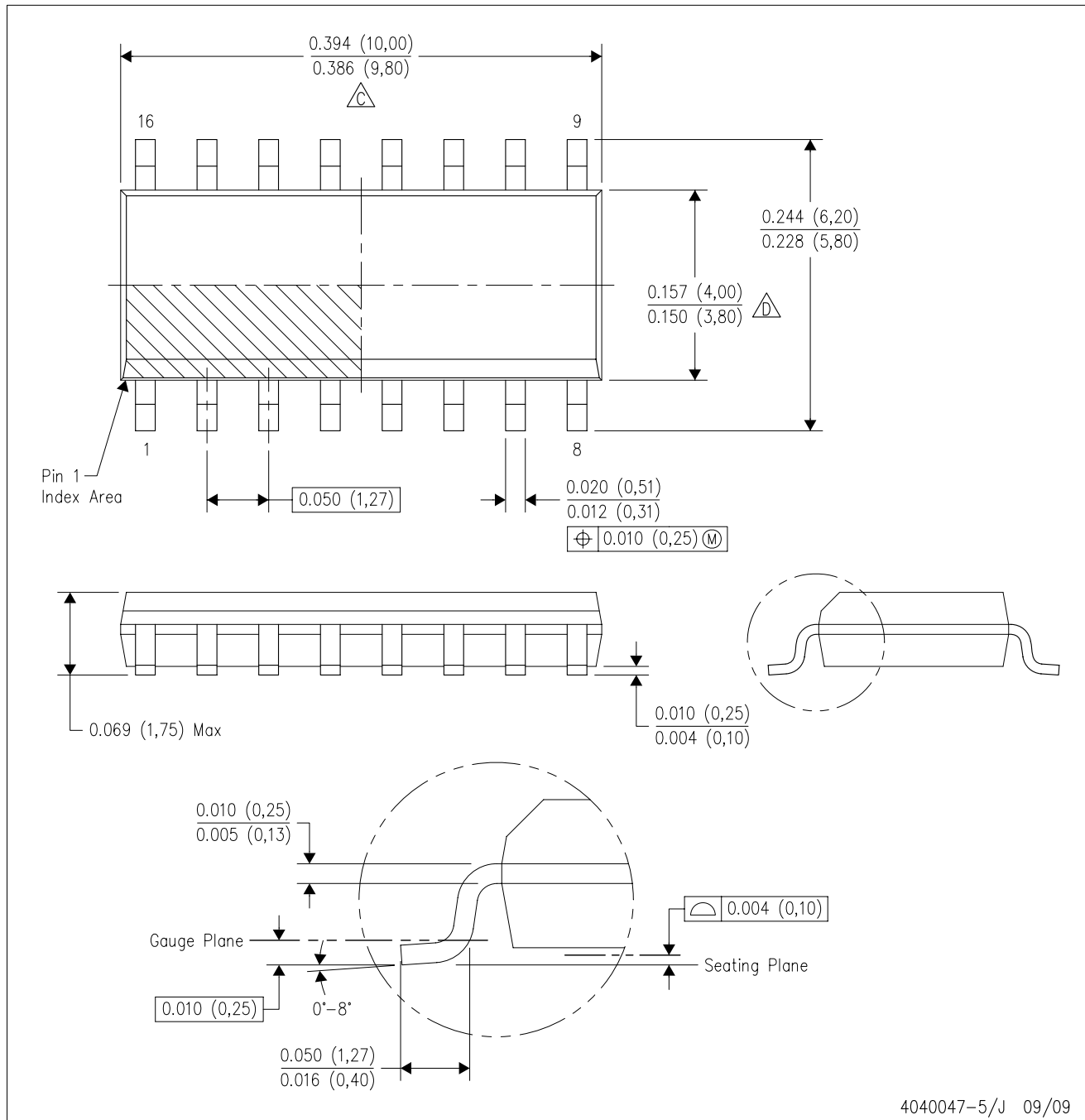


4040180-3/D 07/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-5/J 09/09

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AC.

D(R-PDSO-G16)



4209373/A 03/08

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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