CDP1802AC/3

High-Reliability CMOS 8-Bit Microprocessor

FN1441
Rev 3.00
October 17, 2008

The CDP1802A/3 High-Reliability LSI CMOS 8-bit register oriented Central-Processing Unit (CPU) is designed for use as a general purpose computing or control element in a wide range of stored-program systems or products.

The CDP1802A/3 includes all of the circuits required for fetching, interpreting, and executing instructions which have been stored in standard types of memories. Extensive input/output (I/O) control features are also provided to facilitate system design.

The 1800 Series Architecture is designed with emphasis on the total microcomputer system as an integral entity so that systems having maximum flexibility and minimum cost can be realized. The 1800 Series CPU also provides a synchronous interface to memories and external controllers for I/O devices, and minimizes the cost of interface controllers. Further, the I/O interface is capable of supporting devices operating in polled, interrupt-driven, or direct memory-access modes.

The CDP1802AC/3 is functionally identical to its predecessor, the CDP1802. The “A” version includes some performance enhancements and can be used as a direct replacement in systems using the CDP1802.

This type is supplied in a 40 Ld dual-in-line sidebrazed ceramic package (D suffix).

Features

For Use In Aerospace, Military, and Critical Industrial Equipment

- **Minimum Instruction Fetch-Execute Time of 4.5µs (Maximum Clock Frequency of 3.6MHz) at V_{DD} = 5V, T_A = +25°C**
- **Operation Over the Full Military Temperature Range . . . . . -55°C to +125°C**
- **Any Combination of Standard RAM and ROM Up to 65,536 Bytes**
- **8-Bit Parallel Organization With Bi-directional Data Bus and Multiplexed Address Bus**
- **16x16 Matrix of Registers for Use as Multiple Program Counters, Data Pointers, or Data Registers**
- **On-Chip DMA, Interrupt, and Flag Inputs**
- **High Noise Immunity . . . . . 30% of V_{DD}**
- **Pb-Free (RoHS compliant)**

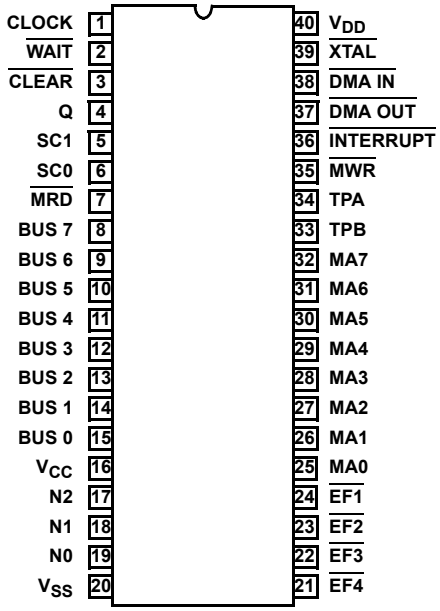
Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	CLOCK FREQUENCY AT 5V	PACKAGE	PKG DWG. #
CDP1802ACD3	CDP1802ACD3	-55 to +125	**Up to 3.2MHz**	40 Ld SBDIP	D40.6

NOTE: These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.

Pinout

CDP1802AC/3
(40 LD SBDIP)
TOP VIEW



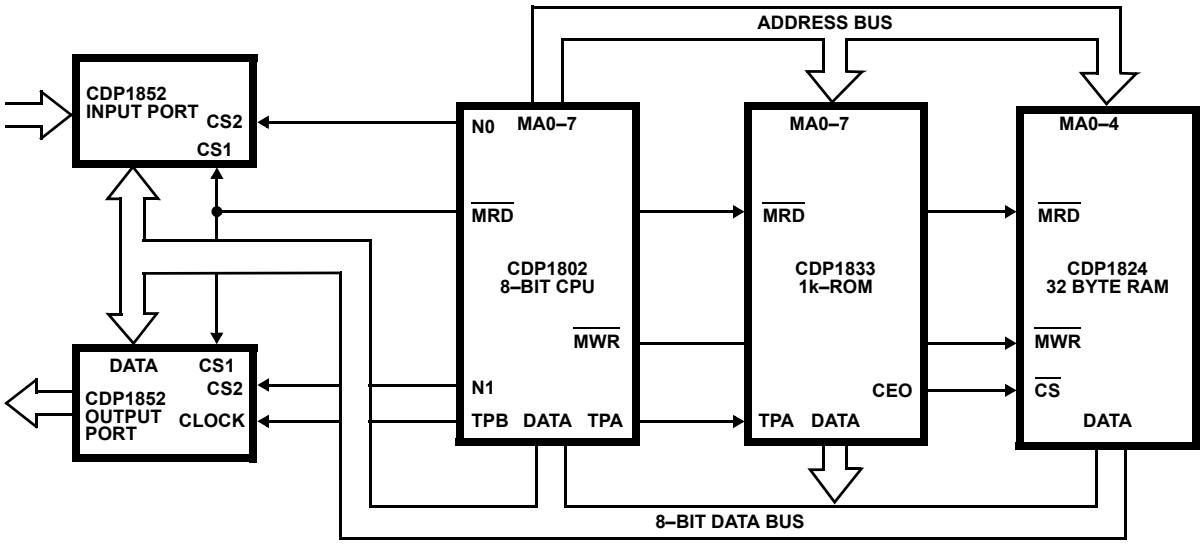
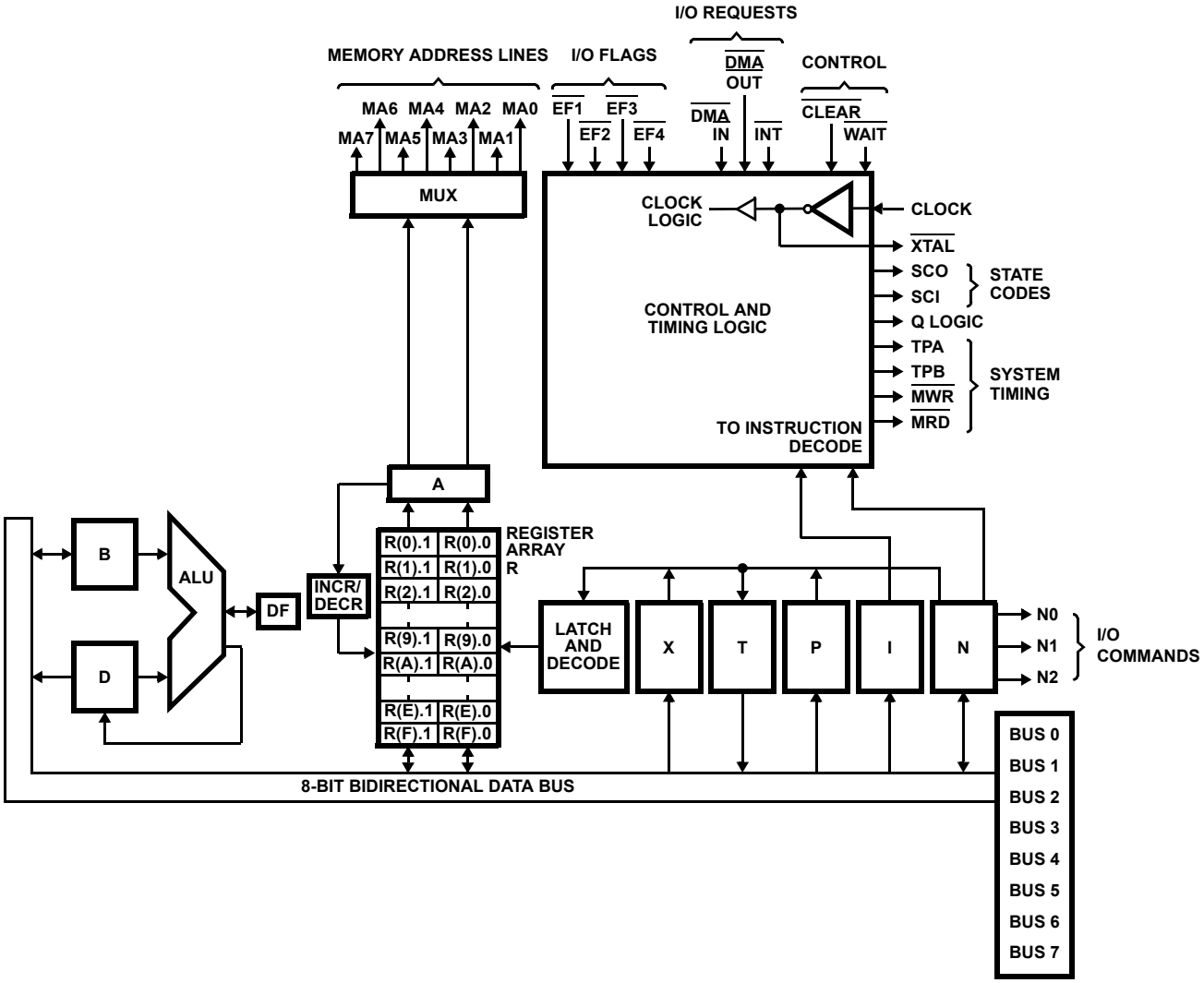


FIGURE 1. TYPICAL CDP1802A/3 SMALL MICROPROCESSOR SYSTEM

CPU Block Diagram



Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal)
CDP1802AC/3 . . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, any One Input . . . . . ±10mA

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SBDIP Package	55	15

Device Dissipation Per Output Transistor
T_A = Full Package Temperature Range 100mW
Operating Temperature Range (T_A)
Package Type D . . . . . -55°C to +125°C
Storage Temperature Range (T_{STG}) . . . . . -65°C to +150°C
Lead Temperature (During Soldering)
At distance 1/16 ± 1/32 In. (1.59 ±0.79mm)
from case for 10s max . . . . . +265°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Recommended Operating Conditions

T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	MIN	MAX	UNITS
DC Operating Voltage Range	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V
Maximum Clock Input Rise or Fall Time	-	1	µs

Performance Specifications

Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	V_{DD} (V)	-55°C TO +25°C	+125°C	UNITS
Minimum Instruction Time (Note 3)	5	4.5	5.9	µs
Maximum DMA Transfer Rate	5	450	340	Kbytes/s
Maximum Clock Input Frequency, Load Capacitance (C_L) = 50pF, f_{CL}	5	DC-3.6	DC-2.7	MHz

NOTE:

3. Equals 2 machine cycles - one Fetch and one Execute operation for all instructions except Long Branch and Long Skip, which require 3 machine cycles - one Fetch and two Execute operations.

Static Electrical Specifications

All Limits are 100% Tested. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	CONDITIONS			-55°C, +25°C		+125°C		UNITS
	V_{OUT} (V)	V_{IN}, (V)	V_{CC}, V_{DD} (V) (Note 4)	MIN	MAX	MIN	MAX	
Quiescent Device Current, I_{DD}	-	-	5	-	100	-	250	µA
Output Low Drive (Sink) Current (Except $\overline{XTAL}$), I_{OL}	0.4	0, 5	5	1.20	-	0.90	-	mA
$\overline{XTAL}$	0.4	5	5	185	-	140	-	µA
Output High Drive (Source) Current (Except $\overline{XTAL}$), I_{OH}	4.6	0, 5	5	-	-0.30	-	-0.20	mA
$\overline{XTAL}$	4.6	0	5	-	-135	-	-100	µA
Output Voltage Low-Level, V_{OL}	-	0, 5	5	-	0.1	-	0.2	V

Static Electrical Specifications

All Limits are 100% Tested. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	CONDITIONS			-55°C, +25°C		+125°C		UNITS
	V_{OUT} (V)	V_{IN}, (V)	V_{CC}, V_{DD} (V) (Note 4)	MIN	MAX	MIN	MAX	
Output Voltage High-Level, V_{OH}	-	0, 5	5	4.9	-	4.8	-	V
Input Low Voltage, V_{IL}	0.5, 4.5	-	5	-	1.5	-	1.5	V
Input High Voltage, V_{IH}	0.5, 4.5	-	5	3.5	-	3.5	-	V
Input Leakage Current, I_{IN}	Any Input	0, 5	5	-	±1	-	±5	µA
Three-State Output Leakage Current, I_{OUT}	0, 5	0, 5	5	-	±1	-	±5	µA

NOTE:

4. 5V level characteristics apply to Part No. CDP1802AC/3, and 5V and 10V level characteristics apply to part No. CDP1802A/3.

Timing Specifications

As a Function of T (T = 1/fCLOCK), C_L = 50 pF. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	V_{DD} (V)	LIMITS (Note 5)		UNITS
		-55°C, +25°C	+125°C	
High-Order Memory-Address Byte Setup to TPA ↘ Time, t_{SU}	5	2T-450	2T-580	ns
High-Order Memory-Address Byte Hold After TPA Time, t_H	5	T/2 +0	T/2 +0	ns
Low-Order Memory-Address Byte Hold After WR Time, t_H	5	T-30	T-40	ns
CPU Data to Bus Hold After WR Time, t_H	5	T-170	T-250	ns
Required Memory Access Time Address to Data, t_{ACC}	5	5T-300	5T-400	ns

NOTE:

5. These limits are not directly tested.

Implicit Specifications

(Note 6) T_A = -55°C to +25°C. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER		SYMBOL	V_{DD} (V)	TYPICAL VALUES	UNITS
Typical Total Power Dissipation Idle "00" at M(0000), C_L = 50pF	f = 2MHz	-	5	4	mW
Effective Input Capacitance any Input	-	C_{IN}	-	5	pF
Effective Three-State Terminal Capacitance Data Bus	-	-	-	7.5	pF
Minimum Data Retention Voltage	-	V_{DR}	-	2.4	V
Data Retention Current	-	I_{DR}	2.4	10	µA

NOTE:

6. These specifications are not tested. Typical values are provided for guidance only.

Dynamic Electrical Specifications

C_L = 50pF, Timing Measurement at 0.5 V_{DD} Point. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETERS	V_{DD} (V)	-55°C TO +25°C		+125°C		UNITS
		MIN	MAX	MIN	MAX	
PROGAGATION DELAY TIMES, t_{PLH}, t_{PHL}						
Clock to TPA, TPB	5	-	275	-	370	ns
Clock-to-Memory High Address Byte, t_{PLH}, t_{PHL}	5	-	725	-	950	ns
Clock-to-Memory Low Address Byte Valid, t_{PLH}, t_{PHL}	5	-	340	-	425	ns
Clock to $\overline{MRD}$, t_{PLH}, t_{PHL}	5	-	340	-	425	ns
Clock to $\overline{MWR}$, t_{PLH}, t_{PHL}	5	-	275	-	370	ns
Clock to (CPU DATA to BUS) Valid, t_{PLH}, t_{PHL}	5	-	430	-	550	ns
Clock to State Code, t_{PLH}, t_{PHL}	5	-	440	-	550	ns
Clock to Q, t_{PLH}, t_{PHL}	5	-	375	-	475	ns
Clock to N (0 to 2), t_{PLH}, t_{PHL}	5	-	400	-	525	ns
INTERFACE TIMING REQUIREMENTS (Note 7)						
Data Bus Input Setup, t_{SU}	5	10	-	10	-	ns
Data Bus Input Hold, t_H	5	175	-	230	-	ns
$\overline{DMA}$ Setup, t_{SU}	5	10	-	10	-	ns
$\overline{DMA}$ Hold, t_H	5	200	-	270	-	ns
Interrupt Setup, t_{SU}	5	10	-	10	-	ns
Interrupt Hold, t_H	5	175	-	230	-	ns
$\overline{WAIT}$ Setup, t_{SU}	5	30	-	30	-	ns
$\overline{EF1\text{-}4}$ Setup, t_{SU}	5	20	-	20	-	ns
$\overline{EF1\text{-}4}$ Hold, t_H	5	100	-	135	-	ns
REQUIRED PULSE WIDTH TIMES						
$\overline{CLEAR}$ Pulse Width, t_{WL}	5	150	-	200	-	ns
$\overline{CLOCK}$ Pulse Width, t_{WL}	5	140	-	185	-	ns

NOTE:

7. Minimum input setup and hold times required by Part CDP1802AC/3.

Timing Waveforms

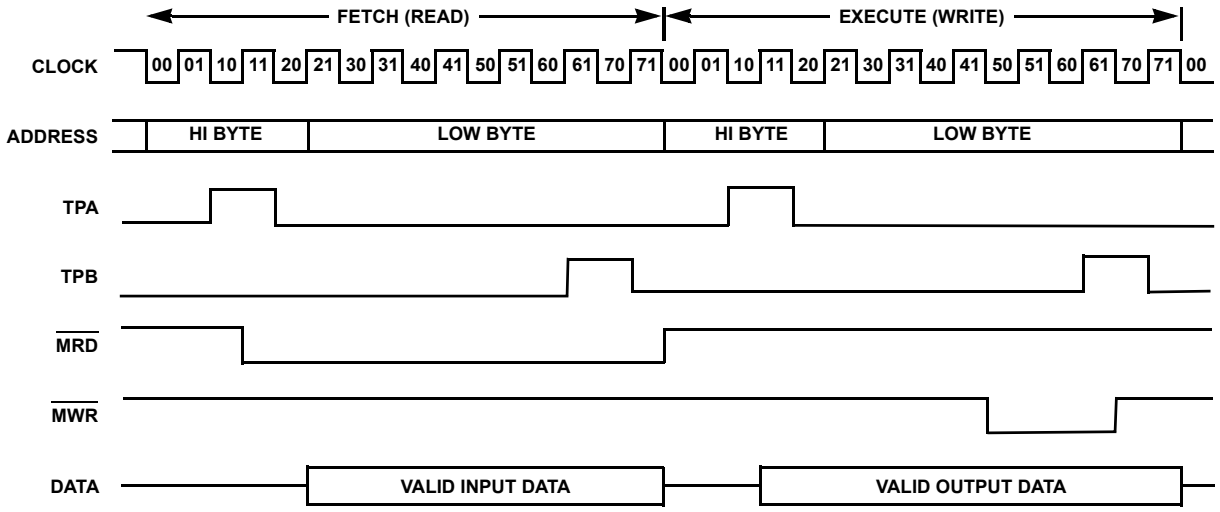


FIGURE 1. BASIC DC TIMING WAVEFORM, ONE INSTRUCTION CYCLE

Timing Waveforms (Continued)

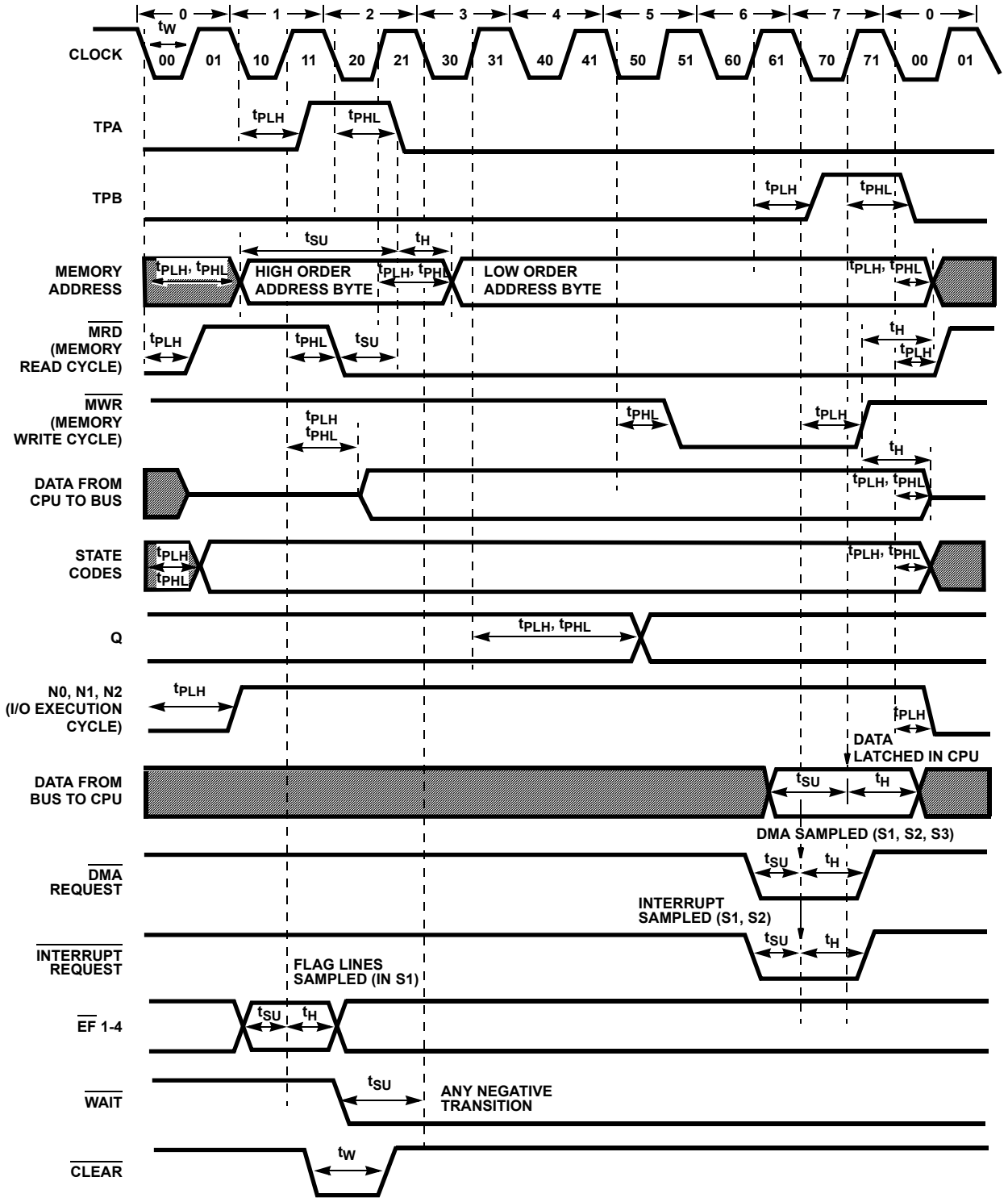


FIGURE 2. TIMING WAVEFORM

NOTES:

8. This timing diagram is used to show signal relationships only and does not represent any specific machine cycle.
9. All measurements are referenced to 50% point of the waveforms.
10. Shaded areas indicate “Don’t Care” or undefined state. Multiple transitions may occur during this period.

Machine Cycle Timing Waveforms (Propagation Delays Not Shown)

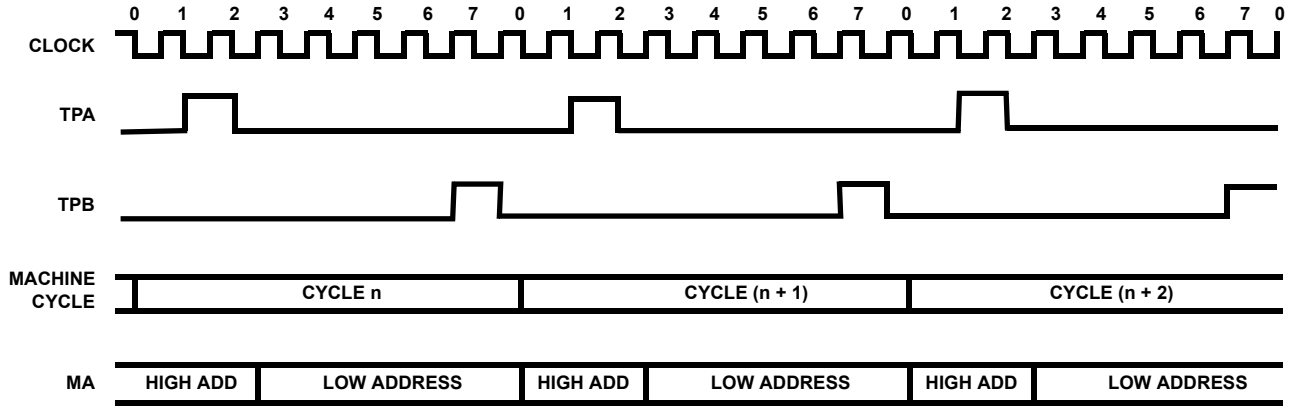


FIGURE 3. GENERAL TIMING WAVEFORMS

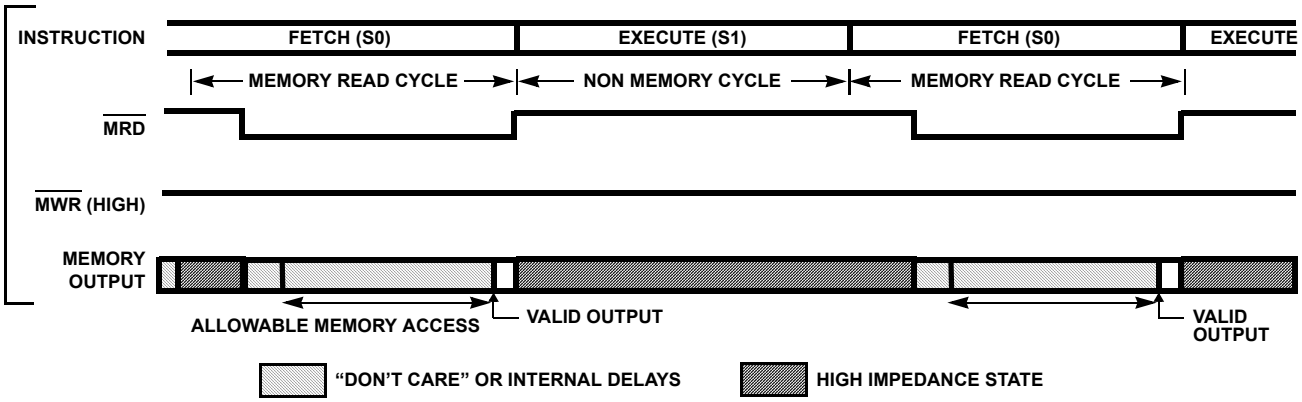


FIGURE 4. NON-MEMORY CYCLE TIMING WAVEFORMS

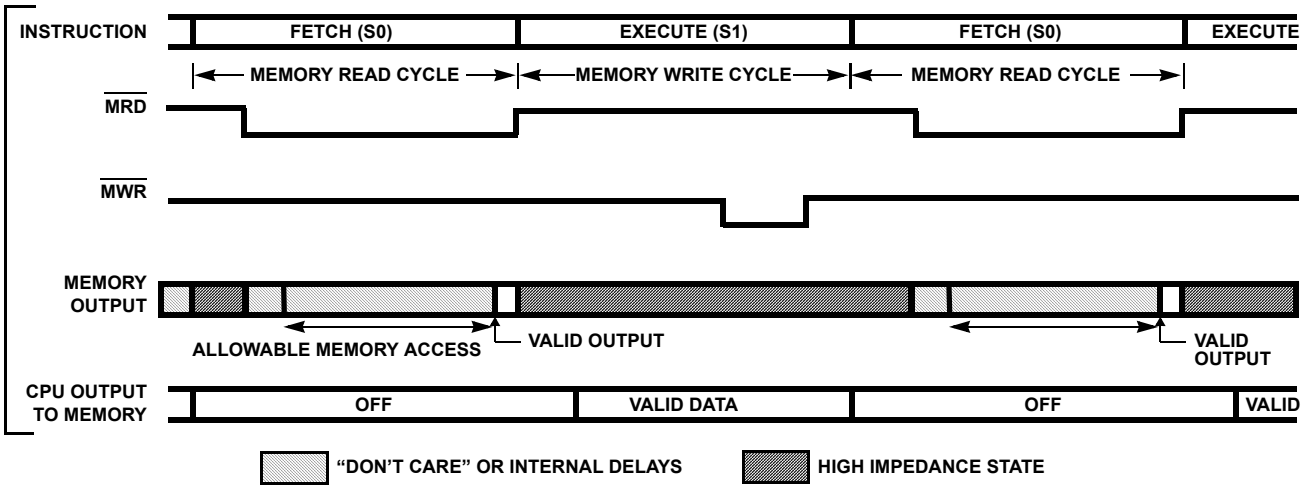


FIGURE 5. MEMORY WRITE CYCLE TIMING WAVEFORMS

Machine Cycle Timing Waveforms (Propagation Delays Not Shown) **(Continued)**

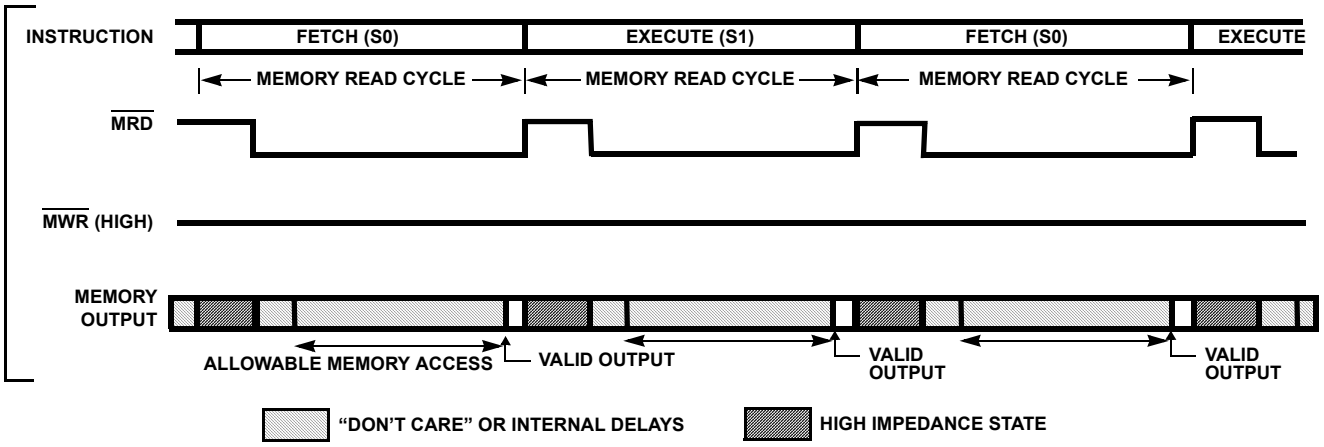


FIGURE 6. MEMORY READ CYCLE TIMING WAVEFORMS

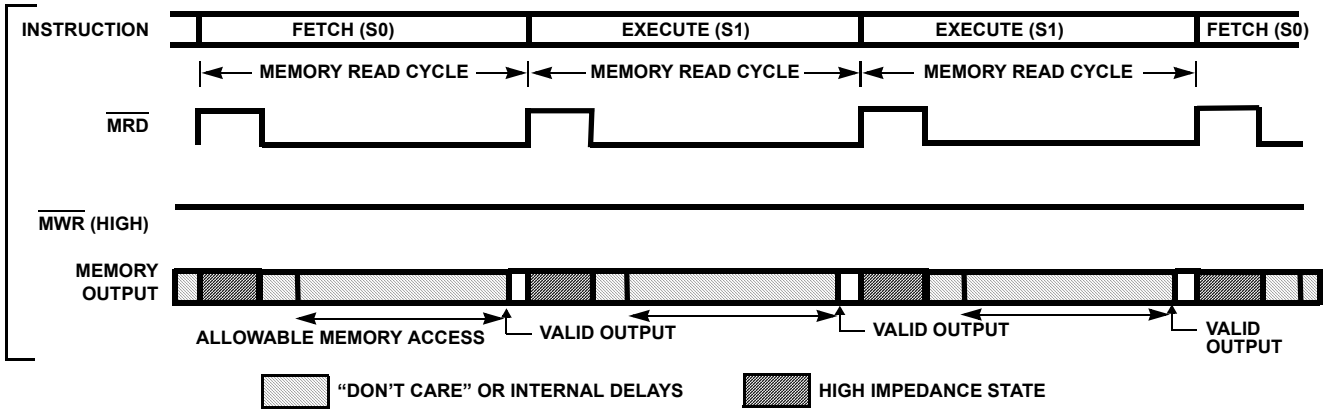


FIGURE 7. LONG BRANCH OR LONG SKIP CYCLE TIMING WAVEFORMS

Machine Cycle Timing Waveforms (Propagation Delays Not Shown) **(Continued)**

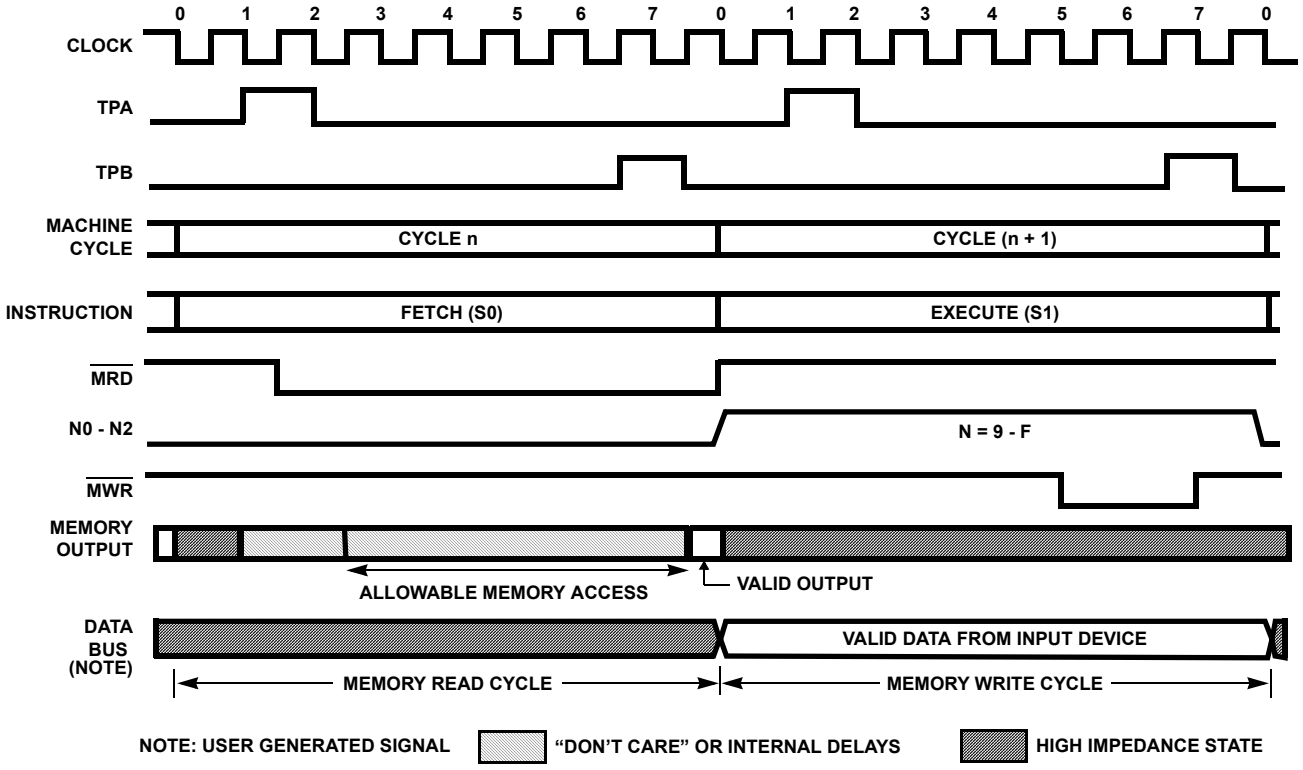


FIGURE 8. INPUT CYCLE TIMING WAVEFORMS

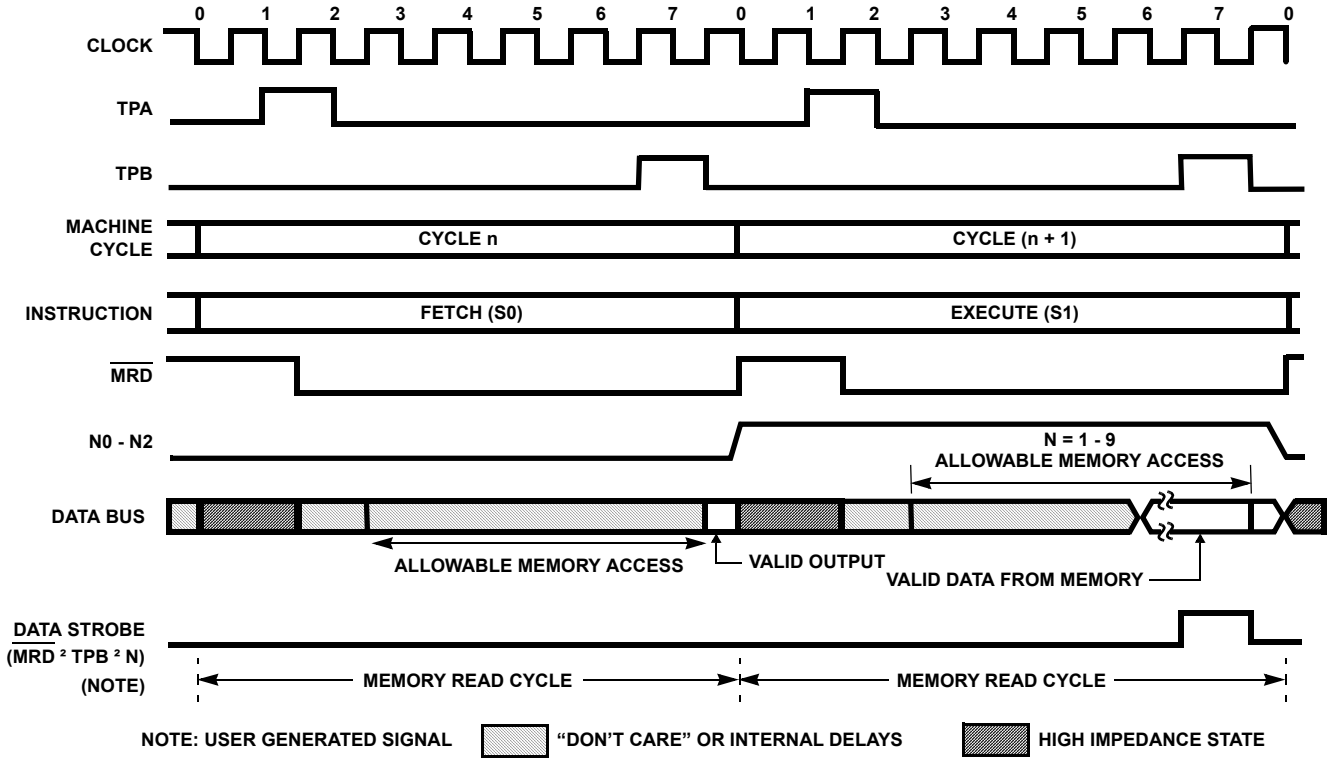


FIGURE 9. OUTPUT CYCLE TIMING WAVEFORMS

Machine Cycle Timing Waveforms (Propagation Delays Not Shown) **(Continued)**

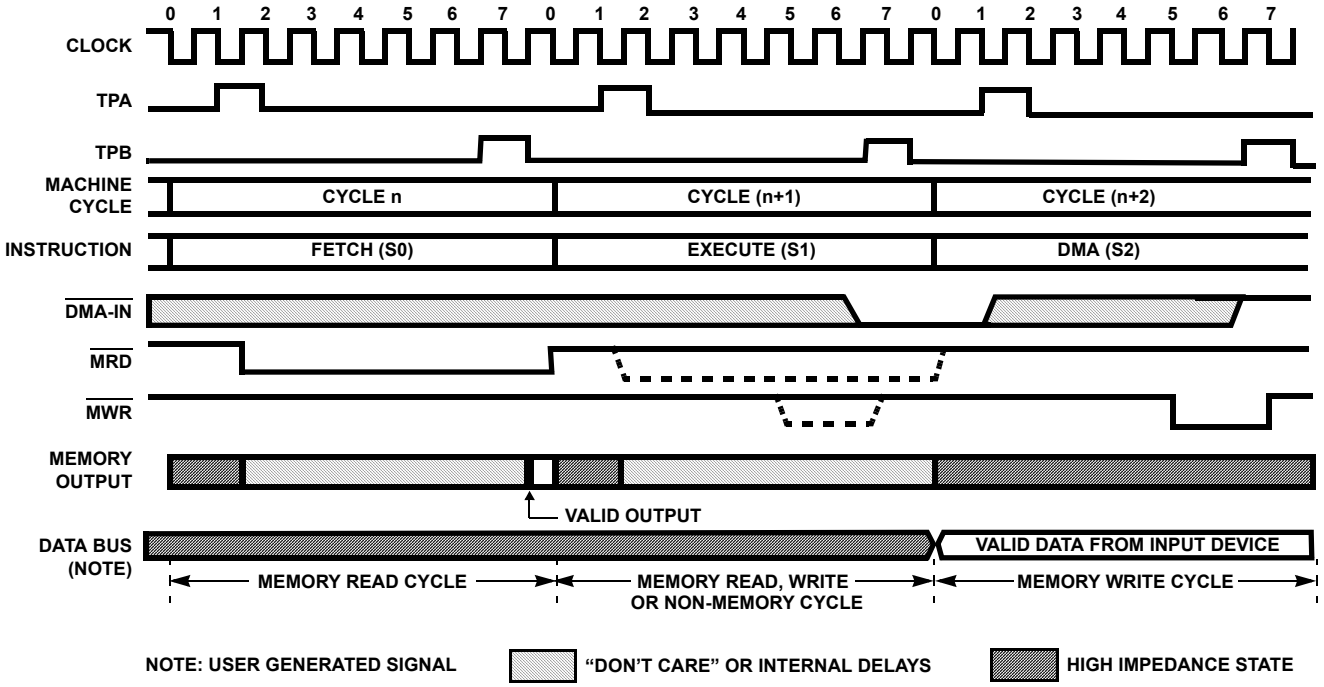


FIGURE 10. $\overline{\text{DMA IN}}$ CYCLE TIMING WAVEFORMS

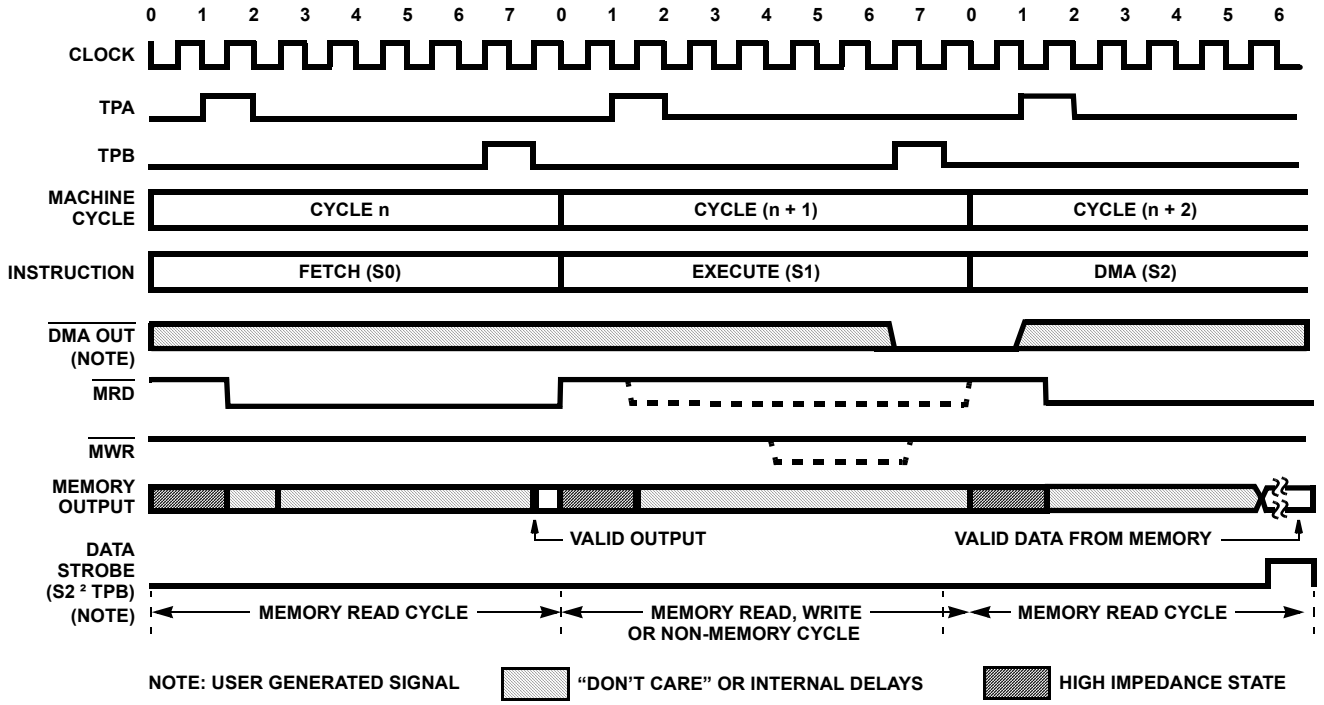


FIGURE 11. $\overline{\text{DMA OUT}}$ CYCLE TIMING WAVEFORMS

Machine Cycle Timing Waveforms (Propagation Delays Not Shown) **(Continued)**

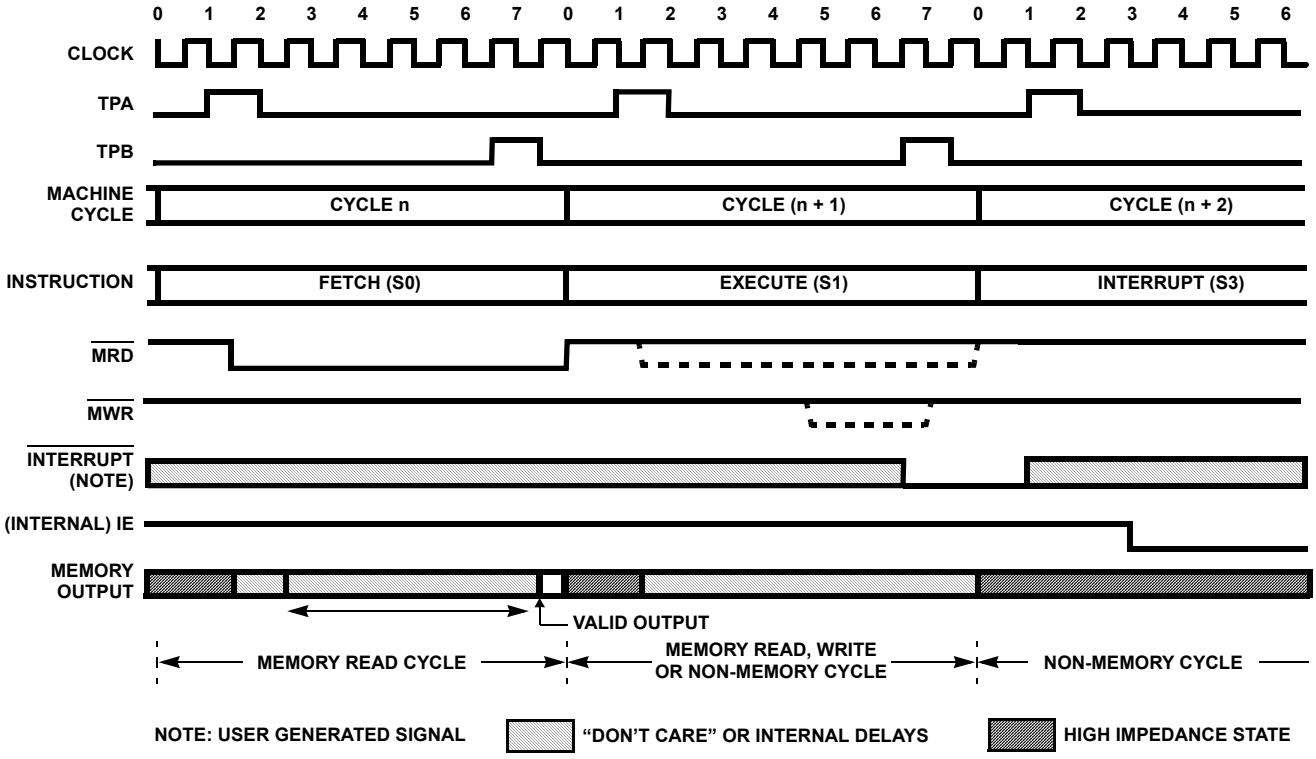


FIGURE 12. INTERRUPT CYCLE TIMING WAVEFORMS

Performance Curves

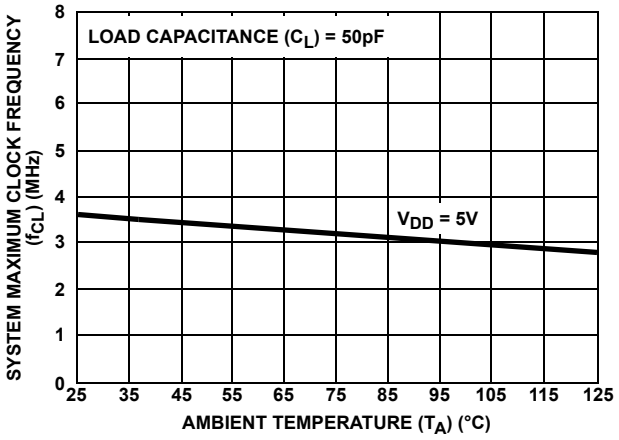


FIGURE 13. TYPICAL MAXIMUM CLOCK FREQUENCY AS A FUNCTION OF TEMPERATURE

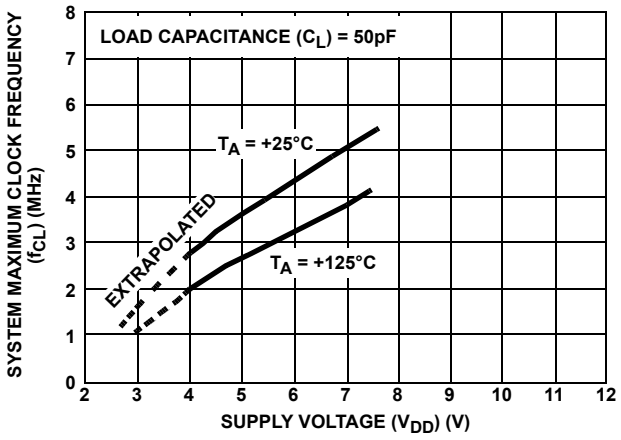


FIGURE 14. TYPICAL MAXIMUM CLOCK FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE

Performance Curves (Continued)

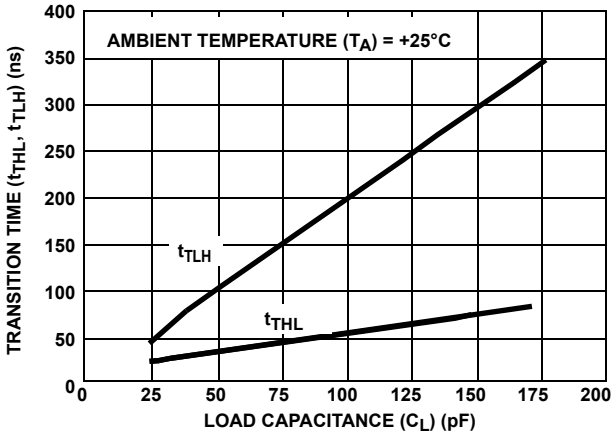


FIGURE 15. TYPICAL TRANSITION TIME vs LOAD CAPACITANCE

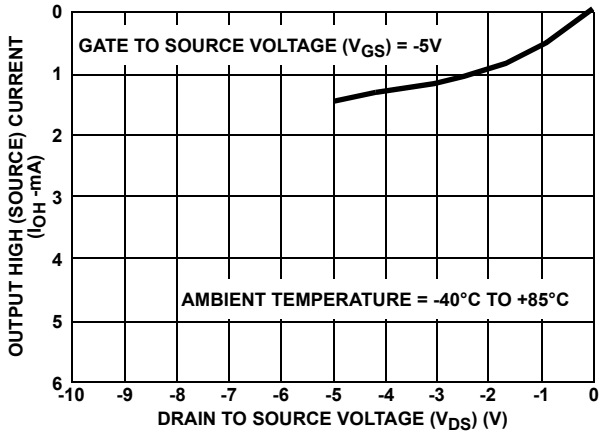


FIGURE 16. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

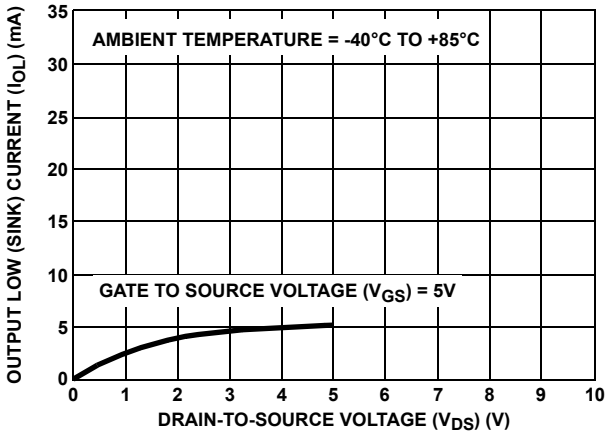


FIGURE 17. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

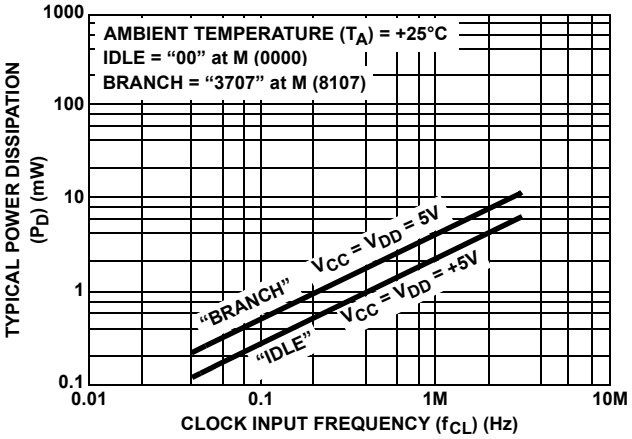


FIGURE 18. TYPICAL POWER DISSIPATION AS A FUNCTION OF CLOCK FREQUENCY FOR BRANCH INSTRUCTION AND IDLE INSTRUCTION

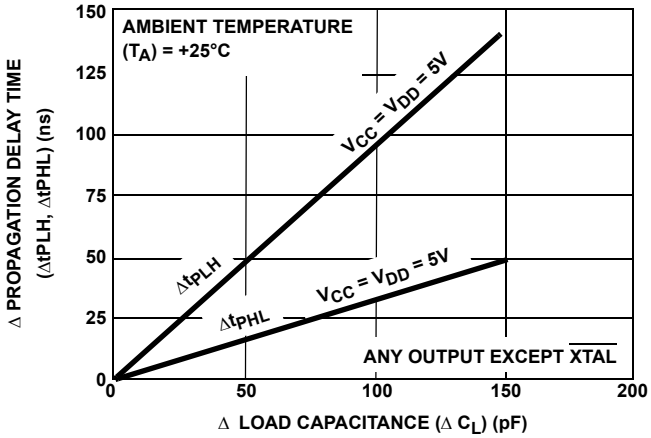


FIGURE 19. TYPICAL CHANGE IN PROPAGATION DELAY AS A FUNCTION OF A CHANGE IN LOAD CAPACITANCE

Signal Descriptions

Bus 0 to Bus 7 (Data Bus)

8-bit bidirectional DATA BUS lines. These lines are used for transferring data between the memory, the microprocessor, and I/O devices.

N0 to N2 (I/O Control Lines)

Activated by an I/O instruction to signal the I/O control logic of a data transfer between memory and I/O interface. These lines can be used to issue command codes or device selection codes to the I/O devices (independently or combined with the memory byte on the data bus when an I/O instruction is being executed). The N bits are low at all times except when an I/O instruction is being executed. During this time their state is the same as the corresponding bits in the N register.

The direction of data flow is defined in the I/O instruction by bit N3 (internally) and is indicated by the level of the MRD signal.

$\overline{MRD}$ = V_{CC}: Data from I/O to CPU and Memory

$\overline{MRD}$ = V_{SS}: Data from Memory to I/O

$\overline{EF1}$ to $\overline{EF4}$ (4 Flags)

These inputs enable the I/O controllers to transfer status information to the processor. The levels can be tested by the conditional branch instructions. They can be used in conjunction with the INTERRUPT request line to establish interrupt priorities. These flags can also be used by I/O devices to “call the attention” of the processor, in which case the program must routinely test the status of these flag(s). The flag(s) are sampled at the beginning of every S1 cycle.

$\overline{INTERRUPT}$, $\overline{DMA\text{-}IN}$, $\overline{DMA\text{-}OUT}$ (3 I/O Requests)

These inputs are sampled by the CPU during the interval between the leading edge of TPB and the leading edge of TPA.

Interrupt Action - X and P are stored in T after executing current instruction; designator X is set to 2; designator P is set to 1; interrupt enable is reset to 0 (inhibit); and instruction execution is resumed. The interrupt action requires one machine cycle (S3).

DMA Action - Finish executing current instruction; R(0) points to memory area for data transfer; data is loaded into or read out of memory; and increment R(0).

NOTE: In the event of concurrent DMA and Interrupt requests, DMA-IN has priority followed by DMA-OUT and then Interrupt.

SC0, SC1 (2 State Code Lines)

These outputs indicate that the CPU is:

1. Fetching an instruction
2. Executing an instruction
3. Processing a DMA request,
4. acknowledging an interrupt request. The levels of state code are tabulated in Table 1. All states are valid at TPA. H = V_{CC}, L = V_{SS}.

TABLE 1. LEVELS OF STATE CODE

STATE TYPE	STATE CODE LINES	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

TPA, TPB (2 Timing Pulses)

Positive pulses that occur once in each machine cycle (TPB follows TPA). They are used by I/O controllers to interpret codes and to time interaction with the data bus. The trailing edge of TPA is used by the memory system to latch the higher-order byte of the 16-bit memory address. TPA is suppressed in IDLE when the CPU is in the load mode.

MA0 to MA7 (8 Memory Address Lines)

In each cycle, the higher-order byte of a 16-bit CPU memory address appears on the memory address lines MA0-7 first. Those bits required by the memory system can be strobed into external address latches by timing pulse TPA. The low order byte of the 16-bit address appears on the address lines after the termination of TPA. Latching of all 8 higher-order address bits would permit a memory system of 64k bytes.

$\overline{MWR}$ (Write Pulse)

A negative pulse appearing in a memory-write cycle, after the address lines have stabilized.

$\overline{MRD}$ (Read Level)

A low level on MRD indicates a memory read cycle. It can be used to control three-state outputs from the addressed memory which may have a common data input and output bus. If a memory does not have a three-state high-impedance output, MRD is useful for driving memory/bus separator gates. It is also used to indicate the direction of data transfer during an I/O instruction. For additional information see Table 4.

Q

Single bit output from the CPU which can be set or reset under program control. During SEQ or REQ instruction execution, Q is set or reset between the trailing edge of TPA and the leading edge of TPB.

CLOCK

Input for externally generated single-phase clock. The clock is counted down internally to 8-clock pulses per machine cycle.

$\overline{XTAL}$

Connection to be used with clock input terminal, for an external crystal, if the on-chip oscillator is utilized. The crystal is connected between terminals 1 and 39 (CLOCK and $\overline{XTAL}$) in parallel with a resistance (10MΩ typ). Frequency trimming capacitors may be required at terminals 1 and 39. For additional information, see Application Note AN6565.

$\overline{WAIT}$, $\overline{CLEAR}$ (2 Control Lines)

Provide four control modes as listed in Table 2:

TABLE 2. TRUTH TABLE

$\overline{CLEAR}$	$\overline{WAIT}$	MODE
L	L	LOAD
L	H	RESET
H	L	PAUSE
H	H	RUN

V_{DD}, V_{SS}, V_{CC} (Power Levels)

The internal voltage supply V_{DD} is isolated from the Input/Output voltage supply V_{CC} so that the processor may operate at maximum speed while interfacing with peripheral devices operating at lower voltage. V_{CC} must be less than or equal to V_{DD}. All outputs swing from V_{SS} to V_{CC}. The recommended input voltage swing is V_{SS} to V_{CC}.

Architecture

The “CPU Block Diagram” is shown on page 3. The principal feature of this system is a register array (R) consisting of sixteen 16-bit scratchpad registers. Individual registers in the array (R) are designated (selected) by a 4-bit binary code from one of the 4-bit registers labeled N, P and X. The contents of any register can be directed to any one of the following three paths:

1. The external memory (multiplexed, higher-order byte first, on to 8 memory address lines).
2. The D register (either of the two bytes can be gated to D).
3. The increment/decrement circuit where it is increased or decreased by one and stored back in the selected 16-bit register.

The three paths, depending on the nature of the instruction, may operate independently or in various combinations in the same machine cycle.

With two exceptions, CPU instruction consists of two 8-clock-pulse machine cycles. The first cycle is the fetch cycle, and the second and third if necessary, are execute cycles. During the fetch cycle the four bits in the P designator select one of the 16 registers R(P) as the current program counter. The selected register R(P) contains the address of the memory location from which the instruction is to be fetched. When the instruction is read out from the memory, the higher order 4 bits of the instruction byte are loaded into the register and the lower order 4 bits into the N register. The content of the program counter is automatically incremented by one so that R(P) is now “pointing” to the next byte in the memory.

The X designator selects one of the 16 registers R(X) to “point” to the memory for an operand (or data) in certain ALU or I/O operations.

The N designator can perform the following five functions depending on the type of instruction fetched:

1. Designate one of the 16 registers in R to be acted upon during register operations.
2. Indicate to the I/O devices a command code or device selection code for peripherals.
3. Indicate the specific operation to be executed during the ALU instructions, types of test to be performed during the Branch instruction, or the specific operation required in a class of miscellaneous instructions (70 - 73 and 78 - 7B).
4. Indicate the value to be loaded into P to designate a new register to be used as the program counter R(P).
5. Indicate the value to be loaded into X to designate a new register to be used as data pointer R(X).

The registers in R can be assigned by a programmer in three different ways: as program counters, as data pointers, or as scratchpad locations (data registers) to hold two bytes of data.

Program Counters

Any register can be the main program counter; the address of the selected register is held in the P designator. Other registers in R can be used as subroutine program counters. By single instruction the contents of the P register can be changed to effect a “call” to a subroutine. When interrupts are being serviced, register R(1) is used as the program counter for the user's interrupt servicing routine. After reset, and during a DMA operation, R(0) is used as the program counter. At all other times the register designated as program counter is at the discretion of the user.

Data Pointers

The registers in R may be used as data pointers to indicate a location in memory. The register designated by X (i.e., R(X)) points to memory for the following instructions (see Table 4).

1. ALU operations F1 - F5, F7, 74, 75, 77
2. Output instructions 61 through 67
3. Input instructions 69 through 6F
4. Certain miscellaneous instructions - 70 - 73, 78, 60, F0

The register designated by N (i.e., R(N)) points to memory for the “load D from memory” instructions 0N and 4N and the “Store D” instruction 5N. The register designated by P (i.e., the program counter) is used as the data pointer for ALU instructions F8 - FD, FF, 7C, 7D, 7F. During these instruction executions, the operation is referred to as “data immediate”.

Another important use of R as a data pointer supports the built-in Direct-Memory-Access (DMA) function. When a

DMA-IN or DMA-Out request is received, one machine cycle is “stolen”. This operation occurs at the end of the execute machine cycle in the current instruction. Register R(0) is always used as the data pointer during the DMA operation. The data is read from (DMA-Out) or written into (DMA-IN) the memory location pointed to by the R(0) register. At the end of the transfer, R(0) is incremented by one so that the processor is ready to act upon the next DMA byte transfer request. This feature in the 1800-series architecture saves a substantial amount of logic when fast exchanges of blocks of data are required, such as with magnetic discs or during CRT-display-refresh cycles.

Data Registers

When registers in R are used to store bytes of data, four instructions are provided which allow D to receive from or write into either the higher-order or lower-order byte portions of the register designated by N. By this mechanism (together with loading by data immediate) program pointer and data pointer designations are initialized. Also, this technique allows scratchpad registers in R to be used to hold general data. By employing increment or decrement instructions, such registers may be used as loop counters.

The Q Flip-Flop

An internal flip-flop, Q, can be set or reset by instruction and can be sensed by conditional branch instructions. The output of Q is also available as a microprocessor output.

Interrupt Servicing

Register R(1) is always used as the program counter whenever interrupt servicing is initiated. When an interrupt request occurs and the interrupt is allowed by the program (again, nothing takes place until the completion of the current instruction), the contents of the X and P registers are stored in the temporary register T, and X and P are set to new values; hex digit 2 in X and hex digit 1 in P. Interrupt Enable is automatically deactivated to inhibit further interrupts. The user's interrupt routine is now in control; the contents of T may be saved by means of a single instruction (78) in the memory location pointed to by R(X). At the conclusion of the interrupt, the user's routine may restore the pre-interrupted value of X and P with a single instruction (70 or 71). The Interrupt Enable flip-flop can be activated to permit further interrupts or can be disabled to prevent them.

CPU Register Summary

D	8 Bits	Data Register (Accumulator)
DF	1-Bit	Data Flag (ALU Carry)
B	8 Bits	Auxiliary Holding Register
R	16 Bits	1 of 16 Scratchpad Registers
P	4 Bits	Designates which register is Program Counter
X	4 Bits	Designates which register is Data Pointer
N	4 Bits	Holds Low-Order Instruction Digit
I	4 Bits	Holds High-Order Instruction Digit
T	8 Bits	Holds old X, P after Interrupt (X is high nibble)
IE	1-Bit	Interrupt Enable
Q	1-Bit	Output Flip-Flop

CDP1802 Control Modes

The $\overline{\text{WAIT}}$ and $\overline{\text{CLEAR}}$ lines provide four control modes as listed in Table 3:

TABLE 3. CONTROL MODES

$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	MODE
L	L	LOAD
L	H	RESET
H	L	PAUSE
H	H	RUN

The functions of the modes are defined as follows:

LOAD

Holds the CPU in the IDLE execution state and allows an I/O device to load the memory without the need for a “bootstrap” loader. It modifies the IDLE condition so that DMA-IN operation does not force execution of the next instruction.

RESET

Registers I, N, Q are reset, IE is set and 0’s (VSS) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The first machine cycle after termination of reset is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1 and register X, P, and R(0) are reset. Interrupt and DMA servicing are suppressed during the initialization cycle. The next cycle is an S0, S1, or an S2 but never an S3. With the use of a 71 instruction followed by 00 at memory locations 0000 and 0001, this feature may be used to reset IE, so as to preclude interrupts until ready for them. Power-up reset can be realized

by connecting an RC network directly to the CLEAR pin, since it has a Schmitt triggered input; see Figure 20.

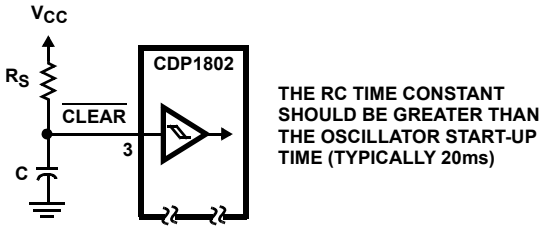


FIGURE 20. RESET DIAGRAM

PAUSE

Stops the internal CPU timing generator on the first negative high-to-low transition of the input clock. The oscillator continues to operate, but subsequent clock transitions are ignored.

RUN

May be initiated from the Pause or Reset mode functions. If initiated from Pause, the CPU resumes operation on the first negative high-to-low transition of the input clock. When initiated from the Reset operation, the first machine cycle following Reset is always the initialization cycle. The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

RUN-MODE STATE TRANSITIONS

The CPU state transitions when in the RUN and RESET modes are shown in Figure 21. Each machine cycle requires the same period of time, 8-clock pulses, except the initialization cycle, which requires 9-clock pulses. The execution of an instruction requires either two or three machine cycles, S0 followed by a single S1 cycle or two S1 cycles. S2 is the response to a DMA request and S3 is the interrupt response. Table 5 shows the conditions on Data Bus and Memory Address lines during all machine states.

INSTRUCTION SET

The CPU instruction summary is given in Table 4. Hexadecimal notation is used to refer to the 4-bit binary codes.

In all registers bits are numbered from the least significant bit (LSB) to the most significant bit (MSB) starting with 0.

R(W): Register designated by W, where:

W = N or X, or P

R(W).0: Lower order byte of R(W)

R(W).1: Higher order byte of R(W)

OPERATION NOTATION

$M(R(N)) \rightarrow D; R(N) + 1 \rightarrow R(N)$

This notation means: The memory byte pointed to by R(N) is loaded into D, and R(N) is incremented by 1.

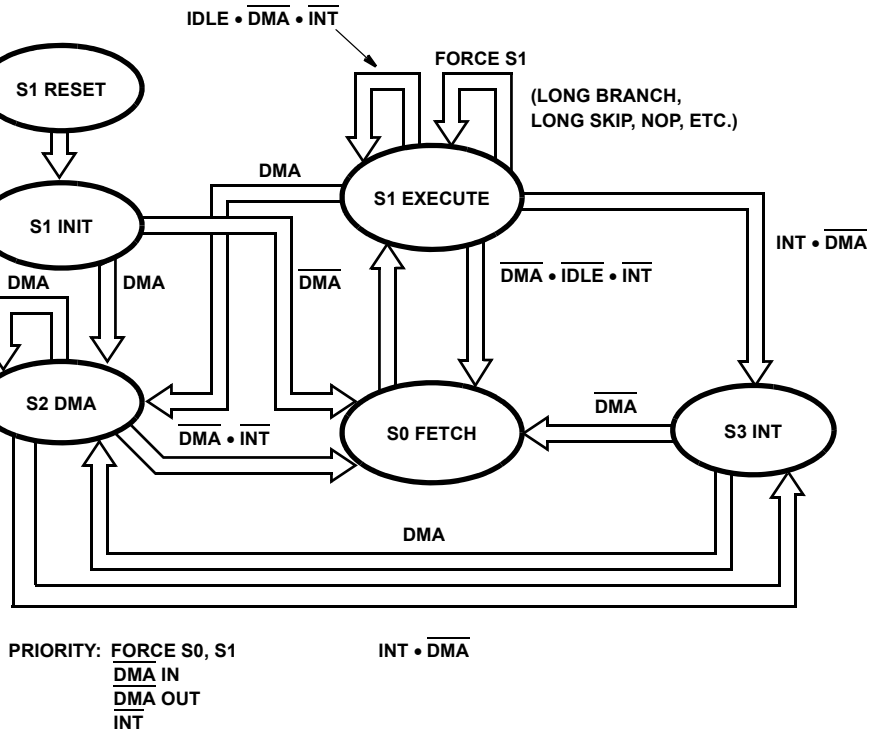


FIGURE 21. STATE TRANSITION DIAGRAM

TABLE 4. INSTRUCTION SUMMARY (See Notes 11 through 16)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
MEMORY REFERENCE			
LOAD VIA N	LDN	0N	M(R(N)) → D; FOR N not 0
LOAD ADVANCE	LDA	4N	M(R(N)) → D; R(N) + 1 → R(N)
LOAD VIA X	LDX	F0	M(R(X)) → D
LOAD VIA X AND ADVANCE	LDXA	72	M(R(X)) → D; R(X) + 1 → R(X)
LOAD IMMEDIATE	LDI	F8	M(R(P)) → D; R(P) + 1 → R(P)
STORE VIA N	STR	5N	D → M(R(N))
STORE VIA X AND DECREMENT	STXD	73	D → M(R(X)); R(X) - 1 → R(X)
REGISTER OPERATIONS			
INCREMENT REG N	INC	1N	R(N) + 1 → R(N)
DECREMENT REG N	DEC	2N	R(N) - 1 → R(N)
INCREMENT REG X	IRX	60	R(X) + 1 → R(X)
GET LOW REG N	GLO	8N	R(N).0 → D
PUT LOW REG N	PLO	AN	D → R(N).0
GET HIGH REG N	GHI	9N	R(N).1 → D
PUT HIGH REG N	PHI	BN	D → R(N).1
LOGIC OPERATIONS (Note 11)			
OR	OR	F1	M(R(X)) OR D → D
OR IMMEDIATE	ORI	F9	M(R(P)) OR D → D; R(P) + 1 → R(P)
EXCLUSIVE OR	XOR	F3	M(R(X)) XOR D → D
EXCLUSIVE OR IMMEDIATE	XRI	FB	M(R(P)) XOR D → D; R(P) + 1 → R(P)
AND	AND	F2	M(R(X)) AND D → D
AND IMMEDIATE	ANI	FA	M(R(P)) AND D → D; R(P) + 1 → R(P)
SHIFT RIGHT	SHR	F6	SHIFT D RIGHT, LSB(D) → DF, 0 → MSB(D)
SHIFT RIGHT WITH CARRY	SHRC	76 (Note 12)	SHIFT D RIGHT, LSB(D) → DF, DF → MSB(D)
RING SHIFT RIGHT	RSHR	76 (Note 12)	SHIFT D RIGHT, LSB(D) → DF, DF → MSB(D)
SHIFT LEFT	SHL	FE	SHIFT D LEFT, MSB(D) → DF, 0 → LSB(D)
SHIFT LEFT WITH CARRY	SHLC	7E (Note 12)	SHIFT D LEFT, MSB(D) → DF, DF → LSB(D)
RING SHIFT LEFT	RSHL	7E (Note 12)	SHIFT D LEFT, MSB(D) → DF, DF → LSB(D)
ARITHMETIC OPERATIONS (Note 11)			
ADD	ADD	F4	M(R(X)) + D → DF, D
ADD IMMEDIATE	ADI	FC	M(R(P)) + D → DF, D; R(P) + 1 → R(P)
ADD WITH CARRY	ADC	74	M(R(X)) + D + DF → DF, D
ADD WITH CARRY, IMMEDIATE	ADCI	7C	M(R(P)) + D + DF → DF, D; R(P) + 1 → R(P)
SUBTRACT D	SD	F5	M(R(X)) - D → DF, D
SUBTRACT D IMMEDIATE	SDI	FD	M(R(P)) - D → DF, D; R(P) + 1 → R(P)
SUBTRACT D WITH BORROW	SDB	75	M(R(X)) - D - (NOT DF) → DF, D

TABLE 4. INSTRUCTION SUMMARY (See Notes 11 through 16) **(Continued)**

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
SUBTRACT D WITH BORROW, IMMEDIATE	SDBI	7D	M(R(P)) - D - (Not DF) → DF, D; R(P) + 1 → R(P)
SUBTRACT MEMORY	SM	F7	D-M(R(X)) → DF, D
SUBTRACT MEMORY IMMEDIATE	SMI	FF	D-M(R(P)) → DF, D; R(P) + 1 → R(P)
SUBTRACT MEMORY WITH BORROW	SMB	77	D-M(R(X))-(NOT DF) → DF, D
SUBTRACT MEMORY WITH BORROW, IMMEDIATE	SMBI	7F	D-M(R(P))-(NOT DF) → DF, D; R(P) + 1 → R(P)
BRANCH INSTRUCTIONS - SHORT BRANCH			
SHORT BRANCH	BR	30	M(R(P)) → R(P).0
NO SHORT BRANCH (See SKP)	NBR	38 (Note 12)	R(P) + 1 → R(P)
SHORT BRANCH IF D = 0	BZ	32	IF D = 0, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF D NOT 0	BNZ	3A	IF D NOT 0, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF DF = 1	BDF	33 (Note 12)	IF DF = 1, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF POS OR ZERO	BPZ		
SHORT BRANCH IF EQUAL OR GREATER	BGE		
SHORT BRANCH IF DF = 0	BNF	3B (Note 12)	IF DF = 0, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF MINUS	BM		
SHORT BRANCH IF LESS	BL		
SHORT BRANCH IF Q = 1	BQ	31	IF Q = 1, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF Q = 0	BNQ	39	IF Q = 0, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF EF1 = 1 ($\overline{EF1}$ = V_{SS})	B1	34	IF EF1 =1, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF EF1 = 0 ($\overline{EF1}$ = V_{CC})	BN1	3C	IF EF1 = 0, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF EF2 = 1 ($\overline{EF2}$ = V_{SS})	B2	35	IF EF2 = 1, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF EF2 = 0 ($\overline{EF2}$ = V_{CC})	BN2	3D	IF EF2 = 0, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF EF3 = 1 ($\overline{EF3}$ = V_{SS})	B3	36	IF EF3 = 1, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF EF3 = 0 ($\overline{EF3}$ = V_{CC})	BN3	3E	IF EF3 = 0, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF EF4 = 1 ($\overline{EF4}$ = V_{SS})	B4	37	IF EF4 = 1, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF EF4 = 0 ($\overline{EF4}$ = V_{CC})	BN4	3F	IF EF4 = 0, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
BRANCH INSTRUCTIONS - LONG BRANCH			
LONG BRANCH	LBR	C0	M(R(P)) → R(P). 1, M(R(P) + 1) → R(P).0
NO LONG BRANCH (See LSKP)	NLBR	C8 (Note 12)	R(P) = 2 → R(P)
LONG BRANCH IF D = 0	LBZ	C2	IF D = 0, M(R(P)) → R(P).1, M(R(P) +1) → R(P).0, ELSE R(P) + 2 → R(P)
LONG BRANCH IF D NOT 0	LBNZ	CA	IF D Not 0, M(R(P)) → R(P).1, M(R(P) + 1) → R(P).0, ELSE R(P) + 2 → R(P)
LONG BRANCH IF DF = 1	LBDF	C3	IF DF = 1, M(R(P)) → R(P).1, M(R(P) + 1) → R(P).0, ELSE R(P) + 2 → R(P)
LONG BRANCH IF DF = 0	LBNF	CB	IF DF = 0, M(R(P)) → R(P).1, M(R(P) + 1) → R(P).0, ELSE R(P) + 2 → R(P)
LONG BRANCH IF Q = 1	LBQ	C1	IF Q = 1, M(R(P)) → R(P).1, M(R(P) + 1) → R(P).0, ELSE R(P) + 2 → R(P)

TABLE 4. INSTRUCTION SUMMARY (See Notes 11 through 16) **(Continued)**

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
LONG BRANCH IF Q = 0	LBNQ	C9	IF Q = 0, M(R(P)) → R(P).1, M(R(P) + 1) → R(P).0 EISE R(P) + 2 → R(P)
SKIP INSTRUCTIONS			
SHORT SKIP (See NBR)	SKP	38 (Note 12)	R(P) + 1 → R(P)
LONG SKIP (See NLBR)	LSKP	C8 (Note 12)	R(P) + 2 → R(P)
LONG SKIP IF D = 0	LSZ	CE	IF D = 0, R(P) + 2 → R(P), ELSE CONTINUE
LONG SKIP IF D NOT 0	LSNZ	C6	IF D Not 0, R(P) + 2 → R(P), ELSE CONTINUE
LONG SKIP IF DF = 1	LSDF	CF	IF DF = 1, R(P) + 2 → R(P), ELSE CONTINUE
LONG SKIP IF DF = 0	LSNF	C7	IF DF = 0, R(P) + 2 → R(P), ELSE CONTINUE
LONG SKIP IF Q = 1	LSQ	CD	IF Q = 1, R(P) + 2 → R(P), ELSE CONTINUE
LONG SKIP IF Q = 0	LSNQ	C5	IF Q = 0, R(P) + 2 → R(P), ELSE CONTINUE
LONG SKIP IF IE = 1	LSIE	CC	IF IE = 1, R(P) + 2 → R(P), ELSE CONTINUE
CONTROL INSTRUCTIONS			
IDLE	IDL	00 (Note 13)	WAIT FOR DMA OR INTERRUPT; M(R(0)) → BUS
NO OPERATION	NOP	C4	CONTINUE
SET P	SEP	DN	N → P
SET X	SEX	EN	N → X
SET Q	SEQ	7B	1 → Q
RESET Q	REQ	7A	0 → Q
SAVE	SAV	78	T → M(R(X))
PUSH X, P TO STACK	MARK	79	(X, P) → T; (X, P) → M(R(2)), THEN P → X; R(2) - 1 → R(2)
RETURN	RET	70	M(R(X)) → (X, P); R(X) + 1 → R(X), 1 → IE
DISABLE	DIS	71	M(R(X)) → (X, P); R(X) + 1 → R(X), 0 → IE
INPUT - OUTPUT BYTE TRANSFER			
OUTPUT 1	OUT 1	61	M(R(X)) → BUS; R(X) + 1 → R(X); N LINES = 1
OUTPUT 2	OUT 2	62	M(R(X)) → BUS; R(X) + 1 → R(X); N LINES = 2
OUTPUT 3	OUT 3	63	M(R(X)) → BUS; R(X) + 1 → R(X); N LINES = 3
OUTPUT 4	OUT 4	64	M(R(X)) → BUS; R(X) + 1 → R(X); N LINES = 4
OUTPUT 5	OUT 5	65	M(R(X)) → BUS; R(X) + 1 → R(X); N LINES = 5
OUTPUT 6	OUT 6	66	M(R(X)) → BUS; R(X) + 1 → R(X); N LINES = 6
OUTPUT 7	OUT 7	67	M(R(X)) → BUS; R(X) + 1 → R(X); N LINES = 7
INPUT 1	INP 1	69	BUS → M(R(X)); BUS → D; N LINES = 1
INPUT 2	INP 2	6A	BUS → M(R(X)); BUS → D; N LINES = 2
INPUT 3	INP 3	6B	BUS → M(R(X)); BUS → D; N LINES = 3
INPUT 4	INP 4	6C	BUS → M(R(X)); BUS → D; N LINES = 4
INPUT 5	INP 5	6D	BUS → M(R(X)); BUS → D; N LINES = 5

TABLE 4. INSTRUCTION SUMMARY (See Notes 11 through 16) **(Continued)**

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
INPUT 6	INP 6	6E	BUS → M(R(X)); BUS → D; N LINES = 6
INPUT 7	INP 7	6F	BUS → M(R(X)); BUS → D; N LINES = 7

NOTES: (For Table 4)

11. The arithmetic operations and the shift instructions are the only instructions that can alter the DF.

    After an add instruction:
    DF = 1 denotes a carry has occurred
    DF = 0 Denotes a carry has not occurred
    After a subtract instruction:
    DF = 1 denotes no borrow. D is a true positive number
    DF = 0 denotes a borrow. D is two's complement
    The syntax "-(not DF)" denotes the subtraction of the borrow.

12. This instruction is associated with more than one mnemonic. Each mnemonic is individually listed.

13. An idle instruction initiates a repeating S1 cycle. The processor will continue to idle until an I/O request ($\overline{\text{INTERRUPT}}$, $\overline{\text{DMA-IN}}$, or $\overline{\text{DMA- OUT}}$) is activated. When the request is acknowledged, the idle cycle is terminated and the I/O request is serviced, and then normal operation is resumed.

14. Long-Branch, Long-Skip and No Op instructions require three cycles to complete (1 fetch + 2 execute).

    Long-Branch instructions are three bytes long. The first byte specifies the condition to be tested; and the second and third byte, the branching address.

    The long-branch instructions can:
    a. Branch unconditionally
    b. Test for D = 0 or D ≠ 0
    c. Test for DF = 0 or DF = 1
    d. Test for Q = 0 or Q = 1
    e. Effect an unconditional no branch

    If the tested condition is met, then branching takes place; the branching address bytes are loaded in the high-and-low order bytes of the current program counter, respectively. This operation effects a branch to any memory location.

    If the tested condition is not met, the branching address bytes are skipped over, and the next instruction in sequence is fetched and executed. This operation is taken for the case of unconditional no branch (NLBR).

15. The short-branch instructions are two bytes long. The first byte specifies the condition to be tested, and the second specifies the branching address.

    The short branch instruction can:
    a. Branch unconditionally
    b. Test for D = 0 or D ≠ 0
    c. Test for DF = 0 or DF = 1
    d. Test for Q = 0 or Q = 1
    e. Test the status (1 or 0) of the four EF flags
    f. Effect an unconditional no branch

    If the tested condition is met, then branching takes place; the branching address byte is loaded into the low-order byte position of the current program counter. This effects a branch within the current 256-byte page of the memory, i.e., the page which holds the branching address. If the tested condition is not met, the branching address byte is skipped over, and the next instruction in sequence is fetched and executed. This same action is taken in the case of unconditional no branch (NBR).

16. The skip instructions are one byte long. There is one Unconditional Short-Skip (SKP) and eight Long-Skip instructions.

    The Unconditional Short-Skip instruction takes 2 cycles to complete (1 fetch + 1 execute). Its action is to skip over the byte following it. Then the next instruction in sequence is fetched and executed. This SKP instruction is identical to the unconditional no-branch instruction (NBR) except that the skipped-over byte is not considered part of the program.
    The Long-Skip instructions take three cycles to complete (1 fetch + 2 execute).

    They can:
    a. Skip unconditionally
    b. Test for D = 0 or D ≠ 0
    c. Test for DF = 0 or DF = 1
    d. Test for Q = 0 or Q = 1
    e. Test for IE = 1

    If the tested condition is met, then Long Skip takes place; the current program counter is incremented twice. Thus two bytes are skipped over, and the next instruction in sequence is fetched and executed. If the tested condition is not met, then no action is taken. Execution is continued by fetching the next instruction in sequence.

TABLE 5. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES

STATE	I	N	SYMBOL	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{MRD}$	$\overline{MWR}$	N LINES	NOTES
S1	RESET			0 → I, N, Q, X, P; 1 → IE	00	XXXX	1	1	0	17
	Initialize, Not Programmer Accessible			0000 → R	00	XXXX	1	1	0	18
S0	FETCH			MRP → I, N; RP + 1 → RP	MRP	RP	0	1	0	19
S1	0	0	IDL	IDLE	MR0	RO	0	1	0	20, Fig. 6
	0	1 - F	LDN	MRN → D	MRN	RN	0	1	0	Fig. 6
	1	0 - F	INC	RN + 1 → RN	Float	RN	1	1	0	Fig. 4
	2	0 - F	DEC	RN - 1 → RN	Float	RN	1	1	0	Fig. 4
	3	0 - F	Short Branch	Taken: MRP → RP.0 Not Taken; RP + 1 → RP	MRP	RP	0	1	0	Fig. 6
	4	0 - F	LDA	MRN → D; RN + 1 → RN	MRN	RN	0	1	0	Fig. 6
	5	0 - F	STR	D → MRN	D	RN	1	0	0	Fig. 5
	6	0	IRX	RX + 1 → RX	MRX	RX	0	1	0	Fig. 5
	6	1	OUT 1	MRX → BUS; RX + 1 → RX	MRX	RX	0	1	1	Fig. 9
		2	OUT 2						2	Fig. 9
		3	OUT 3						3	Fig. 9
		4	OUT 4						4	Fig. 9
		5	OUT 5						5	Fig. 9
		6	OUT 6						6	Fig. 9
		7	OUT 7						7	Fig. 9
		9	INP 1	BUS → MRX, D	Data from I/O Device	RX	1	0	1	Fig. 8
		A	INP 2						2	Fig. 8
		B	INP 3						3	Fig. 8
		C	INP 4						4	Fig. 8
		D	INP5						5	Fig. 8
		E	INP6						6	Fig. 8
		F	INP7						7	Fig. 8
	7	0	RET	MRX → (X, P); RX + 1 → RX; 1 → IE	MRX	RX	0	1	0	Fig. 6
		1	DIS	MRX → (X, P); RX + 1 → RX; 0 → IE	MRX	RX	0	1	0	Fig. 6
		2	LDXA	MRX → D; RX + 1 → RX	MRX	RX	0	1	0	Fig. 6
		3	STXD	D → MRX; RX - 1 → RX	D	RX	1	0	0	Fig. 5
		4	ADC	MRX + D + DF → DF, D	MRX	RX	0	1	0	Fig. 6
		5	SDB	MRX - D - DFN → DF, D	MRX	RX	0	1	0	Fig. 6
		6	SHRC	LSB(D) → DF; DF → MSB(D)	Float	RX	1	1	0	Fig. 4
		7	SMB	D - MRX - DFN → DF, D	MRX	RX	0	1	0	Fig. 6
		8	SAV	T → MRX	T	RX	1	0	0	Fig. 5

TABLE 5. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (Continued)

STATE	I	N	SYMBOL	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{MRD}$	$\overline{MWR}$	N LINES	NOTES
S1	7	9	MARK	(X, P) → T, MR2; P → X; R2 - 1 → R2	T	R2	1	0	0	Fig. 5
		A	REQ	0 → Q	Float	RP	1	1	0	Fig. 4
		B	SEQ	1 → Q	Float	RP	1	1	0	Fig. 4
		C	ADCI	MRP + D + DF → DF, D; RP + 1	MRP	RP	0	1	0	Fig. 6
		D	SDBI	MRP - D - DFN → DF, D; RP + 1	MRP	RP	0	1	0	Fig. 6
		E	SHLC	MSB(D) → DF; DF → LSB(D)	Float	RP	1	1	0	Fig. 4
		F	SMBI	D - MRP - DFN → DF, D; RP + 1	MRP	RP	0	1	0	Fig. 6
	8	0 - F	GLO	RN.0 → D	RN.0	RN	1	1	0	Fig. 4
	9	0 - F	GHI	RN.1 → D	RN.1	RN	1	1	0	Fig. 4
	A	0 - F	PLO	D → RN.0	D	RN	1	1	0	Fig. 4
	B	0 - F	PHI	D → RN.1	D	RN	1	1	0	Fig. 4
S1#1	C	0 - 3, 8 - B	Long Branch	Taken: MRP → B; RP + 1 → RP	MRP	RP	0	1	0	Fig. 7
#2				Taken: B → RP.1; MRP → RP.0	M(RP + 1)	RP + 1	0	1	0	Fig. 7
S1#1				Not Taken: RP + 1 → RP	MRP	RP	0	1	0	Fig. 7
#2				Not Taken: RP + 1 → RP	M(RP + 1)	RP + 1	0	1	0	Fig. 7
S1#1		5 6 7 C D E F	Long Skip	Taken: RP + 1 → RP	MRP	RP	0	1	0	Fig. 7
#2				Taken: RP + 1 → RP	M(RP + 1)	RP + 1	0	1	0	Fig. 7
S1#1				Not Taken: No Operation	MRP	RP	0	1	0	Fig. 7
#2				Not Taken: No Operation	MRP	RP	0	1	0	Fig. 7
S1#1		4	NOP	No Operation	MRP	RP	0	1	0	Fig. 7
#2				No Operation	MRP	RP	0	1	0	Fig. 7
S1	D	0 - F	SEP	N → P	NN	RN	1	1	0	Fig. 4
	E	0 - F	SEX	N → X	NN	RN	1	1	0	Fig. 4
S1	F	0	LDX	MRX → D	MRX	RX	0	1	0	Fig. 6
		1 2 3 4 5 7	OR AND XOR ADD SD SM	MRX OR D → D MRX AND D → D MRX XOR D → D MRX + D → DF, D MRX - D → DF, D D - MRX → DF, D	MRX	RX	0	1	0	Fig. 6
		6	SHR	LSB(D) → DF; 0 → MSB(D)	Float	RX	1	1	0	Fig. 4

TABLE 5. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (Continued)

STATE	I	N	SYMBOL	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{MRD}$	$\overline{MWR}$	N LINES	NOTES
S1	F	8	LDI	MRP → D; RP + 1 → RP	MRP	RP	0	1	0	Fig. 6
		9	ORI	MRP OR D → D; RP + 1 → RP						
		A	ANI	MRP AND D → D; RP + 1 → RP						
		B	XRI	MRP XOR D → D; RP + 1 → RP						
		C	ADI	MRP + D → DF, D; RP + 1 → RP						
		D	SDI	MRP - D → DF, D; RP + 1 → RP						
		F	SMI	D - MRP → DF, D; RP +1 → RP						
		E	SHL	MSB(D) → DF; 0 → LSB(D)	Float	RP	1	1	0	Fig. 4
S2	DMA IN			BUS → MR0; R0 + 1 → R0	Data from I/O Device	R0	1	0	0	22, Fig. 10
	DMAOUT			MR0 → BUS; R0 + 1 → R0	MR0	R0	0	1	0	22, Fig. 11
S3	INTERRUPT			X, P → T; 0 → IE, 1 → P; 2 → X	Float	RN	1	1	0	Fig. 12
S1	LOAD			IDLE ($\overline{CLEAR}$, $\overline{WAIT}$ = 0)	M(R0 - 1)	R0 - 1	0	1	0	21, Fig. 6

NOTES:

17. IE = 1, TPA, TPB suppressed, state = S1.
18. BUS = 0 for entire cycle.
19. Next state always S1.
20. Wait for DMA or INTERRUPT.
21. Suppress TPA, wait for DMA.
22. IN REQUEST has priority over OUT REQUEST.
23. See “Timing Waveforms” beginning on page 7 and Figures 3 through 12 for “Machine Cyle Timing Waveforms beginning on page 9.

Operating and Handling Considerations

Handling

All inputs and outputs of Intersil CMOS devices have a network for electrostatic protection during handling.

Operating

OPERATING VOLTAGE

During operation near the maximum supply voltage limit care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{DD} - V_{SS} to exceed the absolute maximum rating.

INPUT SIGNALS

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 10mA even when the power supply is off.

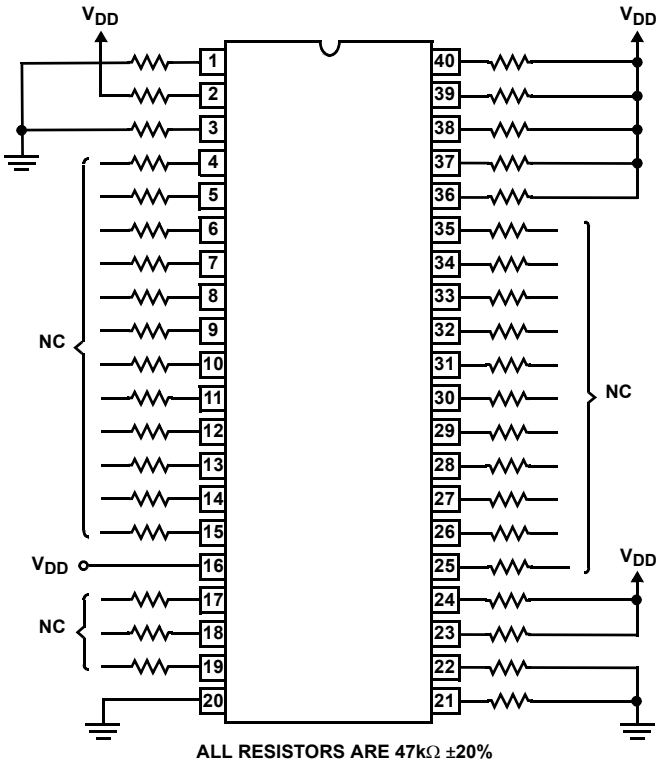
UNUSED INPUTS

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

OUTPUT SHORT CIRCUITS

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

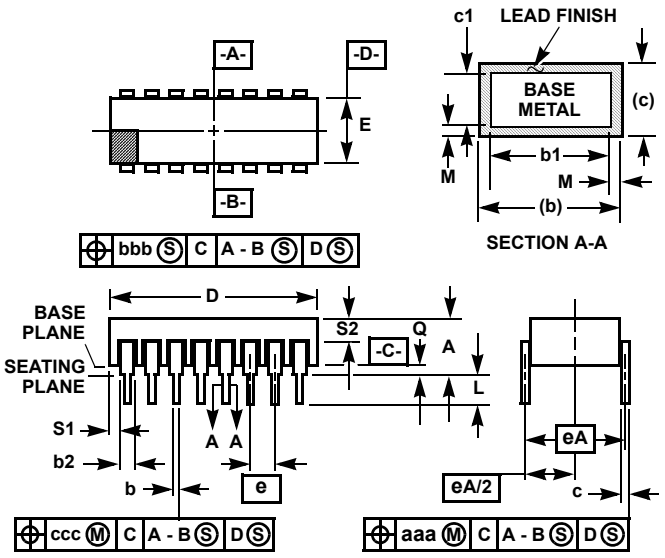
Burn-In Circuit



TYPE	V_{DD}	TEMPERATURE	TIME
CDP1802AC	7V	+125°C	160 Hours

FIGURE 22. BIAS/STATIC BURN-IN CIRCUIT

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

D40.6 MIL-STD-1835 CDIP2-T40 (D-5, CONFIGURATION C)
40 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	2.096	-	53.24	4
E	0.510	0.620	12.95	15.75	4
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	40		40		8

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