Features

- 24 Individual Programmed I/O Pins
- MOTEL Circuit for Bus Compatibility With Many Microprocessors
- Multiplexed Bus Compatible With CDP6805E2 and Competitive Microprocessors
- Data Direction Registers for Ports A, B and C
- Reset Input to Clear Interrupts and Initialize Internal Registers
- Four Port C I/O Pins May Be Used as Control Lines
  - Four Interrupt Inputs
  - Input Byte Latch
  - Output Pulse
  - Handshake Activity
- 15 Registers Addressed as Memory Locations
- Handshake Control Logic for Input and Output Peripheral Operation
- Interrupt Output Pin
- 3V to 5.5V Operating V_{DD}

Description

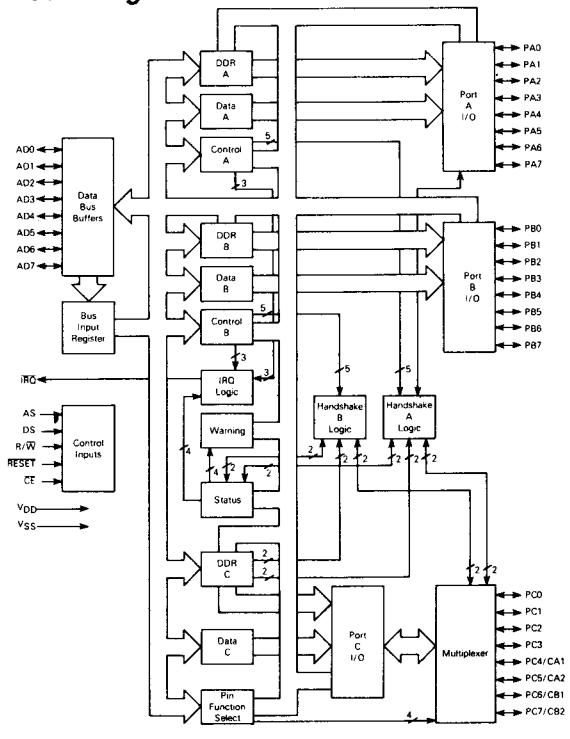
The CDP6823 CMOS parallel interface (CPI) provides a universal means of interfacing external signals with the CDP6805E2 CMOS microprocessor and other multiplexed bus microprocessors. The unique MOTEL circuit on chip allows direct interfacing to most industry CMOS microprocessors, as well as many NMOS MPUs.

The CDP6823 CPI includes three bidirectional 8-bit ports or 24 I/O pins. Each I/O line may be separately established as an input or an output under program control via data direction registers associated with each port. Using the bit change and test instructions of the CDP6805E2, each individual I/O pin can be separately accessed. All port registers are read/write bytes to accomodate read-modify-write instructions.

The CDP6823 is supplied in a 40 lead hermetic dual-in-line sidebrazed ceramic package (D suffix), in a 40 lead dual-in-line plastic package (E suffix) and in a 44 lead plastic chip carrier package (N suffix).

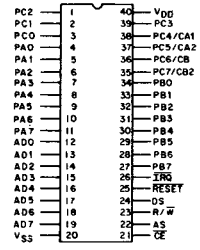
The CDP6823 is equivalent to and is a direct replacement for the industry type MC146823.

Block Diagram

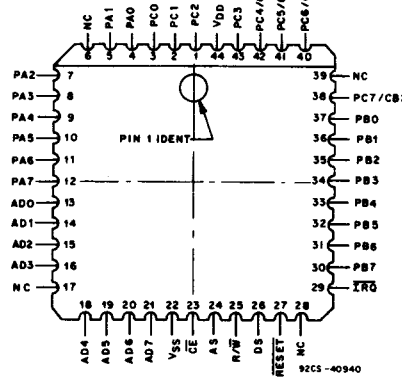


Pinouts

PACKAGE TYPES D AND E
TOP VIEW



PACKAGE TYPE N



5 8-BIT BUS PERIPHERALS

MAXIMUM RATINGS (Voltages reference to V_{SS})

Ratings	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 to +8	V
All Input Voltages	V_{in}	V_{SS} −0.5 to V_{DD} +0.5	V
Current Drain per Pin Excluding V_{DD} and V_{SS}	I	10	mA
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

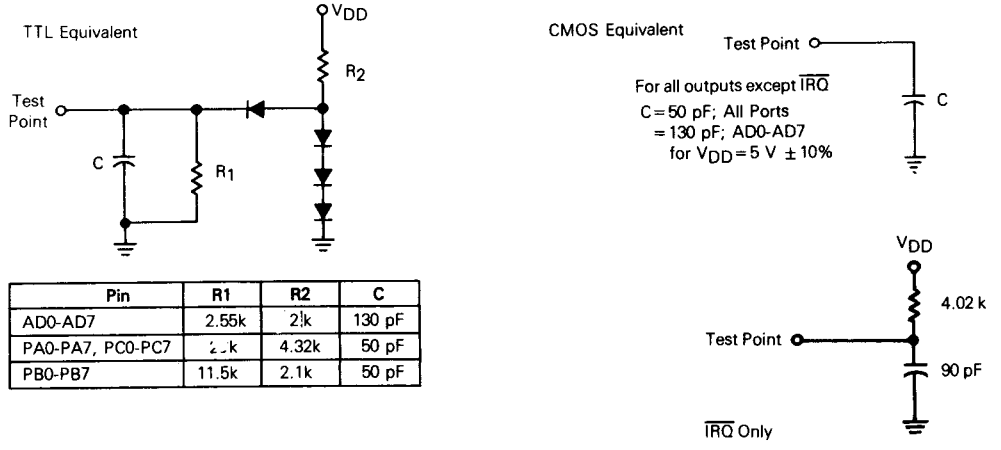
THERMAL CHARACTERISTICS

Characteristics	Symbol	Value	Unit
Thermal Resistance Ceramic Dual-In-Line Plastic Dual-In-Line Plastic Chip-Carrier	θ_{JA}	 50 100 70	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{In}$ or $V_{out}) \le V_{DD}$. Leakage currents are reduced and reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5 Vdc ±10%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C, unless otherwise noted)

Parameter	Symbol	Min	Max	Unit
Output Voltage ($I_{Load} \le 10\ \mu A$)	V_{OL} V_{OH}	− V_{DD} −0.1	0.1 −	V V
Output High Voltage (I_{Load} = −1.6 mA) AD0-AD7 (I_{Load} = −0.2 mA) PA0-PA7, PC0-PC7 (I_{Load} = −0.36 mA) PB0-PB7	 V_{OH} V_{OH} V_{OH}	 4.1 4.1 4.1	 V_{DD} V_{DD} V_{DD}	 V
Output Low Voltage (I_{Load} = 1.6 mA) AD0-AD7, PB0-PB7 (I_{Load} = 0.8 mA) PA0-PA7, PC0-PC7 (I_{Load} = 1 mA) $\overline{IRQ}$	 V_{OL} V_{OL} V_{OL}	 V_{SS} V_{SS} V_{SS}	 0.4 0.4 0.4	 V
Input High Voltage, AD0-AD7, AS, DS, R/$\overline{W}$, $\overline{CE}$, PA0-PA7, PB0-PB7, PC0-PC7 $\overline{RESET}$	V_{IH} V_{IH}	V_{DD} −2.0 V_{DD} −0.8	V_{DD} V_{DD}	V
Input Low Voltage (All Inputs)	V_{IL}	V_{SS}	0.8	V
Quiescent Current − No dc Loads (All Ports Programmed as Inputs, All Inputs = V_{DD} − 0.2 V)	I_{DD}	−	160	μA
Total Supply Current (All Ports Programmed as Inputs, CE = V_{IL}, t_{cyc} = 1 μs)	I_{DD}	−	3	mA
Input Current, $\overline{CE}$, AS, R/$\overline{W}$, DS, $\overline{RESET}$	I_{in}	−	±1	μA
Hi-Z State Leakage, AD0-AD7, PA0-PA7, PB0-PB7, PC0-PC7	I_{TSL}	−	±10	μA



Pin	R1	R2	C
AD0-AD7	2.55k	2.1k	130 pF
PA0-PA7, PC0-PC7	2.55k	4.32k	50 pF
PB0-PB7	11.5k	2.1k	50 pF

Fig. 2 - Equivalent test loads.