iChip™/ iChipSec™

iChip CO710AG
iChipSec CO711AG

Data Sheet

Ver. 1.43

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0.5	May 2003	Changed pin out description. Modified some specifications.
0.7	July 2003	Updated Pin definitions for CS_LAN & 33/66 Frequency select.
1.00	August 2003	Final editing. Added Power consumption figures.
1.02	February 2004	Changed Pin L11 Definition: Canceled H/W pin Power-Save function.
1.05	April 2004	Corrected direction of LANINT signal in block diagram.
1.10	September 2004	Added following sections: Functional Description, Hardware Interface, Interface Timing and Waveforms, Soldering Profile, iChip Designs, Internet Protocol Compliance, and List of Terms and Acronyms.
1.20	March 2005	Corrected iChip Pin numbering. Added supported protocols. Miscellaneous editing.
1.30	August 2005	Added description for new SerialNET Indicator signal
1.40	January 2006	Updated RoHS compliancy; WPA security over WiFi; CO711AG SSL3 support; new remote firmware update method via FTP/HTTP server; parallel interface expected only in 2006.
1.43	July 2006	Revised introduction; added support for the Marvell 88W8385 WiFi chip; updated reflow profile for RoHS.

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1 Introduction

Description

General

iChip™ CO710AG and iChipSec™ CO711AG Internet Controllers™ are high-performance, firmware-based intelligent peripheral devices that provide Internet connectivity solutions for a wide range of embedded devices. The firmware provides Internet communication via 10BaseT and 10/100BaseT Ethernet LANs, 802.11b Wireless LAN with WEP or WPA security, dial-up and wireless modems. CO710AG/CO711AG are packaged in an RoHS compliant 121-ball uBGA form factor. CO710AG/CO711AG firmware is remotely updateable via sockets, FTP/HTTP server or the Web browser.

CO710AG/CO711AG are designed for high-bandwidth applications. The host interface and 33/66 MHz clock support 230 kbits/second in Serial mode. The CO710AG/CO711AG also feature a Power Save mode for saving energy. CO710AG/CO711AG operate in the industrial temperature range.

As an embedded, self-contained Internet engine, iChip acts as mediator device between a host processor and an Internet communications platform. By completely offloading Internet connectivity and standard protocols, it relieves the host from the burden of handling Internet communications. From the perspective of a host device, the complexity of establishing and maintaining Internet-related sessions are reduced to simple, straightforward commands that are entirely dealt with within the domain of iChip/iChipSec.

A serial bus interfaces iChip CO710AG/ iChipSec CO711AG to a device's host processor via an on-chip UART. CO710AG/CO711AG also directly interface an Ethernet controller, a WiFi controller or a serial data modem, through which they support independent communications on the Internet via a dial-up or wireless ISP connection. In addition to supporting dial-up modems, CO710AG/CO711AG also support AMPS, CDMA, CDMA2000, CDPD, GPRS, GSM, IDEN and TDMA cellular modems.

CO710AG/CO711AG support 10BaseT Ethernet LANs with the addition of an external 16-bit Cirrus Logic Crystal LAN CS8900A. It also supports 10/100BaseT LANs with the addition of an SMSC LAN91C111 or ASIX AX88796L Ethernet controller. 802.11b WiFi is supported with an addition of a PCMCIA or CF Wireless LAN module using the Prism 2.5/3.0 WiFi chipset. 802.11b/g WiFi is supported with an addition of an RF module that supports the Marvell 88W8385 WiFi chip. CO710AG/CO711AG also support WEP and WPA security.

Through its host Application Programming Interface (API), iChip and iChipSec accept commands formatted in Connect One's AT+i™ extension to the industry-standard Hayes AT command set. iChip and iChipSec support several levels of status reporting to the host. Commands are available to store and manipulate functional and Internet-related non-volatile parameter data; utilize TCP and UDP sockets; transmit and receive textual Email messages; transmit and receive binary (MIME encoded) Email messages; fetch HTML web pages; manipulate files and directories via FTP; maintain Telnet sessions and download parameter and firmware updates for the host device or iChip/iChipSec itself. iChip and iChipSec include a Web server engine that hosts an internal configuration Web site as well as a customizable application Web site. iChip and iChipSec also include a WAP server to host a WAP site.

When the host CPU issues standard AT commands and the modem platform is selected, iChip/iChipSec gains direct access to the modem, and automatically operates in Transparent mode, emulating a direct host-to-modem environment.

Upon receiving an AT+i command, iChip and iChipSec operate in Internet mode, controls the modem or Ethernet controller, and independently manages standard Internet protocols to transmit and receive messages. iChip/iChipSec provides all the necessary procedures to log onto an ISP, authenticate the user and establish an Internet session.

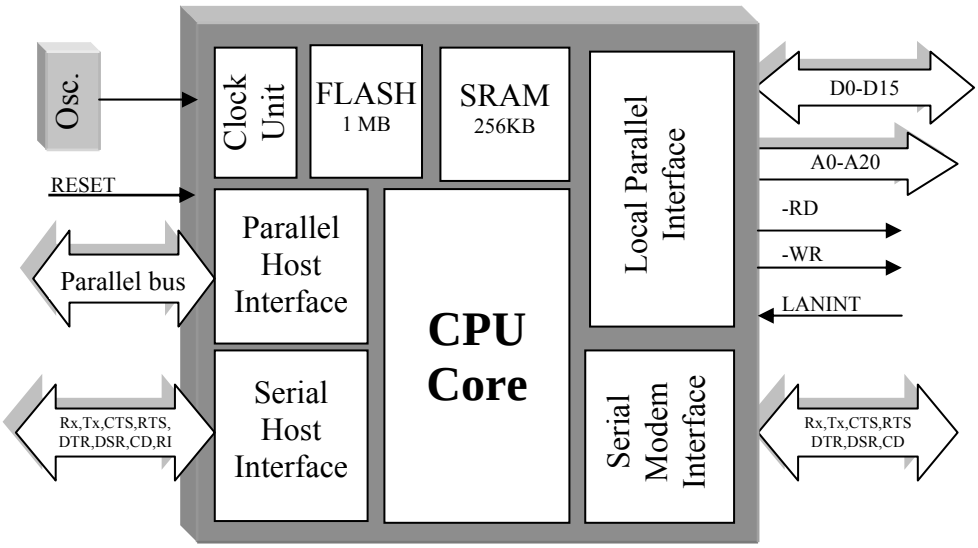
iChipSec CO711AG

iChipSec is a new branch within the iChip family of IP communication coprocessors. It frees up MIPs on the host processor by offloading cryptography, network security and TCP/IP tasks, speeding time-to-market, and minimizing maintenance of new secure embedded designs.

In addition to supporting all the features mentioned above, iChipSec CO711AG supports one secure client socket session or one secure FTP session using an SSL3/TLS1 connection. Only one command is needed to open the SS3/TLS1 socket and an additional command opens the secure FTP session. Just four commands are needed to set the parameters used to define the Cipher suite, the Certificate Authority, the iChipSec Certificate, and the iChipSec Private Key. Cipher suites used for encryption include 3DES, AES-128, AES-256, ARC4, MD5 and SHA-1.

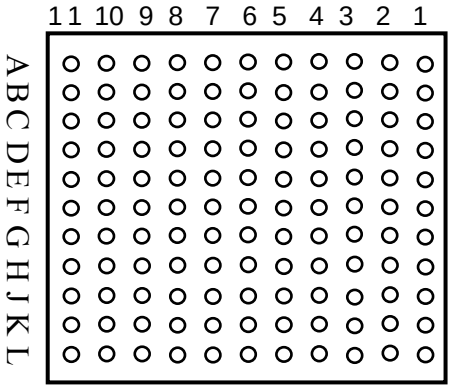
iChipSec uses uses X.509 client and server certificate authentication to perform both client and server authentication and to manage a chain of server certificates. iChipSec supports digital signatures by encrypting RSA public and private keys and using hash algorithms to sign and verify data. iChipSec's flash memory stores the certificate of the Certificate Authority and the private key with its client certificate for client authentication.

2 Functional Block Diagram



Pin Diagram

uBGA-121 Bottom



General Features

- Microprocessor-controllable through a serial connection or parallel bus.
- Supports remote firmware update by host, email, or direct modem-to-modem communications.
- Stores backup copy of previous firmware version.
- 128KB SRAM and 1M flash memory.
- Supports additional external memory.
- Driven by Connect One's "AT+i" extension to the AT command set.
- Stand-alone Internet communication capabilities.
- Binary Base64 encoding and MIME.
- Opens up to 10 simultaneous TCP or UDP sockets and up to 2 Listen (server) sockets.
- Power Save mode.
- 3.3-volts, CMOS technology for I/O and 1.8 volt for core.
- Onboard non-volatile memory stores all functional and Internet-related parameters.
- Supports several layers of status reports.
- Internal self-test procedures.
- Internal "Watchdog" guard circuit.
- Auto baud rate detection.
- Supports up to 230,400 bps in Serial mode.
- Includes hardware and software flow control.
- RoHS compliant 121-ball uBGA package (10 x 10 x 1.2 mm with 0.8 mm ball pitch).

Security Features (iChipSec CO711AG)

- Supports SSL3/TLS1 client sockets and Secure FTP via SSL3/TLS1 socket.
- Supports 3DES, AES-128, AES-256, ARC4, MD5 and SHA-1 Cipher suites.
- Uses RSA public and private key encryption.

General Protocols

- Supports following Internet Protocols: IP, TCP, UDP, DNS, SMTP, POP3, MIME, HTTP, FTP, Telnet, SNTP, SSL3, PING
- Includes embedded Web and WAP server.
- SerialNET mode for serial-to-Internet routing.

Dial-up Features

- Supports dial-up Internet Protocols: PPP, LCP, IPCP, and PAP, CHAP, or Script authentication.
- Supports data modems up to 56 Kbps.
- Supports AMPS, CDMA, CDMA2000, CDPD, GPRS, GSM, IDEN and TDMA wireless modems.
- Stay-on-line feature for multiple send/receive sessions.
- Transparent mode supports direct modem commands.
- Always Online mode with communications "watchdog".

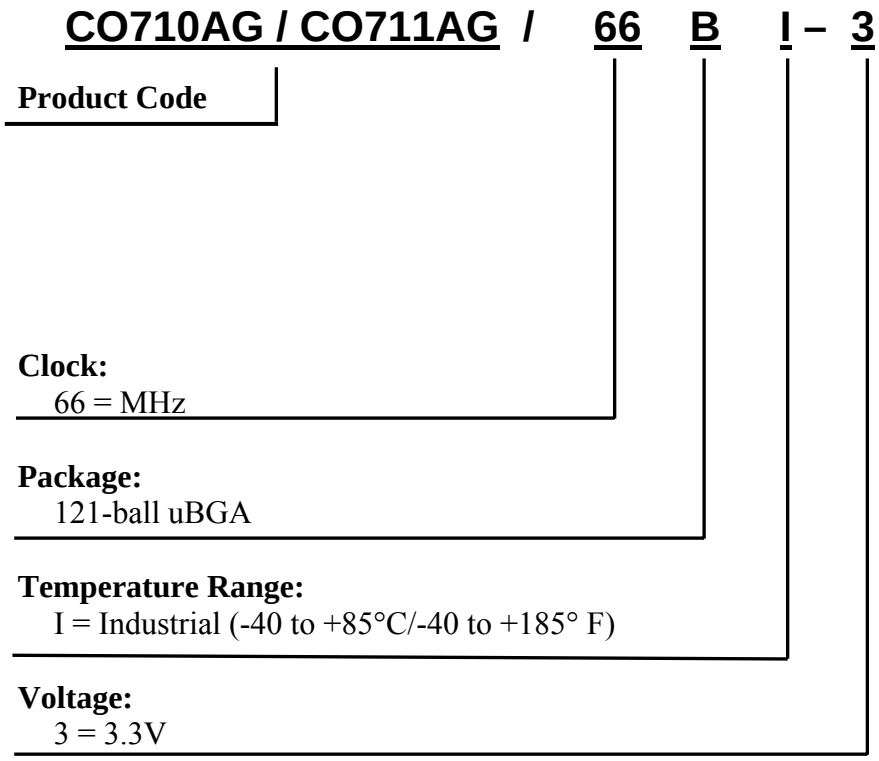
LAN Features

- Supports LAN Internet Protocols: ARP, ICMP, and DHCP.
- Provides 10BaseT Ethernet LAN connectivity via Crystal LAN CS8900A Ethernet controller.
- Provides 10/100BaseT Ethernet LAN connectivity via SMSC LAN91C111 and ASIX AX88796L Ethernet controller.
- Provides 802.11b Wireless LAN connectivity via PCMCIA or CF WiFi card based on Prism 2.5/3.0 chipset
- Provides 802.11b/g Wireless LAN connectivity with the addition of an RF module that supports the Marvell 88W8385 WiFi chip.
- Supports WEP and WPA security for WiFi.

3 Ordering Information

3.1 iChip Order Number

Connect One's standard products are available in several packages and operating ranges. The order number (valid combination) is formed by a combination of the elements below.



4 Functional Description

4.1 Overview

Connect One's CO710AG/CO711AG Internet Controller is an integrated, firmware-driven, self-contained Internet engine that is available in a 121-pin uBGA package. iChip and iChipSec accept simple ASCII commands from a host CPU via a serial communication channel and manages an Internet communication session to send and receive email, Web and WAP pages/files, utilize FTP and Telnet, serve as a serial-to-Internet router, or to manipulate sockets through a linked modem or Ethernet communications platform.

iChipSec CO711AG supports a client SSL3/TLS secure socket, based on RFC2246. It supports the following Cipher suites:

SSL_RSA_WITH_RC4_128_MD5	(0x0004)
SSL_RSA_WITH_RC4_128_SHA	(0x0005)
SSL_RSA_WITH_3DES_EDE_CBC_SHA	(0x000a)

iChipSec CO711AG also supports secure FTP using SSL3/TLS sockets for both Command and Data channels, based on RFC 2228 and the IETF Internet-Draft "Securing FTP with TLS".

For 10BaseT Ethernet applications, CO710AG/CO711AG includes the firmware and pin-out necessary to drive an external Crystal LAN CS8900A Ethernet LAN controller. For 10/100BaseT Ethernet applications, CO710AG/CO711AG includes the firmware and pin-out necessary to drive an external SMSC LAN91C111 or ASIX AX88796L Ethernet LAN controller. For 802.11b Wireless LAN applications, CO710AG/CO711AG includes the firmware and pin-out necessary to drive a PCMCIA or CF WiFi card based on the Prism 2.5/3.0 WiFi chipset. For 802.11b/g Wireless LAN applications, CO710AG/CO711AG provides WiFi connectivity with the addition of an RF module that supports the Marvell 88W8385 WiFi chip. Both WEP and WPA security over WiFi are supported.

iChip and iChipSec contain a non-volatile flash memory to store its firmware and Internet-related operational parameters. Remote firmware and parameter updates are supported through the local host link, by email, using a Web browser or directly through the communications platform.

For the sake of simplicity, the word "iChip" is used in this document to refer to both iChip CO710AG and iChipSec CO711AG, unless the word "iChipSec" is used to refer specifically to CO711AG.

4.2 Technical Specifications

4.2.1 General

iChip constitutes a complete Internet messaging solution for non-PC embedded devices. It acts as a mediator device to completely offload the host processor of Internet-related software and activities. An industry-standard asynchronous serial link connects iChip to the host processor. Programming, monitoring and control are fully supported using Connect One's AT+i™ extension to the standard AT command set.

iChip connects to serial modems and to an Ethernet controller for Internet access. An AT+i command is provided to switch between the serial modem and Ethernet.

4.2.2 Operation

All iChip Internet and parameter operations are controlled by AT+i commands.

4.2.2.1 Transparent Mode

In modem communications mode, iChip defaults to Transparent mode, allowing the host to control the modem device directly. Control is implemented by issuing standard AT commands to iChip. In this mode, iChip transparently echoes the AT commands to the modem, as well as echoing the modem responses back to the host. iChip supports interlacing AT+i and AT commands while the modem is in Command mode. When the modem is put into Data mode by issuing a dial command, Transparent mode is sustained throughout the Data mode session.

4.2.2.2 Command Mode

iChip commands are implemented using the AT+i command set. Command flow exists only on the host serial link between the host and iChip.

4.2.2.3 Internet Mode

iChip enters Internet mode after being issued an Internet command such as to send or receive an email message, open a socket, etc. iChip attempts to establish an Internet connection and carry out the required activity through the communication platform link. While in this mode, AT+i commands are supported to monitor and control the process when needed.

4.2.2.4 Direct Modem Firmware Update Mode

In a modem configuration, issuing an AT+iFU command enters this mode. iChip monitors the modem for an incoming call by detecting the 'RING' response. When called, iChip instructs the modem to answer the call and assumes a YMODEM session to receive a file containing a firmware update. The incoming file contents are downloaded and authenticated. If the new firmware image checks out, the existing firmware is replaced in the on-chip flash memory and iChip is reinitialized.

4.2.2.5 SerialNET Mode

iChip SerialNET mode extends a local asynchronous serial link to a TCP or UDP socket across a LAN or Internet. Its main purpose is to allow simple devices, which normally interact over a serial line, to interact in a similar fashion across a network, without requiring any changes in the device itself. iChip contains a set of associated operational parameters which define the nature of the desired network connection. iChip supports both Server and Client modes in SerialNET mode. AT+i commands are not required to operate SerialNET mode. Thus, SerialNET mode may be used in existing systems with little or no need to modify the application program.

4.2.3 Remote Internet Firmware Update

New firmware may be uploaded from a remote location using standard Internet protocols. iChip accepts firmware updates from a remote FTP or HTTP server, as well as firmware uploads from a remote browser through iChip's Web server.

4.2.4 Local BUS Connection to an Ethernet LAN Controller

iChip interfaces an Ethernet LAN controller connected to its 16-bit local BUS.

4.2.5 Host Connection

iChip can interface a host processor through one of two methods: Serial or Parallel.

4.2.5.1 Host Serial Connection

iChip supports a full-duplex, TTL-level serial communications link with the host processor. Full EIA-232-D hardware flow control, including Tx, Rx, CTS, RTS, DTR, DSR, CD and RI lines, is supported.

iChip supports standard baud rate configurations from 2,400 bps up to 230,400 bps on the host asynchronous serial communications channel. The default baud rate may be changed permanently by using the AT+iBDRF command. Auto baud rate setting is supported for all baud rates except 230,400 bps.

4.2.5.2 Host Parallel Connection (Future implementation)

iChip will support an 8-bit parallel BUS interface with some additional logic. The parallel BUS may be defined as an 80x86 (Intel) BUS or an MC68xxx (Motorola) BUS. This interface will be fully implemented from firmware version 8.01 (expected in 2006).

4.2.6 Serial Connection to Analog Modem

iChip supports a full-duplex, TTL-level serial communications link with the modem device. Full EIA-232-D hardware flow control, including Tx, Rx, CTS, RTS, DTR, DSR and CD lines, is supported. It does not support the RI line.

4.2.7 Hardware and Software Flow Control

Hardware flow control is supported between the host serial connection and iChip. Flow control is programmed via the AT+iFLW command. The default flow control method is set to "Wait/Continue" software flow control (which is similar to XON/XOFF software flow control) between iChip and the host processor.

The hardware flow control method frees the host CPU from monitoring and handling the software flow control. The host can program iChip to either use hardware flow control or "Wait/Continue" software flow control. The flow control mechanism is based on the RTS/CTS signals. The host parallel connection has built-in hardware flow control signals as part of the interface logic.

5 Hardware Interface

iChip CO710AG/CO711AG interface a host CPU in one of two methods: Serial or Parallel. The actual interface depends on the state of the –SER/PAR pin.

5.1 Serial Host Interface

The host interface is a serial DTE interface. Speeds of 2400, 4800, 9600, 19200, 38400, 57600, 115200 and 230400 bps are supported in the following data format:

Parity	Data Length (No. of Bits)	No. of Stop Bits	Transmission Length (No. of Bits)
None	8	1[1]	10

Table 5-1 Host Data Format

5.2 Parallel Host Interface [2]

In Parallel interface mode, iChip connects to a host CPU through a parallel interface using a PAL (i.e., Altera "EPM7032AEC44"). The host parallel BUS may be an 80x86 (Intel) or a 68K (Motorola) BUS. With some small changes to the PAL, the user may customize an interface to any other BUS architecture. iChip is connected to the interface PAL through the following signals:

- **PCS**: Parallel chip select signal. When PCS is HIGH, the PAL is selected.
- **-RD**: When –RD is LOW, iChip reads data from PAL.
- **-WR**: When –WR is LOW, iChip writes data to PAL.
- **D0-D7**: Bi-directional data BUS.
- **-PRES**: Parallel reset. When LOW, generates a reset signal to the parallel interface.
- **-PERR**: Parallel error. When LOW, indicates a parallel interface error.
- **POBE**: Parallel Output Buffer Empty. When HIGH, indicates that the output buffer is empty and iChip may send additional data to host. When iChip sends a data byte, this signal goes LOW until the host reads the data.
- **PIBF**: Parallel Input Buffer Full. When HIGH, indicates that the input buffer is full and iChip may read a data byte from the host. When iChip reads the data byte, this signal goes LOW.

Notes: 1: When hardware flow control is enabled, the iChip transmitter will add an additional stop bit.
2: Parallel interface mode is available only from iChip firmware version 8.01.

5.2.1 80x86 BUS

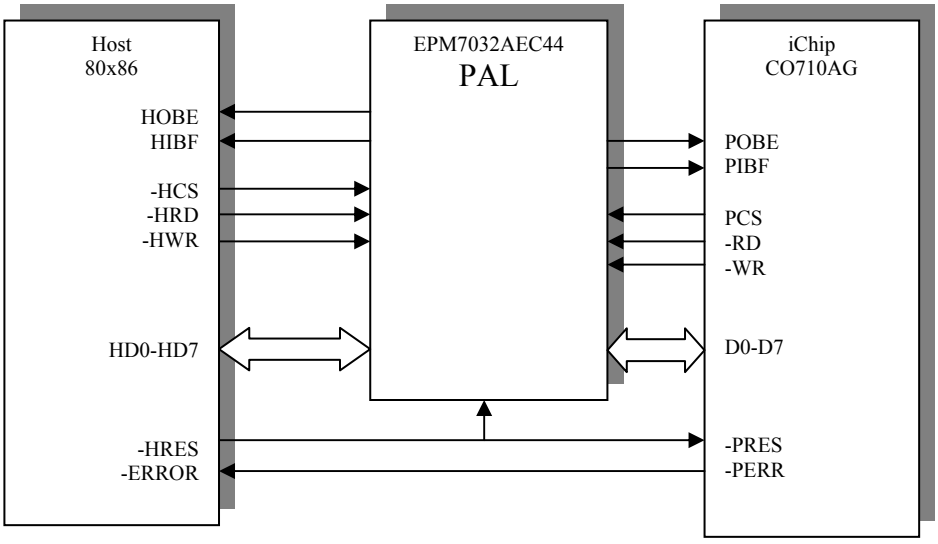


Figure 5-1 Interface to an 80x86 Type BUS

This BUS type includes the following signals:

- **-HCS**: Host Chip-Select signal. When -HCS is LOW, PAL is selected.
- **-HRD**: Host Read Data. When –HRD is LOW, a data byte is read from the PAL.
- **-HWR**: Host Write Data. When –HWR is LOW, a data byte is written to the PAL.
- **HD0 – HD7**: Bi-directional Host data BUS.
- **-HRES**: Parallel reset. A LOW generates a reset signal to the parallel interface. This pin may be connected to an 80x86 output port.
- **-HERR**: Parallel error. A LOW indicates a parallel interface error. This pin may be connected to an input port on the 80x86.
- **HOBE**[1]: Host Output Buffer Empty. When HIGH, indicates that the output buffer is empty and the host may send a data byte to iChip. When the Host sends a data byte, this signal goes LOW until iChip reads the data.
  This signal may be connected to an interrupt or I/O pin on the 80x86.
- **HIBF**[1]: Host Input Buffer Full. When HIGH, indicates that the input buffer is full and the host may read a data byte from iChip. When the host reads the data, this signal goes LOW. This pin may be connected to an interrupt or I/O pin on the 80x86.

Note 1: HOBE and HIBF complement PIBF and POBE respectively.

5.2.2 MC68xxx BUS

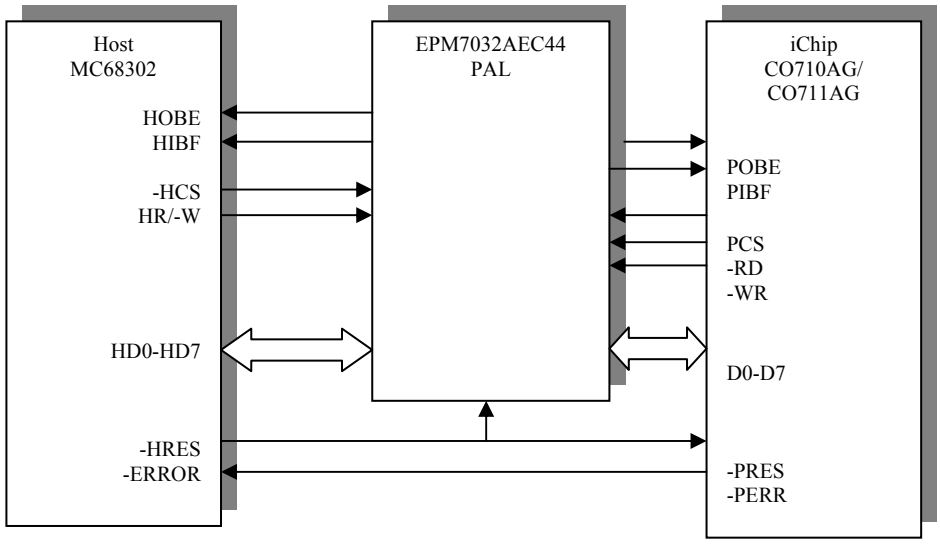


Figure 5-2 Interface to an MC68xxx Type BUS

This BUS type includes the following signals:

- **-HCS**: Host Chip-Select signal. When -HCS is LOW, PAL is selected.
- **-HR/-W**: Host read/write data from/to iChip. When HR/-W is LOW, it indicates a write cycle; otherwise it is a read cycle.
- **HD0 – HD7**: Bi-directional Host data BUS.
- **-HRES**: Parallel reset. A LOW generates a reset signal to the parallel interface. This pin may be connected to a MC68xxx output port.
- **-HERR**: Parallel error. A LOW indicates a parallel interface error. This pin may be connected to an input port on the 80x86.
- **HOBE**[1]: Host Output Buffer Empty. When HIGH, indicates that the output buffer is empty and the host may send a data byte to iChip. When the Host sends a data byte, this signal goes LOW until iChip reads the data. This signal may be connected to an interrupt or I/O pin on the MC68xxx.
- **HIBF**[1]: Host Input Buffer Full. When HIGH, indicates that the input buffer is full and the host may read a data byte from iChip. When the host reads the data, this signal goes low. This pin may be connected to an interrupt or I/O pin on the MC68xxx.

Note 1: HOBE and HIBF complement PIBF and POBE respectively.

5.3 LAN Interface

iChip directly interfaces an Ethernet LAN MAC/PHY device on its 16-bit local BUS. Currently iChip supports the Crystal LAN CS8900A Ethernet controllers for 10BaseT and SMSC LAN91C111 and ASIX AX88796L Ethernet controllers for 10/100BaseT. For 802.11bWireless LAN applications, iChip CO710AG/CO711AG need some minor glue logic to connect to a PCMCIA or CF WiFi card based on the Prism 2.5/3.0 802.11b WiFi chipset. For 802.11b/g Wireless LAN applications, CO710AG/CO711AG provides WiFi connectivity with the addition of an RF module that supports the Marvell 88W8385 WiFi chip.

5.4 Serial Modem Interface

iChip includes a dedicated port to interface a serial modem.

The modem interface is a serial DCE interface. Speeds of 2400, 4800, 9600, 19200, 38400, 57600, 115200 and 230400 bps are supported in the following data format:

Parity	Data Length (No. of Bits)	No. of Stop Bits	Transmission Length (No. of Bits)
None	8	1	10

Table 5-2 Modem Data Format

Actual baud rate may be preprogrammed or dynamically defined as equal to the auto baud rate detected on the serial host interface (when the iChip operates in Serial mode). When iChip operates in Parallel mode, the modem interface baud rate must be preprogrammed.

5.5 Dual Interface

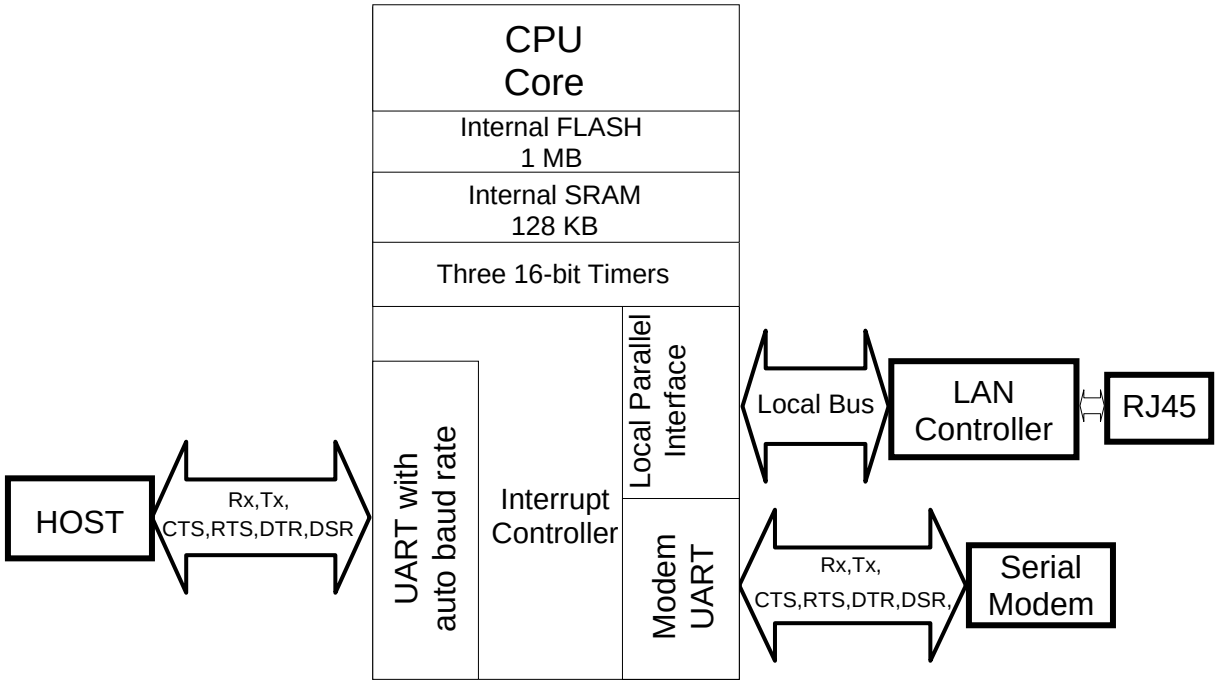


Figure 5-3: iChip CO710AG/CO711AG with LAN and Serial Modem Interface

6 Pin Descriptions

6.1 iChip CO710AG/CO711AG Pin Assignments

11	10	9	8	7	6	5	4	3	2	1	
TXDM	RXDM	VDDi/o	-DTRM	GND	GND	NC	-CS_LAN	-WAIT	-CSE	GND	A
$\overline{33}$/66_FSEL	-RTSM	GND	CLKIN	CLKO/HBT /Z6	NC	-WR	VDDcore	GND	A0	A1	B
MSEL	Z9	-BHE	-RES	NC	GND	A2	VDDi/o	-SNI	GND	A4	C
RXDH	Z8	TXDH	-RTSH/ -PERR	A3	NC	NC	NC	A5	A7	A6	D
GND	-CTSH/ PIBF	NC	VDDi/o	A8	-RD	LBO	LBI	NC	VDDi/o	VDDi/o	E
Z2/POBE	-CTSM	LANINT	VDDi/o	D11	D9	D2	NC	VDDi/o	A10	A9	F
VDDcore	VDDi/o	-DTRH	A14	D10	A11	D5	D0	GND	A13	A12	G
-DSRM	ABDD	-RIH/ -SER	A15	D13	D7	D4	D1	GND	GND	GND	H
Z5	-DSRH/ -PRES	A16	D12	NC	D8	D6	Z1/PCS	A19	A17	VDDi/o	J
GND	GND	D15	D14	NC	NC	GND	NC	VDDi/o	-CDM	A18	K
Z3	Z4	-CDH/ -RCV	VDDi/o	D3	NC	NC	NC	-SER/PAR	VDDcore	A20	L

Figure 6-1: Pinout for 121-ball uBGA Package (Bottom View)

6.2 iChip Pin Functional Descriptions

6.2.1 Local BUS Signals

<table>
<tr><th>Signal</th><th>Type</th><th>Pin No.</th><th>Description</th></tr>
<tr><td>A[20:0]</td><td>O</td><td>L1,J3,K1,
J2,J9,H8,
G8,G2,G1,
G6,F2,F1,
E7,D2,D1,
D3,C1,D7,
C5,B1,B2</td><td>Address BUS: These pins supply addresses to the system.</td></tr>
<tr><td>D[15:0]</td><td>O/I</td><td>K9,K8,H7,
J8,F7,G7,
F6,J6,H6,
J5,G5,H5,
L7,F5,H4,
G4</td><td>Data BUS: These pins supply data to/from the system.</td></tr>
<tr><td>-BHE</td><td>O</td><td>C9</td><td>BUS HIGH Enable: This pin and the least-significant address bit (A0) indicate to the system, which bytes of the data BUS (upper, lower, or both) participate in a BUS cycle. The -BHE and A0 pins are encoded as shown in the table below.
<table>
<tr><th>-BHE</th><th>A0</th><th>Type of BUS cycle</th></tr>
<tr><td>0</td><td>0</td><td>Word Transfer</td></tr>
<tr><td>1</td><td>0</td><td>Even Byte Transfer</td></tr>
<tr><td>0</td><td>1</td><td>Odd Byte Transfer</td></tr>
<tr><td>1</td><td>1</td><td>N/A</td></tr>
</table></td></tr>
<tr><td>-RD</td><td>O</td><td>E6</td><td>READ: This pin indicates that iChip is performing a read cycle.</td></tr>
<tr><td>-WR</td><td>O</td><td>B5</td><td>WRITE: This pin indicates that iChip is performing a write cycle.</td></tr>
<tr><td>-WAIT</td><td>I</td><td>A3</td><td>WAIT: when this pin is LOW, the CPU adds a wait state to each memory cycle. This pin should be pulled up to VDDi/o.</td></tr>
</table>

Signal	Type	Pin No.	Description
LBO	O	E5	Loop Back Out. Must connect to LBI.
LBI	I	E4	Loop Back Input. Must connect to LBO.
-CS_LAN	O	A4	Chip Select for external LAN controller.
-CSE	O	A2	Chip Select Extended this pin is reserved for future use and should be NC (Not Connected).

6.2.2 Miscellaneous Signals

Signal	Type	Pin No.	Description
MSEL	I	C11	Mode Select: • When this pin is held LOW during power up for at least 5 seconds, iChip will automatically enter the Boot loader's monitor mode. • During a firmware update procedure, when an external modem dials to the iChip, pulling this pin down to LOW will cause iChip to immediately answer the call and begin the update session. • When this pin is held LOW during power up for less than 5 seconds, it forces iChip into auto baud rate detection. When not used **must** be pulled up to VDDi/o.
-RES	I	C8	RESET: When -RES is LOW, iChip immediately terminates its present activity and clears its internal logic. -RES must be held LOW for at least 1 ms after power arrive to 90%. This input is provided with a Schmidt trigger to facilitate power-on reset generation via an RC network.
CLKIN	I	B8	Input clock. Selectable to 33MHz or 66MHz via pin B11.
CLKO/HBT/ Z6	O	B7	AT+i Configurable Pin: **CLKO** (default): Clock Output. This pin provides a clock-out to the system at the same frequency as CLKIN. During reset the clock out is disabled. **HBT**: Heartbeat. Provides a 50% duty cycle, 40 mSec frequency square wave when iChip firmware is properly running. In the future, it may be changed to a GPIO. This pin is configurable with the AT+iPN44 command (see AT+i Programmers Manual).
ABDD	I	H10	Auto baud rate detect. Must be connected to RXDH (D11) pin to support auto baud rate.

Signal	Type	Pin No.	Description
LANINT	I	F9	LAN Interrupt. Indicates that LAN controller has information available for iChip. Level depends on external MAC.
-SER/PAR	I	L3	Serial/Parallel mode select. This pin is sampled on the rising edge of the –RES signal. If it is LOW, iChip functions in Serial mode. Otherwise, it functions in Parallel mode.
-SNI	O	C3	**SerialNET Indicator.** This pin is used to indicate that iChip is in SerialNET mode. It is LOW when iChip is in SerialNET mode and otherwise HIGH.
Z1/PCS	I/O	J4	**In Serial mode**, Z1 is available as a GPIO for future use and should be left Not Connected. **In Parallel mode**, PCS is used as a chip-select for the parallel interface PAL.
Z2/POBE	I/O	F11	**In Serial mode**, Z2 is available as a GPIO for future use and should be left Not Connected. **In Parallel mod**e, POBE is used as the Parallel Output Buffer Empty signal. When HIGH, iChip may send a parallel data byte to the host.
Z[9-8] Z[5-3]	I/O	C10,D10 J11, L10, L11	General Purpose I/O (GPIO) for future use. These pins should be NC (Not Connected).
GND	P	A1,A6,A7, B3,B9,C2, C6,E11,G3, H1,H2,H3, K5,K10,K11	Ground: iChip Ground signal.
VDDcore	P	B4,G11,L2	Power Supply: This pin supplies power (+1.8V) to core of iChip.

Signal	Type	Pin No.	Description
VDD I/O	P	A9,C4,E1, E2,E8,F3, F8,G10,J1, K3,L8	Power Supply: This pin supplies power (+3.3V) to I/O pin of iChip.
$\overline{33}$/66_FSEL	I	B11	Oscillator Frequency Select. Connect to GND when CLKIN (Pin B8) is connected to a 33MHz oscillator. Connect to VDDi/o when CLKIN (Pin B8) is connected to a 66MHz oscillator.
NC	---	A5,B6,C7, D4,D5,D6, E3,E9,F4, J7,K4,K6, K7,L4,L5, L6	NC (Not Connected) Pins.

6.2.3 Host Serial Interface Signals

Signal	Type	Pin No.	Description
TXDH	O	D9	Transmit Data Host: This pin supplies asynchronous serial transmit data to the host.
RXDH	I	D11	Receive Data Host: This pin supplies asynchronous serial receive data from the host. When not used, this pin should be connected to VDDi/o. Must be connected to ABDD (H10) pin to support auto baud rate.
-CTSH/PIBF	I	E10	**In Serial mode**, Clear-to-Send Host: -CTSH is active only when host hardware flow control is enabled. When -CTSH is LOW, flow control is enabled for the host serial port, i.e., iChip may transmit to the host. When -CTSH is HIGH, the iChip transmitter holds its data in the serial port transmit register. -CTSH is sampled only at the beginning of a frame transmission. If -CTSH is raised while a character frame is being transmitted, that frame will be completed. Connect -CTSH to -RTSH when not in use. **In Parallel mode**, Parallel Input Buffer Full: when HIGH, indicates that the host has sent a data byte which has not yet been read.
-RTSH/-PERR	O	D8	**In Serial mode**, Ready-to-Send Host: -RTSH is active only when host hardware flow control is enabled. When -RTSH is LOW, flow control is enabled for the host serial port, i.e., the host may transmit to iChip. When -RTSH is HIGH, iChip indicates that its receiver is busy and cannot receive data from host. Connect -RTSH to -CTSH when not in use. **In Parallel mode**, Parallel Error: When LOW, indicates to the host that an error has occurred in the parallel interface circuit.
-DSRH/-PRES	I	J10	**In Serial mode**, Data Set Ready Host: when -DSRH is LOW, it indicates that the host is attached and ready to communicate with iChip. Connect -DSRH to GND when not in use. **In Parallel mode**, Parallel Reset: when LOW, generates a reset to the parallel interface.

Signal	Type	Pin No.	Description
-DTRH	O	G9	Data Terminal Ready Host: When -DTRH is LOW, it indicates to the host that iChip is attached and ready to communicate.
-CDH/-RCV	O	L9	In dial-up mode, this pin functions as –CDH. In LAN mode, it functions as –RCV. **Carrier Detect Host**: This pin indicates to the host that the modem communication device detects a carrier signal. **Receive LAN Packet**: when LOW, indicates that iChip may receive a data packet from the LAN Controller. During firmware update, -CDH and -RIH are used to display the firmware update status.
-RIH/-SER	O	H9	In dial-up mode, this pin functions as –RIH. In LAN mode, it functions as –SER. Ring Indicator Host: This pin indicates to the host that the modem communication device detects a Ring signal. Serial Indicator Host: when LOW, indicates that iChip may receive a legal character from the host. During firmware update, -CDH and -RIH are used to display the firmware update status.

6.2.4 iChip Serial Modem Signals

Signal	Type	Pin No.	Description
TXDM	O	A11	Transmit Data Modem: This pin provides asynchronous serial transmit data to the modem from the serial port. On reset, this pin must remain HIGH.
RXDM	I	A10	Receive Data Modem: This pin provides asynchronous serial receive data from the modem to the asynchronous modem serial port. When this pin is not used, connect it to VDDi/o.
-CTSM	I	F10	Clear-to-Send Modem: -CTSH is active only when modem hardware flow control is enabled. When -CTSM is LOW, flow control is enabled for the modem serial port, i.e., iChip may transmit to the modem. When -CTSM is HIGH, the iChip transmitter holds its data in the serial port transmit register. Connect -CTSM to -RTSM when not in use.
-RTSM	O	B10	Ready-to-Send Modem: -RTSM is active only when modem hardware flow control is enabled. When -RTSM is LOW, flow control is enabled for the modem serial port, i.e., the modem may transmit to iChip. When -RTSM is HIGH, iChip indicates that its receiver is busy and cannot receive data from modem. Connect -RTSM to -CTSM when not in use.
-DSRM	I	H11	Data Set Ready Modem: When -DSRM is LOW, it indicates that the modem is attached and ready to communicate with iChip. Connect -DSRM to GND when not in use.
-DTRM	O	A8	Data Terminal Ready Modem: When -DTRM is LOW, it indicates to the modem that iChip is attached and ready to communicate.
-CDM	I	K2	Carrier Detect Modem: This pin indicates to iChip that the modem detects a carrier signal.

7 Electrical Specifications

7.1 Environmental Specifications

7.1.1 Absolute Maximum Ratings

Parameter	Rating
Voltage at any pin with respect to ground	-0.3 to +3.6 Volts
Operating temperature	-40°C to 85°C (-40°F to 185°F)
Storage temperature	-60°C to 150°C (–76°F to 302°F)

Table 7-1 Environmental Specifications – Maximum Ratings

7.1.2 DC Operating Characteristics

Parameter	Min	Typical	Max	Units
VDDi/o	3.0	3.3	3.6	Volts
VDDcore	1.65	1.8	1.95	Volts
High-level Input	2.0		VDDi/o+0.3	Volts
Low-level Input	-0.3		0.8	Volts
High-level Output[1] @16mA	VDDi/o-0.4			Volts
High-level Output[2] @8mA	VDDi/o-0.4			Volts
High-level Output[3] @2mA	VDDi/o-0.4			Volts
High-level Output[4] @0mA	VDDi/o-0.2			Volts
Low-level Output[1] @16mA			0.4	Volts
Low -level Output[2] @8mA			0.4	Volts
Low -level Output[3] @2mA			0.4	Volts
Low -level Output[4] @0mA			0.2	Volts
Input leakage current			10	µA
Power supply current from VDDcore (Operating Mode)[5]		10		mA
Power supply current from VDDcore (Power Save Mode)[5]		2.4		mA
Power supply current from VDDi/o (Operating Mode)[5]		50		mA
Power supply current from VDDi/o (Power Save Mode)[5]		18		mA
Input Capacitance			6	pF

Table 7-2 DC Operating Characteristics

Notes: [1] On -RD,-WR and -BHE pins.
[2] On D[15-0], A[20-0], -CS0 and –CS1 pins.
[3] All other pins.
[4] All output pins.
[5] CLKIN=33.333MHz.

7.2 Interface Timing and Waveforms

7.2.1 Switching Characteristics

Parameter	Symbol	Min.	Typical	Max.	Units
CLKIN frequency	Fclk	33.33	33.333	33.336	MHz
CLKIN period	Tclk		1/Fck		us
CLKIN falling to address or chip select change	Txfac	3.7		8.6	ns
CLKIN rising to read active	Txrra	3.8		7.3	ns
CLKIN falling to read inactive	Txfri	4.1		8.6	ns
Data setup before read high	Tdsbrh	8			ns
Data setup after read high	Tdsarh	3.1			ns
CLKIN rising to write active	Txrwa	3.8		6.3	ns
CLKIN rising to data valid	Txrdv	4.2		7.5	ns
CLKIN rising to write inactive	Txrwi	4.2		6.7	ns
Data out valid after write high	Tdovaw	2.2			ns
CLKIN fall time [1]	Tckhl			5	ns
CLKIN rise time [2]	Tcklh			5	ns
CLKIN LOW time	Tclck	13.5	15	16.5	ns
CLKIN HIGH time	Tchck	13.5	15	16.5	ns
CLKIN to CLKO skew	Tcico	4.4		6.7	ns
Reset pulse	Trst	1			ms
RXDM high before rising reset	Trmbr	2			us
RXDM high after rising reset	Trmar	2			us
Read rising to input parallel buffer full	Trrbf	0			ns
Write rising to output parallel buffer empty	Twrbe	0			ns

Table 7-3 Switching Characteristics

Notes: All switching timing when CLKIN is 33.333MHz.
[1] Fall time is from 2.3V to 1V.
[2] Rise time is from 1V to 2.3V.

7.2.2 Local BUS Read Cycle

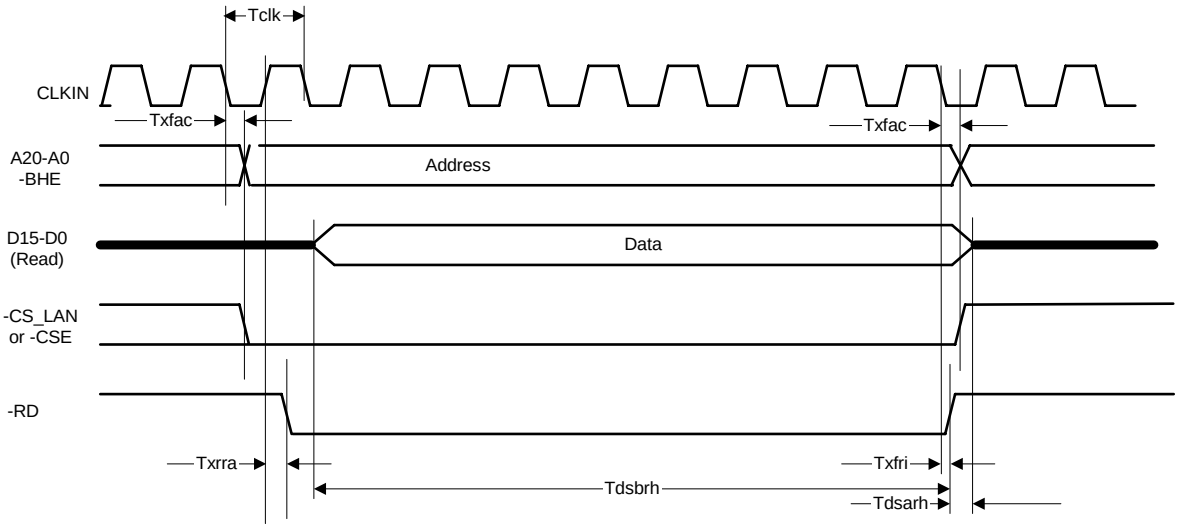


Figure 7-1 Local BUS Read Cycle

7.2.3 Local BUS Write Cycle

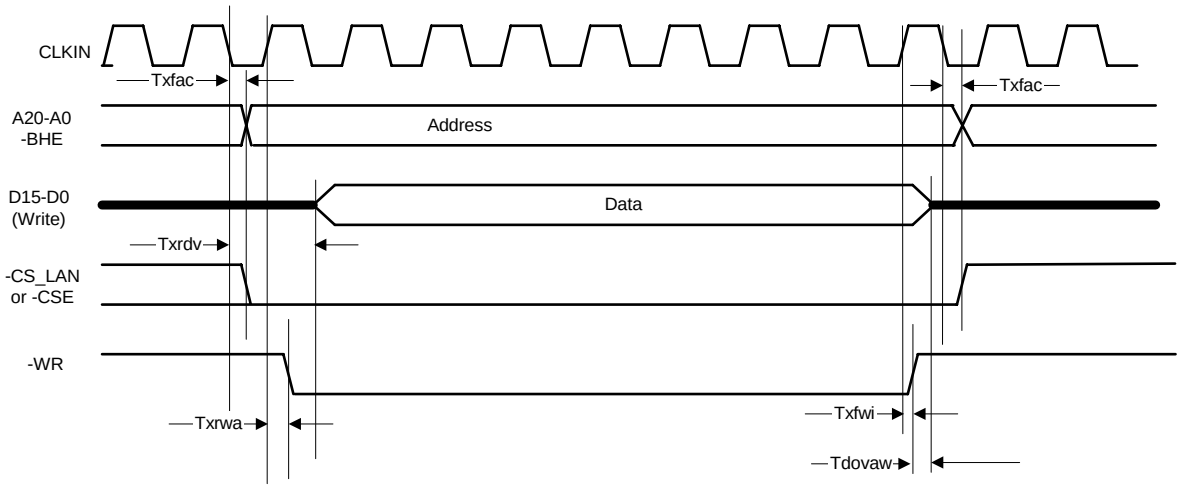


Figure 7-2 Local BUS Write Cycle

7.2.4 Clock Waveform

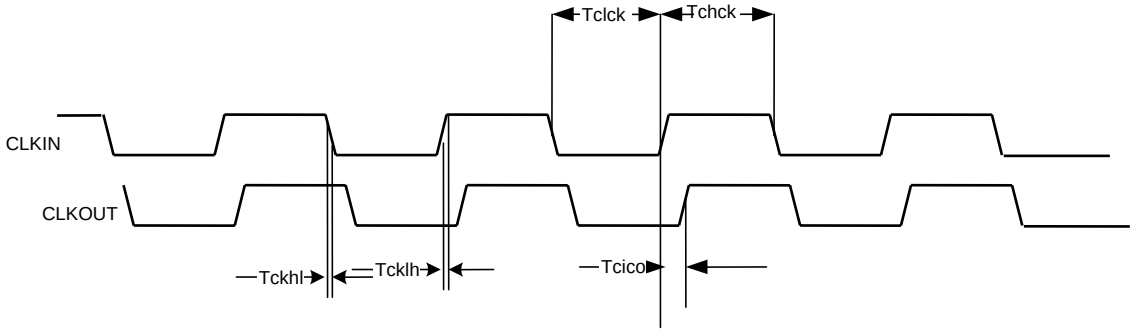


Figure 7-3 Clock Waveform

7.2.5 Reset Timing

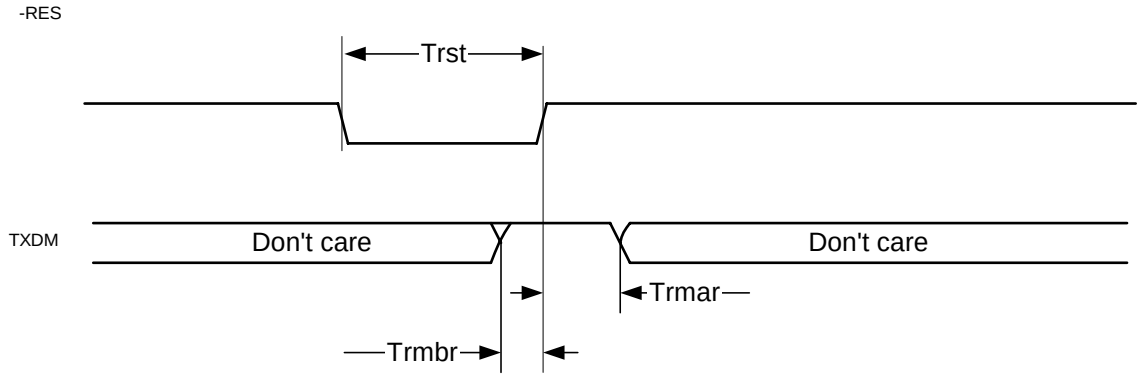


Figure 7-4 Reset Timing

7.2.6 Parallel BUS Read Cycle

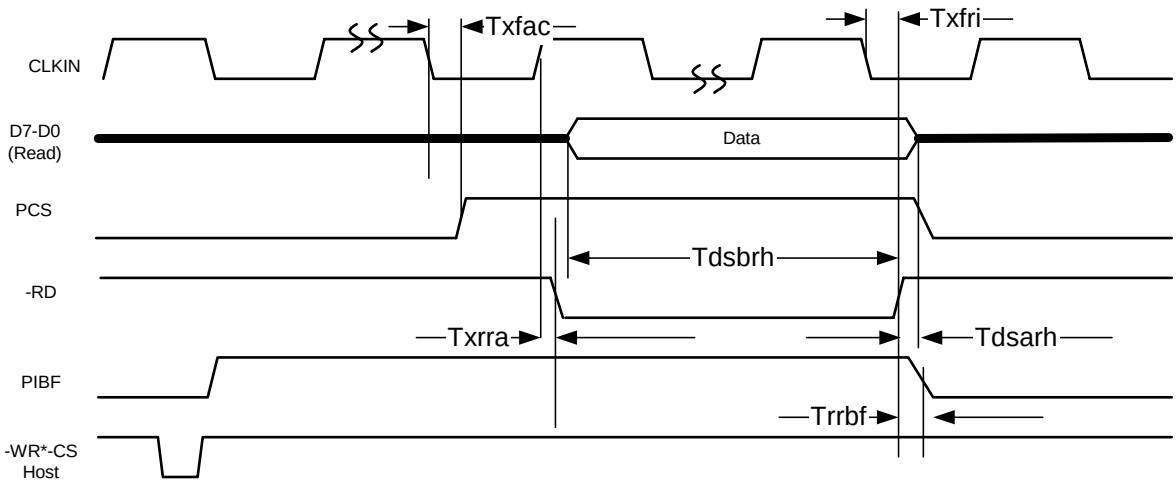


Figure 7-5 Parallel BUS Read Cycle

7.2.7 Parallel BUS Write Cycle

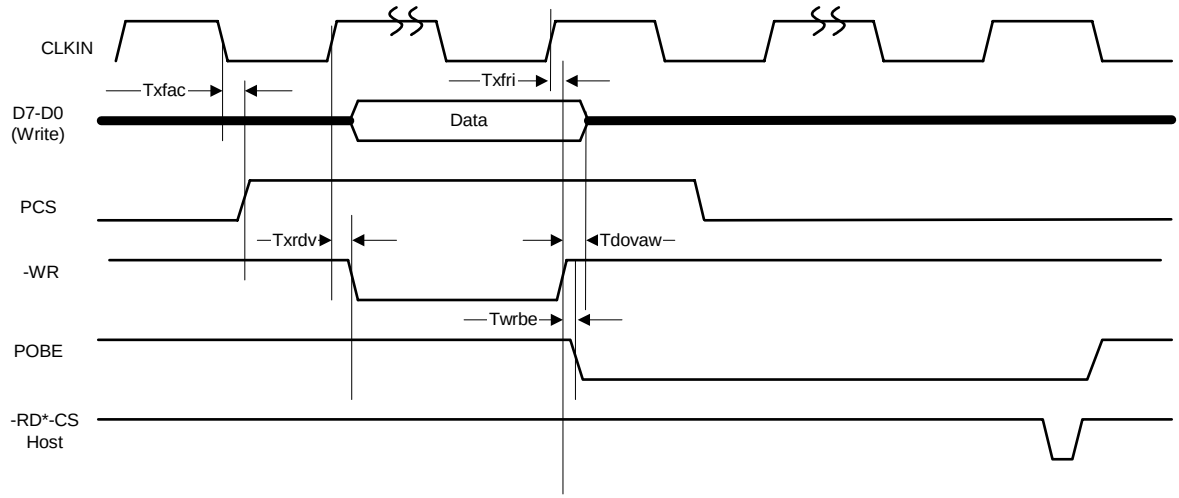


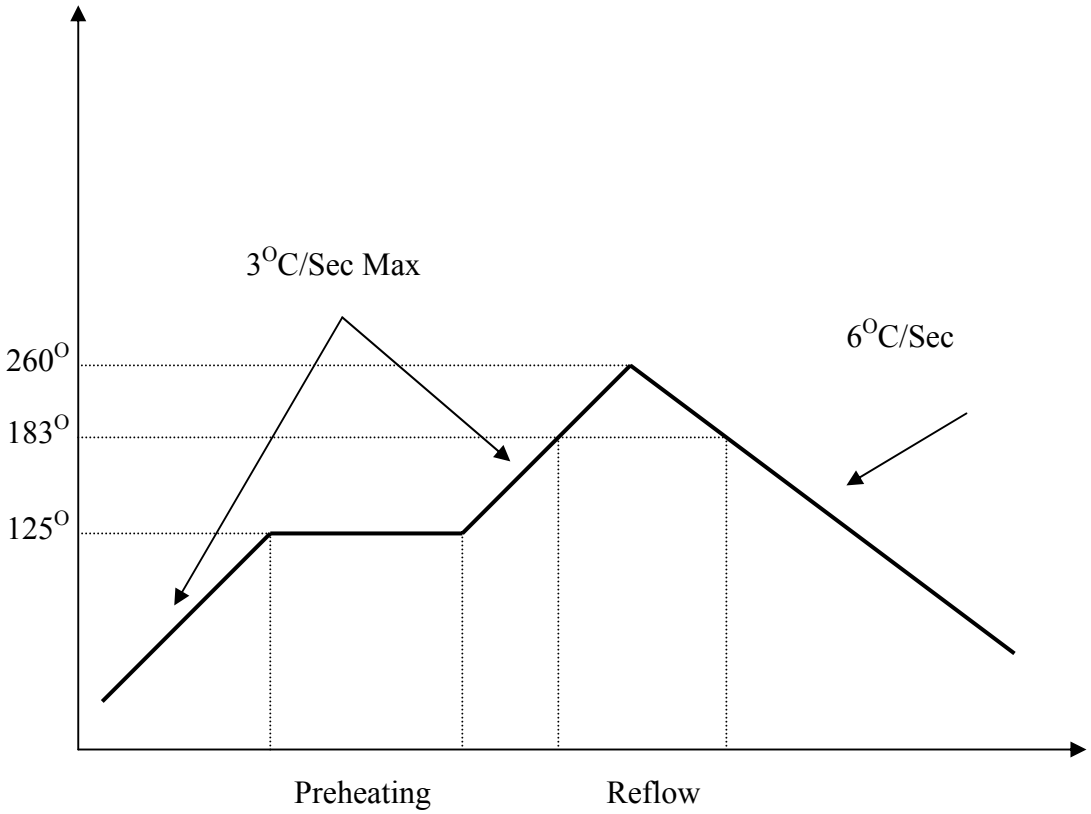
Figure 7-6 Parallel BUS Write Cycle

8 Recommended Soldering Profile

Based on JEDEC J-STD-20C:

	Convection or IR/Convection
Average Ramp-up rate (183ºC to Peak)	3ºC/sec. Max.
Preheat temperature 125ºC ± 25ºC	180 sec. Max.
Temperature maintained above 183ºC	60 sec. to 150 sec.
Time within 5ºC of actual peak temperature	20 sec. to 40 sec.
Peak temperature range	260ºC
Ramp down rate	6ºC/sec.
Time 25ºC to peak temperature	8 min. max.

Table 8-1 Recommended Soldering Profile



Note: ***A maximum of three reflow passes is allowed per component. It is recommended to use a soldering temperature higher than 250°C***

9 Mechanical Dimensions

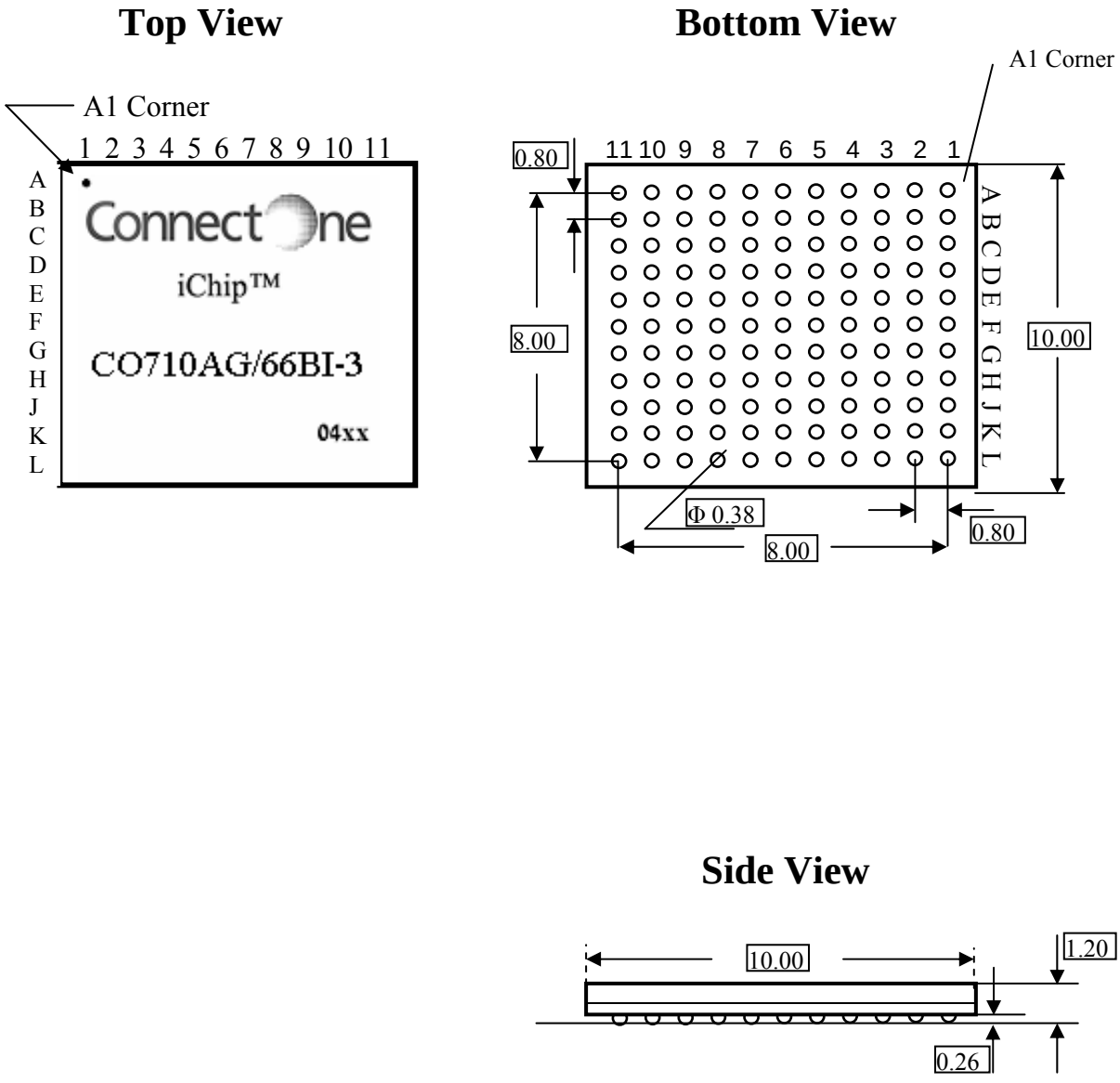


Figure 9-1 Mechanical Dimensions

10 iChip Designs

10.1 Serial Host and Ethernet Controller Environment

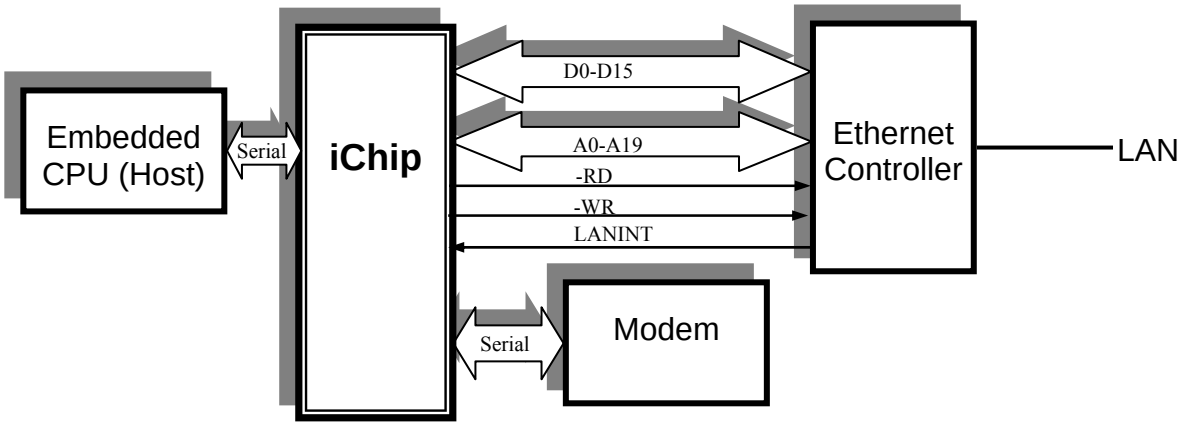


Figure 10-1 Serial Host and Ethernet Controller Environment

10.2 Parallel Host and Ethernet Controller Environment

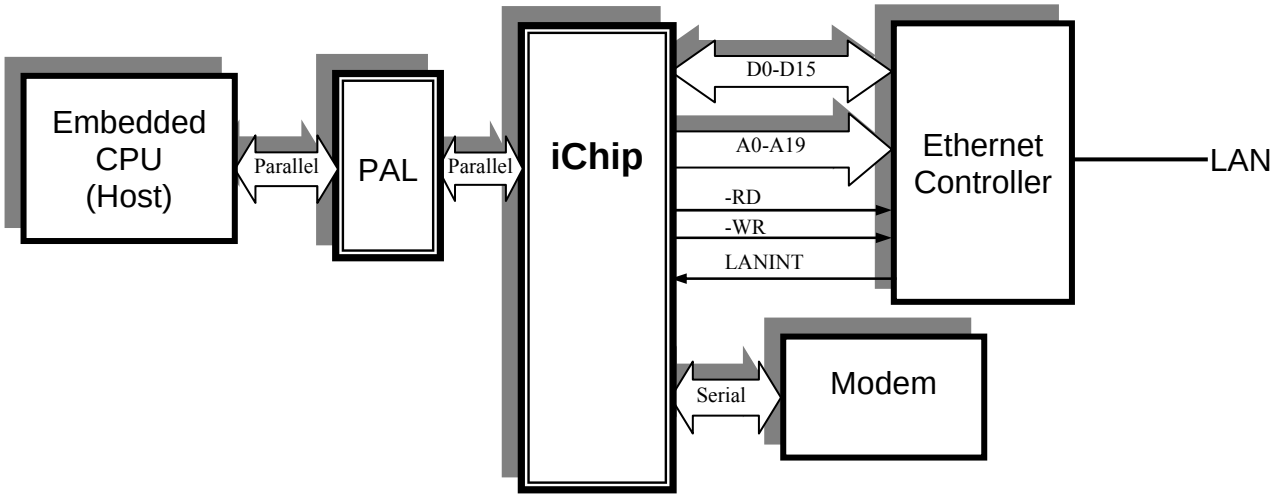


Figure 10-2 Parallel Host and Ethernet Controller Environment

10.3 Selecting the Reset Circuit

10.3.1 RC Network

The Reset signal may be designed with an RC network. τ should be greater than 10 mSec. This is a low-cost solution.

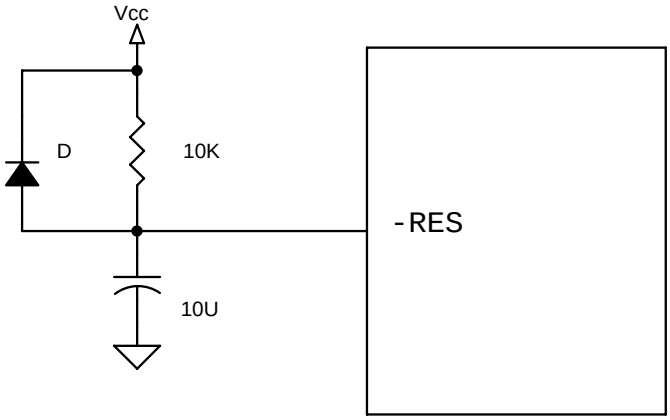


Figure 10-3 RC Reset Circuit

10.3.2 Supervisory Circuit

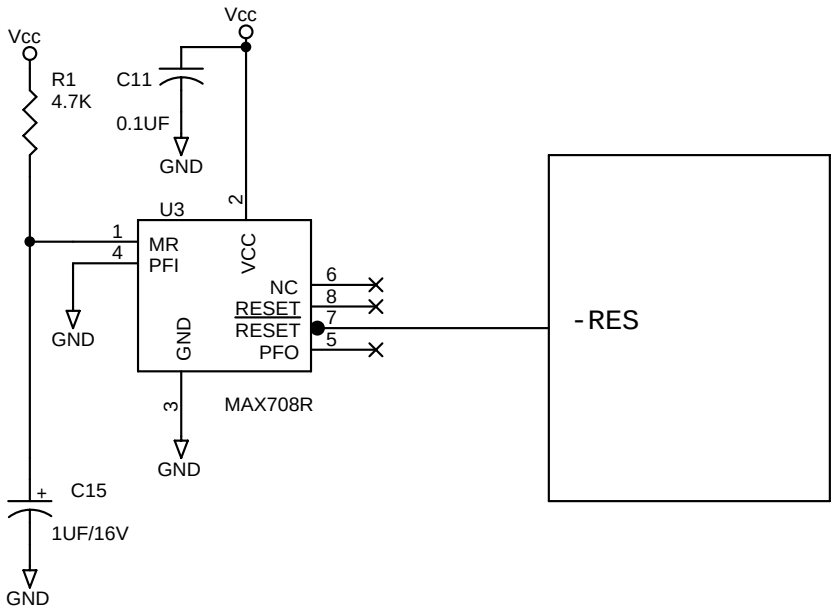


Figure 10-4 Supervisory Reset Circuit

11 Internet Protocol Compliance

iChip CO710AG/iChipSec CO711AG complies with the following Internet standards:

RFC 768	User Datagram Protocol (UDP)
RFC 791	Internet Protocol (IP)
RFC 792	ICMP – Internet Control Message Protocol
RFC 793	Transmission Control Protocol (TCP)
RFC 821	Simple Mail Transfer Protocol (SMTP)
RFC 822	Standard for the Format of ARPA Internet Text Messages
RFC 826	Ethernet Address Resolution Protocol (ARP)
RFC 959	File Transfer Protocol (FTP)
RFC 854	TELNET protocol specification
RFC 857	Telnet ECHO option
RFC 858	Telnet suppress Go-Ahead option
RFC 1034	DOMAIN NAMES (DNS) - Concepts and Facilities
RFC 1035	DOMAIN NAMES (DNS) - Implementation and Specification
RFC 1091	Telnet terminal type option
RFC 1073	Telnet window size option
RFC 1321	MD5 Message Digest Algorithm
RFC 1331	Point-to-Point Protocol (PPP)
RFC 1332	PPP Internet Protocol Control Protocol (IPCP)
RFC 1334	PPP Authentication Protocol (PAP)
RFC 1570	PPP LCP Extensions
RFC 1661	Point-to-Point Protocol (PPP)
RFC 1877	PPP IPCP Extensions for Name Server Addresses
RFC 1939	Post Office Protocol - Version 3 (POP3)
RFC 1957	Some Observations on the Implementations of the Post Office Protocol (POP3)
RFC 1994	PPP Challenge Handshake Authentication Protocol (CHAP)
RFC 2030	Simple Network Time Protocol (SNTP)
RFC 2045	Multipurpose Internet Mail Extensions (MIME) Part One: Format of Internet Message Bodies
RFC 2046	Multipurpose Internet Mail Extensions (MIME) Part Two: Media Types
RFC 2047	MIME (Multipurpose Internet Mail Extensions) Part Three: Message Header Extensions for Non-ASCII Text
RFC 2048	Multipurpose Internet Mail Extensions (MIME) Part Four: Registration Procedures
RFC 2049	Multipurpose Internet Mail Extensions (MIME) Part Five: Conformance Criteria and Examples
RFC 2068	HyperText Transfer Protocol HTTP/1.1
RFC 2131	Dynamic Host Configuration Protocol (DHCP)
RFC 2132	DHCP Options (only relevant parts)

iChipSec CO711AG complies with the following additional Internet standards:

RFC 2228	FTP Security Extensions
RFC 2246	The TLS Protocol Version 1.0

Table 11-1 Internet Protocol Compliance

12 List of Terms and Acronyms

AT+i^{TM}	**Connect One's** Internet extension to the industry-standard Hayes AT command set. Supports simplified Internet connectivity commands in the spirit of the AT syntax.
Base64	**Encoding scheme**, which converts arbitrary binary data into a 64-character subset of US ASCII. The encoded data is 33% larger than the original data.
CHAP	**Challenge Authentication Protocol.** Extends the PAP procedure by introducing advanced elements of security.
DNS	**Domain Name System**. Defines the structure of Internet names and their association with IP addresses.
FTP	File Transfer Protocol**. Used to provide file and directory services for remote server file systems.**
iChip^{TM}	**Connect One's Internet Controller for embedded Internet connectivity.**
ICMP	**Internet Control Message Protocol**. Network layer Internet protocol that reports errors and provides other information relevant to IP packet processing.
IP	**Internet Protocol**. Provides for transmitting blocks of data, called datagrams, from sources to destinations, which are hosts identified by fixed length addresses. Also provides for fragmentation and reassemble of long datagrams, if necessary.
IPCP	**Internet Protocol Control Protocol**. Establishes and configures the Internet Protocol over PPP. Also negotiates Van Jacobson TCP/IP header compression with PPP.
ISP	**Internet Service Provider**. Commercial company that provides Internet access to end (mostly PC) users through a dial-up connection.
LCP	**Link Control Protocol**. Negotiates data link characteristics and tests the integrity of the link.
"Leave on Server"	**An option** designating whether retrieved Email messages are to be left intact on the server for subsequent downloads or are to be deleted from the server after a successful download.
MIME	**Multipurpose Internet Mail Extensions**. Extends the format of mail message bodies to allow multi-part textual and non-textual data to be represented and exchanged between Internet mail servers.
PAP	**Password Authentication Protocol**. Used optionally by the PPP protocol to identify the user to the ISP.
ping	ICMP protocol **ECHO message** and its reply. Often used to debug IP networks and to test the accessibility of a network device.
POP3	**Post Office Protocol Version 3**. Allows a workstation/PC to dynamically retrieve mail from a mailbox kept on a remote server.
PPP	**Point-to-Point Protocol**. Communications protocol used to send data across serial communication links, such as modems.
RFC	**Request For Comments**. Collections of standards that define the way remote computers communicate over the Internet.
SMTP	**Simple Mail Transfer Protocol**. Provides for transferring mail reliably and efficiently over the Internet.
SNTP	**Simple Network Time Protocol.** Used to retrieve accurate time of day from a networked time server. The accurate UTC/GMT time is retrieved.

SSL3	**Secure Socket Layer Ver. 3.** Protocol that uses RSA Public-key exchange to establish an encrypted secure socket.
TCP	**Transmission Control Protocol**. Provides reliable stream-oriented connections over the Internet. Works in conjunction with its underlying IP protocol.
Telnet	**Network Terminal Protocol.** Provides remote terminal connectivity, which allows to execute tasks on a remote application server.
TLS1	**Transport Layer Security Ver. 1.** Supersedes the SSL3 protocol.

Table 12-1 Terms and Acronym