21145 Connection to the Network Using Physical Layer Devices

Application Note

July 1999

Order Number: 278293-001

Contents

Figures

Tables

1.0 Implementing Network Connections

This application note provides a description of how to implement 100BASE-TX and 10BASE-T network connections using the 21145 Phoneline/Ethernet LAN Controller (referred to as the 21145).

While this document will not provide specific recommendations for physical layer devices, it will provide design recommendations and layout recommendations using media-independent interface (MII) based physical layer devices provided by, Integrated Circuit Systems, National Semiconductor, Level One, and Seeq, and symbol (SYM) based physical layer devices provided by Mitel, Quality Semiconductor, and Micro Linear. Throughout this document, a physical layer device is referred to as a PHY or PHY device.

The devices covered in this application note are the following:

- QS6611 SYM PHY
- DP83840A MII PHY
- ICS1890 MII PHY
- TSC 78Q2120 MII PHY
- ML6698 100BASE-TX PHY
- 80220/80221 10/100BASE-TX PHY
- LXT970 Fast Ethernet Transceiver.

This application note was developed with the cooperation and input from different PHY manufacturers. In some cases, these manufacturers or Intel may have sample boards available to aid in your evaluation. Please check with the PHY manufacturer for the latest information available for each specific device.

Note: This application note does not describe the 21145 software interface. For more information on the software interface, refer to the *21145 Phoneline/Ethernet LAN Controller Hardware Reference Manual*.

1.1 Functional Overview

This section provides an overview of the 21145 and the implementation of 100 Mb/s and 10 Mb/s network connections using MII-based or SYM-based PHY devices.

1.1.1 21145 Overview

The 21145 is a single-chip bus master Ethernet/Fast Ethernet device that supports direct memory access (DMA) and has direct interfaces to both the CardBus and the PCI local bus. The 21145 implements a direct interface to the CardBus or PCI bus, which consists of the control and address/data signals.

The 21145 provides a complete implementation of the IEEE 802.3 Ethernet specification. This includes the twisted-pair (10BASE-T) interface, MII SYM port interface, and the interface through the media access control (MAC) layer that creates a direct interface to the PCI bus.

The PCI interface utilizes only about 10% of the bus bandwidth during fully networked operation for 100 Mb/s Fast Ethernet reception or transmission. This bus master design results in high throughput between the system and the network.

1.1.2 Network Interface

The 21145 physical layer design supports 10BASE-T twisted-pair (TP) Ethernet connections. The 21145 implements the 100BASE-T MII layer and the 100/10 Mb/s Ethernet MAC layer. The 21145 provides a dual network interface for both a 100BASE-T and a 10 Mb/s Ethernet. At the 100BASE-T port, the 21145 supports the industry-standard MII for any 100BASE-T implementation.

The 21145 is fully compliant with the MII specifications (as defined in IEEE 802.3). The MII is a nibblewide, general interface, that can be used with various physical interfaces, such as 100BASE-TX, 100BASE-T4, shielded twisted-pair (STP), and fiber. It also supports dual rates of speed (10 Mb/s and 100 Mb/s).

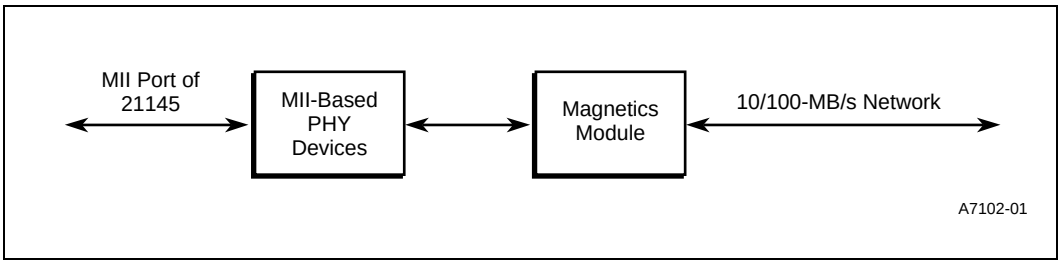
The 21145 includes special support for 100BASE-TX networks by including the PCS section (scrambler and 5B/4B coding/decoding). Integrating the 10BASE-T ENDEC with the 100 Mb/s-only SYM-based PHYs enables full support for a 10/100-implementation.

1.1.3 MII-Based PHY Block Diagram

Figure 1 is a block diagram of a 10BASE-T and 100BASE-T single-connector network connection using a MII-based PHY device with the 21145.

MII-based PHY devices are provided by Integrated Circuit Systems, National Semiconductor, Level One, Seeq, and TDK.

Figure 1. MII-Based PHY Design



The MII-based PHY design includes the following components:

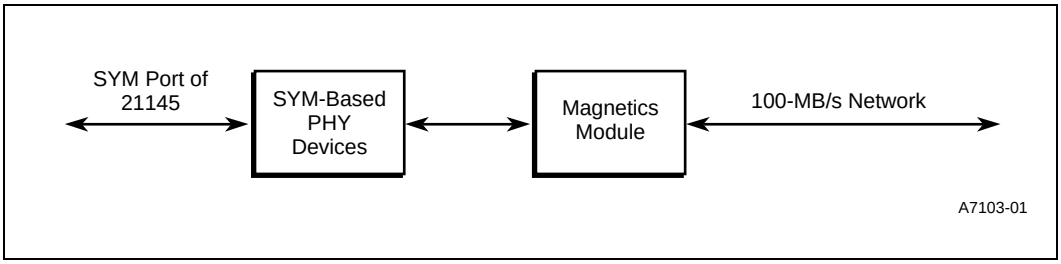
- The MII-based PHY devices, which have a direct interface to the MII port of the 21145 with dual-rate option (as specified in the MII specification) and a full interface to the 10/100 Mb/s magnetics module.
- The magnetics module, which is based on transformers and serial chokes enabling the network connection to the 100 Mb/s network (100BASE-TX or 100BASE-T4) and to the 10 Mb/s network (10BASE-T).

1.1.4 SYM-Based PHY Block Diagram

Figure 2 is a block diagram of a 100BASE-TX single-connector network connection using a SYM-based PHY device with the 21145. For a 10 Mb/s network connection, the network can be connected directly to the 21145 through filters and chokes.

SYM-based PHY devices are provided by Mitel, Quality Semiconductor, and Micro Linear.

Figure 2. SYM-Based PHY Design



The SYM-based PHY design includes the following components:

- The SYM-based PHY devices, which have a direct interface to the SYM port of the 21145 with an interface to the 100 Mb/s magnetics module.
- The magnetics module, which is based on transformers and serial chokes enabling the network connection to the 100 Mb/s-only network (100BASE-TX or 100BASE-T4).

1.2 21145 Ports

Table 1 lists the active twisted-pair signals when the 21145 10BASE-T port is selected.

Table 1. Twisted-Pair Signals

Signal	144-Pin Package Pin Number	176-Pin Package Pin Number
tp_rd–	10	10
tp_rd+	9	9
tp_td–	5	5
tp_td– –	4	4
tp_td+	6	6
tp_td+ +	7	7

Table 2 lists the active MII signals when the 21145 MII port is selected.

Table 2. MII Signals

Signal	144-Pin Package Pin Number	176-Pin Package Pin Number
mii_clsn	118	147
mii_crs	117	146
mii_dv	129	161
mii_mdc	134	166
mii_mdio	135	167
mii_rclk	128	160
mii_rx_err	127	159
mii_rxd <3:0>	133:130	165:162
mii_tclk	124	153
mii_txd<3:0>	119:122	151:148
mii_txen	123	152

Table 3 lists the active SYM signals when the 21145 SYM port is selected.

Table 3. SYM Signals (Sheet 1 of 2)

Signal	144-Pin Package Pin Number	176-Pin Package Pin Number
sd	117	146
sel10_100	127	159
sym_rclk	128	160
sym_rxd<0>	130	162
sym_rxd<1>	131	163
sym_rxd<2>	132	164
sym_rxd<3>	133	165
sym_rxd<4>	118	147
sym_tclk	124	153
sym_txd<0>	122	151

Table 3. SYM Signals (Sheet 2 of 2)

Signal	144-Pin Package Pin Number	176-Pin Package Pin Number
sym_txd<1>	121	150
sym_txd<2>	120	149
sym_txd<3>	119	148
sym_txd<4>	123	152

1.3 Network Connection

The network connections of the 21145 can be used in 10BASE-T, MII, or SYM configurations. Different methods are used to connect each port to the actual cable connector.

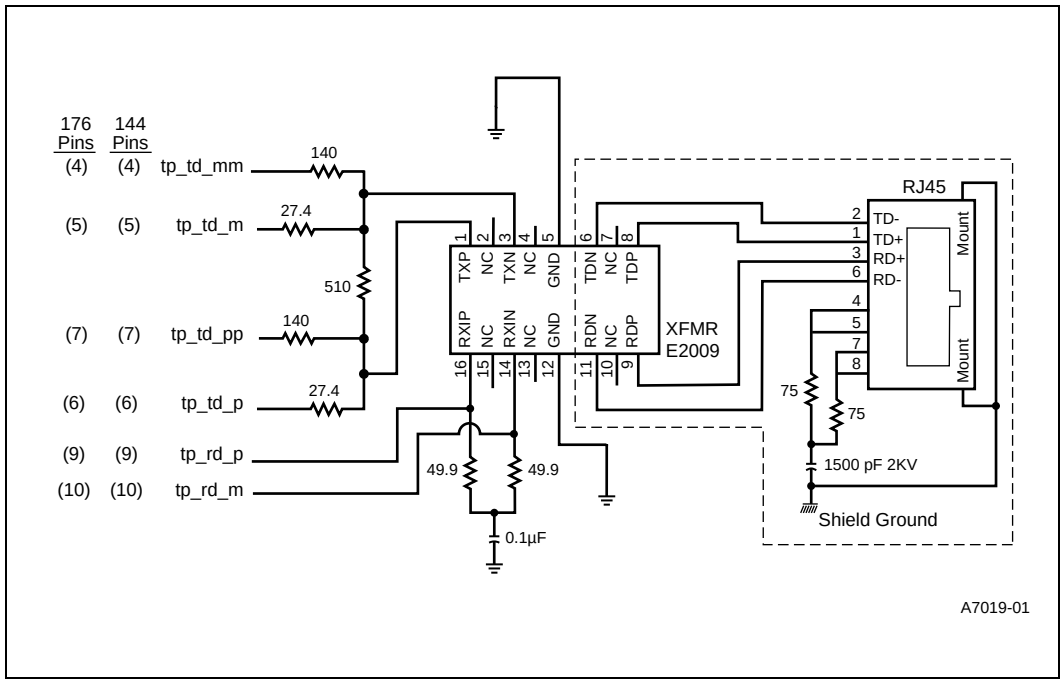
1.3.1 10BASE-T Twisted-Pair Network Port

Figure 3 shows the network connection design options for 10BASE-T type implementations. Figure 3 shows a direct connection to a 1:$\sqrt{2}$ transformer module. This implementation type provides the lowest component count for 10BASE-T. The filter and transformer components minimize any potential electromagnetic interference and radio frequency interface problems. Common-mode noise (when noise between two lines of the same polarity *add* rather than cancel) can radiate energy from the twisted-pair interface. Also, significant common-mode power supply noise can be generated on the board or adapter by other devices. Therefore, Intel recommends the use of filter and transformer modules that incorporate common-mode chokes.

Figure 3 shows the minimum component requirement for the 10BASE-T network connection. This implementation uses a filter transformer module with a 1:$\sqrt{2}$ transformer on the transmit path to compensate for the voltage swing. The required components for this configuration are as follows:

- Terminating and decoupling components
- Filter, transformer, and common-mode chokes
- RJ45 connector

Figure 3. Minimum Components Required for 10BASE-T



1.3.2 100-Ready Designs

The 21145 can also be designed for systems that are “100-Ready.” The term “100-Ready” implies a system that has a 10 Mb/s network that can easily be upgraded to become a 10/100 Mb/s network. There are two methods for providing 100-Ready designs:

- Provide a connector for an internal optional daughtercard.
- Provide an MII connector for an external module that connects to the MII/SYM port.

These two methods are described in Table 4.

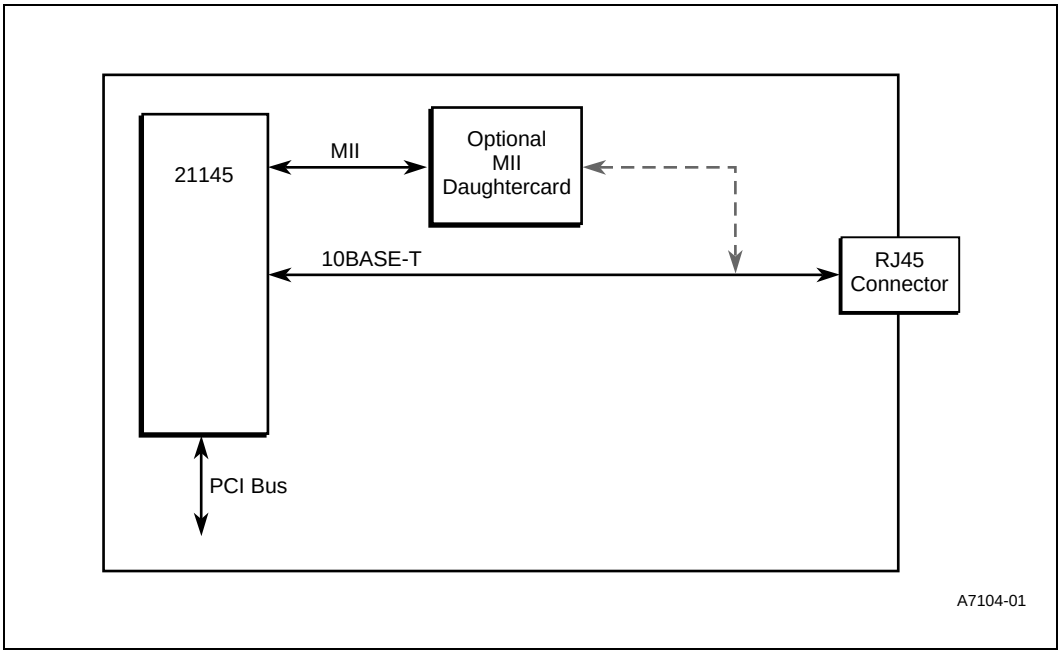
Table 4. Internal vs. External Design Features

Design	Features
Internal optional daughtercard	• Can be designed with an MII or any custom connector. • User opens cabinet to install 100 Mb/s daughtercard.
External MII/SYM module	• User connects module to external MII/SYM connector; user does not have to open cabinet for installation.

1.3.2.1 Internal Optional Daughtercard

Figure 4 shows a block diagram of a 100-Ready design using a daughter card.

Figure 4. 10BASE-T 100-Ready Daughtercard Block Diagram



1.3.2.2 Description of 100-Ready Daughtercard Block Diagram

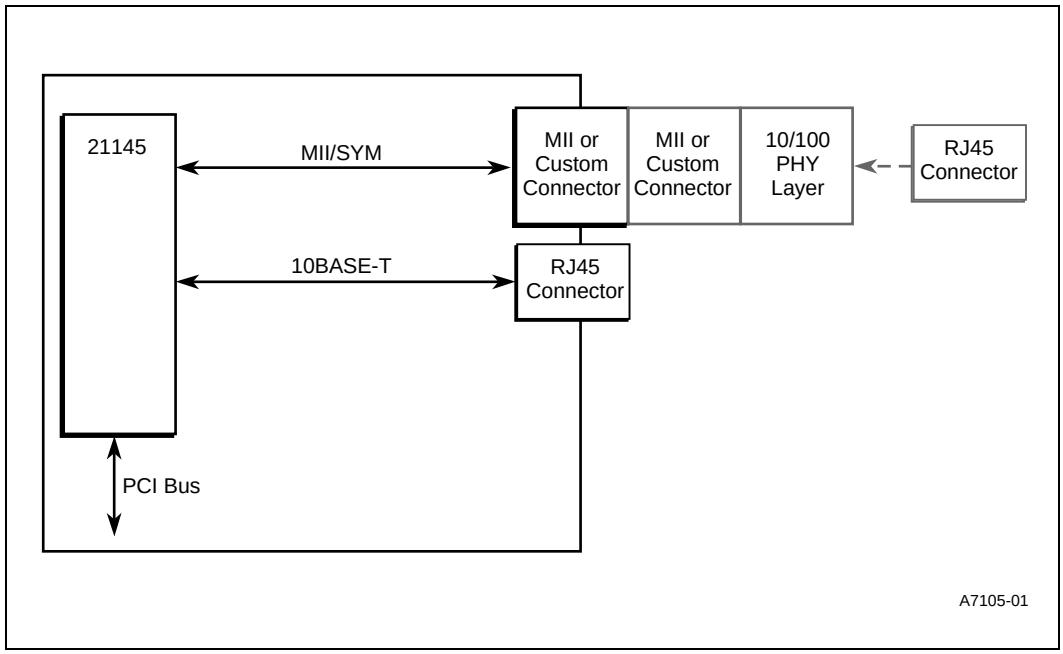
The blocks in the10BASE-T 100-Ready block diagram represent the following components:

- 21145 — A 21145 with all of the external components for operating the network connection (reference parts, XTAL, and so on). The 21145 can use the PCI bus and the MII/SYM, 10BASE-T ports for communication.
- Optional MII/SYM daughtercard — A daughtercard with a 100 Mb/s or 10/100 Mb/s PHY that interfaces with an MII connector or custom connector. The daughtercard can be designed to use the same RJ45 connector.
- RJ45 — A network connection.

1.3.2.3 100-Ready External Module Design

Figure 5 shows a block diagram of a 100-Ready design using an external module.

Figure 5. 10BASE-T 100-Ready External Module Block Diagram



1.3.2.4 Description of 100-Ready External Module Block Diagram

The blocks in the 100-Ready external module block diagram represent the following components:

- 21145—A 21145 with all of the external components for operating the network connection (reference parts, XTAL, and so on). The 21145 can use the PCI bus, and the MII/SYM, 10BASE-T ports for communication.
- Optional external MII/SYM daughtercard—A daughtercard with a 100 Mb/s or 10/100 Mb/s PHY that interfaces with an MII connector or custom connector. The daughtercard uses the magnetics to connect to the RJ45 connector.
- MII connector—An MII or custom connector that connects with the MII/SYM port of the 21145.
- RJ45—A network connection.

1.3.3 MII/SYM Pin Listing

Table 5 describes the MII/SYM pin multiplexing enabling the full flexibility for both network connections options using the same internal connector for the MII-based or the SYM-based PHY device (for detailed implementation notes, refer to the specific PHY device section in this document).

Table 5. MII/SYM Pinout (Sheet 1 of 2)

144-Pin Package Pin Number	176-Pin Package Pin Number	MII Interface Function	SYM Interface Function
117	146	mii_crs	sd
118	147	mii_clsn	sym_rxd<4>
119	148	mi_txd<3>	sym_txd<3>

Table 5. MII/SYM Pinout (Sheet 2 of 2)

144-Pin Package Pin Number	176-Pin Package Pin Number	MII Interface Function	SYM Interface Function
120	149	mi_txd<2>	sym_txd<2>
121	150	mi_txd<1>	sym_txd<1>
122	151	mii_txd<0>	sym_txd<0>
123	152	mii_txen	sym_txd<4>
124	153	mii_tclk	sym_tclk
127	159	mii_rx_err	sel10_100
128	160	mii_rclk	mii_rclk
129	161	mii_dv	N.C.
130	162	mii_rxd<0>	sym_rxd<0>
131	163	mii_rxd<1>	sym_rxd<1>
132	164	mii_rxd<2>	sym_rxd<2>
133	165	mii_rxd<3>	sym_rxd<3>
134	166	mii_mdc	N.C.
135	167	mii_mdio	N.C.

1.3.4 Media-Specific Components

Table 6 lists the media-specific interface components for 10BASE-T access.

Table 6. 10BASE-T Media-Specific Components

Access Type	Components	Available Part Numbers
10BASE-T	Filter, transformer and chokes	Pulse Engineering E2009
—	RJ45 wire jack connector	—

1.4 21145 Requirements

This section provides information about the external component connections for the 21145, and describes the following requirements:

- Current reference and capacitor input
- Crystal connection or crystal oscillator connection for the serial clock connection

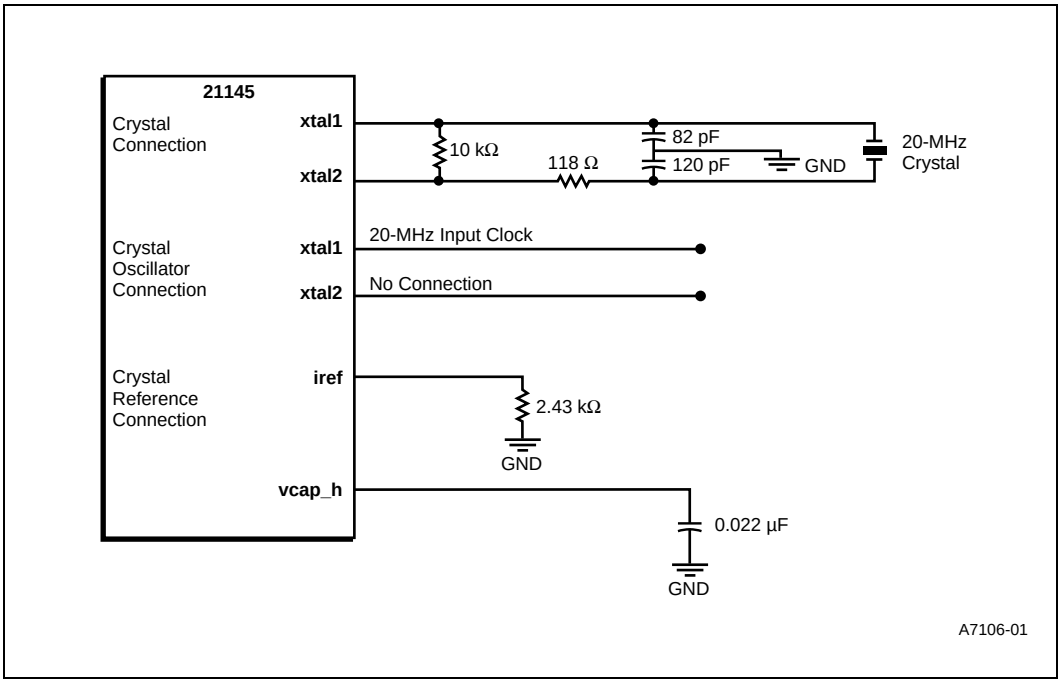
1.4.1 Current Reference and Capacitor Input Requirements

Table 7 describes the current reference and capacitor input requirements for the 21145, and Figure 6 shows the external component connections.

Table 7. Current Reference and Capacitor Inputs

Pin Name	144-Pin Package Pin Number	176-Pin Package Pin Number	Function	Connect This Pin...
iref	108	132	Current reference input for the analog phase-locked loop (PLL)	Through a 2.43 kΩ resistor to ground
vcap_h	110	134	Capacitor input	Through a 0.022 µF capacitor to ground

Figure 6. 21145 External Component Connections



1.4.2 Crystal and Crystal Oscillator Connections

Figure 6 shows two serial clock connections; select either the crystal connection or the crystal oscillator connection. According to the IEEE 802.3 standard, a 20 MHz crystal is required. The crystal frequency must not vary by more than 100 parts per million (PPM), or 0.01%. Place the crystal as close as possible to the 21145.

Because the frequency of crystals from different vendors can vary, test the crystals in the actual circuit. It may be necessary to vary the tuning of the surrounding components. However, after the capacitors have been tuned for the specific crystal, the design does not need to be altered on a board-by-board basis.

The 21145 also supports a crystal oscillator (Figure 6). This configuration requires no external component and xtal2 should be left open.This is useful for applications with multiple network connections.

Table 8 lists the crystal specifications.

Table 8. Crystal Specifications

Specification	Value	Units
Crystal frequency	20.000	MHz
Frequency tolerance	±50	PPM
Load capacitance	50	pF
Frequency stability	±30	PPM
Maximum effective series resistance	40	Ohms (Ω)
Test condition drive level	100	µW

1.5 Signal Routing and Placement

The Ethernet circuitry should be kept free of interference from unrelated signal traces. Routing for other signals must be kept away from the space surrounding the grouped Ethernet components. Place the Ethernet circuitry at the perimeter of the board, as close as possible to the network connector.

The onchip crystal oscillator requires an external crystal and discrete components. For stable and noise-free operation, place the crystal and discrete components as close as possible to the 21145, keeping the etch length as short as possible. Do not route any noisy signals in this area.

The PCI pin ordering is fully compatible with the PCI specification recommendation and can be easily routed within the specified etch limits of the PCI signals. This includes shared signal lengths of up to 3.8 cm (1.5 in) and the clock signal length of 6.41 cm (2.5 in).

Keep all signal paths short and route them as directly as possible.

Systems using 10BASE-T nodes can be connected by cables up to 100 m (328 ft.). As a result, signals that reach the board can be noisy and low in amplitude. To minimize corrupting this data, route these signals, by most direct path, from the network connector and through the magnetics coupler to the 21145.

The length of this path should not exceed 8 cm (3 in) for the active signals. The MII/SYM interface operates at 25 MHz (or 2.5 MHz). All routing of the MII/SYM signals to the MII/SYM device should be as short as possible and should not have significant differences of lengths and characteristics within signal groups. Examples of signal groups include mii_rxd<4:0> and mii_txd<4:0>.

Note: The routing of these signals should be done with caution. The preferred routing of these signals is in the external routing layers of the board. The MII/SYM device should be located between the 21145 and the magnetics port.

1.5.1 Ground and Power Planes

Up to four types of power signals require handling when implementing a design with the 21145:

- Gnd is adapter ground.
- Vcc (+5 V from PCI) drives the external components (boot ROM and Ethernet address ROM).
- Vdd (+3.3 V) drives the 21145.

Intel recommends that at least two power planes be kept on the PCB: Vcc and Gnd. The Vdd power plane (+3.3 V) can be implemented either by a cut in the Vcc power plane, or by a power island under the 21145 on one of the signal routing layers.

Intel recommends that decoupling capacitors should be connected to all power supplies. These capacitors should be placed as close as possible to the power pins of the chips. The recommended values are as follows: 0.1 µF, 0.01 µF, 10 µF (tantalum), and 47 µF (tantalum).

For better noise-testing immunity, separate all power planes between the network connectors and the transformer from the logic and analog power planes of the adapter for the 10BASE-T, and 100BASE-TX connections.

Intel also recommends that the connector's shield of the adapter should be connected to the PC chassis.

1.5.1.1 3.3 V Power Supply

The 21145 operates with a power supply of 3.3 V. At least eight decoupling capacitors are recommended and should contain the following values:

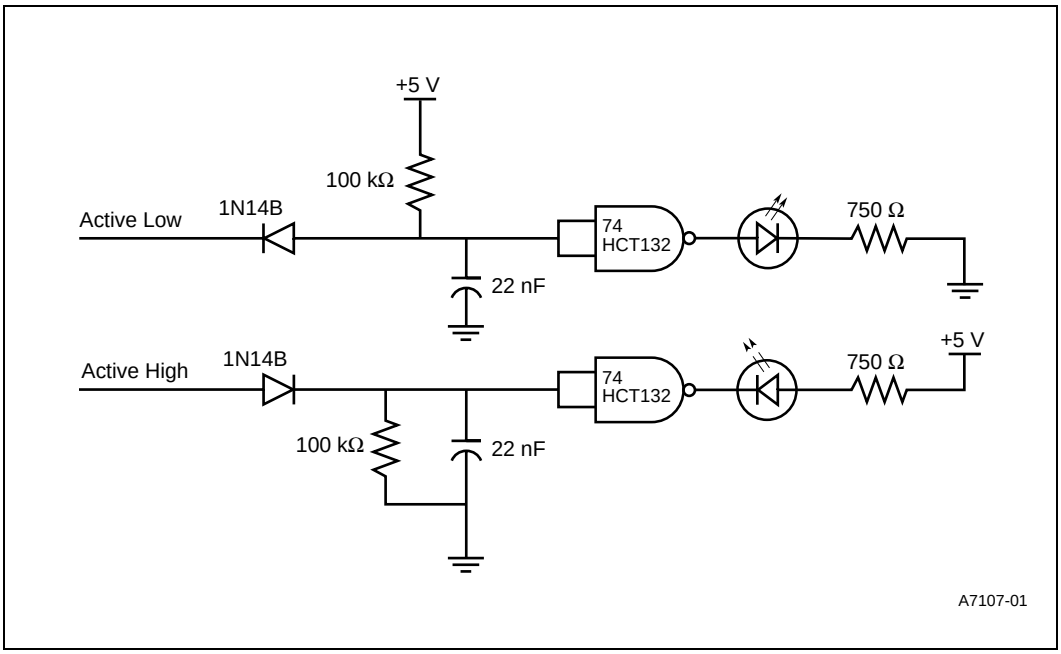
- Three each at 0.1 µF
- Three each at 0.01 µF
- One each at 10 µF (tantalum)
- One each at 47 µF (tantalum)

1.5.2 LED Status Signals

The LED connection requires a serial resistor that is connected to ground. This resistor value should be calculated according to the type of LED used. A typical 2 mA LED requires a 750 Ω resistor. For implementations using the boot ROM, the LED current should not exceed 2 mA. For LED indication and programming information, refer to the CSR15 definition in the *21145 Phoneline/Ethernet LAN Controller Hardware Reference Manual*.

The 21145 requires LED time-stretching logic for a visible indication of the activity signal. Figure 7 shows how to implement this circuit.

Figure 7. LED Time-Stretcher Circuit



1.6 Design Considerations

This section provides information to aid the user in designing Ethernet and Fast Ethernet capabilities onto a motherboard. In addition, it also includes design considerations for FCC compliance.

1.6.1 Designing the Ethernet Corner on Motherboards

This subsection provides a list of routing suggestions and a list of component placement suggestions.

The following list contains routing recommendations:

- Minimize the length of high-frequency signals.
- Route differential signal pairs together.
- Minimize the use of vias for high-frequency signals.

The following list contains component placement recommendations.

- Refer to the *PCI Local Bus Specification, Revision 2.1* for the placement of the 21145 with relation to the PCI bus.
- Place the 21145 as close to the PHY device as possible.
- Place the PHY device as close to the filters and magnetics as possible.
- Place the filters and magnetics as close to the RJ45 connector as possible.

1.6.2 Suggestions for FCC Compliance

Product designs and their associated applications are unique. Therefore, the designer must consider the total system or module implementation when determining a product design for FCC compliance.

The following information is provided as suggestions only to aid the designer in meeting FCC regulations.

1.6.2.1 Suggestions for Quiet Ground and Power Planes

For quiet ground and power planes, consider the following suggestions:

- Isolate power plane for PLL stability and noise isolation of audio digital-analog converters and amplifiers.
- Partition ground planes to isolate the I/O from common system noise. Do not route any etch across an isolated or partitioned ground plane.

Note: Ground plane splits can affect a signal's return path back to its source. If the signal return path is along the ground plane underneath the signal etch, any interruption in the ground plane increases the return path loop area, which in turn, increases its ability to radiate.

- Add common-mode chokes to the design at the output of the isolation transformer to isolate the I/O from common system noise.
- Place high-speed signals between power and ground planes to reduce board-level radiation.

The following books are recommended as additional references:

- *Fundamentals of Electromagnetic Capability*, by William G. Duff
- *Engineering Electromagnetic Capability*, by V. Prasad Kodali

1.6.2.2 Suggestions for Routing

For routing information, consider the following suggestions:

- Never route any etch (power or ground) across a partition or void because the signal loses its return-path integrity and contaminates the isolated plane.
- Avoid placing oscillators, phase-locked loops, and other clock-type devices near I/O connectors.
- Route all critical signals (for example; clocks, video output) directly in the etch and avoid, if possible, using vias (signal paths routed between planes in an etch board).

Note: Critical signals should be prioritized from the fastest to the slowest with respect to frequency and rise time. The fastest critical signals should be routed first.

2.0 QS6611 SYM PHY Network Implementation

This section describes how to interface the 21145 with the Quality Semiconductor QS6611 10/100BASE-TX transceiver (referred to as the QS6611).

2.1 QS6611 Overview

The QS6611 is a low-power CMOS 10/100BASE-TX transceiver that connects ‘gluelessly’ to the 21145. These two devices implement a complete 10/100 Fast Ethernet system with Auto-Negotiation, and a combined power dissipation under 1 W. The QS6611 provides a highly integrated, low-power replacement for previous BiCMOS solutions. It is suitable for use in adapters, routers, switches, both half- and full-duplex, and repeaters/hubs including ‘Class II’ types. The QS6611 performs transceiver, filter, and clock functions that minimize external components and their associated noise pickup and emissions. It also includes a switchable network interface port for both 10BASE-T and 100BASE-TX operation through common magnetics, eliminating the need for dual magnetics and/or external switches or jumpers.

Information on Quality Semiconductor products is available at the following website:

http://www.qualitysemi.com

2.1.1 Features

The QS661 has the following features:

- Low-power all-CMOS design; 1/3-power of BiCMOS: less than 80 mA
- MLT-3 transceiver with PLL clock generation and recovery
- Category 5 UTP and Type 1 STP support
- Replacement for AM78965/6, NS83223, 10BASE-T transmit and receive filters, and 10/100 switching to magnetics
- Integrated waveshaping
- 5-bit symbol interface to PCS
- Built-in PLL loop filters to minimize external components and noise coupling
- Adaptive equalization for phase and amplitude compensation
- BASE-line wander compensation
- Built-in test modes including local and remote loopback
- Serial interface to external 10BASE-T transceiver
- On-chip filters for both 10BASE-T and 100BASE-TX
- Switched interface to common magnetics for 10/100 Mb/s modes
- Single 5 V power supply
- 64-pin QFP and TQFP surface mount packages

2.1.1.1 Features and Benefits

Table 9 outlines the QS6611 features and benefits.

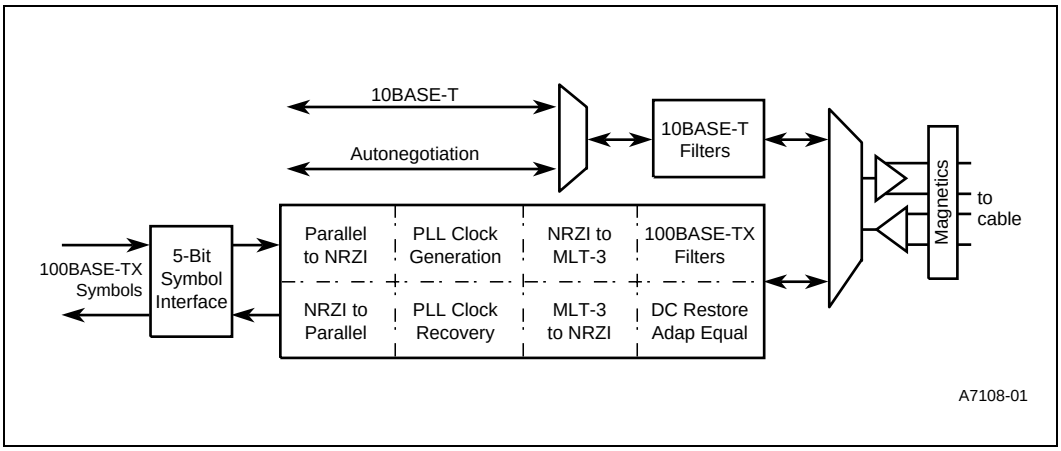
Table 9. QS6611 Features and Benefits

Features	Benefits
Fully CMOS	Low power; less than 80 mA
Adaptive equalizer	Adapts automatically to various cable lengths
QFP and VQFP (thin) packs	PCI/CardBus/hubs/switcher
10BASE-T transmit filters	No external hybrid L-C filters
10/100 multiplexing	No external relay or switchers
Crystal-ready 125/20 MHz clock synthesis	1/3-cost of oscillator module
Digital clock recovery PLL with integrated loop filters	No external loop filter components required

2.2 QS6611 System Diagram

Figure 8 shows the system diagram for the QS6611.

Figure 8. QS6611 System Diagram



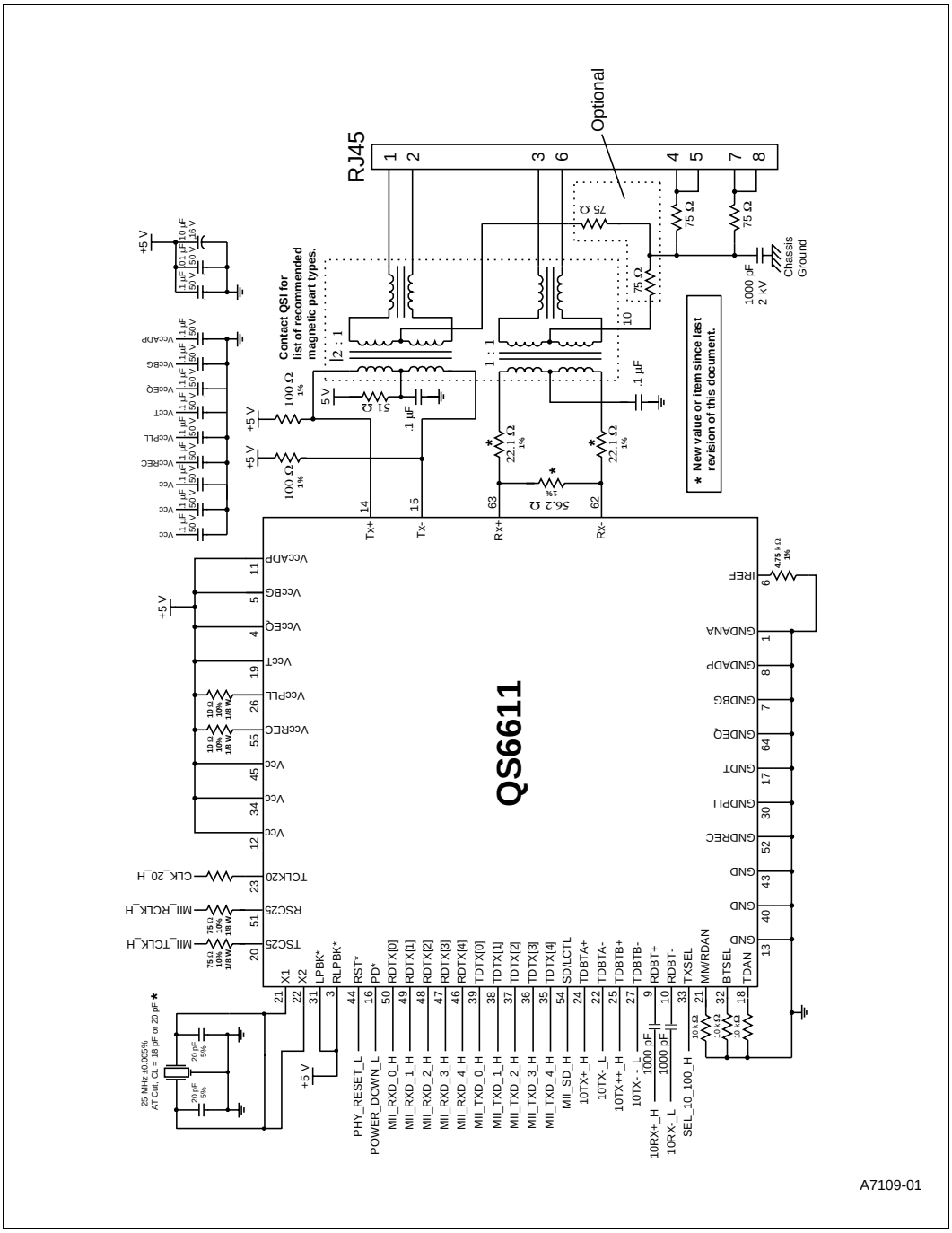
2.3 QS6611 Schematic

This section describes how to connect the QS6611 to the network and to the 21145, and provides layout considerations.

2.3.1 Network Connections

Figure 9 shows how to connect the QS6611 to the network.

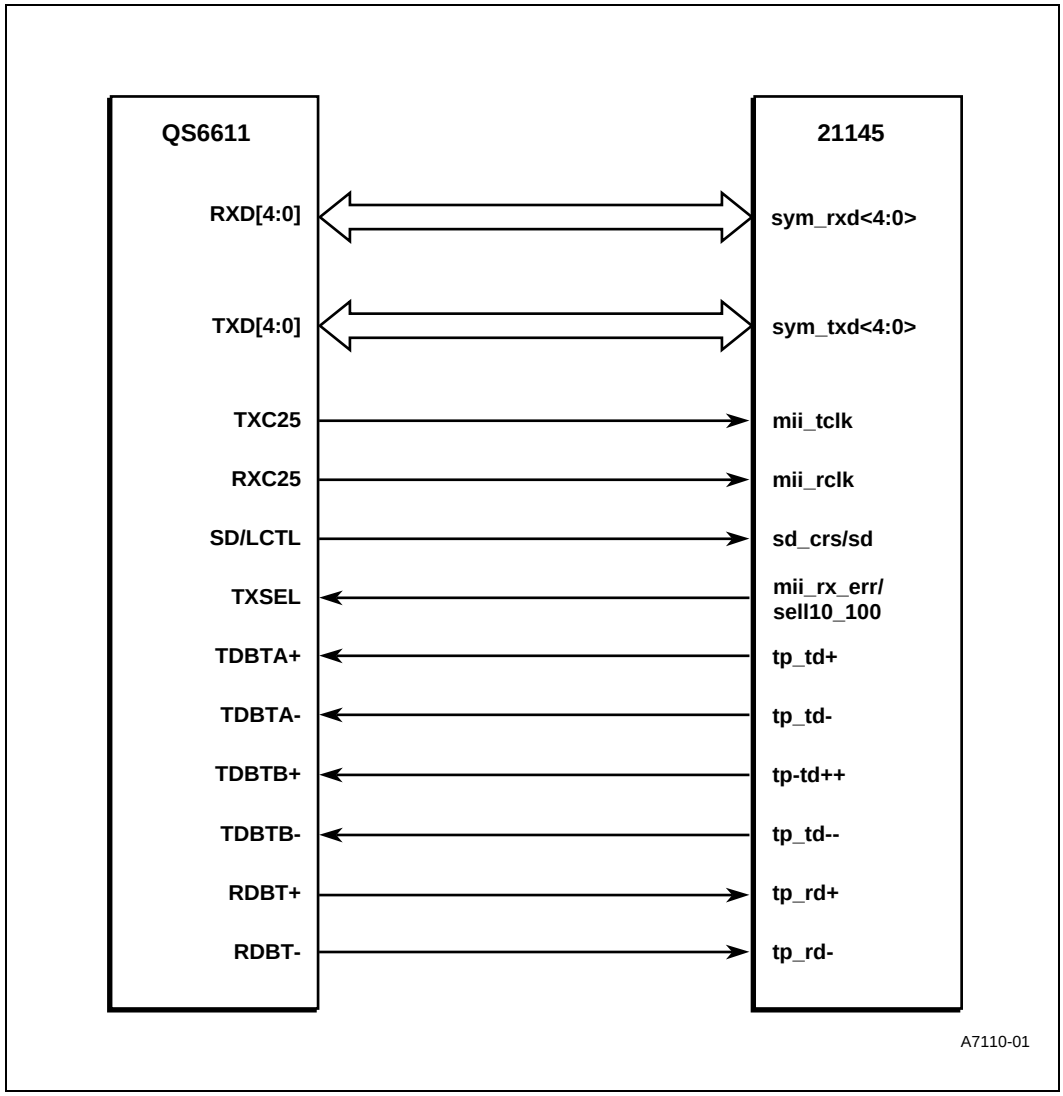
Figure 9. QS6611 Connection to the RJ45-8



2.3.2 21145 Connections

Figure 10 shows how to connect the QS6611 to the 21145.

Figure 10. Connecting the QS6611 to the 21145



2.3.3 Layout Considerations

Consider the following recommendations in Table 10 for the PWB layout of the QS6611 and 21145 in a PCI adapter.

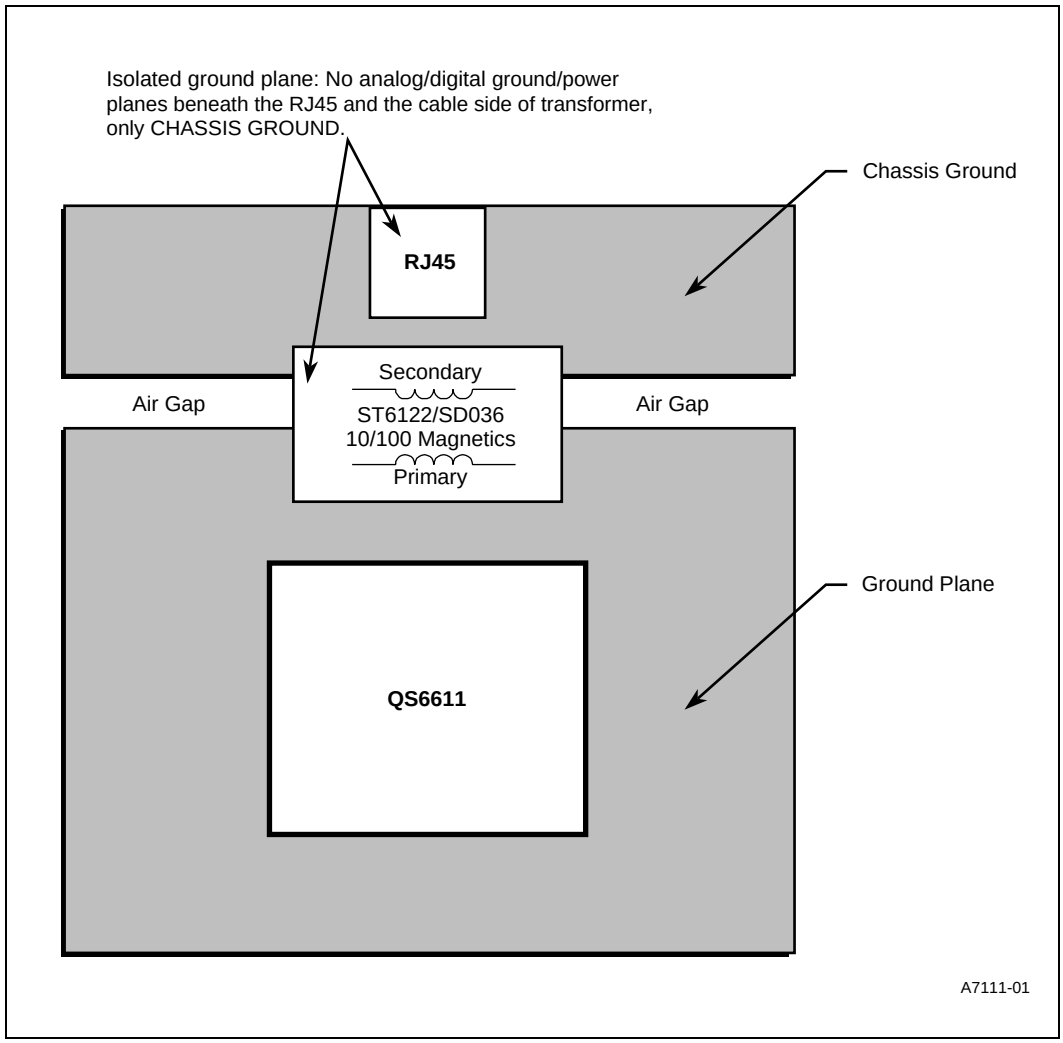
Table 10. QS6611 PWB Layout Recommendations

Recommendation	Comments
Place the 4.75 kΩ, 1%, 1/8 W current reference resistor within 1.5 cm away from the IREF pin (pin 6). (See Figure 9.)	A 4.75 kΩ resistor will ensure the transmitting amplitude to be within 2 V peak-to-peak, +/15%.
Layout the 10 Ω resistor and the 1.0 µF capacitor for pin 26 and for pin 55 with trace lengths less than 3 mm as shown in Figure 12.	These resistor and capacitor circuits filter noise from the PLL circuitry to reduce potential errors due to noisy environments. The RC components need to be placed as close to the pins as possible to be effective.
Remove 75 Ω from the center tap of the transmitting secondary side of the transformer.	This is to avoid common-mode noise being injected back to the ground plane. By removing the 75 Ω resistor, EMI testing improved by typically 6 dB on several designs.
Refer to Figure 11 for recommended parts positioning. Place the QS6611, the transformer module, and the RJ45 connector as close to each other as possible for best transmission and least noise pickup and emissions.	The area under the RJ45 connector and the near edge of the magnetics module (under the pins) should be isolated from the Vcc and ground planes, and should have its own “chassis ground” plane as shown in Figure 11.
Do not segment the Vcc power plane or ground plane. Use a single, continuous plane for Vcc and ground to which all power pins (Vcc and Gnd) will connect through vias as close to the pins as possible.	Splitting the Vcc power supply plane into segments for different Vcc pins on the QS6611 is not needed, and may cause problems in bypassing the various segments.
Refer to Figure 9 for recommended pin connections.	Certain unused pins on the QS6611 need to be tied high or low as shown in Figure 9.
For best results, use a crystal, rather than a clock oscillator. Place the crystal as close to the X1 and X2 pins (pins 21 and 22) as possible, and keep traces short and direct.	Use 25 MHz ±0.005%, CL = 39 pF, AT Cut, Parallel Resonant (for example, ECS250.18).
Place the 4.99 kΩ, 1%, 1/8 W current reference resistor as close to the IREF pin (pin 6) as possible.	See Figure 11.
Keep transmit and receive pair runs as short as possible. Keep the separation between the two conductors of each pair fairly wide, 1 or 1.5 mm if possible, using the same separation width all along the run to improve transmission characteristics. Keep the separation between adjacent pairs on the same layer (or adjacent layers not separated by a power or ground plane) wide, 2 mm or more if possible, to minimize cross-talk.	Transmit and receive pairs should not cross over each other. They should not be laid one on top of the other on adjacent planes (but this is allowed if a power or ground plane is placed between the other planes). The two traces of a pair should never cross over each other.
Keep high-frequency traces short, and space them apart from each other and from traces that may be sensitive, to improve transmission and reduce cross-talk. Especially sensitive are clock lines, high-speed bus lines, high-impedance lines (passively-driven lines), analog lines, and the symbol interface lines.	Where long, high-speed lines cannot be avoided, ringing and echo problems can be treated with series resistors at the source end and termination resistors to ground or Vcc at the far ends.
Never route clock or high-speed signal lines immediately under the body of the QS6611 chip.	If there is a ground or power plane shielding the QS6611, it is allowed.
Layout pads for the 230 Ω resistor and 0.1 µF capacitor on pin 26, and minimum length traces as shown in Figure 12.	Later revision of the QS6611 will probably not need this resistor. The recommended layout allows omission of this resistor without PCB layout change.
Use two 1000 pF capacitors in the RDBT± line (pins 9 and 10) to decouple the DC common-mode voltage between the 21145 and the QS6611.	See Figure 9.

2.3.4 Ground-Plane Partitioning

As shown in Figure 11, isolating circuits on the primary side from the secondary side of the transformer with an air gap can reduce noise.

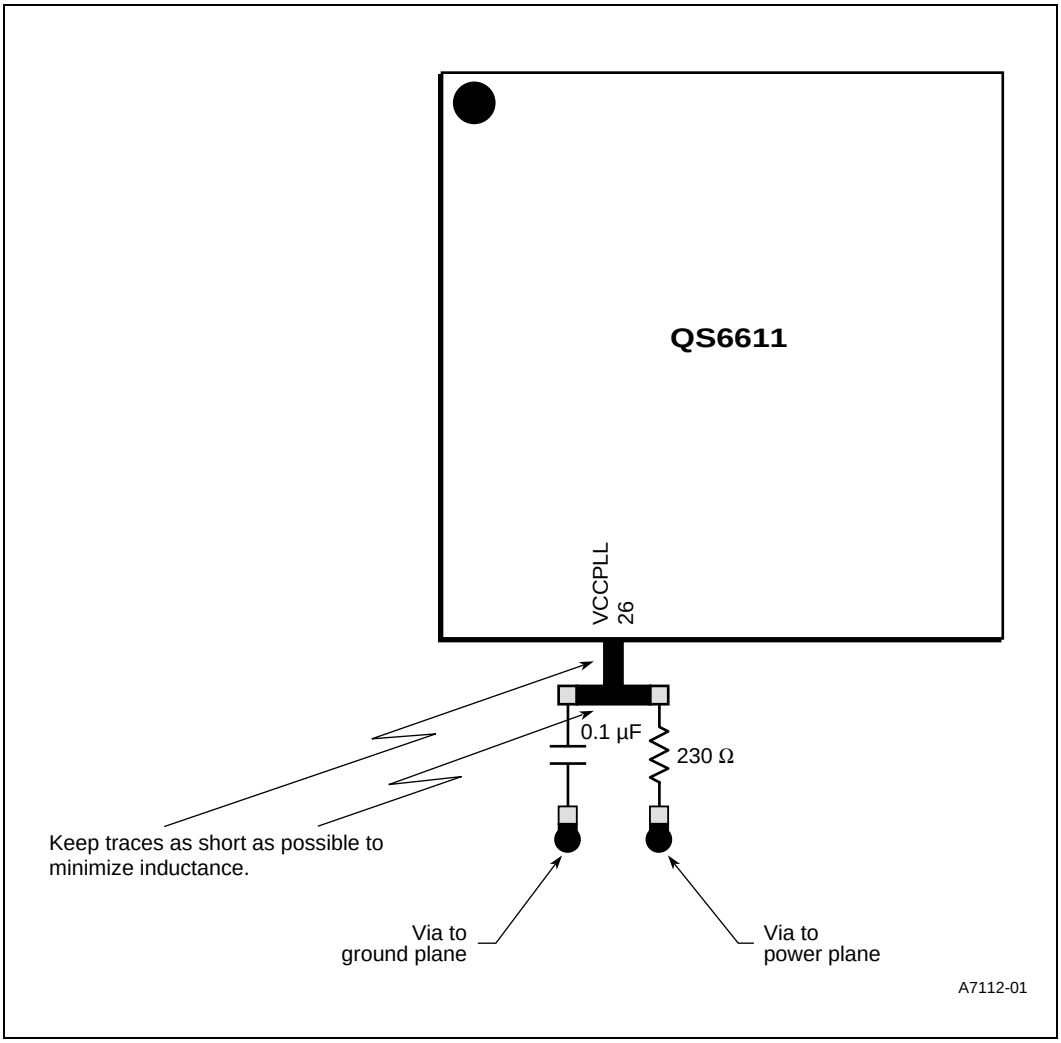
Figure 11. PWB Noise Reduction



2.3.5 VCCPLL Connections

Figure 12 shows how to connect the VCCPLL pin on the QS6611.

Figure 12. Connecting the VCCPLL on the QS6611



3.0 DP83840A MII PHY Network Implementation

This section contains the design recommendations for the National Semiconductor DP83840A 10/100 Mb/s PHY device and the DP83223V TWISTER High-Speed Networking Transceiver (referred to as the DP83840A and DP83223V) in a node application using the 21145.

3.1 DP83840A and DP83223V Overview

The DP83840A PHY device incorporates an integrated 10BASE-T transceiver as well as an MII for a connection to the 21145. The DP83840A is fully compatible with the DP83223V to enable 100BASE-TX compliant signaling.

A design based on these three devices allows for a simple low-cost PCI node design, which will support both 10BASE-T and 100BASE-TX protocols. The comprehensive feature sets of both the 21145 and the DP83840A support several different modes of functionality.

Although design issues such as common magnetics, autonegotiation, and 10/100 Mb/s operation are noted here, detailed emphasis is placed on fundamental design requirements from the MAC layer to the RJ45-8 connector. Schematic diagrams, layout considerations, and power requirements are all provided in this application note. A magnetics scheme is recommended to help the designer integrate the National Semiconductor parts in a system.

For a given application, the component values and design suggestions in this section can and will vary with the particular design. This section illustrates the function of the various components and their relationship to overall system performance. With this knowledge, the system designer can make modifications to the recommendations with an understanding of the potential impact to the system.

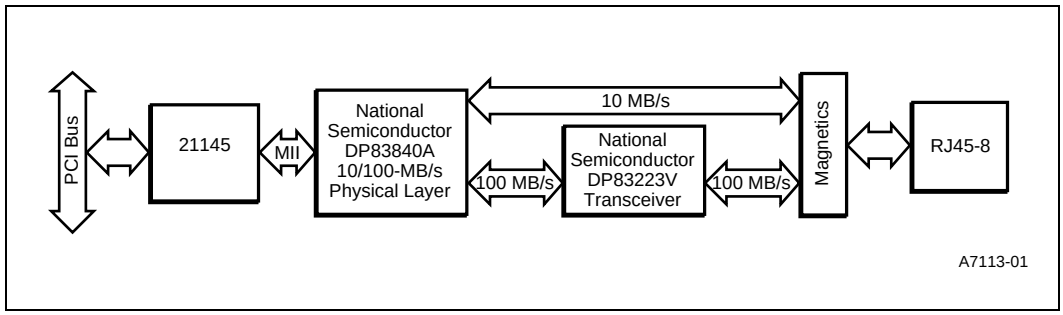
Information on National Semiconductor products is available at the following website:

http://www.national.com

3.2 DP83840A and DP83223V Block Diagram

Figure 13 is the system diagram for a node application. The following sections describe the blocks. For more detailed information on the specifications of these parts, see the documentation listed in Appendix B.

Figure 13. 10/100 Mb/s Block Diagram



3.3 DP83840A Description

The DP83840A finds wide application in data communication systems. It is a PHY device for Ethernet 10BASE-T and 100BASE-X using Category 5 (CAT5) unshielded, Type 1 shielded, and fiber-optic cables. It interfaces to the PMD sublayer through a DP83223V and to the MAC layer through the MII, ensuring interoperability between products from different vendors.

The DP83840A system architecture is based on the integration of the following National Semiconductor industry-proven core technologies:

- 10BASE-T ENDEC/Transceiver module to provide the 10 Mb/s IEEE 802.3 functions
- 100BASE-X physical coding sublayer (PCS) and control logic that integrate the core modules into a dual-speed Ethernet physical layer controller

The DP83840A features include:

- IEEE 802.3 10BASE-T compatibility. ENDEC and UTP/STP transceivers and filters are built in.
- IEEE 802.3 100BASE-X compatibility with support for Category 5 UTP, Type 1 STP, and fiber-optic transceivers. Connects directly to the DP83223V.
- ANSI X3T12 TP-PMD compatibility.
- IEEE 802.3 autonegotiation for automatic speed selection.
- Independent interface (MII) with serial management interface.
- Integrated, high-performance, 100 Mb/s clock recovery circuitry that requires no external filters.
- Full-duplex support for 10 Mb/s and 100 Mb/s.
- MII serial 10 Mb/s output mode.
- Programmable loopback modes for easy system diagnostics.
- Flexible LED support.

3.4 DP83223V Description

The DP83223V twisted-pair transceiver can drive and receive either binary or MLT-3 encoded data streams. The DP83223V allows links of up to 100 m (328 ft.) over both STP and data grade UTP or equivalent. The DP83223V also provides important features such as tristate-capable transmit outputs, and controlled transmit output edge rates (to reduce EMI radiation) for both binary and MLT-3 modes of operation.

The DP83223V features include:

- Integrated transmitter and receiver with adaptive equalization circuit.
- Programmable binary or MLT-3 operation.
- Isolated TX and RX power supplies for minimum noise coupling.
- Controlled transmit output edge rates for reduced EMI.
- Tristate-capable current transmit outputs.
- Loopback feature for board diagnostics.
- Programmable transmit voltage amplitude.

3.4.1 Magnetics

The magnetics block in Figure 13 uses a common magnetics scheme that allows 10 Mb/s and 100 Mb/s data to coexist in the same magnetics package. The concept of common magnetics is based on the interoperation of the DP83840A and the DP83223V, and allows for either 10 Mb/s or 100 Mb/s operation with the use of a single magnetics module and RJ45-8 media connector. (For a complete discussion of the common magnetics concept, refer to the National Semiconductor *10/100 Ethernet Common Magnetics* application note.)

National Semiconductor has patents on a common magnetics scheme, and provides a license to purchasers of both the DP83840A and the DP83223V components to use the common magnetics scheme in their design. Several suppliers have indicated that they intend to provide magnetic components for the National Semiconductor recommended implementation. Appendix A contains a list of these magnetics vendors and the license agreement. This is not an exhaustive list and other vendors could be considered, but the transformer would need to be characterized in relation to the *10/100 Base-T Magnetics Specification* (available from National Semiconductor).

3.4.2 DP83840A and DP83223V Schematic Diagram

Appendix A contains the schematic diagrams for the PHY. Figure 44 illustrates the interconnection of the DP83840A and DP83223V.

3.4.3 Media-Independent Interface (MII)

The DP83840A has a standard IEEE 802.3 MII for connection to external 10 Mb/s or 100 Mb/s PHYs. This comprises nibblewide (4-bits) transmit and receive data streams, transmit and receive clocks, transmit enable, receive collision, receive carrier sense, receive data valid, data error, and serial management data clock and data signals. These signals are: TX_CLK, TXD[3:0], TX_EN, CRS, COL, RXD[3:0], RX_CLK, RX_DV, RX_ER, MDC, and MDIO.

The MII supports two nibble clock rates:

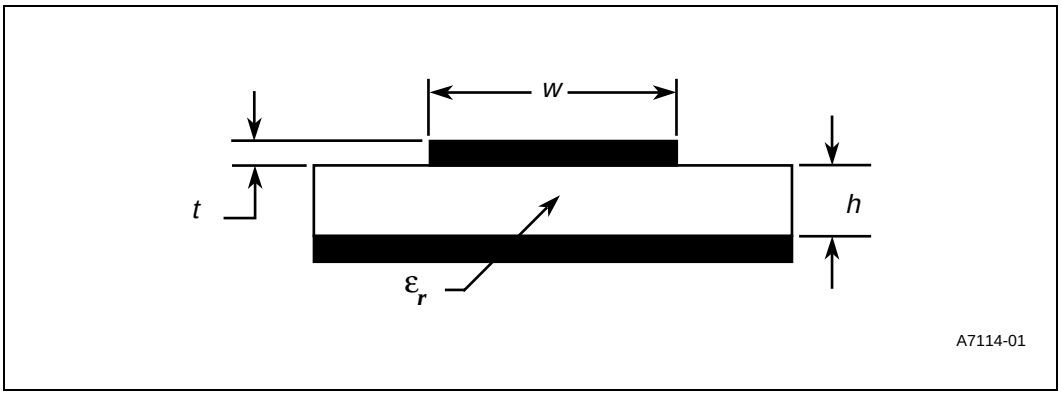
- 2.5 MHz for 10 Mb/s operation
- 25 MHz for 100 Mb/s operation

Operation at 10 Mb/s or 100 Mb/s is transparent to the host.

3.4.4 Signal Terminations

The trace impedance of each MII line should be approximately 68 Ω per the IEEE specification. The design of microstrips for PC boards is straightforward and a function of the microstrip width (*w*), thickness (*t*), height (*h*), and the relative electric permittivity of the substrate (ε), as shown in Figure 14.

Figure 14. Microstrip impedance



Equation 1 shows how the various geometric and material parameters on the printed circuit board (PCB) control the impedance of the trace. Most of the PCB programs calculate the trace impedance directly.

Equation 1. Microstrip Impedance

$$Z = \left(\frac{87}{(\sqrt{\varepsilon_r + 1.41})}\right)\ln\left(\frac{5.98h}{(0.8w + t)}\right)$$

The DP83840A supports 10 Mb/s and 100 Mb/s Ethernet using the DP83223V and the common magnetics approach. The following signal lines between the DP83840A and the DP83223V should be PECL (Thevenin) terminated at the DP83223V: PMRD+, PMRD-, PMID+, PMID-, SD+, and SD-. These signal lines are Thevenin terminated (see Figure 48) with an equivalent resistance equal to the trace impedance. This trace impedance should be controlled and match the device termination resistance. For the preferred case of a 50 Ω transmission interconnect, resistors R23 through R28 are 82.5 Ω to **Vcc**, and R6 through R9, R21, and R22 are 130 Ω to ground. This generates a 50.3 Ω Thevenin resistance. The trace impedance of these signal lines should also be 50 Ω.

It is critical that these lines be kept short (<1 inch) and that termination resistors are as close as possible to the destination. If the PECL termination resistors are not placed close to the signal destination, reflections might result and could corrupt the signal integrity. The midlevel voltage of the termination network should be 3 V and the required bias current is 23.5 mA due to each line termination.

The 50 Ω termination is the low impedance robust approach, requiring 23.5 mA per PECL termination. In this application there are six terminations totaling 141 mA. This might be excessive current draw for certain applications and higher values of termination resistance could be considered. For example, in the National Semiconductor *Managed Repeater* application note, the termination values are 160 Ω to Vcc and 260 Ω to ground. This is a 100 Ω Thevenin resistance and the current draw is reduced to 11.75 mA per termination. A reasonable upper bound might be a Thevenin resistance of approximately 100 Ω to 200 Ω. To ensure that the data maintains integrity as the resistor values increase, check the quality of the high-speed interconnect signal with an oscilloscope, looking for minimal ringing and equal rise and fall times in the waveform.

In Fast Ethernet systems, special attention needs to be given to transmission type effects. If proper line termination is not used for a given application, ringing will occur on these lines. It is worth noting that the SD± signal detect lines are detecting either the presence of a valid signal on the RXI± inputs or that loopback mode has been selected. In either case, SD± is essentially static and higher value termination resistors can be used.

3.4.4.1 Signal Transmission

When the 100 Mb/s port is enabled, the DP83223V TXO± outputs are directly connected across the entire primary of the common magnetics transmit section of the transformer. Because this connection uses a 1:1 isolation transformer, the 2 V peak-to-peak (5%), differential MLT-3 signal generated by the DP83223V is maintained as it is coupled onto the UTP. The 100 Mb/s operation uses the transmit transformer in a unity-gain configuration (less the insertion loss). The source termination resistance is established by the sum of R4 and R5 (47.5 Ω × 2.5), and the ON resistance of the solid-state switches Q3 and Q4 (2.5 Ω × 2), as shown in Figure 47. This circuit resistance should be equal to the cable impedance of 100 Ω. For STP, the circuit resistance of R4, R5, Q2, and Q3 should be equal to the cable impedance of 150 Ω.

The DP83840A TXU± output provides standard 10BASE-T signaling, as shown in Figure 45 and Figure 46 in Appendix A, and Figure 2 of the National Semiconductor *10/100 Ethernet Common Magnetics* application note. This differential signal is coupled to one-half of the transmit isolation transformer primary winding through series resistors R1 and R2, and capacitors C32 and C30. Equation 2 shows the basic transformer equations.

Equation 2. Transformer Equations

$$\frac{V_p}{V_s} = \frac{n_p}{n_s} = N \qquad \text{A.}$$

$$Z_{prim} = N^2 Z_{\text{sec}} \qquad \text{B.}$$

Equation 2A is the turns ratio as a function of the secondary and primary voltages, and Equation 2B is the primary impedance as a function of the secondary load and turns ratio (N). In Equation 2, subscripts *p* and *s* represent primary and secondary, *V* represents voltage, and *Z* represents impedance.

In 10BASE-T transmit mode, the turns ratio (n_p/n_s) is 1/2. The secondary load impedance for UTP cable is 100 Ω. For the primary impedance to match the secondary impedance, a primary impedance of 25 Ω is required. This scales through the transformer voltage gain to appear as

100 Ω. This primary impedance is established by resistors R1 and R2 (10.5 Ω each) and the output impedance of the driver ports TXU± (2.5 Ω each) (see Figure 46). The series sum of these resistances is 25 Ω.

Good signal transfer is maintained by matching the cable impedance to the driving impedance. Resistor R3 and capacitors C1 and C8 are included to provide a balanced impedance across each leg of the transmit transformer primary winding and high-frequency rolloff, which improves FCC characteristics.

Bypass capacitors C29 to C32 and C8 have been added since the initial work on the 10/100 common magnetics. These capacitors compensate for the rising output impedance of the 10 Mb/s transmit driver circuits. This circuit establishes a pole-zero pair, with the zero being at approximately 15 MHz. Placing the zero at 15 MHz balances the increasing output impedance term. The effect of adding these capacitors is a 2 dB to 3 dB improvement in transmit return loss measurement. These capacitors, which increase the output transmit voltage, should be added to existing and new designs if possible.

3.4.4.2 Signal Receive Operation

As shown in Figure 44 in Appendix A and Figure 3 of the National Semiconductor *10/100 Ethernet Common Magnetics* application note, the 100 Mb/s receive signal is coupled from the cable by an isolation transformer with a 1:1 turns ratio. The DP83223V RXI± inputs receive the 100 Mb/s data through the attenuation network comprising resistors R29 through R32 and capacitor C14. This attenuation network is required to optimize the adaptive equalization function within the DP83223V receiver. A recent application note from National Semiconductor, *DP83223 TWISTER Adaptive Equalization Considerations*, discusses the attenuation network details and component selection.

A particular system design must take into account the actual amount of transformer insertion loss. This measured value of insertion loss and the manufacturer-specified tolerances can be used to determine the correct resistor divider ratio for the network attenuator. It is critical that the overall attenuation resistance be maintained at 100 Ω (series resistance of R29 through R32). The attenuation circuit (shown in Figure 46) comprises two series 12.1 Ω resistors (R31 and R32), which provide a 24.2 Ω differential impedance to the incoming signal. Additionally, R29 and R30 form a 76 Ω combination that, when combined with the 24.2 Ω series resistance, creates the required 100 Ω forward cable termination. The attenuation network resistors should have a tolerance of ≤1% (1/8 Watts) to maintain signal tolerance. The DP83223V RXI± inputs receive the signal as it appears across the attenuator voltage divider. This attenuated voltage should be 1.45 V. Measurements should be made on the system to ensure that the correct voltage is being received. This method of measurement is described in the *DP83223 TWISTER Adaptive Equalization Considerations* application note from National Semiconductor.

Capacitor C14 (0.01 µF) is placed at the center point of the attenuation resistors. This capacitor provides common-mode ground reference, reducing system sensitivity to common-mode noise.

Note: The selection of the attenuation network components is extremely critical for good system performance. Refer to the *DP83223 TWISTER Adaptive Equalization Considerations* application note from National Semiconductor for the detailed design of this circuit.

An isolation transformer with a 1:1 turns ratio couples the 10 Mb/s differential receive signal from the cable. This differential signal is capacitively coupled through C9 and C10 to the DP83840A RXI± inputs (see Figure 45). Because the signals are capacitively coupled to the DP83840A RXI± high-impedance inputs, DC current is blocked, ensuring signal levels with the proper common-mode voltage as set by the DP83840A. In addition to the Manchester encoded 10BASE-T data, the DP83840A RXI± inputs receive normal link pulses and fast link pulses to allow Nway autonegotiation functionality.

3.4.5 STP Operation

The DP83840A can be configured, through internal control register access, to source data through the TXS± outputs for shielded twisted-pair operation. In this case, the unshielded TXU± outputs are tristated to eliminate contention. Similarly, the TXS± outputs are tristated during 10 Mb/s unshielded twisted-pair signaling from TXU±.

Other than resistor and capacitor value changes to accommodate 150 Ω STP cable, all remaining interaction between the DP83840A and the DP83223V remains as stated in Section 3.4.3 through Section 3.4.5. Additionally, the RJ45-8 modular jack used for unshielded twisted-pair applications is replaced by a media connector (DB-9). Refer to Section 3.4.7 for the connection information. Table 11 lists the component values required for STP or UTP operation.

Table 11. Component Values Required for STP or UTP Operation

Configuration	R3	C8 (pF)	C1 (pF)	R10	R4	R5	R16 R17	R1 R2	C29/C31 (pF)	C30/C32 (pF)	R31 R32	R29 R30
UTP	10.5	1000	9	511	47.5	47.5	x	10.5	x	1000	12.1	37.9
STP	16.5	620	18	511	73.2	73.2	16.5	x	620	x	29.4	46.4

x = Do not install component.

3.4.6 Common-Mode Termination

The intent of common-mode termination is to help reduce unwanted contributions to EMI emissions and susceptibility by properly terminating the common-mode energy that can exist on the twisted-pair cable. This technique is designed for unshielded twisted-pair applications that, due to the lack of a shield, inherently possess high susceptibility to common-mode noise sources.

3.4.6.1 Transmit Active Pair Termination

Figure 47 and the *10/100 Base-T Common Magnetics* specification suggest the use of a center-tapped transformer within the transmit magnetics. This allows access to the common-mode signal present on the cable. The impedance of the common-mode channel within an unshielded twisted-pair can be calculated to be approximately 75 Ω. To obtain the 75 Ω common-mode resistance, R18 (49.9 Ω) is connected between the transformer center-tap and capacitor C5 (500 pF to 1000 pF @ 2 kV rms). This resistance, when combined with the cable differential termination resistance, provides the required 75 Ω resistance. The other side of C5 is connected to chassis ground. This capacitor requires a 2 kV rms rating to guard against high-energy transients coupled onto the LAN cable systems and static-charge buildup on LAN cables and components. The *TP-PMD* specification (Sections 8.4 to 8.4.2.2, Isolation Requirements) establishes the voltage rating for the capacitor. The inclusion of this capacitor also improves circuit performance, providing a solid common-mode reference and reducing common-mode noise.

The high voltage capacitor can be fabricated using the printed circuit board as the dielectric. The capacitor should be designed onto the chassis side of the board, using all four layers to obtain the required capacitance. Equation 3 is the equation for a parallel plate capacitor.

Equation 3. Parallel Plate Capacitance

$$C = 8.85\left(\frac{\varepsilon_r A}{l}\right)$$

In Equation 3, C is in F, A is the area of the plates in m^2, l is the separation of the plates in m, and ε_r is the relative permittivity of the medium between the capacitor plates, in Fm^{-1}.

Dielectric strength (DS) is a critical parameter of this capacitor. This is the voltage that can be placed across the part prior to breakdown. For a given plate spacing this breakdown is proportional to the dielectric strength of the medium between the plates. The radius of curvature of the edge of the capacitor plate is another factor. With the printed circuit board as the medium (which is essentially epoxy/fiberglass), the DS is 400 V/mil. For a standard 4-layer board with an overall thickness of 0.062 in, the dielectric strength is approximately 6400 V between capacitor plates.

3.4.6.2 Receive Active Pair Termination

Figure 47 shows R57 (49.9 Ω) connected to the center-tap of the receive transformer primary to provide a common-mode attenuation connection point.

3.4.6.3 Unused Pair Termination

Unused pairs 4-5 and 7-8 are tied together and connected to the same 2 kV rms capacitor (C5) through two 75 Ω resistors (R19 and R20). This provides direct termination for potential common-mode noise on the unused pairs. Because of cross-talk, common-mode noise present on the unused pairs can also be detrimental.

3.4.7 Media Connections

Table 12 and Table 13 show the pinout requirements for UTP and STP node connections.

Table 12. Unshielded Twisted-Pair RJ45-8 Connector

10BASE-T/100BASE-TX	Pin
Transmit pair	1 (TX+) and 2 (TX-)
Receive pair	3 (RX+) and 6 (RX-)
Unused pair	4 and 5
Unused pair	7 and 8

Table 13. Shielded Twisted-Pair DB-9 Connector

10BASE-T/100BASE-TX	Pin
Transmit pair	5 (TX+) and 9 (TX-)
Receive pair	1 (RX+) and 6 (RX-)
Unused pins	2, 3, 4, 7, and 8
Ground to chassis	Shield

3.5 DP83840A and DP83223V Layout Considerations

The goal of any complex system design, especially one that includes both analog and digital functionality, is to achieve the most robust system performance possible. Performance aspects such as bit error rate, EMI, and general signal integrity must be considered.

The correct combination of component placement, signal routing practices, and power supply distribution will yield a robust and reliable system.

This section considers the physical design aspects of a 10/100 Ethernet system design using National Semiconductor PHYs in conjunction with common magnetics. The National Semiconductor *1996 National Ethernet Databook* discusses the theory and practice of system design.

3.5.1 Component Placement

The relative placement of the active and passive components within a system design is essentially defined by important design parameters; such as performance, cost, and board area.

Figure 15 shows a potential component layout that will yield good signal integrity and good overall performance. The layout minimizes the required board area while optimizing the relative component placement.

The layout of the dynamic transmit and receive signals at the twisted-pair transceiver interface is critical to good performance. As shown in Figure 15, the DP83840A is orientated such that its TD, RD, and SD signal pins are in close proximity to the PMRD, SD, and PMID signals on the DP83223V. These signals carry the transmit and receive 100 Mb/s data and their length should be minimal. This configuration shows the MII connector adjacent to the DP83840A pins that contain the MII signals (pins 51-80). The oscillator is adjacent to the OSC_IN pin on the DP83840A. Keeping the oscillator close to the device minimizes jitter at the clock output. Clearly, component location can vary depending on the other devices being used in the application.

Note: In the system layout it is critical to maintain short distances between the transmit and receive sections of the DP83840A and DP83223V, and to place the MII adjacent to the DP83840A (pins 51-80).

3.5.1.1 Special Considerations

Incorporate controlled impedance routing for the signal traces that carry the 125 Mb/s serial bit stream. Standard microstrip or stripline techniques are recommended. Choose an impedance of 50 Ω for each trace that transports the 125 Mb/s information between the RJ45-8, common magnetics, and the DP83223V transceiver. This is required to match the 100 Ω differential impedance of the unshielded twisted-pair cable.

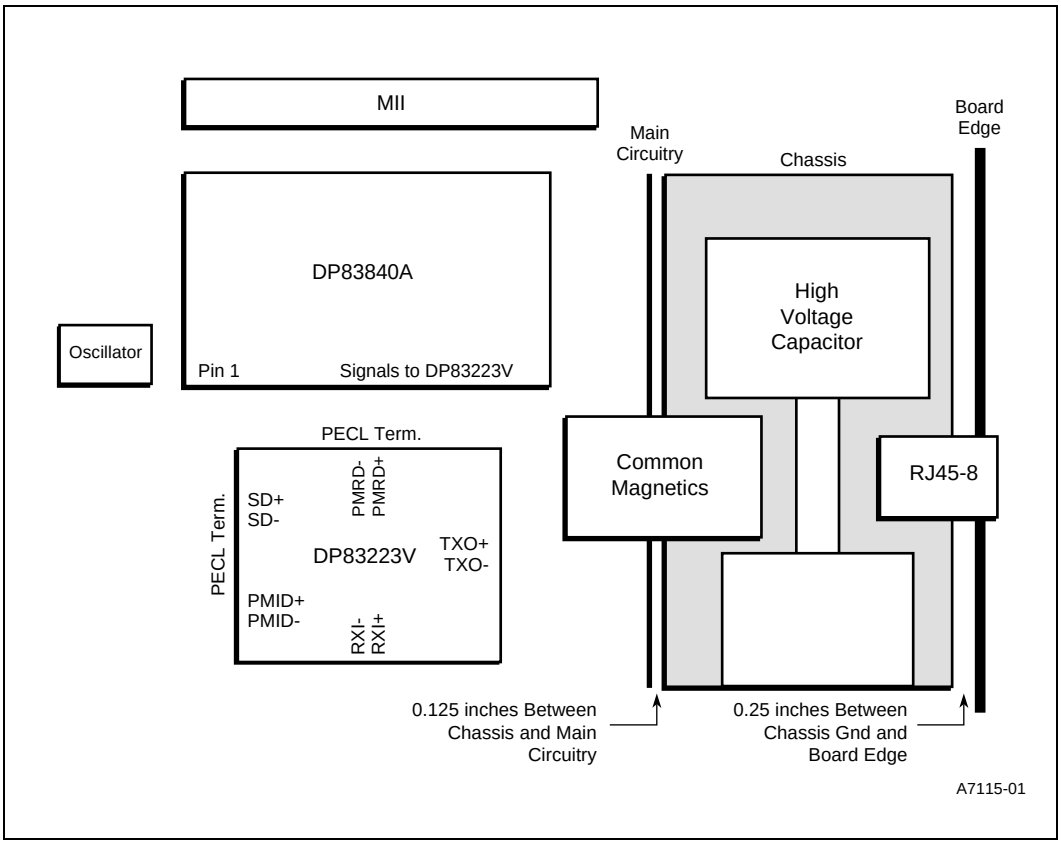
The 125 Mb/s PECL signals connected between the DP83223V and the DP83840A can be designed as 50 Ω to 100 Ω impedance traces. The choice of PECL terminating resistors will determine the trace impedance, such that they are consistent with each other.

3.5.2 General Guidelines

General guidelines for optimal signal trace routing practices include:

- Minimal length, controlled impedance signal traces to minimize reflections and decrease noise sensitivities. The most critical signals are between the DP83840A and the DP83223V, and the signals from the RJ45-8 to the transformer. The signal traces from the RJ45-8 to the transformer should be stripline with an impedance of 50 Ω.
- Matched length differential signal traces to minimize jitter.
- Radiused, route trace corners of greater than 45°.
- Minimum number of vias for a given signal trace to minimize radiation.
- PECL terminations placed close to signal destination.
- All controlled impedance signal traces routed directly over or under uninterrupted power or ground planes on adjacent layers. This minimizes noise coupled into signal lines.

Figure 15. Physical Layer Component Placement Recommendation

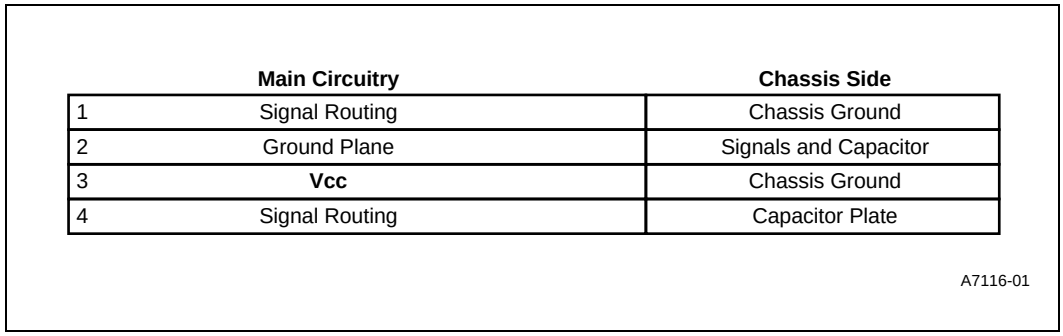


3.5.3 Board Layers

The number of board layers will vary depending on the signal routing density. In general, a 4- to 6-layer design is sufficient. The 4-layer case shown in Figure 16 is sufficient for most node applications.

Figure 16 shows one potential option for PCB layer assignment, a configuration with good FCC results. Layers 1 and 4 are for signal routing, layer 2 is the ground plane, and layer 3 is **Vcc** for the circuit devices. On the chassis side of the card, layer 1 is chassis ground, layer 2 is for signals and capacitor, layer 3 is chassis ground, and layer 4 is the capacitor plate. For the capacitor, layer 2 is connected to 4 (as one plate) and layers 1 and 3 are the ground side of the capacitor. Configuring the capacitor in this way has the net effect of three capacitors in parallel.

Figure 16. Board Layer Recommendation



3.5.4 Ground Plane Partitioning

Recent system measurements at National Semiconductor show that the single ground-plane approach is one way to minimize EMI. Ground-plane partitioning can cause increased EMI emissions that might make the system noncompliant with specific FCC regulations. Figure 15 shows a recommended ground layout scheme and specifies the placement and space between the system ground and chassis ground.

Keeping the chassis ground approximately 0.25 inches from the edge of the system motherboard, and voiding that gap of any copper, will help to reduce any potential fringe radiation that might occur during system operation. This is permissible because no active traces need to be routed in this area.

3.6 Power Requirements

Careful power supply filtering and isolation practices can provide a minimized noise environment for each of the unique digital and analog sections of the DP83223V and DP83840A. A recommendation is to use one power and one ground plane. Recent system measurements made at National Semiconductor on a 10/100 Ethernet system showed reduced (approximately 7 dB) EMI emissions in single ground and Vcc plane systems (as compared to multiple Vcc and ground islands interconnected by ferrite beads).

As the data rates begin to increase, power and ground-plane partitioning require careful consideration. To be compliant with electrical isolation issues, the chassis ground needs to be physically isolated from the system circuit ground. The DC voltage for the circuit card should be derived from a stable power supply. The power supply input decoupling circuit should provide sufficient capacitance that will maintain the supply at a full voltage and provide a low impedance at high frequencies. Typically,

a capacitor to keep the voltage stable (10 µF or 4.7 µF) and a high-frequency bypass capacitor (0.01 µF) are sufficient for the card if the supply is stable and clean. Careful attention to power decoupling is required on the PHYs and is described in Section 3.6.1.

3.6.1 DP83840A and DP83223V Decoupling

The DP83840A internally partitions the power sections into four basic groups: PLL, analog (ANA), RX/TX, and digital. To maintain the integrity of these power partitions, PLL, RX/TX, ANA, and digital power pins are decoupled as shown in Figure 45. The schematic shows a typical connection with parallel 10 µF and 0.01 µF capacitors, and a series inductor (C24, C4, and L3 [Murata BLM31A02]) to the Vcc power plane. This allows for the attenuation of low- and high-frequency noise. For the PLL and ANA Vcc, a series resistor can be added to provide further isolation. The value of this resistor should be <4 Ω to keep the voltage drop low.

In certain applications it might be possible to simplify the decoupling circuit on these pins. The best way to determine if this is the case, is to measure the power supply noise using a spectrum analyzer on the power input and at the device pin. If this value is not influenced by the decoupling circuit, it might be possible to simplify the circuit. The present scheme provides good isolation, filtering, and voltage stability. For local decoupling on the DP83223V, connect RX and TX together with a large pad, and use 10 µF and 0.01 µF capacitors in parallel and a series inductor to the power plane. Figure 45 and Figure 46 show the details of chip decoupling.

3.7 DP83840A and DP83223V Parts List

Table 14 lists the recommended parts for the DP83840A and DP83223V.

Table 14. Recommended Parts List for DP83840A and DP83223V (Sheet 1 of 2)

Description	Value	Volts	Tolerance	Package	Qty	Reference
C/CER	9 pF	50	10%	SMD0805	1	C1
C/CER	27 pF	50	10%	SMD0805	1	C35
C/CER	620 pF	50	10%	SMD0805	2	C29, C31
C/CER	1000 pF	50	20%	SMD1206	2	C30, C32
C/CER	0.01 µF	50	20%	SMD1206	14	C2, C6, C11-C18, C22-C25
C/CER	820 pF	50	10%	SMD1206	1	C8
C/CER	0.1 µF	50	20%	SMD1206	2	C9, C10
C/CER	500 - 1000 pF	2 kV rms	20%	Through-hole	1	C5
Polarized capacitor	10 µF	16	20%	SMD	9	C3, C4, C7, C19-C21, C26, C28, C36
Inductor	—	—	—	SMT	3	L1- L3
Telco connector	—	—	—	TH	1	J2
MII 100 Mb/s connector	—	—	—	RT/A_PCB_CONN	1	J1
Oscillator 50 MHz	—	—	—	Half-size	1	Y3
LED	Green	—	—	LED-dial 5-50 typ05	5	D2-D6
Resistor	1.5 kΩ	—	5%	r500	1	R63
Resistor	10.5 Ω	—	1%	1206	1	R3
Resistor	16.5 Ω	—	1%	1206	2	R16, R17
Resistor	10 κΩ	—	5%	1206	1	R59

Table 14. Recommended Parts List for DP83840A and DP83223V (Sheet 2 of 2)

Description	Value	Volts	Tolerance	Package	Qty	Reference
Resistor	75 Ω	—	5%	1206	2	R19, R20
Resistor	10 Ω	—	5%	0805	1	R56
Resistor	10 kΩ	—	5%	0805	7	R49, R51-55, R59
Resistor	1.5 kΩ	—	5%	0805	9	R14, R15, R42, R43, R60-R63
Resistor	4.7 kΩ	—	5%	0805	8	R34-R40, R64
Resistor	12.1 Ω	—	<1%	0805	2	R31, R32
Resistor	10.5 Ω	—	1%	0805	2	R1, R2
Resistor	37.9 Ω	—	<1%	0805	2	R29, R30
Resistor	47.5 Ω	—	1%	0805	2	R4, R5
Resistor	82.5 Ω	—	1%	0805	6	R23-R28
Resistor	130 Ω	—	1%	0805	6	R6-R9, R1, R22
Resistor	511 Ω	—	1%	0805	1	R10
Resistor	TBD[1]	—	1%	0805	4	R12, R13
Transistor	—	—	—	sot23	3	Q1-Q3
DP83223V	—	—	—	28PLCC	1	U2
DP83840A	—	—	—	PQFP100	1	U1
Fuse	—	—	—	Radial	1	F1
10/100 magnetics	—	—	—	SMD	1	T1

1. Design-dependent value.

3.8 DP83840A and DP83223V Summary

National Semiconductor provides a complete physical solution for 10/100 Ethernet. The component values and design suggestions in this section might vary for a given application. This section described the function of the various components and how they relate to system performance. With this information the system designer can modify the recommendations with an understanding of the potential impact.

Note: This design recommendation is presently being investigated in the laboratory and through computer simulation. These results will be made available to National Semiconductor customers.

4.0 ICS1890 MII PHYceiver Network Implementation

The ICS1890 PHYceiver integrates all physical layer functions of the IEEE 802.3 10BASE-T and 10BASE-TX from the MII to the isolation transformer of the 10/100 Mb/s magnetics module. This device allows system designers to implement the entire 10/100 Mb/s physical layer channel with one chip, using five passive components to support the on-chip analog circuitry, while keeping the total power consumption under one watt. This section describes how to implement a 10/100 Mb/s adapter using the 21145 and the ICS1890.

Information on ICS products is available at the following website:

http://www.icst.com

4.1 ICS1890 Overview

The ICS1890 incorporates an MII 5-bit symbol interface, allowing easy connection to the MAC layer. The interface operates in IEEE standard MII mode for both 10BASE-T and 100BASE-TX.

The ICS1890 employs autonegotiation logic that has three main features.

- Determines the capabilities of the remote link partner
- Advertises its own capabilities to the remote link partner
- Automatically adjusts to the highest performance common operating mode

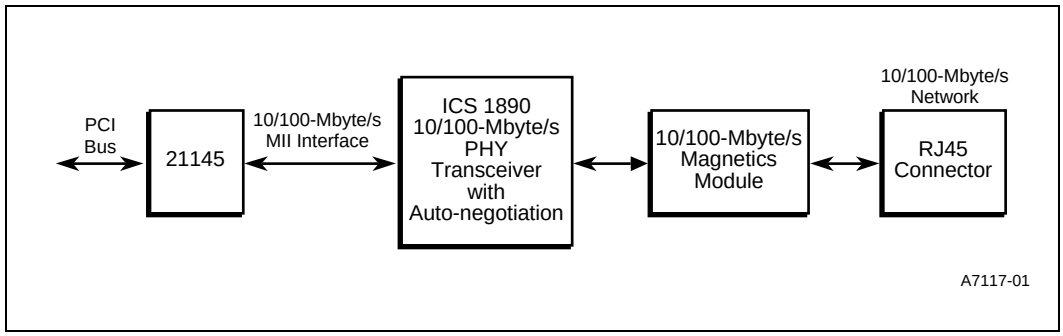
The ICS1890 autonegotiation logic is designed to operate with legacy 10BASE-T networks or newer systems with multiple connection technology options. When operating with a legacy 10BASE-T remote partner, the ICS1890 selects the 10BASE-T operating mode transparent to the remote partner. This allows the preservation of existing legacy network structures without management intervention. Legacy 100BASE-TX devices that do not support autonegotiation are also identified and handled by the ICS1890.

4.2 ICS1890 Block Diagram

Figure 17 shows the physical layer design for the 10BASE-T and 100BASE-TX ICS1890 single-chip implementation and standard MII interface to the 21145 MAC.

The ICS1890 implements a fully compliant IEEE 802.3 MII for connection to MACs or repeaters. This allows connection between the ICS1890 and MAC either on the same board or on a motherboard/daughtercard.

Figure 17. ICS1890 Block Diagram



4.3 ICS1890 Schematic Diagram Description

This section provides a schematic description of the implementation of a complete 10/100 Mb/s physical layer transceiver application from the MII to the RJ45 connector (using the ICS1890). It also provides an external component listing and information for selecting a 10/100 Mb/s magnetics module for the ICS1890 PHY device.

4.3.1 External Component Requirements

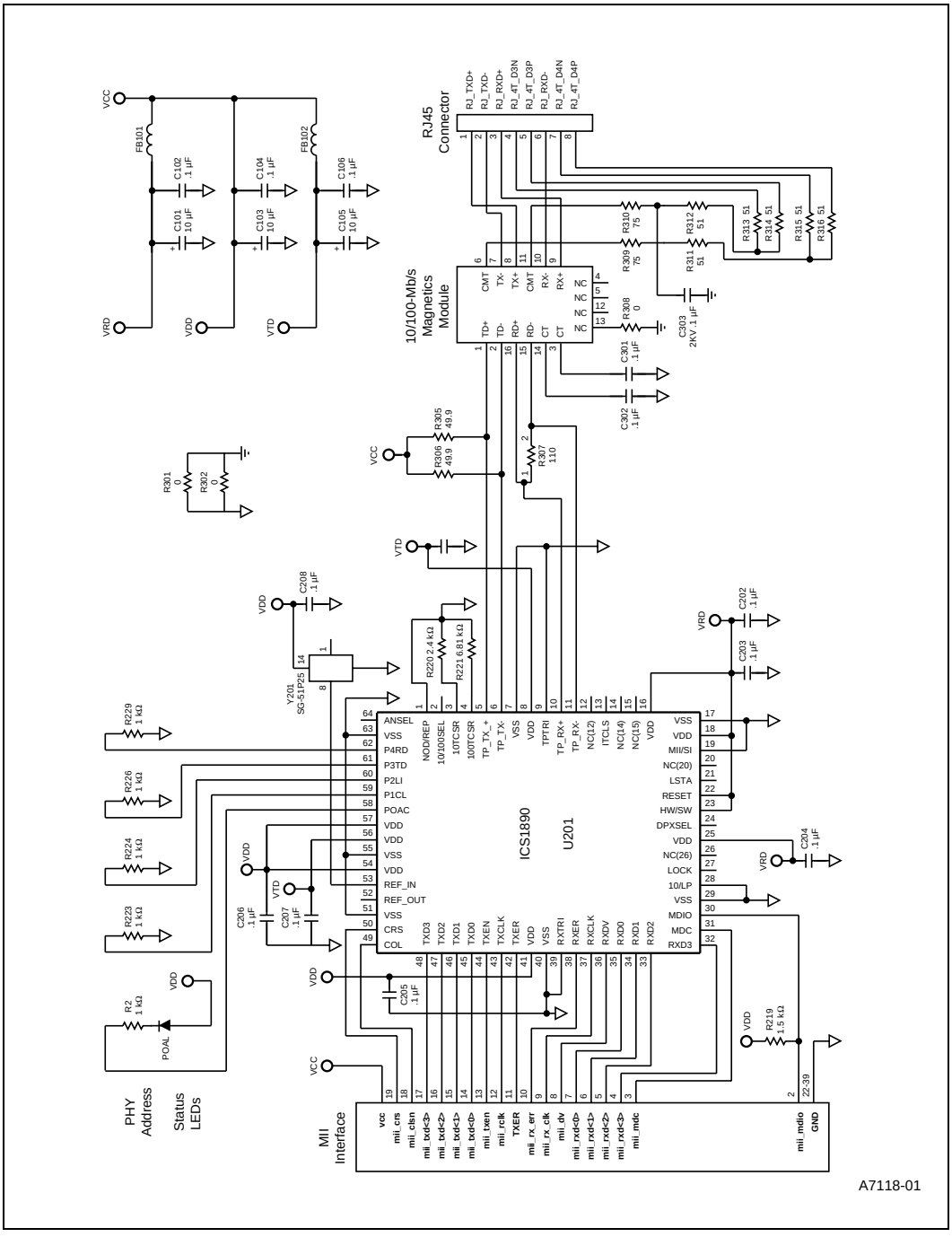
The ICS1890 connects directly to the MII and requires only five additional passive components to set transmit currents and match impedances. In addition, the design is comprised of the following components:

- 25 MHz clock oscillator
- MII PHY address LED or resistor
- Off-the-shelf, 10/100 Mb/s magnetics module
- Unused pair of termination resistors
- Normal bypass and decoupling capacitors

4.3.2 Schematic Information

Figure 18 shows detailed schematic information for the ICS1890 PHY device.

Figure 18. ICS1890 Schematic Diagram



4.3.3 External Component Listing

Table 15 lists the external components used with the ICS1890 in Figure 18. Only five resistors are required for the analog circuitry build. Two of the resistors are used to precisely set the transmit currents for 10BASE-T and 100BASE-TX. The remaining three resistors are used to match the impedance of the twisted-pair cabling. Other components are used optionally to enhance system design when using an MII connector or multiple LED indicators.

Table 15. ICS1890 External Components

Component	Description	Qty	Comments
Resistor	2.4 kΩ, 1/2 W, 1%	1	10BASE-T transmit current setting
Resistors	49.9 Ω, 1/2 W, 1%	2	Impedance matching
Resistor	110 Ω, 1/2 W, 1%	1	Impedance matching
Resistors[1]	51 Ω, 1/2 W	6	Unused twisted-pair terminations (for termination if desired)
Resistors[1]	75 Ω, 1/2 W	2	Unused twisted-pair terminations (for termination if desired)
Resistor	6.81 kΩ, 1/2 W, 1%	1	100BASE-TX transmit current setting
Resistor[1]	1.5 kΩ, 1/2 W	1	MDIO pull-up, optional if internal to the MAC
Resistors[1]	1 kΩ, 1/2 W	5	For LEDs (nominal range 510 Ω to 10 kΩ, 1/2 W)
Capacitors	0.1 µF	14	For supply bypass
Capacitors	10 µF	3	For supply decoupling
LED[1]	—	1	—
Ferrite beads or inductors	—	2	21145 and transmit/receive isolation
10/100 Mb/s magnetics module	—	1	Section 4.3.4 provides recommendations
Oscillator[1]	25 MHz, ±50 PPM	1	Values true for all conditions. A frequency reference with the same performance can also be substituted
RJ45 connector	—	1	Network connection

1. Component(s) not required for all system designs.

4.3.4 10/100 Mb/s Magnetics Module Selection

Table 16 lists some of the vendor magnetic modules that are compatible with the ICS1890 10/100 Mb/s, twisted-pair, PHY transceiver. These modules are off-the-shelf type modules designed for use with 10/100 Mb/s Ethernet devices.

Two configuration styles are available:

- No choke style
- Extra choke style

The no choke style in Figure 20 has an exposed center tap on the transmit side, therefore, it does not have a primary side common-mode choke.

The extra choke style adds a common-mode choke to the primary of the transmit side. This is possible because the ICS1890 drives the transmitter 1:1 for both 10BASE-T and 100BASE-TX.

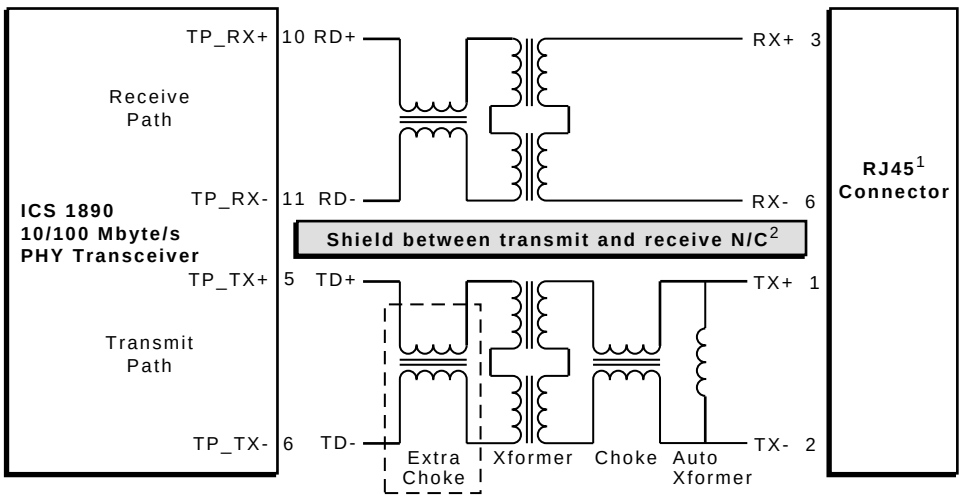
Table 16 lists the vendors that provide pin-compatible modules using the no choke style and the extra choke style transformers. Some vendors offer more than one type of module.

Table 16. 10/100 Mb/s Magnetic Module Vendors

Manufacturer	No Choke Style Part Number	Extra Choke Style Part Number
Bel Fuse	—	S558-5999-01
Halo (singles) – With extra choke – No choke – 3-wire choke (in place of autotransformer)	 TG32-3506ND TG22-3506ND TG32-S020ND	 TG22-S010ND — —
Nano Pulse	NP16170-30	NP16120-30
Pulse Engineering Valor	PE-68515 ST6118 ST6116	PE-68517 SF6035
Nano Pulse (SIP package)	—	NP16120-00

Figure 19 shows the data paths for the 10/100 Mb/s magnetics module.

Figure 19. 10/100 Mb/s Magnetics Module Data Paths



Notes:

[1] The RJ45 pinout shown is for the NIC side of the link. The hub side typically implements crossover function by swapping the 3 and 6 and 1 and 2 pairs.

[2] The shield between transmit and receive is an option that is available from some vendors like Nano Pulse. A 0 Ω resistor connection from this pin to the shield ground should be used so that this pin can be left not connected (N/C) when using modules that do not support a shield.

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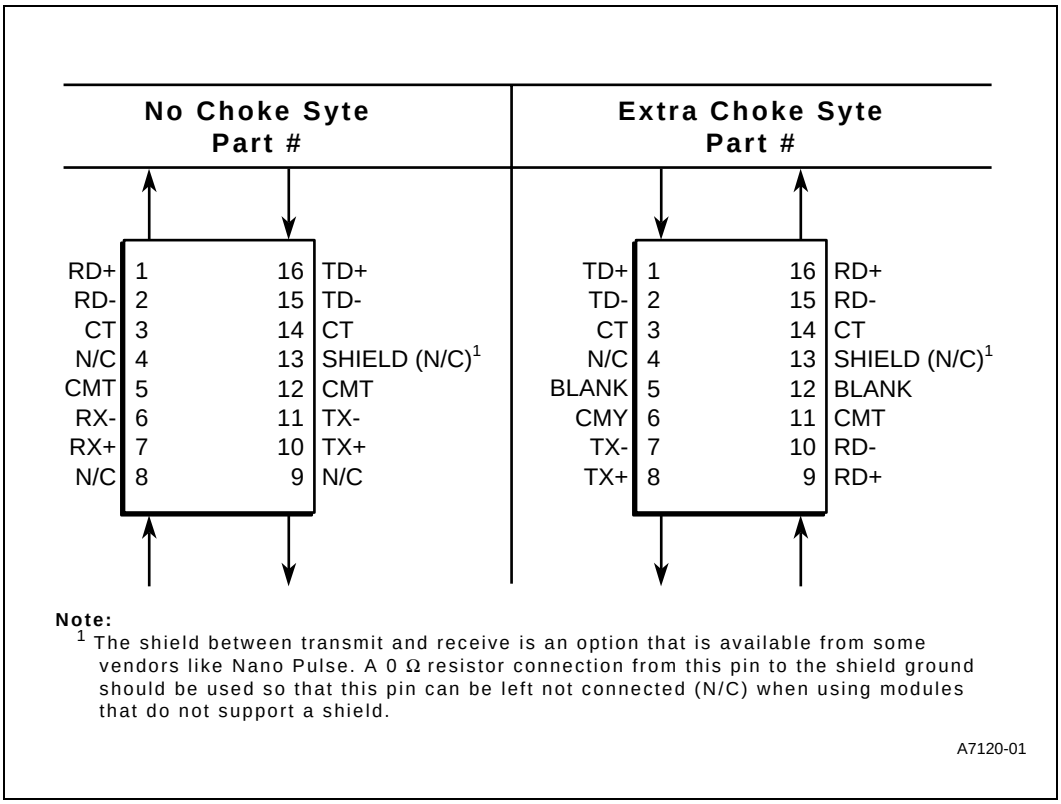
Figure 20 shows the footprints for both the no choke style and extra choke style transformers.

Figure 20. No Choke, Extra Choke Style Transformer Footprints



Note:
[1] The shield between transmit and receive is an option that is available from some vendors like Nano Pulse. A 0 Ω resistor connection from this pin to the shield ground should be used so that this pin can be left not connected (N/C) when using modules that do not support a shield.

A7120-01

4.3.5 MII Data Interface

The MII data interface is a specification of signals and protocols that formalizes the interface of a 10/100 Mb/s Ethernet MAC to the underlying physical layer. This specification supports 100BASE-TX, 100BASE-T4, and 100BASE-FX physical type media transparently to the MAC. Table 17 maps the 21145 MII interface to the ICS1890 MII interface.

Table 17. 21145 to ICS1890 Interface Signal Mapping

Signal	21145	144-Pin	176-Pin	ICS1890	Pin
Transmit clock	mii/sym_tclk	124	153	TXCLK	43
Transmit enable	mii_txen/sym_txd<4>	123	152	TXEN[1]	44
Transmit error	—	—	—	TXER[1]	42
Transmit data 3	mii/sym_txd<3>	119	148	TXD3	48
Transmit data 2	mii/sym_txd<2>	120	149	TXD2	47
Transmit data 1	mii/sym_txd<1>	121	150	TXD1	46
Transmit data 0	mii/sym_txd<0>	122	157	TXD0	45
Receive clock	mii/sym_rclk	128	160	RXCLK	37
Data valid	mii_dv	129	161	RXDV	36
Receive error	mii_rx_err/sel10_100	127	159	RXER	38
Receive data 3	mii/sym_rxd<3>	133	165	RXD3	32
Receive data 2	mii/sym_rxd<2>	132	164	RXD2	33
Receive data 1	mii/sym_rxd<1>	131	163	RXD1	34
Receive data 0	mii/sym_rxd<0>	130	162	RXD0	35
Carrier sense	mii_crs/sd	117	146	CRS	50
Collision detect	mii_clsn/sym_rxd<4>	118	147	COL	49
Management data clock	mii_mdc	134	166	MDC	31
Management data input/output	mii_mdio	135	167	MDIO	30

1. The 21145 does not support the transmit error function, so this pin should be grounded.

The MII data interface specifies both a 4-bit transmit path and a 4-bit receive path allowing for a transfer of a data nibble. The transmit path includes a transmit clock for synchronous transfers, a transmit enable signal, and a transmit error signal. The receive path includes a receive data clock for synchronous transfers, a receive data valid signal, and a receive error signal. The ICS1890 sources both the transmit clock and receive clock.

4.3.5.1 Carrier Sense and Collision Detect Signals

Table 18 describes the operation of the MII Carrier Sense and Collision Detect signals.

Table 18. MII Carrier Sense and Collision Detect Signal Operation

In...	Carrier sense is...	Collision detect is...
Half-duplex mode	True when data is being transmitted or received.	True when data is being received while a transmission is in progress.
Full-duplex mode	True when data is being received.	Always false. Collisions never occur in this mode.

4.3.6 LED and PHY Pins

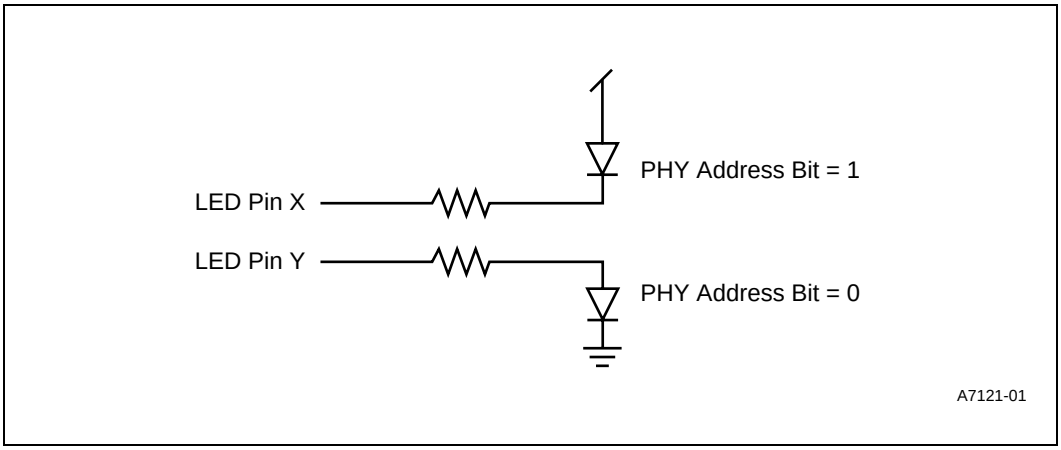
The ICS1890 device uses a unique pin-sharing scheme that allows the five LED pins to also be used to set the PHY address. During power-up and reset, these pins define the address of the PHY device. Following power-up and reset, these pins are used as status indicators.

The address of the PHY can be any number from 0 to 31. If an address of 0 is used for the PHY, the MII interface is isolated on power-up or reset and must be enabled through the MII management port (register 0, bit 10) as defined by the IEEE specification. All other address selections leave the MII interface active by default.

If both the 21145 and the ICS1890 are mounted directly on the same printed circuit board, an address of 1 for the PHY is recommended.

The actual value that is used for the individual address of the PHY depends on the configuration of the LED components (see Figure 21). When a value of “1” is needed, the LED and resistor are connected between the LED pin and Vdd (LED pin X). When a value of “0” is needed, the LED and resistor are connected between the LED pin and ground (LED pin Y). The special driver senses the polarity and adjusts its drive logic to appropriately turn the LED on or off. Resistor values should be in the range of 510 Ω to 10 kΩ (1/2 W). The recommended resistor value is 1 kΩ (1/2 W).

Figure 21. Configuring LED Components



If LEDs are not required for your application, only a resistor is required to set the address of the PHY. If LEDs are not required for your application and the ICS1890 will not be accessed by the serial MII management interface, only a single resistor to Vdd on any one of the LED pins is required. This ensures that the address of the PHY is not 0, preventing the ICS1890 from being powered up in an isolated state without an enable from management to the MII interface.

4.3.7 ICS1890 Power Supply and Layout Considerations

It is very important to properly isolate the ICS1890 10/100 Mb/s PHY device from noise sources in a system design. The following are the two main areas of consideration for filtering noise:

- Isolation from 21145 noise
- Noise coupling between the ICS1890 transmitter and receiver

Two methods for isolating the 21145, transmit, and receive power supplies are described in Table 19.

Table 19. Methods for Filtering Noise

Method	Description
Using a single Vdd plane	Isolate the supply domains with ferrite beads and point-to-point routing as described in Table 20 and Figure 22. The corresponding ground pins are tied directly below to a single internal layer ground plane.
Using split **Vdd** planes	Connect the power pins to the planes directly below them (except for pin 56 which must be point-to-point trace routed as shown in Figure 27). As with the single Vdd method, all ground pins are tied directly below to a single ground plane.

Filtering for the ICS1890 is accomplished by separating the power supply into three domains:

- 21145
- Transmit
- Rreceive

Table 20 lists all supply pins on the device into one of these three categories. Each supply pin is followed directly by its corresponding ground pin. Supply pins are shown paired up with their appropriate neighbor for bypass purposes. All ground pins are tied to a single ground plane below. Each supply pair should be bypassed with a 0.1 µF capacitor located as close to the device as possible.

Table 20. Power Supply Filtering

21145 Domain	Transmit Domain	Receive Domain
41 Vdd 40 Vss	8 Vdd 7 Vss	16 Vdd 18 Vdd 17 Vss
54 Vdd 51 Vss	56 Vdd 55 Vss	25 Vdd 29 Vss
57 Vdd 63 Vss	—	—

Figure 22 illustrates a single Vdd plane isolation with point-to-point trace routing. The 21145 domain Vdd pins drop directly down to the single power plane while the transmit and receive domain pins are isolated using point-to-point routing and in-line ferrite beads.

Figure 22. Single Vdd Plane Isolation

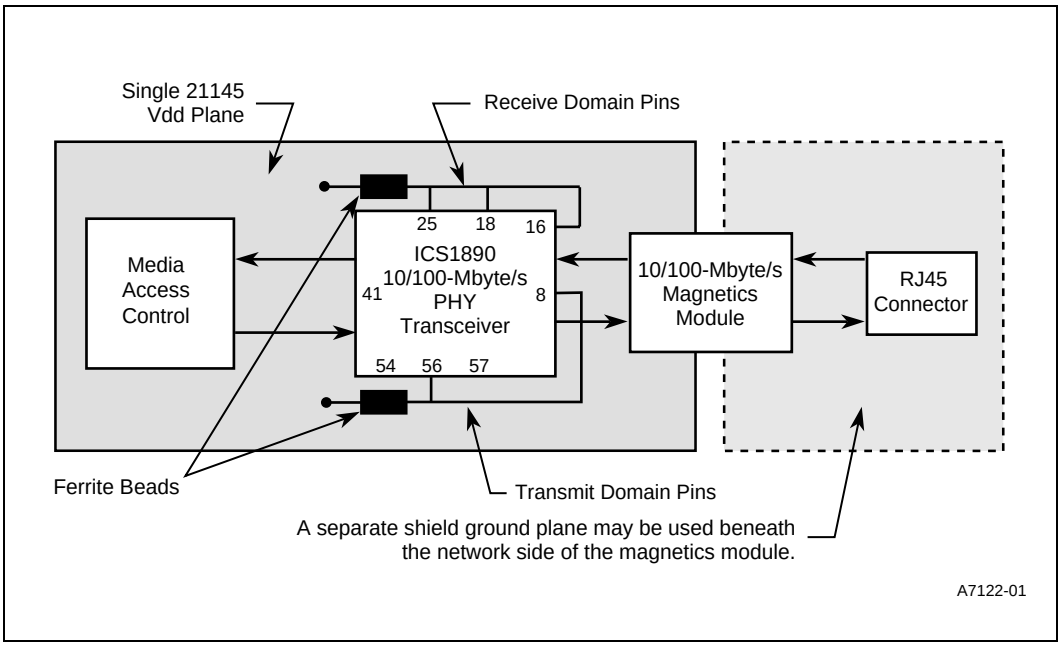
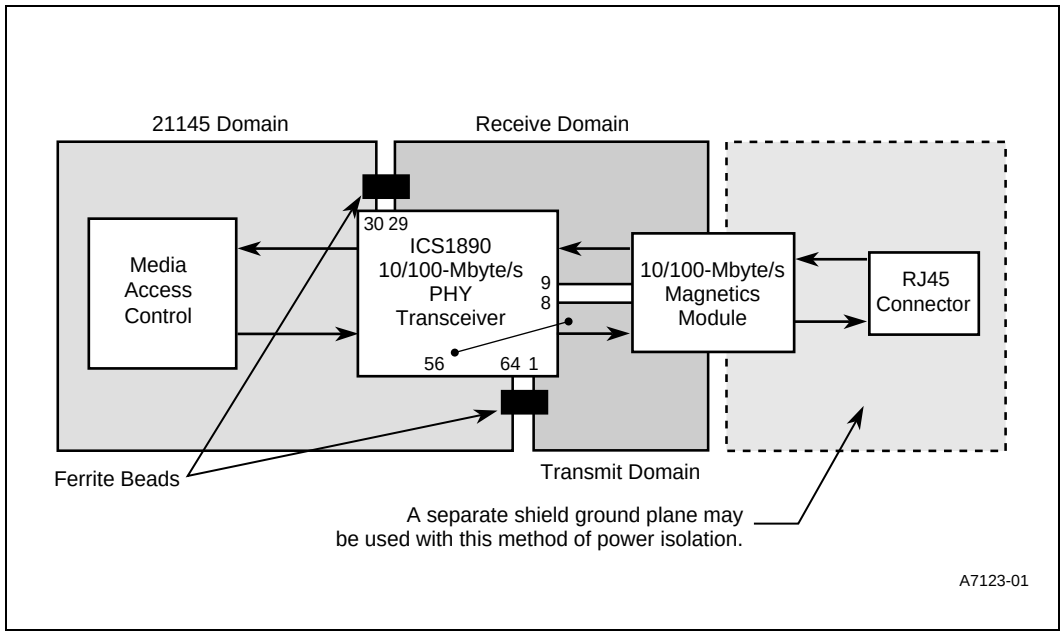


Figure 23 illustrates split Vdd planes power supply isolation. The power planes must be split as shown in this figure. The pin number callouts specify where the power plane splits should occur in the board. Note that pin 56, transmit Vdd, is above the 21145 domain Vdd plane. This pin must be point-to-point trace routed to the transmit domain power plane as shown. All other power pins besides pin 56 connect directly to their corresponding power planes below them. A single, uniform plane should be used for ground. Both the receive and transmit domains should be connected to the 21145 domain through a ferrite bead or inductor.

Figure 23. ICS1890 Power Management Considerations



4.3.7.1 Power Management Considerations

The ICS1890 supports the following two power saving modes:

- Low power—Activated by holding the RESET pin continuously low or by writing a logic one to the power-down bit (status register 0, bit 11). When the device is in low-power mode, all functions are disabled except for register access through the MII management interface. All register values are maintained during low-power mode, except for latching status bits that are reset to their default values.
- Automatic 100BASE-T power-down—Automatically reduces total power requirements when operating in 10BASE-T mode by powering down the 100BASE-TX modules.

Table 21 describes the power consumption values.

Table 21. ICS1890 Power Consumption (Sheet 1 of 2)

Power Consumption Value	Description
Total power consumption	Maximum power consumption is less than one watt and maximum supply current is 195 ma.
Low-power modes: *System reset mode*	Pin 22 held low causes ICS1890 to reset and enter low-power mode. Supply current is approximately 30 mA.

Table 21. ICS1890 Power Consumption (Sheet 2 of 2)

Power Consumption Value	Description
Power-down mode	Status register 0, bit 11, set to a logic 1 causes the ICS1890 to enter low-power mode with only management interface and logic remaining active. This action isolates the transmit data output and the MII. Supply current is approximately 10 mA.
Reference input stop mode	When the 25 MHz clock signal is removed (or stopped) the ICS1890 supply current drops to approximately 30 mA.
Automatic 100BASE-TX power-down mode	Extended control register 2 (register 19), setting bit 0 to a logic 1 with 10BASE-T selected for network connection, automatically turns off the 100BASE-TX transceiver. Automatic 100BASE-TX power-down mode supply current is approximately 100 mA.

Note: Power-down mode supply current values are not tested and are approximated. ICS advises its customers to obtain the latest version of all device data from ICS to verify that any information being relied on by the customer is current and accurate.

4.4 ICS1890 Summary

This section described how to design a 10/100 Mb/s adapter card using the 21145 and the ICS1890. Compatible vendor magnetic modules that use the no choke style and extra choke style were also listed. Layout considerations for filtering noise and isolating the 21145, transmit, and receive power supplies were also provided.

5.0 NWK914 SYM PHY Network Implementation

This section describes how to interface the 21145 with the Mitel Semiconductor's NWK914 HuRiCAN PLUS transceiver and clock recovery device (referred to as the NWK914).

5.1 NWK914 Overview

The NWK914 was designed for three-level signaling at data rates of 100 Mb/s and 10 Mb/s. The NWK914 was designed to operate at cable lengths up to 100 m (328 ft) using 100 Ω Category 5 unshielded twisted-pair UTP or 150 Ω Type 1 shielded twisted-pair STP. The NWK914 incorporates the PHY including the Medium Dependent Interface (MDI), Physical Media Attachment (PMA), and Physical Media Dependent (PMD) sublayers. It interfaces to the Physical Coding Sublayer (PCS) at the symbol level.

Information on Mitel products is available at the following website:

http://www.mitelsemi.com

5.2 NWK914 Operation

For dual 10/100 Mb/s Ethernet operation, correct impedance matching must be achieved to ensure signal integrity in either 10BASE-T or 100BASE-T mode. To minimize cost, electromagnetic relays cannot be used. To overcome these constraints, the solution uses common magnetics for 10/100 Mb/s signaling with a 2:1 transmit and 1:1 receive turns ratio. Two transistors act as a differential amplifier to maintain impedance matching and for regeneration of the 10BASE-T signal. For clarity, the transmit and receive operations are described separately in the next sections for the 10 Mb/s and 100 Mb/s operations.

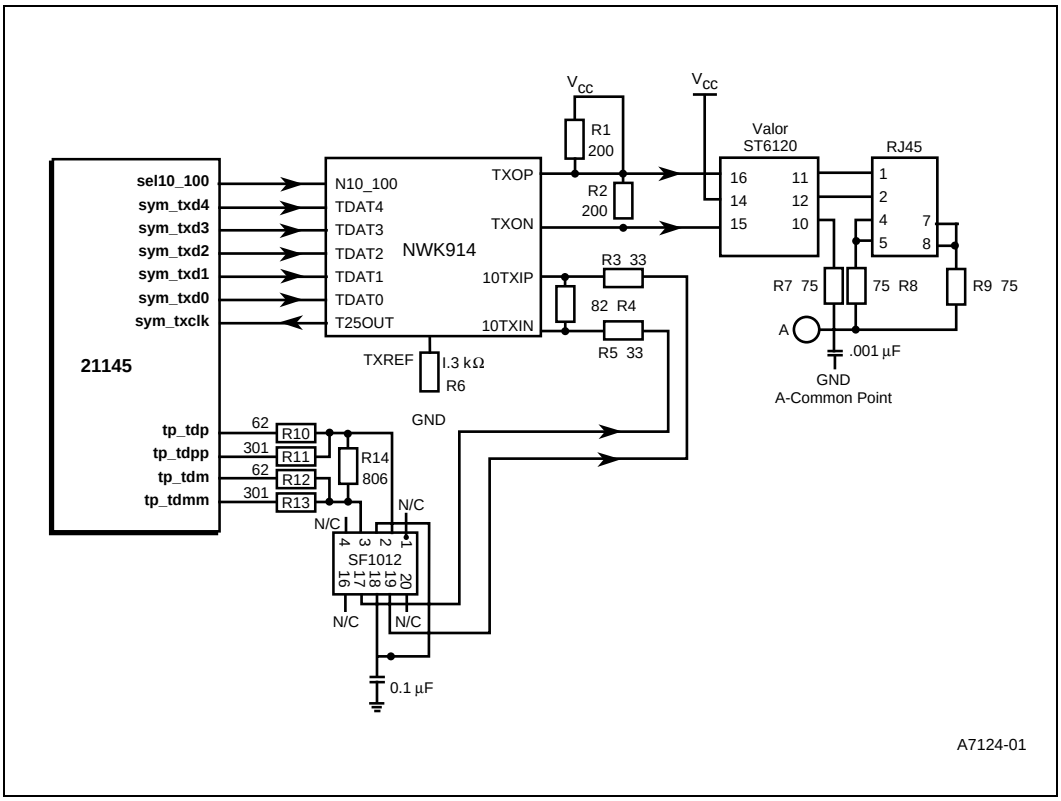
5.2.1 10-Mb/s Transmit Operation

As illustrated in Figure 24, the Intel tp_tdp/m outputs provide the standard 10BASE-T signals without any pulse shaping or filtering. The pulse shaping and filtering is provided by the resistor network (R10-R14) and the Valor SF1012 (which includes the isolation transformer and low-pass filters). The differential signal from the SF1012 is passed via the attenuation network (R3-R5) to the 10TXIP/N inputs of the NWK914 10-Mb/s driver.

The 10BASE-T signal is then buffered and outputs to the line through the NWK914 TXOP/N outputs. The 400-Ω differential impedance presented to the NWK914 outputs provide an ideal termination to absorb reflections due to far-end impedance mismatch. The impedance transfer of the transformer is n 2 where n is the turns ratio. To match the 100 Ω on the cable side of the transformer, the terminating impedance needs to be 400 Ω. To ensure the correct output voltage level, the TXREF resistor is set to 1.3 KΩ (see the GEC Plessey Semiconductor Data Sheet DS4046 1.5). This produces a 10 V peak-to-peak signal on the TXOP/N pins of the NWK914, but this is reduced to the correct 5 V level for Ethernet signaling on the cable side of the transformer due to it being a 2:1 stepdown.

The NWK914 transmitter outputs are controlled by the N10/100 input pin and the 21145 sel10_100 output pin. When the N10/100 is low, the NWK914 operates in 10 Mb/s mode. This automatically sets the correct internal current ratio for the output driver of the NWK914 when in either 10BASE-T or 100BASE-TX mode.

Figure 24. Transmit Operation



5.2.2 100 Mb/s Transmit Operation

As illustrated in Figure 24, the 100 Mb/s mode is selected by a logic high on the N10/100 pin of the NWK914, the signal for which is derived from the sel10_100 pin of the 21145. In 100 Mb/s mode, the NWK914 disables the signal from the 10TXIN/P pins thus isolating the 10 Mb/s signal path. The 100 Mb/s data is sourced directly from the 21145 via the sym_txd0/4 pins, with the 100 Mb/s transmit signals provided on the TXOP/N pins of the NWK914. The differential source impedance of 400 Ω remains the same as that for 10 Mb/s operation.

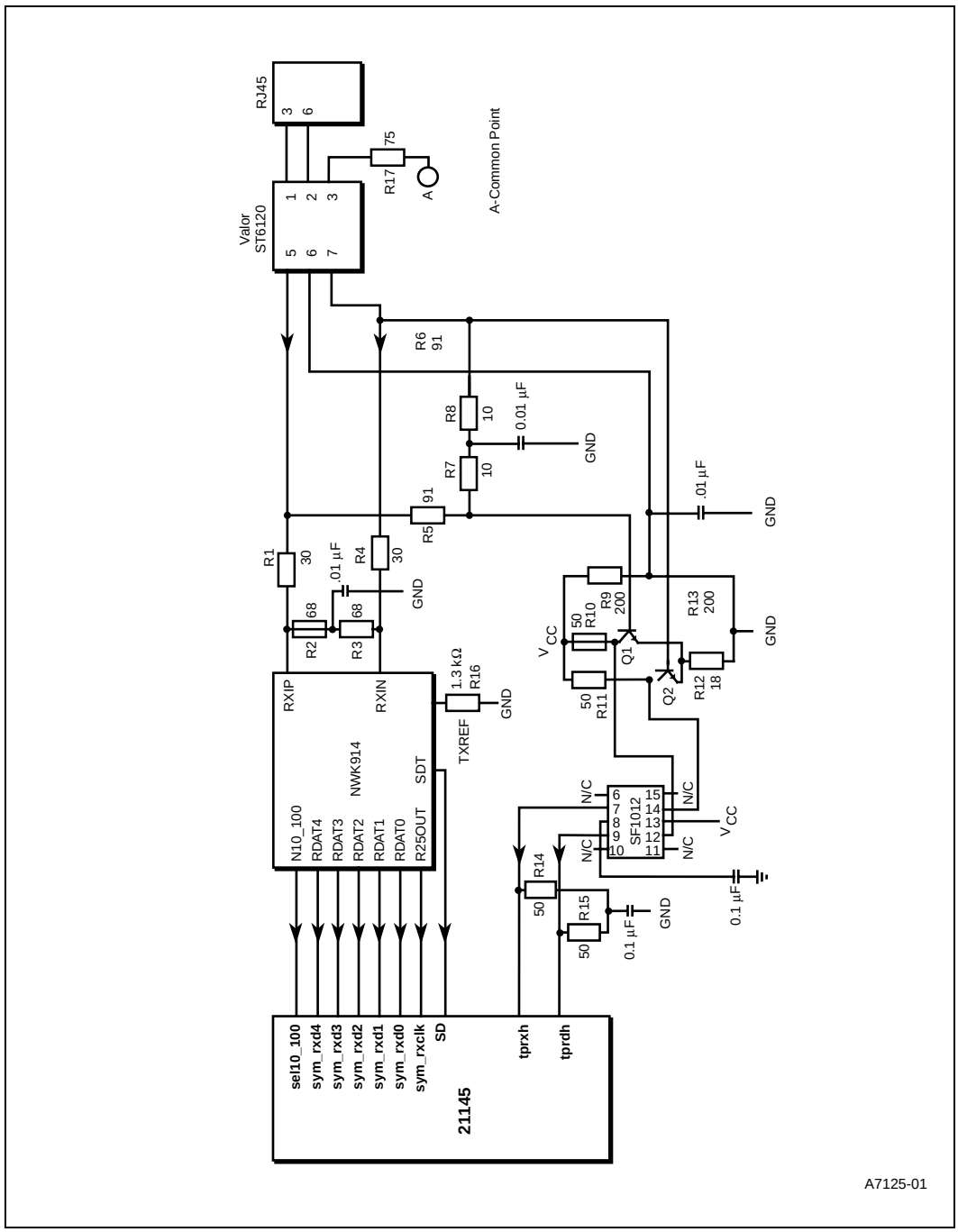
5.2.3 10 Mb/s Receive Operation

Figure 25 illustrates the 10 Mb/s differential signal coupled from the cable by a 1:1 isolation transformer. The 100 Ω receive termination is achieved with the resistive network R1- R4 being 200 Ω in parallel with (R5-R8), which is also 200 Ω. The differential signals then drive the transistors Q1 and Q2 though (R5-R8). These resistors are required to ensure that the transistors Q1 and Q2 do not saturate and degrade the 10BASE-T signal quality. The transistors Q1 and Q2 are biased at Vcc/2~2.5 V via the common-mode choke of the Valor ST6120 1:1 receive transformer and the resistors R9 and R13.

The resistor R12 is selected to provide 100 mA in either collector of Q1 or Q2 to accommodate the 5 V swing required for 10BASE-T operation. It was calculated assuming that V_{bias} =2.5 V, V_{be} =0.7 V, and that I_T =100 mA.

The resistors R11 and R10 provide the correct impedance matching for the Valor SF1020 10BASE-T transformer and filters. The Valor transformer module outputs then drive the 21145 inputs tprxh and tprdh with the resistors R14 and R15 that provide the correct impedance matching for the Valor transformer module.

Figure 25. Receive Operation



5.2.4 100-Mb/s Receive Operation

The 100 Mb/s signal is coupled through the same Valor ST6120 1:1 receive transformer. The 100 Ω forward cable termination is provided by the same R1-R4 and R5-R8 network. Due to the high ß of Q1 and Q2, the shunt resistance is much greater than 100 Ω, and the correct cable termination is maintained.

The NWK914 RXIP/N input pins receive the 100 Mb/s data via the resistive network (R1-R4) to optimize the adaptive equalizer of the NWK914. For standard TP-PMD signaling, the adaptive equalizer requires a signal level of 1.12 V peak-to-peak. Given that 100BASE-TX transmission is 2 V peak-to-peak, the attenuation is approximately 56% provided by R1-R4.

The NWK914 generates a TTL signal detect output. This is asserted upon reception of a signal from the twisted-pair cable that meets the minimum amplitude specification as stated in the TP-PMD standard. The NWK914 SDT output is connected to the 21145 sd input pins. When asserted high, the SDT output indicates to the 21145 that the NWK914 might be receiving a valid 100BASE-TX signal.

5.3 NWK914 Block Diagram

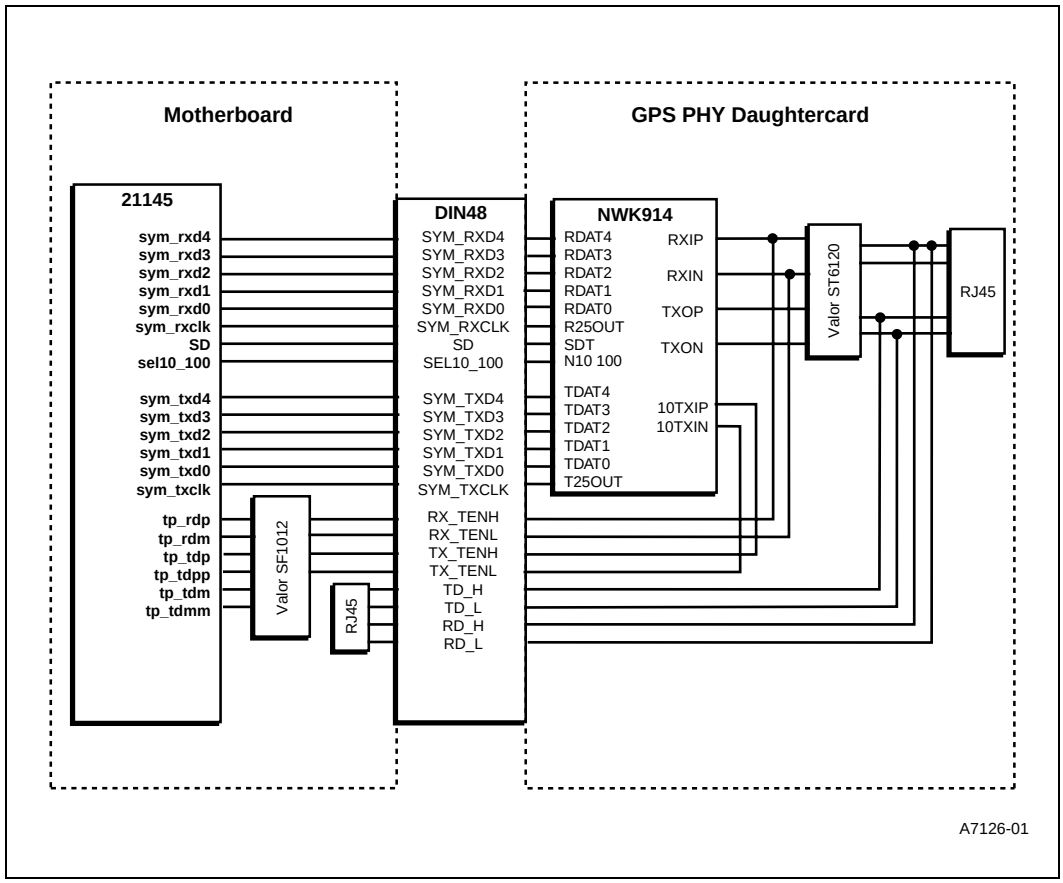
The NWK914 interfaces with the 21145 to provide a low-cost, low-part-count solution. The block diagram in Figure 26 illustrates the GPS daughtercard design that is based upon the design outlined in Section 5.2. It interfaces directly to the 21145 motherboard via a standard 48-pin DIN connector.

The following signals are passed through the 48-pin DIN connector:

- 10 Mb/s transmit signal to the NWK914 10TX buffer
- 10 Mb/s receive data directly to the 21145
- 100 Mb/s symbol data, clock, and control signals from the 21145 to the NWK914
- 100 Mb/s signal to and from the cable can be sourced in either of the following ways:
  a. Through the RJ45-8 on the Intel motherboard, through the connector, and on to the GPS daughtercard
  b. Directly from the GPS daughtercard

     Choice b optimizes 100 Mb/s performance but requires removal of the cable from the Intel board to the GPS board. This is considered a necessary user option because it is not desirable to have 125 Mb/s passing through a connector, which will slow data-edge speeds and potentially increase the noise level on symbol data and clocks. The RJ45-8 on the Intel board can be enabled or disabled with solder links (see Figure 26).

Figure 26. GPS PHY Daughtercard Interface



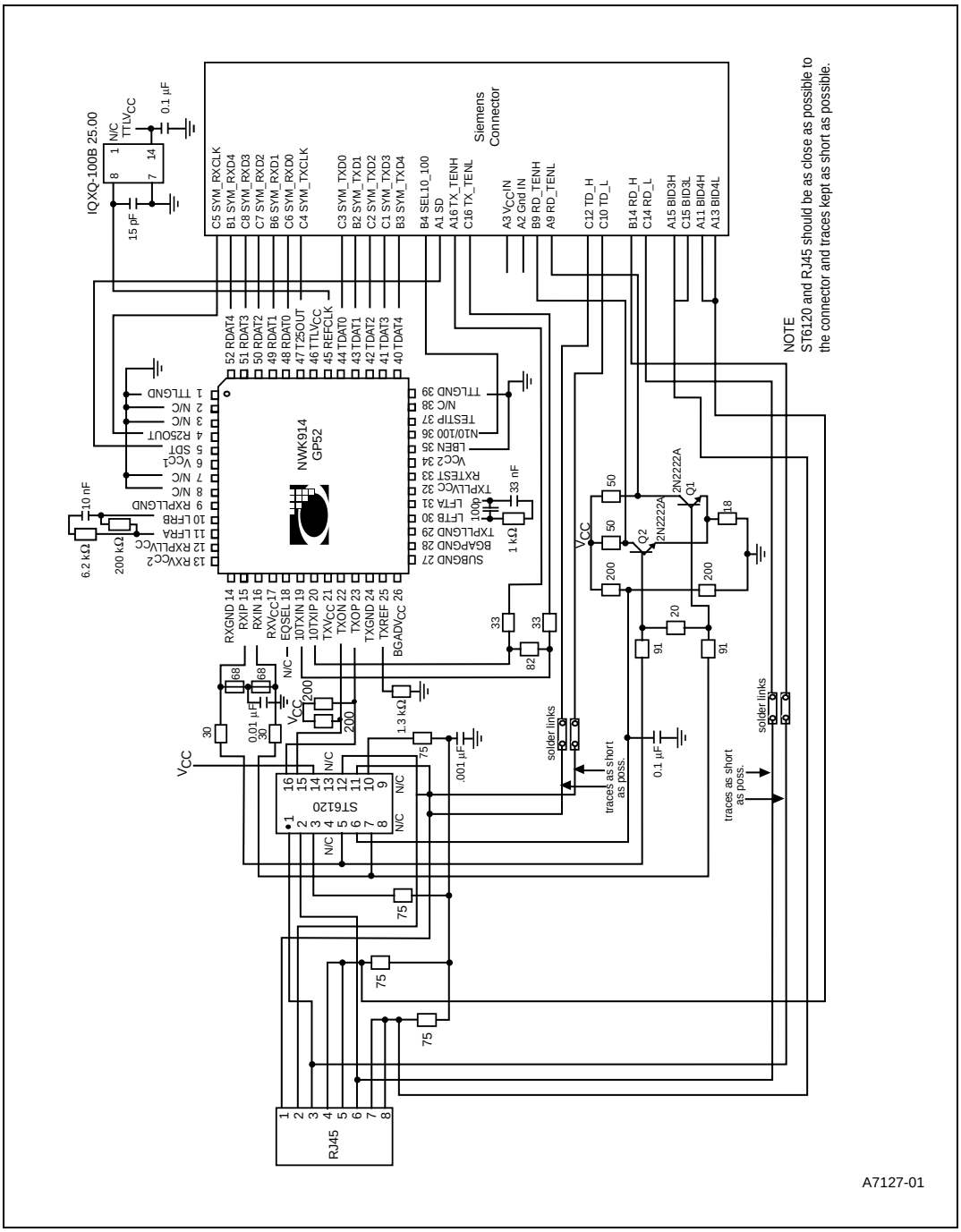
5.4 Using the NWK914

This section provides schematic information, layout considerations, and the power requirements for using the NWK914.

5.4.1 NWK914 Schematic

Figure 27 shows the schematic required to implement the GPS PHY daughtercard.

Figure 27. GPS PHY Daughtercard Schematic



5.4.2 Layout Considerations

In order to ensure robust operation and meet FCC compliant layout, extra considerations must be taken when designing a PCB for high-speed applications. The following parameters should be minimized:

- The distance of connecting high-speed differential data lines between components. These traces should be impedance controlled and of equal length, thus reducing ringing and delay problems.
- The number of corners. Where corners are necessary, they should be smooth and free of right angles (90°) to avoid any high-frequency aerial effects.
- Signal traces changing planes. Avoid changing signal planes to maintain a constant impedance characteristic.
- The distance the solder links are from the GPS RJ45-8. Minimize the distance to reduce signal distortion if the Intel RJ45-8 is unused.

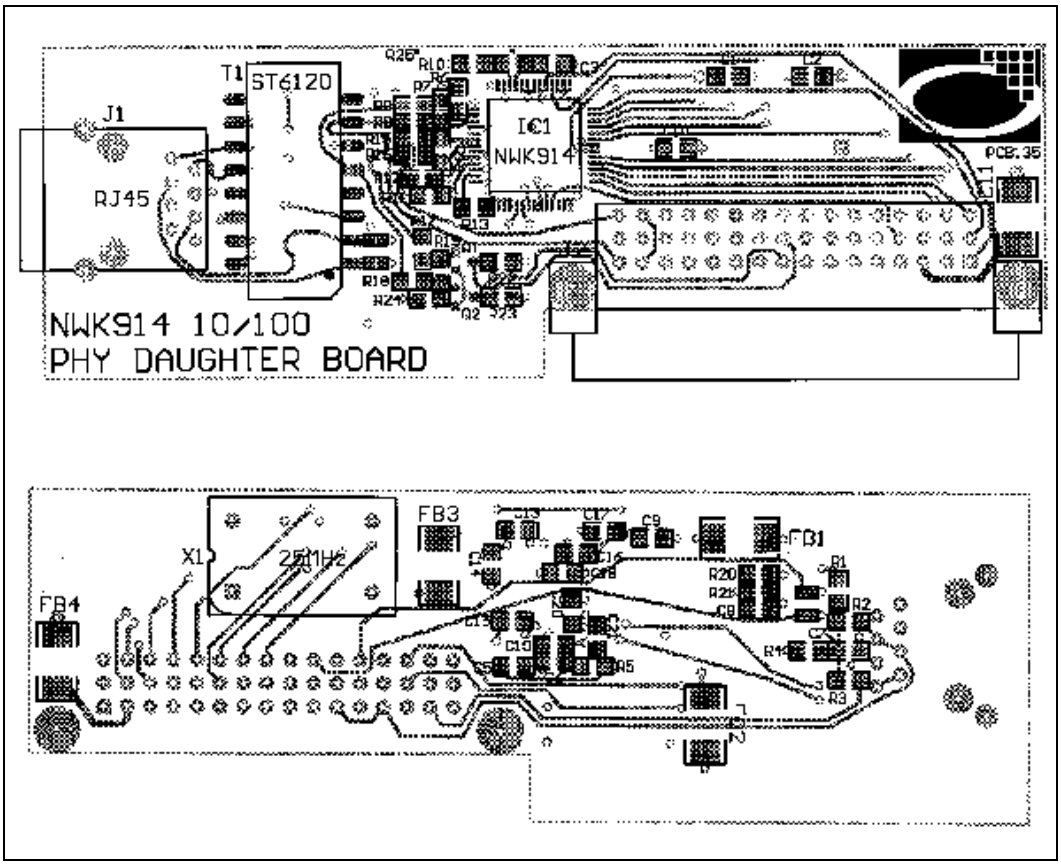
Sensitive data and clock signals should be hand routed, kept as short as possible, and kept away from clock lines (therefore, reducing noise and cross-talk).

Decoupling capacitors and the TX/RX resistors should be placed as close to the NWK914 as possible.

A shielded RJ45-8 CAT5 connector should be used to control impedances within the connector, and to prevent noise pickup. The shield should have a good electrical connection to chassis ground.

The PCB layout for the GPS daughtercard is illustrated in Figure 28.

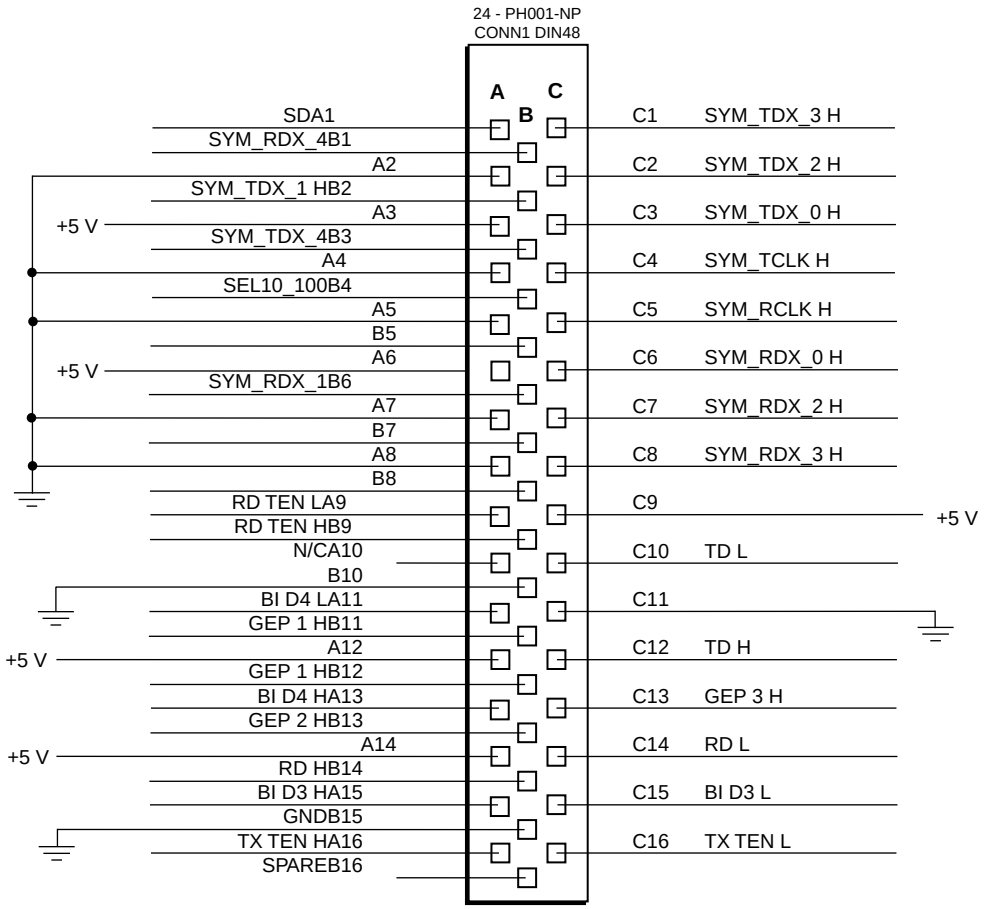
Figure 28. NWK914 10/100 PHY Daughtercard Layout



5.4.3 48-Pin DIN Connector

The specific details of the 48-pin DIN connector are illustrated in Figure 29.

Figure 29. 48-Pin DIN Connector



Note:
C row is the inner row (that is, A row is the closest to the edge of the card)
C16 is the closest pin to RJ45

A7128-01

5.4.4 NWK914 Bill-of-Materials

The bill-of-materials required to build the GPS daughtercard is shown in Table 22.

Table 22. NWK914 Bill-of-Materials

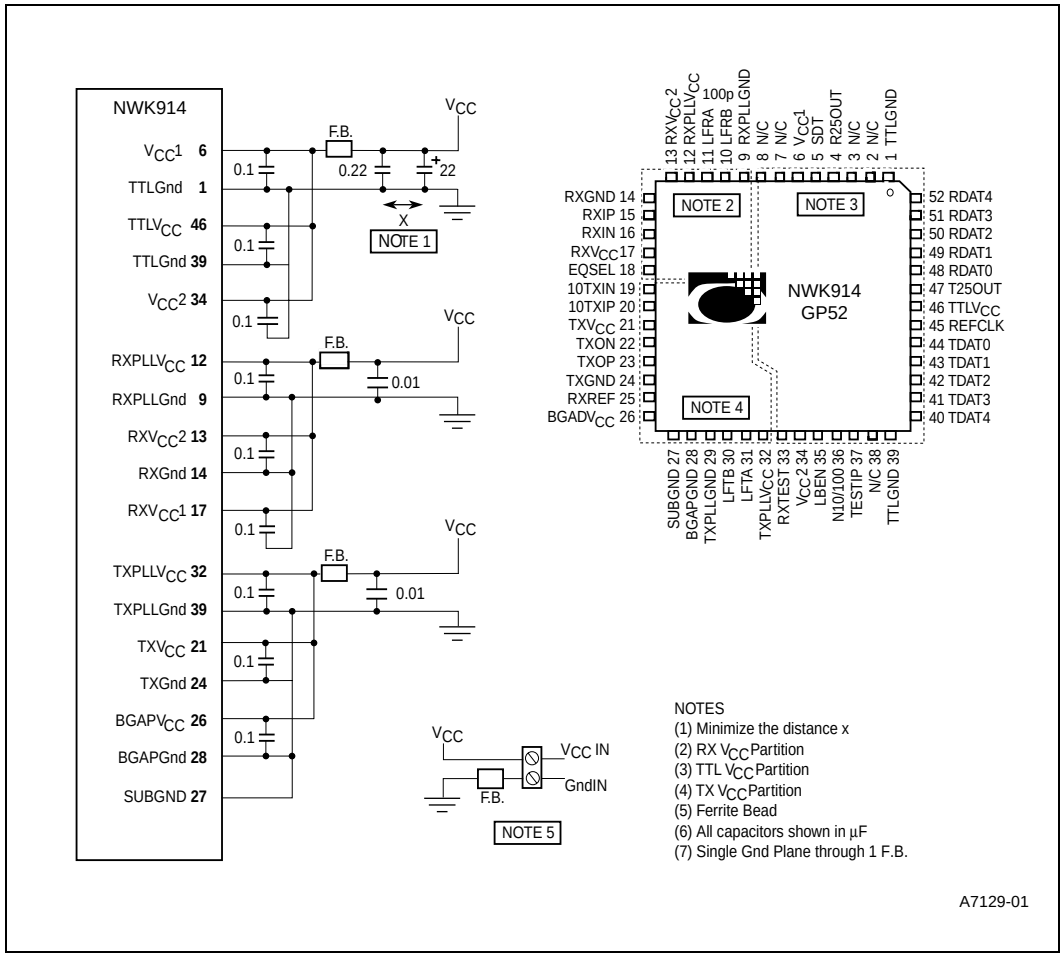
Comment	Pattern	Quantity	Component	Comment	Pattern	Quantity	Component
100 n	805	2	C2, C9	2N2222A	SOT-23 SMBT2222A	2	Q1, Q2
100 P	805	1	C6	33 n	805	1	C5
100 n	805	9	C13, C14, C15, C16, C17, C18, C19, C20, C21	33 R	805	2	R15, R16
10 n	805	2	C3, C8	30 R	805	2	R8, R9
15 P	805	1	C1	51 R	805	2	R22, R23
18 R	805	1	R24	68 R	805	2	R6, R7
1 K	805	1	R5	6.2 K	805	1	R10
1.3 K	805	1	R13	75 R	805	4	R1, R2, R3, R4
1 n	805	1	C7	82 R	805	1	R10
200 K	805	1	R25	91 R	805	2	R17, R18
200 R	805	4	R11, R12, R20, R21	DIN48	DIN48RA	1	J2
20 R	805	1	R19	FERR	1812+	4	FB1, FB2, FB3, FB4
220 n	805	1	C10	NWK914	FPQ52-0.65	1	J1
22 µ	1812+	1	C11	ST6120	'VALOR2' TRAN	1	T1
25 MHz	IQXQ-10 0B25.00	1	X1	—	—	—	—

5.5 Power Requirements

Figure 30 shows the decoupling required for the partitioning of power planes. As shown, the TX and RX power planes should be decoupled with two chip capacitors and a ferrite bead. A continuous ground plane is practical but it can be segmented with ferrite.

The power plane should not extend in the region beyond the magnetics; this prevents noise on the plane from bypassing the common-mode filtering and coupling onto the cable. The ground plane should also not extend in the region directly underneath the magnetics. A fully integrated design including the daughtercard and motherboard, outlined in this document, will be available as a single-board network interface card reference design.

Figure 30. Power Planes and Decoupling for the GPS PHY Daughtercard



5.6 NWK914 Summary

This section showed how the GEC Plessey Semiconductor's NWK914 PHY device provided a cost-effective solution to the Fast Ethernet 100BASE-TX physical layer. It illustrated how to interface the Intel 21145 PCI/CardBus 10/100 Mb/s Ethernet LAN controller to the NWK914 to provide 10/100 Mb/s Ethernet functionality with a low part count and cost.

This design is only to confirm compatibility between the NWK914 and the 21145. The design is not intended to meet Agency Certification requirements. For more details on the availability of the GPS NWK914 and reference design, please contact your local GEC Plessey Semiconductor Customer Service Centre.

6.0 TSC 78Q2120 MII PHY Network Implementation

This section contains the design recommendations for interfacing the TDK Semiconductor 78Q2120 10/100BASE-TX Fast Ethernet transceiver to the 21145.

6.1 78Q2120 Overview

The 78Q2120 is a 10BASE-T/100BASE-TX Fast Ethernet transceiver. It includes integrated MII, ENDECs, scrambler/descrambler, dual-speed clock recovery, and full-featured Auto-Negotiation functions. The transmitter includes an onchip pulse-shaper and a low-power line driver. The receiver has an adaptive equalizer and a baseline restoration circuit required for accurate clock and data recovery.

The transceiver interfaces to Category 5 unshielded twisted-pair (Cat-5 UTP) cabling, and is connected to the line media via 1:1 isolation transformers. No external filter is required. Interface to the MAC is accomplished through an IEEE-802.3 compliant media independent interface (MII). The product is fabricated in a BiCMOS process for high-performance and low-power operation, and can operate from a single 3.3 V or 5 V supply.

Information on TDK Semiconductor products is available at the following website:

http://www.tsc.tdk.com

6.1.1 78Q2120 Features

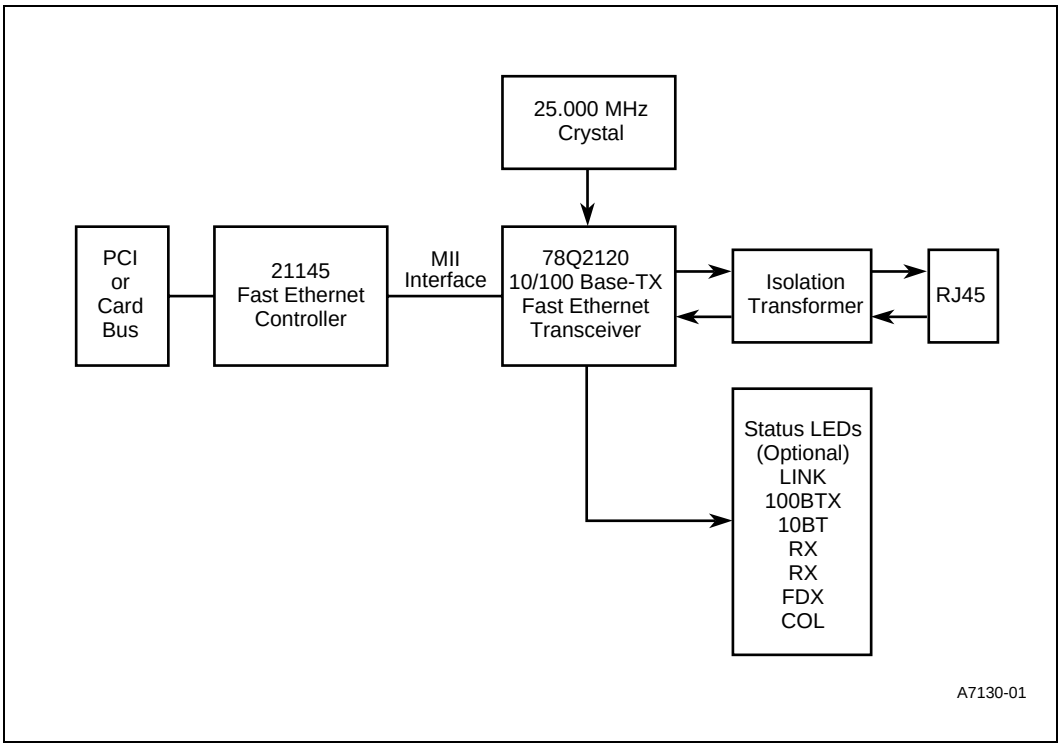
The 78Q2120 features the following attributes:

- 10BASE-T/100BASE-TX IEEE-802.3 compliant TX and RX functions requiring a dual 1:1 isolation transformer interface to the line
- Integrated MII, 10BASE-T/100BASE-TX ENDEC, 100BASE-TX scrambler/descrambler, and full-featured Auto-Negotiation function
- Full-duplex operation capable
- PCS bypass supporting a 5-bit symbol interface
- Dual-speed clock recovery
- Automatic polarity correction during Auto-Negotiation and 10BASE-T signal reception
- LED indicators: LINK, TX, RX, COL, 100, 10, FDX
- User programmable interrupt pin
- General-purpose I/O interface
- 80-Lead TQFP package, 12 mm x 12 mm x 1.5 mm
- Power-saving and power-down modes
- BiCMOS technology, operating with a single 3.3 V or 5 V supply
- 320 mW typical 100BASE-TX power dissipation

6.2 78Q2120 Block Diagram

Figure 31 is the system diagram for a 78Q2120 PHY to 21145 MAC connection. The 78Q2120 provides a single chip 10BASE-T and 100BASE-TX implementation with an IEEE 802.3 MII interface. The 78Q2120 and 21145 comprise an efficient network interface.

Figure 31. 78Q2120 Block Diagram



6.3 78Q2120 Description

6.3.1 Supply Voltage and Power Management

The 78Q2120 can operate from either a single 3.3 V (10%) or 5 V (10%) power supply. The chip automatically adapts to the supply voltage used. No pin configuration is required.

The TSC 78Q2120 has two power-saving modes:

- Chip power-down
- Receive power management

Chip power-down is activated by setting the PWRDN bit in the MII register (MR0.11) or pulling high the PWRDN pin. When the chip is in power-down mode, all on-chip circuitry is shut off, and the device consumes minimum power. While in power-down state, the 78Q2120 still responds to management transactions.

Receive-power management (RXCC mode) is activated by setting the RXCC bit in the MII register (MR16.0). In this mode of operation, the adaptive equalizer, clock recovery phase lock loop (PLL), and transmitter circuitry will be powered down when no valid signal is present at the UTP receive line interface. As soon as a valid signal is detected, all circuits will **a**utomatically be powered up to resume normal operation. During this mode of operation, RX_CLK and TX_CLK will be inactive when there is no data being received. See Table 23 for the recommended operating conditions and Table 24 for the power consumption.

Note: The RXCC mode is not supported during 10BASE-T operation.

Table 23. TSC 78Q2120 Recommended Operating Conditions

Parameter	Specification
DC Voltage Supply	Vcc 3.3 V 10%, 5 V 10% Vdc
Ambient Operating Temperature, T_a	0–70 degrees C

Table 24. 78Q2120 Power Consumption

Parameter	Symbol	Conditions	Nominal	Maximum	Unit
Supply Current	Icc	Vcc=3.3 V Auto-Negotiation 10BT (Idle) 10BT (Normal Activity) 10BT (Peak) 100BTX	 25 25 85 95	 30 30 100 155 115	mA
Supply Current	Icc	Vcc=5.0 V Auto-Negotiation 10BASE-T (Idle) 10BASE-TX (Normal Activity) 10BASE-T (Peak) 100BASE-TX	 30 30 90 105	 35 35 115 170 135	mA
Supply Current	Icc	Power-down mode RXCC mode	500 5	800 10	uA mA

6.3.2 TX and RX Clock Selection

The 78Q2120 defaults to using the onchip crystal oscillator. In this mode, a 25 MHz crystal is connected between the XTLP and XTLN pins. The CKIN pin should be tied low. Alternately, an externally generated 25 MHz clock can be connected to the CKIN pin. The chip senses activity on the CKIN pin, and will automatically configure itself to use the external clock. In this mode of operation, a crystal is not required and the XTLP and XTLN pins should be connected.

The transmitter uses an onchip frequency synthesizer to generate the transmit clock. In 100BASE-TX operation, the synthesizer multiplies the reference clock to obtain the internal 125 MHz serial transmit clock. In 10BASE-T mode, it generates an internal 20 MHz transmit clock. The synthesizer references either the local 25 MHz crystal oscillator or the externally applied clock.

The integrated signal qualifier has separate squelch and unsquelch thresholds, and includes a built-in timer to ensure fast and accurate signal detection and receive noise rejection. Upon detection of valid 10BASE-T or 100BASE-TX pulses on the line receive port, the adaptive circuits are allowed to lock onto the incoming data.

In 100BASE-TX mode, the 125 MHz receive clock is extracted using a narrow-band PLL. When no receive signal is present, the PLL is directed to lock onto the transmit 125 MHz clock. When a valid signal is present, the PLL uses the received NRZI signal as the clock reference. The recovered clock is used to retime the data signal and for conversion of the data to NRZ format.

In 10BASE-T mode, the 10 MHz clock is recovered using a PLL. For fast acquisition, the receive PLL is locked onto the transmit reference clock during idle receive periods. When Manchester-coded preambles are detected, the clock recovery PLL immediately adjusts its phase and resynchronizes with the incoming Manchester data.

6.3.3 100BASE-TX Transmit and Receive

The 78Q2120 contains all of the necessary circuitry to convert the transmit MII signaling from a MAC to an IEEE-802.3 compliant datastream driving Cat-5 UTP cabling. The internal PCS interface maps 4-bit nibbles from the MII to 5-bit code groups as defined in Table 24-1 of IEEE-802.3. These 5-bit code groups are then scrambled and converted to a serial stream before being sent to the MLT-3 pulse-shaping circuitry and line driver. The pulse-shaper uses current modulation to produce the desired output waveform. Controlled rise/fall times in the MLT-3 signal are achieved using an accurately controlled C/I filter. The line driver requires an external 1:1 isolation transformer to interface with the line media. The center-tap of the primary side of the transformer should be connected to Vcc.

The 78Q2120 receives a 125Mb MLT-3 signal from Cat-5 UTP cable through a 1:1 transformer. The signal then goes through a combination of adaptive offset adjustment (baseline wander correction) and adaptive equalization. The equalized MLT-3 data signal is then sliced and the resulting bit stream is presented to the clock recovery PLL and to a serial-to-parallel converter. The parallel data from the converter is then descrambled and aligned into 5-bit code groups. The receive PCS interface maps these code groups to 4-bit data for the MII as outlined in Table 24-1, in Clause 24 of IEEE-802.3.

The PCS bypass mode is entered by pulling PCSBP high. In this mode the 78Q2120 accepts scrambled 5-bit code into the pins TX_EN and TXD[3:0]. TX_EN is the MSB data input. The 5-bit code groups are converted to an MLT-3 signal.

The received MLT-3 signal is converted to 5-bit NRZ code groups and output from the RX_ER and RXD[3:0] pins. The RX_ER pin is the MSB data output. The RX_DV and TX_EN pins are unused in PCS bypass mode.

6.3.4 10BASE-T Transmit and Receive

The 78Q2120 takes 4-bit parallel NRZ data via the MII interface and passes it through a parallel-to-serial converter. The data is then passed through a Manchester encoder and, to the twisted-pair pulse-shaping circuitry and twisted-pair drive circuitry. An advanced pulse-shaper employs a Gm-C filter to predistort the output waveform to meet the output voltage template and spectral content requirements detailed in Clause 14 of IEEE-802.3. Interface to the twisted-pair media is through a center-tapped 1:1 transformer; no external filtering is required. During Auto-Negotiation and during 10BASE-T idle periods, link pulses are transmitted.

The 78Q2120 employs an onboard timer to prevent the MAC from capturing a network through excessively long transmissions. When this timer is exceeded, the chip enters the jabber state and transmission is disabled.

The 78Q2120 receives Manchester encoded 10BASE-T data through twisted-pair inputs reestablishing logic levels through a slicer with a smart squelch function. The slicer automatically adjusts its level after valid data when appropriate levels are detected. Data is passed to the 10BASE-T PLL, where the clock is recovered and data retimed and passed through a Manchester decoder. From there data enters the serial-to-parallel converter for transmission to MAC via media independent interface. Interface to twisted-pair media is through a 1:1 center-tapped transformer; no external filtering is required.

The 78Q2120 is capable of either automatic or manual polarity reversal for 10BASE-T and Auto-Negotiation. These features are controlled by register bits MR16.5 and MR16.4. The default is automatic mode, where MR16.5 is low and MR16.4 indicates that the detection circuitry has inverted the input signal. To enter manual mode, MR16.5 is set high and MR16.4 controls the signal polarity.

6.3.5 Auto-Negotiation

The 78Q2120 supports the Auto-Negotiation functions in Clause 28 of IEEE-802.3. This function can be enabled via a pin strap to the device or through registers. If the ANEGA pin is tied high, the Auto-Negotiation function defaults to on and bit MR0.12, ANEGEN, is high after reset. Otherwise, the function defaults to off and bit MR0.12 is low after reset. Software can disable the Auto-Negotiation function by writing to bit MR0.12.

The contents of register MR4 are sent to the 78Q2120's link partner during Auto-Negotiation, coded in fast link pulses. Bits MR4.8:5 reflect the state of the TECH[2:0] pins after reset. If TECH[2:0] = 111, then all 4 bits are high. After reset, software can change any of these bits from a 1 to a 0 but not from a 0 to a 1. Therefore, a technology permitted by setting the TECH pins can be disabled by software; however, a technology not permitted by the TECH pins cannot be enabled via software.

With Auto-Negotiation enabled, the 78Q2120 sends fast link pulses at power on, loss of link, or command to restart. At the same time, it looks for either 10BASE-T idle, 100BASE-TX idle, or fast link pulses from its link partner. If either idle pattern is detected, the TSC 78Q2120 configures itself in half-duplex mode at the appropriate speed. If it detects fast link pulses, it decodes and analyzes the link code transmitted by the link partner. When three identical link code words are received (ignoring acknowledge bit), the link code word is stored in register 5. Upon receiving three more identical link code words, with the acknowledge bit set, the TSC 78Q2120 configures itself to the highest priority technology common to the two link partners.

The technology priorities are, in descending order:

- 100BASE-TX, full-duplex
- 100BASE-TX, half-duplex
- 10BASE-T, full-duplex
- 10BASE-T, half-duplex

Once Auto-Negotiation is complete, register bits MR18.11:10 will reflect the actual speed and duplex that was chosen. If Auto-Negotiation fails to establish a link for any reason, it starts from the beginning and tries again. Writing a one to bit MR0.9, RANEG, will also cause Auto-Negotiation to restart.

6.3.6 MII Interface

The MII interface on the 78Q2120 provides independent transmit and receive paths for both 10 Mb/s and 100 Mb/s data rates as described in Clause 22 of the IEEE-802.3 standard.

The transmit clock, TX_CLK, provides the timing reference for the transfer of TX_EN, TXD[3:0], and TX_ER signals from the MAC to the 78Q2120. TXD[3:0] is captured on the rising edge of TX_CLK when TX_EN is asserted. TX_ER is also captured on the rising edge of TX_CLK and is asserted by the MAC to request that an error code group be transmitted. The assertion of TX_ER has no effect when the 78Q2120 is operating in 10BASE-T mode.

The receive clock, RX_CLK, provides the timing reference to transfer RX_DV, RXD[3:0], and RX_ER signals from the 78Q2120 to the MAC. RX_DV transitions synchronously with respect to RX_CLK and is asserted when the 78Q2120 presents valid data on RXD[3:0]. RX_ER is asserted when a code group violation has been detected in the current receive packet and is also synchronous to RX_CLK.

The station management interface consists of circuitry that implements the serial protocol as described in Clause 22.2.4.4 of IEEE-802.3. A 16-bit shift register receives serial data applied to the MDIO pin at the rising edge of the MDC clock signal. Once the preamble is received, the station management control logic looks for the start-of-frame sequence and a read or write op-code, followed by the PHYAD and REGAD fields. For a read operation, the MDIO port becomes

enabled as an output and the register data is loaded into a shift register for transmission. The 78Q2120 can work with a 1-bit preamble rather than the 32 bits proscribed by IEEE-802.3. This allows for faster programming of the registers. If a register does not exist at an address indicated by the REGAD field or if the PHYAD field does not match the 78Q2120 PHYAD indicated by the PHYAD pins, a read of the MDIO port will return all ones. For a write operation, the data is shifted in and loaded into the appropriate register after the sixteenth data bit has been received. Writes to registers not supported by the 78Q2120 are ignored.

When the PHYAD field is all zeros, the Station Management Entity (STA) is requesting a broadcast data transaction. All PHYs sharing the same management interface must respond to this broadcast request. All 78Q2120 registers that are addressable via the REGAD field will respond to the broadcast data transaction except for the vendor-Specific-registers (MR16, MR17, and MR18).

6.3.7 LED Indicators

There are seven LED pins that can be used to indicate various states of operation for the 78Q2120. They are valid link (LEDL), transmitting (LEDTX), receiving (LEDRX), collision detected (LEDCOL), data rate (LEDBTX and LEDBT), and full-duplex mode of operation (LEDFDX).

6.3.8 General Purpose I/O Interface

The 78Q2120 has a 2-pin, bidirectional, general-purpose interface that can be used for external control or to monitor external signals. The direction of these pins and the data that is either written to or read from these pins is configured via bits MR16.9:6 as detailed in the vendor-specific-register description of MR16.

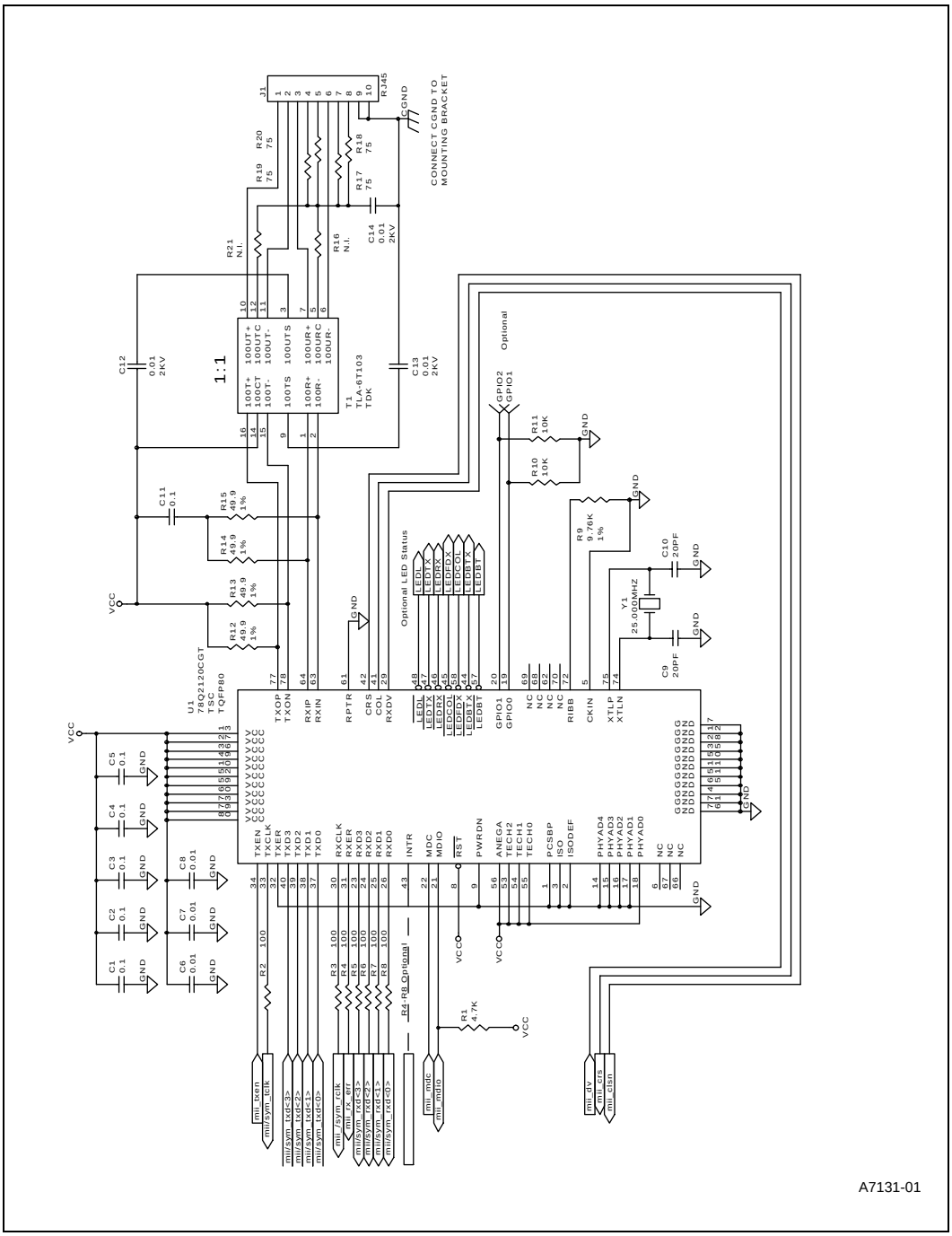
6.3.9 Interrupt Pin

The 78Q2120 has an interrupt pin (INTR) that is asserted whenever any of the eight interrupt bits of MR17.7:0 are set. These interrupt bits can be disabled via MR17.15:8 interrupt enable bits. The active level of the INTR pin is controlled by the interrupt level bit, MR16.14. When the INTR pin is not asserted, the pin is held in a high-impedance state.

6.4 78Q2120 Schematic

Figure 32 details the 78Q2120 schematic layout.

Figure 32. 78Q2120 Schematic Diagram



6.4.1 78Q2120 Parts List

Table 25 contains the 78Q2120 parts list.

Table 25. 78Q2120 Parts List

Qty	Reference Number	Description	Part Number	Package	Manufacturer
1	U1	IC, 10/100BASE-TX Transceiver	78Q2120CGT	TQFP80	TSC
1	T1	XFRM, 10BASE-T/100BASE-TX	TLA-6T103	SOW16	TDK
1	Y1	Crystal, 25.000 MHz	ECCM1-25.000MHZ	ECCM1	Ecliptek
4	R17, R18, R19, R20	Resistor, 75, 5%	—	CC0603	—
7	R2, R3, R4, R5, R6, R7, R8	Resistor, 100, 5%	—	CC0603	—
1	R1	Resistor, 4.7K, 5%	—	CC0603	—
2	R10, R11	Resistor, 10K, 5%	—	CC0603	—
4	R12, R13, R14, R15	Resistor, 49.9, 1%	—	CC0603	—
1	R9	Resistor, 9.76K, 1%	—	CC0603	—
2	C9, C10	Capacitor, Ceramic, 20 picofarad	—	CC0603	—
3	C6, C7, C8	Capacitor, Ceramic, 0.01 microfarad	—	CC0603	—
6	C1, C2, C3, C4, C5, C11	Capacitor, Ceramic, 0.1 microfarad	C2012-Y5D-1H-104Z	CC0805	TDK
3	C12, C13, C14	Capacitor, Ceramic, 0.01microfarad, 2 kV	—	CC01812	—

6.5 10/100 Mb/s Transformer Selection

The line interface for the 78Q2120 requires a pair of 1:1 isolation transformers. Integrated common-mode chokes are recommended for satisfying FCC radiated EMI requirements. Additional filtering is not required with the 78Q2120 due to internal waveform shaping circuitry. The line transformer characteristics are outlined in Table 26.

Table 26. Line Transformer Characteristics

Name	Value	Condition
Turns Ratio	1 CT: 1 CT	—
Open-Circuit Inductance	350 µH (min)[a]	@ 10 mV, 10 KHz
Leakage Inductance	0.40 µH (max)	@ 1 M hz (min)
Inter-Winding Capacitance	12 pF (max)	—
DC Resistance	0.9 ohm (max)	—
Insertion Loss	1.1 dB (typ)	0–100 Mhz
HIPOT	1500 Vrms	—

a. The receive line transformer's open-circuit inductance can be as low as 100 mH for the 78Q2120. The 78Q2120 incorporates baseline wander correction circuitry, which allows the receiver to track the incoming data signal when there is excessive transformer droop.

TSC has performed line testing of the transformers in Table 27 and found their performance acceptable with the 78Q2120. All transformers listed either meet or exceed IEEE's 802.3 Bit Error Rate requirements of 10^{-8}.

Table 27. Acceptable Transformers

Manufacturer	Part Number
TDK	TLA-6T103
Bel Fuse	S558-5999-46
Halo	TG22-3506ND
Pulse	PPE-68515
Valor	ST6118
YCL	20PMT04
The following transformers are low-profile packages (0.100 inch/2.5 mm or less)	
TDK	TLA-6T203
Halo	HTG110-S050
PCA	EPF8023G

6.6 78Q2120 Layout Considerations

The following recommendations enhance the 78Q2120's performance while minimizing EMC emissions:

- Make the transformer-to-transceiver signal traces into effective 50 Ω transmission lines.
- Place the termination network components near the input data pins of the transceiver or transformer.
- Make all differential signal pairs short and of the same length.
- Decouple the transceiver thoroughly with 0.01 µf and 0.1 µf capacitors.
- Locate decoupling capacitors as close as possible to the respective transceiver Vcc and Gnd pins.
- All decoupling capacitor and transceiver Vcc and Gnd connections should tie immediately to a Vcc or Gnd-plane via with minimum trace inductance.
- Total decoupling capacitance should be greater than the load capacitance that the digital output drivers must drive.
- Use low-inductance, ceramic-surface mount decoupling capacitors.
- Use a multilayer PCB with the inner layers dedicated to GND and Vcc.
- A single Vcc and Gnd plane is recommended for optimum performance. The lowest possible series impedance is required among the analog Vcc, digital Vcc, and Gnd pins, respectively of the transceiver.
- The outer layers of a 4-layer PCB are to be used for signal routing.
- Place the highest speed signals on the layer adjacent to the Gnd plane.
- Physically separate the analog signals from the digital signals by placing them on opposite layers or routing them away from each other.
- Additional component and solder side ground layers may be added for maximum EMC containment.
- The Gnd plane should extend to the transceiver side of the transformer.
- The chassis ground plane extends from the backplate and RJ45 to the line side termination components only. Do not allow the chassis ground plane to cross over the transceiver Gnd plane. Minimum separation must accommodate over 1.5 kV.
- Provide onboard termination of the unused signal pairs in the CAT-5 cable.
- Use a shielded RJ45 connector with its case stakes soldered to the chassis ground.
- Locate the transformer adjacent to the RJ45 to minimize the shunt capacitance to the line.
- Minimize RF current fringing by making the Vcc plane 0.10 inch smaller than the Gnd plane. If multiple transceivers are used, provide partitions in the Vcc and Gnd planes between the analog sections. Maintain the partition from the transformer up to the transceiver's analog interface. Do not cross these partitions with signal traces; in particular, any digital signals from adjacent transceivers.
- Add series resistors on all transceiver MII outputs to minimize digital output driver peak currents.
- Minimize the use of vias when routing the analog signal traces.
- Locate Ribb as close as possible to the transceiver's pin (and preferable on the same side).

- Isolate the crystal and its capacitors from the analog signals with a guard ring.

6.7 78Q2120 Summary

A highly efficient network interface has been presented utilizing TDK Semiconductor's 78Q2120 and the 21145. Use of the 78Q2120 and 21145 produces a 10/100 Mb/s Fast Ethernet interface with the following attributes:

- Simplicity of design
- Single 3.3 V interface
- Minimal power consumption
- Minimal PCB footprint

7.0 ML6698 100 BASE-TX PHY

This section describes the interface between the 21145 media access controller (MAC) and the Micro Linear ML6698 100 BASE-TX physical layer (PHY) for the designing of a 10/100 Mb/s network interface card (NIC).

7.1 ML6698 Overview

The PHY connects the MAC to the physical network via the 5-bit symbol interface. The ML6698 PHY integrates the 100BASE-TX transceiver and the receive and transmit PLLs. The ML6698 contains a 10BASE-T transmit buffer for a common external magnetic 10/100 Mb/s solution. These features permit the designer to use the 10BASE-T and Auto-Negotiation functions of the 21145 with the ML6698 to provide a single-jack connection to the network.

Information on Micro Linear products is available at the following website:

http://www.microlinear.com

The 21145 provides the following features:

- PCI interface
- 10/100 Mb/s MAC functions
- PCS layer coding and scrambling
- 5-bit symbol transmit and receive interface
- Unfiltered 10BASE-T transceiver
- Auto-Negotiation state machine

The ML6698 provides the following features:

- 5-bit (or symbol) interface
- 125 MHz receive clock recovery/generation
- MLT-3 encoder/decoder
- Adaptive equalization
- Baseline wander correction

An analog buffer, with a gain of 10, is used to pass on the 10BASE-T transmit signals. Switching between 10 Mb/s and 100 Mb/s Tx drivers is done internally so that the same output pins can be used with a common external magnetic module.

The interface between the 21145 and the ML6698 is a mixture of digital and analog signals. The 21145's 5-bit interface connects to the ML6698's 5-bit interface for 100-BASE-TX operation. The ML6698 100BASE-TX functions are accessible through the 5-bit interface. The following signals comprise the 5-bit interface:

- TXCLK—transmit clock input to provide a 25 MHz reference clock source. It should be the same clock connected to the MAC's TXCLK.
- TXD0 through TXD4—transmit data bits 0 through 4.
- RXCLK—receive clock output to the MAC.
- RXD0 through RXD4—receive data bits 0 through 4.
- SDO—signal detection valid output.

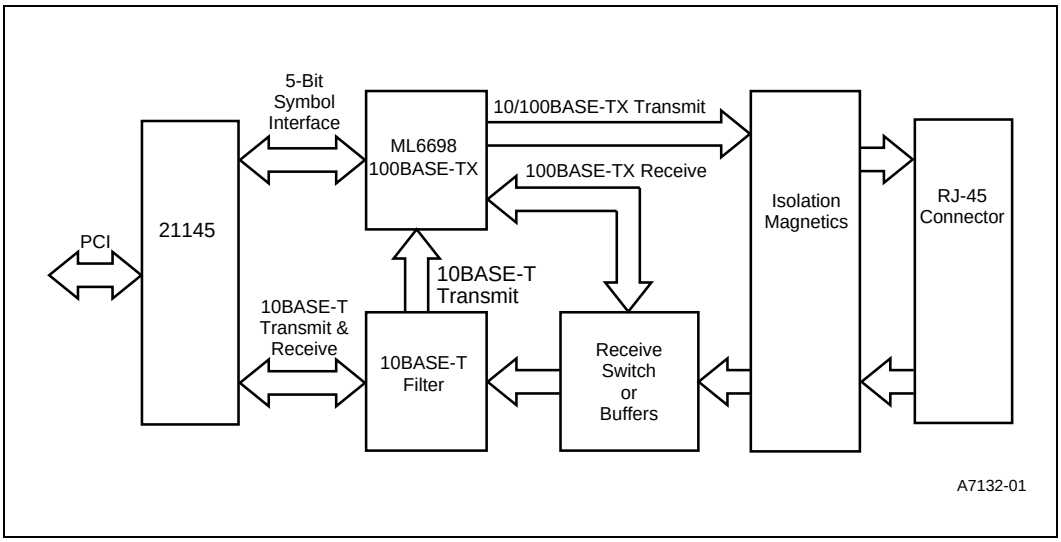
The 10BASE-T transmit signal from the 21145 should be filtered and attenuated before it is transmitted by the ML6698 during 10BASE-T operation. The 10BASE-T receive signals are routed to the 21145 10BASE-T receive inputs through an external analog switch and filter.

7.2 Block Diagram

Figure 33 shows a block diagram of the adapter card design using the ML6698. It includes the following components and capabilities:

- 21145
- ML6698
- 10BASE-T filter-transformer module and attenuator resistive network
- Receive switch or receive buffers
- A 10/100 Mb/s magnetics module consisting of transformers and series common-mode chokes to enable connection to either the 100BASE-TX or 10BASE-T network.

Figure 33. PCI Adapter Block Diagram: Signal Flow



7.3 Transmit and Receive Operation

The following sections refer to Figure 34 through Figure 38. The 10/100 mode select is controlled by the 21145 SEL10_L signal.

7.3.1 100BASE-TX Transmit Operation

In 100BASE-TX operation, the 5-bit signals from the 21145 connect to the corresponding pins of the ML6698. All access to the 100BASE-TX functions are through the 5-bit interface. No termination of the 5-bit interface is required. The transmit data is serialized, retimed, and then transmitted onto the twisted-pair cable.

A 25 MHz reference clock signal is fed to the ML6698's TXCLK and the 21145's MII_TCLK. The current drive outputs (pins 39 and 40) are open collector devices that pull current through the transformer while transmitting.

The single-ended signal level should be 2 V peak-to-peak, before it is stepped down 2:1 by an isolation transformer. Because the output is stepped down 2:1, the source impedance decreases by a factor of 4, therefore, pull-up resistors R95 and R96 are 200 Ω (when the output is designed for a 1:1 isolation transformer, R95 and R96 usually are 50 Ω). The RTSET resistor, R97, sets the transmit amplitude by providing a precise constant bias current.

7.3.2 100BASE-TX Receive Operation

The receive path is split into two paths at the two receive windings. One winding is routed to the 10BASE-T receive filter via either the mux or buffers, and the other winding is routed to the ML6698 receive inputs. When the Pericom mux is used, each path is terminated with 200 Ω. Termination resistors R94 and R93 are 100 ohms each for the 100BASE-TX receive path. The effective equivalent termination resistor is 100 ohms because two 100 Ω resistors (R22, R33) will be in parallel with R94, R93 when the SEL pin of the U11 mux is in 100 Mb/s mode.

The RGMSET resistor, R98, is used to set the equalization threshold for the 100BASE-TX receive path. The design value for R98 is 9.53 KΩ. The CMREF pin generates the common mode reference voltage (Vcc–1.26 V) to properly bias the receive inputs for operation. When buffers are used (see Section 7.3.4, Options for 10BASE-T Receive Operation, option 2), R93 and R94 are 50 Ω.

7.3.3 10BASE-T Transmit Operation

In 10BASE-T transmit operation, the transmit path consists of the following components:

- Pre-emphasis resistors
- Voltage swing compensator
- Transmit filter
- Resistor attenuator
- Common mode bias generator

The 74ACT244 voltage swing compensator is used because the U9 transformer ratio is 1:1, and the 21145 operates at 3.3 V. The 74ACT244 raises the output levels to 5 V in order to be compatible with the ML6698 PHY. Since the 10BASE-T output of the 21145 is unfiltered, the transmit signals must pass through a transmit filter prior to being amplified by the ML6698 analog buffer. The single-ended 10BASE-T input to the ML6698 must have a swing of 500 mV peak-to-peak (via the attenuating resistor network with a common mode bias of Vcc/2). With this small swing of input voltages, the 74ACT244 can be omitted (replace R8, R9, R11, and R17 with 0 Ω) by changing the values of R87 and R89 to 22 Ω, thus reducing the component count and cost.

The ML6698 amplifies the transmit signal by a factor of 10, and then with isolation transformers, steps it down by a factor of two. The resultant output is an IEEE 802.3 10BASE-T standard complaint signal of 2.5 V peak-to-peak, single ended or 5 V peak-to-peak differential output from the RJ45 connector.

7.3.4 Options for 10BASE-T Receive Operation

The following describes two options for receive operation

1. Using an analog multiplexer—In 10BASE-T receive operation, the receive path requires a receive filter. However, the 10BASE-T filter causes an impedance mismatch for 100BASE-TX receive signals, so it must be switched out when 100BASE-TX operation is selected. This is accomplished using an analog mux such as the Pericom P15L200 LAN switch, which is controlled by the SEL10_L signal from the 21145 MAC.
    a. The proper 100BASE-TX termination of the 10BASE-T filter and termination combination is automatically switched by the 21145 when Auto-Negotiation is complete or when the protocol speed is forced. Receive impedance is balanced by two 100 Ω resistors, R19 and R20, in parallel with R93 and R94.
2. Using buffers—The ML65L541 is a very high-speed buffer that uses a unique analog unity-gain buffer implementation. The ML65L541 has high input impedance in parallel with R93 and R94 to provide a common 100 Ω termination. The termination is made of R93=R94=50 ohms each. Since the buffers have 75 ohms in series internally, a pair of 1 KΩ (R28, R29) pull-up resistors are placed at the outputs of the buffers. The outputs of the 10BASE-T Rx filter are terminated with R19=R20=50 ohms each, for a total of 100 Ω.

7.3.5 Wake-Up-LAN-Option Operation (Demonstration Only)

Revision B of the 21145 implements the wake-up-LAN function. This feature can be enabled if pin 2 of jumper JP1 is connected to pin 3. The 21145's gep-2 signal activates an LED to indicate if a wake-up-LAN packet is received. The function is disabled if pin 2 is connected to pin 1. When the Revision A of the 21145 is used, pin 2 of Jumper JP1 must be connected to pin 1.

7.3.6 Other Considerations

Noise coupled at the TPINP/TPINN inputs of the ML6698 can be reduced by installing a 10 pF capacitor across the pins. Return loss can also be improved by inserting 130 nH (rated at 50 MHz) inductors, thereby connecting TPOUTP and TPOUTN to the magnetics (T2, pins 1 and 3).

Figure 34. ML6698 and 21145 Schematic: Part 1

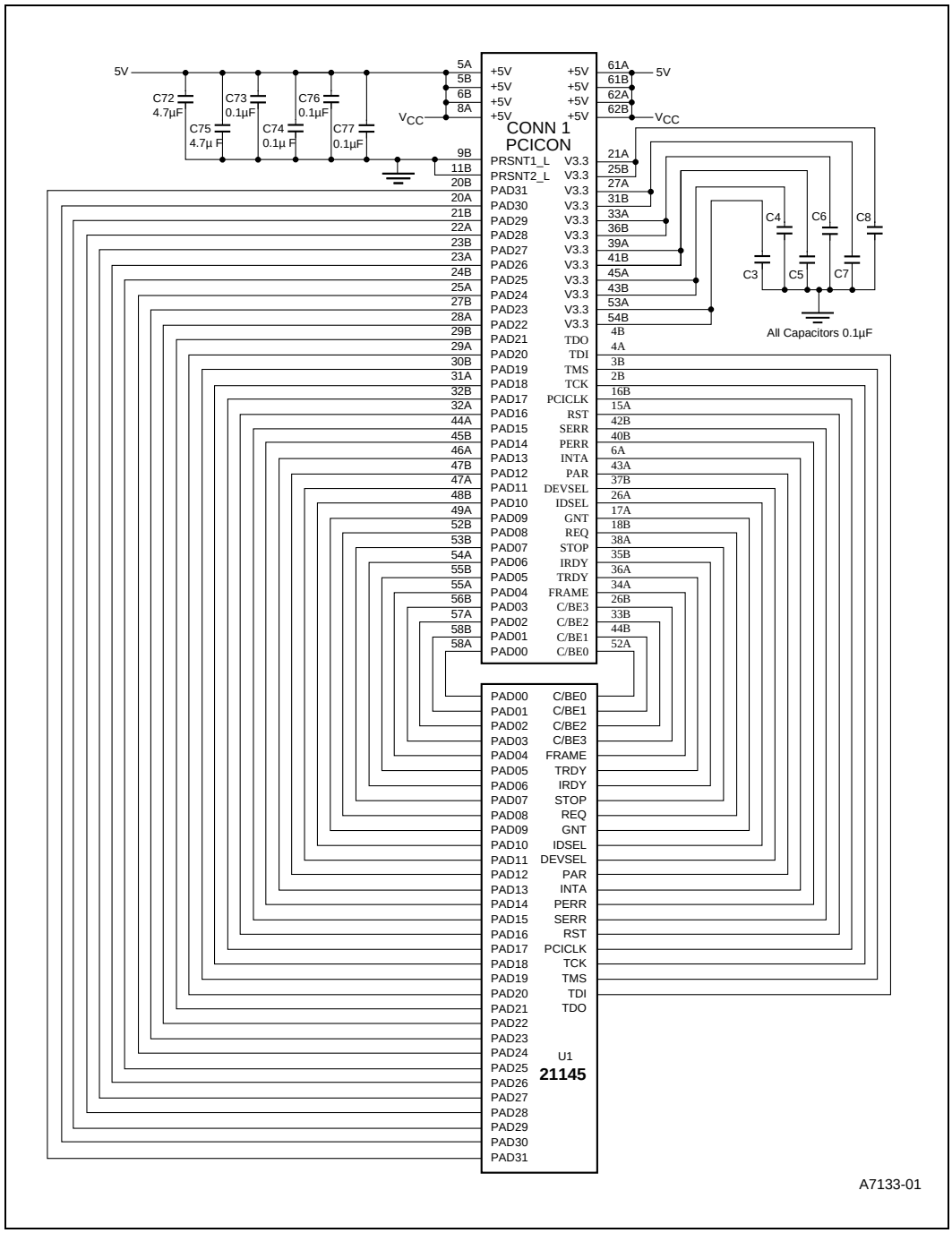


Figure 35. ML6698 and 21145 Schematic: Part 2

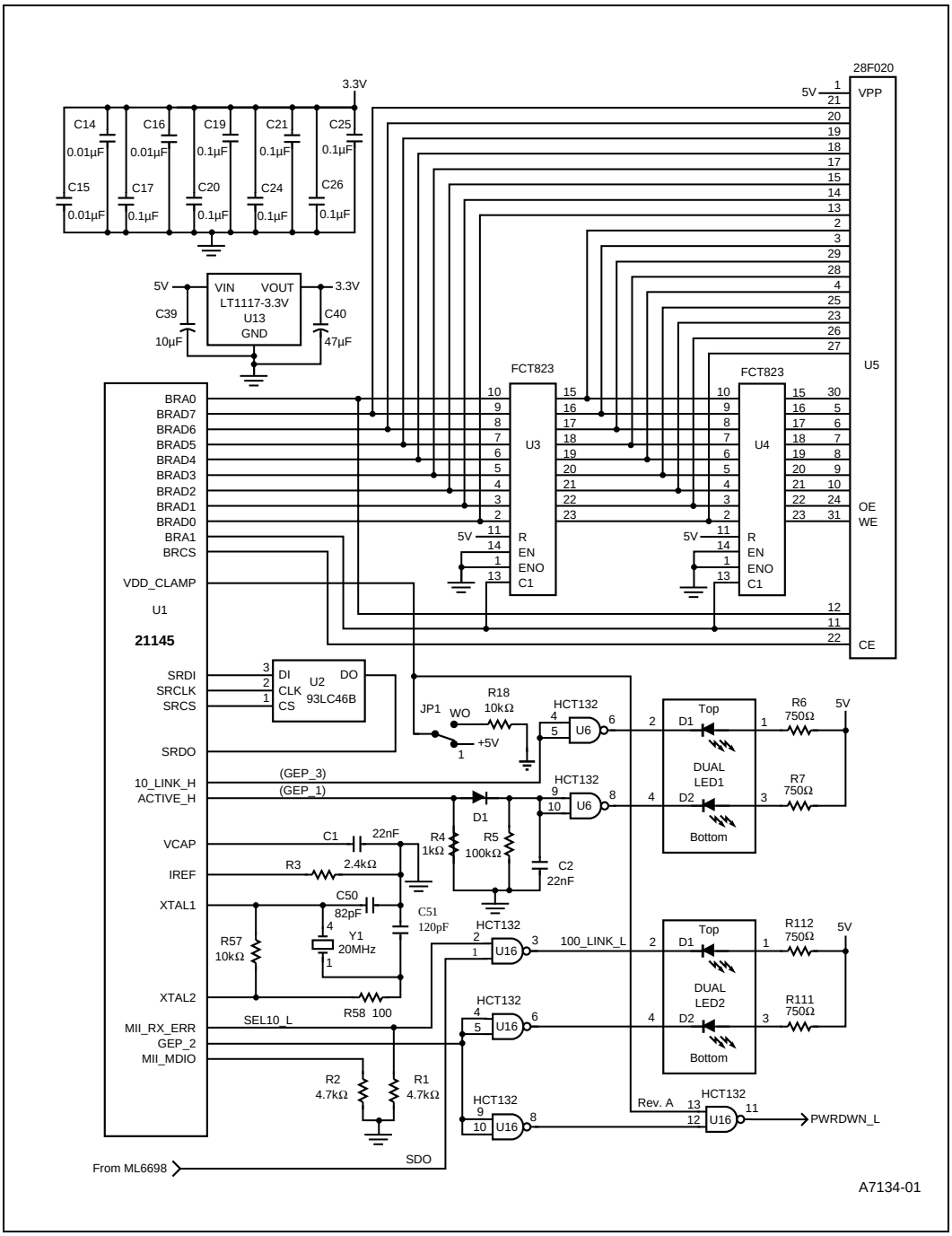


Figure 36. ML6698 and 21145 Schematic: Part 3

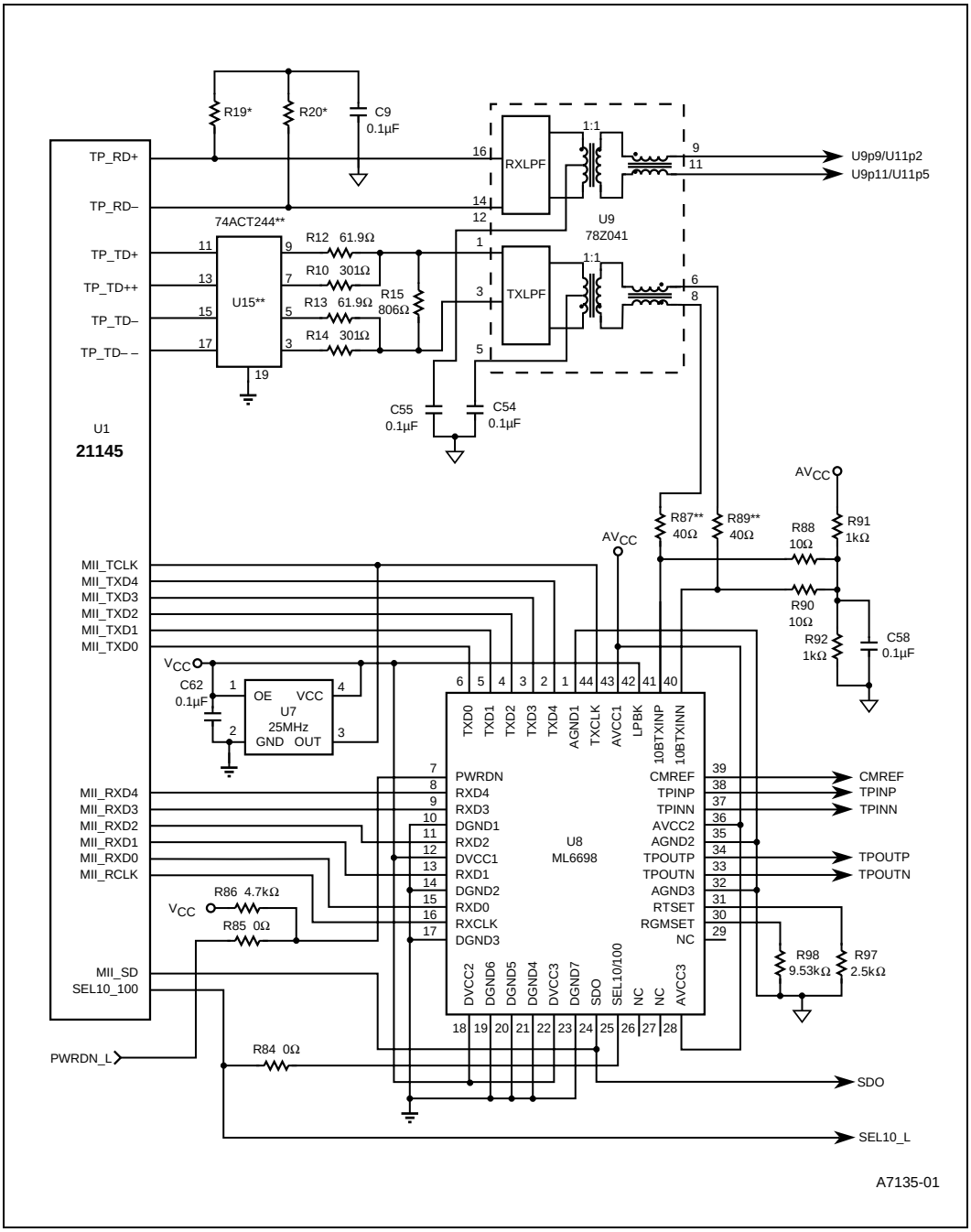


Figure 37. ML6698 and 21145 Schematic: (MUX)

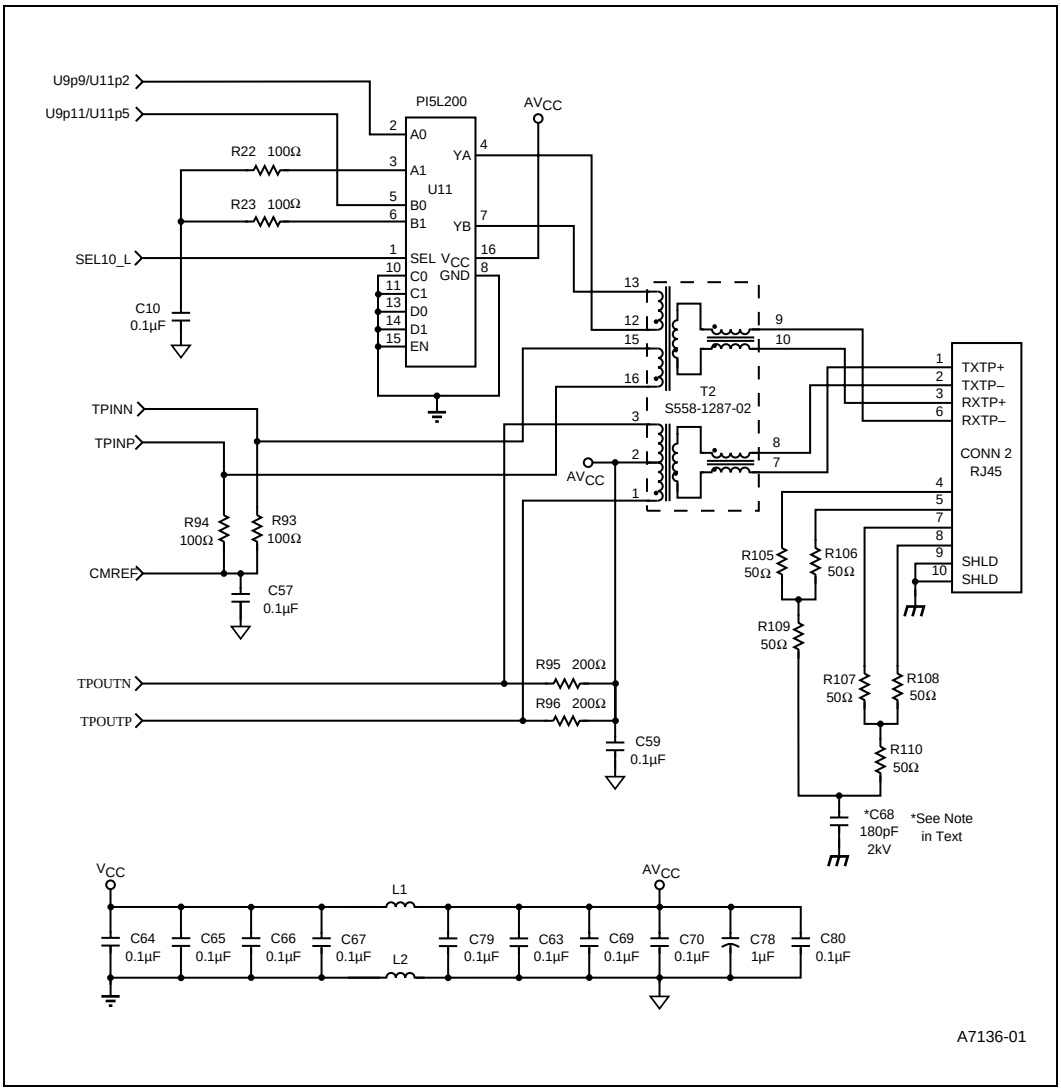


Figure 38. ML6698 and 21145 Schematic: (Buffer)

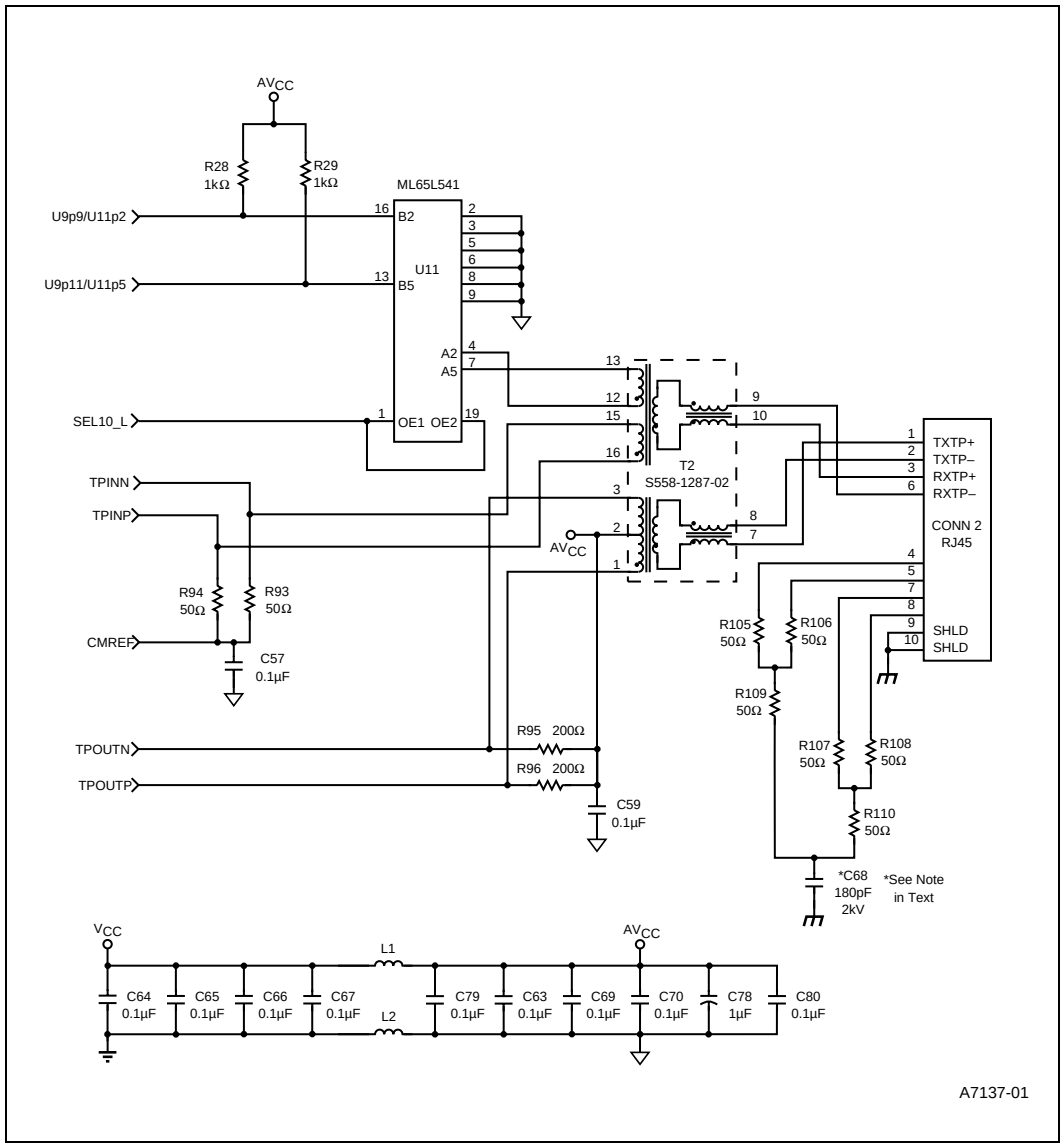


Table 28. 21145 and ML6698 Board Parts List (Sheet 1 of 3)

Quantity	Designator	Description	Manufacturer	Part Number
3	R1, R2, R86	4.75 kilohm, 0.1 W, 1%, surface mount	ASJ PTE Ltd. Dale Roederstein	CR21 4.75K 1% CRCW-0805-4751-F D124K75FCS
1	R3	2.43 kilohm, 0.1 W, 1%, surface mount	ASJ PTE Ltd. Dale Roederstein	CR21 2.43K 1% CRCW-0805-2431-F D122K43FCS
3	R4, R91, R92	1.00 kilohm, 0.1 W, 1%, surface mount	ASJ PTE Ltd. AVX/Kyocera Dale	CR21 1.00K 1% CR21-1001F CRCW-0805-1001-F
1	R5	100 kilohm, 0.1 W, 1%, surface mount	ASJ PTE Ltd. AVX/Kyocera Dale	CR21 100K 1% CR21-1003F CRCW-0805-1003-F
4	R6, R7, R111, R112	750 ohm, 0.1 W, 1%, surface mount	ASJ PTE Ltd. Dale Roederstein	CR21 750 1% CRCW-0805-7500-F D12750RFCS
2	R10, R14	301 ohm, 0.1 W, 1%, surface mount	ASJ PTE Ltd. Dale Roederstein	CR21 301 1% CRCW-0805-3010-F D12301RFCS
2	R12, R13	61.9 ohm, 0.1 W, 1%, surface mount	ASJ PTE Ltd. AVX/Kyocera Dale	CR21 61.9 1% CR21-61R9F CRCW-0805-61R9-F
1	R15	806 ohm, 0.1 W, 1%, surface mount	ASJ PTE Ltd. Dale Roederstein	CR21 806 1% CRCW-0805-8060-F D12806RFCS
2	R95, R96	200 ohm, 0.1 W, 1%, surface mount	ASJ PTE Ltd. Dale Roederstein	CR21 200 1% CRCW-0805-2000-F D12200RFCS
1	R57	10 kilohm, 0.1W, 1%, surface mount	ASJ PTE Ltd. AVX/Kyocera Dale	CR21 10.0K 1% CR21-1002F CRCW-0805-1002-F
7	R58, R19, R20, R22, R23, R93, R94	100 ohm, 0.1 W, 1%, surface mount (For buffer option: R19, R20, R93, R94 will be 50 ohm, 0.1 W, 1%)	ASJ PTE Ltd. AVX/Kyocera Dale	CR21 100 1% CR21-1000F CRCW-0805-1000-F
1	R85	0 Ω jumper	ASJ PTE Ltd. AVX/Kyocera Dale	CR21 ZERO OHMS CJ21-000 CRCW-0805-9-0000
2	R87, R89	40.2 ohm, 0.1 W, 1%, surface mount	Dale Roederstein Yaego	CRCW-0805-40R2-F D12402R2FCS RC05 1/8W 1% 40E2
2	R88, R90	10.0 ohm, 0.1 W, 1%, surface mount	ASJ PTE Ltd. Dale Roederstein	CR21 10.0 1% CRCW-0805-10R0-F D12010RFCS

Table 28. 21145 and ML6698 Board Parts List (Sheet 2 of 3)

Quantity	Designator	Description	Manufacturer	Part Number
2	R28, R29	150 ohm, 0.1 W, 1%, surface mount	ASJ PTE Ltd. AVX/Kyocera Dale	CR21 150 1% CR21-1500F CRCW-0805-1500-F
1	R97	2.49 kilohm, 0.1 W, 1%, surface mount	ASJ PTE Ltd. AVX/Kyocera Dale	CR21 2.49K 1% CR21-2491F CRCW-0805-2491-F
1	R98	9.53 kilohm, 0.1 W, 1%, surface mount	ASJ PTE Ltd. AVX/Kyocera Dale	CR21 9.53K 1% CR21-9531F CRCW-0805-9531-F
6	R105–R110	50 ohm, 0.1 W, 1%, surface mount	ASJ PTE Ltd. Dale	CR21 50.0 1% CRCW-0805-50R0-F
2	C1, C2	0.022 µF, 50 V, 20%, ceramic chip	AVX Murata	08055E223MATMA GRM40Z5U223M050AD
38	C3– C10, C17, C19–C21, C24–C26, C52–C67, C69–C70, C73, C74, C76, C77, C79, C80	0.1 µF, 50 V, 20%, ceramic chip	AVX AVX Vitramon	08055E104MAT2A 08055E104MAT00J 7739U104MXAMC
3	C14–C16	0.01 µF, 50 V, 20%, ceramic chip	AVX AVX Murata	08055E103MATMA 08055C103MAT00J GRM40Z5U103M050AD
2	C31, C39	10 µF, 16 V, 10%, tantalum chip	AVX KEMET Sprague	TAJC106K016RNJ T491C106K016AS 293D106X9016C2T
2	C72, C75	4.7 µF, 6.3 V, 10%, tantalum "A"	AVX Sprague	TAJ475K6R3RNJ 293D475X96R3A2T
1	C40	4.7 µF, 10 V, 10%, tantalum "D"	AVX Sprague	TAJD476K010RNJ 293D476X9010D2T
1	C50	82 pF, 100 V, 5%, ceramic chip	AVX Murata Vitramon	08051A820JAT2A GRO40COG820J100AD 0805A820JXBMT
1	C51	120 pF, 100 V, 5%, ceramic chip	AVX Murata Vitramon	08051A121JAT2A GRO40COG121J100AD 0805A121JXBMT
1	C68[a]	180 pF, 2000 V, 10%, ceramic chip	AVX	2225HA681KAT1A
1	U1	LAN Controller	Intel	21145
1	U2	Serial EEPROM, 1024 bits	Microchip National Semiconductor	93LC46B/SN 93C46M8
2	U3, U4	Buffered 9-bit register	Integrated. Device	74FCT823BSO

Table 28. 21145 and ML6698 Board Parts List (Sheet 3 of 3)

Quantity	Designator	Description	Manufacturer	Part Number
1	U5	(Optional) 256Kx8 Flash, 120 ns	AMD	AM28F020-120PC
2	U6, U16	Quad Schmitt Trigger CMOS nand gate	Philips	74HCT132D
1	U7	25 MHz crystal oscillator, plastic	Epson Toyocom	SG-615P 25.000M C TCO-711JT 25.000M
1	U8	100BASE-TX symbol transceiver	Micro Linear	ML6698CQ
1	U9	10BASE-T magnetic	Fil-Mag	78Z041
1	U11	Wide bandwidth LAN switch (5 V)	Pericom	P15L200W
1	U13	Voltage regulator	Linear Tech	LT1117CST-3.3 or LT11173
1	U15	CMOS octal buffer	National Semiconductor Toshiba	74ACT244 74ACT244
1	D1	Diode, PIV=75, 4 ns	BKC Intl. National Semiconductor Philips	1N4148 1N4148.TR 1N4148
2	LED1, LED2	RTAN VTSTK 2MC 2 mA G/Y 3M, assembly	Dialight Lumex	553-0223 SSF-LXH240GYD-DEC
1	Y1	20.0000 MHz crystal	Seiko Ecliptek	MA-506 20.000M-AD ECSM-20.000M
1	(Ref. U5)	IC DIP socket, 0.1 x 0.6, tin, (optional)	Hon Hai Precision AMP Augut	PA01160-T 2-644018-5 332-AG19DC
1	CONN 2	Modular phone jack connector	AMP Berg Hon Hai Precision	555141-1 94909-088 JM51115-12-1
2	L1, L2	Ferrite bead	Steward Fair-Rite Mag Layers	28R0121-OSR 2743019447 SMB-403025
1	T2	10/100 Mb/s transformer module	Bel Fuse	S558-1287-01
1	—	PCB board	Micro Linear/Intel	
1	U11 (buffer option)	8-Bit high speed buffer (5 V)	Micro Linear	ML65L541

a. This capacitance is composed of four PCB layers. Value is measured, but not fully tested. See Figure 37.

7.4 Layout Considerations

It is important that the designer pay particular attention to the layout of the board. Both the board's analog performance and electromagnetic (EM) emissions are determined by the board layout.

The best printed circuit board (PCB) for the NIC is a multilayered PCB. A four-layer board with 2-ounce copper power planes minimizes switching transients by providing a lower impedance power source. Creating an ideal power source is the goal when laying out power planes. Therefore, it is preferable to combine (with the help of ferrite beads) both the 21145 and analog power supplies of the ML6698 into a common low-impedance supply. The use of split planes can be advantageous, but in a small form-factor design, this advantage is lost because the planes cannot be made large enough to be effective.

Liberal usage of capacitors on the 21145 power pins minimizes any noise that may be coupled into the power plane. Power-supply noise contributes to EM emissions in circuit layouts. EM emissions are reduced by many orders of magnitude when the 21145 switching intensive 5-bit interface is turned off. It is imperative that low ESR capacitors with multiple via connections to the power and ground planes be placed in close proximity to all power pins.

The power and ground planes should extend underneath both the ML6698 and the bypass capacitors. The power and ground planes should not extend underneath any network signal path (the twisted-pair transmit and receive lines located between the ML6698 and the RJ45 connector) because common-mode power-supply noise will be coupled to the network signals, causing them to act like radiating antennas. Therefore, the design goal is to provide low-impedance power and ground planes around the ML6698 power and ground pins, while removing all grounds from the network signal paths. The greater the distance between the power plane and the network signal paths, the lower the EM emissions. The 10BASE-T signal paths between the 21145 and the ML6698 should be routed away from the power and ground planes.

The emission frequencies of the ML6698 are usually in 25 MHz harmonics because the system clock operates at 25 MHz. Emission frequencies can be as high as 250 MHz. A stray capacitance of 5 pF has an impedance of 127 Ω at 250 MHz. This impedance determines how much current flows when the power noise couples to the network signal paths. The current, in turn, determines how much of the 250 MHz component is radiated. To reduce the radiated noise, minimize the stray capacitance.

Use the chassis of the instrument where the adapter is installed to allow coupled noise to flow to ground. The chassis is not a perfect ground, but, with proper instrument power supply design, the chassis can be used to redirect common-mode noise. The object is to surround the network signals on the RJ45 connector side of the isolation transformer with a chassis ground plane. The small coupling of the network signals to the chassis help attenuate the common-mode noise before leaving the chassis. This layout technique is called stripline. As with network signal paths, the farther the power and ground planes are away from the chassis, the lower the EM emissions.

7.5 ML6698 Summary

This section provided the designer with sufficient information to design an interface between the 21145 and the ML6698. A NIC adapter card can be designed using the built-in Auto-Negotiation and 10BASE-T functions of the 21145 and the 100BASE-TX functions of the ML6698. With proper power-supply layout, this circuit can pass CISPR "B" emission limits with a four-layer PCB. Figure 34 through Figure 38 provided a full schematic of such a NIC.

8.0 80220/80221 10/100BASE-TX PHY

This section describes the implementation details on interfacing the 21145 Ethernet controller and the SEEQ Technology 80220/80221 10/1000BASE-TX physical layer (PHY) device.

8.1 Overview

The 80220/80221 is a 10/100BASE-TX PHY that complies with IEEE 802.3 requirements. It is a single chip with an MII interface that can directly interface to the 21145 Ethernet controller. It can operate at either 10 Mb/s or 100 Mb/s and has a built-in Auto-Negotiation algorithm to interface to different physical layer devices. The 80220/80221 also has built-in base-line-wander correction circuitry that has been tested against several kinds of killer packets with varying dc shifts successfully over different cable lengths.

There are two different package options available:

- The 80220 is a 44-pin PLCC
- The 80221 is a 64-pin LQFP

The LQFP package has additional features and two additional LEDs not included in the PLCC.

All the LEDs in the device are user programmable to be asserted on several different events in many different ways.

Information on SEEQ products is available at the following website:

http://www.seeq.com

8.2 Interface to the 21145

The 80220 or 80221 interfaces easily with the 21145 MAC using the MII interface for operation at 10 Mb/s or 100 Mb/s. Use of the MII interface allows the simplest circuitry to be used and a single set of magnetics for both 10 Mb/s and 100 Mb/s operation.

Figure 39 shows the connection between the 21145 controller and the 80220/80221 physical layer device. The MII signal pins are mapped 1-to-1 between these two devices, including the MII interface pins (mdc, mdio), allowing full software support through the IEEE-specified register set (register 0 through register 5).

For compatibility, the TX_ER pin on the 80220/80221 should be grounded because this signal is not supported on the MII interface of the 21145. In addition to the standard MII signal connections, two optional signals, MDINT-, and RX_EN/JAM, are shown in the schematic diagram.

The MDINT- pin provides a low active interrupt output when certain indicator bits change in the status register. These status bits can be masked to assert the interrupt only under selected conditions. This is a powerful feature that allows efficient software to be written to monitor the physical layer without the need to continuously poll each port. The MDINT- pin also shares its function with the high-order address select bit (MDA4) of the 80220/80221 transceiver during power-on reset.

In most cases, where the PHY address is between 0 and 15, the MDINT- pin is internally pulled up to Vdd. This sets the MDA4 bit to "0" during power on reset, because the 80220 inverts the state of this pin for address determination.

In normal default operation, RX_EN/JAM should be externally tied to Vdd, which enables the receive MII interface. This must be done to enable data to be passed to the 21145. This pin can be used to tristate the receive MII pins if a shared bus architecture is used to connect to the MAC. For special applications, the 80220/80221 can be configured to send a JAM packet. This happens if RX_EN/JAM is low and if receive activity is detected. The 80220/80221 sets configuration register 2, bit 1 to a value of 1. The normal default state is no JAM transmission, with this bit automatically set to 0.

The 80220 (shown in Figure 39) has four LED Driver outputs for status information (the 80221 has six). These pins can be programmed under software control to display different status conditions on the pins. These pins also double as the PHY address select pins during power-on reset.

The default status assignment of these pins are:

PLED3-	Link at 100 Mb/s
PLED2-	Activity
PLED1-	Full-duplex
PLED0-	Link at 10 Mb/s

Because the 80220/80221 is fully compliant with the IEEE MII and register specifications, no software modifications are required to any drivers that use standard register functions as specified by the IEEE. Default conditions for power-on reset enable full Auto-Negotiation for operation at 10 or 100 Mb/s with full or half-duplex capability.

A hardware pin is also available on the 80221 (RPTR) which automatically configures the transceiver to 100 Mb half-duplex operation with no software intervention required.

For other operating configurations, the control register (0) can be written under software control, allowing for many flexible modes of operation. Refer to the 80220/80221 data sheet (available from the manufacturer) for details of the proprietary registers (above 5), which offer a large variety of features, including interrupt on status operation.

8.3 80220 PHY Board Schematic Diagram

Figure 39 shows a schematic diagram of an adapter card designed using the 80220 and 21145.

Figure 39. 80220 PHY Board Block Diagram

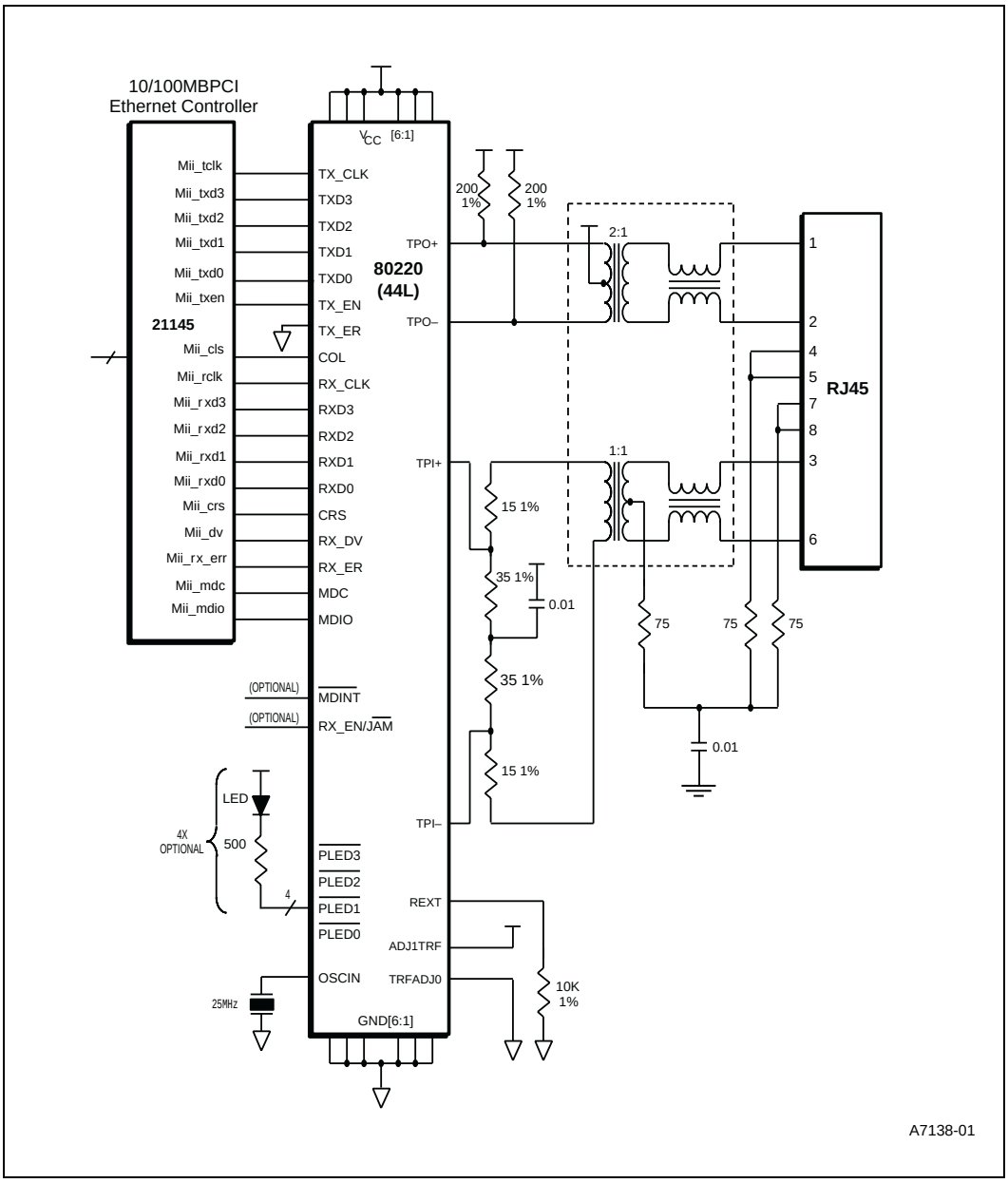


Table 29. 80220 PHY Board Component Listing

Quantity	Component	Description
2	Resistor	200 ohm, 1%
2	Resistor	15 ohm, 1%
2	Resistor	35 ohm, 1%
1	Resistor	10 kilohm, 1%
2	Resistor	75 ohm, 5%
1	Capacitor	0.001 to 0.01 μF at 2000 V
8	Capacitor	0.01 to 0.1 μF, bypass at > 10 V
1	Transformer	2:1 transmit CT primary, 1:1 receive CT line side. See Table 30 and Table 31.
1	Crystal/Oscillator	A 25 MHz crystal or oscillator module is required. Typical crystal part number is Ecliptek EC2F-25M. See Table 33.
Optional Components		
4	LEDs	
4	Limit Resistors	500 to 100 ohms

8.4 Design Considerations

The following subsections detail the various elements used to create an adapter board.

8.4.1 Choosing a Transformer

The transformer for the 80220/80221 requires a 2:1 winding ration on the transmit center tap on the primary side, tied to Vcc as shown in Figure 39. Table 30 details other transformer parameters.

Table 30. Transformer Parameters

Parameter	Specification	
	Transmit	**Receive**
Turns Ration	2:1 CT	1:1
Inductance (μH minimum)	350	350
Leakage Inductance	0.05–0.15	0.0–0.2
Capacitance (pF maximum)	15	15
DC Resistance (ohms maximum)	0.4	0.4

Table 31 lists some transformers and vendors that meet the above specifications.

Table 31. Transformer Vendors

Transformer Vendor	Part Number
Valor	ST6129
Nano Pulse	NPI 6254-30
PCA	EPF 8025G
Bel Fuse	558-5999-96 558-599-E3
Pulse Engineering	H1038/H1039
TDK	TLA6T107
YCL	PT 163042

8.4.2 Termination Requirements

The transmit output needs to be terminated with two external termination resistors in order to meet the output impedance and return loss requirements of IEEE 802.3. These two resistors should be connected from Vcc to each of the TPO+/TPO- outputs, and their values must be chosen to provide the correct termination impedance when looking back through the transformer from the twisted-pair cable, as shown in Figure 39.

The receive input needs to be terminated with the correct termination impedance to meet the input impedance and return loss requirements of IEEE 802.3. The values shown in Figure 39 are for a typical unshielded twisted-pair cable.

Table 32 shows the termination resistors to be used with different cable types.

Table 32. Termination Specifications

Cable Type	Cable Type Select Bit (16.7)	Resistor (Ohms, Tolerance 1%)
100 Ohms UTP, CAT5	UTP	R1=15 R2=35 R3=35 R4=15 R5=200 R6=200
150 Ohms, STP	STP	R1=22.5 R2=52.5 R3=52.5 R4=22.5 R5=300 R6=300

It is also recommended that a 0.01 µF capacitor be placed at the center of the ac ground for attenuating common-mode signals at the input. This capacitor is also shown in Figure 39. To meet the susceptibility requirements and to minimize common-mode noise, it may be necessary to add a common-mode choke on the receive input. All the transformers listed in Table 31 have a common-mode choke built in on both transmit and receive.

8.4.3 Meeting IEEE-Specified Output Amplitude Levels

The output current level is determined by the value of the external resistor tied between REXT and ground, called the bias resistor. The value of the output current is inversely proportional to the value of the bias resistor. The suggested value of this resistor is10 KΩ, 1%, which should meet the IEEE-specified levels for a typical application.

Because the TP output is a current source, capacitive and inductive loading can reduce the value of the output amplitude from the ideal. Therefore, if a board design has more loading than normal, it may be necessary to adjust the output levels by either reducing the bias resistor value or by using the transmit-level register bits. The register bits are described in detail in the 80220/80221 data sheet.

8.4.4 MII Interface

The MII interface on the 80220/80221 is designed to interface gluelessly to the 21145 Ethernet controller. No termination resistors are needed when the 80220/80221 is connected to the controller on the same PCB with no MII connectors.

The MII interface can be disabled by setting the MII disable bit in the MII serial port control register. When this bit is set to the default state, the TP outputs are also disabled and the transmission is inhibited.

The default value of this bit when the device powers up or after reset is dependent on the configured physical address. If the physical address is 0, the device powers up with the MII interface disabled, and can be enabled by writing a 0 to the MII_DIS bit in the control register. If the device is configured to any address other than zero, the MII interface is enabled on power-up.

8.4.5 Clock Requirements

The 80220/80221 requires a 25 MHz reference frequency for internal signal generation. This 25 MHz reference frequency can be generated by either connecting an external 25 MHz crystal between the **O**SCIN and GND or by applying an external 25 MHz clock to OSCIN.

If a crystal oscillator is used, it needs only a crystal; no other external capacitors or components are required. The crystal must have the characteristics shown in Table 33.

Table 33. Crystal Specifications

Parameter	Specification
Type	Parallel resonant
Frequency	25 MHz +/- 0.01%
Equivalent Series Resistance	15 Ω
Load Capacitance	18 pF, typical
Case Capacitance	7 pF, maximum
Power Dissipation	1 mW, maximum

8.5 Programming Considerations

The following subsections describe some 80220/80221 programming considerations. Complete details on 80220/80221 control register assignments are detailed in the 80220/80221 data sheet. The software commands shown here are based on the Evaluation Board Debug Software (EVBDEBUG.EXE).

8.5.1 Determination of the PHY Address

There are five address inputs called MDA[:4:0]* on the 80220. The MDA[:4:0]* inputs share the same pins as the MDINT* and the PLED[3:0]*outputs respectively. At power-up or reset, the PLED[3:0]* and MDINT* outputs are tristated for an interval called the power-on reset time. During this interval, the values on these pins are latched into the device, inverted, and used as the serial-port physical-device address.

If all five inputs (MDA[:4:0]*) are pulled up, then the device gets configured to function at the PHY address of 0000. When the 80220 is configured to be at an address of zero, then the device comes up with the MII disabled. This is to ensure that the PHY does not drive the MII bus when the bus is shared by multiple PHYs. For example:

MDA[4:0]	Physical address in the MDIO bit stream
11111	00000
11110	00001

8.5.2 Initialization

Once the PHY address is determined, the device will respond to reads and writes to that physical address. The software should reset the device before beginning to do any configuration reads and writes. The chip can be reset by writing a 1 to bit 15 of the control register at the 0 location. For example, the command:

WMI 1 0 8000

Will write the following:

WMI–Write to the MI

1–Physical address of 1

0–Control register at address location of 0

8000–Data

After a reset, the chip takes a minimum of 50 ms (IEEE specification is 500 ms) to complete the reset. It is important the make sure that the software does not attempt to configure the device through the serial port during this reset period. After a period of 10 µs from reset, the device can be polled to verify the completion of the reset cycle by monitoring the reset bit. The MII_DIS bit gets updated only at the end of the reset cycle, because its default value depends on the physical address of the device.

8.5.3 Configurations

The 80220 can be configured to either Auto-Negotiation with a remote device or forced to function in a particular mode. Bit 12 of the control register enables or disables Auto-Negotiation, and bit 13 sets the speed to either 10 Mb/s or 100 Mb/s. For further details, refer to the 80220/80221 data sheet.

8.6 Layout Guidelines

The following subsections contain details about PCB layout considerations.

8.6.1 Decoupling

There are six Vccs and six Gnds on the 80220/80221. All the Vccs should be tied together (as close to the device as possible) into a Vcc plane, and all the Gnds should be tied together (as close to the device as possible) into a Gnd plane. These steps are necessary in order to make sure that the Vccs do not vary in potential with respect to each other. All the Vccs should be kept within 50 mV of each other. The same rules apply to the Gnds. Each Vcc–Gnd pair should be decoupled separately. Table 34 lists the valid Vcc–Gnd pairs.

Table 34. Vcc-Gnd Pair

Vcc	Gnd
Vcc1 (pin 44)	Gnd1 (pin 41)
Vcc2 (pin 1)	Gnd2 (pin 4)
Vcc3 (pin 10)	Gnd3 (pin 9)
Vcc4 (pin 11)	Gnd3 (pin 9)
Vcc5 (pin 24)	Gnd5 (pin 25)
Vcc6 (pin 28)	Gnd4 (pin 36)
Vcc6 (pin 28)	Gnd6 (pin 27)

Any capacitor value from 0.1 µF to 0.01 µF can be chosen as a decoupling capacitor between each Vcc–Gnd pair. The value should be chosen based on the frequency of the noise expected from the Vcc plane. A safer approach would be to use two decoupling capacitors for each Vcc–Gnd pair: one 0.1 µF capacitor for low frequency noise and another 0.001 µF capacitor for high frequency noise from the power supply. The capacitor pair has to be placed as close to the device as possible, preferably within 0.5 inches.

The Vcc connection to the transmit center tap (shown in Figure 39) has to be well decoupled in order to minimize common-mode noise injection from the supply into the twisted-pair cable. It is recommended that 0.01 µF of decoupling capacitor be placed between the center tap **Vcc** to the ground plane. This decoupling capacitor should be physically placed as close as possible to the transformer.

The decoupling recommendations described previously should result in the following:

- The resultant ac noise voltage measured across each Vcc–Gnd pair should be less than 100 mV peak-to-peak.
- All Vccs should be within 50 mV peak-to-peak of each other.

8.6.2 Traces

The twisted-pair output and input pins are arranged so that their data paths do not cross each other in the layout, all the way to the RJ45 connector. The distance between the two signal lines of the differential pairs should be uniformly maintained to the RJ45 connector. The transformers qualified to work with the 80220 are designed with a pinout that can support such a streamlined layout.

The length of the traces going from the 21145 to the 80220/80221 should be kept to a minimum. Avoid running the traces from the LED pins under the differential pair traces. Because the traces going to the LED constantly switch, it might induce noise in the twisted pair lines.

It is important to maintain the impedance of the clock and signal traces uniformly from the source to the destination in the MII interface section. It is also important to keep the length of the trace to the OSCIN pin to a minimum to reduce parasitic capacitance.

8.6.3 Power Planes

It is important to separate the chassis ground from the digital ground (as shown in Figure 39) to prevent noise coupling into the digital ground. The unused pairs on the RJ45 connector should be tied into the chassis ground through 75 Ω resistors and a 0.01 µF capacitor (also shown in Figure 39). The metal shell of the connector should be tied to the chassis ground and not the digital ground. It is also a good practice to leave the area from the secondary of the transformer to the connector free of any copper. This is a safe way of ensuring that RF currents do not propagate to different parts of the board by radiative conductive means.

8.6.4 Clock Considerations

If a crystal is used as a clock source, it is important to place it as close to the device as possible. This will ensure that the length of the trace is kept to a minimum so that the parasitics on the clock input are greatly reduced.

8.7 80220/80221 Summary

This section provided the designer with sufficient information to design an interface between the 21145 and the 80220/80221 PHY. An Ethernet controller card can be designed using the built-in Auto-Negotiation and 10BASE-T functions of the 21145 and the 100BASE-TX functions of the 80220/80221.

9.0 LXT970 Fast Ethernet Transceiver

This section describes how to implement 10/100 Mb/s network connections using the 21145 LAN controller and the Level One Communications LXT970 Fast Ethernet transceiver.

9.1 LXT970 Overview

The LXT970 is a full -integrated, full-featured Ethernet PHY transceiver that supports both copper and fiber media. It supports 100BASE-TX and 10BASE-T copper applications from a single twisted-pair interface. It also provides a pseudo-ECL interface that can be connected to an external fiber transceiver to support 100BASE-FX applications. It provides a standard MII interface, which can operate in either normal (4-bit) or symbol (5-bit) mode. For copper media, the LXT970 fully supports Auto-Negotiation with parallel detection. The LXT970 can be configured through the MII interface or through its hardware configuration pins.

Features of the LXT970 include:

- Full- or half-duplex operation for any application (100BASE-TX, 100BASE-FX, or 10BASE-T)
- A robust receiver, which includes baseline wander correction for long-line-length performance
- Integrated transmit and receive filtering, which reduces the cost and complexity of the output stage
- Integrated LED drivers
- Integrated supply monitor and line disconnect during low-supply fault

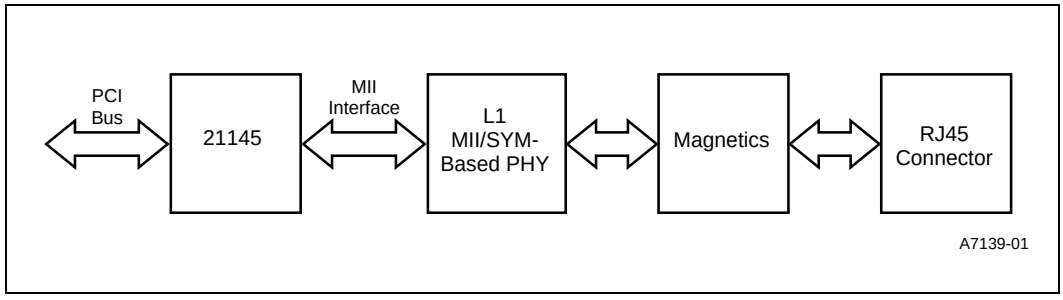
Information on Level One Communications products is available at the following website:

http://www.level1.com

9.2 Block Diagram

Figure 40 is a block diagram of a 10BASE-T/100BASE-TX network connection. The LXT970 directly interfaces with the MII/SYM port of the 21145 LAN controller through an MII interface. The MII on the LXT970 may be used for either MII or SYM network connection options.

Figure 40. Network Connection



9.3 MII Interface

The LXT970 interfaces to the 21145 controller through a fully compliant IEEE 802.3 MII interface for all applications: 10BASE-T, 100BASE-TX, and 100BASE-FX. The MII interface supports both 5 V and 3.3 V operation, and operates at either 2.5 MHz or 25 MHz, depending on the network link speed.

9.3.1 MII Data Interface

There are ten signals used to pass received data through the MII to the 21145 controller (RXD<4:0>, RX_CLK, RX_ER, RX_DV, CRS, and COL). There are eight signals used to transmit data from the 21145 controller to the network (TXD<4:0>, TXD_CLK, TXD_ER, and TXD_EN).

9.3.1.1 4-Bit Nibble Mode and 5-Bit Symbol Mode

The MII data interface on the LXT970 supports either Nibble Mode or Symbol Mode. In Nibble Mode, 4-bit nibbles are passed across the MII data interface, with RXD4 and TXD4 ignored. In Symbol Mode 5-bit symbols are passed across the MII data interface, with RXD4 and TXD4 active.

9.3.2 MII Connection

The LXT970 provides a single MII interface that connects to either the MII or SYM port of the 21145 controller. The connections and signals are shown in Table 35 and Table 36.

Table 35. 21145 MII Connection

21145 Signal	144-Pin Package Pin Number	176-Pin Package Pin Number	LXT970 Signal	LXT970 Pin Number
mii_clsn	118	147	COL	64
mii_crs	117	146	CRS	1
mii_dv	129	161	RX_DV	51
mii_mdc	134	166	MDC	45
mii_mdio	135	167	MDIO	44
mii_rclk	128	160	RX_CLK	54
mii_rx_err	127	159	RXD_ER	55
mii_rxd<3:0>	133:130	165:162	RXD<3:0>	47:50
mii_tclk	124	153	TX_CLK	57
mii_txd<3:0>	119:122	148:151	TXD<3:0>	59:62
mii_txen	123	152	TX_EN	58

Table 36. 21145 SYM Connection

21145 Signal	144-Pin Package Pin Number	176-Pin Package Pin Number	LXT970 Signal	LXT970 Pin Number
sd	117	146	CRS	1
sel10_100	127	159	RXD_ER	55
sym_rclk	128	160	RX_CLK	54
sym_rxd<0>	130	162	RXD0	50
sym_rxd<1>	131	163	RXD1	49
sym_rxd<2>	132	164	RXD2	48
sym_rxd<3>	133	165	RXD3	47
sym_rxd<4>	118	147	RXD4	46
sym_tclk	124	153	TX_CLK	57
sym_txd<0>	122	151	TXD0	59
sym_txd<1>	121	150	TXD1	60
sym_txd<2>	120	149	TXD2	61
sym_txd<3>	119	148	TXD3	62
sym_txd<4>	123	152	TXD4	63

9.3.3 MII Management Interface

The management interface allows the 21145 controller to monitor and control the LXT970. This interface consists of a data line (MDIO) and a clock line (MDC). The 21145 addresses the LXT970 using a 5-bit address, which is set through the hardware control interface.

Operation of the management interface is determined by the MDDIS input of the LXT970. If MDDIS is low, the LXT970 supports both read and write operations. If MDDIS is high, the MDIO pin becomes a read-only interface.

9.3.4 MII Registers

Table 37 summarizes the MII registers supported by the LXT970. The LXT970 supports all the registers described in the IEEE 802.3 standard. It also supports several registers that have been defined by the manufacturer. For a complete description of the registers, consult the LXT970 data sheet (available from the manufacturer).

Table 37. MII Registers (Sheet 1 of 2)

Register	Usage
0	Standard 802.3 control register—enables Auto-Negotiation, sets speed/duplex state, and so forth.
1	Standard 802.3 status register—supplies link and Auto-Negotiation complete state
2	Vendor ID Register (802.3 defined)
3	Vendor/Revision ID (802.3 defined)
4	Advertisement Register (802.3 defined)

Table 37. MII Registers (Sheet 2 of 2)

Register	Usage
5	Link Partner's Advertisement Register (802.3 defined)
6	Standard 802.3 Register—contains various status bits regarding link and Auto-Negotiation state
16	Level One specific—mirrors Register 6
17	Level One specific—Interrupt Enable and Test Register
18	Level One specific—Interrupt Status Register
19	Level One specific—Control register, enables FX/TX, 4B/5B, and other modes
20	Level One specific—provides link, speed, and duplex status.

9.4 Hardware Control Interface

The hardware control interface allows the user to program operation of the LXT970 without using the MII management interface. This interface allows selection of the following:

- Copper or fiber media
- Normal or symbol mode
- Enabling or disabling of Auto-Negotiation
- Speed and duplex setting
- Advertisement
- PHY address (5 bits)

9.4.1 Multifunction Pins

The hardware control interface consists of the following pins: MF<4:0>, CFG<1:0>, and FDE. The MF pins are dual-function inputs that accept a quaternary (1-of-4) voltage level. The voltage levels are 5 V, 3.5 V, 1.5 V and 0 V. These can be established using three 1-kW resistors between Vcc and ground as shown in Figure 42. FDE and the CFG pins are simple one-function binary inputs.

The first function of the MF pins is to set the PHY address of the LXT970. If any input pin is high (5 V or 3.5 V), the corresponding PHY address bit will be set to 1. If any MF input is low (1.5 V or 0 V), the corresponding PHY address bit will be set to 0.

Each MF pin has a second function that sets a particular operational characteristic of the LXT970. Default voltage levels (5 V and 0 V) are used to set the operational characteristic one way. The "middle" voltage levels (3.5 V and 1.5 V) are used to set that characteristic the other way. Applications using the 21145 do not require all of the operational characteristics provided by the MF pins. Table 38 summarizes the multifunction pin functions and their settings.

Table 38. MF Pin Functions

MF Pin	Function	Default Voltages (5 V and 0 V)	Middle Voltages (3.5 V and 1.5 V)
MF0	Auto-Negotiation	Disable	Enable
MF1	Not Applicable	Always Use	Do Not Use
MF2	MII/SYM Mode	MII Mode (4B MII)	SYM Mode (5B MII)

Table 38. MF Pin Functions

MF Pin	Function	Default Voltages (5 V and 0 V)	Middle Voltages (3.5 V and 1.5 V)
MF3	Not Applicable	Always Use	Do Not Use
MF4	Operation of MF4 depends on status of Auto-Negotiation (A/N): enabled or disabled.		
	If A/N is disabled, select FX or TX.	Selects 100BASE-FX operation.	Selects 100BASE-TX or 10BASE-T operation.
	If A/N is enabled, MF4 works in combination with CFG1 and FDE. See Table 39.		

When Auto-Negotiation is disabled, MF4 selects between copper and fiber media. CFG0 sets the speed of the interface: 1=100 Mb/s and 0 = 10 Mb/s. If fiber is selected, CFG0 must be set high. FDE sets the duplex state of the interface: 1= full-duplex and 0 = half-duplex.

When Auto-Negotiation is enabled, MF4, CFG1 and FDE together determine what capabilities the LXT970 will advertise to its link partner. The LXT970 supports all capabilities (100Full/Half, 10Full/Half), but the system designer can choose what will be advertised. The link will always negotiate to the highest common denominator shared by both sides. Table 39 summarizes the choices.

Table 39. Operating Advertisement Capabilities

MF4 Voltage Setting	CFG1	FDE	Capabilities Advertised
Default	Low	N/A	All—100F, 100H, 10F, and 10H
Default	High	Low	10 Mb/s—Half only
Default	High	High	100 Mb/s —Half and Full only
Inner	Low	Low	100 Mb/s—Half only
Inner	Low	High	100 Mb/s— Half and Full only
Inner	High	Low	10 Mb/s—Half and 100 Half only
Inner	High	High	All—100F, 100H, 10F, and 10H

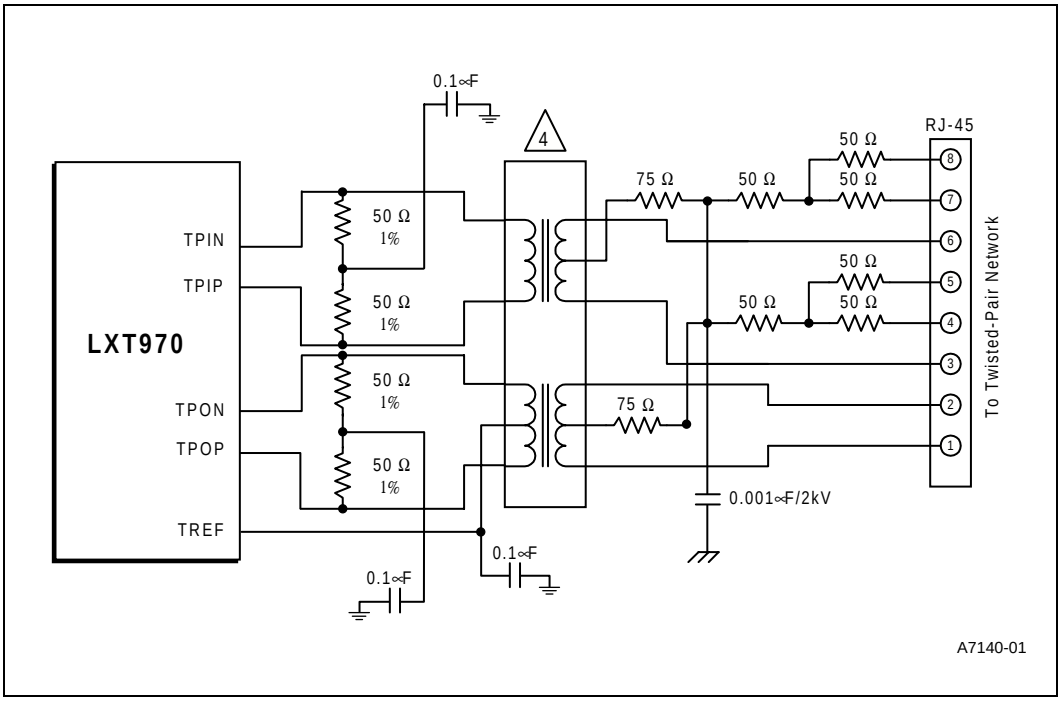
When Auto-Negotiation is disabled, CFG1 enables or disables the 10 Mb/s link detection function (0 = Disabled, 1 = Enabled). Normally, this function should be left enabled.

When Auto-Negotiation is enabled, a low-to-high transition on CFG0 causes Auto-Negotiation to restart. In this mode, CFG0 can be tied to ground.

9.5 Network Connection

Figure 41 shows layout of the components required for the twisted-pair network connection. This single interface can be used to drive both 100BASE-TX and 10BASE-T applications. When the fiber interface is used, the twisted-pair interface can be left disconnected (no components needed on inputs or outputs).

Figure 41. Twisted-pair Interface



9.5.1 Magnetics

The LXT970 requires a 1:1 ratio for both the receive and the transmit transformers. Table 40 lists some suitable magnetics.

Table 40. Suitable Magnetics

Manufacturer	Part Number
Halo	TG22-3506ND TG22-3506G1 TG22-S010ND TG22-S012ND

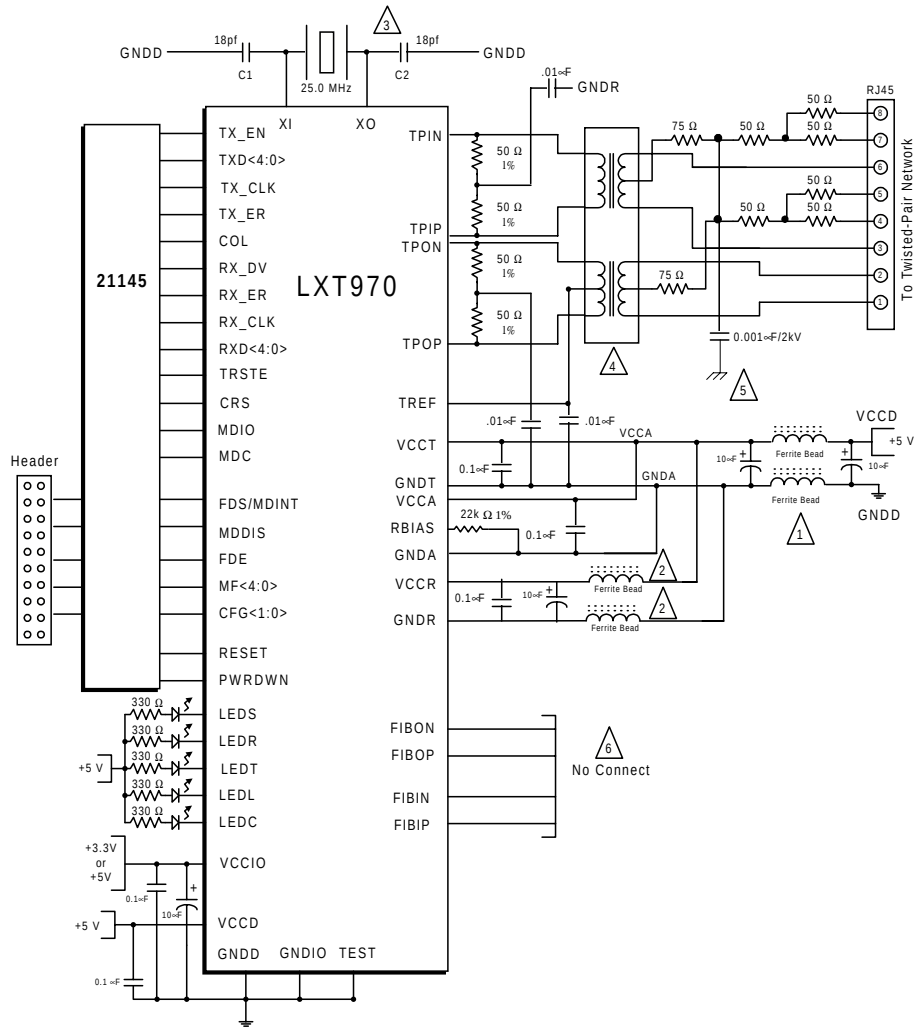
Table 40. Suitable Magnetics

Manufacturer	Part Number
Nanopulse	NPI 6120-30 NPI 6120-37 NPI 6170-30 NPI 6181-37
Pulse	PE-68517 PE-68515
Valor	ST6114 ST6118

9.5.2 Schematic Information

Figure 42 shows a typical schematic layout of the LXT970 and 21145 LAN controller.

Figure 42. LXT970 Schematic



9.6 External Components

This section shows external component requirements for the network connection.

9.6.1 Clock Requirements

The LXT970 requires a constant clock that must be enabled at all times. An external 25 MHz crystal connected across XI and XO is recommended to supply the LXT970 internal clock reference. See Table 41 for some suitable crystal components and manufacturers. The LXT970 automatically sets the speed of TX_CLK and RX_CLK to match line conditions. If the line is operating at 100 Mb/s, TX_CLK and RX_CLK will be set to 25 MHz. If the line is operating at 10 Mb/s, or the LXT970 is auto-negotiating, TX_CLK and RX_CLK will be set to 2.5 MHz.

Table 42 contains a listing of the external components.

Table 41. Suitable Crystals

Manufacturer	Part Number
CTS	CTX093
Epson America	MA-505-25.000M-C2

Table 42. 21145/LXT970 NIC External Components

Quantity	Reference	Description
5	Capacitor	0.1µF 50 V 10%, 1206 SMD
4	Capacitor	10 µF 6.3 V, SMD DAP EIA A
2	Capacitor	18 pF 50 V 5%, .0805
2	Capacitor	0.01 µF 50 V 10%, .0805 SMD
3	LED	Red LED DIFF
2	LED	Green LED DIFF
1	LED	Yellow LED DIFF
1	RJ45 Connector	RJ45 1-Position Jack Shielded PC Grade
4	Ferrite Beads	Ferrite SMD Bead
1	Connector	25-pin Dual Row Header
5	Resistor	332 Ω 1% Metal SMD Resistor
10	Resistor	49.9 Ω 1% Metal SMD Resistor
2	Resistor	75 Ω 1% Metal SMD Resistor
1	Resistor	22 KΩ 1% Metal SMD Resistor
2	T1	10/100 MB Transformer
1	PHY Transceiver	LXT970
1	IC	HEX Inverter SMD SO-14 Package
1	MAC Controller	Intel 21145 LAN Controller 144-pin PQFP
1	EEPROM	1-Kb 5 V EEPROM 8 DIP Package
1	IC	Surface Mount PLCC Package–90ns
1	Crystal	25 MHz Crystal HC49 Case

9.7 Layout Requirements

This section contains details on PCB layout requirements.

9.7.1 Twisted-Pair Interface Layout Considerations

When designing for a twisted-pair interface, consider the following:

- The transformer isolation voltage should be rated at 2 KV to protect the circuitry from static voltages across the connectors and cables.
- Place the transformer as close as possible to the connector.
- The traces running from the transformer to the connector should run in close pairs directly to the connector.
- Be careful not to cross the transmit and receive pairs.
- Vias should be avoided as much as possible.

9.7.2 Plane Layout Considerations

Ground plane layout depends on the availability and quality of chassis ground. If a solid circuit ground is not available, there should be no power or ground planes in the area between the LXT970, the transformers, and the connectors. High-frequency noise on these planes causes interference on the data signals and induces EMI emissions. The data signals should be the only traces in this area, except for the termination of unused pairs or LEDs.

If a solid and quiet circuit ground is available that is well-decoupled from the active power and ground planes, it can be routed under the twisted-pair signal traces to reduce EMI emissions. However, this should always be a secondary approach. The primary goal should always be to make each differential pair perfectly matched and completely self-sufficient, meaning that all magnetic and electrical fields are completely canceled between the pair. A recommendation is to pretend that no ground plane whatsoever is available, and then if one is available, use it only as necessary.

A good design practice is to create a chassis ground at the edge of the card that is completely isolated from circuit ground. Unused connections can be terminated to chassis ground through what is commonly called a “Bob Smith” network. The center taps of the line side of the magnetics can also be referenced to chassis ground. 2 KV isolation caps must be put either between the line connections and chassis ground, or between chassis ground, and circuit ground. No active signals should be routed over chassis ground except for differential line signals and LED outputs.

9.7.3 The RBIAS Pin

The RBIAS pin sets the levels for the LXT970 output drivers. Any emissions or common mode noise entering the device here could be measured on the twisted pair output signals. The LXT970 requires a 22.1 KΩ, 1% resistor directly connected between the RBIAS pin and ground. This resistor should be as close to the device as possible and the traces should be as short as possible. Keep all high-speed signals away from the RBIAS pin. The ground traces from adjacent pin GNDA should come directly off the device to enclose the resistor and pin-forming a shielded area between the RBIAS connection and the switching signals on the PCB.

9.7.4 Power Supply Decoupling

Ferrite beads are recommended for decoupling the analog and digital supplies. Two beads are recommended for all applications—one on Vcc and one on ground. The Vcc bead can be used to supply the VCCR, VCCT and VCCA pins. The ground bead can be used to supply the GNDA, GNDT, and GNDR pins.

For applications where long line length is important (>120 m), a second set of beads for GNDR and **VCCR** is recommended. The ferrite bead used should have an impedance of at least 100 ohms at 100 MHz. A suitable bead is the Panasonic surface mount bead, part number EXCCL4532U, or equivalent.

9.7.5 Bypass Caps

Bypass caps are required between each supply and its associated ground return **(**VCCA/GNDA, VCCR/GNDR, CCT/GNDT, VCCD/GNDD and VCCIO/GNDIO). The recommended capacitor is 0.01 µF. The 10 µF tantalum capacitors are recommended between each Vcc plane and its associated ground plane—in other words on the LXT970-side of each pair of ferrite beads.

Extra decoupling is recommended on the VCCIO pin, which is the supply for the MII interface.

For a standard crystal capable of driving an 18 pF load, a 15 pF capacitor to digital ground is recommended on each side of the crystal.

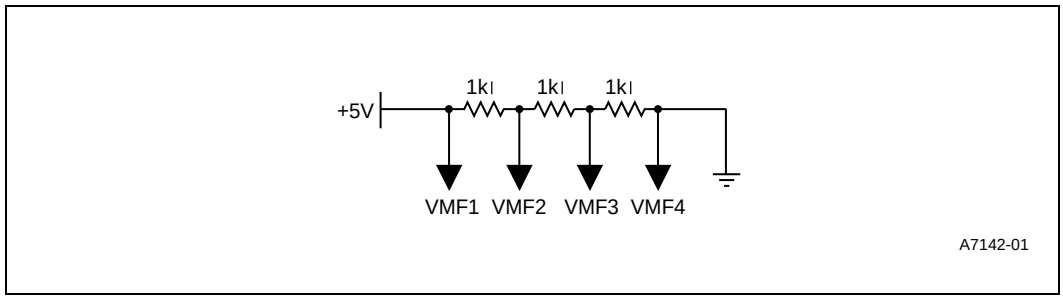
9.7.6 MII Interface

The MII interface is supplied by the VCCIO pin. This interface can be driven with either a 3.3 V or 5 V supply. When operating in 3.3 V mode, it is not 5 V tolerant that is, it cannot be interfaced to devices driving 5 V signals. Ample bypassing and decoupling is recommended on the VCCIO input (55 Ω series termination resistors are recommended on all MII signal lines).

9.7.7 Voltage Divider for MF Inputs

The LXT970 requires an external voltage divider to provide optional (Vmf2 and Vmf3) multilevel inputs to the multifunction (MF) pins. These voltage levels are designated as Vmf1–Vmf4. Figure 43 **s**hows a voltage divider with three 1 KΩ resistors configured in series between Vcc and ground. A single voltage divider may be used to drive the MF pins in applications using multiple LXT970s.

Figure 43. Voltage Divider



9.8 LXT970 Summary

This section provided the designer with sufficient information to design an interface between the 21145 and the LXT970 Fast Ethernet transceiver. Using the information in this section, a NIC can be designed using the built-in Auto-Negotiation and 10BASE-T functions of the 21145 and the 100BASE-TX functions of the LXT970.

Appendix A National Semiconductor License Agreement

A.1 Common Magnetics License Agreement

Dear Customer:

The attached application notes describe a common magnetics implementation of a 10/100 Ethernet physical layer and transceiver using National Semiconductor Corporation's DP83840AVCE 10/100 Mb/s Ethernet Physical Layer and DP83223V TWISTER™ High Speed Networking Transceiver Device.

The following suppliers have indicated that they intend to provide magnetic components for the National Semiconductor Corporation recommended implementation. This is not an exclusive list and National Semiconductor makes no warranty as to the suitability of any of the magnetics suppliers listed:

- Bel Fuse
- Fil-Mag Technical
- HALO Electronics
- Kappa Technology
- Nano Pulse
- PCA
- Pulse Engineering
- Valor Electronics
- TDK

The above referenced companies' product(s) in conjunction with National Semiconductor Corporation's part number DP83840AVCE 10/100 Mb/s Ethernet Physical Layer and National Semiconductor Corporation's part number DP83223V may be designed as a common magnetics front end for a 10/100 Mb/s Ethernet system. A system utilizing this common magnetics arrangement is intended to provide combination 10BASE-T and 100BASE-T capabilities.

National Semiconductor Corporation's part number DP83223V is covered by U.S. Patent Nos. 5,337,025 and 5,444,410, and the system and methods of operation of the common magnetics arrangement are covered by one or more pending patents of National Semiconductor Corporation. National Semiconductor Corporation offers a non-transferable license under the patents, which license is subject to royalties to be agreed on between National Semiconductor Corporation and the customer. National Semiconductor hereby also grants purchasers of both National Semiconductor Corporation's DP83840AVCE 10/100 Mb/s Ethernet Physical Layer and DP83223V components a non-exclusive, paid-up, non-transferable license under such pending patents and those patents which issue therefrom, to make, use and sell such systems **which utilize both of National Semiconductor Corporation's DP83840AVCE 10/100 Mb/s Ethernet Physical Layer and DP83223V components**.

A.2 National Semiconductor Physical Layer Design Recommendations

Figures Figure 44–Figure 48 represent the National Semiconductor 10/100 Ethernet Physical Layer design recommendations. This implementation might vary from the Intel Semiconductor Reference Design, due to the designer's preferences, and might differ from any other given application implementation as well. Again these recommendations are intended to improve the designer's understanding of Fast Ethernet systems, and with that understanding, a designer is able to develop systems more effectively.

Note: The value of C8 should be 820 pF instead of 1000 pF as shown in Figure 47.

Figure 44. 10/100 Ethernet Physical Layer Block Diagram

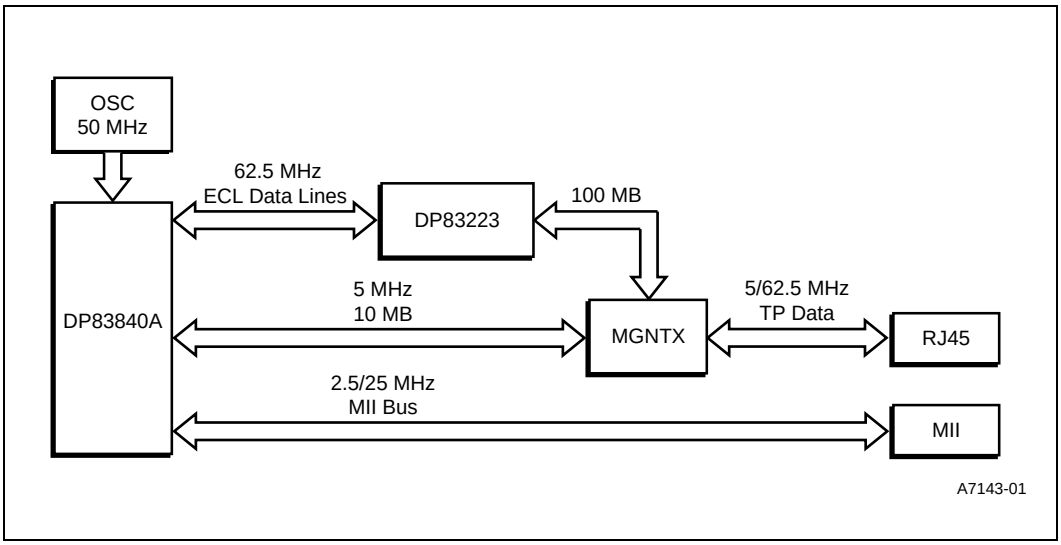


Figure 45. DP83840A

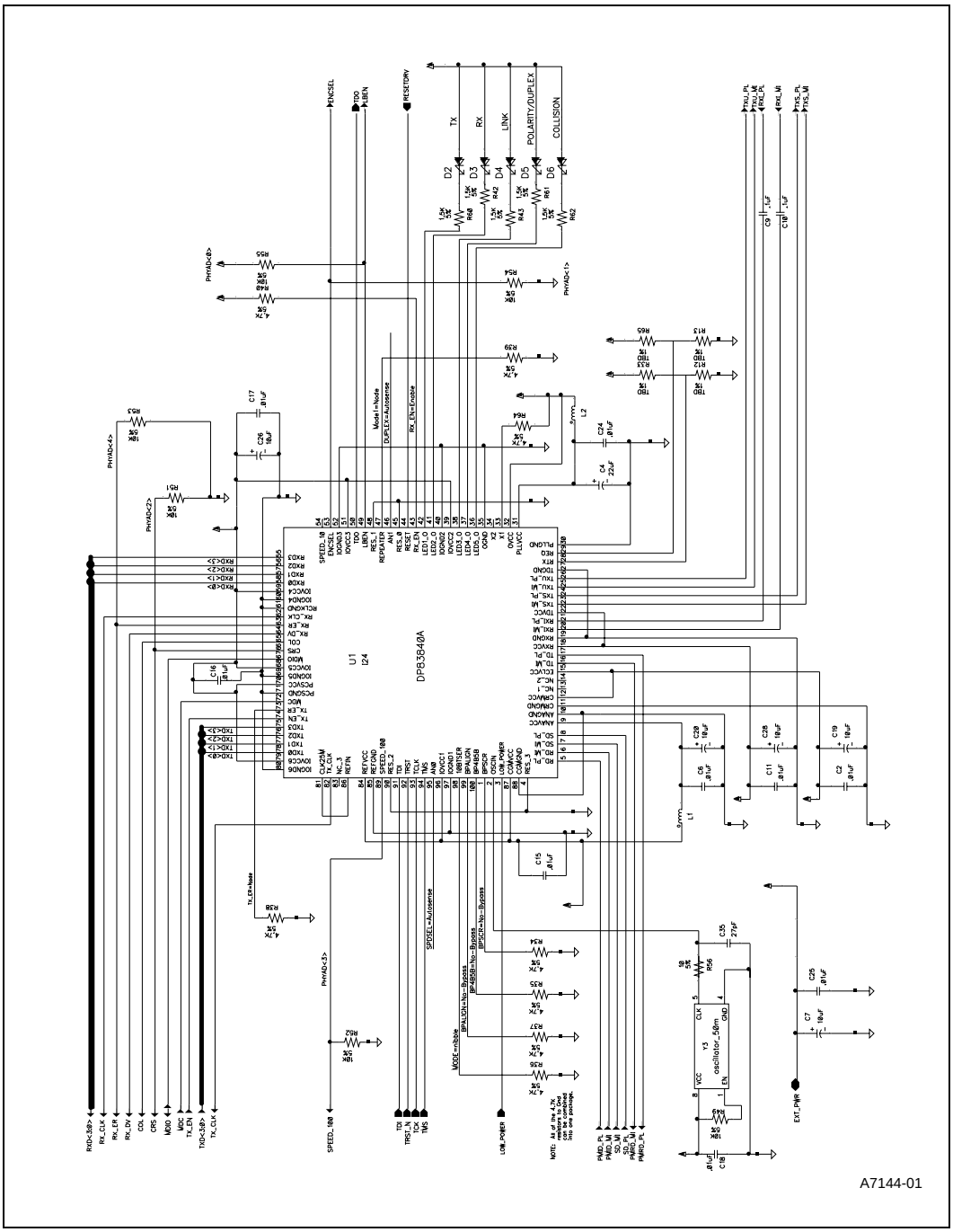


Figure 46. DP83223V

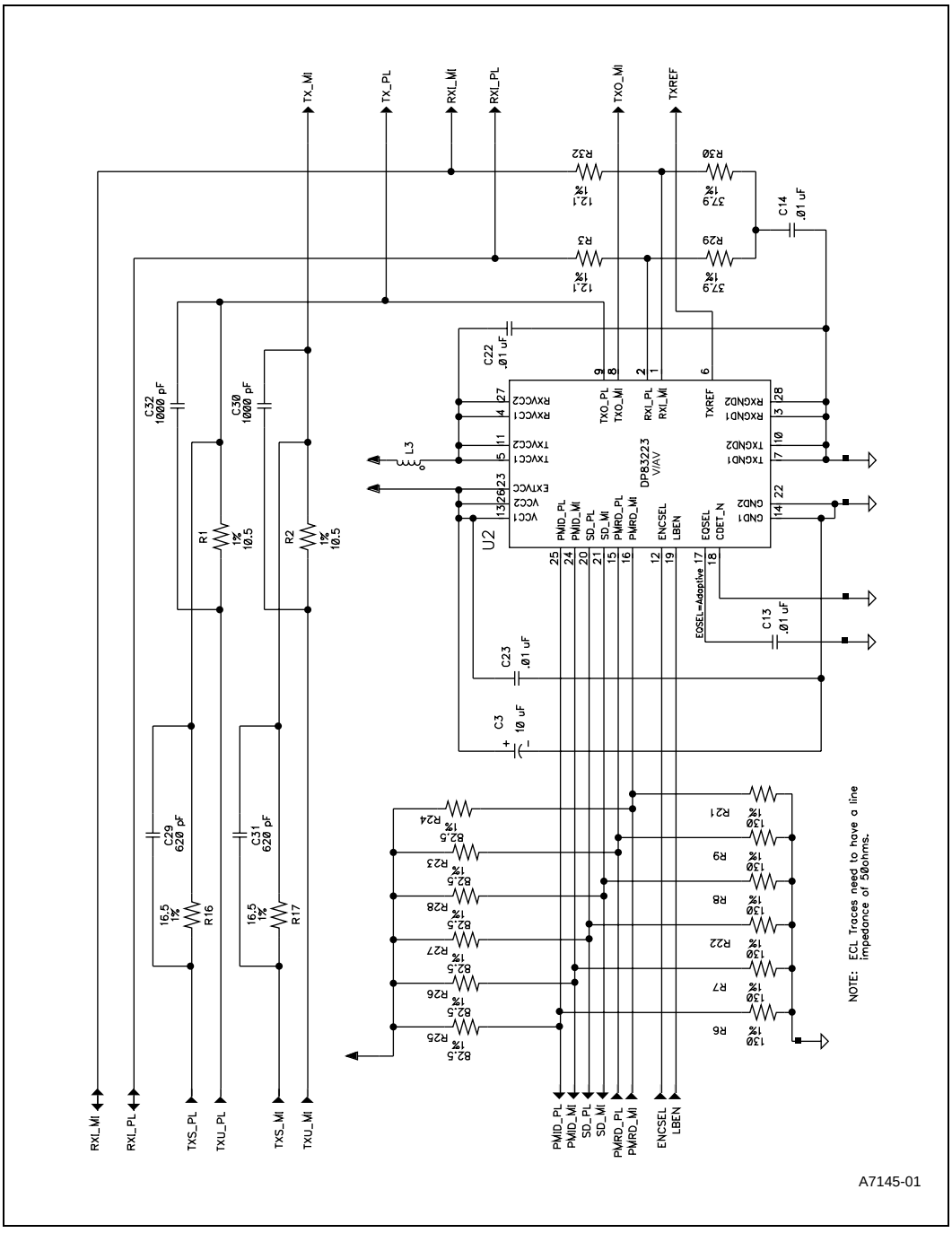


Figure 47. Twisted Pair

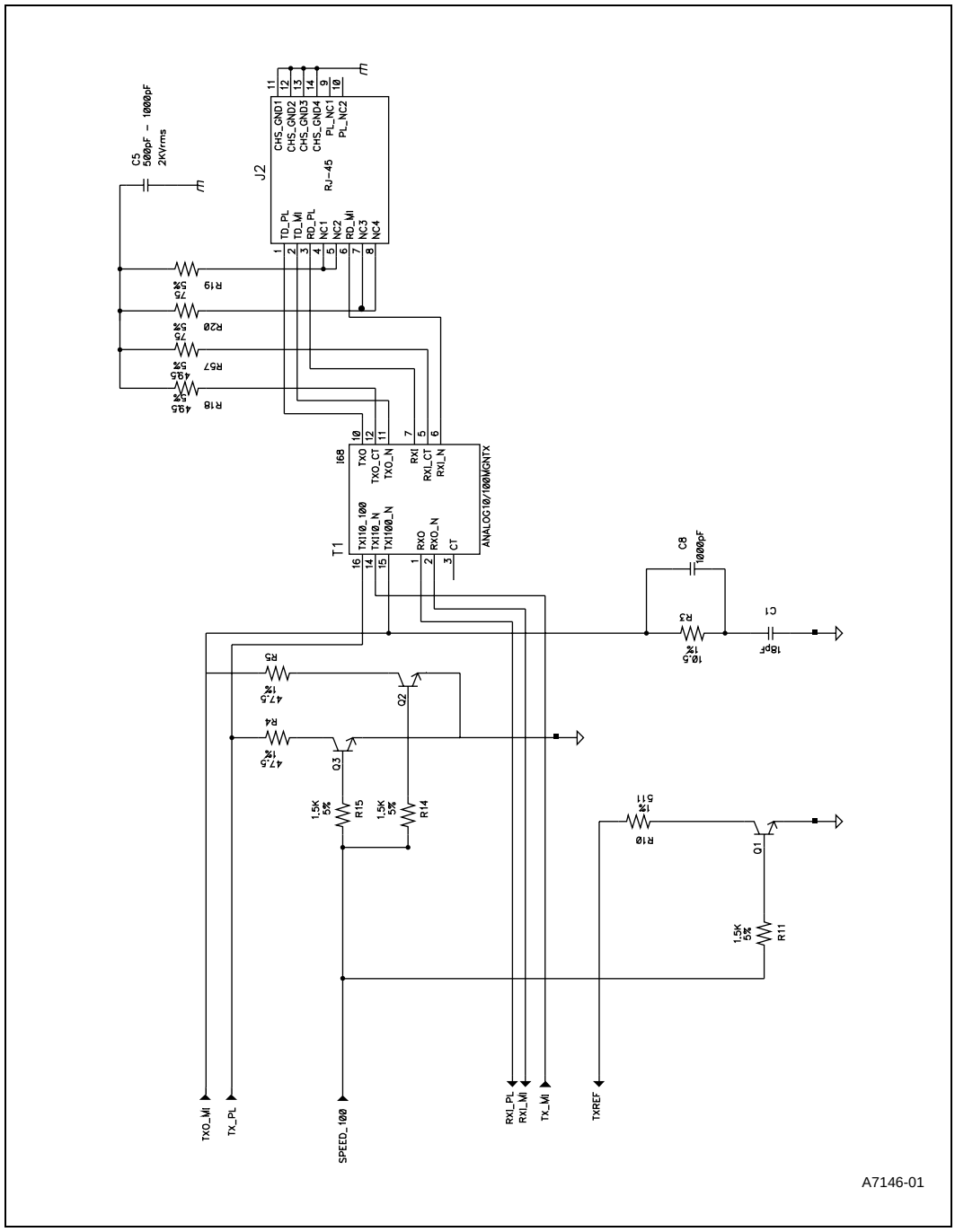
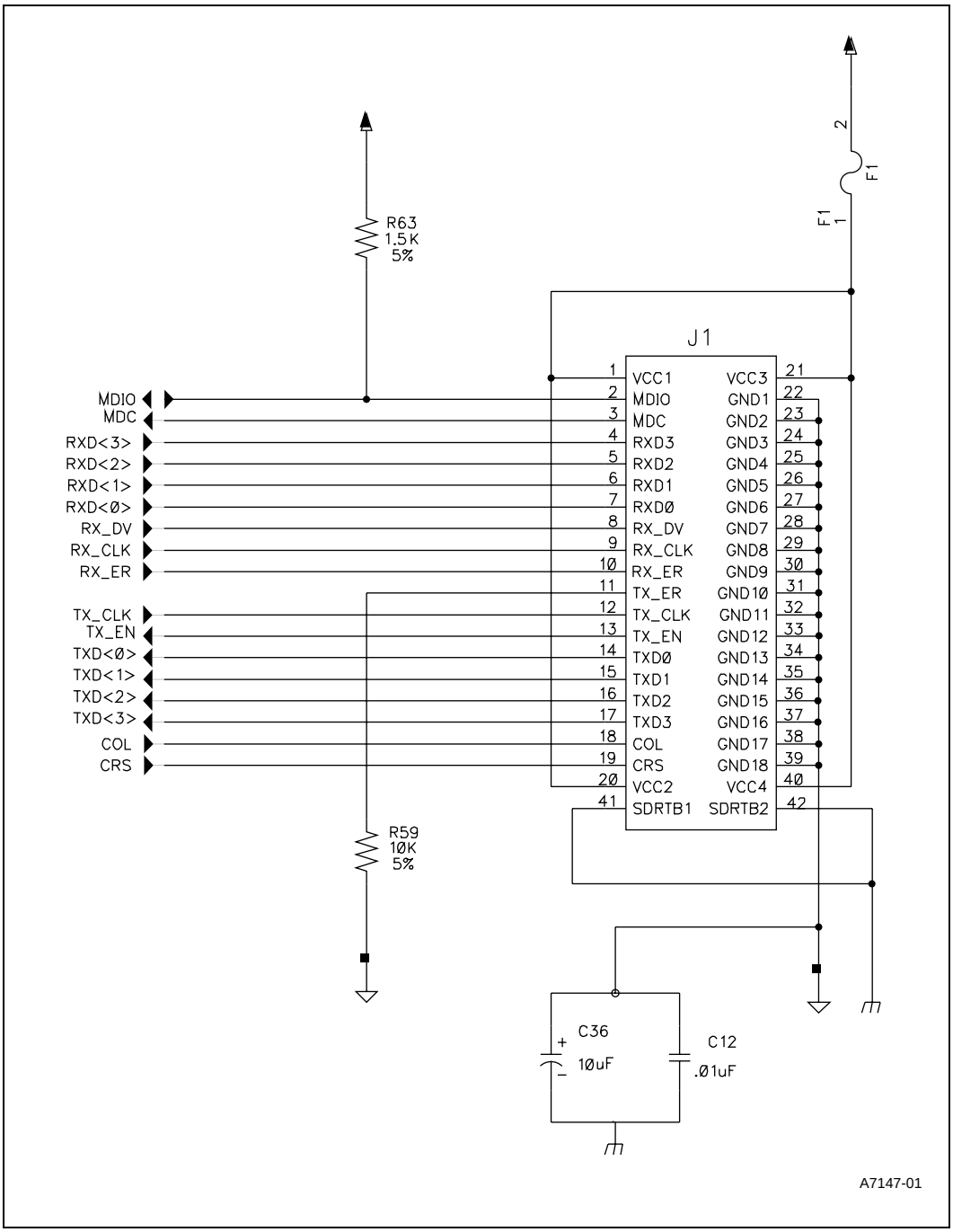


Figure 48. MII Interface



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