CMOS μ-255 law CODEC set
designed for . . .

Siliconix

- ■ **Channel Banks**
- ■ **Central Offices and PABXs**
- ■ **Microprocessor Interface**
- ■ **Remote Data Acquisition Systems**
- ■ **Audio Delay Lines**
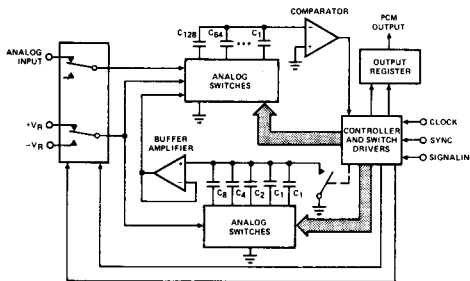
BENEFITS

- ● Minimizes System Power Requirements
  - ○ Standby Power 11 mW Typ
  - ○ Typical Power 80 mW
- ● Reduces External Component Requirements
- ● Reduces System Costs
- ● Easily Interfaced
- ● Eliminates Channel Crosstalk Problems
- ● Eliminates External Signalling Logic
- ● No External Zero Code Suppression Required
- ● Reduced System Noise Problems
- ● No External Sample and Hold or MUX Required
- ● No Additional Logic Required for Extended Bandwidth Applications
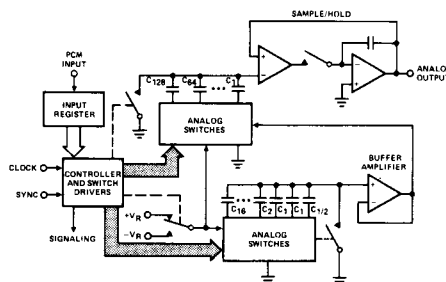 - ○ 3.5 to 9 KHz Bandwidth Possible With Clock Frequency From 1.25 to 3.0 MHz

DESCRIPTION

The DF331A (coder) is an A/D converter which has a transfer characteristic conforming to the telecommunication industry μ-255 law. Its counterpart, the DF332A or DF334A (decoder) is a D/A converter which also conforms to the μ-255 law.

Together the DF331A and DF332A or DF331A and DF334A form a CODEC (coder-decoder set) which is designed to meet the needs of the telecommunications industry for per channel voice frequency CODECs used in PCM Channel Bank and PBX systems. Digital output and input of the coder and decoder is in serial format. Actual transmission and reception of 8-bit data words containing the analog information is typically done at a 1.544 megabit/sec rate with analog signal sampling occurring at an 8 KHz rate. A sync pulse input pin is provided for synchronizing transmission and reception of multi-channel information being multiplexed over a single transmission line. The DF332A and DF334A differ in the output device for the A/B signal output pins, refer to the Functional Description. The devices have TTL logic input levels of 0.6 V and 3.4 V that are compatible with TTL logic using a pullup resistor to +5 V; they directly interface to CMOS logic.

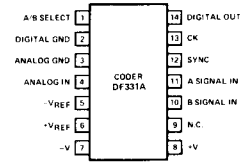## FUNCTIONAL BLOCK DIAGRAMS

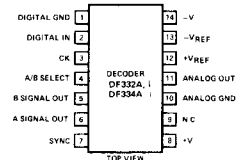
DF331A

DF332A, DF334A

Figure 1

PIN CONFIGURATIONS

Dual In-Line Package

A/B SELECT 1		14 DIGITAL OUT
DIGITAL GND 2		13 CK
ANALOG GND 3	CODER	12 SYNC
ANALOG IN 4	DF331A	11 A SIGNAL IN
−VREF 5		10 B SIGNAL IN
+VREF 6		9 N.C.
−V 7		8 +V

TOP VIEW

PLASTIC DIP
ORDER NUMBER: DF331ACJ
SEE PACKAGE 7

CERAMIC DIP
ORDER NUMBER: DF331ACP
SEE PACKAGE 11

Dual In-Line Package

DIGITAL GND 1		14 −V
DIGITAL IN 2		13 −VREF
CK 3		12 +VREF
A/B SELECT 4	DECODER	11 ANALOG OUT
B SIGNAL OUT 5	DF332A, I DF334A	10 ANALOG GND
A SIGNAL OUT 6		9 N.C
SYNC 7		8 +V

TOP VIEW

PLASTIC DIP
ORDER NUMBER: DF332ACJ, DF334ACJ
SEE PACKAGE 7

CERAMIC DIP
ORDER NUMBER: DF332ACP, DF334ACP
SEE PACKAGE 11

ABSOLUTE MAXIMUM RATINGS

V_{in} (Digital Inputs) . . . -0.3 V, $\leqslant V_{in} \leqslant +V +0.3$ V
V_{in} (Analog Inputs) . . . $-V -0.3$ V, $\leqslant V_{in} \leqslant +V +0.3$ V
$+V$ . . . . $0 \leqslant +V \leqslant 11$ V
$-V$ . . . . -11 V $\leqslant -V \leqslant 0$
$+V_{ref}$ . . . . $-V \leqslant +V_{ref} \leqslant +V$
$-V_{ref}$ . . . . $-V \leqslant -V_{ref} \leqslant +V$

V_O (Digital Output) DF331A, DF334A . . $-0.3V \leqslant V_O \leqslant 15V$
$V_{A/B}$ Signal Out DF332A . . . $+V+0.3$ V $\geqslant V_O \geqslant -7.5$ V
Operating Temperature . . . . 0 to $70°C$
Storage Temperature . . . . -55 to $+125°C$
Power Dissipation . . . . 450 mW
Derate 6.5 mW/$°C$ above $25°C$

Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at $25°C$. Lots are sample-tested for AC parameters to assure conformance with specifications.

		Characteristic	$T_A = 25°C$			Unit	Test Conditions, See Note 2 Clock = 1.544 MHz, Sample Rate = 8 KHz, $+V = 7.5$ V, $-V_{ref} = -3.0$ V, $-V = -7.5$ V, $+V_{ref} = 3.0$ V, $R_L = 820$ Ω, $C_L = 12.5$ pF
			Min	Typ Note 1	Max		
DC Characteristics DF331A (Coder)							
1	I N P U T S	I_{in} (Analog) Analog Input Current		0.5		mA	See Note 3
2		I_{inL} (Clock) Clock Input Low Current		-0.1	-100		$V_{IN} = 0$
3		I_{inL} (Sync) Sync Input Low Current		-0.1	-100	nA	
4		I_{inH} (Clock) Clock Input High Current		0.1	100		$V_{IN} = 7.5$ V
5		I_{inH} (Sync) Sync Input High Current		0.2	100		
6		R_{in} (Analog) Analog Input Series Resistance		1		$K\Omega$	Present During Sampling Time Only
7		C_{in} (Analog) Analog Input Series Capacitance		200		pF	
8		V_{offset} Analog Input Offset Voltage		5	10	mV	
9	O U T	C_O (Digital) Digital Output Capacitance		3		pF	$V_O = 7.5$ V
10		V_{OL} Digital Output Low Voltage		0.3	0.5	V	$I_{OL} = 3$ mA
11		V_{OH} (max) Digital Output High Voltage			12		$I_{OH} = 10$ μA
12	S U P P L Y	I^+ Positive Supply Current		2.5	6		Clock = 1.544 MHz Sample Rate = 8 KHz
13		I^- Negative Supply Current		-2	-6	mA	
14		I^+_{stdby} Standby Positive Supply Current		0.6			Analog Ground (Pin 3) Open
15		I^-_{stdby} Standby Negative Supply Current		-0.05			
16		Supply Tolerance		±10		%	
17		I_{ref}^+ Positive Reference Current		3.5		μA	Average Current See Note 3
18		I_{ref}^- Negative Reference Current		-3.5			
AC Characteristics DF331A (Coder)							
19	D Y N A M I C	$|t_{ds}|$ Sync to Clock Delay Time			100		
20		$t_{d(on)}$ Digital Output to Sync Delay Time		75	130		
21		$t_{d(off)}$ Digital Output to Sync Delay Time		165	220		See Figure 2
22		t_{dbr} Digital Output to Clock Delay Time		65	130		
23		t_{dbf} Digital Output to Clock Delay Time		70	130	ns	
24		t_{fo} Digital Output Fall Time		65	130		$C_L = 100$ pF
25		t_{ro} Digital Output Rise Time		175	250		
26		t_{ss} (min) A/B Signaling Input Setup Time			200		See Figure 4
27		t_{scs} (min) A/B Select Setup Time			1000		
28		DC_c Clock Duty Cycle	30		70	%	
29		t_{conv} Complete A/D Conversion (Sampling, Data Storage, Resetting)			168	clocks	

DF331A DF332A DF334A

Telecommunications

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ELECTRICAL CHARACTERISTICS (Cont'd)

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters to assure conformance with specifications.

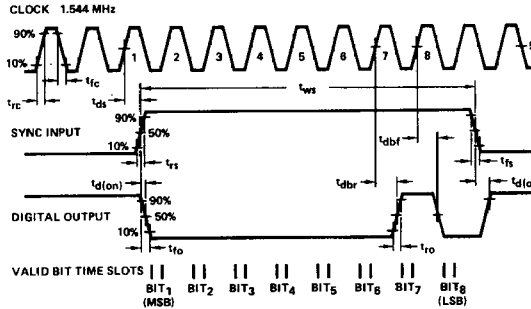|		Characteristic		Min	Typ Note 1	Max	Unit	Test Conditions, See Note 2 +V = 7.5 V, −V = −7.5 V, V_{ref} = 3.0 V, −V_{ref} = −3.0 V, Clock = 1.544 MHz, Sync = 8 KHz Period, 8 Clock Pulses Wide
DC Characteristics DF332A, DF334A (Decoder)								
1	I N	I_{inL} (Logic)	Digital Inputs Low Current		−0.1	−100	nA	V_{in} = 0
2		I_{inH} (Logic)	Digital Inputs High Current		0.1	100		V_{in} = 7.5 V
3		I_{OL} (Signaling)	A/B Output Low Current — DF332A Only		0.1	100		V_{OL} = 0
4		I_{OH} (Signaling)	A/B Output High Current — DF332A Only	0.2	0.5		mA	V_{OH} = 6.5 V
5	O U T	V_{OH} (max) (Signaling)	A/B Output High Voltage — DF334A Only			12	V	I_{OH} = 10 µA
6		V_{OL} (Signaling)	A/B Output Low Voltage — DF334A Only		0.3	0.5		I_{OL} = 1.5 mA
7		C_L (Analog)	Analog Output Load Capacitance			100	pF	
8		R_0 (Analog)	Analog Output Series Resistance		50	150	Ω	See Input/Output Schematics, See Note 4
9		V_{offset}	Analog Output Offset Voltage		50	100	mV	
10	S U P P L Y	I^+	Positive Supply Current		3.5	8		
11		I^-	Negative Supply Current		−2.5	−7	mA	
12		I^+_{stdby}	Standby Positive Supply Current		0.8			Analog Ground (Pin 10) Open
13		I^-_{stdby}	Standby Negative Supply Current		−0.07			
14			Supply Tolerance		±10		%	
15		I_{ref}^+	Positive Reference Current		3.5		µA	Average Current See Note 3
16		I_{ref}^-	Negative Reference Current		−3.5			
AC Characteristics DF332A, DF334A (Decoder)								
17	D Y N A M I C	t'_{ds}	Sync to Clock Delay Time	25		450		See Figure 3
18		t'_{dc}	Clock to Sync Delay Time	10				
19		t'_{sd}	Data to Clock Setup Time	100			ns	
20		t'_{scs} (min)	A/B Select Setup Time			1000		See Figure 5
		t'_d	A/B Output Delay Time		5	10	µs	
21		t'_{do}	Analog Output to Sync Delay Time			15		See Figure 3
22		$Slew^+$	−3 V to +3 V Analog Output Slew Rate		5		V/µs	C_L = 100 pF
23		$Slew^-$	+3 V to −3 V Analog Output Slew Rate		5			
24		Droop	Analog Output Droop Rate		0.01		%/µs	
25		t'_{conv}	Complete D/A Conversion (from Data Input, to Analog Output and Internal Resetting)			39	clocks	
System Characteristics, Per Individual Part: DF331A, DF332A, DF334A								
26	S Y S T E M	S/D	Signal to Total Distortion: Total of Quantizing Noise, Thermal Noise and Harmonic Distortion with Sinusoidal Input and C Message Weighting Filter. See Note 5	35	39			P_{in} = 0 to −30 dBmO
27				30	34			P_{in} = −40 dBmO
28				25	30			P_{in} = −45 dBmO
29		G_T	Gain Tracking: Deviation of Gain from 0 dBmO Input Sinusoidal Signal	−0.25	±0.15	+0.25	dB	P_{in} = +3 to −40 dBmO
30				−0.5	±0.15	+0.5		P_{in} = −40 to −50 dBmO
31				−1.5	±0.25	+1.5		P_{in} = −50 to −55 dBmO
			Deviation of Gain from −10 dBmO, White Noise Source Signal Input	−0.25	±0.1	+0.25		P_{in} = −10 to −55 dBmO
				−0.5	±0.2	+0.5		P_{in} = −55 to −60 dBmO
32		N_{IC}	Idle Channel Noise: Coder (DF331A) to Decoder (DF332A or DF334A) of Known Quiet Code Output		12	15	dBrncO	V_{in} = 0
33		N_{QC}	Quiet Code Output: Output of Decoder (DF332A or DF334A) for +0 V Equivalent Digital Input Coder		10	12		Digital In = All "1" (Corresponds to +0 V Input)

f_{in} = 1020 Hz +3 dBmO = 3 V Peak into Coder

NOTES:
1. Typical values are for Design Aid only and not subject to production testing.
2. $V_{in} \geqslant$ 3.4 V for logic "1", $V_{in} \leqslant$ 0.6 V for logic "0" for logic input levels.
3. Peak currents of up to 2 mA occur during reconstruction of Analog Output and during encoding of Analog Input.
4. Use of a load resistance $\geqslant$ 10K Ω is recommended to avoid output attenuation.
5. Specifications are for pair (coder and decoder)

DF331A ICBL-II
DF332A ICBM-II-A
DF334A ICBM-II-B

SWITCHING AND LOGIC WAVEFORMS

DF331A Coder Waveforms
Figure 2A

Parameter		Test Condition	Min	Max	Unit
t_{rc}	Clock Rise Time	50		100	
t_{fc}	Clock Fall Time	50		80	ns
t_{rs}	Sync Rise Time	50		100	
t_{fs}	Sync Fall Time	50		100	
t_{ws}	Sync Pulse Width	5.18	$8/F_{CLOCK}$		μs
t_{ps}	Sync Pulse Period	125			

DF331A Coder Waveforms
Figure 2B

Parameter		Test Condition	Min	Max	Unit
t'_{rc}	Clock Rise Time	50		100	
t'_{fc}	Clock Fall Time	50		80	ns
t'_{rs}	Sync Rise Time	50		100	
t'_{fs}	Sync Fall Time	50		100	
t'_{ws}	Sync Pulse Width	5.18	$8/F_{CLOCK}$		μs
t'_{ps}	Sync Pulse Period	125			

DF332A, DF334A Decoder Waveforms
Figure 3B

DF332A, DF334A Decoder Waveforms
Figure 3A

DF331A Signaling Waveforms
Figure 4

DF332A, DF334A Signaling Waveforms
Figure 5

1-15

FUNCTIONAL DESCRIPTION

Analog Input (Coder DF331A): The analog input accepts signals which have peak amplitudes less than the value of the voltage references, and which are bandlimited to less than 1/2 of the CODEC sample rate.

Digital Output (Coder DF331A): The digital output of the encoder is an 8-bit serial bit stream which is a sign-plus-magnitude binary representation of the analog input. This output is an open drain N-channel output, which allows for easy wire-OR multiplexing.

Sync Input (Coder and Decoder): The sync input accepts a sync pulse which should be 8 clock periods wide. The period of the sync pulse sets the sample rate. The sync pulse causes the encoder to serially shift its digital output data out at a rate equal to that of the clock, and it causes the decoder to accept the serial digital data.

Clock Input (Coder and Decoder): The clock input accepts a clocking signal which sets the data transmission rate for the CODEC, and also provides the clocking of the internal CODEC logic. Typical clock rate is 1.544 MHz.

Digital Input (Decoder DF332A, DF334A): The digital input accepts the 8-bit serial data output of the encoder upon reception of the sync pulse.

Analog Output (Decoder DF332A, DF334A): The analog output of the decoder is in the form of voltage steps having a width equal to the inverse of the sample rate, with amplitude equal to the value of the sample of the signal taken at the encoder analog input.

Reference Voltage Inputs (Coder and Decoder): Positive and negative DC reference voltages are required for both encoding and decoding. The maximum analog signal swing is set by the reference voltages.

Signaling Inputs and A/B Select (Coder DF331A): Two signaling inputs A and B are provided on the encoder allowing insertion of digital signaling data into the transmitted bit stream, which allows telecommunications users to transmit digital signaling information along with the data stream. When signaling is enabled, the voice signal is encoded with only 7 bits, the 8th bit being used for signaling. The signaling function is enabled by the application of a transition to the A/B select input. A positive transition at the A/B select input will insert the data at the A input into the 8th bit (the LSB) position in the transmitted word, whereas a negative transition will insert the data at the B input into the 8th bit position in the transmitted word. Refer to the timing diagram in Figure 4. To disable signaling function, simply tie the A/B select input to logic high or low, so that no transitions appear.
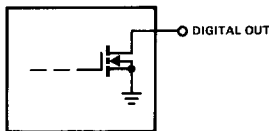
Signaling Outputs and A/B Select (Decoder DF332A, DF334A): Two outputs are provided on the decoder to output the signaling data. Application of a positive transition to the A/B select input places the 8th bit (the LSB) of the transmitted word at the A signaling output. Application of a negative transition to the A/B select input places the LSB at the B signaling output. These outputs are open drain P-channel outputs on the DF332A and are open drain N-channel outputs on the DF334A. Refer to output schematic for configuration, and to Figure 5 for timing waveforms.
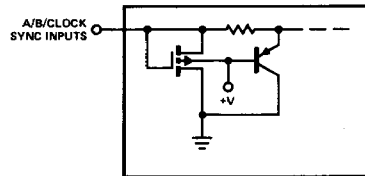
INPUT-OUTPUT CIRCUIT SCHEMATICS

Analog Input (DF331A)
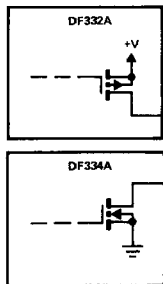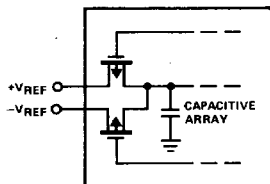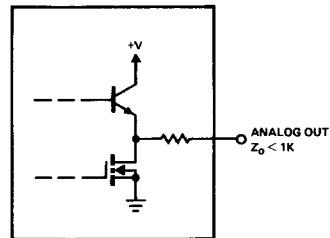
Digital Output (DF331A)

Digital Inputs

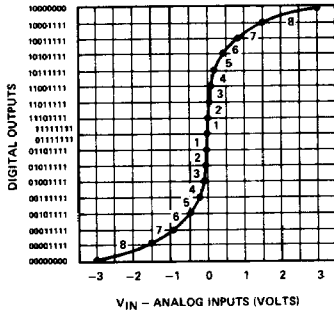A/B Signaling Outputs (DF332A, DF334A)

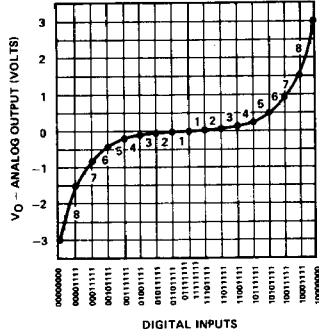Reference Inputs

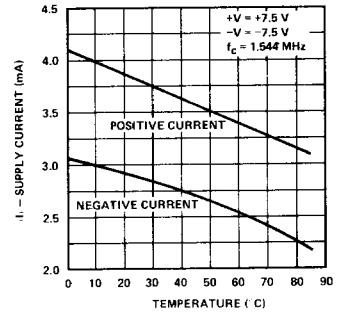Analog Output (DF332A, DF334A)

TYPICAL CHARACTERISTICS

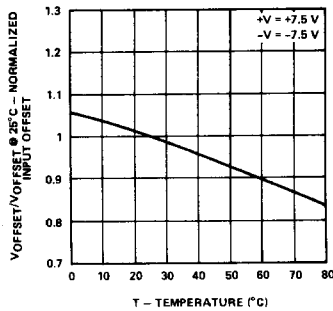### DF331A μ-Law Coder Transfer Characteristic

DF332A μ-Law Decoder Transfer Characteristic
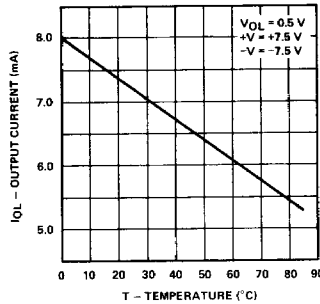

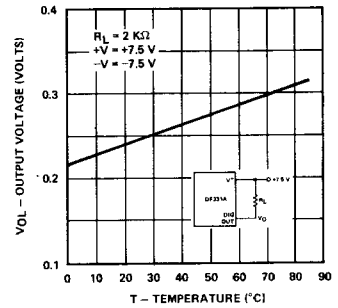### Positive and Negative Supply Current vs Temperature DF331A

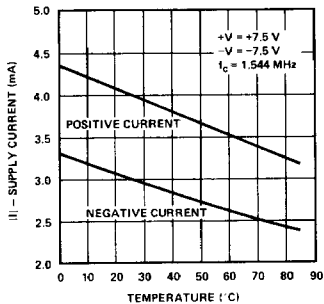

Normalized Input Offset vs Temperature DF331A

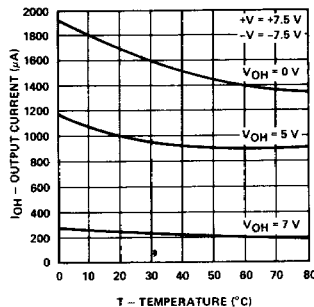### Digital Output Low Current vs Temperature DF331A

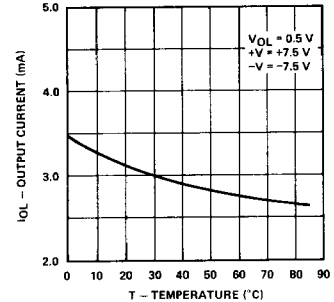### Digital Output Low Voltage vs Temperature DF331A

Positive and Negative Supply Current vs Temperature DF332A, DF334A

A/B Signaling Output Current vs V_{OH} and Temperature DF332A Only
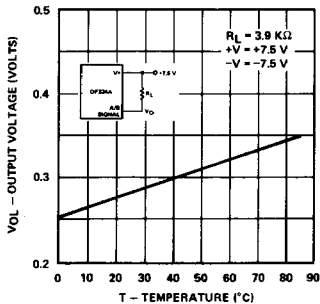

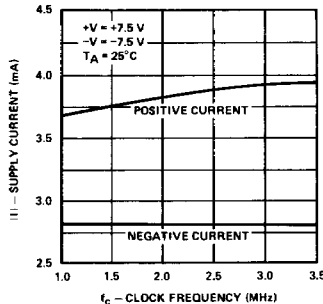### A/B Signaling Digital Output Low Current vs Temperature DF334A
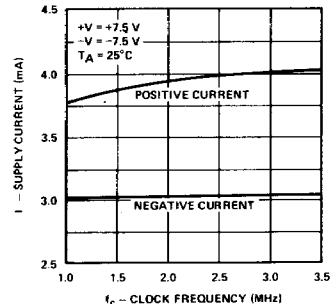
TYPICAL CHARACTERISTICS (Cont'd)

A/B Signaling Digital Output Low Voltage vs Temperature DF334A

Positive and Negative Supply Current vs Clock Frequency DF331A
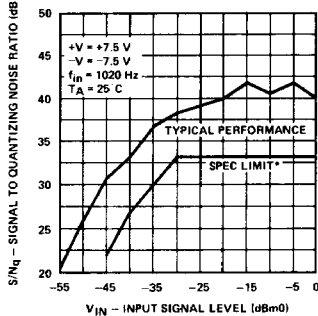
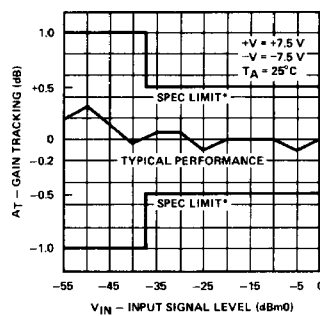**Positive and Negative Supply Current vs Clock Frequency DF332A, DF334A**

Signal to Quantizing Noise Ratio vs Input Level DF331A/DF332A or DF331A/DF334A Pair

Gain Tracking vs Input Level DF331A/DF332A or DF331A/DF334A Pair

*SPECIFICATION LIMITS FROM A.T.T. CHANNEL BANK D-3 SPEC

APPLICATIONS INFORMATION

Positive and negative voltage references should be bypassed to analog ground with a 10 μF capacitor to supply the peak currents required (up to 2 mA) during sampling. Inadequate bypassing may cause sampling inaccuracy and crosstalk between adjacent channels. The absolute value of the voltage references should match and track each other to prevent asymmetry in the analog waveforms. The recommended reference value is ±3.0 V. Increasing this level may increase harmonic distortion in the CODEC, while decreasing the references will lower the system dynamic range.

The sync pulses to the decoder and encoder should be staggered as in Figure 6. The sync to the decoder precedes the sync to the encoder by one half of a clock period to allow for the delay times which can occur if the sync pulse is derived from the clock. If all syncs and clocks are coincident without delay, then the staggering is unnecessary.

All digital inputs will work when driven from TTL logic providing that the outputs of the TTL gates are pulled up to the 5.0 V TTL supply.

The sample rate of the CODEC is determined by the clock rate and the period between sync pulses. The minimum period between sync pulses is 168 clock periods, which is the time that the encoder requires to complete an analog-to-digital conversion (see Figure 6). The maximum clock rate for a functional system is 3.0 MHz. The actual sample rate of the CODEC is equal to the inverse of the period between sync pulses.
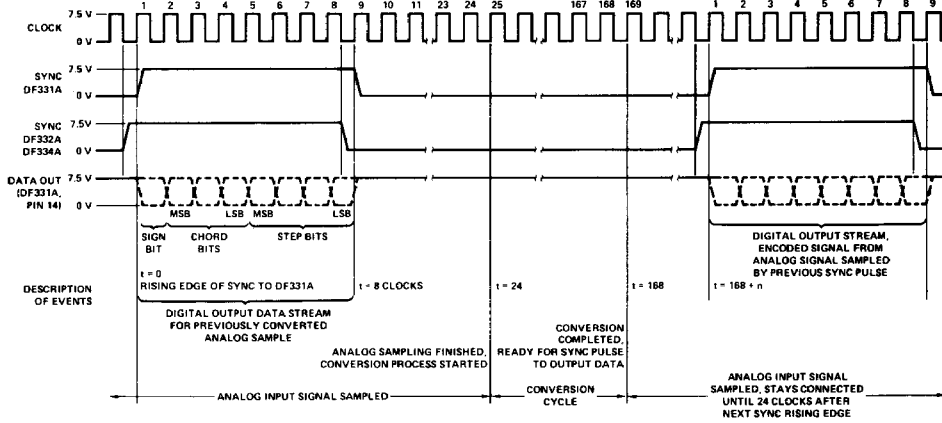
Zero code suppression is included in the A/D conversion to prevent the transmission of an all zeroes digital output code, which could cause a repeater to go down in a telecommunications system. Should an all zeroes code result from the A/D conversion (indicating a negative overvoltage condition), then bit 7 in the data stream is forced to a logic "1".

Open drain signaling outputs on the decoder allow easy interface to logic. The open drain P-channel of the DF332A allows a pull-down to ground or a negative voltage ($V_O \geqslant$ −7.5 V absolute max) giving logic compatibility with CMOS or other MOS logic. The open drain N-channel of the DF334A allows a pull-up to a positive supply (e.g., +5 V for TTL or up to +12 V for CMOS). This output has logic low level near ground making it compatible with TTL or CMOS logic.
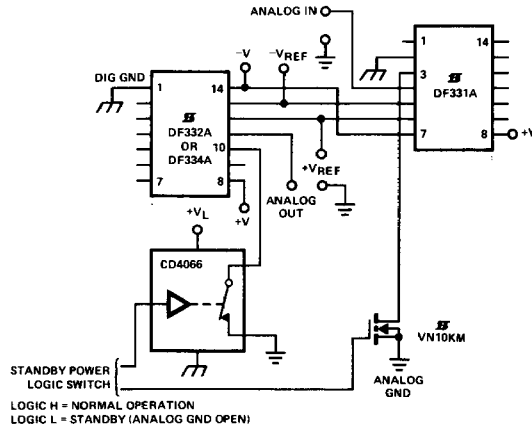
APPLICATIONS INFORMATION

The CODECs can be put into a lower power standby condition. For standby, analog ground lines are open circuited. Relays or FET switches can be used. Figure 7 shows one implementation for standby switching. For the encoder (DF331A) the switch must be low $R_{DS(ON)}$

($<25\ \Omega$) and have very low total offset voltage (<5 mV at 200 μA current). The VMOS switch shown (VN10KM) achieves these requirements. The decoder is not as critical, offset voltage should be minimized (<50 mV); use of a CD4066 CMOS switch is satisfactory.

CODEC Timing Relationships
Figure 6

Coder/Decoder Circuit with Switches
for Standby Power Condition
Figure 7

APPLICATIONS

Typical Coder/Decoder Circuit Configurations

Transmit Section

Receive Section

−V = −7.5 V
+V = +7.5 V
−V$_{REF}$ = −3.0 V
+V$_{REF}$ = +3.0 V
V$_I$ = AS REQUIRED FOR INTERFACING
CK = 1.544 MHz
SYNC = 8 kHz (PER DATA SHEET)