National Semiconductor

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DP8224 Clock Generator and Driver

General Description

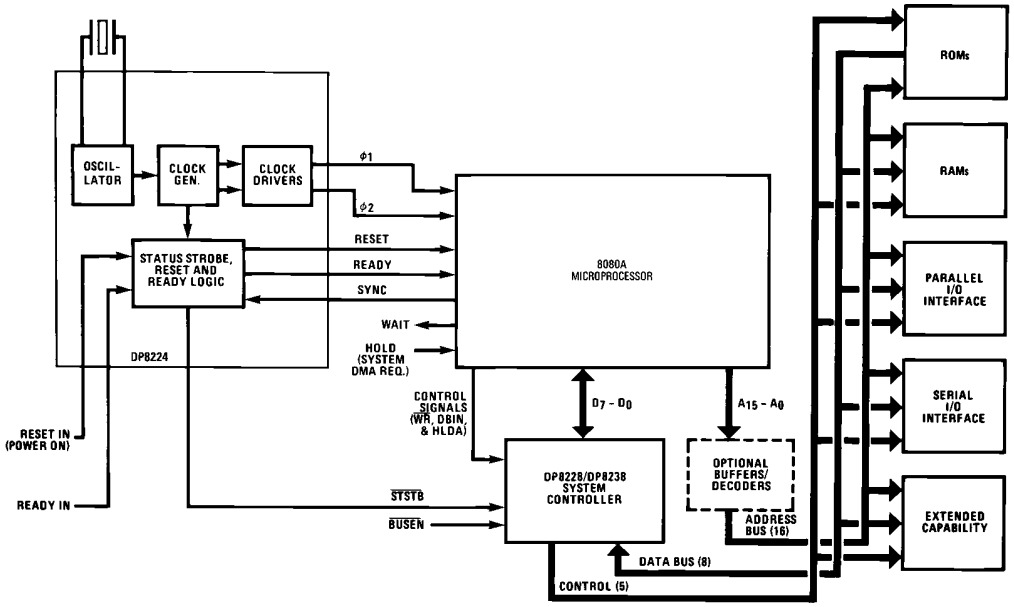
The DP8224 is a clock generator/driver contained in a standard, 16-pin dual-in-line package. The chip, which is fabricated using Schottky Bipolar technology, generates clocks and timing for the 8080A microcomputer family.

Included in the DP8224 is an oscillator circuit that is controlled by an external crystal, which is selected by the designer to meet a variety of system speed requirements. Also included in the chip are circuits that provide: a status strobe for the DP8228 or DP8238 system controllers, power-on reset for the 8080A microprocessor, and synchronization of the READY input to the 8080A.

Features

- Crystal-controlled oscillator for stable system operation
- Single chip clock generator and driver for 8080A microprocessor
- Provides status strobe for DP8228 or DP8238 system controllers
- Provides power-on reset for 8080A microprocessor
- Synchronizes READY input to 8080A microprocessor
- Provides oscillator output for synchronization of external circuits
- Reduces system component count

8080A Microcomputer Family Block Diagram



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RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	
V_{CC}	7V
V_{DD}	15V
Input Voltage	−1V to +5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temperature (Soldering, 4 seconds)	260°C

* Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage			
V_{CC}	4.75	5.25	V
V_{DD}	11.4	12.6	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_F	Input Current Loading	V_F = 0.45V			−0.25	mA
I_R	Input Leakage Current	V_R = 5.25V			10	μA
V_C	Input Forward Clamp Voltage	I_C = −5 mA			−1.0	V
V_{IL}	Input "Low" Voltage	V_{CC} = 5V			0.8	V
V_{IH}	Input "High" Voltage	$\overline{RESIN}$ Input	2.6			V
		All Other Inputs	2.0			V
$V_{IH}-V_{IL}$	$\overline{RESIN}$ Input Hysteresis	V_{CC} = 5V	0.25			V
V_{OL}	Output "Low" Voltage					
	(ϕ1, ϕ2), Ready, Reset $\overline{STSTB}$	I_{OL} = 2.5 mA			0.45	V
	Osc., ϕ2 (TTL)	I_{OL} = 10 mA			0.45	V
	Osc., ϕ2 (TTL)	I_{OL} = 15 mA			0.45	V
V_{OH}	Output "High" Voltage					
	ϕ1, ϕ2	I_{OH} = −100 μA	9.4			V
	Ready, Reset	I_{OH} = −100 μA	3.6			V
	Osc., ϕ2 (TTL), $\overline{STSTB}$	I_{OH} = −1 mA	2.4			V
I_{SC}	Output Short-Circuit Current (All Low Voltage Outputs Only), (Note 1)	V_O = 0V, V_{CC} = 5V	−10		−60	mA
I_{CC}	Power Supply Current				115	mA
I_{DD}	Power Supply Current				12	mA

Note 1: Caution −ϕ1 and ϕ2 output drivers do not have short circuit protection.

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 3: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DP8224. All typical values are for T_A = 25°C, V_{CC} = 5V, and V_{DD} = 12V.

Crystal Requirements*

Tolerance	0.005% at 0°C to +70°C	Equivalent Resistance	75Ω to 20Ω
Resonance	Fundamental	Power Dissipation (Min)	4 mW
Load Capacitance	20 pF to 30 pF		

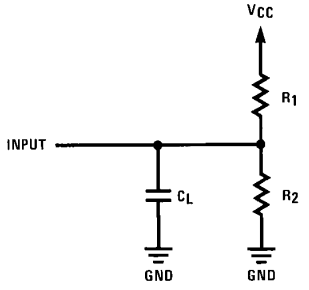
*It is good design practice to ground the case of the crystal

**With tank circuit, use 3rd overtone mode

Switching Characteristics (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{\phi 1}$	$\phi 1$ Pulse Width	$C_L = 20$ pF to 50 pF	$\frac{2t_{CY}}{9} - 20$			ns
$t_{\phi 2}$	$\phi 2$ Pulse Width		$\frac{5t_{CY}}{9} - 35$			ns
t_{D1}	$\phi 1$ to $\phi 2$ Delay		0			ns
t_{D2}	$\phi 2$ to $\phi 1$ Delay		$\frac{2t_{CY}}{9} - 14$			ns
t_{D3}	$\phi 1$ to $\phi 2$ Delay		$\frac{2t_{CY}}{9}$		$\frac{2t_{CY}}{9} + 20$	ns
t_r	$\phi 1$ and $\phi 2$ Rise Time				20	ns
t_f	$\phi 1$ and $\phi 2$ Fall Time				20	ns
$t_{D\phi 2}$	$\phi 2$ to $\phi 2$ (TTL) Delay	$\phi 2$ TTL, $C_L = 30$ pF, $R1 = 300\Omega$, $R2 = 600\Omega$	-5		15	ns
t_{DSS}	$\phi 2$ to $\overline{STSTB}$ Delay	$\overline{STSTB}$, $C_L = 15$ pF $R1 = 2\ k\Omega$, $R2 = 4\ k\Omega$	$\frac{6t_{CY}}{9} - 30$		$\frac{6t_{CY}}{9}$	ns
t_{PW}	$\overline{STSTB}$ Pulse Width		$\frac{t_{CY}}{9} - 15$			ns
t_{DRS}	RDYIN Set-Up Time to Status Strobe		$50 - \frac{4t_{CY}}{9}$			ns
t_{DRH}	RDYIN Hold Time After $\overline{STSTB}$		$\frac{4t_{CY}}{9}$			ns
t_{DR}	READY or RESET to $\phi 2$ Delay	Ready and Reset, $C_L = 10$ pF, $R1 = 2\ k\Omega$, $R2 = 4\ k\Omega$	$\frac{4t_{CY}}{9} - 25$			ns
t_{CLK}	CLK Period			$\frac{t_{CY}}{9}$		ns
f_{MAX}	Maximum Oscillating Frequency		27			MHz
C_{IN}	Input Capacitance	$V_{CC} = 5V$, $V_{DD} = 12V$, $V_{BIAS} = 2.5V$, f = 1 MHz			8	pF

Test Circuit



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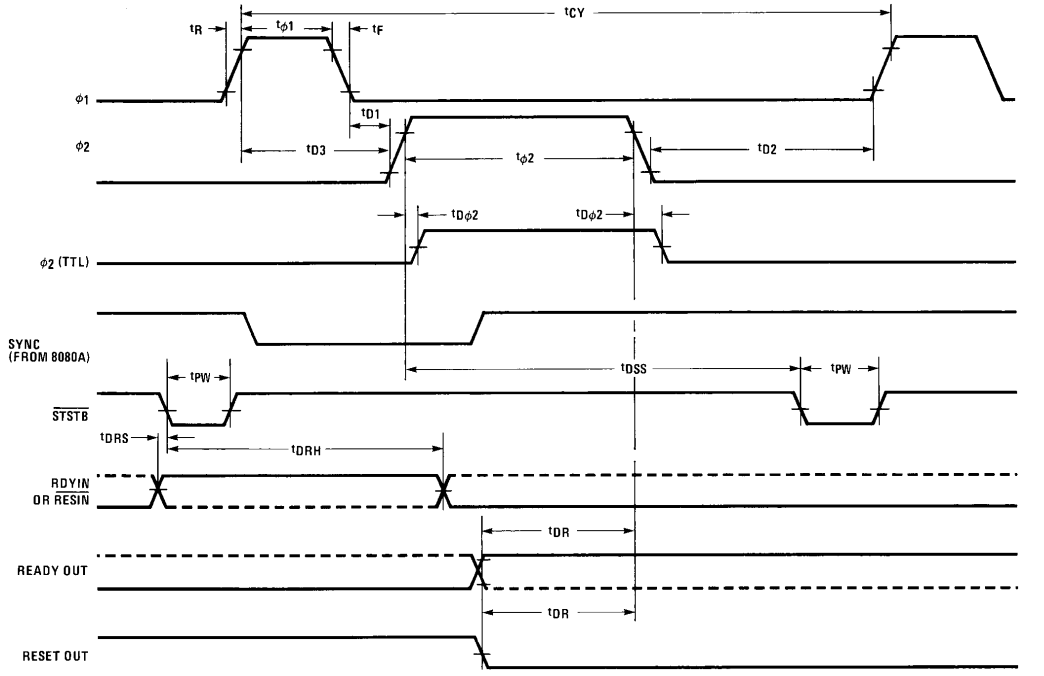
Waveforms



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Voltage Measurement Points: $\phi 1$, $\phi 2$ Logic "0" = 1.0V, Logic "1" = 8.0V. All other signals measured at 1.5V.

Switching Characteristics (For t_{CY} = 488.28 ns)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{\phi 1}$	$\phi 1$ Pulse Width	$\phi 1$ and $\phi 2$ Loaded to C_L = 20 to 50 pF Ready and Reset Loaded to 2 mA/10 pF All Measurements Referenced to 1.5V unless Specified Otherwise	89			ns
$t_{\phi 2}$	$\phi 2$ Pulse Width		236			ns
t_{D1}	Delay $\phi 1$ to $\phi 2$		0			ns
t_{D2}	Delay $\phi 2$ to $\phi 1$		95			ns
t_{D3}	Delay $\phi 1$ to $\phi 2$ Leading Edges		109		129	ns
t_r	Output Rise Time				20	ns
t_f	Output Fall Time				20	ns
t_{DSS}	$\phi 2$ to $\overline{STSTB}$ Delay		296		326	ns
$t_{D\phi 2}$	$\phi 2$ to $\phi 2$ (TTL) Delay		−5		15	ns
t_{PW}	Status Strobe Pulse Width		40			ns
t_{DRS}	RDYIN Set-Up Time to $\overline{STSTB}$		−167			ns
t_{DRH}	RDYIN Hold Time after $\overline{STSTB}$		217			ns
t_{DR}	READY or RESET to $\phi 2$ Delay		192			ns
f_{MAX}	Oscillator Frequency				18.432	MHz

Functional Pin Definitions

The following describes the function of all of the DP8224 input/output pins. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Crystal Connections (XTAL 1 and XTAL 2): Two inputs that connect an external crystal to the oscillator circuit of the DP8224. Normally, a fundamental mode crystal is used to determine the basic operating frequency of the oscillator. However, overtone mode crystals may also be used. The crystal frequency is 9 times the desired microprocessor speed (that is, crystal frequency equals $1/t_{CY} \times 9$). When the crystal frequency is above 10 MHz, a selected capacitor (3 to 10 pF) may have to be connected in series with the crystal to produce the exact desired frequency. *Figure A*.

Tank: Allows the use of overtone mode crystals with the oscillator circuit. When an overtone mode crystal is used, the tank input connects to a parallel LC network that is ac coupled to ground. The formula for determining the resonant frequency of this LC network is as follows:

$$F = \frac{1}{2\pi\sqrt{LC}}$$

Synchronizing (SYNC) Signal: When high, indicates the beginning of a new machine cycle. The 8080A microprocessor outputs a status word (which describes the current machine cycle) onto its data bus during the first state (SYNC interval) of each machine cycle.

Reset In ($\overline{\text{RESIN}}$): Provides an automatic system reset and start-up upon application of power as follows. The $\overline{\text{RESIN}}$ input, which is obtained from the junction of an external RC network that is connected between V_{CC} and ground, is routed to an internal Schmitt Trigger circuit. This circuit converts the slow transition of the power supply rise into a sharp, clean edge when its input reaches a predetermined value. When this occurs, an internal D-type flip-flop is synchronously reset, thereby providing the RESET output signal discussed below.

For manual system reset, a momentary contact switch that provides a low (ground) when closed is also connected to the $\overline{\text{RESIN}}$ input.

Ready In (RDYIN): An asynchronous READY signal that is re-clocked by a D-type flip-flop of the DP8224 to provide the synchronous READY output discussed below.

+5 Volts: V_{CC} supply.

+12 Volts: V_{DD} supply.

Ground: 0 volt reference.

OUTPUT SIGNALS

Oscillator (OSC): A buffered oscillator signal that can be used for external timing purposes.

ϕ_1 and ϕ_2 Clocks: Two non-TTL compatible clock phases that provide nonoverlapping timing references for internal storage elements and logic circuits of the 8080A microprocessor. The two clock phases are produced by an internal clock generator that consists of a divide-by-nine counter and the associated decode gating logic. *Figure B*.

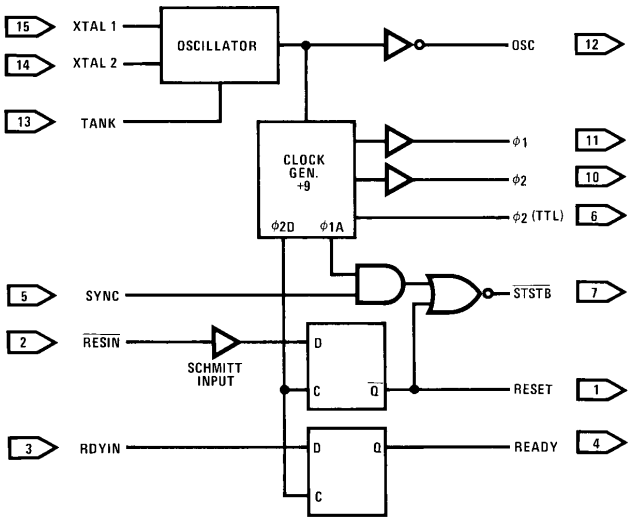
ϕ_2 (TTL) Clock: A TTL ϕ_2 clock phase that can be used for external timing purposes.

Status Strobe ($\overline{\text{STSTB}}$): Activated (low) at the start of each new machine cycle. The $\overline{\text{STSTB}}$ signal is generated by gating a high-level SYNC input with the ϕ_{1A} timing signal from the internal clock generator of the DP8224. The $\overline{\text{STSTB}}$ signal is used to clock status information into the status latch of the DP8228 system controller and bus driver.

Reset: When the RESET signal is activated, the content of the program counter of the 8080A is cleared. After RESET, the program will start at location 0 in memory.

Ready: The READY signal indicates to the 8080A that valid memory or input data is available. This signal is used to synchronize the 8080A with slower memory or input/output devices.

Logic and Connection Diagrams



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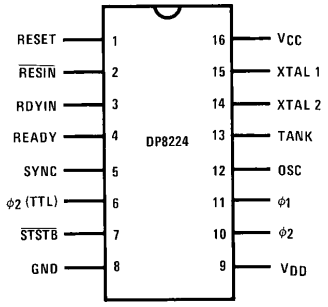
Dual-In-Line Package



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Top View

Order Number DP8224J or DP8224N
See NS Package Number
J16A or N16A

Applications Information

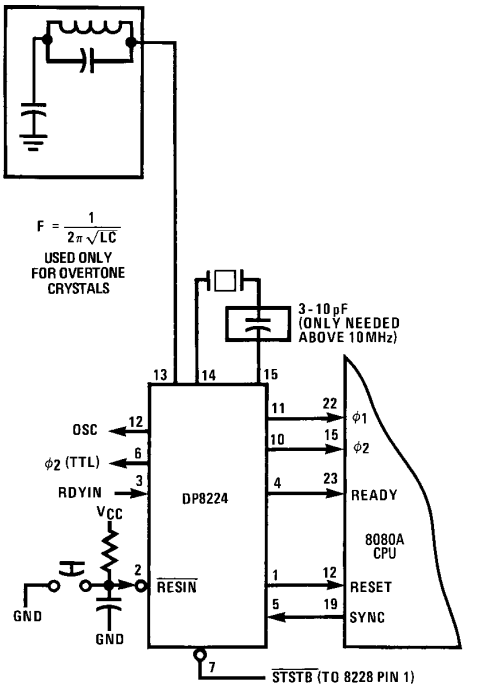

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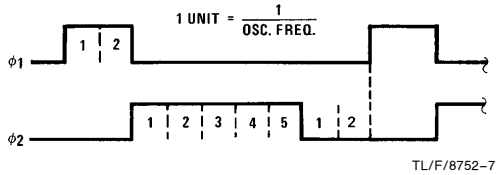
FIGURE A. DP8224 Connection Diagram



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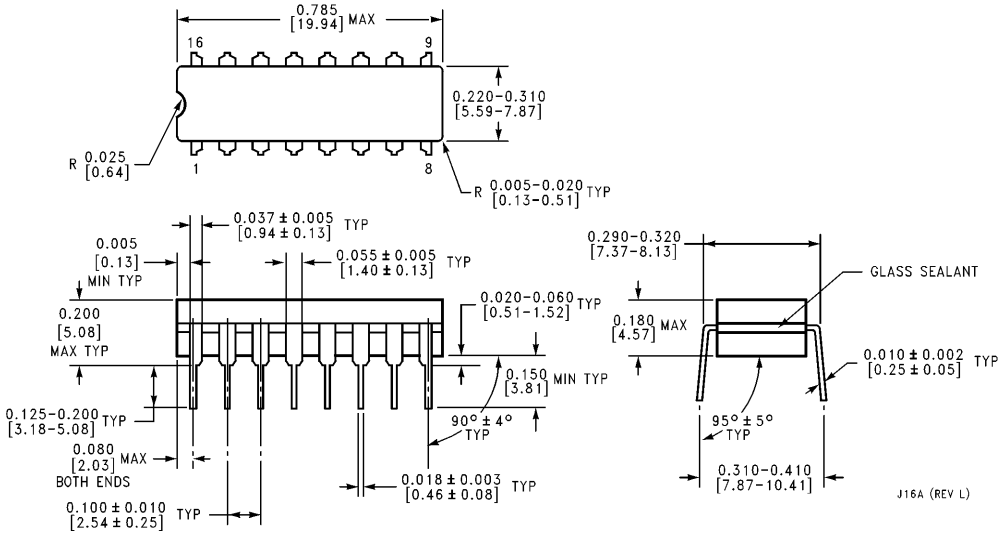
EXAMPLE: (8080 t_{CY} = 500 ns)
OSC = 18 MHz/55 ns
ϕ_1 = 110 ns (2 × 55 ns)
ϕ_2 = 275 ns (5 × 55 ns)
$\phi_2-\phi_1$ = 110 ns (2 × 55 ns)

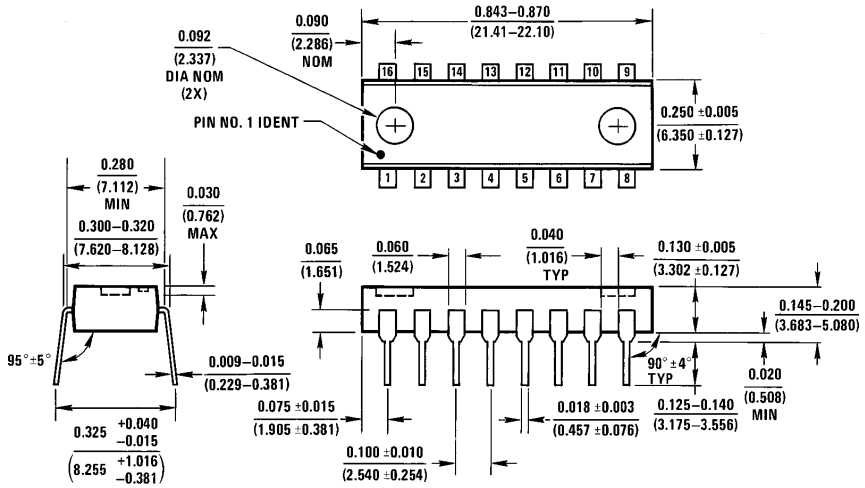
FIGURE B. DP8224 Clock Generator Waveforms

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number DP8224J
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)



N16A (REV E)

Molded Dual-In-Line Package (N)
Order Number DP8224N
NS Package Number N16A

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