

## Low Power Windowed Watchdog with Reset, Sleep Mode Functions

### Description

The EM6151 offers a high level of integration by combining voltage monitoring and software monitoring using a windowed watchdog.

A comparator monitors the voltage applied at the  $V_{IN}$  input comparing it with an internal voltage reference  $V_{REF}$ . The power-on reset function is initialized after  $V_{IN}$  reaches  $V_{REF}$  and takes the reset output inactive after a delay  $T_{POR}$  depending on external resistance  $R_{OSC}$ . The reset output goes active low when the  $V_{IN}$  voltage is less than  $V_{REF}$ . The  $\overline{RES}$  and  $\overline{EN}$  outputs are guaranteed to be in a correct state for a supply voltage as low as 1.2 V. The watchdog function monitors software cycle time and execution.

If software clears the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution) it will cause the system to be reset. For enhanced security, the watchdog must be serviced within an "open" time window. During the remaining time, the watchdog time window is "closed" and a reset will occur should a  $\overline{TCL}$  pulse be received by the watchdog during this "closed" time window. The ratio of the open/closed window is either 33%/67% or 67%/33%.

The system ENABLE output prevents critical control functions being activated until software has successfully cleared the watchdog three times. Such a security could be used to prevent motor controls being energized on repeated resets of a faulty system.

When the microcontroller goes in stand-by mode or stops working, no signal is received on the  $\overline{TCL}$  input of the EM6151 (version 55) and it goes into a stand-by mode in order to save power (CAN-bus sleep detector).

### Features

- Low quiescent current 35  $\mu$ A
- 40°C to +125°C temperature range
- Windowed watchdog with an adjustable time windows, guaranteeing a minimum time and a maximum time between software clearing of the watchdog
- Time base accuracy  $\pm 8\%$  (at 100ms)
- Voltage reference accuracy  $\pm 3\%$
- Sleep mode function (V55)
- Adjustable threshold voltage using external resistors
- Adjustable power on reset (POR) delay using one external resistor
- Open-drain active-low RESET output
- Reset output guaranteed for regulated output voltage down to 1.2 V
- System ENABLE output offers added security
- Qualified according to AEC-Q100
- Green SO-8 package (RoHS compliant)

### Applications

- Automotive systems
- Industrial
- Home security systems
- Telecom / Networking
- Computers
- Set top boxes

### Typical Operating Configuration

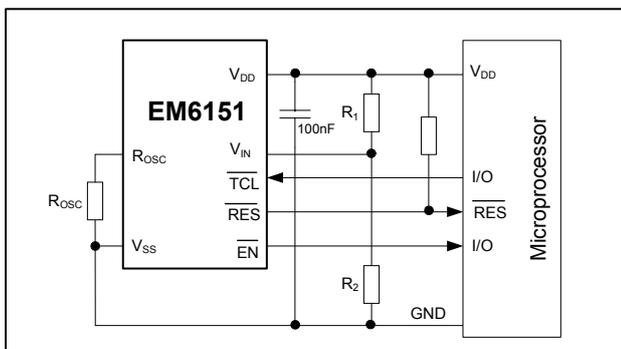


Fig. 1

### Selection Table

Part Number	$V_{REF}$	Closed Window	Open Window	CAN-bus sleep detector
EM6151V30	1.17 V	67%	33%	No
EM6151V50	1.52 V	67%	33%	No
EM6151V53	1.52 V	33%	67%	No
EM6151V55	1.275 V	67%	33%	Yes

Please refer to Fig. 4 for more information about the open/closed window of the watchdog.

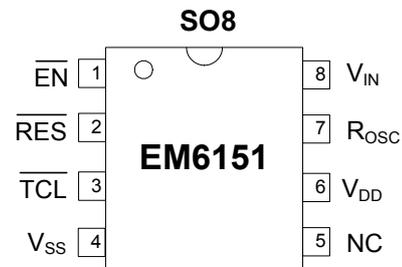
## Ordering Information

Part Number	Version	V <sub>REF</sub>	Package	Delivery Form	Package Marking
EM6151V30SO8A+ EM6151V30SO8B+	V30	1.17 V	SO-8	Stick, 97 pcs Tape & Reel, 2500 pcs	6151030
EM6151V50SO8A+ EM6151V50SO8B+	V50	1.52 V	SO-8	Stick, 97 pcs Tape & Reel, 2500 pcs	6151050
EM6151V53SO8A+ EM6151V53SO8B+	V53	1.52 V	SO-8	Stick, 97 pcs Tape & Reel, 2500 pcs	6151053
EM6151V55SO8A+ EM6151V55SO8B+	V55	1.275 V	SO-8	Stick, 97 pcs Tape & Reel, 2500 pcs	6151055

**Note:** the “+” symbol at the end of the part number means that this product is RoHS compliant (green). For version V30, please contact EM Microelectronic.

## Pin Assignment and Description

SO8	Name	Function
1	$\overline{\text{EN}}$	Push-pull active low enable output
2	$\overline{\text{RES}}$	Open drain active low reset output. $\overline{\text{RES}}$ must be pulled up to V <sub>DD</sub> even if unused
3	$\overline{\text{TCL}}$	Watchdog timer clear input signal
4	V <sub>SS</sub>	GND terminal
5	NC	No connect
6	V <sub>DD</sub>	Supply voltage
7	R <sub>OSC</sub>	R <sub>OSC</sub> input for RC oscillator tuning
8	V <sub>IN</sub>	Voltage comparator input



## Block Diagram EM6151

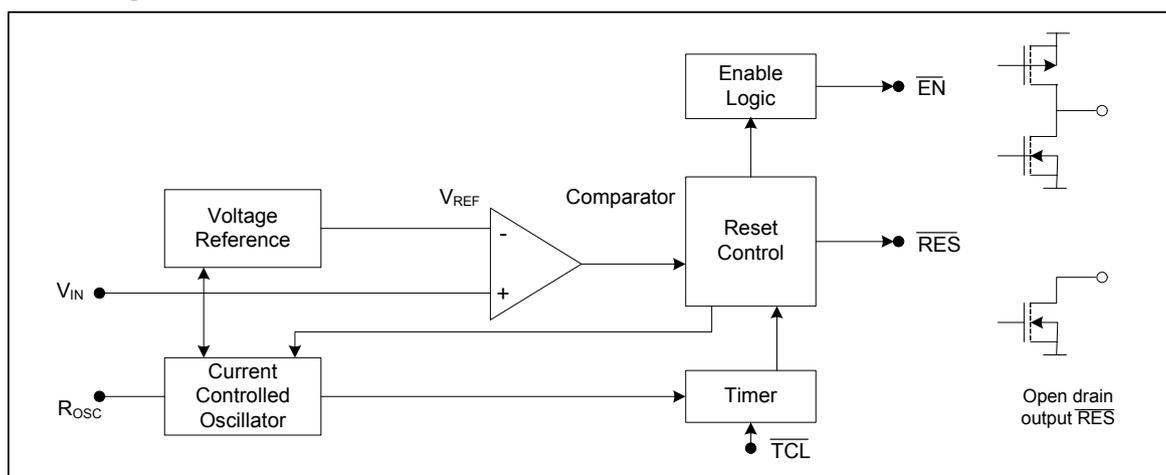


Fig. 2

## Absolute Maximum Ratings

Parameter	Symbol	Conditions
Max. voltage at $V_{DD}$	$V_{DDMAX}$	$V_{SS} + 7.0V$
Max. voltage at any signal pin	$V_{MAX}$	$V_{DD} + 0.3V$
Min. voltage at any signal pin	$V_{MIN}$	$V_{SS} - 0.3V$
Storage temperature	$T_{STO}$	-65 to +150 °C
ESD According to MIL-STD-883C method 3015.7	$V_{Smax}$	2000V

Table 1

Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

## Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, it is advised that normal precautions be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. At any time, all inputs must be tied to a defined logic voltage level.

## Electrical Characteristics

$V_{DD} = 5.0V$ ,  $T_j = -40$  to  $+125^\circ C$ , unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply current	$I_{DD}$	$R_{OSC} = 100k\Omega$ $V_{IN}$ and $\overline{TCL} = V_{DD}$ , $O/P_S$ $1M\Omega$ to $V_{DD}$		35	60	$\mu A$
Supply current in standby mode and sleep mode for V55	$I_{DD}$	$R_{OSC} = \text{don't care}$ , $\overline{TCL} = V_{DD}$ , $V_{IN} = 0V$		25	50	$\mu A$
<b>RES and EN</b> Output Low Voltage	$V_{OL}$	$V_{DD} = 4.5V$ , $I_{OL} = 8mA$		0.25	0.45	V
		$V_{DD} = 2.0V$ , $I_{OL} = 4mA$		0.2	0.4	V
		$V_{DD} = 1.2V$ , $I_{OL} = 0.5mA$		0.04	0.2	V
<b>EN</b> Output High Voltage	$V_{OH}$	$V_{DD} = 4.5V$ , $I_{OH} = -1mA$	3.5	4.1		V
		$V_{DD} = 2.0V$ , $I_{OH} = -100\mu A$	1.8	1.9		V
		$V_{DD} = 1.2V$ , $I_{OH} = -20\mu A$	0.9	1.05		V
TCL Input Low Level	$V_{IL}$		$V_{SS}$		0.5	V
TCL Input High Level	$V_{IH}$		2.5		$V_{DD}$	V
Leakage current	$I_{LI}$	$V_{SS} \leq V_{TCL} \leq V_{DD}$		0.05		$\mu A$
Comparator reference (note 2)	$V_{REF}$	Version V30 (replaces V6130)	1.135	1.170	1.205	V
		Version V50 (replaces V6150)	1.475	1.520	1.565	V
		Version V53	1.475	1.520	1.565	V
		Version V55 (replaces V6155)	1.235	1.275	1.315	V
Comparator hysteresis (note 2)	$V_{HY}$			2		mV
$V_{IN}$ input resistance	$R_{VIN}$			100		$M\Omega$

Table 3

**Note 1:**  $\overline{RES}$  must be pulled up externally to  $V_{DD}$  even if it is unused. ( $\overline{RES}$  and  $\overline{EN}$  are used as inputs by EM test)

**Note 2:** the comparator reference is the power-down reset threshold. The power-on reset threshold equals the comparator reference voltage plus the comparator hysteresis (see Fig. 5).

## Timing Characteristics

$V_{DD} = 5.0\text{ V}$ ,  $T_j = -40$  to  $+125\text{ }^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Propagation delay $\overline{\text{TCL}}$ to Output Pins	$T_{DIDO}$			250	500	ns
$V_{IN}$ sensitivity	$T_{SEN}$	$V_{INhigh}=1.1 \times V_{REF}$ , $V_{INlow}=0.9 \times V_{REF}$	1	5	20	$\mu\text{s}$
Watchdog Reset Pulse Period	$T_{WDRP}$	$\overline{\text{TCL}}$ inactive	$T_{CW} + T_{OW} + T_{WDR}$			ms
<b>Version V30</b>						
Power-on Reset delay	$T_{POR}$	$R_{OSC} = 116.9\text{ k}\Omega \pm 1\%$	91.6	100	108.3	ms
Closed Window Time	$T_{CW}$		74	80	85.76	
Open Window Time	$T_{OW}$		37	40	42.88	
Watchdog Time	$T_{WD}$		92.5	100	107.2	
Watchdog Reset Pulse Width if no $\overline{\text{TCL}}$	$T_{WDR}$		2.25	2.5	2.75	
<b>Version V50</b>						
Power-on Reset delay	$T_{POR}$	$R_{OSC} = 121.6\text{ k}\Omega \pm 1\%$	91.6	100	108.3	ms
Closed Window Time	$T_{CW}$		74	80	85.76	
Open Window Time	$T_{OW}$		37	40	42.88	
Watchdog Time	$T_{WD}$		92.5	100	107.2	
Watchdog Reset Pulse Width if no $\overline{\text{TCL}}$	$T_{WDR}$		2.25	2.5	2.75	
<b>Version V53</b>						
Power-on Reset delay	$T_{POR}$	$R_{OSC} = 23.2\text{ k}\Omega \pm 1\%$	4.57	5.0	5.44	ms
Closed Window Time	$T_{CW}$		9.24	10	10.77	
Open Window Time	$T_{OW}$		18.48	20	21.54	
Watchdog Time	$T_{WD}$		18.48	20	21.54	
Watchdog Reset Pulse Width if no $\overline{\text{TCL}}$	$T_{WDR}$		0.56	0.625	0.69	
<b>Version V55</b>						
Power-on Reset delay	$T_{POR}$	$R_{OSC} = 107.5\text{ k}\Omega \pm 1\%$	91.6	100	108.3	ms
Closed Window Time	$T_{CW}$		74	80	85.76	
Open Window Time	$T_{OW}$		37	40	42.88	
Watchdog Time	$T_{WD}$		92.5	100	107.2	
Watchdog Reset Pulse Width if no $\overline{\text{TCL}}$	$T_{WDR}$		2.25	2.5	2.75	
Watchdog Reset Pulse Width in Sleep Mode	$T_{WDRS}$	$R_{OSC}$ off; $R_{INT}=1\text{M}\Omega$	2.8	3.2	3.6	
Watchdog Reset Pulse Period in Sleep Mode	$T_{WDRPS}$	$\overline{\text{TCL}}$ inactive	750	1100	1450	

Table 4

For different values of  $T_{WD}$  and  $R_{OSC}$ , see figures 9 to 12.

## Timing Waveforms

### Watchdog Timeout Period

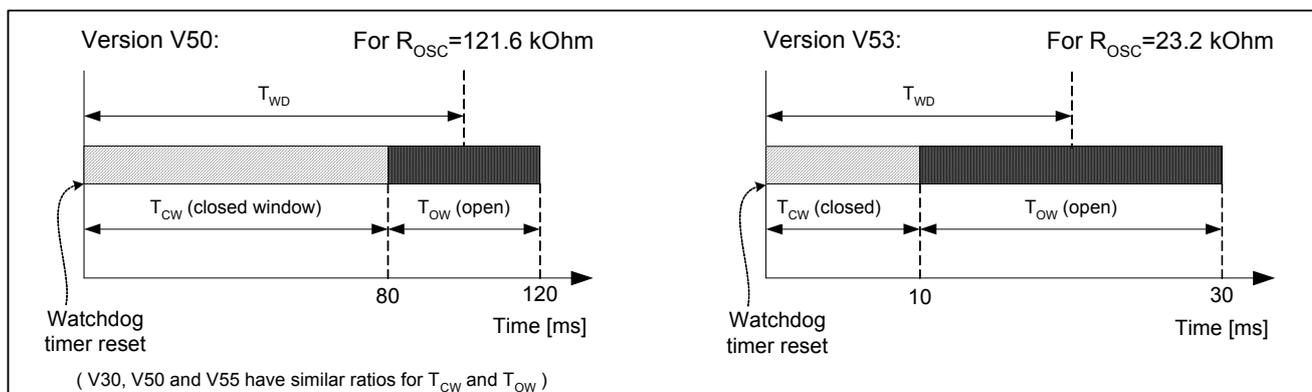


Fig. 4

## Voltage Monitoring

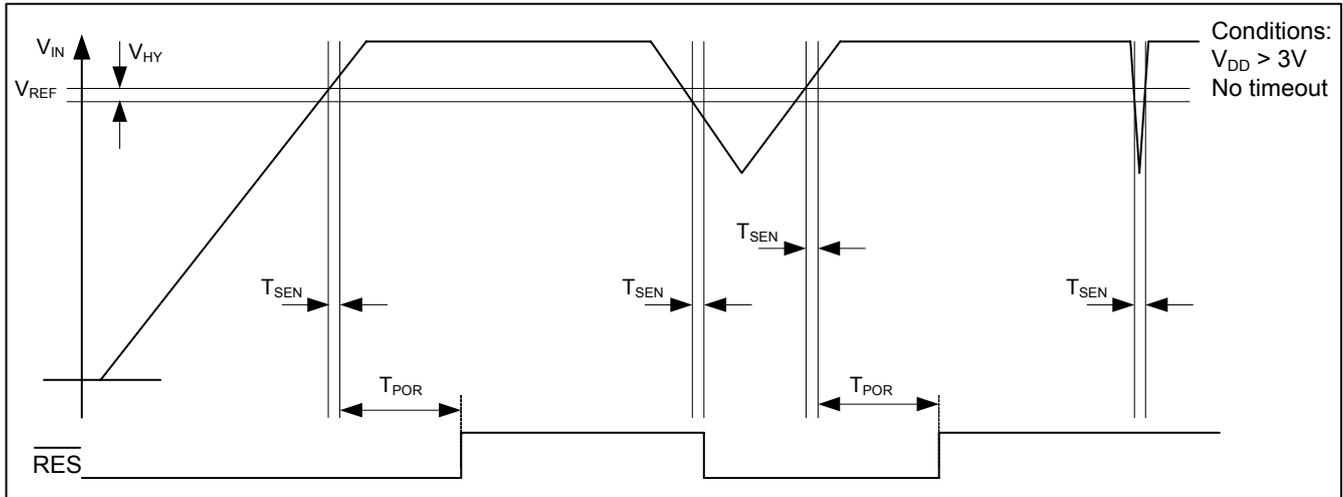


Fig. 5

## Timer Reaction

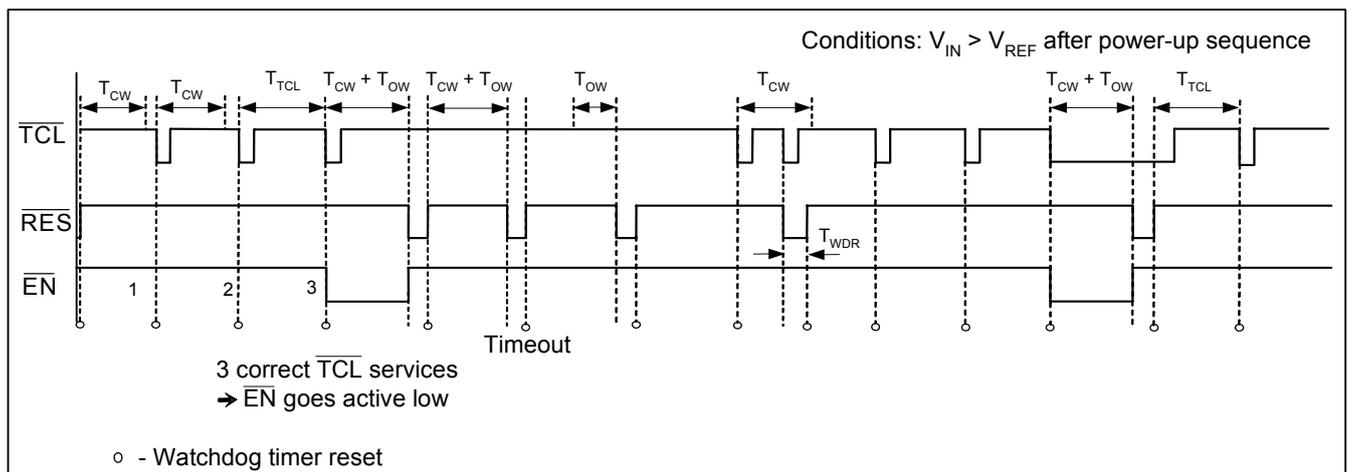


Fig. 6

## Combined Voltage and Timer Reaction

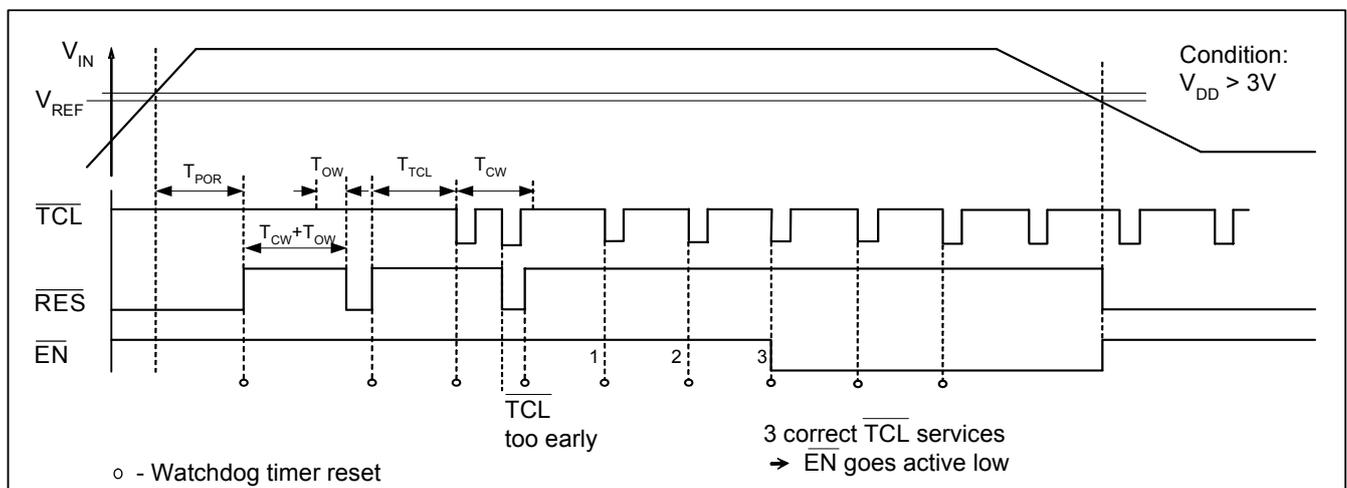


Fig. 7

## Functional Description

### V<sub>IN</sub> Monitoring

The power-on reset and the power-down reset are generated as a response to the external voltage level applied on the V<sub>IN</sub> input. The threshold voltage at which reset is asserted or released (V<sub>RESET</sub>) is determined by the external voltage divider between V<sub>DD</sub> and V<sub>SS</sub>, as shown on Fig. 8. A part of V<sub>DD</sub> is compared to the internal voltage reference. To determine the values of the divider, the leakage current at V<sub>IN</sub> must be taken into account as well as the current consumption of the divider itself. Low resistor values will need more current, but high resistor values will make the reset threshold less accurate at high temperature, due to a possible leakage current at the V<sub>IN</sub> input. The sum of the two resistors (R<sub>1</sub> + R<sub>2</sub>) should stay below 500 kΩ. The formula is:

$$V_{\text{RESET}} = V_{\text{REF}} \times (1 + R_1/R_2).$$

Example: choosing R<sub>1</sub> = 200 kΩ and R<sub>2</sub> = 100 kΩ gives V<sub>RESET</sub> = 4.56 V (typical) for version V50 and V53.

At power-up the reset output ( $\overline{\text{RES}}$ ) is held low (see Fig. 5). When V<sub>IN</sub> becomes greater than V<sub>REF</sub>, the  $\overline{\text{RES}}$  output is held low for an additional power-on-reset (POR) delay T<sub>POR</sub> (defined with the external resistor connected at R<sub>OSC</sub> pin). The T<sub>POR</sub> delay prevents repeated toggling of  $\overline{\text{RES}}$  even if V<sub>DD</sub> voltage drops out and recovers. The T<sub>POR</sub> delay allows the microprocessor's crystal oscillator time to start and stabilize and ensures correct recognition of the reset signal to the microprocessor.

The  $\overline{\text{RES}}$  output goes active low generating the power-down reset whenever V<sub>IN</sub> falls below V<sub>REF</sub>. The sensitivity or reaction time of the internal comparator to the voltage level on V<sub>IN</sub> is typically 3 μs.

### Timer Programming

The on-chip oscillator allows the user to adjust the power-on reset (POR) delay T<sub>POR</sub> and the watchdog time T<sub>WD</sub> by changing the resistor value of the external resistor R<sub>OSC</sub> connected between the pin R<sub>OSC</sub> and V<sub>SS</sub> (see Fig. 8). The closed and open window times (T<sub>CW</sub> and T<sub>OW</sub>) as well as the watchdog reset pulse width (T<sub>WDR</sub>), which are T<sub>TCL</sub> dependent, will vary accordingly. The watchdog time T<sub>WD</sub> can be obtained with figures 9 to 12 or with the Excel application EM6151ResCalc.xls available on EM website. T<sub>POR</sub> is equal to T<sub>WD</sub> with the minimum and maximum tolerances increased by 1% (For Version 53, T<sub>POR</sub> is one fourth of T<sub>WD</sub>).

Note that the current consumption increases as the frequency increases.

### CAN-Bus Sleep Mode Detector (version 55)

When the microcontroller goes into a standby mode, it implies that it does not send any pulses on the  $\overline{\text{TCL}}$  input of the EM6151. After three reset pulse periods (T<sub>CW</sub> + T<sub>OW</sub> + T<sub>WDR</sub>) on the  $\overline{\text{RES}}$  output, the circuit switches on an internal resistor of 1 MΩ, and it will have a reset pulse of typically 3 ms every 1 second on the  $\overline{\text{RES}}$  output. When a  $\overline{\text{TCL}}$  edge (rising or falling) appears on the  $\overline{\text{TCL}}$  input or the power supply goes down and up, the circuit switches to the R<sub>OSC</sub>.

### Watchdog Timeout Period Description

The watchdog timeout period is divided into two periods, a closed window period (T<sub>CW</sub>) and an open window period (T<sub>OW</sub>), see Fig. 4. If no pulse is applied on the  $\overline{\text{TCL}}$  input during the open window period T<sub>OW</sub>, the  $\overline{\text{RES}}$  output goes low for a time T<sub>WDR</sub>. When a pulse is applied on the  $\overline{\text{TCL}}$  input, the cycle is restarted with a close window period.

For example if T<sub>WD</sub> = T<sub>POR</sub> = 100ms, T<sub>CW</sub> = 80 ms, T<sub>OW</sub> = 40ms and T<sub>WDR</sub> = 2.5ms.

When V<sub>IN</sub> recovers after a drop below V<sub>REF</sub>, the pad  $\overline{\text{RES}}$  is set low for the time T<sub>POR</sub> during which any  $\overline{\text{TCL}}$  activation is disabled.

### Timer Clearing and $\overline{\text{RES}}$ Action

The watchdog circuit monitors the activity of the processor. If the user's software does not send a pulse to the  $\overline{\text{TCL}}$  input within the programmed open window timeout period a short watchdog  $\overline{\text{RES}}$  pulse is generated which is equal to T<sub>WDR</sub> (see Fig. 6).

With the open window constraint, new security is added to conventional watchdogs by monitoring both software cycle time and execution. Should software clear the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution) it will cause the system to be reset. If software is stuck in a loop which includes the routine to clear the watchdog then a conventional watchdog would not make a system reset even though the software is malfunctioning; the circuit would make a system reset because the watchdog would be cleared too quickly.

If no  $\overline{\text{TCL}}$  signal is applied before the closed and open windows expire,  $\overline{\text{RES}}$  will start to generate square waves of period (T<sub>CW</sub> + T<sub>OW</sub> + T<sub>WDR</sub>). The watchdog will remain in this state until the next  $\overline{\text{TCL}}$  falling edge appears during an open window, or until a fresh power-up sequence. The system enable output,  $\overline{\text{EN}}$ , can be used to prevent critical control functions being activated in the event of the system going into this failure mode (see section "Enable-EN Output").

The  $\overline{\text{RES}}$  output must be pulled up to V<sub>DD</sub> even if the output is not used by the system (see Fig 8).

### Combined Voltage and Timer Action

The combination of voltage and timer actions is illustrated by the sequence of events shown in Fig. 6. On power-up, when the voltage at V<sub>IN</sub> reaches V<sub>REF</sub>, the power-on-reset, POR, delay is initialized and holds  $\overline{\text{RES}}$  active for the time of the POR delay. A  $\overline{\text{TCL}}$  pulse will have no effect until this power-on-reset delay is completed. When the risk exists that  $\overline{\text{TCL}}$  temporarily floats, e.g. during T<sub>POR</sub>, a pull-up to V<sub>DD</sub> is required on that pin. After the POR delay has elapsed,  $\overline{\text{RES}}$  goes inactive and the watchdog timer starts acting. If no  $\overline{\text{TCL}}$  pulse occurs,  $\overline{\text{RES}}$  goes active low for a short time T<sub>WDR</sub> after each closed and open window period. A  $\overline{\text{TCL}}$  pulse coming during the open window clears the watchdog timer. When the  $\overline{\text{TCL}}$  pulse occurs too early (during the closed window),  $\overline{\text{RES}}$  goes active and a new timeout sequence starts. A voltage drop below the V<sub>REF</sub> level for longer than typically 3 μs overrides the timer and immediately forces  $\overline{\text{RES}}$  active and  $\overline{\text{EN}}$  inactive. Any further  $\overline{\text{TCL}}$  pulse has no effect until the next power-up sequence has completed.

## Enable - $\overline{EN}$ Output

The system enable output,  $\overline{EN}$ , is inactive always when  $\overline{RES}$  is active and remains inactive after a  $\overline{RES}$  pulse until the watchdog is serviced correctly 3 consecutive times (i.e. the  $\overline{TCL}$  pulse must come in the open window). After three consecutive services of the watchdog with  $\overline{TCL}$  during the open window, the  $\overline{EN}$  goes active low.

A malfunctioning system would be repeatedly reset by the watchdog. In a conventional system critical motor controls

could be energized each time reset goes inactive (time allowed for the system to restart) and in this way the electrical motors driven by the system could function out of control. The circuit prevents the above failure mode by using the  $\overline{EN}$  output to disable the motor controls until software has successfully cleared the watchdog three times (i.e. the system has correctly re-started after a reset condition).

## Typical Application

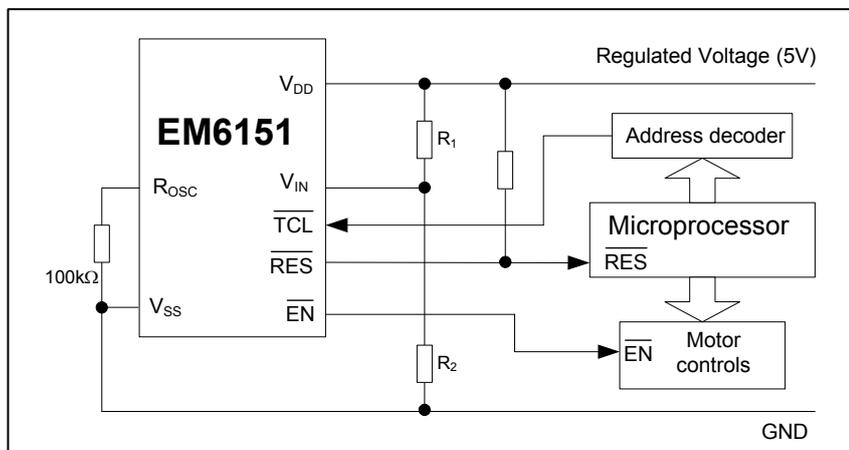


Fig. 8

## V30 R<sub>OSC</sub> Coefficient versus T<sub>WD</sub> at V<sub>DD</sub>= 5.0V and T<sub>j</sub>=-40 to +125°C

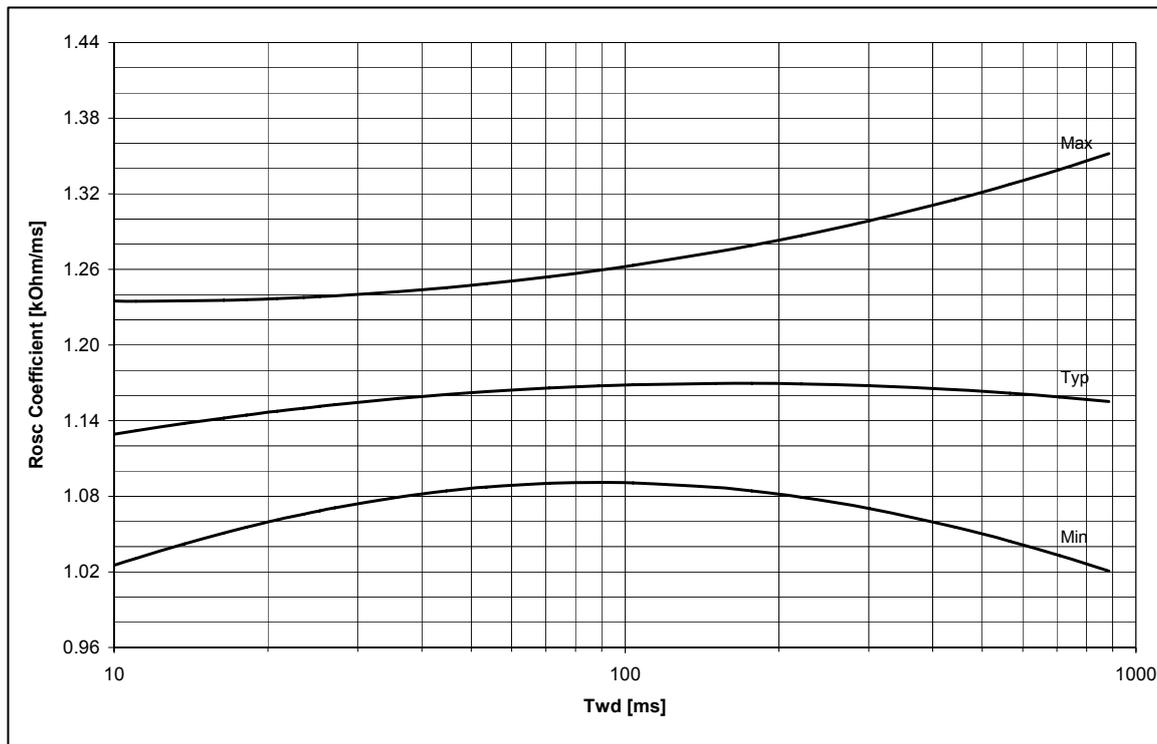


Fig. 9

## V50 R<sub>OSC</sub> Coefficient versus T<sub>WD</sub> at V<sub>DD</sub>= 5.0V and T<sub>j</sub>=-40 to +125°C

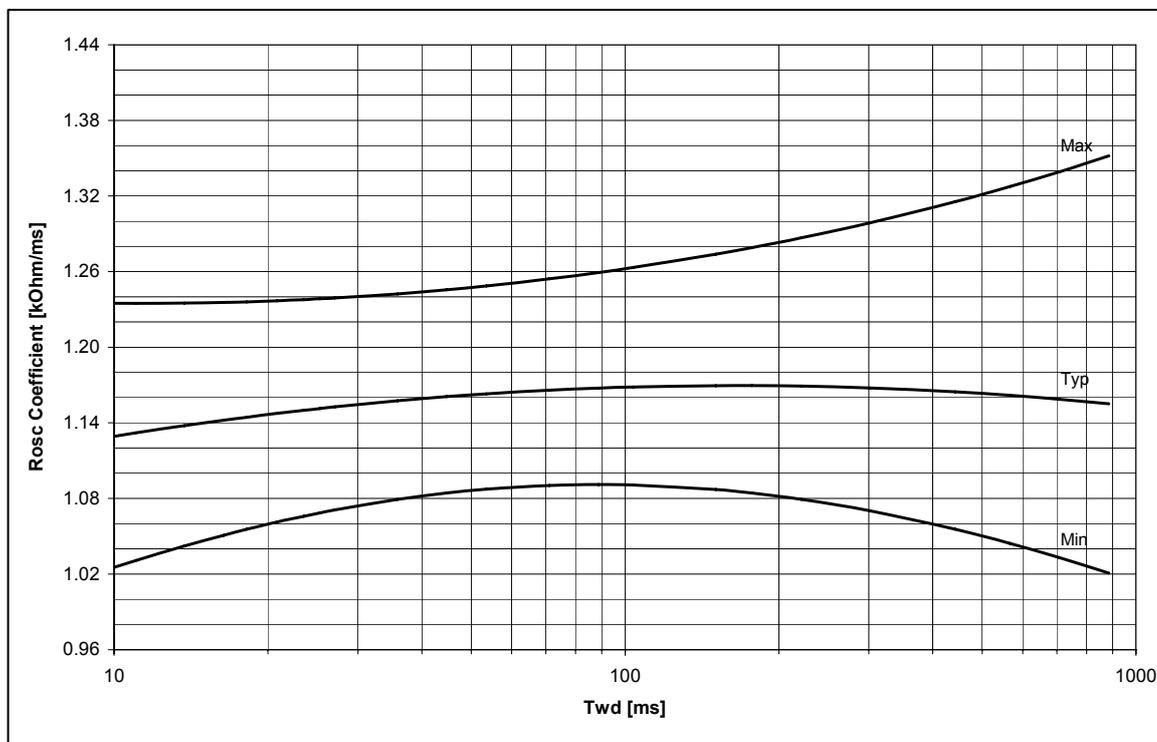


Fig. 10

## V53 R<sub>OSC</sub> Coefficient versus T<sub>WD</sub> at V<sub>DD</sub>= 5.0V and T<sub>j</sub>=-40 to +125°C

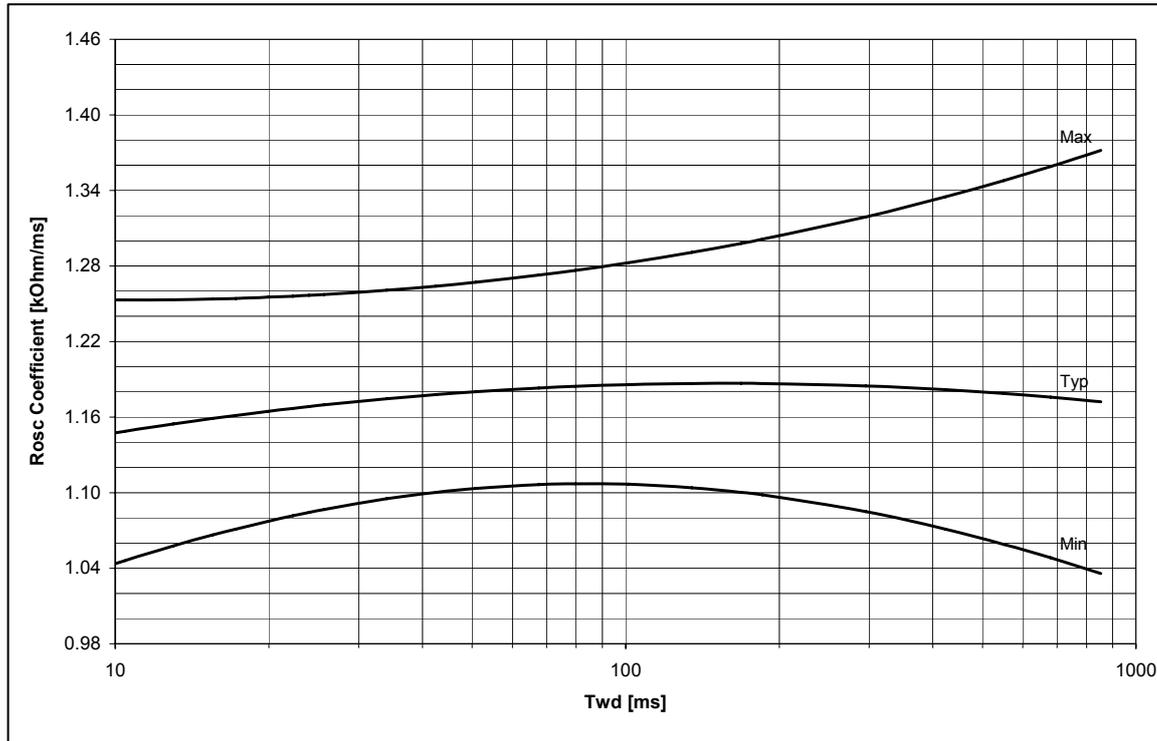


Fig. 11

## V55 R<sub>OSC</sub> Coefficient versus T<sub>WD</sub> at V<sub>DD</sub>= 5.0V and T<sub>j</sub>=-40 to +125°C

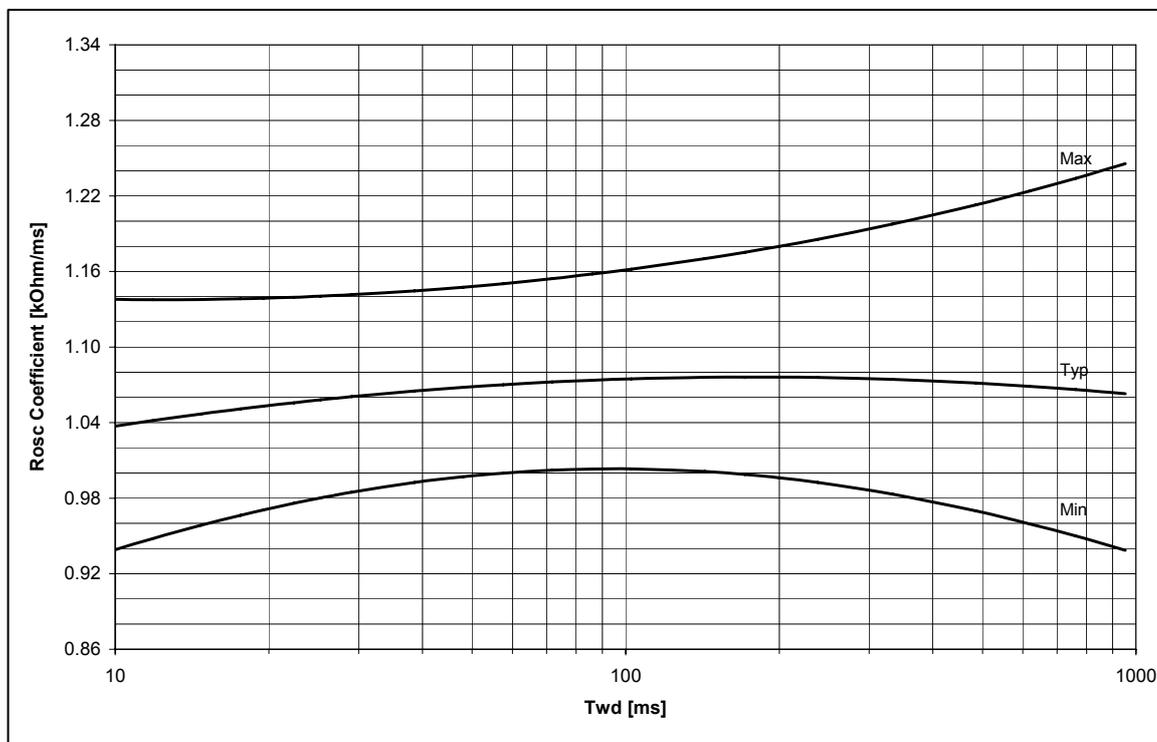


Fig. 12

## Package Information

### Dimensions of 8-pin SOIC Package

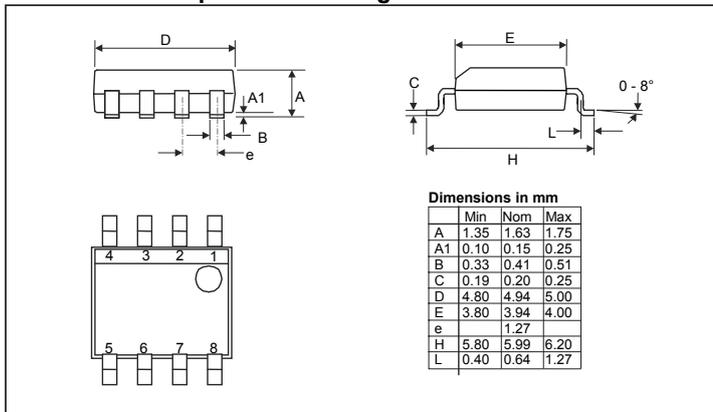


Fig. 13

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