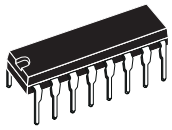
ETC5054
ETC5057

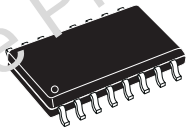
SERIAL INTERFACE CODEC/FILTER

- COMPLETE CODEC AND FILTERING SYSTEM (DEVICE) INCLUDING:
  - Transmit high-pass and low-pass filtering.
  - Receive low-pass filter with sin x/x correction.
  - Active RC noise filters
  - μ-law or A-law compatible COder and DECoder.
  - Internal precision voltage reference.
  - Serial I/O interface.
  - Internal auto-zero circuitry.
- A-LAW 16 PINS (ETC5057FN, 20 PINS)
- μ-LAW WITHOUT SIGNALING, 16 PINS (ETC5054FN, 20 PINS)
- MEETS OR EXCEEDS ALL D3/D4 AND CCITT SPECIFICATIONS
- ±5V OPERATION
- LOW OPERATING POWER - TYPICALLY 60 mW
- POWER-DOWN STANDBY MODE - TYPICALLY 3 mW
- AUTOMATIC POWER-DOWN
- TTL OR CMOS COMPATIBLE DIGITAL INTERFACES
- MAXIMIZES LINE INTERFACE CARD CIRCUIT DENSITY
- 0 to 70°C OPERATION



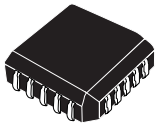
DIP16 (Plastic)

ORDERING NUMBERS:
ETC5057N
ETC5054N



SO16 (Wide)

ORDERING NUMBERS:
ETC5057D
ETC5054D



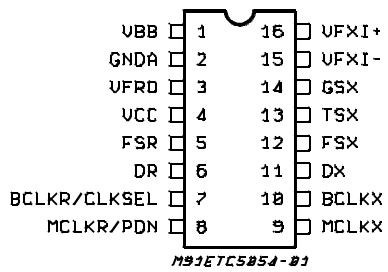
PLCC20

ORDERING NUMBERS:
ETC5057FN
ETC5054FN

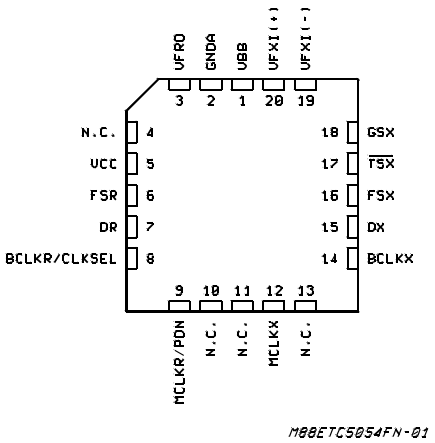
DESCRIPTION

The ETC5057/ETC5054 family consists of A-law and μ–law monolithic PCM CODEC/filters utilizing the A/D and D/A conversion architecture shown in the block diagram below, and a serial PCM interface. The devices are fabricated using double-poly CMOS process. The encode portion of each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. Also included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded A-law or μ–law PCM format. The decode portion of each device consists of an expanding decoder, which reconstructs the analog signal from the companded A-law or μ–law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz and is followed by a single-ended power amplifier capable of driving low impedance loads. The devices require 1.536 MHz, 1.544 MHz, or 2.048 MHz transmit and receive master clocks, which may be asynchronous, transmit and receive bit clocks which may vary from 64 kHz to 2.048 MHz, and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.

PIN CONNECTIONS (Top view)

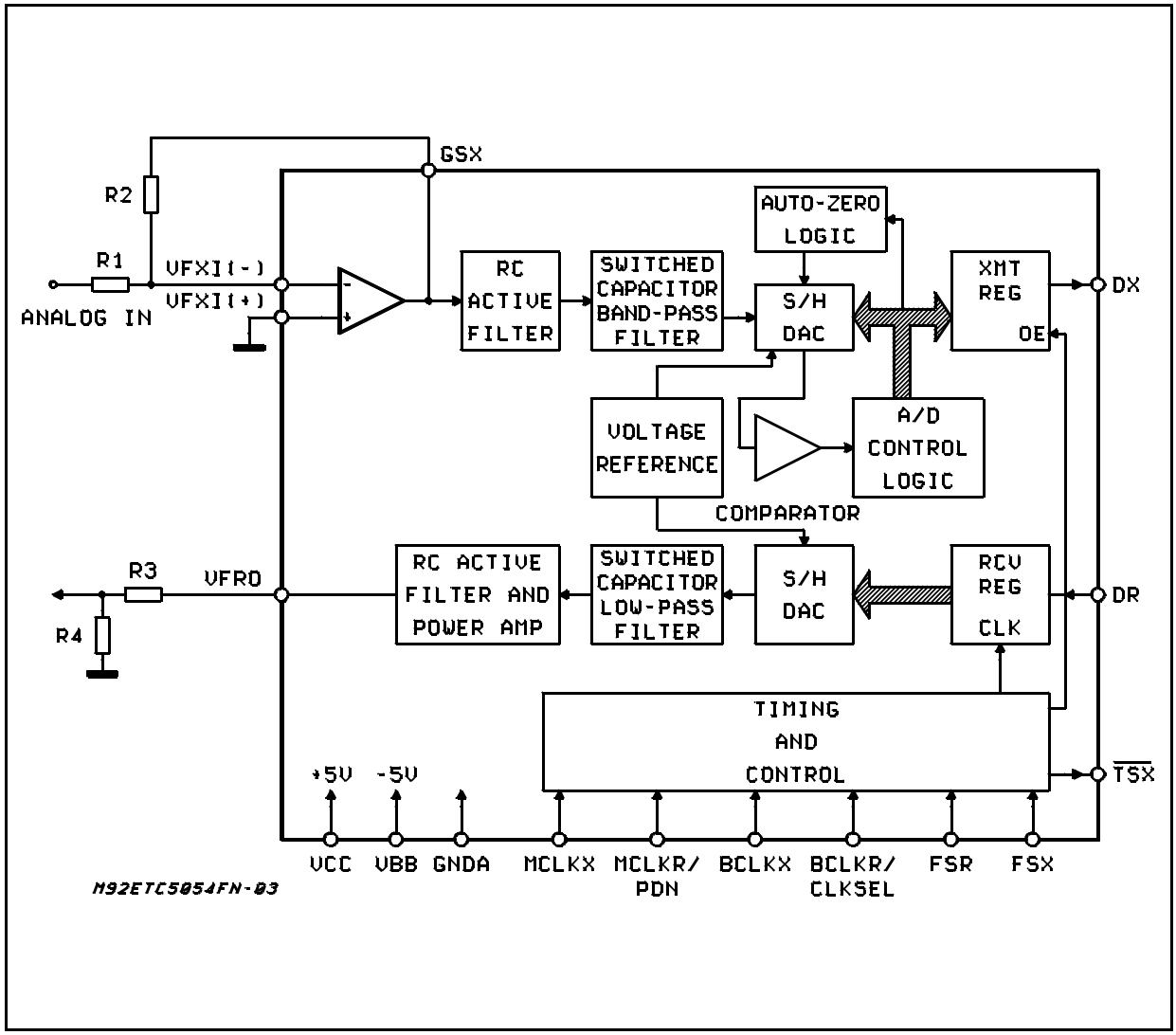


DIP and SO



PLCC

BLOCK DIAGRAM



PIN DESCRIPTION

Name	Pin Type *	N° DIP and SO	N° PLCC (**)	Function	Description
V_{BB}	S	1	1	Negative Power Supply	V_{BB} = – 5 V ± 5 %.
GNDA	GND	2	2	Analog Ground	All signals are referenced to this pin.
VF_RO	O	3	3	Receive Filter Output	Analog Output of the Receive Filter
V_{CC}	S	4	5	Positive Power Supply	V_{CC} = + 5 V ± 5 %.
FS_R	I	5	6	Receive Frame Sync Pulse	Enables $BCLK_R$ to shift PCM data into D_R. FS_R is an 8kHz pulse train. See figures 1, 2 and 3 for timing details.
D_R	I	6	7	Receive Data Input	PCM data is shifted into D_R following the FS_R leading edge.
$BCLK_R$/CLKSEL	I	7	8	Shift-in Clock	Shifts data into D_R after the FS_R leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (see table 1). This input has an internal pull-up.
$MCLK_R$/PDN	I	8	9	Receive Master Clock	Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.
$MCLK_X$	I	9	12	Transmit Master Clock	Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$.
$BCLK_X$	I	10	14	Shift-out Clock	Shifts out the PCM data on DX. May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
D_X	O	11	15	Transmit Data Output	The TRI-STATE® PCM data output which is enabled by FS_X.
FS_X	I	12	16	Transmit Frame Sync Pulse	Enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8 kHz pulse train. See figures 1, 2 and 3 for timing details.
$\overline{TS_X}$	O	13	17	Transmit Time Slot	Open drain output which pulses low during the encoder time slot. Recommended to be grounded if not used.
GS_X	O	14	18	Gain Set	Analog output of the transmit input amplifier. Used to set gain externally.
VF_XI^-	I	15	19	Inverting Amplifier Input	Inverting Input of the Transmit Input Amplifier.
VF_XI^+	I	16	20	Non-inverting Amplifier Input	Non-inverting Input of the Transmit Input Amplifier.

(*) I: Input, O: Output, S: Power Supply
(**) Pins 4,10,11 and 13 are not connected
TRI-STATE® is a trademark of National Semiconductor Corp.

FUNCTIONAL DESCRIPTION

POWER-UP

When power is first applied, power-on reset circuitry initializes the device and places it into the power-down mode. All non-essential circuits are deactivated and the D_X and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin and FS_X and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high ; the alternative is to hold both FS_X and FS_R inputs continuously low. The device will power-down approximately 2 ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The TRI-STATE PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R$/PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCLK_R$/CKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. With a fixed level on the $BCLK_R$/CLKSEL pin, $BCLK_X$ will be selected as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R$/CLKSEL. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With and FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$ (or $BCLK_R$ if running). FS_X and FS_R must be synchronous with $MCLK_{X/R}$.

Table 1: Selection of Master Clock Frequencies.

$BCLK_R$/CLKSEL	Master Clock Frequency Selected	
	ETC5057	ETC5054
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1 (or open circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied, $MCLK_X$ and $MCLK_R$ must be 2.048 MHz for the ETC5057, or 1.536 MHz, 1.544 MHz for the ETC5054, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R$/PDN pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see pin description). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$. $BCLK_R$ must be a clock, the logic levels shown in table 1 are not valid in asynchronous mode. $BCLK_X$ and $BCLK_R$ may operate from 64 kHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The device can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X and FS_R, must be one bit clock period long, with timing relationships specified in figure 2. With FS_X high during a falling edge of $BCLK_X$ the next rising edge of $BCLK_X$ enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. Both devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long frame mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships specified in figure 3. Based on the transmit frame sync, FS_X, the device will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns (see fig. 1). The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising

edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by FS_X going low, which-ever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$ ($BCLK_X$ in synchronous mode). Both devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see figure 6. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unitygain filter consisting of RD active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to A-law (ETC5057) or µ–law (ETC5054) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5V peak (see table of transmission characteristics). The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165 µs (due to the transmit filter) plus 125µs (due to encoding delay), which totals 290µs. Any offset vol-tage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (ETC5057) or µ–law (ETC5054) and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample and hold. The filter is then followed by a 2nd order RC active post-filter and power amplifier capable of driving a 600Ω load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10µs later the decoder DAC output is updated. The total decoder delay is ~ 10µs (decoder update) plus 110µs (filter delay) plus 62.5µs (1/2 frame), which gives approximately 180µs. A mute circuitry is a active during 10ms when power up.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to GNDA	7	V
V_{BB}	V_{BB} to GNDA	– 7	V
V_{IN}, V_{OUT}	Voltage at any Analog Input or Output	V_{CC} + 0.3 to V_{BB} – 0.3	V
	Voltage at Any Digital Input or Output	V_{CC} + 0.3 to GNDA – 0.3	V
T_{oper}	Operating Temperature Range	– 25 to + 125	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
	Lead Temperature (soldering, 10 seconds)	300	°C

ELECTRICAL OPERATING CHARACTERISTICS V_{CC} = 5.0 V ± 5 %, V_{BB} = – 5.0 V ± 5%GNDA = 0 V, T_A = 0 °C to 70 °C; Typical Characteristics Specified at V_{CC} = 5.0 V, V_{BB} = – 5.0 V, T_A = 25 °C ; all signals are referenced to GNDA.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage			0.6	V
V_{IH}	Input High Voltage	2.2			V
V_{OL}	Output Low Voltage I_L = 3.2mA D_X I_L = 3.2mA, Open Drain TS_X			 0.4 0.4	 V V
V_{OH}	Output High Voltage I_H = 3.2mA D_X	 2.4			 V
I_{IL}	Input Low Current (GNDA ≤ V_{IN} ≤ V_{IL}, all digital inputs)	–10		10	µA
I_{IH}	Input High Current (V_{IH} ≤ V_{IN} ≤ V_{CC}) except $BCLK_R$/BCLKSEL	–10		10	µA
I_{OZ}	Output Current in HIGH Impedance State (TRI-STATE) (GNDA ≤ V_O ≤ V_{CC}) D_X	 –10		 10	 µA

ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (all devices)

Symbol	Parameter		Min.	Typ.	Max.	Unit
I_IXA	Input Leakage Current ($-2.5V \le V \le +2.5V$)	VF_XI^+ or VF_XI^-	– 200		200	nA
R_IXA	Input Resistance ($-2.5V \le V \le +2.5V$)	VF_XI^+ or VF_XI^-	10			MΩ
R_OXA	Output Resistance (closed loop, unity gain)			1	3	Ω
R_LXA	Load Resistance	GS_X	10			kΩ
C_LXA	Load Capacitance	GS_X			50	pF
V_OXA	Output Dynamic Range ($R_L \ge 10K\Omega$)	GS_X	±2.8			V
AV_XA	Voltage Gain (VF_XI^+ to GS_X)		5000			V/V
F_UXA	Unity Gain Bandwidth		1	2		MHz
$V_{OS}XA$	Offset Voltage		– 20		20	mV
$V_{CM}XA$	Common-mode Voltage		– 2.5		2.5	V
CMRRXA	Common-mode Rejection Ratio		60			dB
PSRRXA	Power Supply Rejection Ratio		60			dB

ANALOG INTERFACE WITH RECEIVE FILTER (all devices)

Symbol	Parameter		Min.	Typ.	Max.	Unit
R_ORF	Output Resistance	VF_RO		1	3	Ω
R_LRF	Load Resistance (VF_RO = ±2.5V)		600			Ω
C_LRF	Load Capacitance				500	pF
VOS_RO	Output DC Offset Voltage		– 200		200	mV

POWER DISSIPATION (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{CC}0$	Power-down Current		0.5	1.5	mA
$I_{BB}0$	Power-down Current		0.05	0.3	mA
$I_{CC}1$	Active Current		6.0	9.0	mA
$I_{BB}1$	Active Current		6.0	9.0	mA

TIMING SPECIFICATIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
$1/t_{PM}$	Frequency of master clocks Depends on the device used and the $BCLK_R$/CLKSEL Pin $MCLK_X$ and $MCLK_R$		1.536 1.544 2.048		MHz MHz MHz
t_{WMH}	Width of Master Clock High $MCLK_X$ and $MCLK_R$	160			ns
t_{WML}	Width of Master Clock Low $MCLK_X$ and $MCLK_R$	160			ns
t_{RM}	Rise Time of Master Clock $MCLK_X$ and $MCLK_R$			50	ns
t_{FM}	Fall Time of Master Clock $MCLK_X$ and $MCLK_R$			50	ns
t_{PB}	Period of Bit Clock	485	488	15.725	ns
t_{WBH}	Width of Bit Clock High (V_{IH} = 2.2V)	160			ns
t_{WBL}	Width of Bit Clock Low (V_{IL} = 0.6V)	160			ns
t_{RB}	Rise Time of Bit Clock (t_{PB} = 488ns)			50	ns
t_{FB}	Fall Time of Bit Clock (t_{PB} = 488ns)			50	ns
t_{SBFM}	Set-up time from $BCLK_X$ high to $MCLK_X$ falling edge. (first bit clock after the leading edge of FS_X)	100			ns
t_{HBF}	Holding Time from Bit Clock Low to the Frame Sync (long frame only)	0			ns
t_{SFB}	Set-up Time from Frame Sync to Bit Clock (long frame only)	80			ns
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (long frame only) FS_X or FS_R	100			ns
t_{DZF}	Delay time to valid data from FS_X or $BCLK_X$, whichever comes later and delay time from FS_X to data output disabled. (C_L = 0pF to 150pF)	20		165	ns
t_{DBD}	Delay time from $BCLK_X$ high to data valid. (load = 150pF plus 2 LSTTL loads)	0		180	ns
t_{DZC}	Delay time from $BCLK_X$ low to data output disabled.	50		165	ns
t_{SDB}	Set-up time from D_R valid to $BCLK_{R/X}$ low.	50			ns
t_{HBD}	Hold time from $BCLK_{R/X}$ low to D_R invalid.	50			ns
t_{HOLD}	Holding Time from Bit Clock High to Frame Sync (short frame only)	0			ns
t_{SF}	Set-up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low (short frame sync pulse) - Note 1	80			ns
t_{HF}	Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low (short frame sync pulse) - Note 1	100			ns
t_{XDP}	Delay Time to TS_Xlow (load = 150pF plus 2 LSTTL loads)			140	ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (low level) 64kbit/s operating mode)	160			ns

Note 1: For short frame sync timing FS_X and FS_R must go high while their respective bit clocks are high.

Figure 1: 64kbits/s TIMING DIAGRAM (see next page for complete timing).

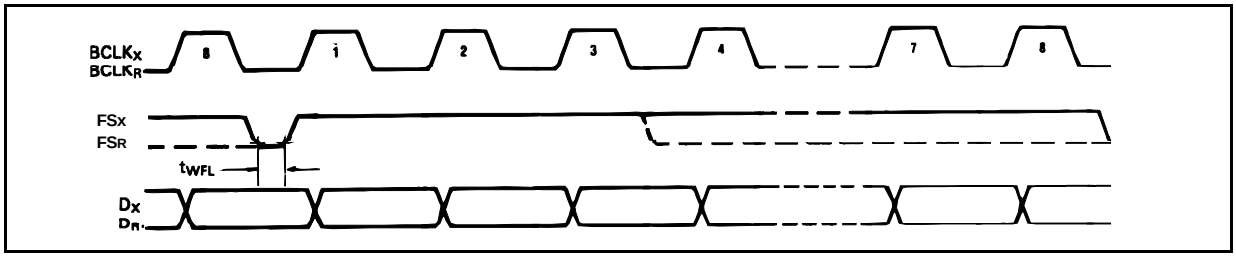


Figure 2: Short Frame Sync Timing

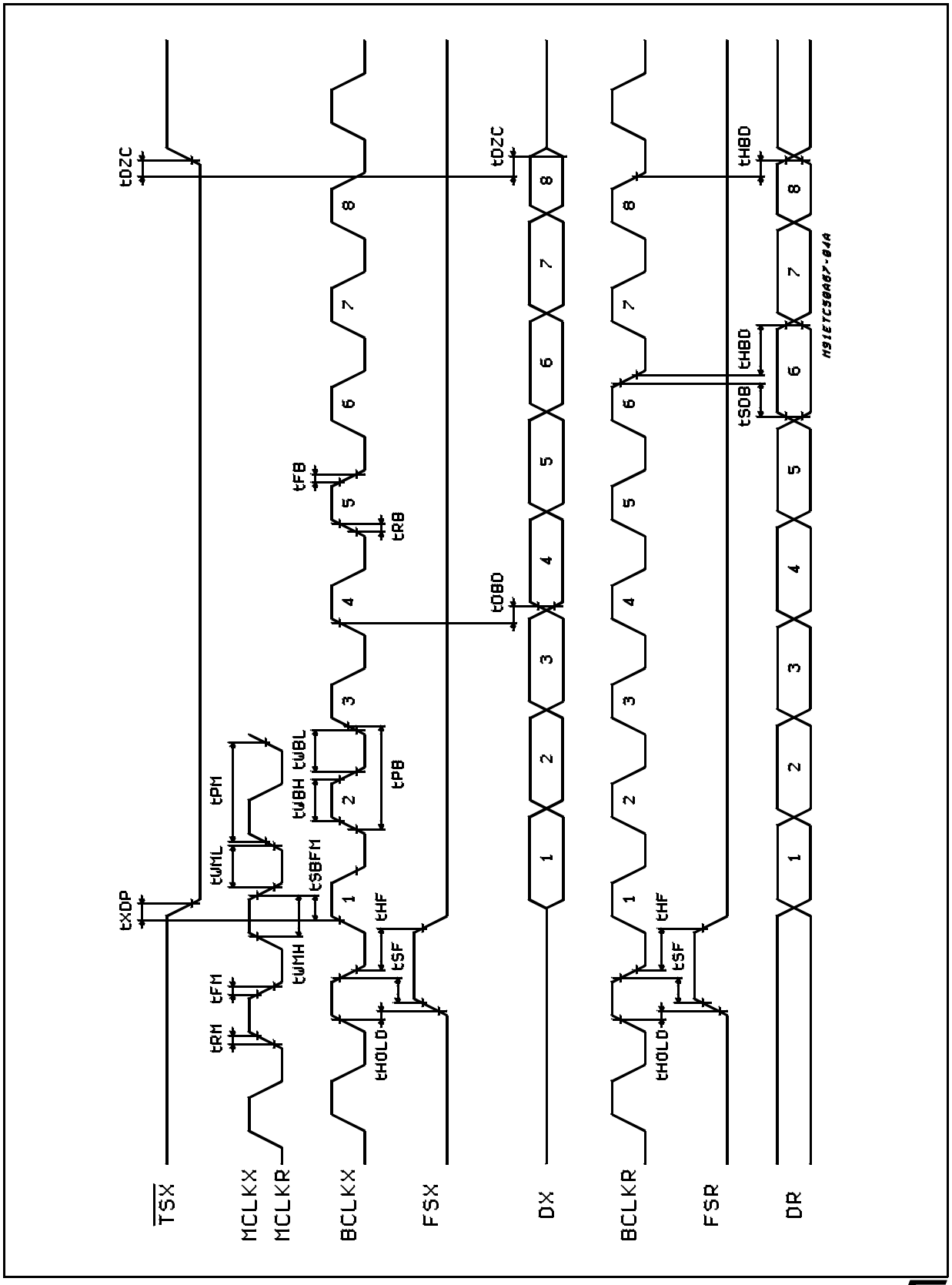
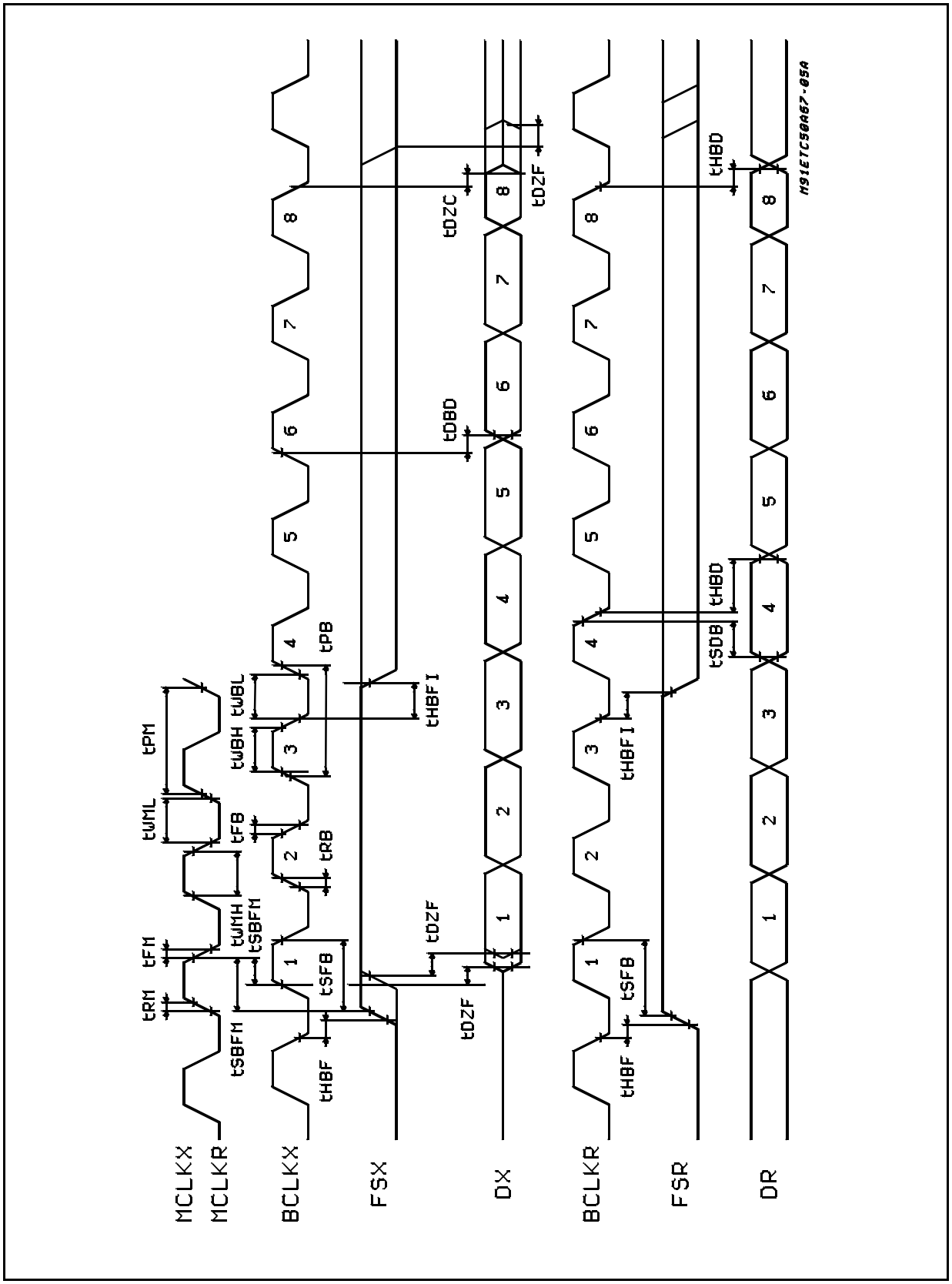


Figure 3: Long Frame Sync Timing



TRANSMISSION CHARACTERISTICS

T_A = 0 to 70°C, V_{CC} = +5V ±5%, V_{BB} = –5V ±5%, GNDA = 0V, f = 1.0KHz, V_{IN} = 0dBm0 transmit input amplifier connected for unity-gain non-inverting (unless otherwise specified).

AMPLITUDE RESPONSE

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Absolute levels - nominal 0 dBm0 level is 4 dBm (600 Ω) 0 dBm0		1.2276		Vrms
t_{MAX}	Max Overload Level 3.14 dBm0 (A LAW) 3.17 dBm0 (U LAW)		 2.492 2.501		 V_{PK} V_{PK}
G_{XA}	Transmit Gain, Absolute (TA = 25 °C, V_{CC} = 5 V, V_{BB} = – 5 V) Input at GS_X = 0 dBm0 at 1020 Hz	 – 0.15		 0.15	 dB
G_{XR}	Transmit Gain, Relative to GXA f = 16 Hz f = 50 Hz f = 60 Hz f = 180 Hz f = 200 Hz f = 300 Hz - 3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz f = 4600 Hz and up, Measure Response from 0 Hz to 4000 Hz	 – 2.8 – 1.8 – 0.15 – 0.35 – 0.7		 – 40 – 30 – 26 – 0.2 – 0.1 0.15 0.05 0 – 14 – 32	 dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature TA = 0 to +70°C	 – 0.1		 0.1	 dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage (V_{CC} = 5 V ± 5 %, V_{BB} = – 5 V ± 5 %)	 – 0.05		 0.05	 dB
G_{XRL}	Transmit Gain Variations with Level Sinusoidal Test Method Reference Level = – 10 dBm0 VFXI+ = – 40 dBm0 to + 3 dBm0 VF_XI+ = – 50 dBm0 to – 40 dBm0 VF_XI+ = – 55 dBm0 to – 50 dBm0	 – 0.2 – 0.4 – 1.2		 0.2 0.4 1.2	 dB dB dB
G_{RA}	Receive Gain, Absolute (T_A = 25°C, V_{CC} = 5V, V_{BB} = –5V) Input = Digital Code Sequence for 0dBm0 Signal at 1020Hz	 – 0.15		 0.15	 dB
G_{RR}	Receive Gain, Relative to GRA f = 0Hz to 3000Hz f = 3300Hz f = 3400Hz f = 4000Hz	 – 0.35 – 0.35 – 0.7		 0.20 0.05 0 – 14	 dB dB dB dB
G_{RAT}	Absolute Transmit Gain Variation with Temperature T_A = 0 to +70°C	 – 0.1		 0.1	 dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage (V_{CC} = 5 V ± 5 %, V_{BB} = – 5 V ± 5 %)	 – 0.05		 0.05	 dB
G_{RRL}	Receive Gain Variations with Level Sinusoidal Test Method; Reference input PCM code corresponds to an ideally encoded – 10 dBm0 signal PCM level = – 40 dBm0 to + 3 dBm0 PCM level = – 50 dBm0 to – 40 dBm0 PCM level = – 55 dBm0 to – 50 dBm0	 – 0.2 – 0.4 – 1.2		 0.2 0.4 1.2	 dB dB dB
V_{RO}	Receive Output Drive Level (R_L = 600Ω)	– 2.5		2.5	V

TRANSMISSION (continued)

ENVELOPE DELAY DISTORTION WITH FREQUENCY

Symbol	Parameter	Min.	Typ.	Max.	Unit
D_{XA}	Transmit Delay, Absolute (f = 1600Hz)		290	315	µs
D_{XR}	Transmit Delay, Relative to D_{XA} f = 500Hz - 600Hz f = 600Hz - 800Hz f = 800Hz - 1000Hz f = 1000Hz - 1600Hz f = 1600Hz - 2600Hz f = 2600Hz - 2800Hz f = 2800Hz - 3000Hz		 195 120 50 20 55 80 130	 220 145 75 40 75 105 155	µs
D_{RA}	Receive Delay, Absolute (f = 1600Hz)		180	200	µs
D_{RR}	Receive Delay, Relative to D_{RA} f = 500Hz - 1000Hz f = 1000Hz - 1600Hz f = 1600Hz - 2600Hz f = 2600Hz - 2800Hz f = 2800Hz - 3000Hz	 – 40 – 30	 – 25 – 20 70 100 145	 90 125 175	µs

NOISE

Symbol	Parameter	Min.	Typ.	Max.	Unit
N_{XP}	Transmit Noise, P Message Weighted (A LAW, $VFXI^+$ = 0 V) 1)		– 74	– 69	dBm0p
N_{RP}	Receive Noise, P Message Weighted (A LAW, PCM code equals positive zero)		– 82	– 79	dBm0p
N_{XC}	Transmit Noise, C Message Weighted µ LAW ($VFXI^+$ = 0 V)		12	15	dBmC0
N_{RC}	Receive Noise, C Message Weighted (µ LAW, PCM Code Equals Alternating Positive and Negative Zero)		8	11	dBrnC0
N_{RS}	Noise, Single Frequency f = 0 kHz to 100 kHz, Loop around Measurement, VF_XI^+ = 0 Vrms			– 53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit (note 2) V_{CC} = 5.0 V_{DC} + 100 mVrms, f = 0 kHz-50 kHz	40			dBp
$NPSR_X$	Negative Power Supply Rejection, Transmit (note 2) V_{BB} = – 5.0 V_{DC} + 100 mVrms, f = 0 kHz-50 kHz	40			dBp
$PPSR_R$	Positive Power Supply Rejection, Receive (PCM code equals positive zero, V_{CC} = 5.0 VD_C + 100mVrms) f = 0Hz to 4000Hz f = 4KHz to 25KHz f = 25KHz to 50KHz	 40 40 36			 dBp dB dB
$NPSR_R$	Negative Power Supply Rejection, Receive (PCM code equals positive zero, VBB = 5.0 VD_C + 100mVrms) f = 0Hz to 4000Hz f = 4KHz to 25KHz f = 25KHz to 50KHz	 40 40 36			 dBp dB dB

TRANSMISSION CHARACTERISTICS (continued)

NOISE (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SOS	Spurius out-of-band Signals at the Channel Output Loop around measurement, 0dBm0, 300Hz - 3400Hz input applied to DR, measure individual image signals at DX 4600Hz - 7600Hz 7600Hz - 8400Hz 8400Hz - 100,000Hz			 – 32 – 40 – 32	 dB dB dB

DISTORTION

Symbol	Parameter		Min.	Typ.	Max.	Unit
STD_X or STD_R	Signal to Total Distortion (sinusoidal test method) Transmit or Receive Half-channel Level = 3.0dBm0 Level = 0dBm0 to –30dBm0 Level = –40dBm0 Level = –55dBm0	 XMT RCV XMT RCV	 33 36 29 30 14 15			 dBp
SFD_X	Single Frequency Distortion, Transmit (T_A = 25°C)				–46	dB
SFD_R	Single Frequency Distortion, Receive (T_A = 25°C)				–46	dB
IMD	Intermodulation Distortion Loop Around Measurement, VFXI+ = –4dBm0 to –21dBm0, two Frequencies in the Range 300Hz - 3400Hz				–41	dB

CROSSTALK

Symbol	Parameter	Min.	Typ.	Max.	Unit
CT_{X-R}	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level f = 300Hz to 3400Hz, D_R = Steady PCM Mode		– 90	– 75	dB
CT_{R-X}	Receive to Transmit Crosstalk, 0 dBm0 Receive Level f = 300Hz to 3400Hz, (note 2)		– 90	– 70	dB

Notes:
1) Measured by extrapolation from distortion test results.
2) $PPSR_X$, $NPSR_X$, CT_{R-X} is measured with a –50dBm0 activating signal applied at VF_XI^+.

ENCODING FORMAT AT D_X OUTPUT

	A-Law (including even bit inversion)								**μLaw**							
V_{IN} (at GS_X) = +Full-scale	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0
V_{IN} (at GS_X) = 0V	1 0	1 1	0 0	1 1	0 0	1 1	0 0	1 1	1 0	1 1	1 1	1 1	1 1	1 1	1 1	1 1
V_{IN} (at GS_X) = – Full-scale	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0

APPLICATION INFORMATION

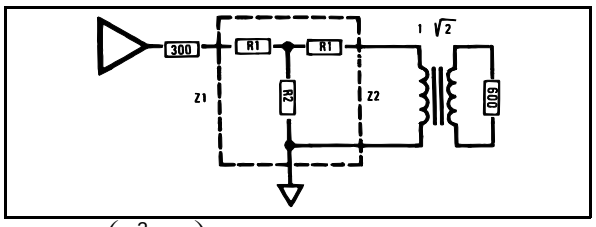
POWER SUPPLIES

While the pins at the ETC505X family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any-other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1µF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB} as close to the device as possible.

For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10µF capacitors.

Figure 4: T-PAD Attenuator



$$R1 = Z1\left(\frac{N^2+1}{N^2-1}\right) - 2\sqrt{Z1 \cdot Z2}\left(\frac{N}{N^2-1}\right)$$

$$R2 = 2\sqrt{Z1.Z2}\left(\frac{N}{N^2-1}\right)$$

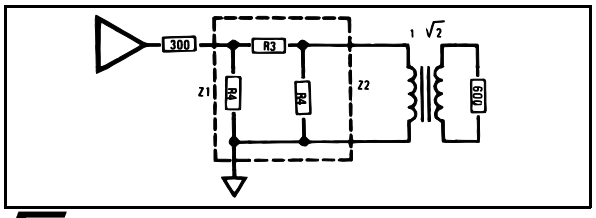
Where: $N = \sqrt{\frac{POWERIN}{POWEROUT}}$

and: $S = \sqrt{\frac{Z1}{Z2}}$

Also : $Z = \sqrt{Z_{SC} \cdot Z_{OC}}$

Where Z_{SC} = impedance with short circuit termination and Z_{OC} = impedance with open circuit termination.

Figure 5: Π-PAD Attenuator



$$R3 = \sqrt{\frac{Z1 \cdot Z2}{2}}\left(\frac{N^2-1}{N}\right)$$

$$R3 = Z1\left(\frac{N^2-1}{N^2-2NS+1}\right)$$

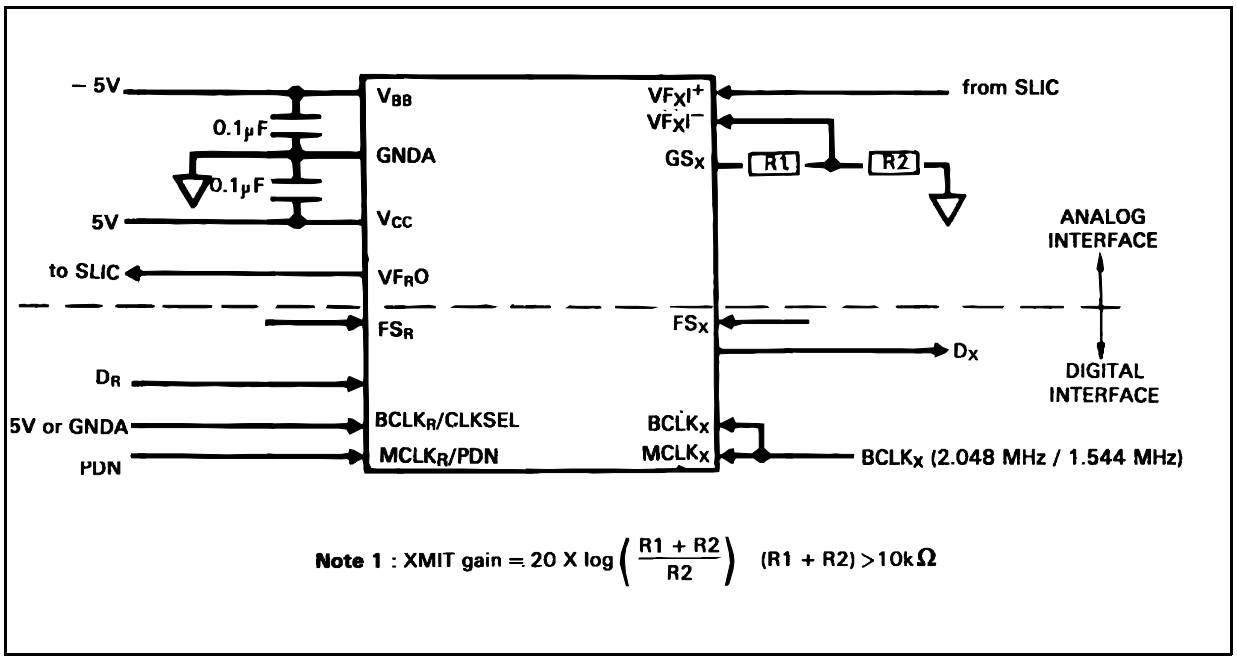
RECEIVE GAIN ADJUSTMENT

For applications where a ETC505X family CODEC/filter receive output must drive a 600Ω load, but a peak swing lower then ± 2.5V is required, the receive gain can be easily adjusted by inserting a matched T-pad or π –pad at the output. Table II lists the required resistor values for 600Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closest pratical set of resistors. It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss. For example a 30dB return loss against 600Ω is obtained if the output impedance of the attenuator is in the range 282Ω to 319Ω (assuming a perfect transformer).

Table 2 : Attenuator Tables For
Z1 = Z2 = 300 Ω (all values in Ω).

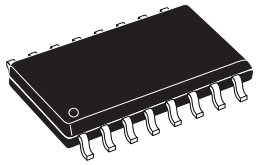
dB	R1	R2	R3	R4
0.1	1.7	26k	3.5	52k
0.2	3.5	13k	6.9	26k
0.3	5.2	8.7k	10.4	17.4k
0.4	6.9	6.5k	13.8	13k
0.5	8.5	5.2k	17.3	10.5k
0.6	10.4	4.4k	21.3	8.7k
0.7	12.1	3.7k	24.2	7.5k
0.8	13.8	3.3k	27.7	6.5k
0.9	15.5	2.9k	31.1	5.8k
1.0	17.3	2.6k	34.6	5.2k
2	34.4	1.3k	70	2.6k
3	51.3	850	107	1.8k
4	68	650	144	1.3k
5	84	494	183	1.1k
6	100	402	224	900
7	115	380	269	785
8	129	284	317	698
9	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	816	430
16	218	98	924	413
18	233	77	1.17k	386
20	246	61	1.5k	366

Figure 6: Typical Synchronous Application.

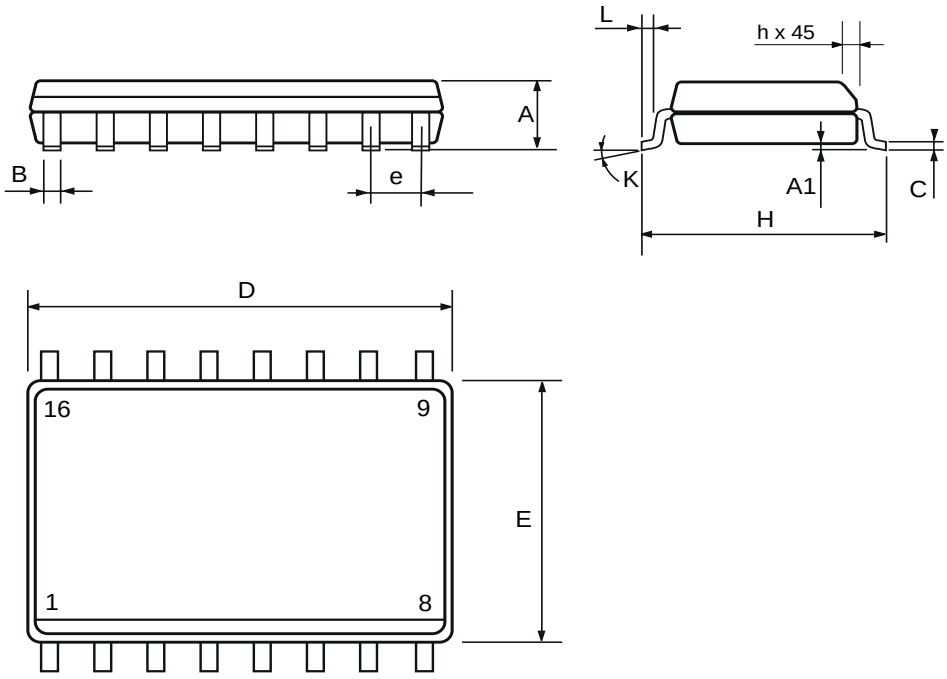


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.1		0.3	0.004		0.012
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	10.1		10.5	0.398		0.413
E	7.4		7.6	0.291		0.299
e		1.27			0.050	
H	10		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.4		1.27	0.016		0.050
K	0° (min.)8° (max.)					

OUTLINE AND MECHANICAL DATA

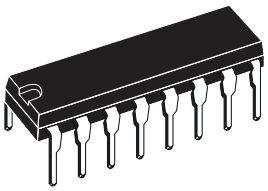


SO16 Wide

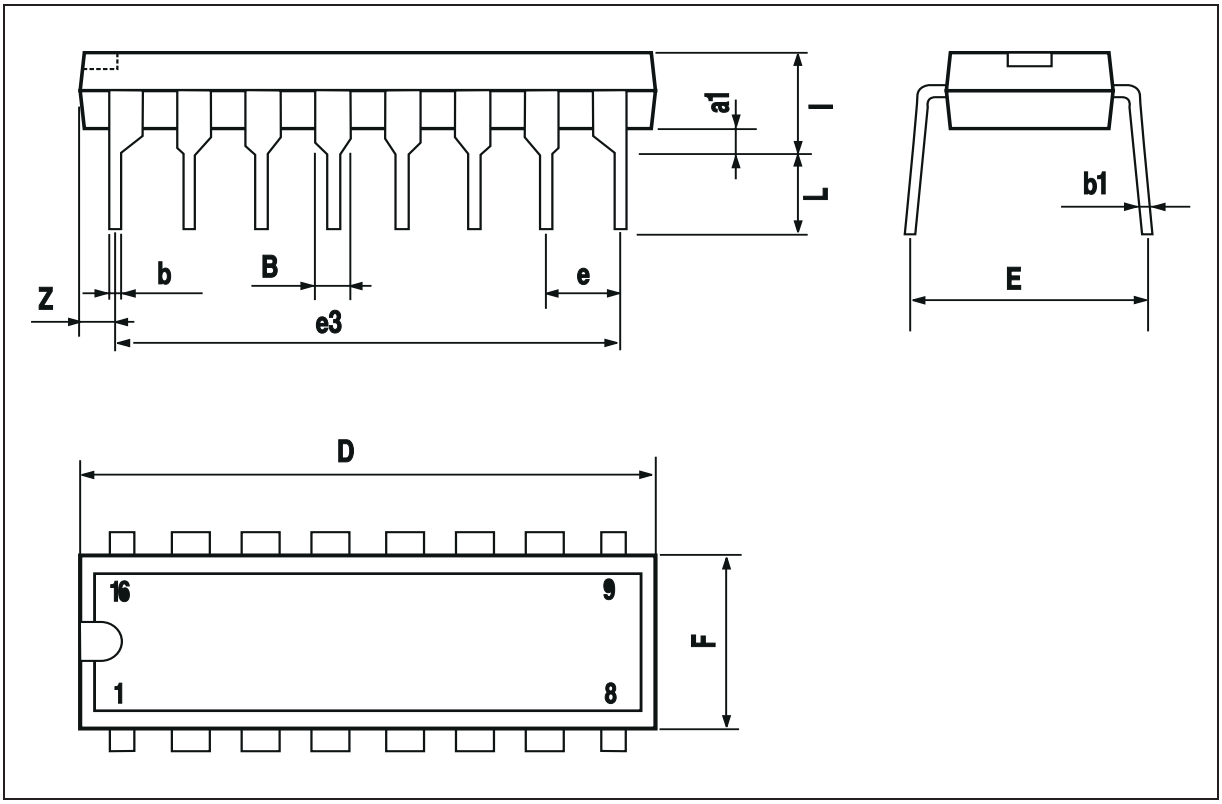


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

OUTLINE AND MECHANICAL DATA

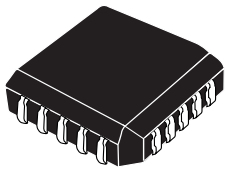


DIP16



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	

OUTLINE AND MECHANICAL DATA



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