

HD61102

(Dot Matrix Liquid Crystal Graphic Display Column Driver)

Description

HD61102 is a column (segment) driver for dot matrix liquid crystal graphic display systems. It stores the display data transferred from a 8-bit micro-controller in internal display RAM and generates dot matrix liquid crystal driving signals.

Each data bit of display RAM corresponds to the on/off state of a dot of the liquid crystal display.

As it is internally equipped with 64 output drivers for display, it is available for liquid crystal graphic displays with many dots.

The HD61102, which is produced by the CMOS process, can complete a portable battery drive equipment in combination with a CMOS micro-controller, utilizing the liquid crystal display's low power dissipation.

Moreover it can facilitate dot matrix liquid crystal graphic display system configuration in combination with the row (common) driver HD61103A.

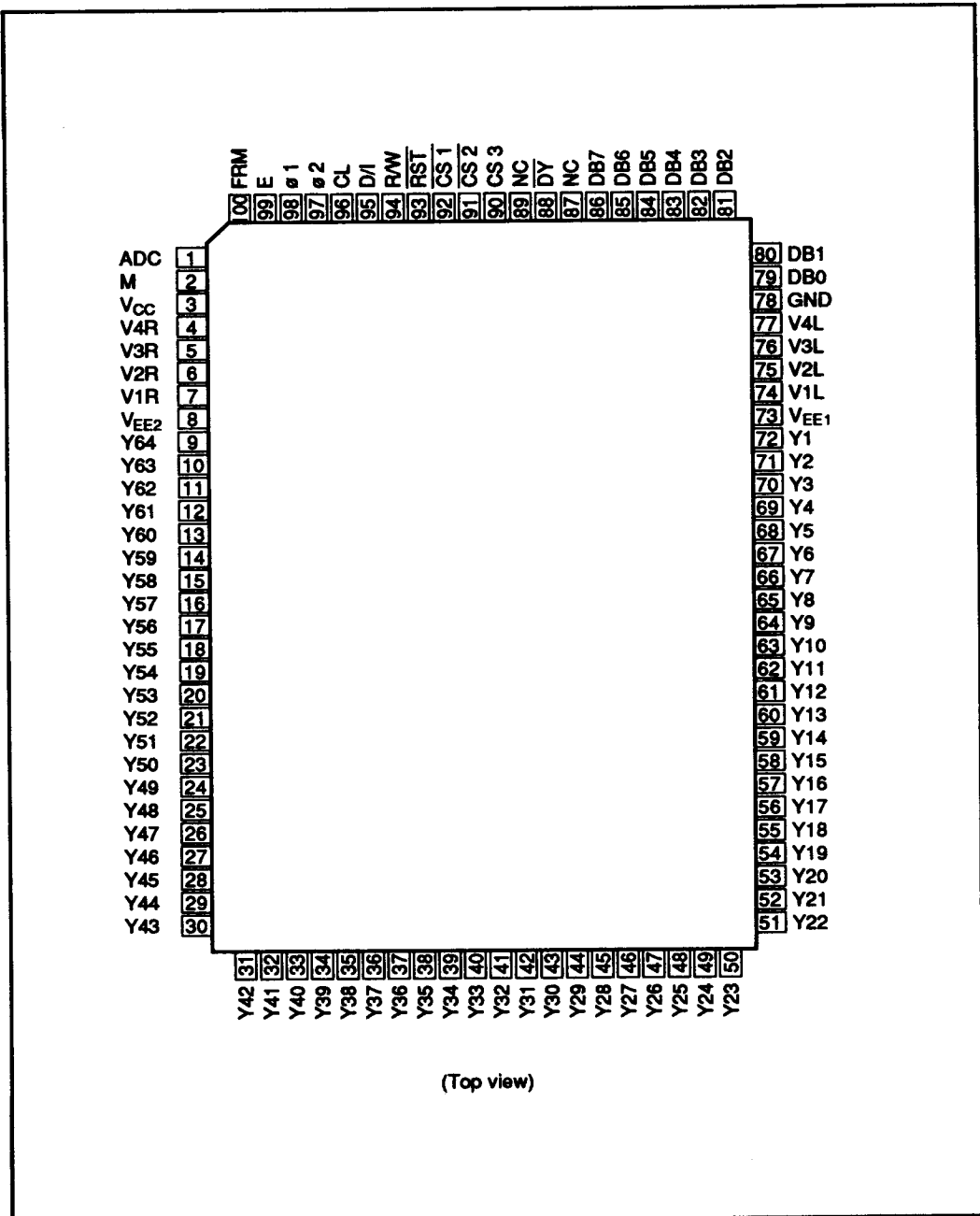
Features

- Dot matrix liquid crystal graphic display column driver incorporating display RAM
- RAM data direct display by internal display RAM
 - RAM bit data 1: On
 - RAM bit data 0: Off
- Internal display RAM address counter:
 - Preset, increment
- Display RAM capacity: 512 bytes (4096 bits)
- 8-bit parallel interface
- Internal liquid crystal display driver circuit: 64
- Display duty:
 - Combination of frame control signal and data latch synchronization signal make it possible to select static or optional duty cycle
- Wide range of instruction function:
 - Display Data Read/Write, Display On/Off, Set Address, Set Display Start Line, Read Status
- Lower power dissipation: during display 2mW max
- Power supply:
 - V_{CC} : +5 V \pm 10%
 - V_{EE} : 0 V to -10 V
- Liquid crystal display driving level: 15.5 V max
- CMOS process
- 100-pin flat plastic package (FP-100)

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Pin Arrangement



(Top view)

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Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	-0.3 to +7.0	V	2
	V_{EE}	$V_{CC} - 16.5$ to $V_{CC} + 0.3$	V	3
Terminal voltage (1)	V_{T1}	$V_{EE} - 0.3$ to $V_{CC} + 0.3$	V	4
Terminal voltage (2)	V_{T2}	-0.3 to $V_{CC} + 0.3$	V	2, 5
Operating temperature	T_{opr}	-20 to +75	°C	
Storage temperature	T_{stg}	-55 to +125	°C	

- Notes: 1. LSIs may be destroyed if they are used beyond the absolute maximum ratings. In ordinary operation, it is desirable to use them within the recommended operating conditions. Use beyond these conditions may cause malfunction and poor reliability.
2. All voltage values are referenced to GND = 0 V.
3. Apply the same supply voltage to V_{EE1} and V_{EE2} .
4. Applies to V1L, V2L, V3L, V4L, V1R, V2R, V3R, and V4R.
Maintain
 $V_{CC} \geq V1L = V1R \geq V3L = V3R \geq V4L = V4R \geq V2L = V2R \geq V_{EE}$
5. Applies to M, FRM, CL, RST, ADC, $\phi 1$, $\phi 2$, $\overline{CS1}$, $\overline{CS2}$, CS3, E, R/W, D/I, ADC, and DB0-DB7.

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Electrical Characteristics

(GND = 0 V, $V_{CC} = 4.5$ to 5.5 V, $V_{EE} = 0$ to -10 V, $T_a = -20$ to $+75^\circ\text{C}$)

Item	Symbol	Limit			Unit	Test Condition	Note
		Min	Typ	Max			
Input high voltage	V_{IHc}	$0.7 \times V_{CC}$	—	V_{CC}	V		1
	V_{IHt}	2.0	—	V_{CC}	V		2
Input low voltage	V_{ILc}	0	—	$0.3 \times V_{CC}$	V		1
	V_{ILt}	0	—	0.8	V		2
Output high voltage	V_{OH}	2.4	—	—	V	$I_{OH} = -205 \mu\text{A}$	3
Output low voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 1.6 \text{ mA}$	3
Input leakage current	I_{IL}	-1.0	—	+1.0	μA	$V_{in} = \text{GND} - V_{CC}$	4
High impedance off input current	I_{TSL}	-5.0	—	+5.0	μA	$V_{in} = \text{GND} - V_{CC}$	5
Liquid crystal supply leakage current	I_{LSL}	-2.0	—	+2.0	μA	$V_{in} = V_{EE} - V_{CC}$	6
Driver on resistance	R_{ON}	—	—	7.5	$\text{K}\Omega$	$V_{CC} - V_{EE} = 15 \text{ V}$ $\pm I_{LOAD} = 0.1 \text{ mA}$	7
Dissipation current	$I_{CC(1)}$	—	—	100	μA	During display	8
	$I_{CC(2)}$	—	—	500	μA	During access access cycle = 1 MHz	8

- Notes:
1. Applies to M, FRM, CL, $\overline{\text{RST}}$, ADC, $\phi 1$, and $\phi 2$.
 2. Applies to CS1, CS2, CS3, E, R/W, D/I, and DB0-DB7.
 3. Applies to DB0-DB7.
 4. Applies to terminals except for DB0-DB7.
 5. Applies to DB0-DB7 at high impedance.
 6. Applies to V1L-V4L and V1R-V4R.
 7. Applies to Y1-Y64.
 8. Specified when liquid crystal display is in 1/64 duty.
 Operation frequency: $f_{CLK} = 250 \text{ kHz}$ ($\phi 1$ and $\phi 2$ frequency)
 Frame frequency: $f_M = 70 \text{ Hz}$ (FRM frequency)
 Specified in the state of
 Output terminal: Not loaded
 Input level: $V_{IH} = V_{CC}$ (V)
 $V_{IL} = \text{GND}$ (V)
 Measured at V_{CC} terminal

Interface AC Characteristics

MPU Interface

(GND = 0 V, V_{CC} = 4.5 to 5.5 V, V_{EE} = 0 to -10 V, Ta = -20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Note
E cycle time	t _{CYC}	1000	—	—	ns	1, 2
E high level width	P _{WEH}	450	—	—	ns	1, 2
E low level width	P _{WEL}	450	—	—	ns	1, 2
E rise time	t _r	—	—	25	ns	1, 2
E fall time	t _f	—	—	25	ns	1, 2
Address setup time	t _{AS}	140	—	—	ns	1, 2
Address hold time	t _{AH}	10	—	—	ns	1, 2
Data setup time	t _{DSW}	200	—	—	ns	1
Data delay time	t _{DDR}	—	—	320	ns	2, 3
Data hold time (Write)	t _{DHW}	10	—	—	ns	1
Data hold time (Read)	t _{DHR}	20	—	—	ns	2

Notes: 1.

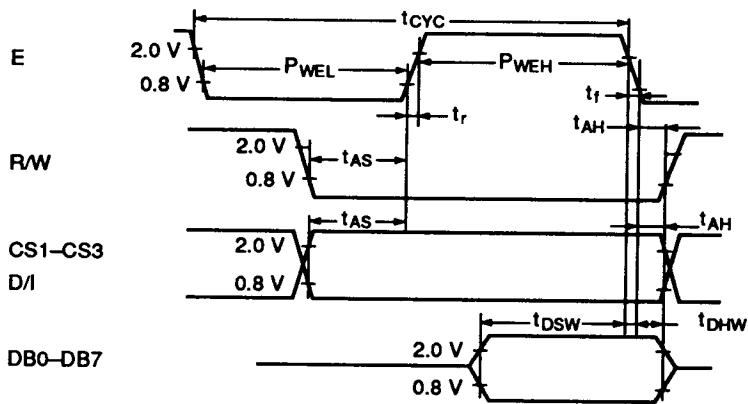


Figure 1 CPU Write Timing

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2.

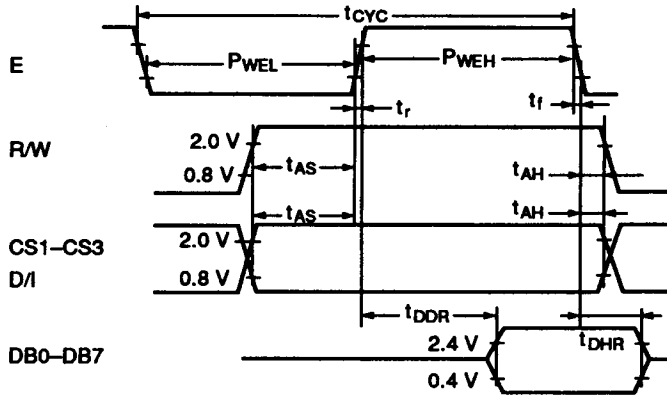
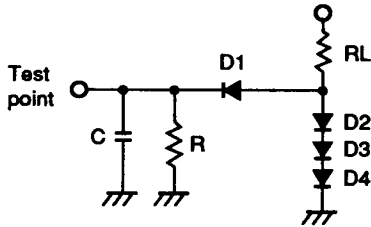


Figure 2 CPU Read Timing

3. DB0-DB7: load circuit



$R_L = 2.4 \text{ k}\Omega$
 $R = 11 \text{ k}\Omega$
 $C = 130 \text{ pF}$ (including jig capacitance)
 Diodes D1 to D4 are all IS2074 (H).

Clock Timing

(GND = 0 V, V_{CC} = 4.5 to 5.5 V, V_{EE} = 0 to -10V, T_a = -20 to +75°C)

Item	Symbol	Limit			Unit	Test Condition
		Min	Typ	Max		
φ1, φ2 cycle time	t _{cyc}	2.5	—	20	μs	Fig. 3
φ1 low level width	t _{WLφ1}	625	—	—	ns	Fig. 3
φ2 low level width	t _{WLφ2}	625	—	—	ns	Fig. 3
φ1 high level width	t _{WHφ1}	1875	—	—	ns	Fig. 3
φ2 high level width	t _{WHφ2}	1875	—	—	ns	Fig. 3
φ1-φ2 phase difference	t _{D12}	625	—	—	ns	Fig. 3
φ2-φ1 phase difference	t _{D21}	625	—	—	ns	Fig. 3
φ1, φ2 rise time	t _r	—	—	150	ns	Fig. 3
φ1, φ2 fall time	t _f	—	—	150	ns	Fig. 3

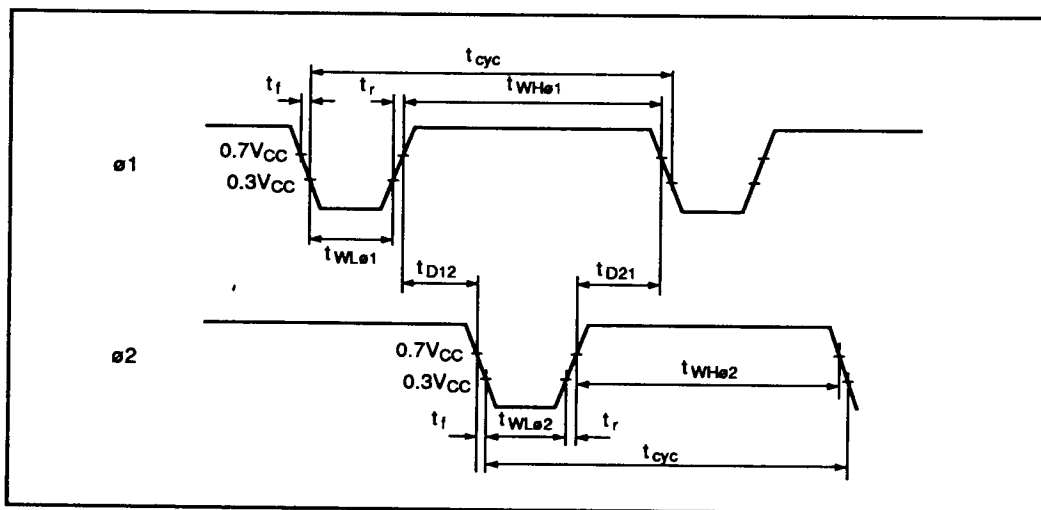


Figure 3 External Clock Waveform

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Display Control Timing

(GND = 0 V, V_{CC} = 4.5 to 5.5 V, V_{EE} = 0 to -10V, Ta = -20 to +75°C)

Item	Symbol	Limit			Unit	Test Condition
		Min	Typ	Max		
FRM delay time	t _{DFRM}	-2	—	+2	μs	Fig. 4
M delay time	t _{DM}	-2	—	+2	μs	Fig. 4
CL low level width	t _{WLCL}	35	—	—	μs	Fig. 4
CL high level width	t _{WHCL}	35	—	—	μs	Fig. 4

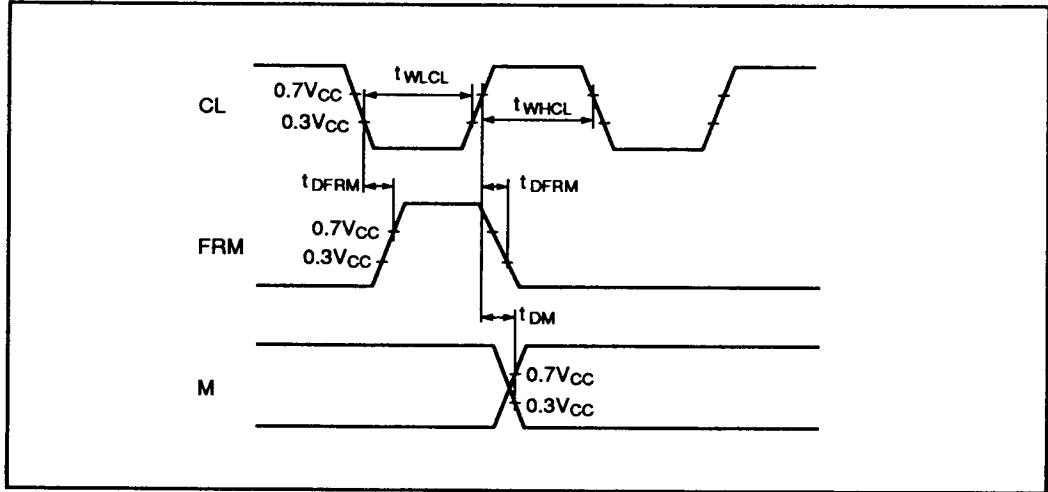


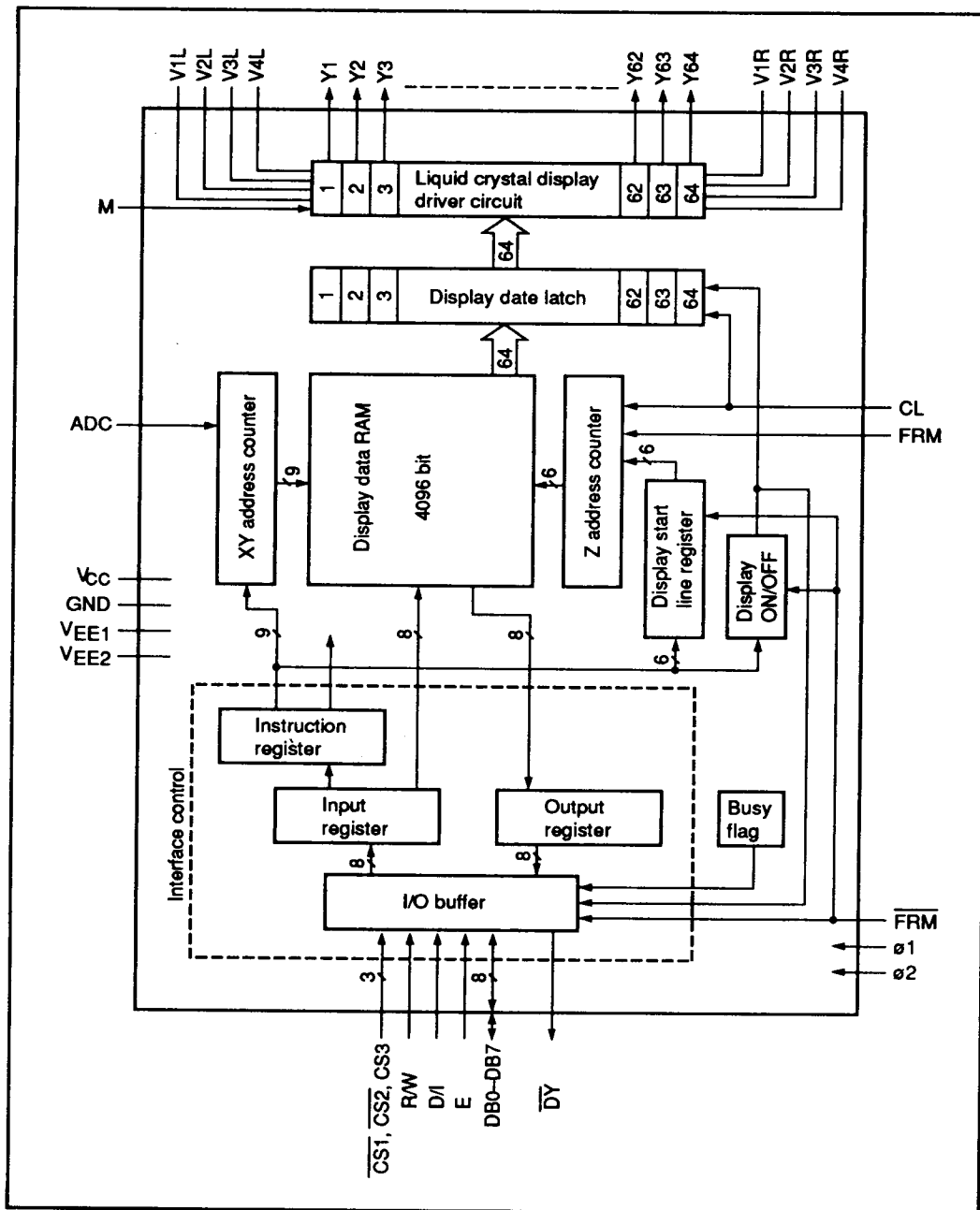
Figure 4 Display Control Signal Waveform

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Block Diagram



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Terminal Functions

Terminal Name	Number of Terminals	I/O	Connected to	Functions
V _{CC} GND	2		Power supply	Power supply for internal logic. Recommended voltage is GND = 0 V V _{CC} = +5 V ± 10%
V _{EE1} V _{EE2}	2		Power supply	Power supply for liquid crystal display drive circuit. Recommended power supply voltage is V _{CC} -15 to GND. Connect the same power supply to V _{EE1} and V _{EE2} . V _{EE1} and V _{EE2} are not connected to each other in the LSI.
V1L, V1R V2L, V2R V3L, V3R V4L, V4R	8		Power supply	Power supply for liquid crystal display drive. Apply the voltage specified for the liquid crystals within the limit of V _{EE} through V _{CC} . V1L (V1R), V2L (V2R): Selection level V3L (V3R), V4L (V4R): Non-selection level Power supplies connected with V1L and V1R (V2L & V2R, V3L & V3R, V4L & V4R) should have the same voltages.
$\overline{CS1}$ $\overline{CS2}$ CS3	3	I	MPU	Chip selection. Data can be input or output when the terminals are in the following conditions: Terminal name $\overline{CS1}$ $\overline{CS2}$ CS3 Condition L L H
E	1	I	MPU	Enable At write (R/W = low): Data of DB0 to DB7 is latched at the fall of E. At read (R/W = high): Data appears at DB0 to DB7 while E is high.
R/W	1	I	MPU	Read/write. R/W = High: Data appears at DB0 to DB7 and can be read by the CPU when E = high, $\overline{CS1}$, $\overline{CS2}$ = low and CS3 = high. R/W = Low: DB0 to DB7 accepted at fall of E when $\overline{CS1}$, $\overline{CS2}$ = low and CS3 = high.
D/I	1	I	MPU	Data/Instruction. D/I = High: Indicates that the data of DB0 to DB7 is display data. D/I = Low: Indicates that the data of DB0 to DB7 is display control data.
ADC	1	I	V _{CC} /GND	Address control signal determine the relation between Y address of display RAM and terminals from which the data is output. ADC = High: Y1-\$0, Y64-\$63 ADC = Low: Y64-\$0, Y1-\$63

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Terminal Functions (cont)

Terminal Name	Number of Terminals	Connected I/O to	Functions
DB0-DB7	8	I/O MPU	Data bus, three-state I/O common terminal.
M	1	I HD61103A	Switch signal to convert liquid crystal drive waveform into AC.
FRM	1	I HD61103A	Display synchronous signal (frame signal). Presets the 6-bit display line counter and synchronizes a common signal with the frame timing when the FRM signal becomes high.
CL	1	I HD61103A	Synchronous signal to latch display data. The rising edge of the CL signal increments the display output address counter and latches the display data.
φ1, φ2	1	I HD61103A	2-phase clock signal for internal operation. The φ1 and φ2 clocks are used to perform operations (I/O of display data and execution of instructions) other than display.
Y1-Y64	64	O Liquid crystal display	Liquid crystal display column (segment) drive output. These pins output light on level when 1 is in the display RAM, and light off level when 0 is in it. Relation among output level, M, and display data (D) is as follows: <div style="text-align: center;"> <p>The diagram shows two digital signals, M and D, over time. M is high for the first two segments and low for the last two. D is high for the first and third segments, and low for the second and fourth. Below, the output level is shown with segments V1, V3, V2, and V4. V1 and V3 are high, while V2 and V4 are low, corresponding to the M signal. The D signal is high during V1 and V3, and low during V2 and V4.</p> </div>
RST	1	I CPU or external CR	The following registers can be initialized by setting the RST signal to low level: <ol style="list-style-type: none"> On/off register set to 0 (display off) Display start line register set to line 0 (displays from line 0) After releasing reset, this condition can be changed only by instruction.
DY	1	O Open	Output terminal for test. Normally, don't connect any lines to this terminal.
NC	2	Open	Unused terminals. Don't connect any lines to these terminals.

Note: 1 corresponds to high level in positive logic.

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Function of Each Block

Interface Control

1. I/O buffer

Data is transferred through 8 data buses (DB0-DB7).

DB7: MSB (most significant bit)

DB0: LSB (least significant bit)

Data can neither be input nor output unless $\overline{CS1}$ to CS3 are in the active mode. Therefore, when $\overline{CS1}$ to CS3 are not in active mode it is useless to switch the signals of input terminals except \overline{RST} and ADC, that is namely, the internal state is maintained and no instruction executes. Besides, pay attention to \overline{RST} and ADC which operate irrespectively by $\overline{CS1}$ to CS3.

2. Register

Both input register and output register are provided to interface to MPU whose the speed is different from that of internal operation. The selection of these registers depend on the combination of R/W and D/I signals.

a. Input Register

The input register is used to store data temporarily before writing it into display data RAM. The data from MPU is written into input register, then into display data RAM automatically by internal operation.

When $\overline{CS1}$ to CS3 are in the active mode and D/I and R/W select the input register as shown in table 1, data is latched at the fall of E signal.

b. Output Register

The output register is used to store data temporarily that is read from display data RAM. To read out the data from the output register, $\overline{CS1}$ to CS3 should be in the active mode and both D/I and R/W should be 1. The read display data instruction outputs data stored in the output register while E is high. Then, at the fall of E, the display data at the indicated address is latched into the output register and the address is increased by 1. The contents in the output register is rewritten with READ instruction, while is held with address set instruction, etc.

Therefore, the data of the specified address cannot be output with the read display data instruction right after the address is set, but can be output at the second read of data. That is to say, one dummy read is necessary. Figure 5 shows the CPU read timing.

Table 1 Register Selection

D/I	R/W	Operation
1	1	Reads data out of output register as internal operation (display data RAM → output register).
1	0	Writes data into input register as internal operation (input register → display data RAM).
0	1	Busy check. Read of status data.
0	0	Instruction.

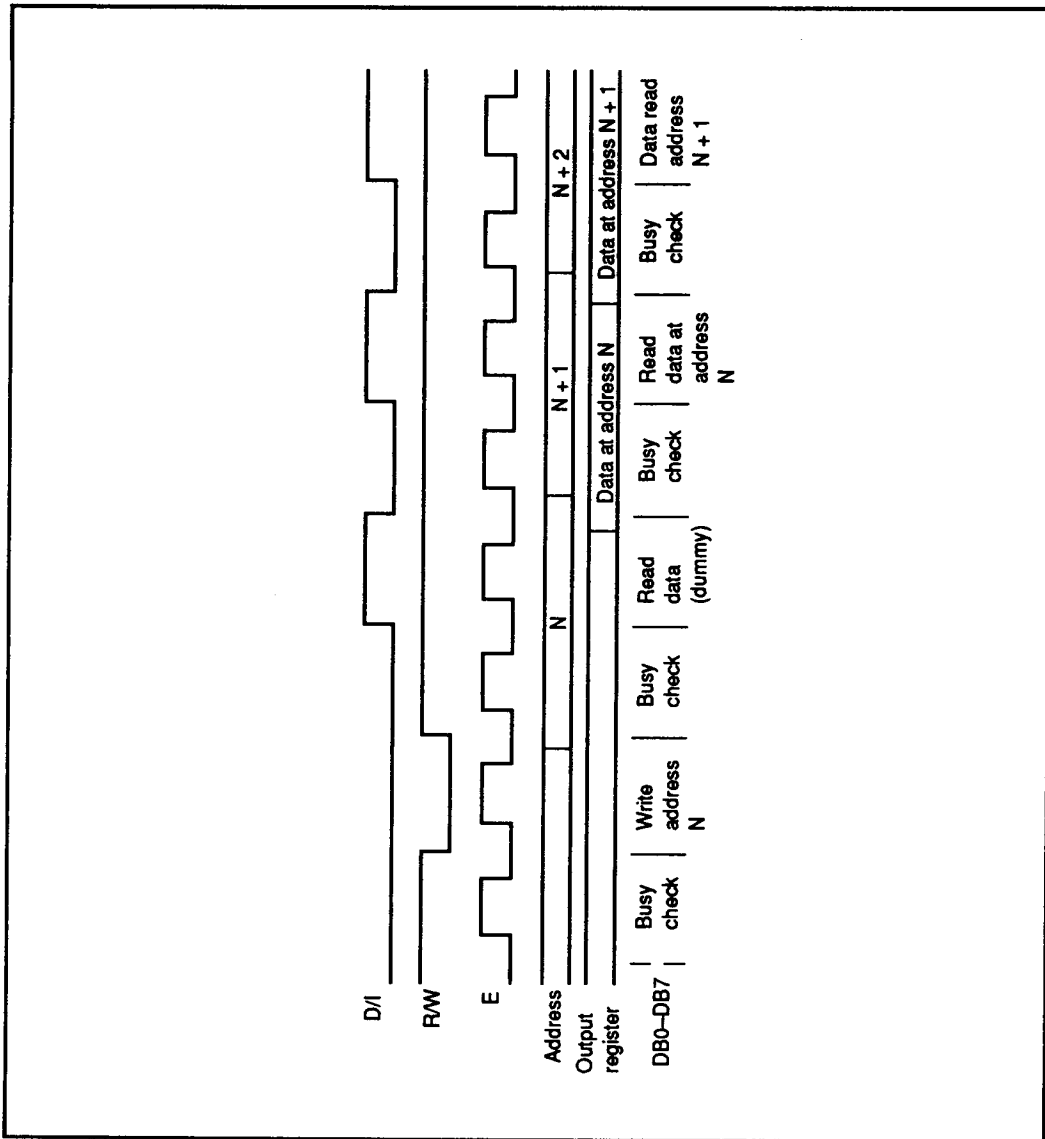


Figure 5 CPU Read Timing

Busy Flag

Busy flag = 1 indicates that HD61102 is operating and no instructions except status read can be accepted (figure 6). The value of the busy flag is

read out on DB7 by the Status Read instruction. Make sure that the busy flag is reset (0) before issuing an instruction.

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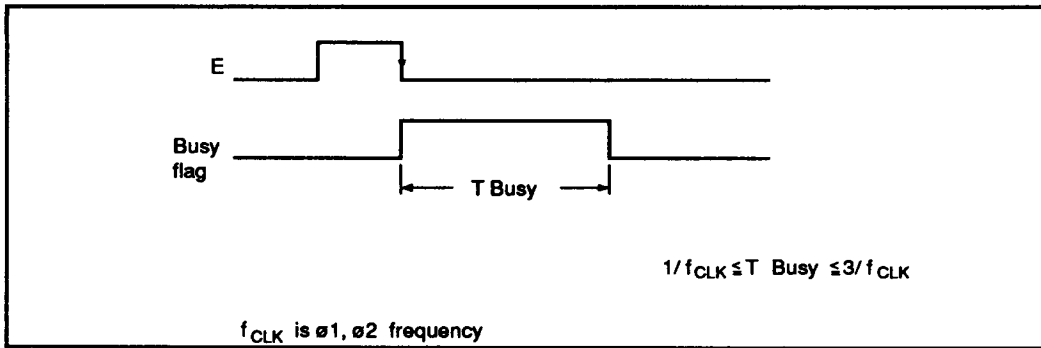


Figure 6 Busy Flag

Display On/Off Flip/Flop

The display On/off flip/flop selects one of two states, on state and off state of segments Y1 to Y64. In on state, the display data corresponding to that in RAM is output to the segments. On the other hand, the display data at all segments disappear in off state independent of the data in RAM. It is controlled by the display on/off instruction. RST signal = 0 sets the segments in off state. The status of the flip/flop is output to DB5 by the status read instruction. The display on/off instruction does not influence data in RAM. To control display data latch by this flip/flop, CI signal (display synchronous signal) should be input correctly.

Display Start Line Register

The register specifies a line in RAM that corresponds to the top line of the LCD panel, when displaying contents in display data RAM on the LCD panel. It is used for scrolling the screen.

6-bit display start line information is written into this register by the display start line set instruction, with high level of FRM signal signalling the start of the display, the information in this register is transferred to the Z address counter, which controls the display address, and the Z address counter is preset.

X, Y Address Counter

A 9-bit counter that designates addresses of internal display data RAM. X address counter (upper 3 bits) and Y address counter (lower 6 bits) should be set by the respective instructions.

1. X address counter

Ordinary register with no count functions. An address is set by instruction.

2. Y address counter

An address is set by instruction and it is increased by 1 automatically by display data R/W operations. The Y address counter loops the values of 0 to 63 to count.

Display Data RAM

Dot data for display is stored in this RAM. 1-bit data of this RAM corresponds to light on (data = 1) and light off (data = 0) of 1 dot in the display panel. The correspondence between Y addresses of RAM and segment PINs can be reversed by ADC signal.

As the ADC signal controls the Y address counter, a reverse of the signal during the operation causes malfunction and destruction of the contents of register and data of RAM. Therefore, always connect ADC pin to V_{CC} or GND when using.

Figure 7 shows the relations between Y address of RAM and segment pins in the cases of ADC = 1 and ADC = 0 (display start line = 0, 1/64 duty cycle).

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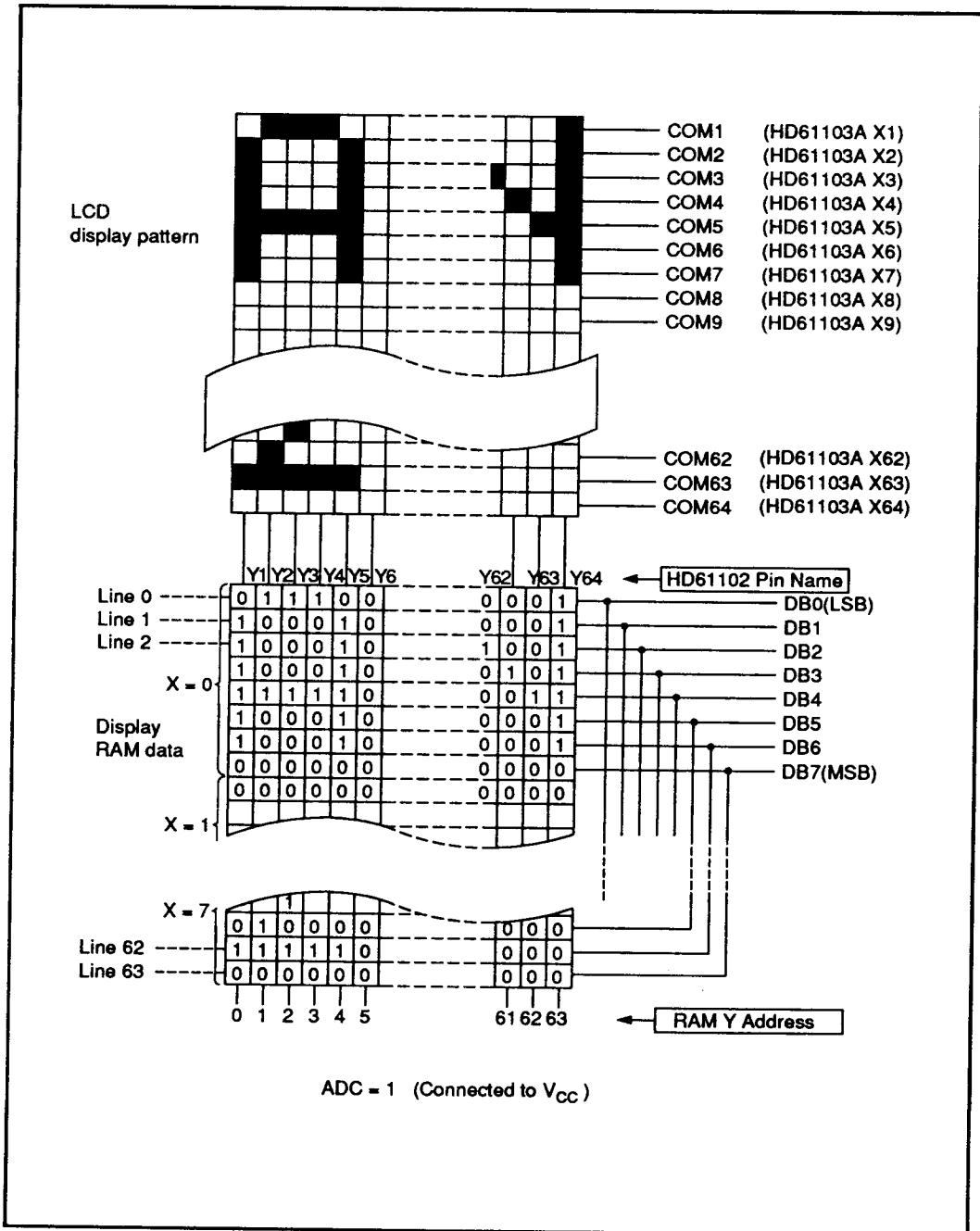


Figure 7 Relation between RAM Data and Display

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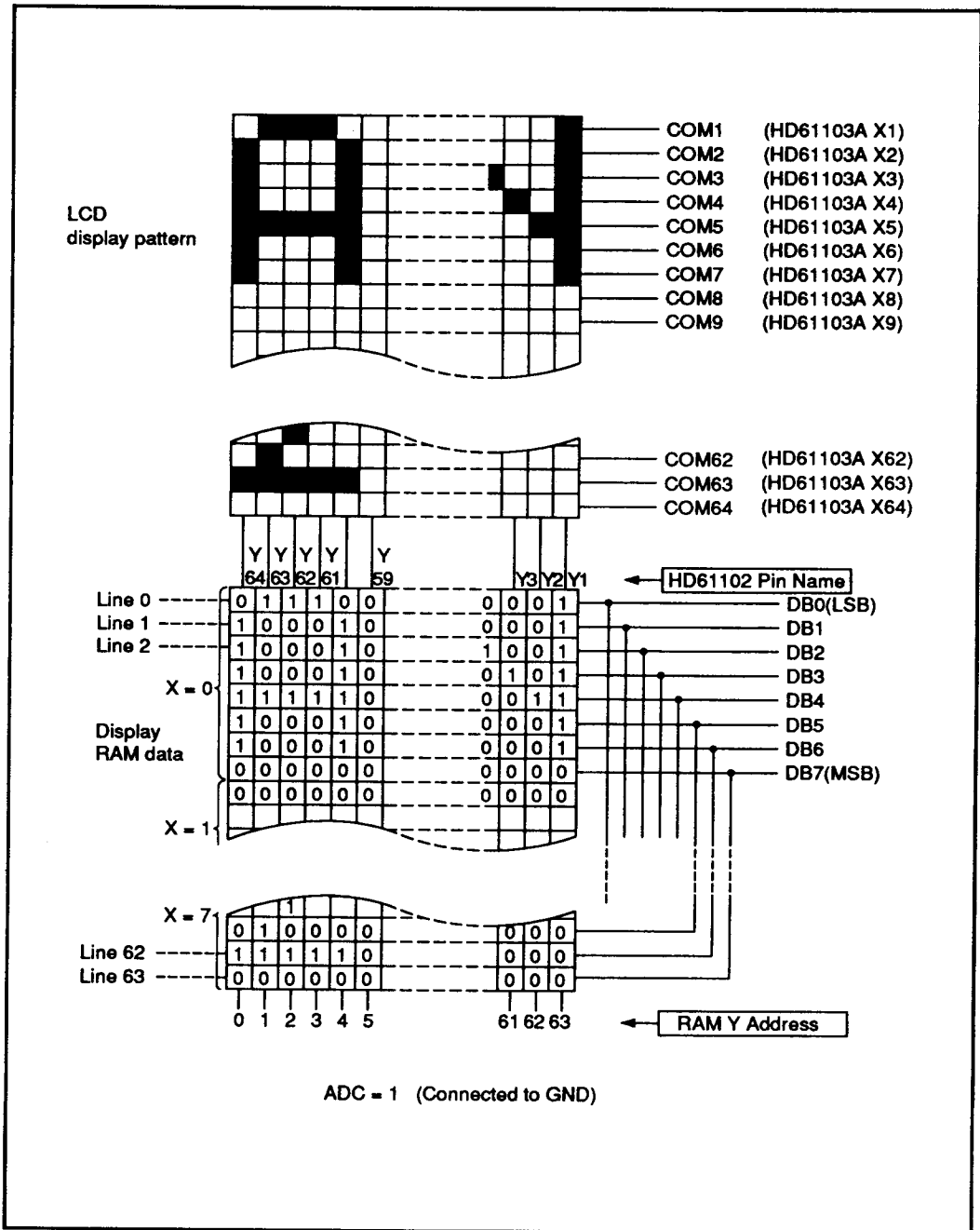


Figure 7 Relation between RAM Data and Display (cont)

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Z Address Counter

The Z address counter generates addresses for outputting the display data synchronized with the common signal. This counter consists of 6 bits and counts up at the fall of the CL signal. At FRM high, the contents of the display start line register are preset in the Z counter.

Display Data Latch

The display data latch stores the display data temporarily that is output from display data RAM to the liquid crystal driving circuit.

Data is latched at the rise of the CL signal. The display on/off instruction controls the data in this latch and does not influence data in display data RAM.

Liquid Crystal Display Driver Circuit

The combination of latched display data and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3, and V4 to be output.

Reset

The system can be initialized by setting \overline{RST} terminal to low when turning power on.

1. Display off
2. Set display start line register line 0

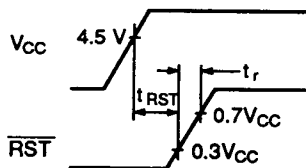
While \overline{RST} is low level, no instruction except status read can be accepted. Therefore, carry out other instructions after making sure that DB4 = 0 (clear RESET) and DB7 = 0 (ready) by status read instruction.

The conditions of the power supply at initial power up are as in table 2.

Table 2 Power Supply Initial Conditions

Item	Symbol	Min	Typ	Max	Unit
Reset time	t_{RST}	1.0	—	—	μs
Rise time	t_r	—	—	200	ns

Do not fail to set the system again because RESET during operation may destroy the data in all the registers except on/off register and in RAM.



Display Control Instructions

Outline

Table 3 shows the instructions. Read/write (R/W) signal, data/instruction (D/I) signal and data bus signals (DB0 to DB7) are also called instructions because the internal operation depends on the signals from MPU.

These explanations are detailed in the following pages. Generally, there are the following three kinds of instructions.

1. Instruction to set addresses in the internal RAM
2. Instruction to transfer data from/to the internal RAM
3. Other instructions

In general use, the second type of instruction are used most frequently. Since Y address of the internal RAM is increased by 1 automatically after writing (reading) data, the program can be shortened. During the execution of an instruction, the system cannot accept instructions other than the status read instruction. Send instructions from MPU after making sure that the busy flag is 0, which is the proof that an instruction is not being executed.

Table 3 Instructions

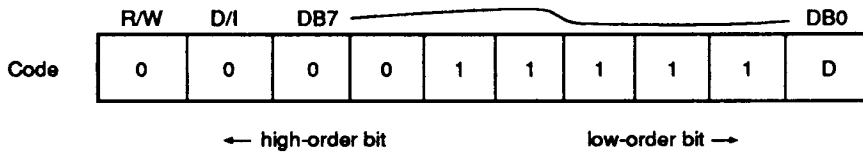
Instructions	Code										Functions
	R/W	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Display on/off	0	0	0	0	1	1	1	1	1	1/0	Controls display on/off. RAM data and internal status are not affected. 1: on, 0: off.
Display start line	0	0	1	1	Display start line (0-63)						Specifies the RAM line displayed at the top of the screen.
Set page (X address)	0	0	1	0	1	1	1	Page (0-7)			Sets the page (X address) of RAM in the page (X address) register.
Set Y address	0	0	0	1	Y address (0-63)						Sets the Y address in the Y address counter.
Status read	1	0	Busy	0	ON/OFF	RE-	0	0	0	0	Reads the status. RESET 1: Reset 0: Normal ON/OFF 1: Display off 0: Display on Busy 1: Executing internal operation 0: Ready
Write display data	0	1	Write data								Writes data DB0 (LSB) to DB7 (MSB) on the data bus into display RAM. Has access to the address of the display RAM specified in advance. After the access, Y address is increased by 1.
Read display data	1	1	Read data								Reads data DB0 (LSB) to DB7 (MSB) from the display RAM to the data bus.

Note: 1. Busy time varies with the frequency (f_{CLK}) of φ₁ and φ₂.
(1/f_{CLK} ≤ T_{BUSY} ≤ 3/f_{CLK})

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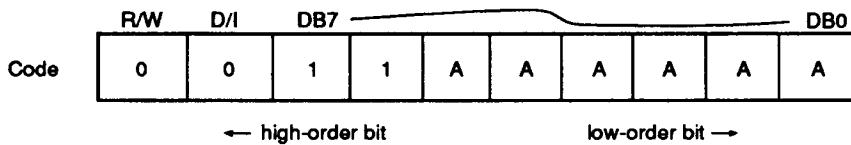
Detailed Explanation

1. Display on/off



The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen when D = 0, it remains in the display data RAM. Therefore, you can make it appear by changing D = 0 into D = 1.

2. Display start line



Z address AAAAAA (binary) of the display data RAM is set in the display start line register and displayed at the top of the screen.

Figure 7 shows examples of display (1/64 duty cycle) when the start line = 0-3. When the display duty cycle is 1/64 or more (ex. 1/32, 1/24 etc.), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

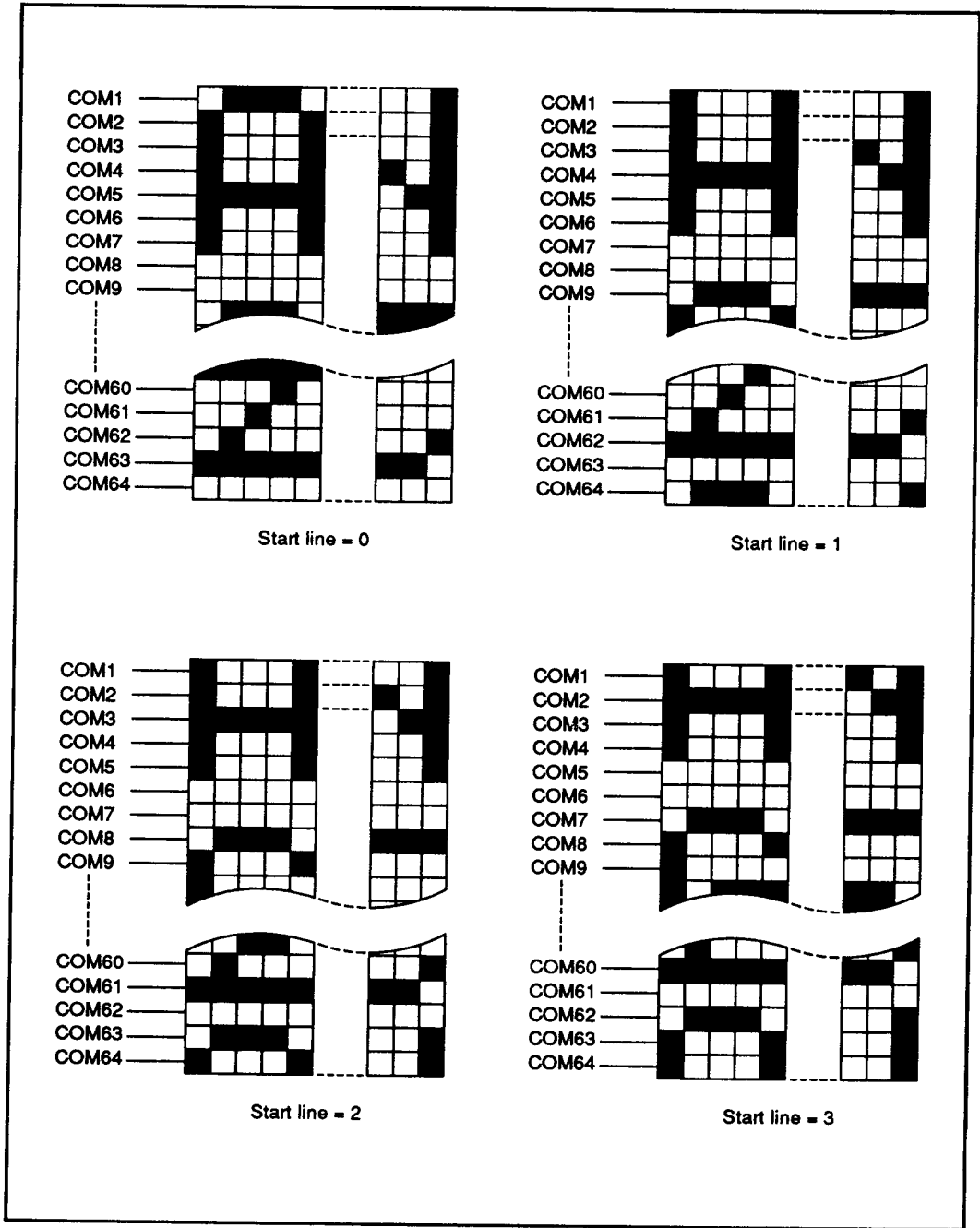
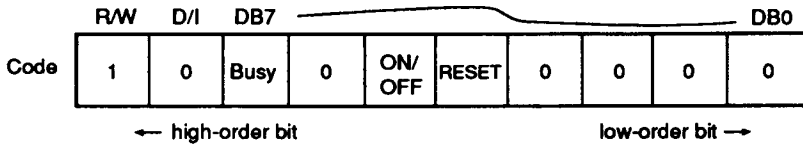


Figure 7 Relation Between Start Line and Display

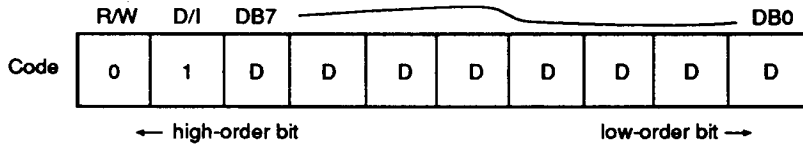
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5. Status Read



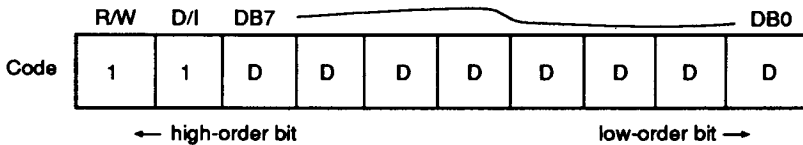
- Busy:** When Busy is 1, the LSI is executing internal operations. No instructions are accepted while Busy is 1, so you should make sure that Busy is 0 before writing the next instruction.
- ON/OFF:** Shows the liquid crystal display conditions: on condition or off condition.
When ON/OFF is 1, the display is in off condition.
When ON/OFF is 0, the display is in on condition.
- RESET:** RESET = 1 shows that the system is being initialized. In this condition, no instructions except status read can be accepted.
RESET = 0 shows that initializing has finished and the system is in the usual operation condition.

6. Write Display Data



Writes 8-bit data DDDDDDDD (binary) into the display data RAM. Then Y address is increased by 1 automatically.

7. Read Display Data



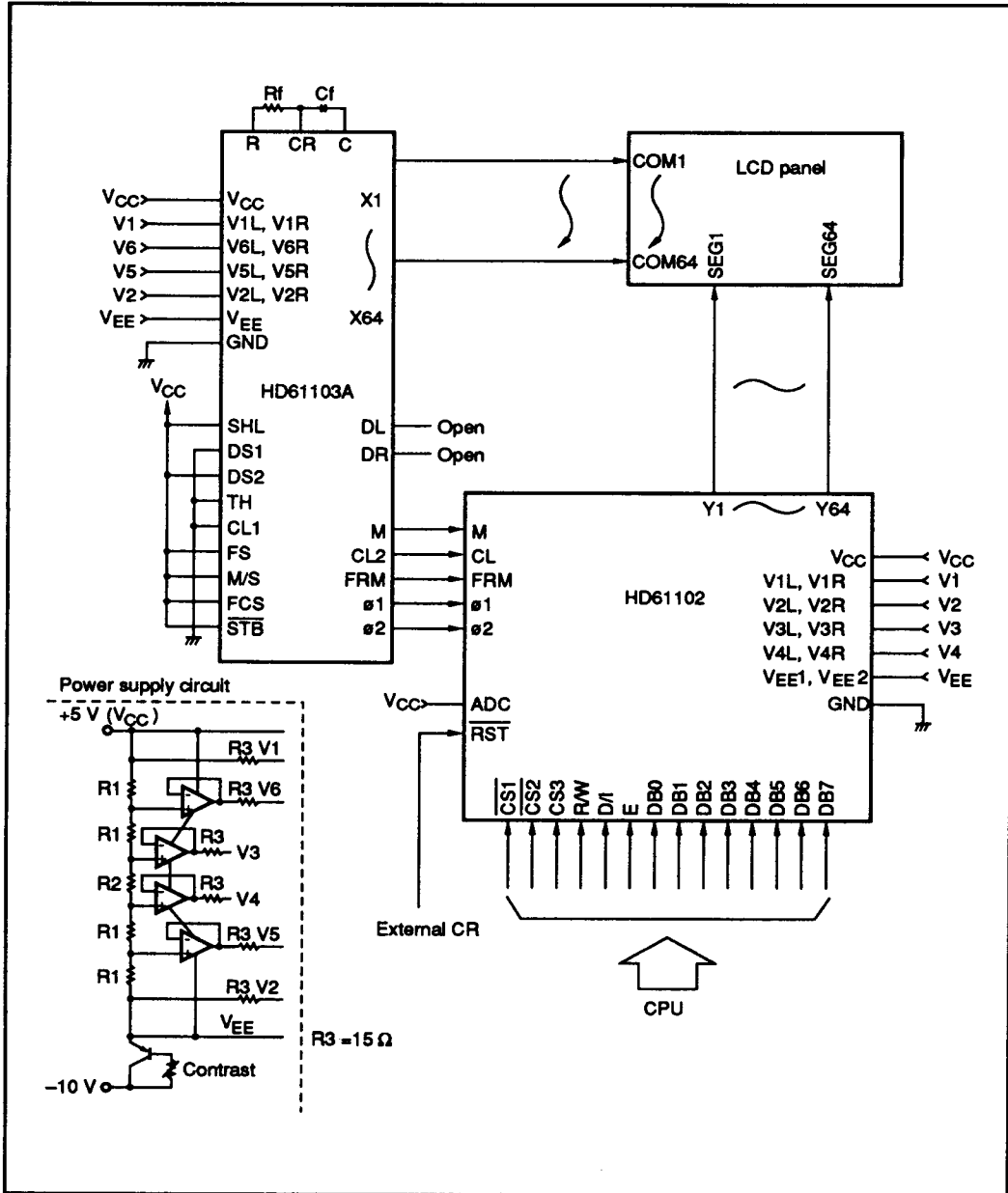
Reads out 8-bit data DDDDDDDD (binary) from the display data RAM. Then Y address is increased by 1 automatically.

One dummy read is necessary right after the address setting. For details, refer to the explanation of output register in "FUNCTION OF EACH BLOCK".

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Use of HD61102

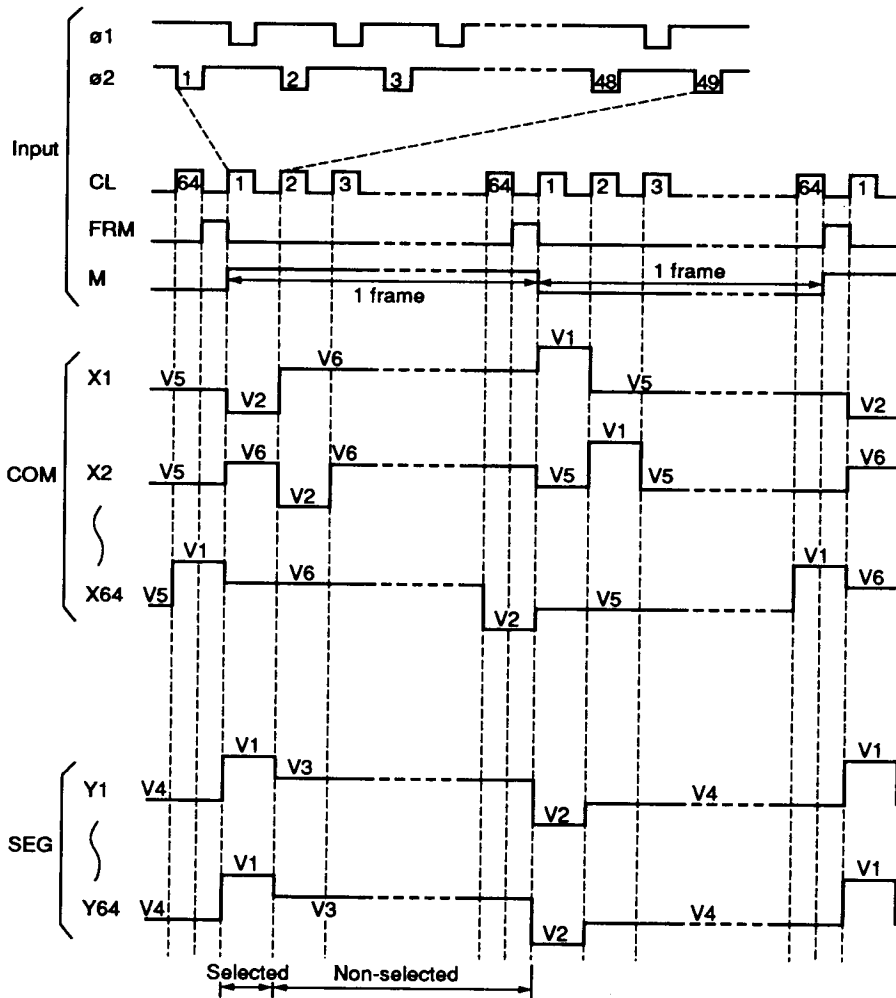
Interface with HD61103A (1/64 duty cycle)



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The waveforms of Y1 to Y64 outputs vary with the display date. In this example, the top line of the panel lights up and other dots do not.

Figure 9 LCD Driver Timing Chart (1/64 duty cycle)

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Interface with CPU

1. Example of connection with HD6800

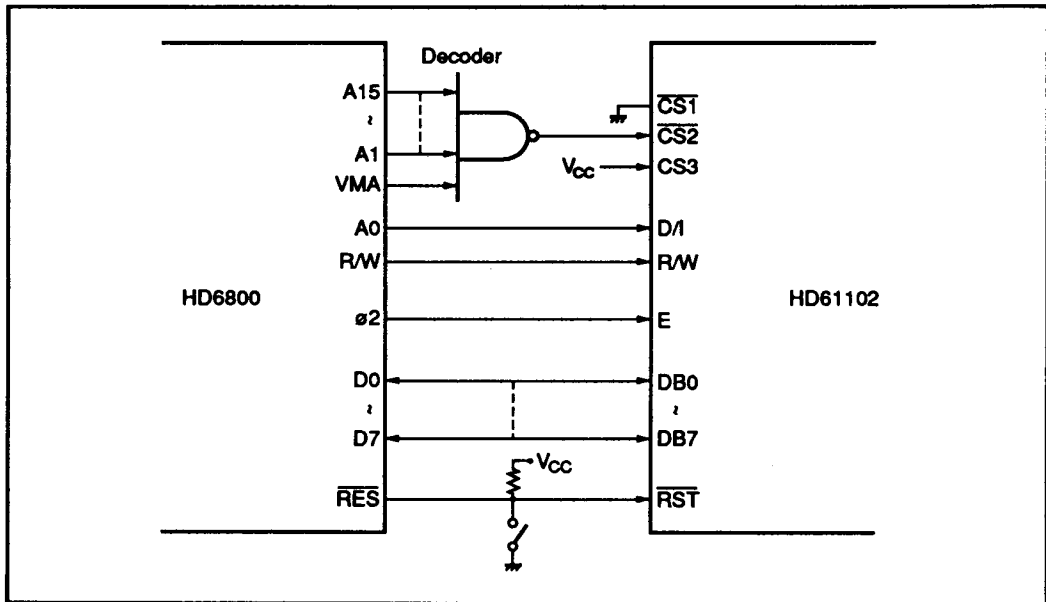


Figure 10 Example of Connection with HD6800 Series

In this decoder (figure 10), addresses of HD61102 in the address area of HD6800 are:

- Read/write of the display data \$FFFF
- Write of display instruction \$FFFE
- Read out of status \$FFFE

Therefore, you can control HD61102 by reading/writing the data at these addresses.

2. Example of connection with HD6801

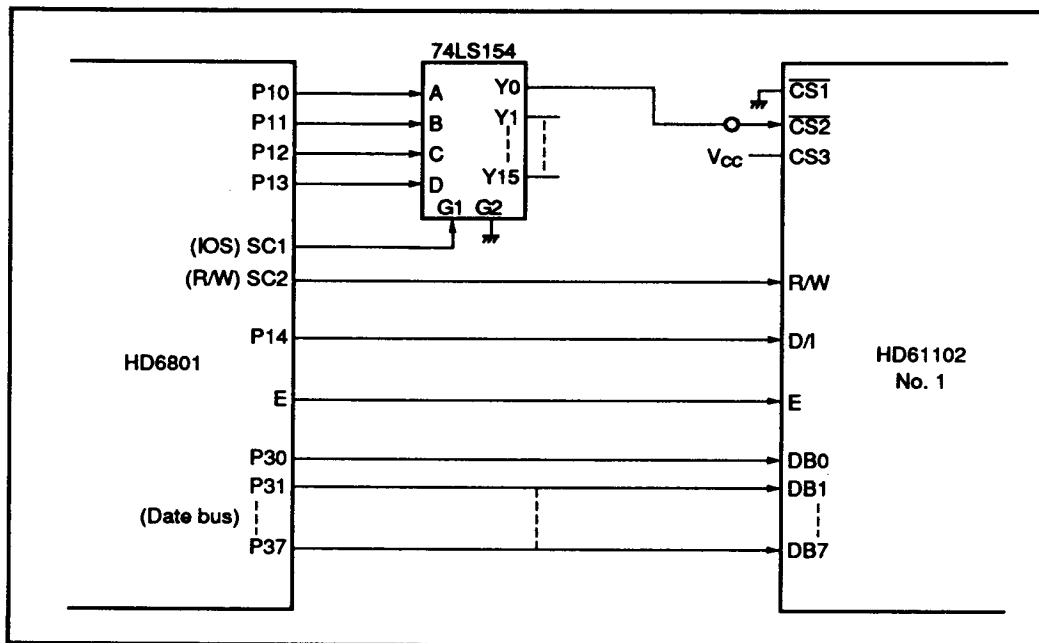


Figure 11 Example of Connection with HD6801

- Set HD6801 to mode 5. P10 to P14 are used as the output port and P30 to P37 as the data bus (table 11).
- 74LS154 4-to-16 decoder generates chip select signal to make specified HD61102 active after decoding 4 bits of P10 to P13.
- Therefore, after enabling the operation by P10 to P13 and specifying D/I signal by P14, read/write from/to the external memory area (\$0100 to \$01FE) to control HD61102. In this case, IOS signal is output from SC1 and R/W signal from SC2.
- For details of HD6800 and HD6801, refer to their manuals.

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Example of Application

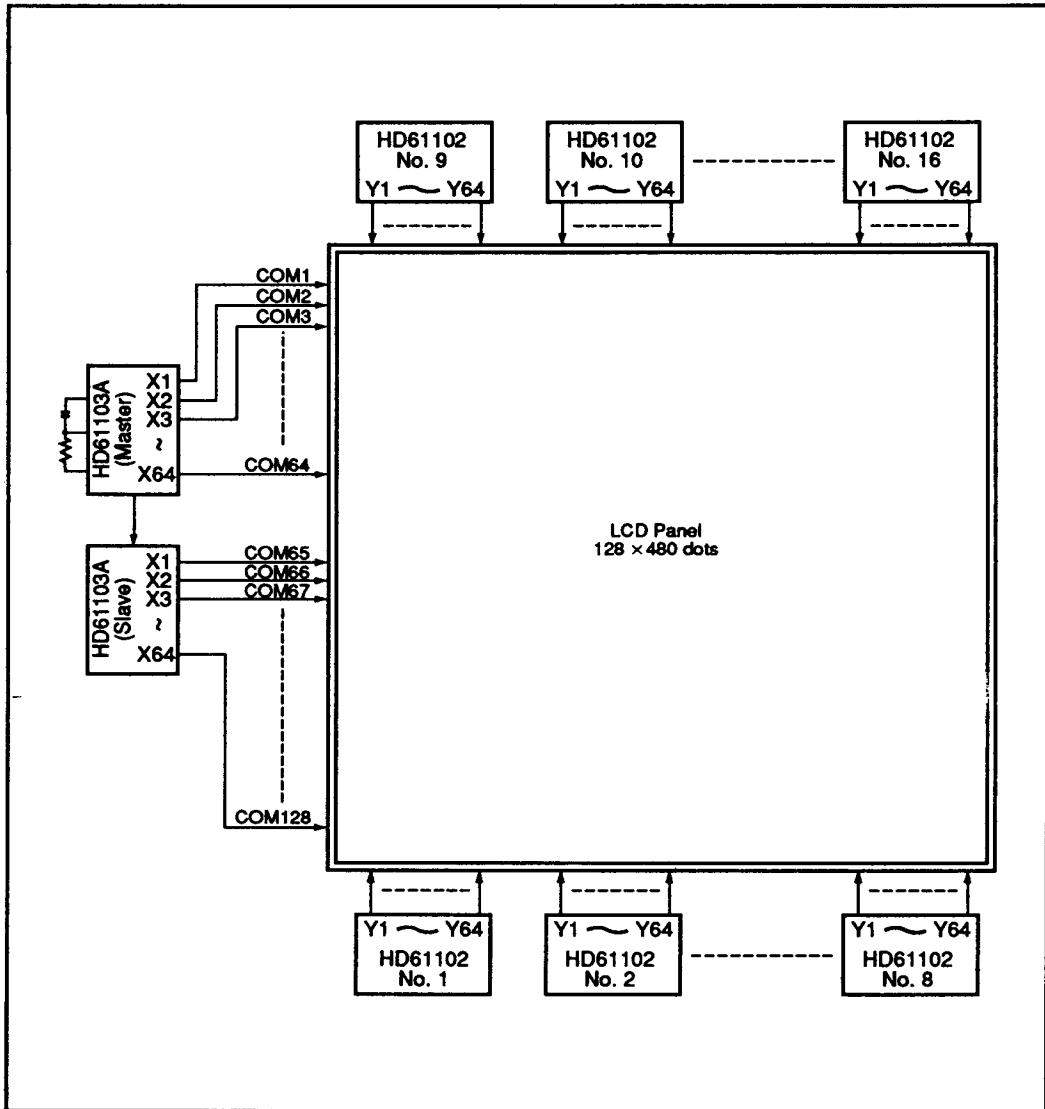


Figure 12 Application Example

Note: In this example (figure 12), two HD61103As output the equivalent waveforms. So, stand-alone operation is possible. In this case, connect COM1 and COM65 to X1, COM2 and COM66 to X2, ..., and COM64 and COM128 to X64. However, for the large screen display, it is better to drive in 2 rows as in this example to guarantee the display quality.

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