IH5341, IH5352

Dual SPST, Quad SPST CMOS RF/Video Switches

December 1993

Features

- $R_{DS(ON)} < 75\Omega$
- **Switch Attenuation Varies Less Than 3dB From DC to 100MHz**
- **"OFF" Isolation > 70dB Typical at 10MHz**
- **Cross Coupling Isolation > 60dB at 10MHz**
- **Compatible With TTL, CMOS Logic**
- **Wide Operating Power Supply Range**
- **Power Supply Current < 1μA**
- **"Break-Before-Make" Switching**
- **Fast Switching (80ns/150ns Typ)**

Applications

- **Video Switch**
- **Communications Equipment**
- **Disk Drives**
- **Instrumentation**
- **CATV**

Description

The IH5341 (IH5352) is a dual (quad) SPST, CMOS monolithic switch which uses a "Series/Shunt" ("T" switch) configuration to obtain high "OFF" isolation while maintaining good frequency response in the "ON" condition.

Construction of remote and portable video equipment with extended battery life is facilitated by the extremely low current requirements. Switching speeds are typically t_{ON} = 150ns and t_{OFF} = 80ns. "Break-Before-Make" switching is guaranteed.

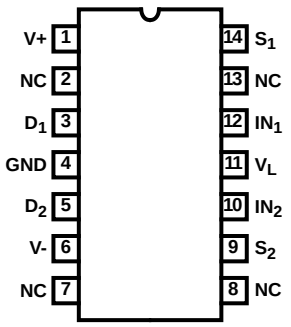
Switch "ON" resistance is typically 40Ω - 50Ω with ±15V power supplies, increasing to typically 175Ω for ±5V supplies.

Ordering Information

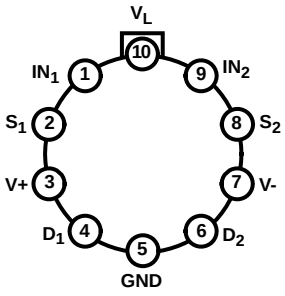
PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH5341CPD	0°C to +70°C	14 Lead Plastic DIP
IH5341ITW	-25°C to +85°C	10 Pin TO-100 Can
IH5341MTW	-55°C to +125°C	10 Pin TO-100 Can
IH5341MTW/883B	-55°C to +125°C	10 Pin TO-100 Can
IH5352CPE	0°C to +70°C	16 Lead Plastic DIP
IH5352IJE	-25°C to +85°C	16 Lead Ceramic DIP
IH5352MJE	-55°C to +125°C	16 Lead Ceramic DIP
IH5352MJE/883B	-55°C to +125°C	16 Lead Ceramic DIP
IH5352CBP	0°C to +70°C	20 Lead SOIC
IH5352IBP	-25°C to +85°C	20 Lead SOIC

Pinouts

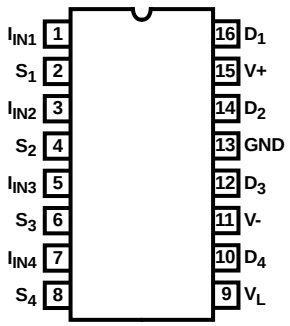
IH5341 (PDIP) TOP VIEW



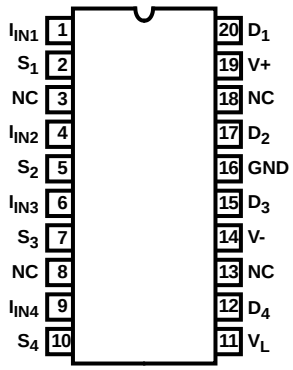
IH5341 (TO-100 CAN) TOP VIEW



IH5352 (CDIP, PDIP) TOP VIEW



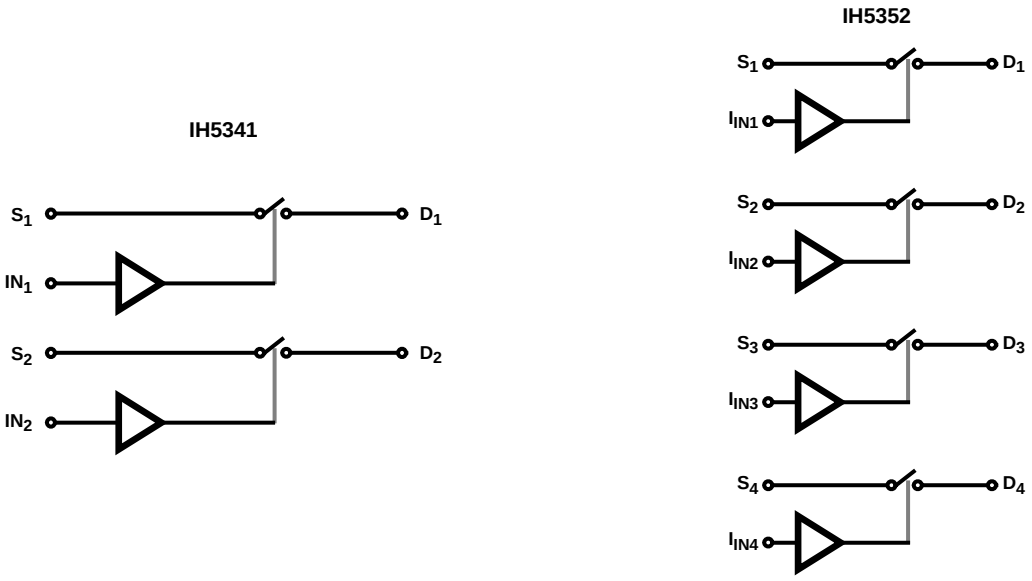
IH5352 (SOIC) TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

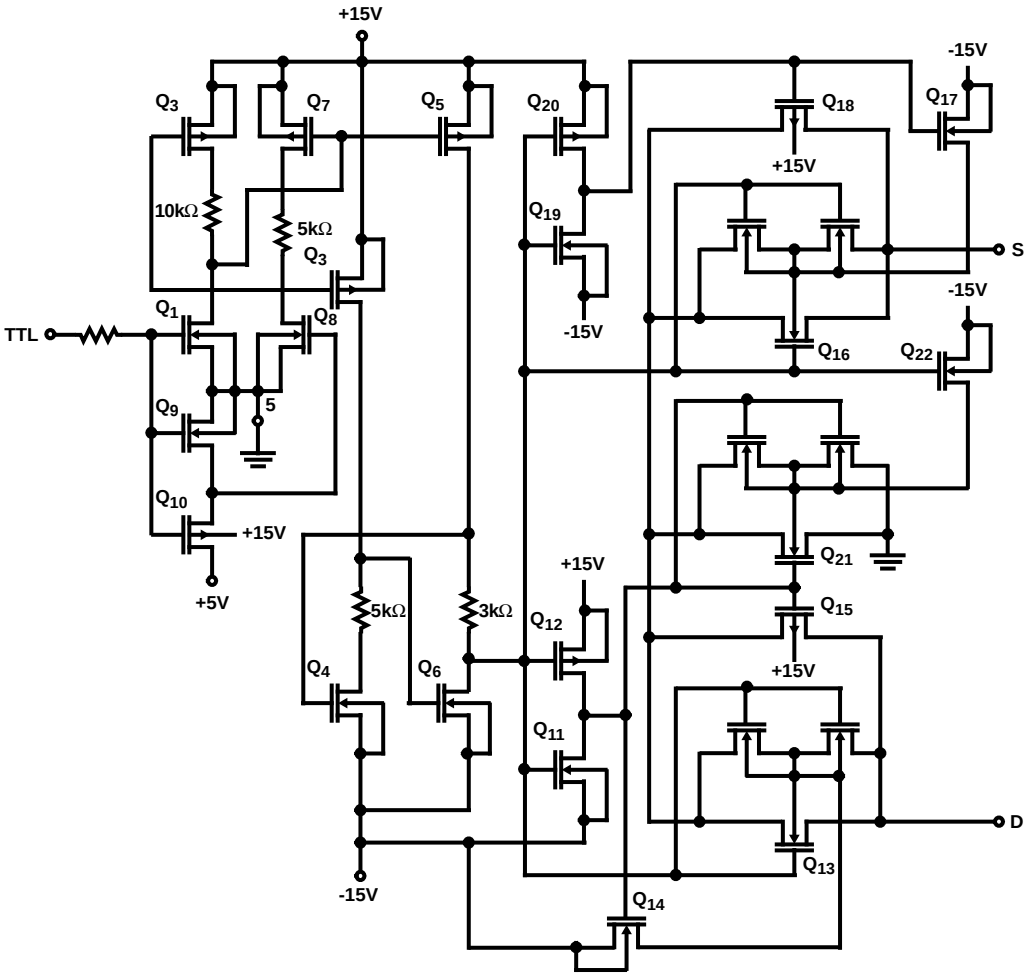
File Number **3134**

Functional Block Diagrams



Switches are open for a logic “0” control input, and closed for a logic “1” control input.

Schematic Diagram ($^1/_2$ IH5341, $^1/_4$ IH5352)



Absolute Maximum Ratings

V+ to Ground . . . . . +18V
V- to Ground . . . . . -18V
V_L to Ground. . . . . V+ to V-
Logic Control Voltage . . . . . V+ to V-
Analog Input Voltage . . . . . V+ to V-
Current (Any Terminal) 50mA
Storage Temperature . . . . . -65^oC to $+150^oC$
Lead Temperature (Soldering, 10s) . . . . . $+300^oC$

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package	$70^oC/W$	$19^oC/W$
TO-100 Can Package	$136^oC/W$	$65^oC/W$
SOIC Package	$120^oC/W$	-
Plastic DIP Package	$100^oC/W$	-

Operating Temperature
(M Version) . . . . . -55^oC to $+125^oC$
(I Version) . . . . . -25^oC to $+85^oC$
(C Version). . . . . 0^oC to $+70^oC$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$V+ = +15V$, $V_L = +5V$, $V- = -15V$, $T_A = +25^oC$ Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS		(NOTE 1) TYP	M GRADE DEVICE			I/C GRADE DEVICE			UNITS
				-55^oC	$+25^oC$	$+125^oC$	-25^oC/ 0^oC	$+25^oC$	$+85^oC$/ $+70^oC$	
DC CHARACTERISTICS										
Supply Voltage Ranges (Note 3)										
Positive Supply, V+			5 to 15	-	-	-	-	-	-	V
Logic Supply, V_L			5 to 15	-	-	-	-	-	-	V
Negative Supply, V-			-5 to -15	-	-	-	-	-	-	V
Switch "ON" Resistance, $R_{DS(ON)}$	$V_D = \pm5V$, $I_S = 10mA$, $V_{IN} \geq 2.4V$ (Note 4)		50	75	75	100	75	75	100	Ω
	$V_D = \pm10V$, $I_S = 10mA$, $V_{IN} \geq 2.4V$ (Note 4)		100	125	125	cd175	150	150	175	Ω
Switch "ON" Resistance, $R_{DS(ON)}$	$V+ = V_L = +5V$, $V_{IN} = 3V$, $V- = -5V$, $V_D = \pm3V$, $I_S = 10mA$		175	250	250	350	300	300	350	Ω
On Resistance Match Between Channels, $\Delta R_{D-S(ON)}$	$I_S = 10mA$, $V_D = \pm5V$		5	-	-	-	-	-	-	Ω
Logic "I" Input Voltage, V_{IH}			>2.4	-	-	-	-	-	-	V
Logic "0" Input Voltage, V_{IL}			<0.8	-	-	-	-	-	-	V
Switch "OFF" Leakage, $I_{D(OFF)}$ or $I_{S(OFF)}$	$V_{S/D} = \pm5V$ or $\pm14V$, $V_{IN} \leq 0.8V$ (Notes 2 and 4)	IH5341	-	-	±0.5	50	-	±1	100	nA
		IH5352	-	-	±1	50	-	±2	100	nA
Switch "ON" Leakage, $I_{D(ON)} + I_{S(ON)}$	$V_{S/D} = \pm5V$, $V_{IN} \geq 2.4V$	IH5341	-	-	±1	50	-	±2	100	nA
	$V_{S/D} = \pm14V$, $V_{IN} \geq 2.4V$		-	-	±1	100	-	±2	100	nA
	$V_{S/D} = \pm5V$ or $\pm14V$, $V_{IN} \leq 0.8V$	IH5352	-	-	±1	100	-	±2	100	nA
Input Logic Current, I_{IN}	$V_{IN} > 2.4V$ or $< 0V$		0.1	±1	±1	10	±1	±1	10	mA
Positive Supply Quiescent Current, I+	$V_{IN} = 0V$ or $+5V$		0.1	1	1	10	1	1	10	mA
Negative Supply Quiescent Current, I-	$V_{IN} = 0V$ or $+5V$		0.1	1	1	10	1	1	10	µA
Logic Supply Quiescent Current, I_L	$V_{IN} = 0V$ or $+5V$		0.1	1	1	10	1	1	10	µA

Electrical Specifications V+ = +15V, V_L = +5V, V- = -15V, T_A = +25°C Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 1) TYP	M GRADE DEVICE			I/C GRADE DEVICE			UNITS
			-55°C	+25°C	+125°C	-25°C/ 0°C	+25°C	+85°C/ +70°C	
AC CHARACTERISTICS									
Switch "ON" Time, t_{ON}		-	-	150	300	-	-	-	ns
Switch "OFF" Time, t_{OFF}		-	-	80	150	-	-	-	ns
"OFF" Isolation Rejection Ratio, OIRR		-	-	70	-	-	-	-	dB
Cross Coupling Rejection Ratio, CCRR		-	-	60	-	-	-	-	dB
Switch Attenuation 3dB Frequency, f_{3dB}		-	-	100	-	-	-	-	MHz

NOTES:

1. Typical values are not tested in production. They are given as a design aid only.
2. Positive and negative voltages applied to opposite sides of switch, in both directions successively.
3. These are the operating voltages at which the other parameters are tested, and are not directly tested.
4. The logic inputs are either greater than or equal to 2.4V or less than or equal to 0.8V, as required, for this test.

Typical Performance Curves

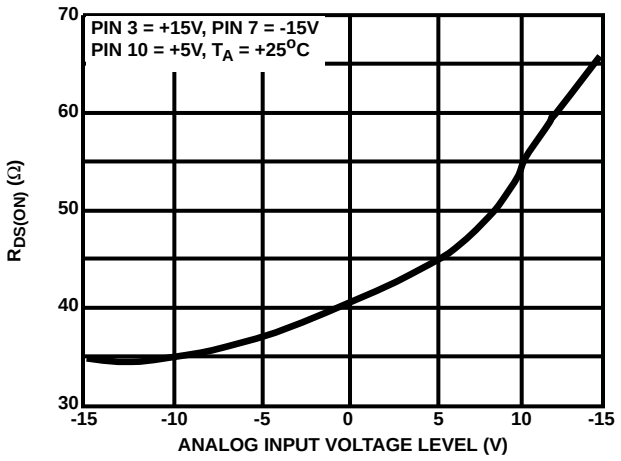


FIGURE 1. $R_{DS(ON)}$ vs ANALOG INPUT VOLTAGE WITH ±15V POWER SUPPLIES

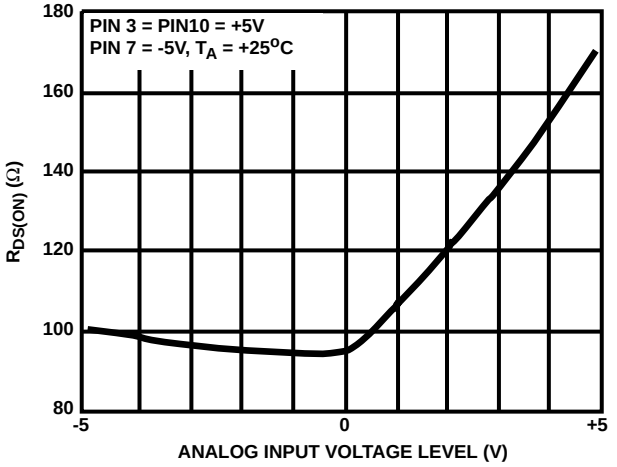


FIGURE 2. $R_{DS(ON)}$ vs ANALOG INPUT LEVEL WITH ±5V POWER SUPPLIES

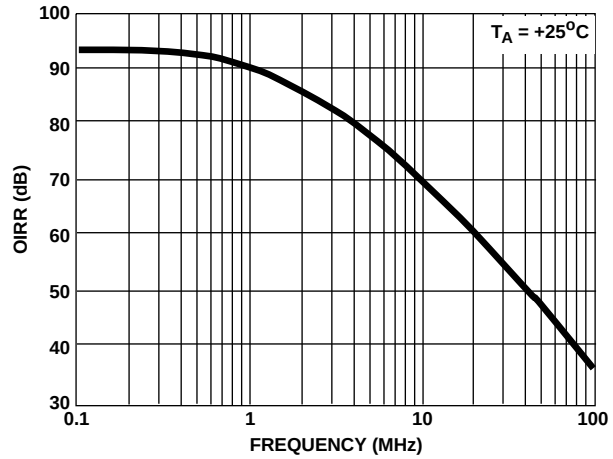


FIGURE 3. OFF ISOLATION REJECTION vs FREQUENCY (SEE FIGURE 8)

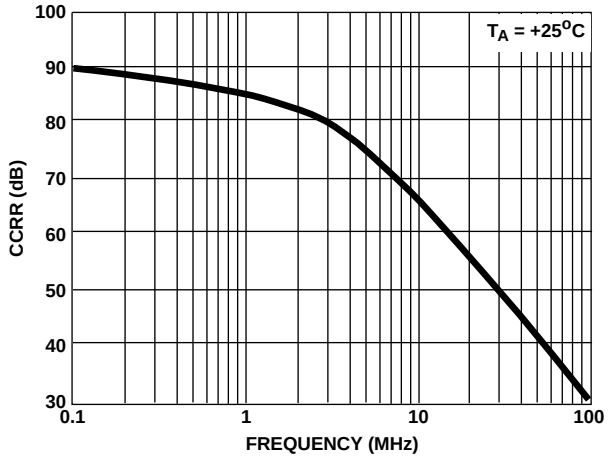


FIGURE 4. CROSS COUPLING REJECTION vs FREQUENCY (SEE FIGURE 9)

Typical Performance Curves (Continued)

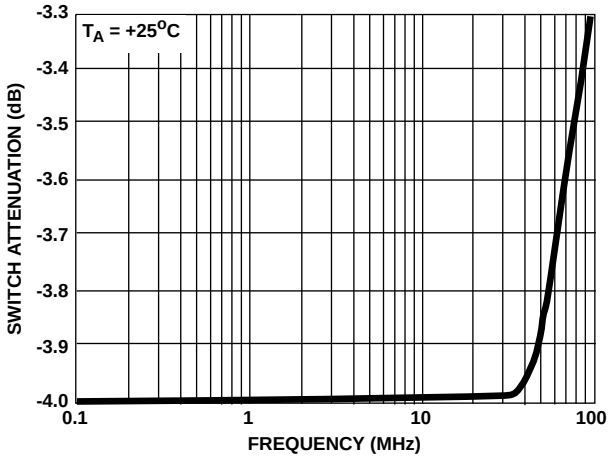
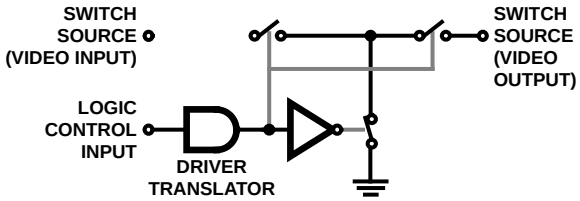


FIGURE 5. TYPICAL SWITCH ATTENUATION vs FREQUENCY (R_L = 75Ω, SEE FIGURE 10)

Detailed Description

Figure 6 shows the internal circuit of one channel of the IH5352. This is identical to the IH5341 "T-Switch" configuration. Here, a shunt switch is closed, and the two series switches are open when the video switch channel is open or off. This provides much better isolation between the input and output terminals than a simple series switch does, especially at high frequencies. The result is excellent off-isolation in the Video and RF frequency ranges when compared to conventional analog switches.

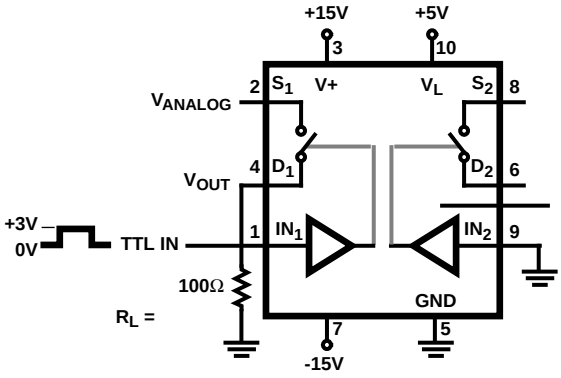
The control input level shifting circuitry is very similar to that of the IH5140 series of Analog Switches, and gives very high speed, guaranteed "Break-Before-Make" action, low static power consumption and TTL compatibility.



NOTE: 1 channel of 4 shown.

FIGURE 6. INTERNAL SWITCH CONFIGURATION

Test Circuits



NOTE: Only one channel shown. Other acts identically.

FIGURE 7A. SWITCHING TIME TEST CIRCUIT

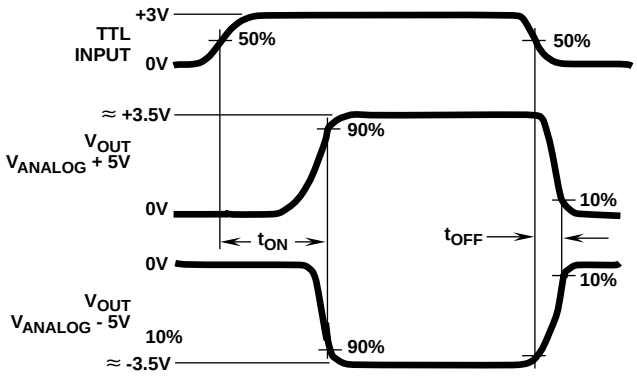
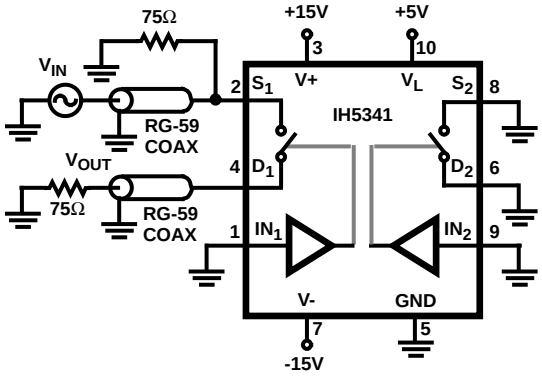


FIGURE 7B. SWITCHING TIME WAVEFORMS

FIGURE 7.

Test Circuits (Continued)

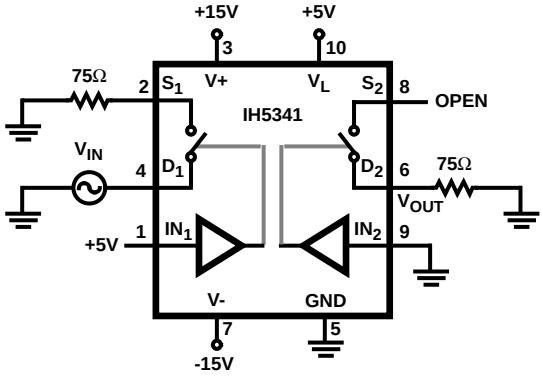


V_{IN} = ±5V (10V_{P-P}) at f = 10MHz

$$OIRR = 20\log\frac{V_{IN}}{V_{OUT}}$$

NOTE: Only one channel shown. Other acts identically.

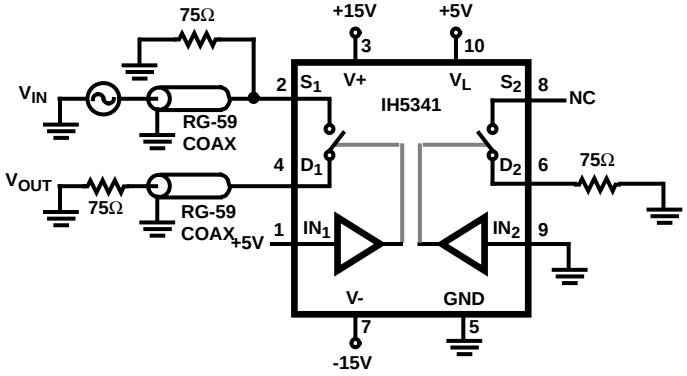
FIGURE 8. OFF ISOLATION TEST CIRCUIT



V_{IN} = 225mV_{RMS} at f = 10MHz

$$CCRR = 20\log\frac{V_{IN}}{V_{OUT}}$$

FIGURE 9. OFF ISOLATION TEST CIRCUIT



$$ATTN: = 20\log\frac{R_L}{R_{DS(ON)} + R_L}$$

Nominally, at DC, this ratio is equal to -4dB. When the attenuation reaches -1dB, the frequency at which this occurs is f_{3dB}

NOTE: Only one channel shown. Other acts identically.

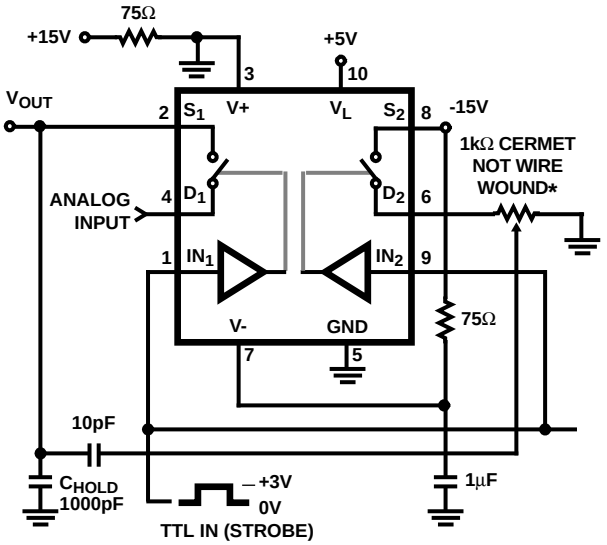
FIGURE 10. SWITCH ATTENUATION vs FREQUENCY

Typical Applications

Charge Compensation Techniques

Charge injection results from the signals out of the level translation circuit being coupled through the gate-channel and gate-source/drain capacitances to the switch inputs and outputs. This feedthrough is particularly troublesome in Sample-and-Hold or Track-and-Hold applications, as it causes a Sample (Track) to Hold offset. The IH5341 devices have a typical injected charge of 30pC-50pC (corresponding to 30mV-50mV in a 1000pF capacitor), at $V_{S/D}$ of about 0V.

This Sample (Track) to Hold offset can be compensated by bringing in a signal equal in magnitude but of the opposite polarity. The circuit of Figure 11 accomplishes this charge injection compensation by using one side of the device as a S & H (T & H) switch, and the other side as a generator of a compensating signal. The 1kΩ potentiometer allows the user to adjust the net injected charge to exactly zero for any analog voltage in the -5V to +5V range.



* Adjust pot for $0mV_{P-P}$ steip at V_{OUT} with no analog (AC) signal present.

FIGURE 11. CHARGE INJECTION COMPENSATION

Since individual parts are very consistent in their charge injection, it is possible to replace the potentiometer with a pair of fixed resistors, and achieve less than 5mV error for all devices without adjustment.

An alternative arrangement, using a standard TTL inverter to generate the required inversion, is shown in Figure 12. The capacitor needs to be increased, and becomes the only method of adjustment. A fixed value of 22pF is good for analog values referred to ground, while 35pF is optimum for AC coupled signals referred to -5V as shown in the figure. The choice of -5V is based on the virtual disappearance at this analog level of the transient component of switching charge injection. This combination will lead to a virtually “glitch-free” switch.

Overvoltage Protection

If sustained operation with no supplies but with analog signals applied is possible, it is recommended that diodes (such as 1N914) be inserted in series with the supply lines to the IH5341. Such conditions can occur if these signals come from a separate power supply or another location, for example. The diodes will be reverse biased under this type of operation, preventing heavy currents from flowing from the analog source through the IH5341.

The same method of protection will provide over 25V overvoltage protection on the analog inputs when the supplies are present. The schematic for this connection is shown in Figure 13.

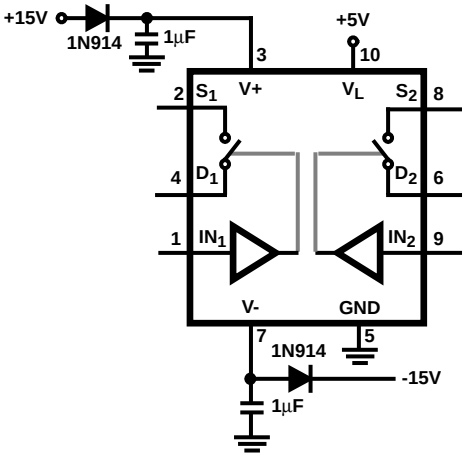


FIGURE 13. OVERVOLTAGE PROTECTION

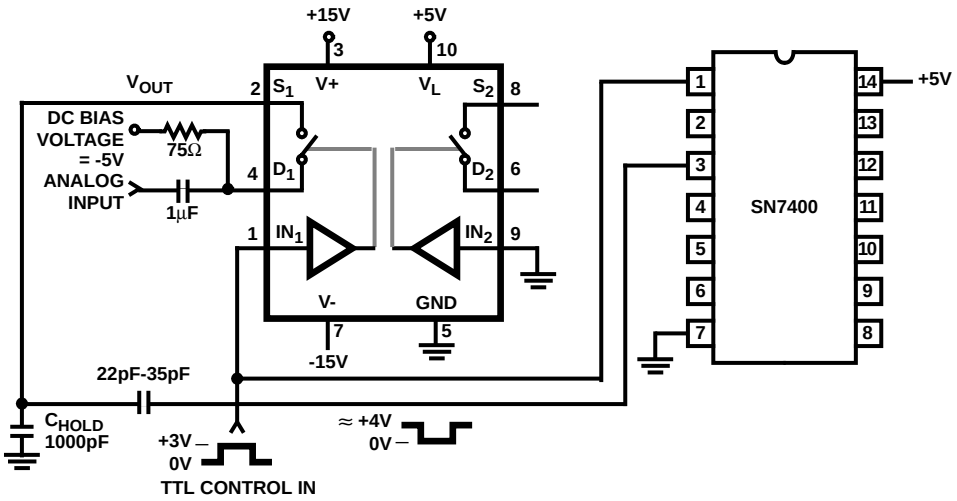


FIGURE 12. ALTERNATIVE COMPENSATION CIRCUIT

Die Characteristics

DIE DIMENSIONS:
2388µm x 2515µm

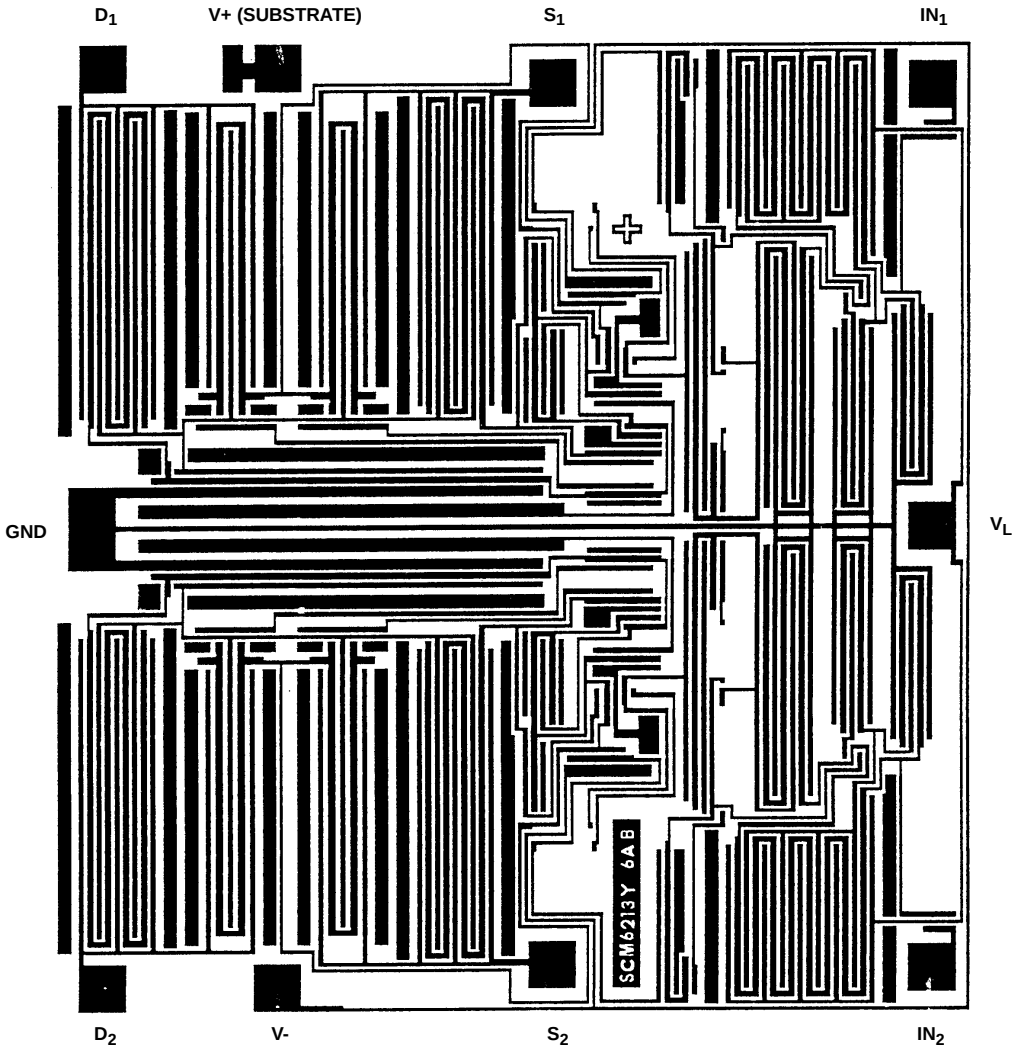
METALLIZATION:
Type: Al
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: PSG/Nitride
PSG Thickness: 7kÅ ± 1.4kÅ
Nitride Thickness: 8kÅ ± 1.2kÅ

WORST CASE CURRENT DENSITY:
9.1×10^4 A/cm^2

Metallization Mask Layout

IH5341



Die Characteristics

DIE DIMENSIONS:
2617µm x 5233µm

METALLIZATION:
Type: Al
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: PSG/Nitride
PSG Thickness: 7kÅ ± 1.4kÅ
Nitride Thickness: 8kÅ ± 1.2kÅ

WORST CASE CURRENT DENSITY:
9.1×10^4 A/cm^2

Metallization Mask Layout

IH5352