Data Sheet | June 13, 2013 | FN8093.4

5 Ld Voltage Supervisors with Adjustable Power-On Reset, Dual Voltage Monitoring or Watchdog Timer Capability

The ISL88011, ISL88012, ISL88013, ISL88014, ISL88015 family of devices offer both fixed and/or adjustable voltage-monitoring that combine popular functions such as Power-On reset control, watchdog timer, supply voltage supervision, and manual reset assertion in a small 5 Ld SOT-23 package.

Unique features on the ISL88013 and ISL88015 include a watchdog timer with a 51s start-up timeout and a 1.6s normal timeout duration. On the ISL88011 and ISL88014, users can increase the nominal 200ms Power-On reset timeout delay by adding an external capacitor to the C_{POR} pin. Both fixed and adjustable voltage monitors are provided by the ISL88012. Complementary active-low and active-high reset outputs are available on the ISL88011, ISL88012 and ISL88013 devices. All devices provide manual reset capability (see “Product Features Table” on page 5).

Seven preprogrammed reset threshold voltages accurate to ±1.5% over temperature are offered (see “Ordering Information” on page 3). The ISL88012, ISL88014 and ISL88015 have a user-adjustable voltage input available for custom monitoring of any voltage down to 0.6V. All parts are specifically designed for low power consumption and high threshold accuracy.

Features

- Single/dual voltage monitoring supervisors
- Fixed-voltage options allow precise monitoring of +2.5V, +3.0V, +3.3V, and +5.0V power supplies
- Dual supervisor has one fixed voltage input and another that is user-adjustable down to 0.6V.
- Both RST and $\overline{RST}$ outputs available
- Adjustable POR timeout delay options
- Watchdog timer with 1.6s normal and 51s start-up timeout durations
- Manual reset input on all devices
- Reset signal valid down to V_{DD} = 1V
- Accurate ±1.5% voltage threshold
- Immune to power-supply transients
- Ultra low 5.5µA supply current
- Small 5 Ld SOT-23 Pb-Free package
- Pb-Free (RoHS Compliant)

Applications

- Process control systems
- Intelligent instruments
- Embedded control systems
- Computer systems
- Critical µP and µC power monitoring
- Portable/battery-powered equipment
- PDA and handheld PC devices

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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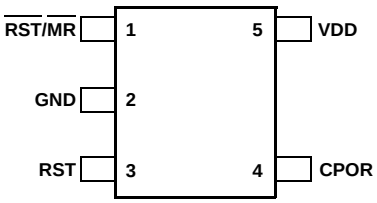
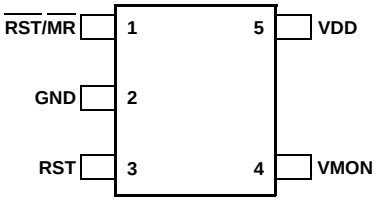
Pinouts

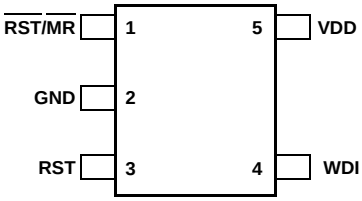
ISL88011
(5 LD SOT-23)
TOP VIEW



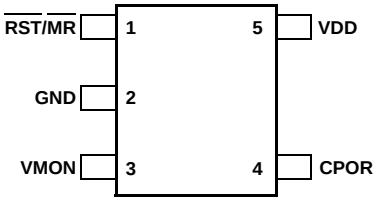
ISL88012
(5 LD SOT-23)
TOP VIEW



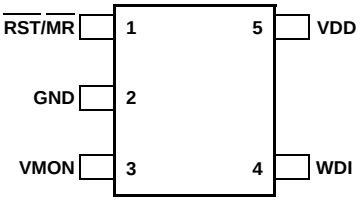
ISL88013
(5 LD SOT-23)
TOP VIEW



ISL88014
(5 LD SOT-23)
TOP VIEW



ISL88015
(5 LD SOT-23)
TOP VIEW



Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING (Note 4)	V_{THVDD} (V)	V_{THVMON} (V)	TEMPERATURE RANGE (°C)	PACKAGE TAPE AND REEL (Pb-free)	PKG. DWG. #
ISL88011IH546Z-TK	AGU	4.64	N/A	-40 to +85	5 Ld SOT-23	P5.064
ISL88011IH546Z-T7A	AGU	4.64	N/A	-40 to +85	5 Ld SOT-23	P5.064
ISL88011IH544Z-TK	AGV	4.38	N/A	-40 to +85	5 Ld SOT-23	P5.064
ISL88011IH544Z-T7A	AGV	4.38	N/A	-40 to +85	5 Ld SOT-23	P5.064
ISL88011IH531Z-TK	AGW	3.09	N/A	-40 to +85	5 Ld SOT-23	P5.064
ISL88011IH531Z-T7A	AGW	3.09	N/A	-40 to +85	5 Ld SOT-23	P5.064
ISL88011IH529Z-TK	AGX	2.92	N/A	-40 to +85	5 Ld SOT-23	P5.064
ISL88011IH529Z-T7A	AGX	2.92	N/A	-40 to +85	5 Ld SOT-23	P5.064
ISL88011IH526Z-TK	AGY	2.63	N/A	-40 to +85	5 Ld SOT-23	P5.064
ISL88011IH526Z-T7A	AGY	2.63	N/A	-40 to +85	5 Ld SOT-23	P5.064
ISL88011IH523Z-TK	AGZ	2.32	N/A	-40 to +85	5 Ld SOT-23)	P5.064
ISL88011IH523Z-T7A	AGZ	2.32	N/A	-40 to +85	5 Ld SOT-23)	P5.064
ISL88011IH522Z-TK	AHE	2.19	N/A	-40 to +85	5 Ld SOT-23	P5.064
ISL88011IH522Z-T7A	AHE	2.19	N/A	-40 to +85	5 Ld SOT-23	P5.064
ISL88012IH546Z-TK	AHF	4.64	0.6 (Note 2)	-40 to +85	5 Ld SOT-23	P5.064
ISL88012IH546Z-T7A	AHF	4.64	0.6 (Note 2)	-40 to +85	5 Ld SOT-23	P5.064
ISL88012IH544Z-TK	AHG	4.38	0.6 (Note 2)	-40 to +85	5 Ld SOT-23	P5.064
ISL88012IH544Z-T7A	AHG	4.38	0.6 (Note 2)	-40 to +85	5 Ld SOT-23	P5.064
ISL88012IH531Z-TK	AHH	3.09	0.6 (Note 2)	-40 to +85	5 Ld SOT-23	P5.064
ISL88012IH531Z-T7A	AHH	3.09	0.6 (Note 2)	-40 to +85	5 Ld SOT-23	P5.064
ISL88012IH529Z-TK	AHI	2.92	0.6 (Note 2)	-40 to +85	5 Ld SOT-23	P5.064
ISL88012IH529Z-T7A	AHI	2.92	0.6 (Note 2)	-40 to +85	5 Ld SOT-23	P5.064
ISL88012IH526Z-TK	AHJ	2.63	0.6 (Note 2)	-40 to +85	5 Ld SOT-23	P5.064
ISL88012IH526Z-T7A	AHJ	2.63	0.6 (Note 2)	-40 to +85	5 Ld SOT-23	P5.064
ISL88012IH523Z-TK	AHK	2.32	0.6 (Note 2)	-40 to +85	5 Ld SOT-23	P5.064
ISL88012IH523Z-T7A	AHK	2.32	0.6 (Note 2)	-40 to +85	5 Ld SOT-23	P5.064
ISL88012IH522Z-TK	AHL	2.19	0.6 (Note 2)	-40 to +85	5 Ld SOT-23	P5.064
ISL88012IH522Z-T7A	AHL	2.19	0.6 (Note 2)	-40 to +85	5 Ld SOT-23	P5.064
ISL88013IH546Z-TK	AHM	4.64	N/A	-40 to +85	5 Ld SOT-23	P5.064
ISL88013IH546Z-T7A	AHM	4.64	N/A	-40 to +85	5 Ld SOT-23	P5.064
ISL88013IH544Z-TK	AHN	4.38	N/A	-40 to +85	5 Ld SOT-23	P5.064
ISL88013IH544Z-T7A	AHN	4.38	N/A	-40 to +85	5 Ld SOT-23	P5.064
ISL88013IH531Z-TK	AHO	3.09	N/A	-40 to +85	5 Ld SOT-23	P5.064
ISL88013IH531Z-T7A	AHO	3.09	N/A	-40 to +85	5 Ld SOT-23	P5.064
ISL88013IH529Z-TK	AHP	2.92	N/A	-40 to +85	5 Ld SOT-23	P5.064
ISL88013IH529Z-T7A	AHP	2.92	N/A	-40 to +85	5 Ld SOT-23	P5.064
ISL88013IH526Z-TK	AHQ	2.63	N/A	-40 to +85	5 Ld SOT-23	P5.064
ISL88013IH526Z-T7A	AHQ	2.63	N/A	-40 to +85	5 Ld SOT-23	P5.064

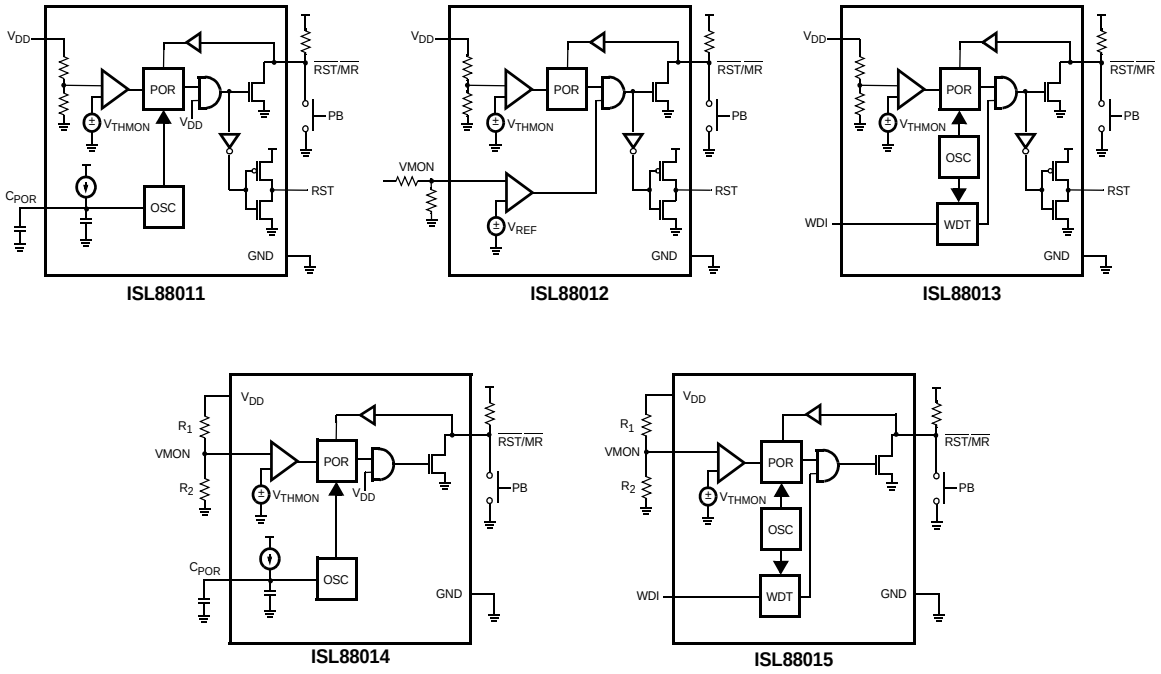
Ordering Information (Continued)

PART NUMBER (Notes 1, 2, 3)	PART MARKING (Note 4)	V_{THVDD} (V)	V_{THVMON} (V)	TEMPERATURE RANGE (°C)	PACKAGE TAPE AND REEL (Pb-free)	PKG. DWG. #
ISL88013IH523Z-TK	AHR	2.32	N/A	-40 to +85	5 Ld SOT-23	P5.064
ISL88013IH523Z-T7A	AHR	2.32	N/A	-40 to +85	5 Ld SOT-23	P5.064
ISL88013IH522Z-TK	AHS	2.19	N/A	-40 to +85	5 Ld SOT-23	P5.064
ISL88013IH522Z-T7A	AHS	2.19	N/A	-40 to +85	5 Ld SOT-23	P5.064
ISL88014IH5Z-TK	AHT	N/A	0.6 (Note 2)	-40 to +85	5 Ld SOT-23	P5.064
ISL88014IH5Z-T7A	AHT	N/A	0.6 (Note 2)	-40 to +85	5 Ld SOT-23	P5.064
ISL88015IH5Z-TK	AHU	N/A	0.6 (Note 2)	-40 to +85	5 Ld SOT-23	P5.064
ISL88015IH5Z-T7A	AHU	N/A	0.6 (Note 2)	-40 to +85	5 Ld SOT-23	P5.064
ISL88011EVAL1Z	ISL88011 Evaluation Card					
ISL88012EVAL1Z	ISL88012 Evaluation Card					
ISL88013EVAL1Z	ISL88013 Evaluation Card					
ISL88014EVAL1Z	ISL88014 Evaluation Card					
ISL88015EVAL1Z	ISL88015 Evaluation Card					

NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. The voltage trip point can be adjusted to be greater than 0.6V using 2 external resistors. By default, the VTHVMON trip point is 0.6V if no external resistors are used.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL88011, ISL88012, ISL88013, ISL88014, ISL88015. For more information on MSL please see techbrief TB363.
4. The part marking is located on the bottom of the part.

Functional Block Diagrams



Product Features Table

FUNCTION	ISL88011	ISL88012	ISL88013	ISL88014	ISL88015
Active-Low Reset ($\overline{RST}$)	x	x	x	x	x
Active-High Reset (RST)	x	x	x		
Watchdog Timer (WDI)			x		x
Dual Voltage Supervision		x			
Adjustable POR Timeout (C_{POR})	x			x	
Manual Reset Input ($\overline{MR}$)	x	x	x	x	x
Fixed Trip Point Voltage	x	x	x		
Adjustable Trip Point Voltage		x		x	x

Pin Descriptions

PIN					NAME	FUNCTION
ISL88011	ISL88012	ISL88013	ISL88014	ISL88015		
1	1	1	1	1	$\overline{RST}/\overline{MR}$	Combined Active-Low Reset Output and Manual Reset Input
2	2	2	2	2	GND	Ground
	4		3	3	VMON	Adjustable Threshold Voltage Input
3	3	3			RST	Active-High Reset Output
4			4		C_{POR}	Adjustable POR Timeout Delay Input
		4		4	WDI	Watchdog Timer Input
5	5	5	5	5	V_{DD}	Supply Voltage and Monitored Input

Absolute Maximum Ratings

Temperature Under Bias . . . . . .-40°C to +125°C
Storage Temperature . . . . . .-65°C to +150°C
Voltage on any pin with respect to GND . . . . . .-1.0V to +7V
DC Output Current. 5mA
ESD Rating
Human Body Model (Tested per JESD22-A114) 2500V
Charged Device Model (Tested per JESD22-C101E) 1200V
Machine Model (Tested per JESD22-A115) 250V

Recommended Operating Conditions

Temperature Range (Industrial) . . . . . .-40°C to +85°C
Pull-up Resistance (R_{PU}) . . . . . 5kΩ to 100kΩ

Thermal Information

Thermal Resistance (Typical	θ_{JA} (°C/W)
5 Ld SOT-23 (Note 5).	190

Maximum Junction Temperature (Plastic Package) . . . . . .+125°C
Maximum Storage Temperature Range. . . . . .-65°C to +150°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief **TB379** for details.

Electrical Specifications

Over the recommended operating conditions unless otherwise specified, R_{PU} = 10kΩ.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage Range		2.0		5.5	V
I_{DD}	Supply Current for ISL88011, ISL88012, ISL88013	V_{DD} = 5.0V		8	11.5	µA
		V_{DD} = 3.3V		7	10	µA
		V_{DD} = 2.5V		5.5	9	µA
	Supply Current for ISL88014, ISL88015	V_{DD} = 3.3V		4.5	8	µA
I_{LI}	Input Leakage Current (VMON)				100	nA
I_{LO}	Output Leakage Current (VMON)				100	nA
VOLTAGE THRESHOLDS						
V_{THVDD}	Fixed V_{DD} Voltage Trip Point	ISL88011, ISL88012, ISL88013IH5**46**	4.57	4.64	4.71	V
		ISL88011, ISL88012, ISL88013IH5**44**	4.31	4.38	4.45	V
		ISL88011, ISL88012, ISL88013IH5**31**	3.04	3.09	3.14	V
		ISL88011, ISL88012, ISL88013IH5**29**	2.88	2.92	2.96	V
		ISL88011, ISL88012, ISL88013IH5**26**	2.59	2.63	2.67	V
		ISL88011, ISL88012, ISL88013IH5**23**	2.29	2.32	2.35	V
		ISL88011, ISL88012, ISL88013IH5**22**	2.16	2.19	2.22	V
V_{THVDD} HYST	Hysteresis at V_{DD} Input	V_{THVDD} = 4.64V		46		mV
		V_{THVDD} = 4.38V		44		mV
		V_{THVDD} = 3.09V		31		mV
		V_{THVDD} = 2.92V		29		mV
		V_{THVDD}= 2.63V		26		mV
		V_{THVDD} = 2.32V		23		mV
		V_{THVDD} = 2.19V		22		mV
V_{THVMON}	Adj. Reset Voltage Trip Point (Note 6)	V_{THVDD} = 4.64V	599	605	611	mV
		V_{THVDD} = 4.38V	597	603	609	mV
		V_{THVDD} = 3.09V	589	595	601	mV
		V_{THVDD} = 2.92V	589	595	601	mV
		V_{THVDD}= 2.63V	589	595	601	mV
		V_{THVDD} = 2.32V	597	603	609	mV
		V_{THVDD} = 2.19V	597	603	609	mV

Electrical Specifications

Over the recommended operating conditions unless otherwise specified, R_{PU} = 10kΩ. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{THVMON}	Adj. Reset Voltage Trip Point (Note 7)		594	600	606	mV
$V_{THVMON\ HYST}$	Hysteresis Voltage (Notes 6, 7)			3		mV
RESET						
V_{OL}	Reset Output Voltage Low	$V_{DD} \geq 3.3V$, Sinking 0.5mA		0.05	0.40	V
		$V_{DD} < 3.3V$, Sinking 0.5mA		0.05	0.40	V
V_{OH}	Reset Output Voltage High	$V_{DD} \geq 3.3V$, Sourcing 0.4mA	V_{DD}-0.6	V_{DD}-0.4		V
		$V_{DD} < 3.3V$, Sourcing 0.4mA	V_{DD}-0.6	V_{DD}-0.4		V
t_{RPD}	V_{TH} to Reset Asserted Delay			60		µs
t_{POR}	POR Timeout Delay	ISL88012, ISL88013, ISL88015	140	200	260	ms
		ISL88011, ISL88014 with C_{POR} = OPEN	200	250		ms
C_{LOAD}	Load Capacitance on Reset Pins			5		pF
MANUAL RESET						
V_{MR}	$\overline{MR}$ Input Voltage		0		100	mV
t_{MR}	$\overline{MR}$ Minimum Pulse Width		1			µs
WATCHDOG TIMER (Note 8)						
Start t_{WDT}	Start-up Watchdog Timeout Period		32	51	64	sec
t_{WDT}	Normal Watchdog Timeout Period		1.0	1.6	2.0	sec
t_{WDPS}	WDI Minimum Pulse Width		100			ns
V_{IL}	Watchdog Input Voltage Low				0.3 x V_{DD}	V
V_{IH}	Watchdog Input Voltage High		0.85 x V_{DD}			V
I_{WDT}	Watchdog Input Current				100	nA

NOTES:

6. Applies to ISL88012.
7. Applies to ISL88014 and ISL88015.
8. Applies to ISL88013 and ISL88015.

Pin Description

RST

The push-pull RST output is set to V_{DD} (HIGH) listed in the following:

1. The device is first powered up.
2. Either V_{DD} or the voltage on VMON falls below their respective minimum voltage sense levels.
3. $\overline{MR}$ is asserted.
4. The watchdog timeout expires.

$\overline{RST}$/$\overline{MR}$

This pin functions as both a reset output and a manual reset input. The $\overline{RST}$ output functions identically to the complementary RST output but is an open drain output that is pulled to GND (LOW) when reset is asserted. The $\overline{MR}$ input is an active-low debounced input to which a user can connect a push-button to add manual reset capability or drive with active low signal from a controller.

V_{DD}

The V_{DD} pin is the power supply terminal. It is monitored by the ISL88011, ISL88012 and ISL88013. For these devices, the voltage at this pin is compared against an internal factory-programmed voltage trip point, V_{THVDD}. A reset is first asserted when the device is initially powered up to ensure that the power supply has stabilized. Thereafter, reset is again asserted whenever V_{DD} falls below V_{THVDD}. The device is designed with hysteresis to help prevent chattering due to noise.

VMON

The VMON pin on the ISL88012, ISL88014 and ISL88015 is a monitored input voltage that is user-adjustable. The voltage at this pin is compared against an internal 600mV reference voltage (V_{THVMON}) and a reset is asserted whenever the monitored voltage falls below this trip point.

WDI

The Watchdog Input takes an input from a microprocessor and ensures that it periodically toggles the WDI pin, otherwise the internal watchdog timer runs out and reset is asserted. The internal Watchdog Timer is cleared whenever the WDI input pin sees a rising or falling edge or the device is manually reset.

C_{POR}

The C_{POR} input pin lets users increase the Power-On Reset timeout delay (t_{POR}) by connecting a capacitor between C_{POR} and ground. (See Figure 3)

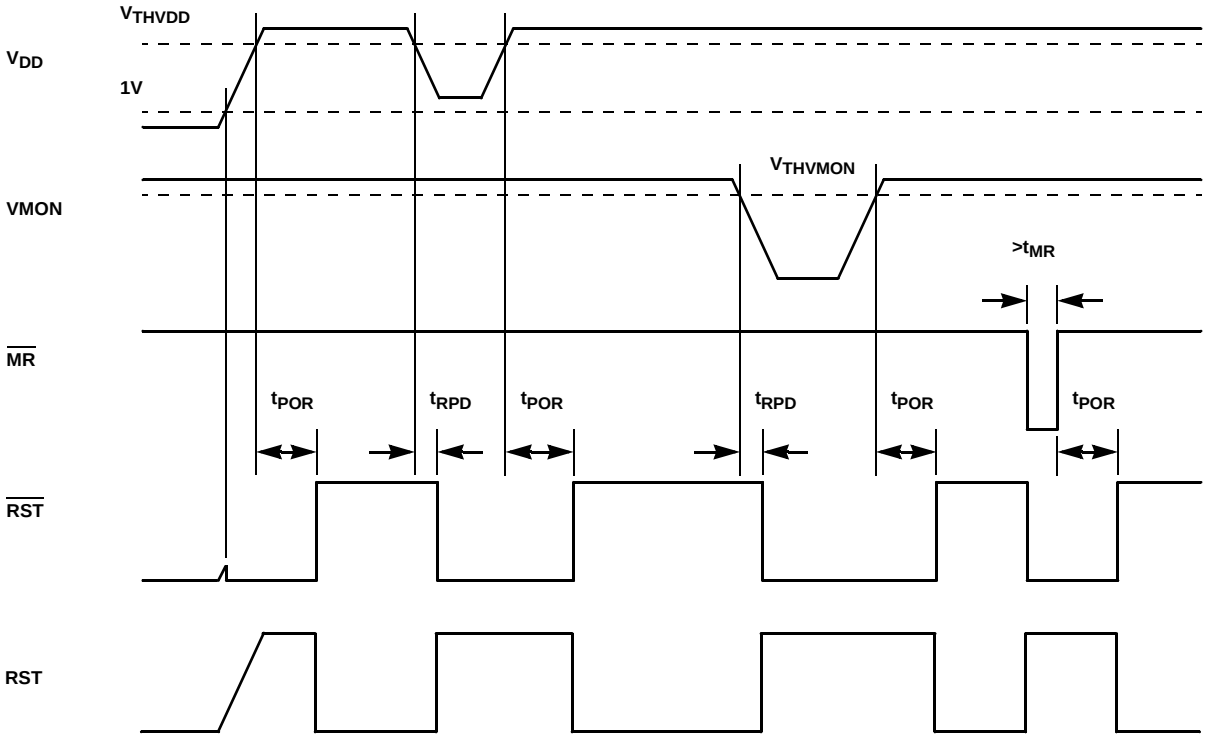


FIGURE 1. VOLTAGE MONITORING TIMING DIAGRAM

Principles of Operation

The ISL88011, ISL88012, ISL88013, ISL88014, ISL88015 devices provide those functions needed for critical voltage monitoring. These features include Power-On Reset control, customizable supply voltage supervision, Watchdog Timer capability, and manual reset assertion. By integrating all of these features into a small 5 Ld SOT-23 package and using only 5.5µA of supply current, the ISL88011, ISL88012, ISL88013, ISL88014, ISL88015 devices can assist in lowering system cost, reducing board space requirements, and increasing the reliability of a system.

Low Voltage Monitoring

During normal operation, these supervisors monitor both the voltage level of V_{DD} (ISL88011, ISL88012, ISL88013) and/or VMON (ISL88012, ISL88014, ISL88015). The device asserts a reset if any of these voltages falls below their respective trip points. The reset signal effectively prevents the system from operating during a power failure or brownout condition. This reset signal remains asserted until V_{DD} and the voltage on VMON exceed their voltage threshold setting for the reset time delay period t_{POR} of 200ms (See Figure 1)

The ISL88012, ISL88014 and ISL88015 allow users to customize the minimum voltage sense level on the VMON input pin. To do this, connect an external resistor divider network to the VMON pin in order to set the trip point to some voltage above 600mV according to the following Equation 1 (See Figure 2).

:

$$V_{INTRIP} = 0.6 \times \frac{(R_1 + R_2)}{R_2} \quad \text{(EQ. 1)}$$

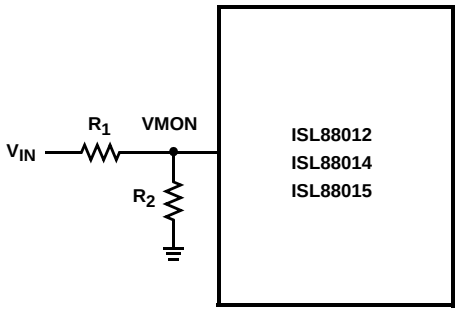


FIGURE 2. USING VMON TO MONITOR V_{IN} VIA RESISTORS

Power-On Reset (POR)

Applying at least 1V to the V_{DD} pin activates a POR circuit which asserts reset (i.e., RST goes HIGH while $\overline{RST}$ goes LOW). The reset signals remain asserted until the voltage at V_{DD} and/or VMON rise above the minimum voltage sense level for time period t_{POR}. This ensures that the voltages have stabilized.

These reset signals provide several benefits:

- It prevents the system microprocessor from starting to operate with insufficient voltage.
- It prevents the processor from operating prior to stabilization of the oscillator.
- It ensures that the monitored device is held out of operation until internal registers are properly loaded.
- It allows time for an FPGA to download its configuration prior to initialization of the circuit.

Adjusting POR Timeout via C_{POR} Pin

On the ISL88011 and ISL88014, users can adjust the Power-On Reset timeout delay (t_{POR}) up to many times the normal t_{POR} of 250ms. To do this, connect a capacitor between C_{POR} and ground (see Figure 3). For example, connecting a 30pF capacitor to C_{POR} will increase t_{POR} from a typical 250ms to about 2.5s. **NOTE:** Care should be taken in PCB layout and capacitor placement in order to reduce stray capacitance as much as possible, which lengthens the t_{POR} timeout period.

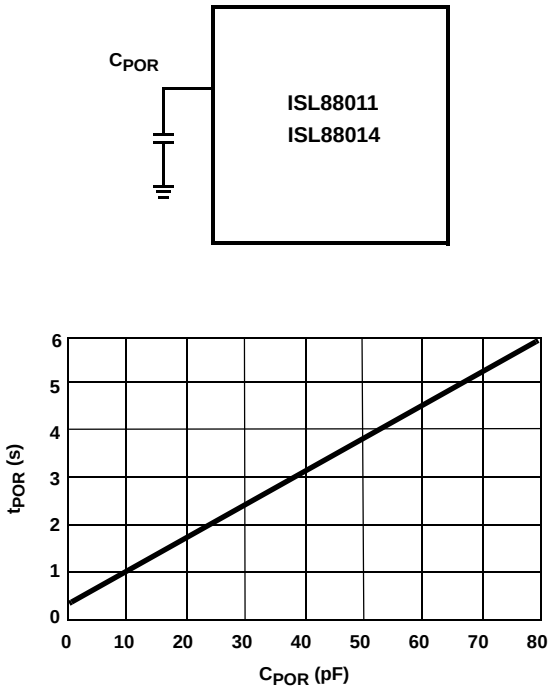


FIGURE 3. ADJUSTING t_{POR} WITH A CAPACITOR

Manual Reset

The manual reset input ($\overline{MR}$) allows the user to trigger a reset by using a push-button switch. The $\overline{MR}$ input is an active-low debounced input. By connecting a push-button directly from $\overline{MR}$ to ground, the designer adds manual system reset capability (see Figure 4). Reset is asserted if the $\overline{MR}$ pin is pulled low to less than 100mV for 1µs or longer while the push-button is closed. After $\overline{MR}$ is released, the reset outputs remain asserted for t_{POR} (200ms) and then released.

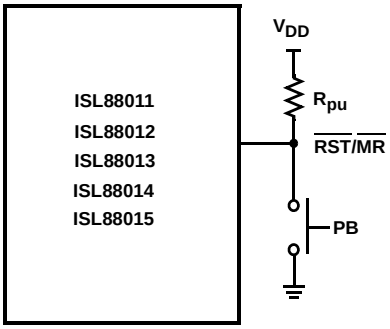


FIGURE 4. CONNECTING A MANUAL RESET PUSH-BUTTON

Watchdog Timer

The Watchdog Timer circuit checks microprocessor activity by monitoring the WDI input pin. The microprocessor must periodically toggle the WDI pin within t_{WDT} (1.6s nominal), otherwise the reset signal is asserted (see Figure 5). Internally, the 1.6s timer is cleared by either a reset or by toggling the WDI input.

Besides the 1.6s default timeout during normal operation, these devices also have a longer 51s timeout for start-up. During this time, a reset cannot be asserted due to the WDI not being toggled. The longer delay at power-on allows an operating system to boot, an FPGA to initialize, or the system software to initialize without the burden of dealing with the Watchdog.

Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

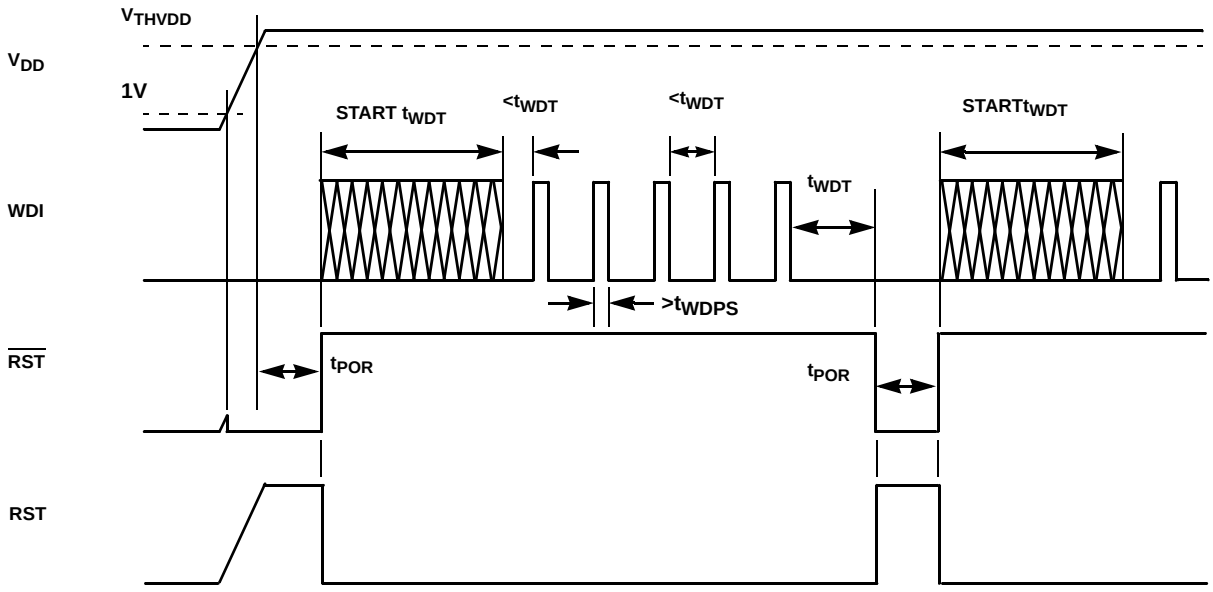


FIGURE 5. WATCHDOG TIMING DIAGRAM

Typical Parametric Performance Curves

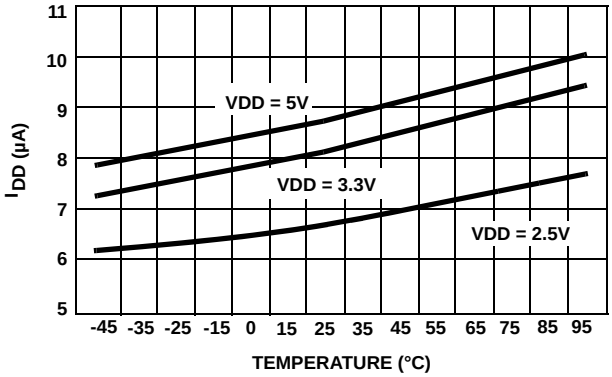


FIGURE 6. I_{DD} (ISL88011, ISL88012, ISL88013) vs TEMPERATURE

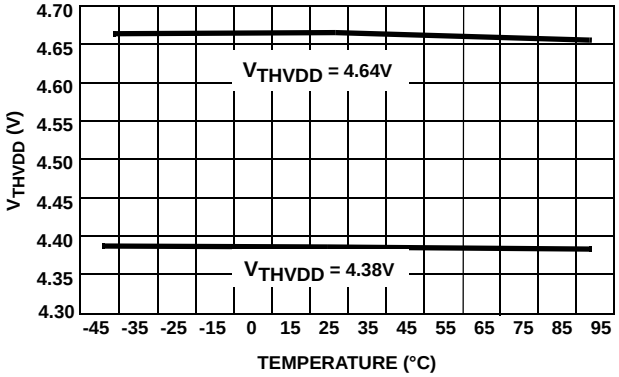


FIGURE 7. V_{THVDD}, V_{DD} = 5V vs TEMPERATURE

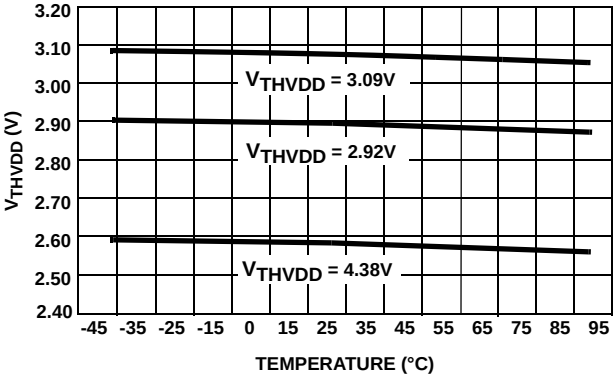


FIGURE 8. V_{THVDD}, V_{DD} = 3.3V vs TEMPERATURE

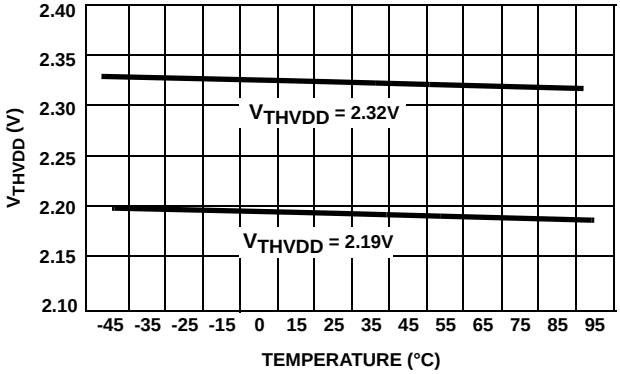


FIGURE 9. V_{THVDD}, V_{DD} = 2.5V vs TEMPERATURE

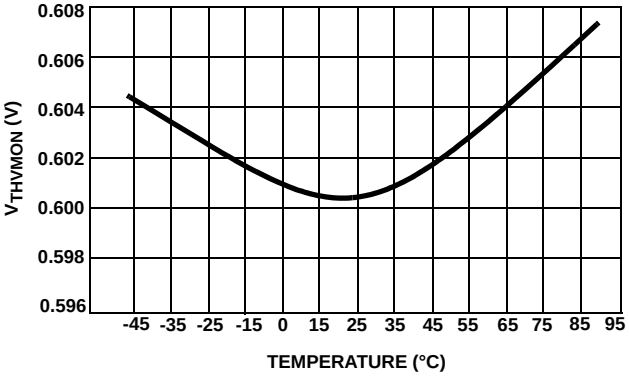


FIGURE 10. V_{THVMON} vs TEMPERATURE

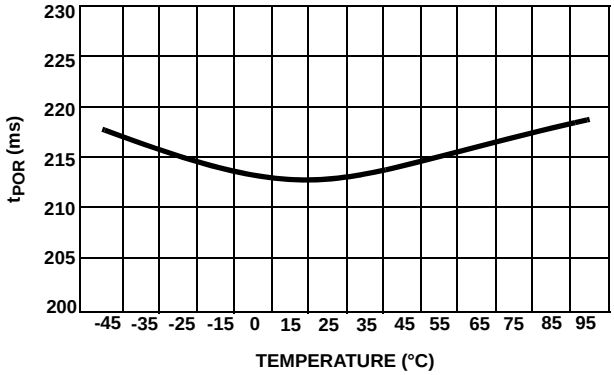


FIGURE 11. t_{POR} (C_{POR} OPEN) vs TEMPERATURE

Typical Application Circuits

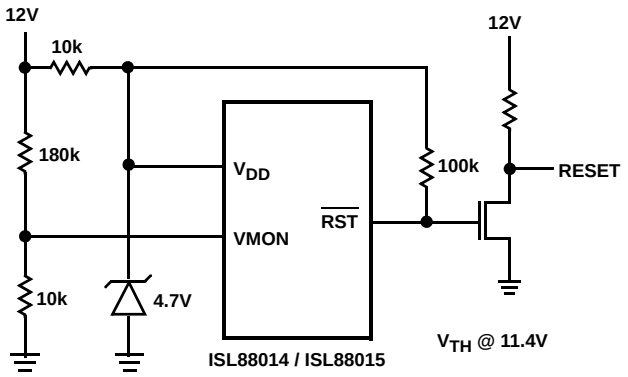


FIGURE 12. HIGH ACCURACY 12V SUPPLY MONITOR

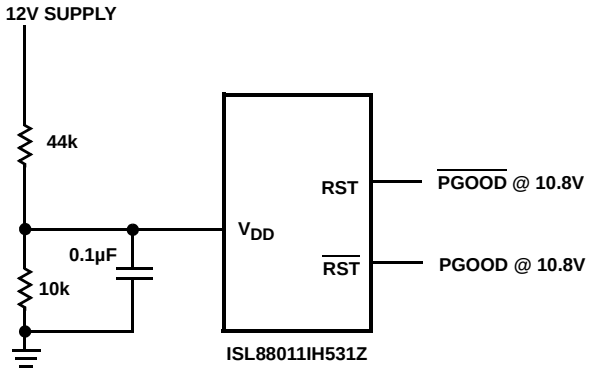


FIGURE 13. 12V SUPPLY PGOOD or $\overline{\text{PGOOD}}$

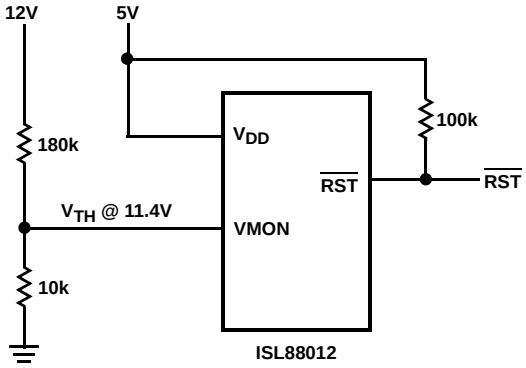
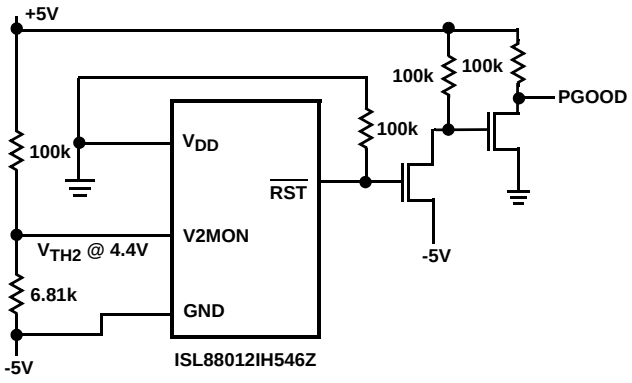
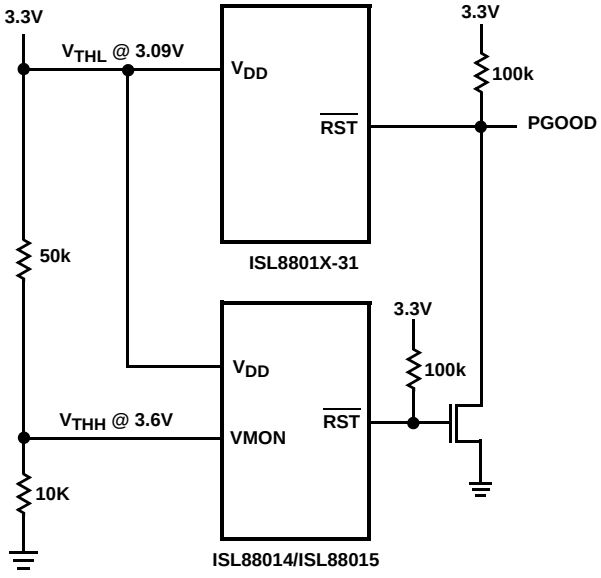


FIGURE 14. MONITOR 5V AND 12V SUPPLIES



PGOOD = HIGH IF -V < -4.6V AND -V + +V > 9.4 (abs)

FIGURE 15. +5V AND -5V MONITOR



VOLTAGE OUT OF RANGE = P_{GOOD} LOW

FIGURE 16. OVER/UNDERVOLTAGE MONITOR

ISL8801XEVAL1Z Board Schematics

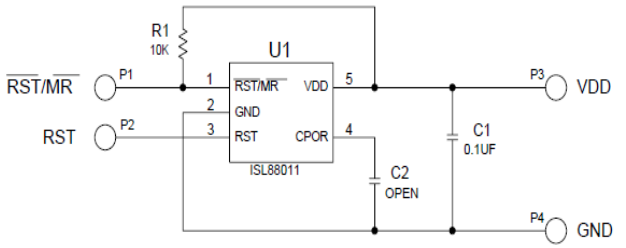


FIGURE 17. ISL88011EVAL1Z

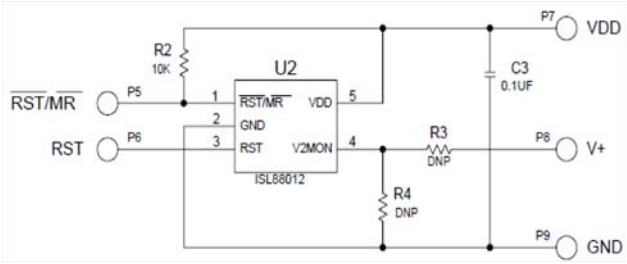


FIGURE 18. ISL88012EVAL1Z

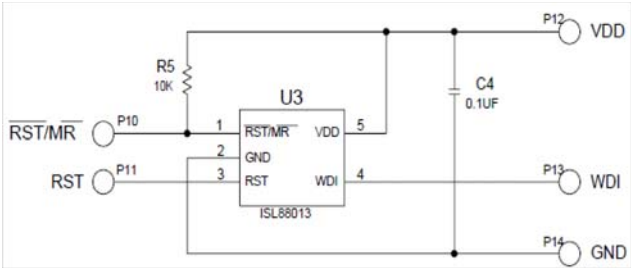


FIGURE 19. ISL88013EVAL1Z

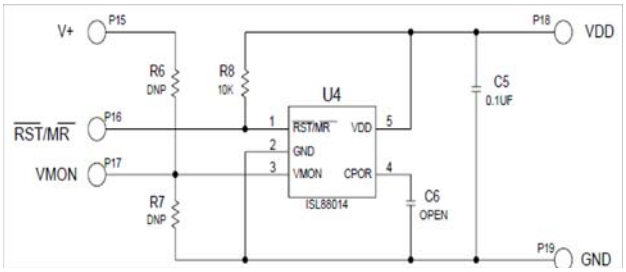


FIGURE 20. ISL88014EVAL1Z

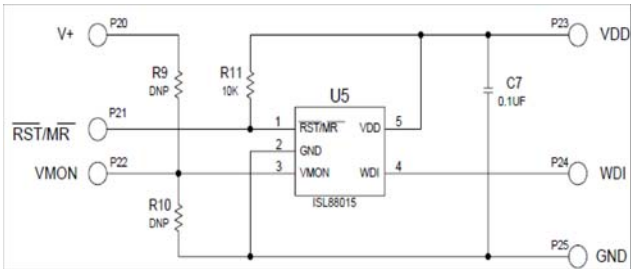


FIGURE 21. ISL88015EVAL1Z

Each of the ISL8801X parts has its own evaluation board provided with minimal customization, allowing the user to program with passive components both the POR timing and adjustable VMON thresholds, where applicable. The ISL88011EVAL1Z, ISL88012EVAL1Z and ISL88013EVAL1Z have a 4.6V Vth part installed.

FIGURE 22. THE TYPICAL ISL8801XEVAL1Z MEASURING 0.5” x 1”

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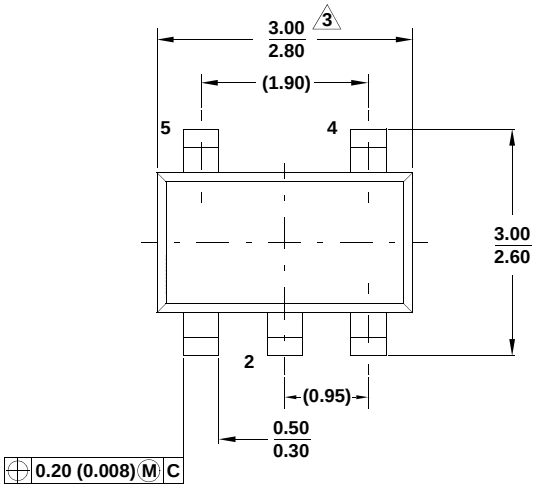
Package Outline Drawing

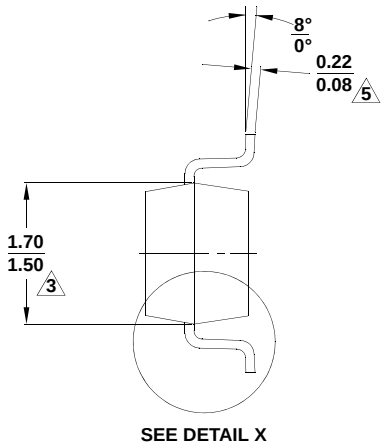
P5.064

5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

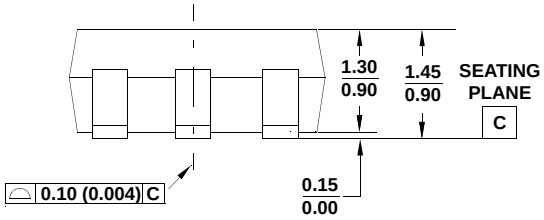
Rev 3, 4/11



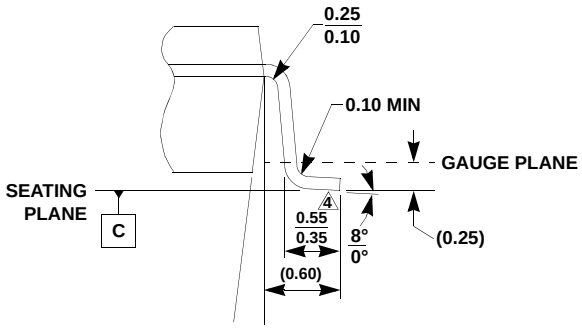
TOP VIEW



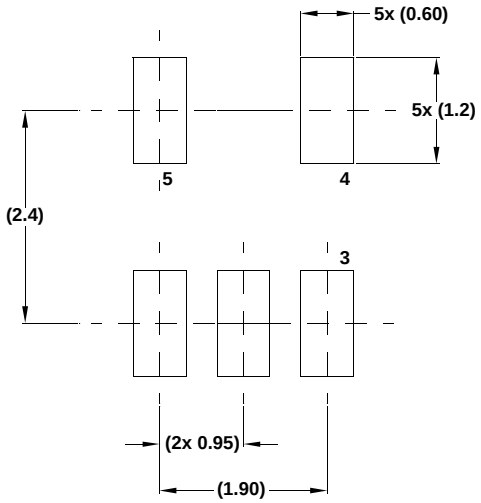
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerance per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC-74 and JEDEC MO178AA.
3. Package length and width are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength measured at reference to gauge plane.
5. Lead thickness applies to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
6. Controlling dimension: MILLIMETER. Dimensions in ( ) for reference only.