LV8498CT

ON Semiconductor®

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Bi-CMOS IC

For VCMs

Constant-current Driver IC Application Note

Overview

The LV8498CT is a constant current driver IC for voice coil motors that supports I^2C control integrating a digital/analog converter (DAC). It uses an ultraminiature WLP package and includes a current detection resistor for constant current control, which makes the IC ideal for miniaturization of camera modules intended for use in camera-equipped mobile phones. The output transistor has a low on-resistance of 1Ω and the resistance of the built-in current detection resistor is 1Ω, which minimizes the voltage loss and helps withstand voltage drop in V_{CC}. The function is incorporated, which, by changing the current in a stepped pattern while taking time at rise and fall of the output current, provides the current a slope, improving the converging stability of the voice coil motor (current slope function).

Functions

- Constant current driver for voice coil motors.
- Constant current control enabled by DAC (10 bits).
- I^2C bus control supported.
- Wide operating voltage range (2.2 to 5.0V).
- Built-in current detection resistor.
- 6-pin WLP package used (1.27 × 0.87 × 0.25mm).
- Built-in voltage drop protection circuit (V_{CC} = 2V output off).
- Built-in thermal protection circuit.
- Low output block total-resistance of 2Ω helps withstand voltage drop in V_{CC}. (Current detection resistance + output transistor on-resistance).
- Built-in VCM overshoot preventive function (current slope function).

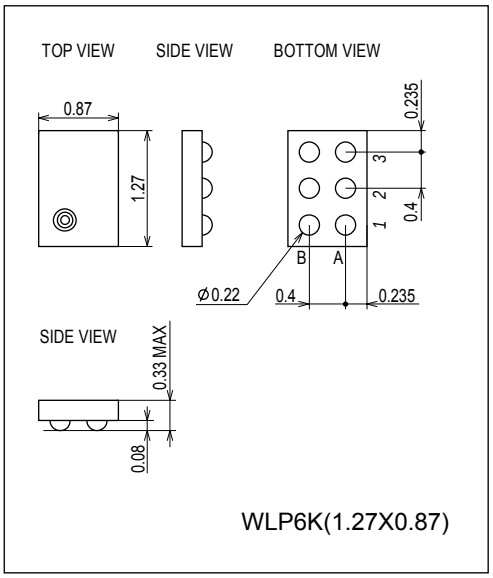
Typical Applications

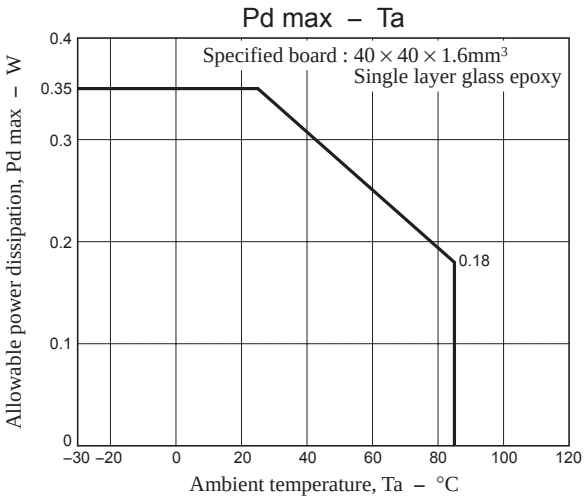
- Cell phone
- Pocket movie

Package Dimensions

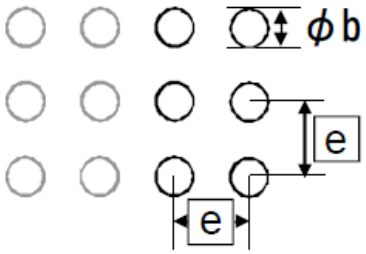
unit: mm (typ)

3390





Recommended Soldering Footprint



(Unit:mm)

Reference symbol	WLP6K
e	0.40
b	0.22

Caution: The package dimension is a reference value, which is not a guaranteed value.

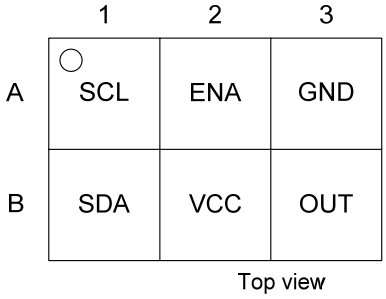


Figure 1. Pin Assignment

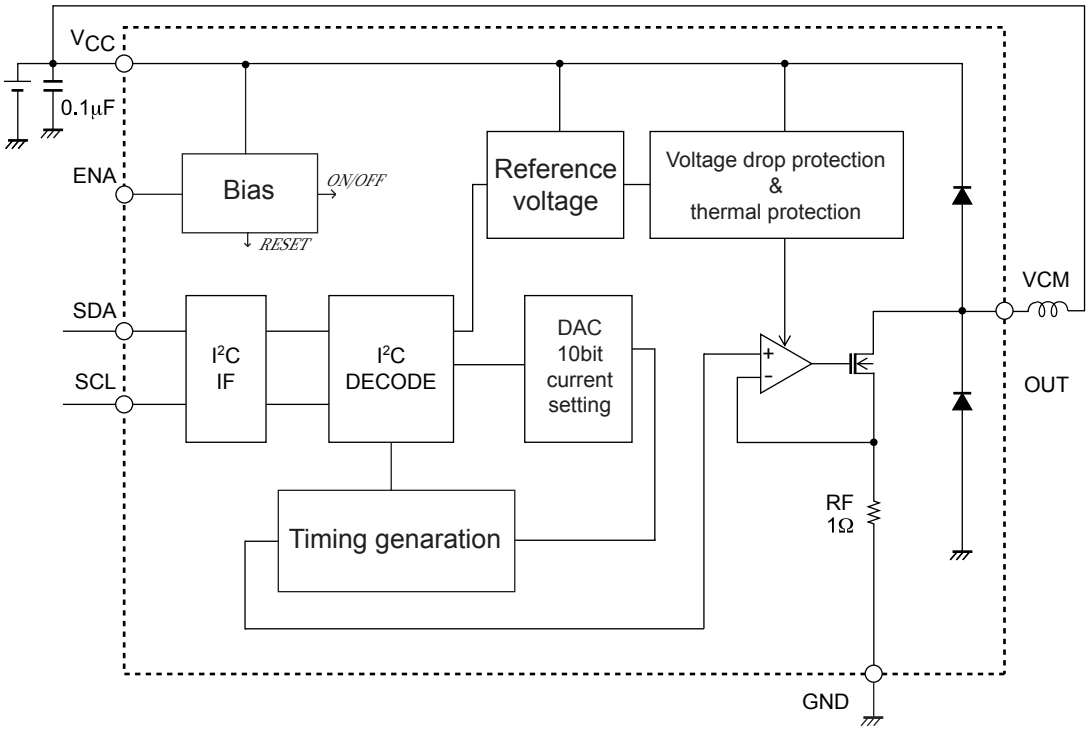


Figure 2. Block Diagram

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		5.5	V
Output voltage	V_{OUT} max		V_{CC} + 0.5	V
Input voltage	V_{IN} max	SCL, SDA, ENA	5.5	V
GND pin source current	I_{GND}		200	mA
Allowable power dissipation	Pd max	With specified substrate *	350	mW
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		-40 to +150	°C

* Specified substrate : 40mm × 40mm × 1.6mm, Single layer glass epoxy substrate

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.
Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{CC}		2.2		5.0	V
Maximum preset output current	I_O			150		mA
Input signal voltage	V_{IN}		-0.3		V_{CC}+0.3	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 2.8V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current	I_{CC}0a	ENA = 0V, SCL=SDA=V_{CC}			1	μA
	I_{CC}0b	ENA=SCL=SDA=V_{CC}, PD = 1			1	μA
	I_{CC}0c	ENA=SCL=SDA=V_{CC}, D0 to D9 = 0			1	μA
	I_{CC}1	ENA=SCL=SDA=V_{CC} , D0 to D9 ≠ 0		0.5	3	mA
Input current	I_{IN}	SCL, SDA, ENA	-1	0	1	μA
High level input voltage	V_IH	Applied to SCL, SDA and ENA pin.	1.5		VCC+0.3	V
Low level input voltage	V_IL		-0.3		0.5	V
Total resistance value of the output block (built-in resistor + transistor on-resistance)	RTTL	V_{CC} = 2.8V, I_{OUT} = 80mA		2	3	Ω
DAC block						
Resolution				10		bits
Relative accuracy	INL				±2	LSB
Differential linearity	DNL				±1	LSB
Full code current	Ifull	D0 to D9 = 1		150		mA
Error code current 0	Izero	D0 to D9 = 0		0		mA
Spark killer diode						
Reverse current	IS (leak)				1	μA
Forward voltage	VSF	I_{OUT}=100mA			1.3	V

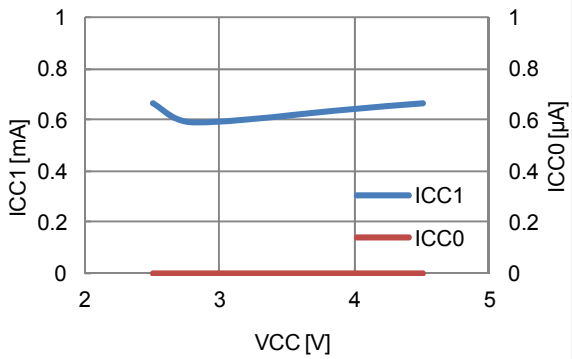


Figure 3. VCC supply current vs VCC Voltage

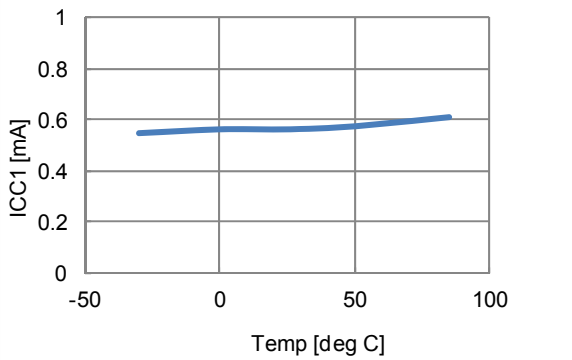


Figure 4. VCC supply current vs Temparature (VCC=2.8V)

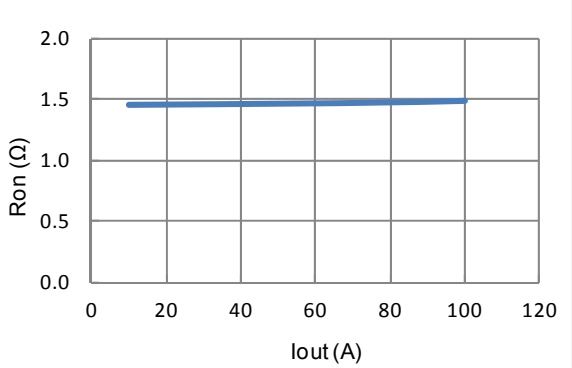


Figure 5. Output on Resistance vs Output Current (VCC= 2.8V)

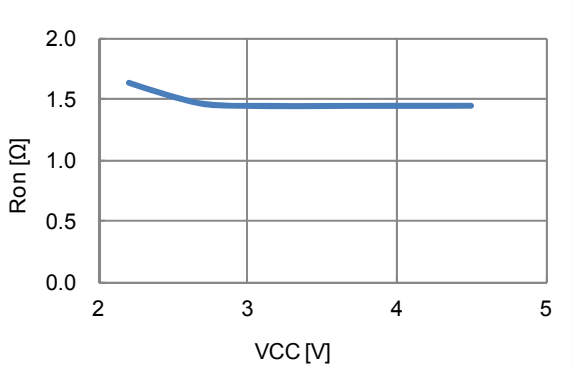


Figure 6. Output on Resistance vs VCC Voltage (Iout= 80mA)

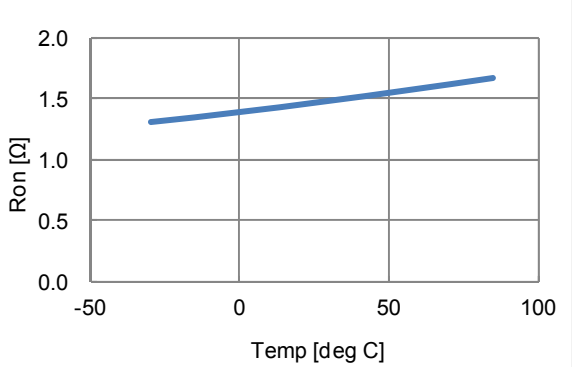


Figure 7. Output on Resistance vs Temparature (VCC=2.8V, Iout= 80mA)

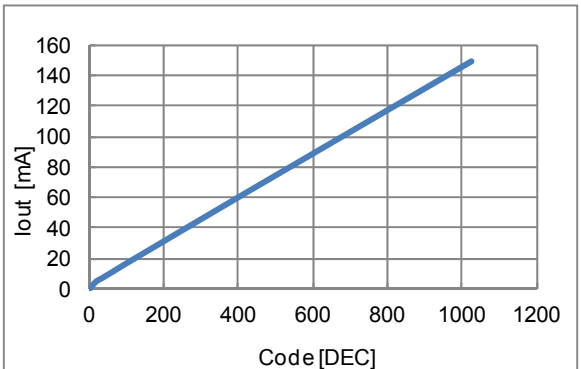


Figure 8. Output current vs Setting code (VCC=2.8V)

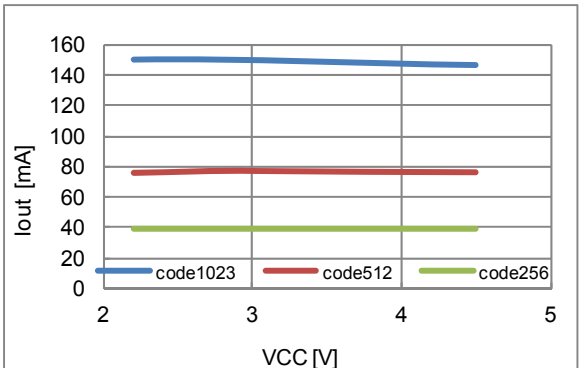


Figure 9. Output current vs VCC Voltage

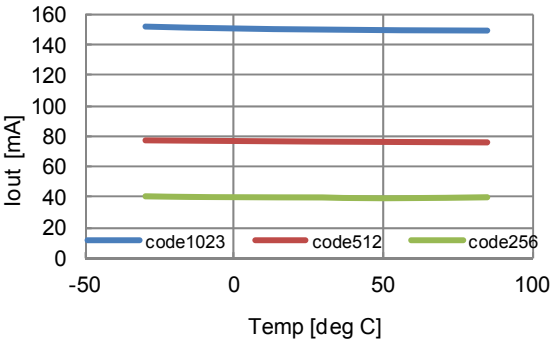


Figure 10. Output current vs Temparature (VCC=2.8V)

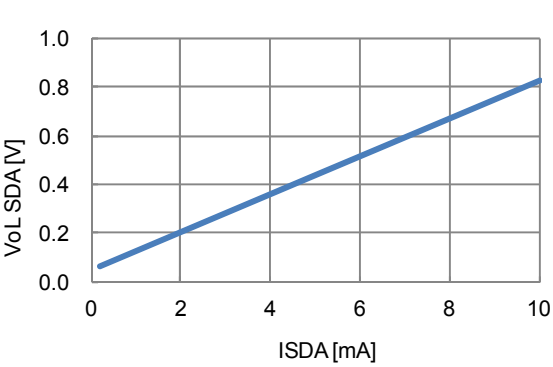


Figure 11. Saturation voltage of SDA vs ISDA(VCC=2.8V)

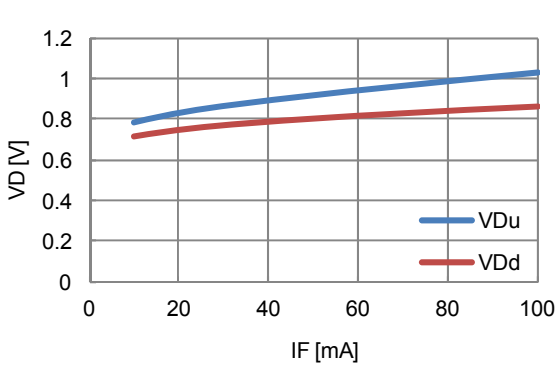
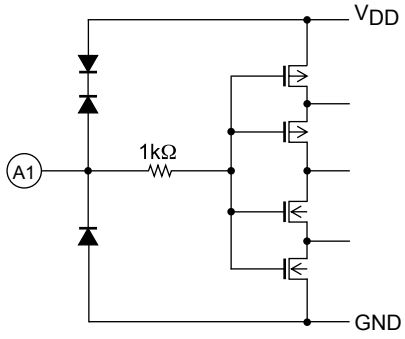
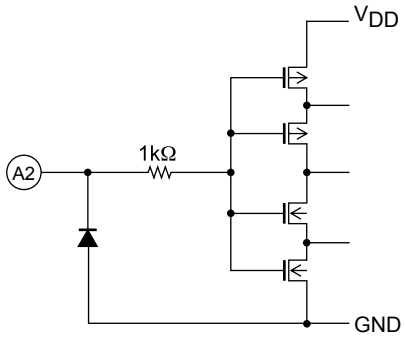
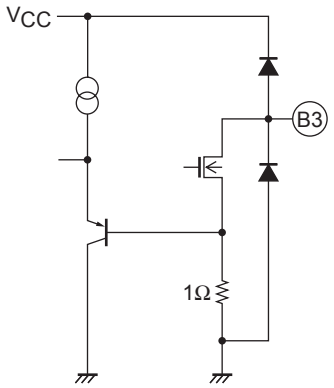
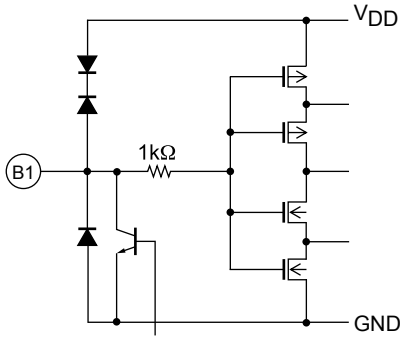


Figure 12. Diode Forward Voltage vs Diode Forward Current

Pin Functions

Pin No.	Pin name	Pin Function	Equivalent circuit
A1	SCL	This is the I^2C serial clock input pin Input high level : 1.5V to V_{CC}-0.3V Input low level : -0.3V to 0.5V	
A2	ENA	This pin switches chip enable. When low, standby mode and reset is performed at the same time. This pin is held high for normal use. Do not set to OPEN under any circumstance. Input high level : 1.5V to V_{CC}-0.3V Input low level : -0.3V to 0.5V	
A3	GND	The logic and low level analog signals shall be connected to this pin.	
B3	OUT	This is an NMOS open drain output, and the voice coil motor is connected between this pin and the V_{CC} pin for use.	
B2	V_{CC}	This pin is connected to the Power supply and monitored by the LV8498. The operation is inhibited when V_{CC} is below the minimum 2.0 V value by the Low Voltage Shut Down function. Refer to (2) on P.8 for details.	
B1	SDA	This is the I^2C serial data input pin Input high level : 1.5V to V_{CC}-0.3V Input low level : -0.3V to 0.5V	

Operation Description

LV8498CT is a driver IC for auto focus (AF: VCM) via I^2C interface.
It is a uni-polar type driver wherein actuator is connected between VCC and OUT and driven by sink current from OUT.
As for the drive current, linear constant current is controlled by the internal current detection resistor and the control circuit. Moreover, the current slope function shortens settling time of the actuator.

LV8498CT can drive actuator with coil resistance which satisfies the following relation:

R_{AF} +RTTL < V_{CC} / I_{AF}

(R_{AF}: Coil resistor of AF VCM, RTTL: OUT ON resistance, I_{AF}: Drive current of AF VCM)

Where V_{CC}=2.8V:

R_{AF} < V_{CC} / I_{AF}- RTTL
< 2.8V/ 80mA- 3 Ω
< 32 Ω

Make sure to allow margin for coil resistor, V_{CC} voltage and drive current based on the above relation.

(1) Function and setup for ENA pin
ENA is set to active mode at high level input and to standby mode at low level input. During standby mode, I^2C signal is not receivable even if V_{CC} is impressed. Since all the circuits are turned off, current consumption is zero.
ENA pin does not incorporate pull-up nor pull-down. Hence, ENA cannot be set to open. ENA can be set to pull-up externally. In this case, it is recommended to transfer “All-zero” to the entire register data when V_{CC} is impressed.

(2) V_{CC} Low Voltage Shut Down
The built-in comparator, associated with the band gap reference, continuously monitors the V_{CC} input while ENA is High.
When V_{CC} drops 2.0V (typical) or lower, this IC generates power saving sequence to turn off the output. However, this status is not the standby mode; therefore, current consumption is not quite zero.

(3) Output transistor operation mode
When the output transistor is ON, coil current flow through the VCM.
The output voltage is obtained as follows:
V_{SAT}OUT + 1Ω × Iout = RTTL × Iout
* V_{SAT}OUT: Saturation voltage of the output transistor when it energizes Iout.

When the output transistor is OFF after energization, coil current flows through upper Diode.
In this case, output voltage is:
V_{CC} + V_F
Do not exceed the absolute maximum ratings under no circumstance.

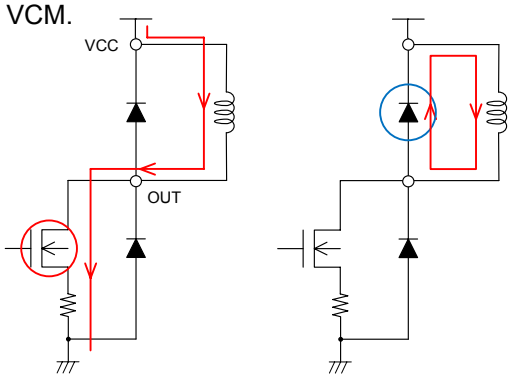


Figure 13. Output transistor operation

Serial Bus Communication Specifications

(1) I^2C serial transfer timing conditions

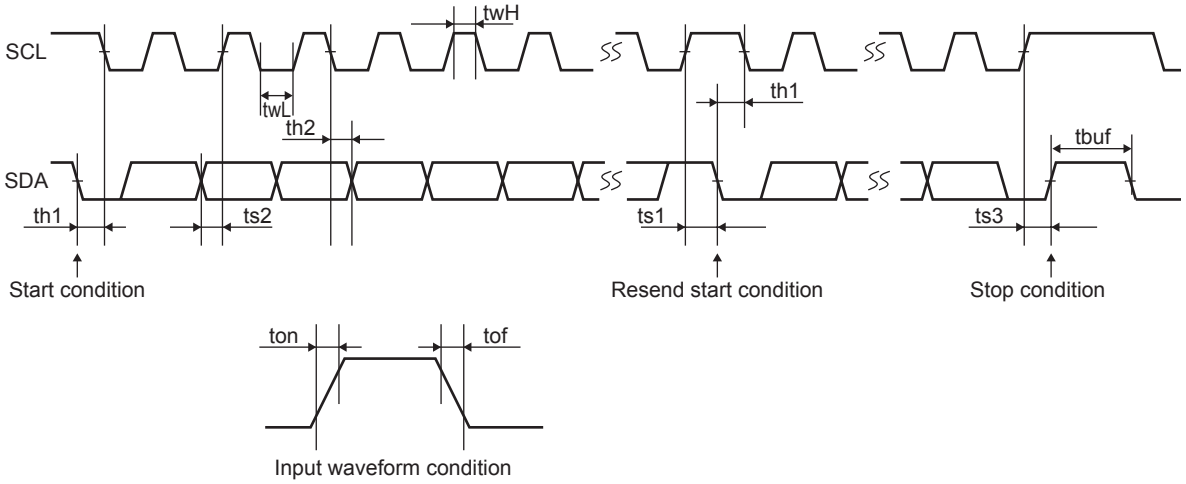


Figure 14. I^2C serial transfer timing Diagram

Standard mode

Parameter	symbol	Conditions	min	typ	max	unit
SCL clock frequency	fscl	SCL clock frequency	0		100	kHz
Data setup time	ts1	Setup time of SCL with respect to the falling edge of SDA	4.7			μs
	ts2	Setup time of SDA with respect to the rising edge of SCL	250			ns
	ts3	Setup time of SCL with respect to the rising edge of SDA	4.0			μs
Data hold time	th1	Hold time of SCL with respect to the rising edge of SDA	4.0			μs
	th2	Hold time of SDA with respect to the falling edge of SCL	0			μs
Pulse width	twL	SCL low period pulse width	4.7			μs
	twH	SCL high period pulse width	4.0			μs
Input waveform conditions	ton	SCL, SDA (input) rising time			1000	ns
	tof	SCL, SDA (input) falling time			300	ns
Bus free time	tbuf	Interval between stop condition and start condition	4.7			μs

High-speed mode

Parameter	Symbol	Conditions	min	typ	max	unit
SCL clock frequency	fscl	SCL clock frequency	0		400	kHz
Data setup time	ts1	Setup time of SCL with respect to the falling edge of SDA	0.6			μs
	ts2	Setup time of SDA with respect to the rising edge of SCL	100			ns
	ts3	Setup time of SCL with respect to the rising edge of SDA	0.6			μs
Data hold time	th1	Hold time of SCL with respect to the rising edge of SDA	0.6			μs
	th2	Hold time of SDA with respect to the falling edge of SCL	0			μs
Pulse width	twL	SCL low period pulse width	1.3			μs
	twH	SCL high period pulse width	0.6			μs
Input waveform conditions	ton	SCL, SDA (input) rising time			300	ns
	tof	SCL, SDA (input) falling time			300	ns
Bus free time	tbuf	Interval between stop condition and start condition	1.3			μs

(2) I^2C bus transmission method

2-1) Start and stop conditions

The I^2C bus requires that the state of SDA be preserved while SCL is high as shown in the timing diagram below during a data transfer operation.

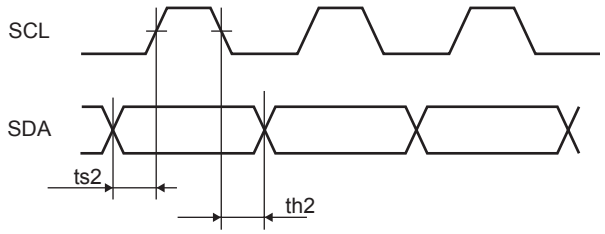


Figure 15. The timing chart of the state of SDA

When data is not being transferred, both SCL and SDA are in the high level. The start condition is generated and access is started when SDA is changed from high to low while SCL and SDA are high.
Conversely, the stop condition is generated and access is ended when SDA is changed from low to high while SCL is high.

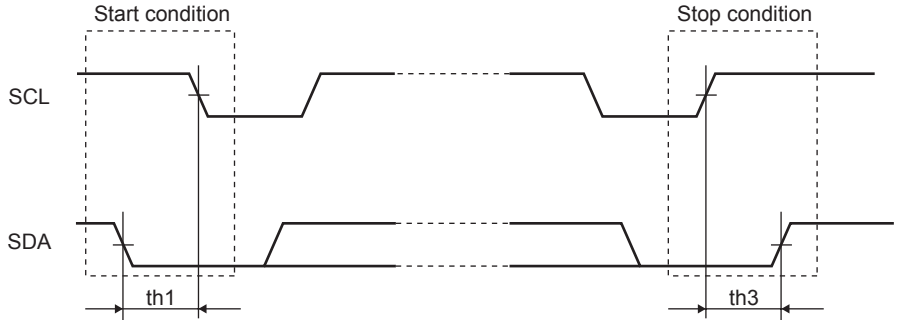


Figure 16. I^2C Start and Stop conditions

2-2) Data transfer and acknowledgement response

After the start condition has been generated, the data is transferred one byte (8 bits) at a time. Generally, in an I^2C bus, a unique 7-bit slave address is assigned to each device, and the first byte of the transfer data is allocated to the 7-bit slave address and to the command (Write/Read) indicating the transfer direction of the subsequent data. However, this IC is provided with only a write mode for receiving the data. Every time 8 bits of data for each byte are transferred, the ACK signal is sent from the receiving end to the sending end. Immediately after the clock pulse of SCL bit 8 in the data transferred has fallen to low, SDA at the sending end is released, and SDA is set to low at the receiving end, causing the ACK signal to be sent. When, after the receiving end has sent the ACK signal, the transfer of the next byte remains in the receiving status, the receiving end releases SDA at the falling edge of the ninth SCL clock.

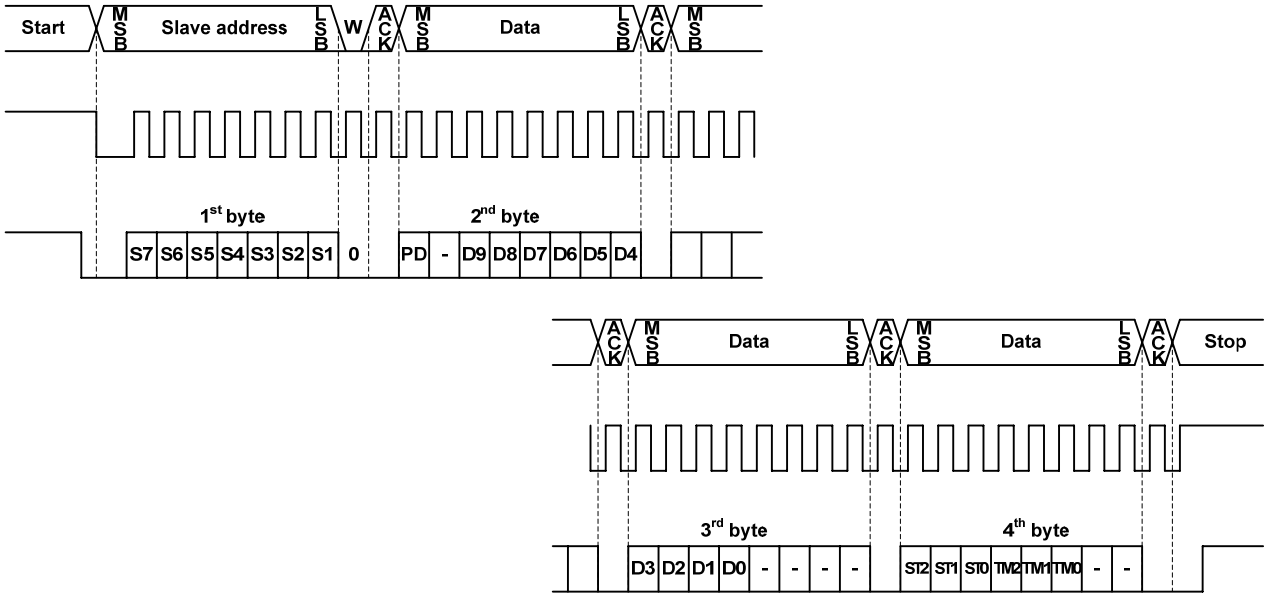


Figure 17. The chain of signals from Start to Stop

A set of data transferred to LV8498CT should bundle the following 4 data: the slave address of the first byte and the data of the second, third and fourth bytes.

Slave address: 0110011(S7→S1)

The table below shows the format of the second, third and fourth bytes.

	2nd byte								3rd byte							
Serial data bits	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
Function	PD	-	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	-	-	-	-

4th byte							
SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
ST2	ST1	ST0	TM2	TM1	TM0	-	-

Serial Mode Setting

(1) AF mode setting

1-1) Setup for power down data
SD7 is in the 2nd byte to which power down data (PD) is allocated. (PD=0, Active. PD=1, Power down.)
Where PD=1, the IC does not operate even if a following data is configured.
Also when PD=1 is set during energization, the output current decreases according to the setting in 1-3) Current slope Setting and eventually turns zero.

1-2) AF current DAC setting
AF drive current is configured by 10-bit DAC. See the chart below for the relation between setup data and drive current.

AF DAC code	D9	D8	D7	D6	D5	D4	D3	D2	D1	Setting current [mA]
0	0	0	0	0	0	0	0	0	0	0 (drive-OFF)
1	0	0	0	0	0	0	0	0	1	0.1466
2	0	0	0	0	0	0	0	1	0	0.293
3	0	0	0	0	0	0	0	1	1	0.440
1021	1	1	1	1	1	1	1	0	1	149.68
1022	1	1	1	1	1	1	1	1	0	149.83
1023	1	1	1	1	1	1	1	1	1	150

Note: When “AF DAC code” is 0, AF driver is OFF.
If other codes are selected, AF driver starts to drive at the same time as 4 bytes data are set.
Setting current is the theory value provided by following formula.
Setting current = {(Full code current)/1023} × (AF DAC code)

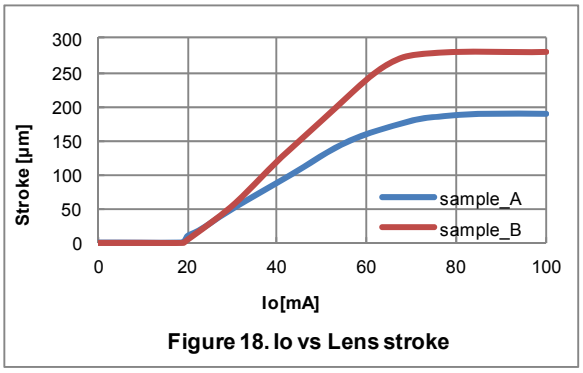


Figure 18. Io vs Lens stroke

The above graph shows the measurement result of lens stroke using Laser Displacement Sensor when 2 types of lens module are driven by LV8498CT. The measurement has been conducted with the 2 modules placed horizontally.
The characteristics may vary depends on the usage AF-VCM and lens module. Therefore, make sure to perform examination and adjustment thoroughly as needed.

1-3) AF current slope Setting

The gradient of AF current slope is configured by the 2 parameters of step time and step current value. Since each parameter uses 3 bits, 6 bits are used in total. 001000 sets the highest gradient whereas 111111 sets the lowest gradient. 000XXX turns off current slope function and AF drive current changes to a setting value step by step.

Since register data is the 4th byte of AF current DAC Setting, it needs to be set with AF current DAC Setting simultaneously.

AF current slope setting STP (ST2, ST1, ST0) TIM (TM2, TM1, TM0)

STP \ TIM	000	001	010	011	100	101	110	111
000	Current slope function OFF							
001	0.032	0.064	0.128	0.256	0.512	1.024	2.048	4.096
	0.1466	0.1466	0.1466	0.1466	0.1466	0.1466	0.1466	0.1466
010	0.064	0.128	0.256	0.512	1.024	2.048	4.096	8.192
	0.293	0.293	0.293	0.293	0.293	0.293	0.293	0.293
011	0.128	0.256	0.512	1.024	2.048	4.096	8.192	16.38
	0.586	0.586	0.586	0.586	0.586	0.586	0.586	0.586
100	0.256	0.512	1.024	2.048	4.096	8.192	16.38	32.77
	1.173	1.173	1.173	1.173	1.173	1.173	1.173	1.173
101	0.512	1.024	2.048	4.096	8.192	16.38	32.77	65.54
	2.345	2.345	2.345	2.345	2.345	2.345	2.345	2.345
110	1.024	2.048	4.096	8.192	16.38	32.77	65.54	131.08
	4.691	4.691	4.691	4.691	4.691	4.691	4.691	4.691
111	2.048	4.096	8.192	16.38	32.77	65.54	131.08	262.16
	9.382	9.382	9.382	9.382	9.382	9.382	9.382	9.382

In the above table,

Upper row of each field: Step time (Tst) [mSec]

Lower row of each field: Step current value (Ist) [mA]

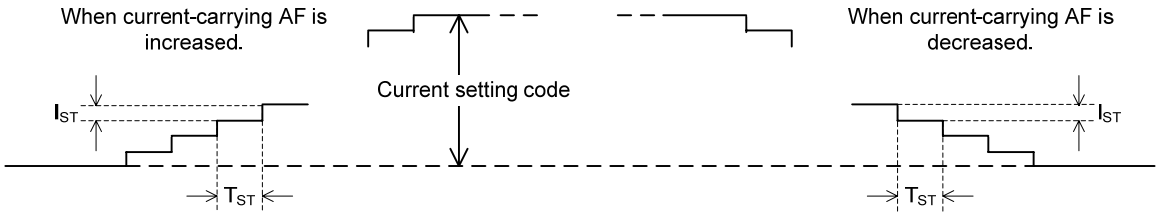


Figure 19. Current slope function Image Diagram

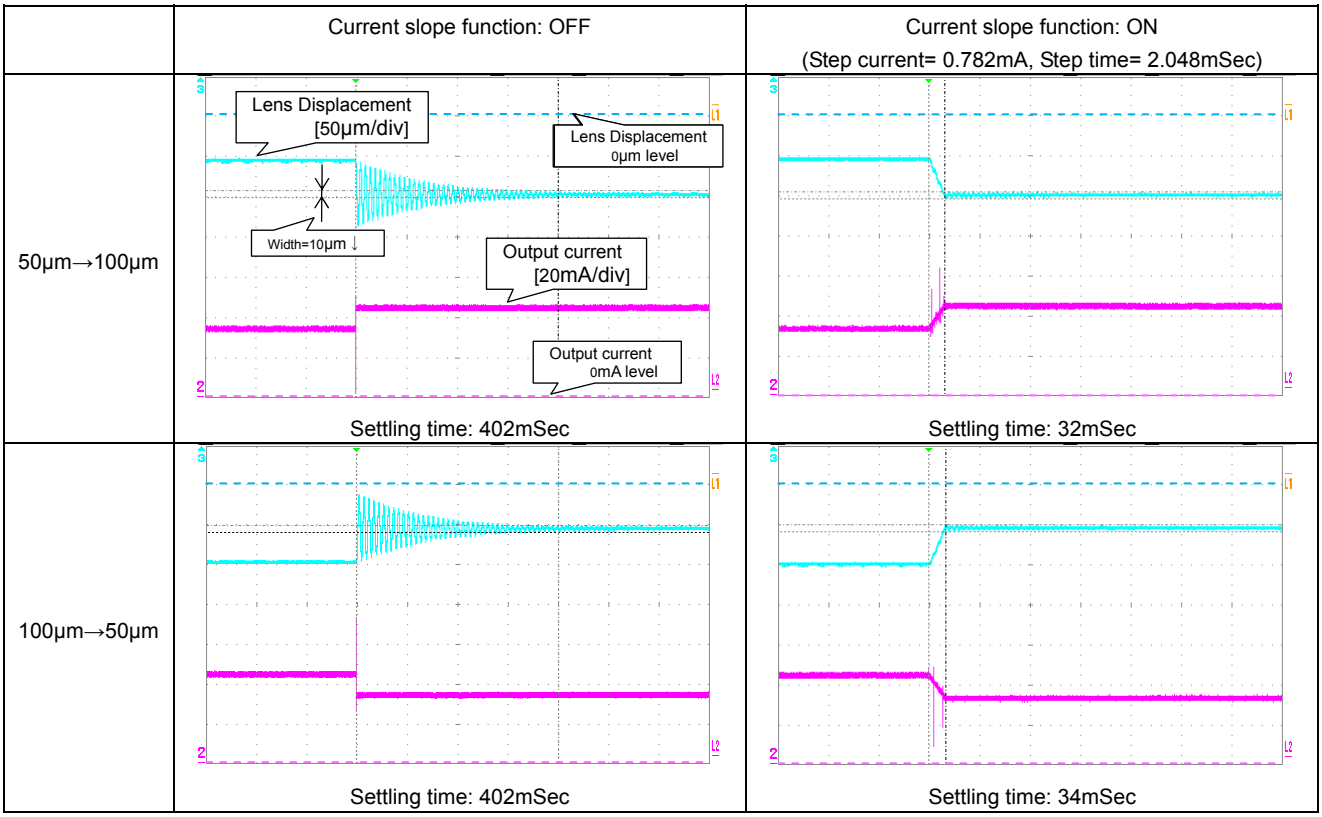


Figure 20. The sample of Current slope function effect

The above figure is the comparison of the settling time with or without current slope function measured by laser displacement sensor. Depends on the characteristics of VCM, an optimum gradient of slope variers. Make sure to test with AF-VCM thoroughly and make an adjustment if necessary.

1-4) Relationship between the ENA pin input, I^2C input data PD, and current setting 0 (code 0)
This IC supports the following three modes of setting up the standby mode:
1) Setting the ENA pin low.
2) Setting the PD bit to 1 (high) with I^2C input data.
3) Setting the output current to 0 with I^2C input data.

Execution of one of the steps 1) to 3) causes the output current to 0 and stops operation of the circuit. When the ENA pin is set low, the I^2C data register is reset and the IC is reset to its default state (PD bit set to 0 and output current setting to code 0).

Typical Application Circuit

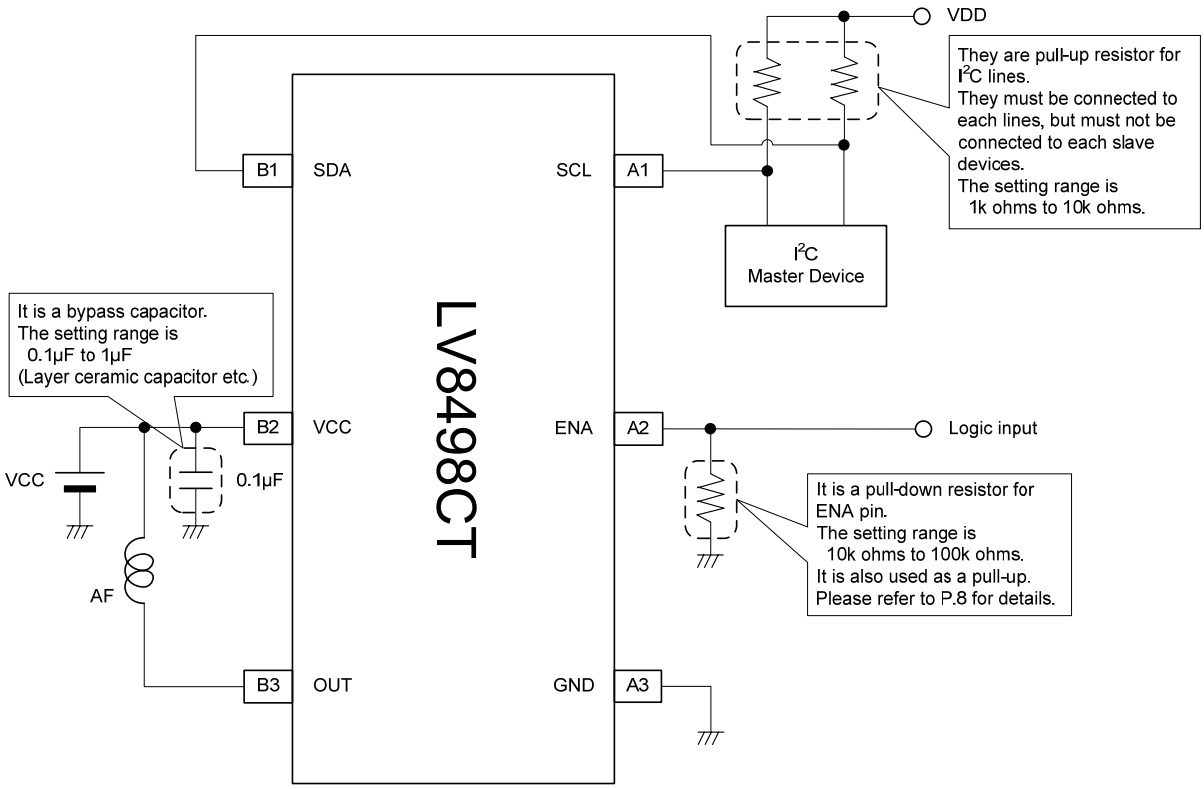


Figure 21. Typical Application Circuit

Evaluation Board

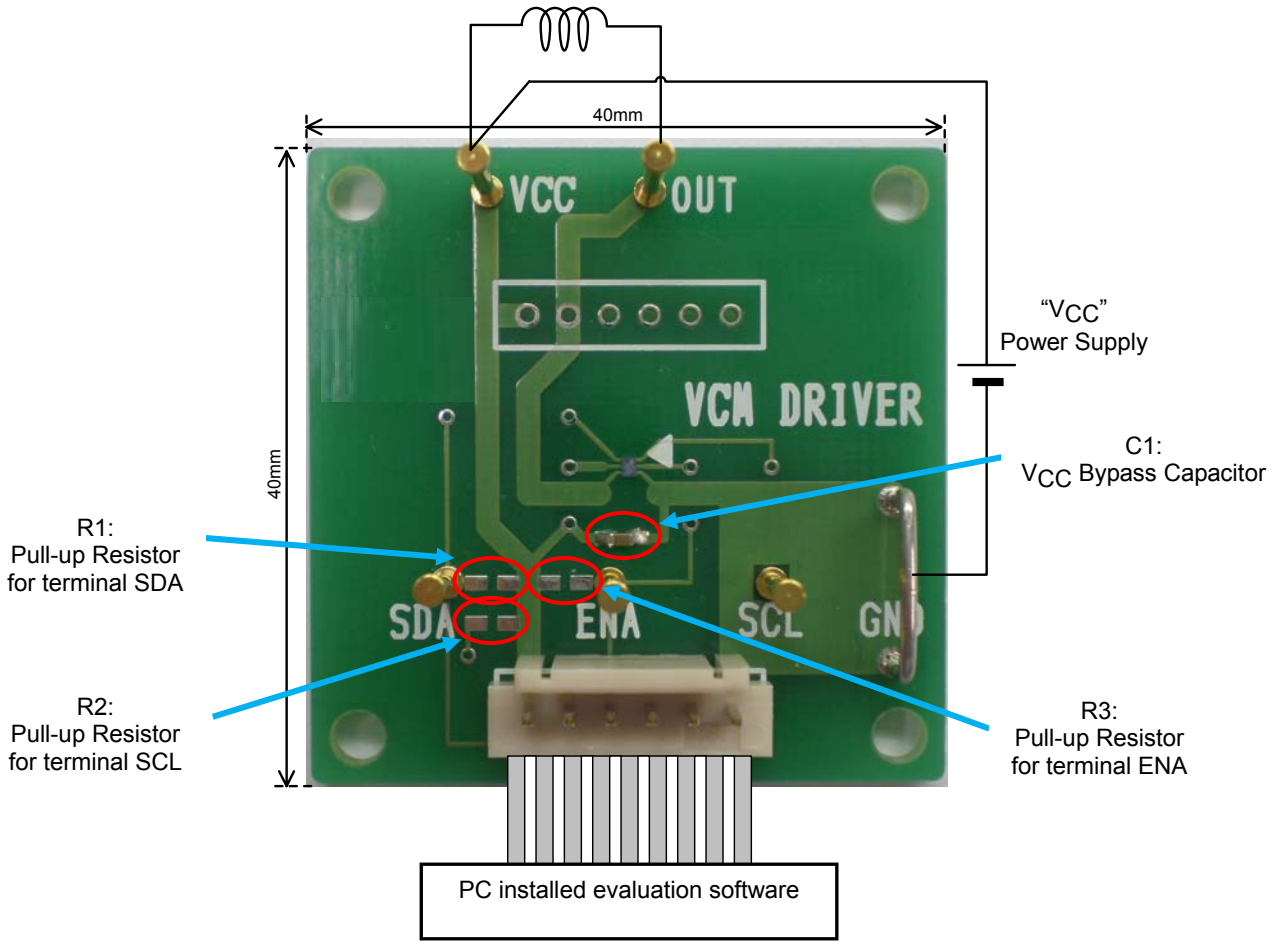


Figure 22. Evaluation Board overview

Bill of Materials for LV8498CT Evaluation Board

Designator	Quantity	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	Lead Free
C1	1	VCC Bypass Capacitor	0.1μF, 50V	±10%		Murata	GRM188B31H104KA92*	Yes	Yes
R1(*)		Pull-up Resistor for terminal SDA	1kΩ 1/10W	±5%		KOA	RK73B1JT**102J	Yes	Yes
R2(*)		Pull-up Resistor for terminal SCL	1kΩ 1/10W	±5%		KOA	RK73B1JT**102J	Yes	Yes
R3(**)		Pull-up Resistor for terminal ENA	100kΩ 1/10W	±5%		KOA	RK73B1JT**104J	Yes	Yes
IC1	1	Motor Driver				ON semiconductor	LV8498CT	No	Yes
CNCT1	1	Pin Header Straight Type				HIROSE	DF1-6P-2.5DSA		
TP1-TP5	5	Test Point				MAC8	ST-1-3		

(*) It is the part we recommend. If I^2C Master device does not have pull-up resistors for SDA and SCL lines, mount on the space.

(**) It is the part we recommend. If the ENA pin is to be used with pull-up. Refer to P.8.

Evaluation Board circuit

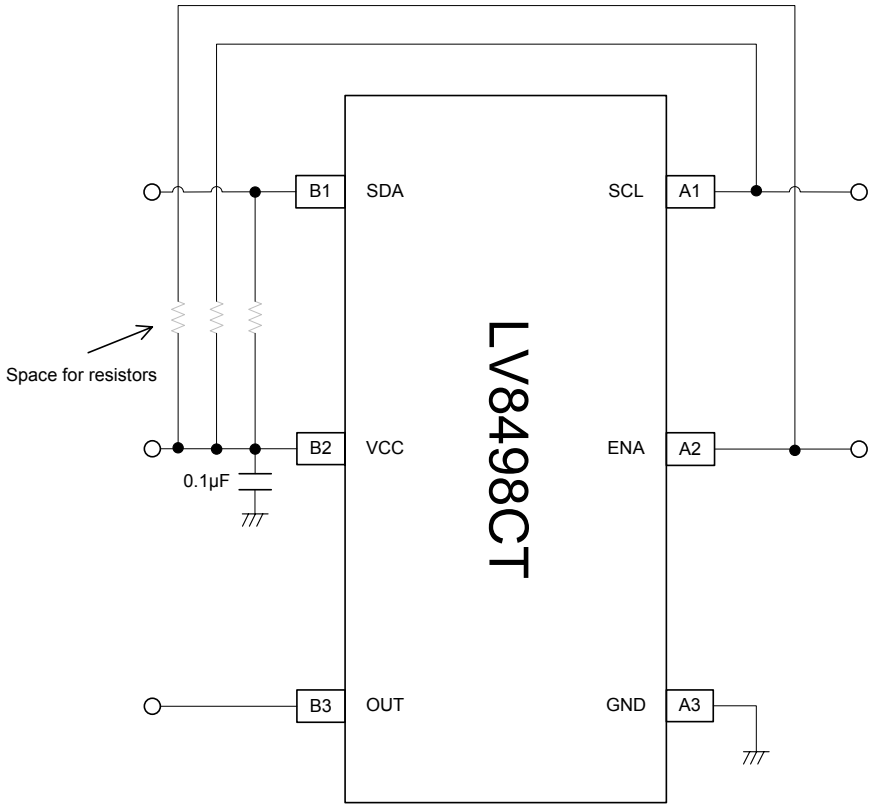


Figure 23. Evaluation Board circuit schematic

Operation Guide

- Connect AF-VCM with OUT and V_{CC}.
- Connect a power supply with V_{CC}.
  Connect GND line with GND pin.
- If you use the master device we provided, connect USB adapter with the evaluation board.
  If you have the original master device, connect I^2C lines with SDA pin and SCL pin.
  Check if pull-up resistors have been connected to the lines. If not, mount R1 and R2 on the evaluation board.
  The USB adapter we provided has built-in resistors. Therefore, you do not need to mount any resistor.
- Confirm that ENA pin is not OPEN. And supply power.
  After that, if the ENA pin is pull-down, input High signal to the pin.
  If the pin is pull-up, transfer zero-code to all data and ENABLE “H”.
  When you transfer ENABLE “L”, current flows from V_{CC} to GND.
- If you have the original master device, refer to “Operation Description” from P.8 and create I^2C program.

The points of attention to design applications

- V_{CC}, GND and OUT where a large current flows are laid out fat and short as much as possible.
- V_{CC} bypass capacitor should be mounted as near as possible to the IC.
- Do not exceed the absolute maximum ratings under no circumstance. The terminal OUT can exceed V_{CC} due to reversed voltage or regenerated current. Refer to P.8.
- SCL and other fast switching digital signals should be shielded from other parts of the board.