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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

MITSUBISHI 16-BIT SINGLE-CHIP MICROCOMPUTER
M16C FAMILY

M30201
Group

User's manual

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How to Use This Manual

This user's manual is written for the M30201 group.

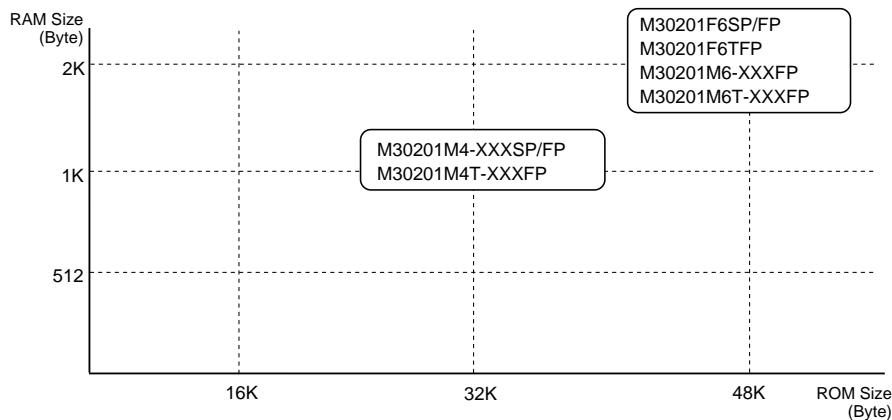
The reader of this manual is expected to have the basic knowledge of electric and logic circuits and microcomputers.

This manual is for the use of the models below.

- M30201M4-XXXSP/FP
- M30201M4T-XXXFP
- M30201M6-XXXFP
- M30201M6T-XXXFP
- M30201F6SP/FP
- M30201F6TFP

These products have similar features except for the memories, which differ from one product to another. This manual gives descriptions of M30201M4-XXXSP. Memories built-in are as shown below. Be careful when writing a program, as the memories have different capacities.

The figure of each register configuration describes its functions, contents at reset, and attributes as follows :



This manual comprises of eight chapters. Use the suggested chapters as a reference for the following topics:

- Bit attribute

R.....Read
 O.....Possible to read
 X.....Impossible to read

W.....Write
 O.....Possible to write
 X.....Impossible to write

One-shot start flag

Bit	Symbol	Address	When reset	Bit attribute			
b7	ONSF	0382 ₁₆	00X00000 ₂	R, W			
b6					TA0OS	Timer A0 one-shot start flag	O, O
b5					TA1OS	Timer A1 one-shot start flag	O, O
b4					TA2OS	Timer A2 one-shot start flag	O, O
b3					TA3OS	Timer A3 one-shot start flag	O, O
b2					TA4OS	Timer A4 one-shot start flag	O, O
b1	Nothing is assigned. In an attempt to write to this bit, write "0". The value, if read, turns out to be indeterminate.			-			
b0	TA0TGL	Timer A0 event/trigger select bit	b7b6 0 0 : Input on TA0 _{IN} is selected (Note) 0 1 : TB2 overflow is selected 1 0 : TA4 overflow is selected 1 1 : TA1 overflow is selected	O, O			
	TA0TGH			O, O			

Note: Set the corresponding port direction register to "0".

This manual comprises of five chapters. Use the suggested chapters as a reference for the following topics:

- * To understand hardware specifications Chapter 1 Hardware
- * To understand the basic way of using peripheral features and the operation timing Chapter 2 Peripheral Functions Usage
- * To observe applications of peripheral features Chapter 3 Examples of Peripheral Functions Applications
- * To understand interrupt timing in detail Chapter 4 Interrupts
- * To understand standard data Chapter 5 Standard Characteristics

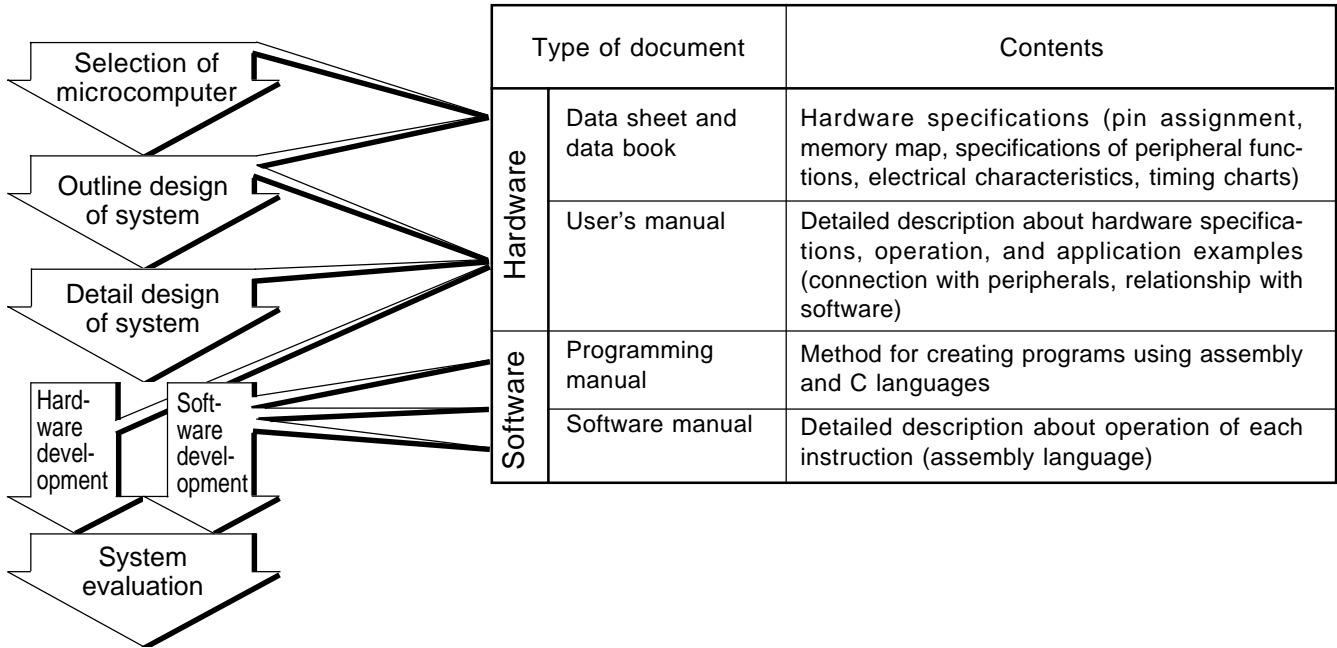
This manual includes a quick reference immediately following the Table of Contents, indicate the page of the topic to be pursued.

- * To find a page describing a specific register by the register address Quick Reference to Pages Classified by Address

M16C Family-related document list

Usages

(Microcomputer development flow)



M16C Family Line-up

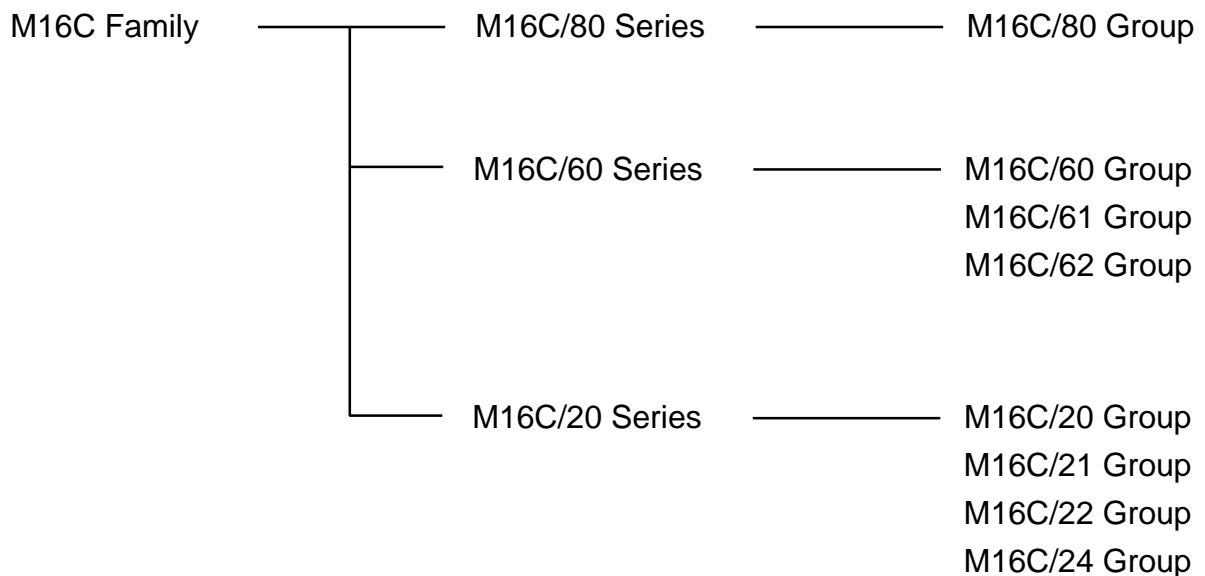


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03B9 ₁₆			03F9 ₁₆		
03BA ₁₆			03FA ₁₆		
03BB ₁₆			03FB ₁₆		
03BC ₁₆			03FC ₁₆	Pull-up control register 0 (PUR0)	
03BD ₁₆			03FD ₁₆	Pull-up control register 1 (PUR1)	
03BE ₁₆			03FE ₁₆	Pull-up control register 2 (PUR2)	
03BF ₁₆			03FF ₁₆		

Note: This register is only exist in flash memory version.

Chapter 1

Hardware

Description

Description

The M30201 group of single-chip microcomputers are built using the high-performance silicon gate CMOS process using a M16C/60 Series CPU core. M30201 group is packaged in a 52-pin plastic molded SDIP, or 56-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, they are capable of executing instructions at high speed.

The M30201 group includes a wide range of products with different internal memory types and sizes and various package types.

Features

- Basic machine instructions Compatible with the M16C/60 series
- Memory capacity ROM/RAM (See figure 1.4. ROM expansion.)
- Shortest instruction execution time 100ns (f(XIN)=10MHz)
- Supply voltage 4.0 to 5.5V (f(XIN)=10MHz) :mask ROM version
 2.7 to 5.5V (f(XIN)=3.5MHz) :mask ROM version
 4.0 to 5.5V (f(XIN)=10MHz) :flash memory version
- Interrupts 13 internal and 3 external interrupt sources, 4 software
 (including key input interrupt)
- Multifunction 16-bit timer Timer A x 1, timer B x 2, timer X x 3
- Clock output
- Serial I/O 1 channel for UART or clock synchronous, 1 for UART
- A-D converter 10 bits X 8 channels (Expandable up to 13 channels)
- Watchdog timer 1 line
- Programmable I/O 43 lines
- LED drive ports 8 ports
- Clock generating circuit 2 built-in clock generation circuits
 (built-in feedback resistor, and external ceramic or quartz oscillator)

Applications

Home appliances, Audio, office equipment, Automobiles

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Description

Pin Configuration

Figures 1.1 to 1.2 show the pin configurations (top view).

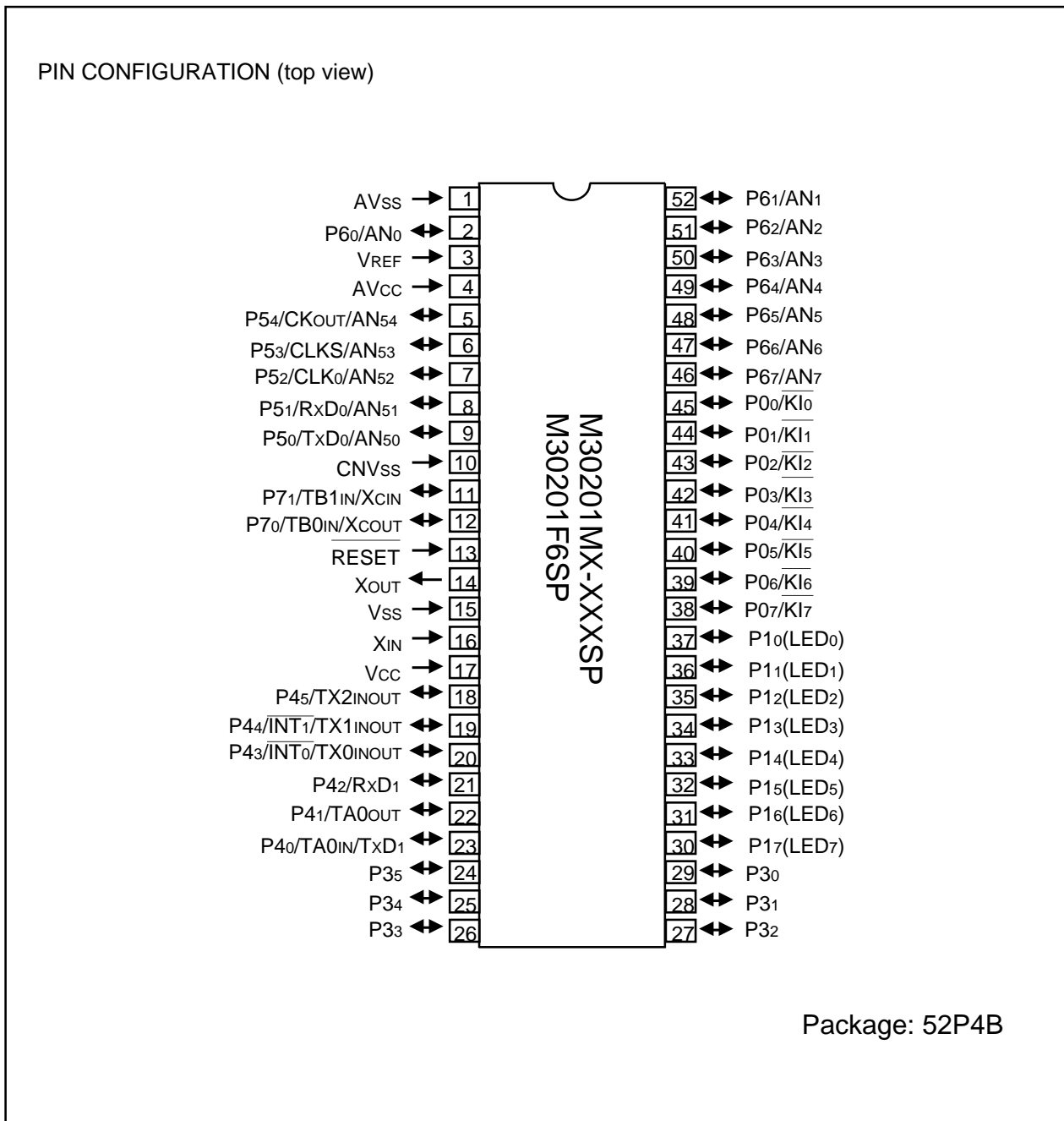


Figure 1.1. Pin configuration for the M30201 group (shrink DIP product) (top view)

Description

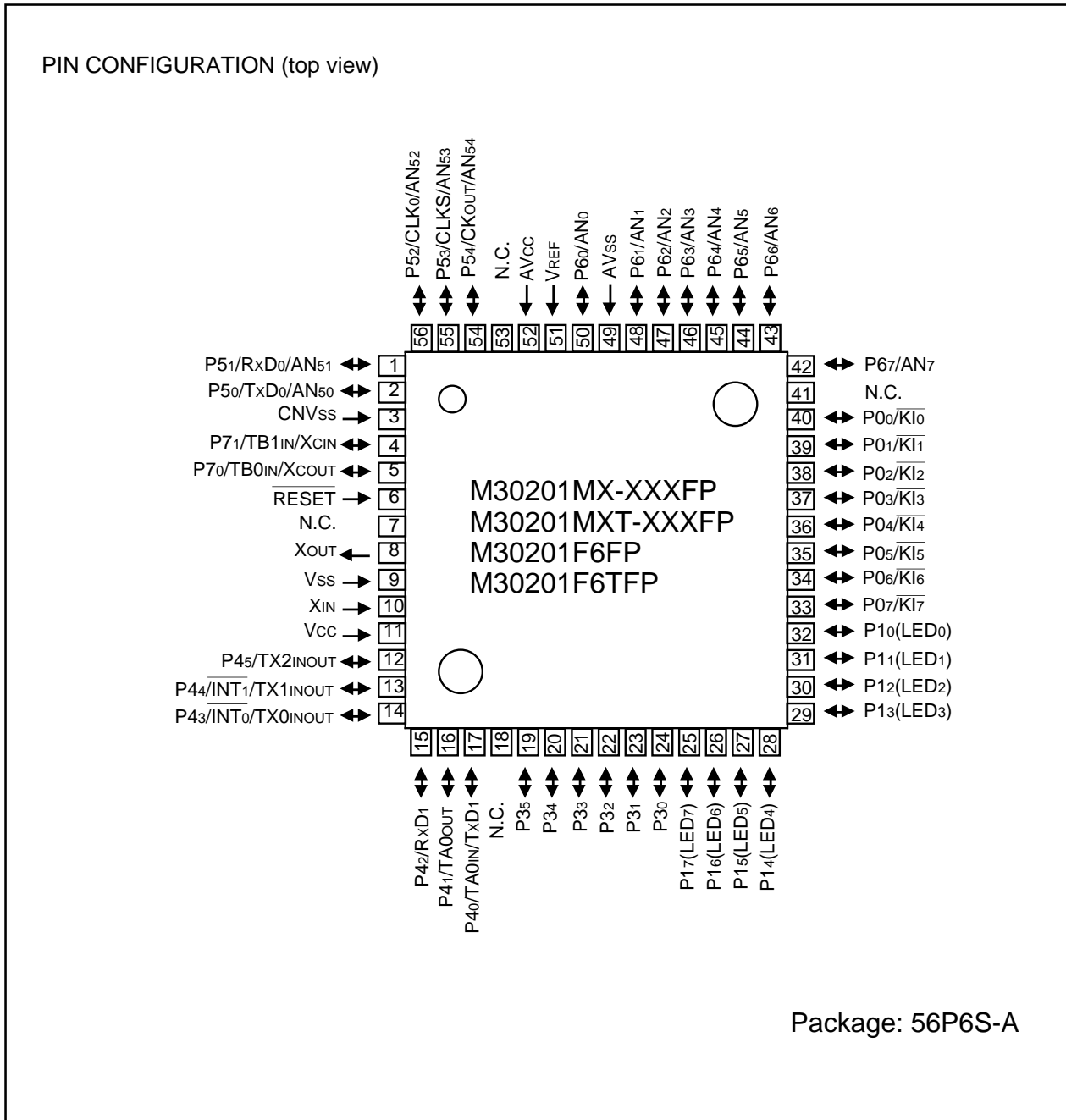


Figure 1.2. Pin configuration for the M30201 group (QFP product) (top view)

Description

Block Diagram

Figure 1.3 is a block diagram of the M30201 group.

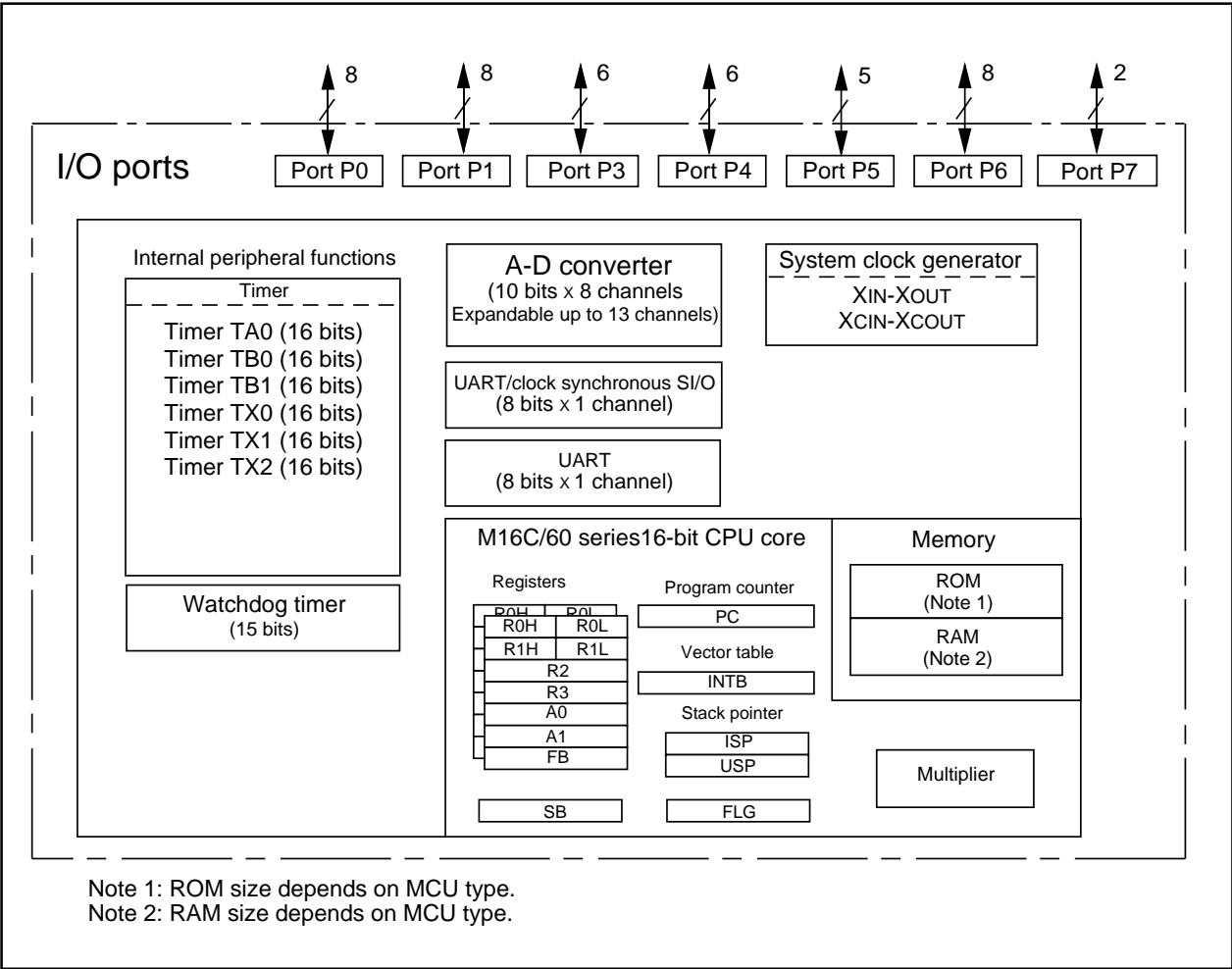


Figure 1.3. Block diagram for the M30201 group

Description

Performance Outline

Table 1.1 is performance outline of M30201 group.

Table 1.1. Performance outline of M30201 group

Item		Performance
Number of basic instructions		91 instructions
Shortest instruction execution time		100ns (f(XIN)=10MHz)
Memory capacity	ROM	(See figure 4. ROM expansion.)
	RAM	(See figure 4. ROM expansion.)
I/O port	P0 to P7	43 lines
Multifunction timer	TA0	16 bits x 1
	TB0, TB1	16 bits x 2
	TX0, TX1, TX2	16 bits x 3
Serial I/O	UART0	(UART or clock synchronous) x 1
	UART1	UART x 1
A-D converter		10 bits x 8 channels (Expandable up to 13 channels)
Watchdog timer		15 bits x 1 (with prescaler)
Interrupt		13 internal and 3 external sources, 4 software sources
Clock generating circuit		2 built-in clock generation circuits (built-in feedback resistor, and external ceramic or quartz oscillator)
Supply voltage		4.0 to 5.5V (f(XIN)=10MHz) :mask ROM version 2.7 to 5.5V (f(XIN)=3.5MHz) :mask ROM version 4.0 to 5.5V (f(XIN)=10MHz) :flash memory version
Power consumption		11mW (f(XIN)=3.5MHz , Vcc=3V) :mask ROM version 95mW (f(XIN)=10MHz, Vcc=5V) :flash memory version
I/O characteristics	I/O withstand voltage	5V
	Output current	5mA (15mA:LED drive port)
Device configuration		CMOS silicon gate
Package		52-pin plastic mold SDIP 56-pin plastic mold QFP

Description

Mitsubishi plans to release the following products in the M30201 group:

- (1) Support for mask ROM version and flash memory version
- (2) ROM capacity
- (3) Package

- 52P4B : Plastic molded SDIP (mask ROM version and flash memory version)
- 56P6S-A : Plastic molded QFP (mask ROM version and flash memory version)

Apr. 2001

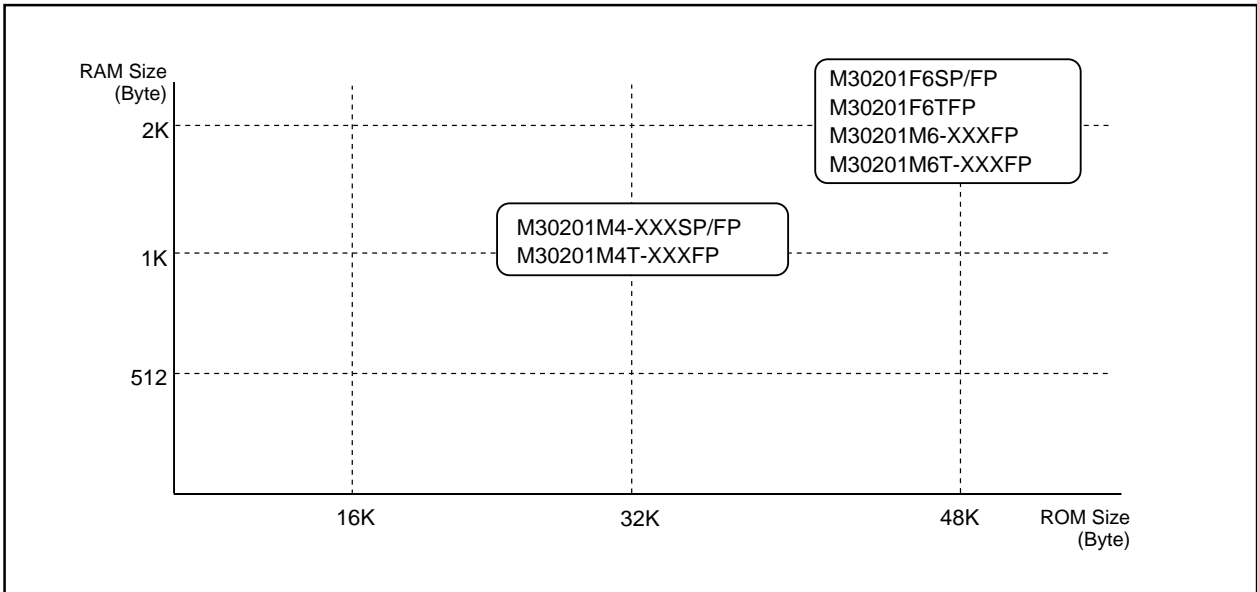


Figure 1.4. ROM expansion

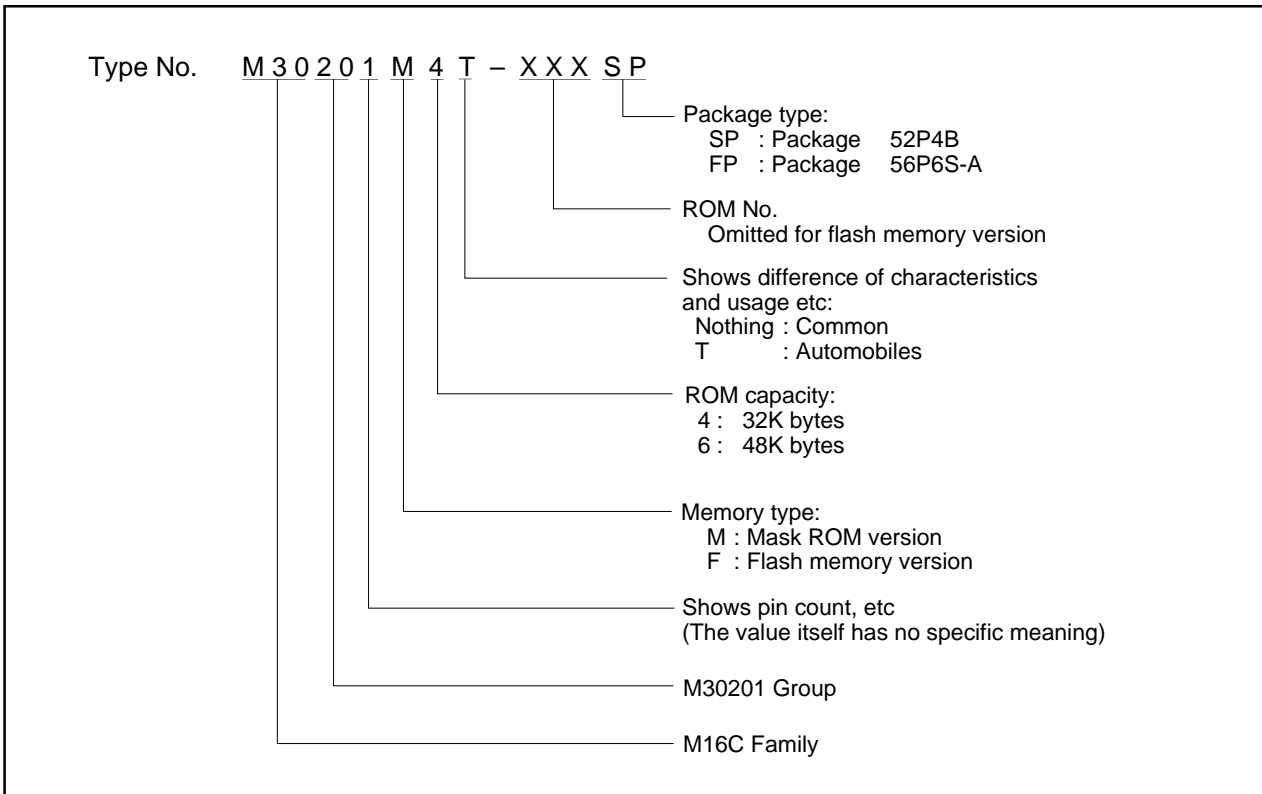


Figure 1.5. Type No., memory size, and package

Pin Description**Pin Description**

Pin name	Signal name	I/O type	Function
Vcc, Vss	Power supply input		Supply 2.7 to 5.5 V to the Vcc pin. Supply 0 V to the Vss pin.
CNVss	CNVss	Input	Connect it to the Vss pin.
RESET	Reset input	Input	A "L" on this input resets the microcomputer.
XIN XOUT	Clock input Clock output	Input Output	These pins are provided for the main clock generating circuit. Connect a ceramic resonator or crystal between the XIN and the XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
AVCC	Analog power supply input		This pin is a power supply input for the A-D converter. Connect it to Vcc.
AVss	Analog power supply input		This pin is a power supply input for the A-D converter. Connect it to Vss.
VREF	Reference voltage input	Input	This pin is a reference voltage input for the A-D converter.
P00 to P07	I/O port P0	Input/output	This is an 8-bit CMOS I/O port. It has an input/output port direction register that allows the user to set each pin for input or output individually. When set for input, the user can specify in units of four bits via software whether or not they are tied to a pull-up resistor.
P10 to P17	I/O port P1	Input/output	This is an 8-bit I/O port equivalent to P0.
P30 to P35	I/O port P3	Input/output	This is a 6-bit I/O port equivalent to P0.
P40 to P45	I/O port P4	Input/output	This is a 6-bit I/O port equivalent to P0. The P40 pin is shared with timer A0 input and serial I/O output TxD1. The P41 pin is shared with timer A0 output. The P42 pin is shared with serial I/O input RxD1. The P43 pin is shared with external interrupt INT0 and timer X0 input/output TX0INOUT. The P44 pin is shared with external interrupt INT1 and timer X1 input/output TX1INOUT. The P45 pin is shared with timer X2 input/output TX2INOUT.
P50 to P54	I/O port P5	Input/output	This is a 5-bit I/O port equivalent to P0. The P50, P51, P52, and P53 pins are shared with serial I/O pins TxD0, RxD0, CLK0, and CLKS. The P54 pin is shared with clock output CLKOUT. Also, these pins are shared with analog input pins AN50 through AN54.
P60 to P67	I/O port P6	Input/output	This is an 8-bit I/O port equivalent to P0. These pins are shared with analog input pins AN0 through AN7.
P70 to P71	I/O port P7	Input/output	This is a 2-bit I/O port equivalent to P0. These pins are used for input/output to and from the oscillator circuit for the clock. Connect a crystal oscillator between the XCIN and the XCOU pins.

Memory

Operation of Functional Blocks

The M30201 accommodates certain units in a single chip. These units include ROM and RAM to store instructions and data and the central processing unit (CPU) to execute arithmetic/logic operations. Also included are peripheral units such as timers, serial I/O, A-D converter, and I/O ports.

The following explains each unit.

Memory

Figure 1.6 is a memory map of the M30201. The address space extends the 1M bytes from address 00000_{16} to $FFFFFF_{16}$. From $FFFFFF_{16}$ down is ROM. For example, in the M30201M4-XXXSP, there is 32K bytes of internal ROM from $F8000_{16}$ to $FFFFFF_{16}$. The vector table for fixed interrupts such as the reset are mapped to $FFFDC_{16}$ to $FFFFFF_{16}$. The starting address of the interrupt routine is stored here. The address of the vector table for timer interrupts, etc., can be set as desired using the internal register (INTB). See the section on interrupts for details.

From 00400_{16} up is RAM. For example, in the M30201M4-XXXSP, there is 1K byte of internal RAM from 00400_{16} to $007FF_{16}$. In addition to storing data, the RAM also stores the stack used when calling subroutines and when interrupts are generated.

The SFR area is mapped to 00000_{16} to $003FF_{16}$. This area accommodates the control registers for peripheral devices such as I/O ports, A-D converter, serial I/O, and timers, etc. Any part of the SFR area that is not occupied is reserved and cannot be used for other purposes.

The special page vector table is mapped to $FFE00_{16}$ to $FFFDB_{16}$. If the starting addresses of subroutines or the destination addresses of jumps are stored here, subroutine call instructions and jump instructions can be used as 2-byte instructions, reducing the number of program steps.

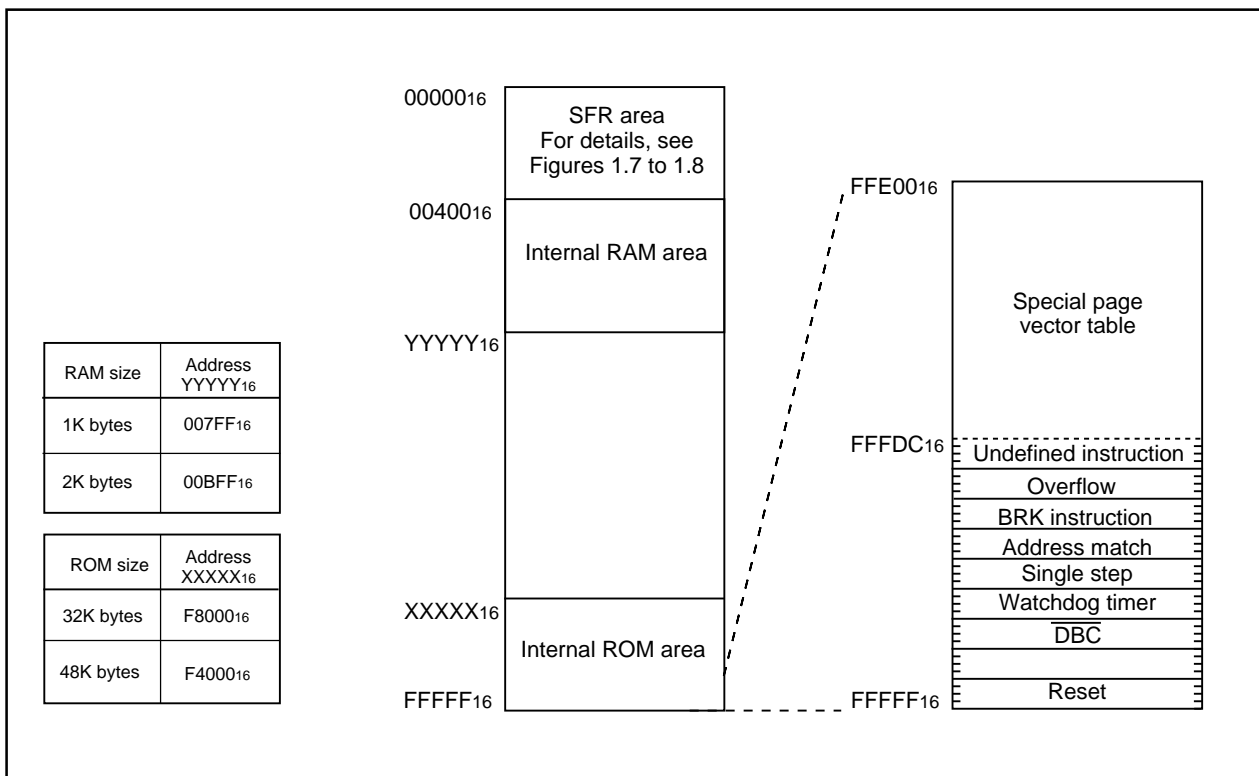


Figure 1.6. Memory map

Memory

0000 ₁₆		0040 ₁₆	
0001 ₁₆		0041 ₁₆	
0002 ₁₆		0042 ₁₆	
0003 ₁₆		0043 ₁₆	
0004 ₁₆	Processor mode register 0 (PM0)	0044 ₁₆	
0005 ₁₆	Processor mode register 1 (PM1)	0045 ₁₆	
0006 ₁₆	System clock control register 0 (CM0)	0046 ₁₆	
0007 ₁₆	System clock control register 1 (CM1)	0047 ₁₆	
0008 ₁₆		0048 ₁₆	
0009 ₁₆	Address match interrupt enable register (AIER)	0049 ₁₆	
000A ₁₆	Protect register (PRCR)	004A ₁₆	
000B ₁₆		004B ₁₆	
000C ₁₆		004C ₁₆	
000D ₁₆		004D ₁₆	Key input interrupt control register (KUPIC)
000E ₁₆	Watchdog timer start register (WDTS)	004E ₁₆	A-D conversion interrupt control register (ADIC)
000F ₁₆	Watchdog timer control register (WDC)	004F ₁₆	
0010 ₁₆		0050 ₁₆	
0011 ₁₆	Address match interrupt register 0 (RMAD0)	0051 ₁₆	UART0 transmit interrupt control register (S0TIC)
0012 ₁₆		0052 ₁₆	UART0 receive interrupt control register (S0RIC)
0013 ₁₆		0053 ₁₆	UART1 transmit interrupt control register (S1TIC)
0014 ₁₆		0054 ₁₆	UART1 receive interrupt control register (S1RIC)
0015 ₁₆	Address match interrupt register 1 (RMAD1)	0055 ₁₆	Timer A0 interrupt control register (TA0IC)
0016 ₁₆		0056 ₁₆	Timer X0 interrupt control register (TX0IC)
0017 ₁₆		0057 ₁₆	Timer X1 interrupt control register (TX1IC)
0018 ₁₆		0058 ₁₆	Timer X2 interrupt control register (TX2IC)
0019 ₁₆		0059 ₁₆	
001A ₁₆		005A ₁₆	Timer B0 interrupt control register (TB0IC)
001B ₁₆		005B ₁₆	Timer B1 interrupt control register (TB1IC)
001C ₁₆		005C ₁₆	
001D ₁₆		005D ₁₆	INT0 interrupt control register (INT0IC)
001E ₁₆		005E ₁₆	INT1 interrupt control register (INT1IC)
001F ₁₆		005F ₁₆	
0020 ₁₆			
0021 ₁₆			
0022 ₁₆			
0023 ₁₆			
0024 ₁₆			
0025 ₁₆			
0026 ₁₆			
0027 ₁₆			
0028 ₁₆			
0029 ₁₆			
002A ₁₆			
002B ₁₆			
002C ₁₆			
002D ₁₆			
002E ₁₆			
002F ₁₆			
0030 ₁₆			
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0038 ₁₆			
0039 ₁₆			
003A ₁₆			
003B ₁₆			
003C ₁₆			
003D ₁₆			
003E ₁₆			
003F ₁₆			

Note: Locations in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

Figure 1.7. Location of peripheral unit control registers (1)

Memory

0380 ₁₆	Count start flag (TABSR)	03C0 ₁₆	A-D register 0 (AD0)
0381 ₁₆	Clock prescaler reset flag (CPSRF)	03C1 ₁₆	
0382 ₁₆	One-shot start flag (ONSF)	03C2 ₁₆	A-D register 1 (AD1)
0383 ₁₆	Trigger select register (TRGSR)	03C3 ₁₆	
0384 ₁₆	Up-down flag (UDF)	03C4 ₁₆	A-D register 2 (AD2)
0385 ₁₆		03C5 ₁₆	
0386 ₁₆	Timer A0 (TA0)	03C6 ₁₆	A-D register 3 (AD3)
0387 ₁₆		03C7 ₁₆	
0388 ₁₆	Timer X0 (TX0)	03C8 ₁₆	A-D register 4 (AD4)
0389 ₁₆		03C9 ₁₆	
038A ₁₆	Timer X1 (TX1)	03CA ₁₆	A-D register 5 (AD5)
038B ₁₆		03CB ₁₆	
038C ₁₆	Timer X2 (TX2)	03CC ₁₆	A-D register 6 (AD6)
038D ₁₆		03CD ₁₆	
038E ₁₆	Clock divided counter (CDC)	03CE ₁₆	A-D register 7 (AD7)
038F ₁₆		03CF ₁₆	
0390 ₁₆	Timer B0 (TB0)	03D0 ₁₆	
0391 ₁₆		03D1 ₁₆	
0392 ₁₆	Timer B1 (TB1)	03D2 ₁₆	
0393 ₁₆		03D3 ₁₆	
0394 ₁₆		03D4 ₁₆	A-D control register 2 (ADCON2)
0395 ₁₆		03D5 ₁₆	
0396 ₁₆	Timer A0 mode register (TA0MR)	03D6 ₁₆	A-D control register 0 (ADCON0)
0397 ₁₆	Timer X0 mode register (TX0MR)	03D7 ₁₆	A-D control register 1 (ADCON1)
0398 ₁₆	Timer X1 mode register (TX1MR)	03D8 ₁₆	
0399 ₁₆	Timer X2 mode register (TX2MR)	03D9 ₁₆	
039A ₁₆		03DA ₁₆	
039B ₁₆	Timer B0 mode register (TB0MR)	03DB ₁₆	
039C ₁₆	Timer B1 mode register (TB1MR)	03DC ₁₆	
039D ₁₆		03DD ₁₆	
039E ₁₆		03DE ₁₆	
039F ₁₆		03DF ₁₆	
03A0 ₁₆	UART0 transmit/receive mode register (U0MR)	03E0 ₁₆	Port P0 (P0)
03A1 ₁₆	UART0 bit rate generator (U0BRG)	03E1 ₁₆	Port P1 (P1)
03A2 ₁₆	UART0 transmit buffer register (U0TB)	03E2 ₁₆	Port P0 direction register (PD0)
03A3 ₁₆		03E3 ₁₆	Port P1 direction register (PD1)
03A4 ₁₆	UART0 transmit/receive control register 0 (U0C0)	03E4 ₁₆	Port P2 (P2) (Reserved)
03A5 ₁₆	UART0 transmit/receive control register 1 (U0C1)	03E5 ₁₆	Port P3 (P3)
03A6 ₁₆	UART0 receive buffer register (U0RB)	03E6 ₁₆	Port P2 direction register (PD2) (Reserved)
03A7 ₁₆		03E7 ₁₆	Port P3 direction register (PD3)
03A8 ₁₆	UART1 transmit/receive mode register (U1MR)	03E8 ₁₆	Port P4 (P4)
03A9 ₁₆	UART1 bit rate generator (U1BRG)	03E9 ₁₆	Port P5 (P5)
03AA ₁₆	UART1 transmit buffer register (U1TB)	03EA ₁₆	Port P4 direction register (PD4)
03AB ₁₆		03EB ₁₆	Port P5 direction register (PD5)
03AC ₁₆	UART1 transmit/receive control register 0 (U1C0)	03EC ₁₆	Port P6 (P6)
03AD ₁₆	UART1 transmit/receive control register 1 (U1C1)	03ED ₁₆	Port P7 (P7)
03AE ₁₆	UART1 receive buffer register (U1RB)	03EE ₁₆	Port P6 direction register (PD6)
03AF ₁₆		03EF ₁₆	Port P7 direction register (PD7)
03B0 ₁₆	UART transmit/receive control register 2 (UCON)	03F0 ₁₆	
03B1 ₁₆		03F1 ₁₆	
03B2 ₁₆		03F2 ₁₆	
03B3 ₁₆		03F3 ₁₆	
03B4 ₁₆	Flash memory control register 0 (FCON0) (Note1)	03F4 ₁₆	
03B5 ₁₆	Flash memory control register 1 (FCON1) (Note1)	03F5 ₁₆	
03B6 ₁₆	Flash command register (FCMD) (Note)	03F6 ₁₆	
03B7 ₁₆		03F7 ₁₆	
03B8 ₁₆		03F8 ₁₆	
03B9 ₁₆		03F9 ₁₆	
03BA ₁₆		03FA ₁₆	
03BB ₁₆		03FB ₁₆	
03BC ₁₆		03FC ₁₆	Pull-up control register 0 (PUR0)
03BD ₁₆		03FD ₁₆	Pull-up control register 1 (PUR1)
03BE ₁₆		03FE ₁₆	Port P1 drive control register (DRR)
03BF ₁₆		03FF ₁₆	

Note 1: This register is only exist in flash memory version.
Note 2: Locations in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

Figure 1.8. Location of peripheral unit control registers (2)

CPU

Central Processing Unit (CPU)

The CPU has a total of 13 registers shown in Figure 1.9. Seven of these registers (R0, R1, R2, R3, A0, A1, and FB) come in two sets; therefore, these have two register banks.

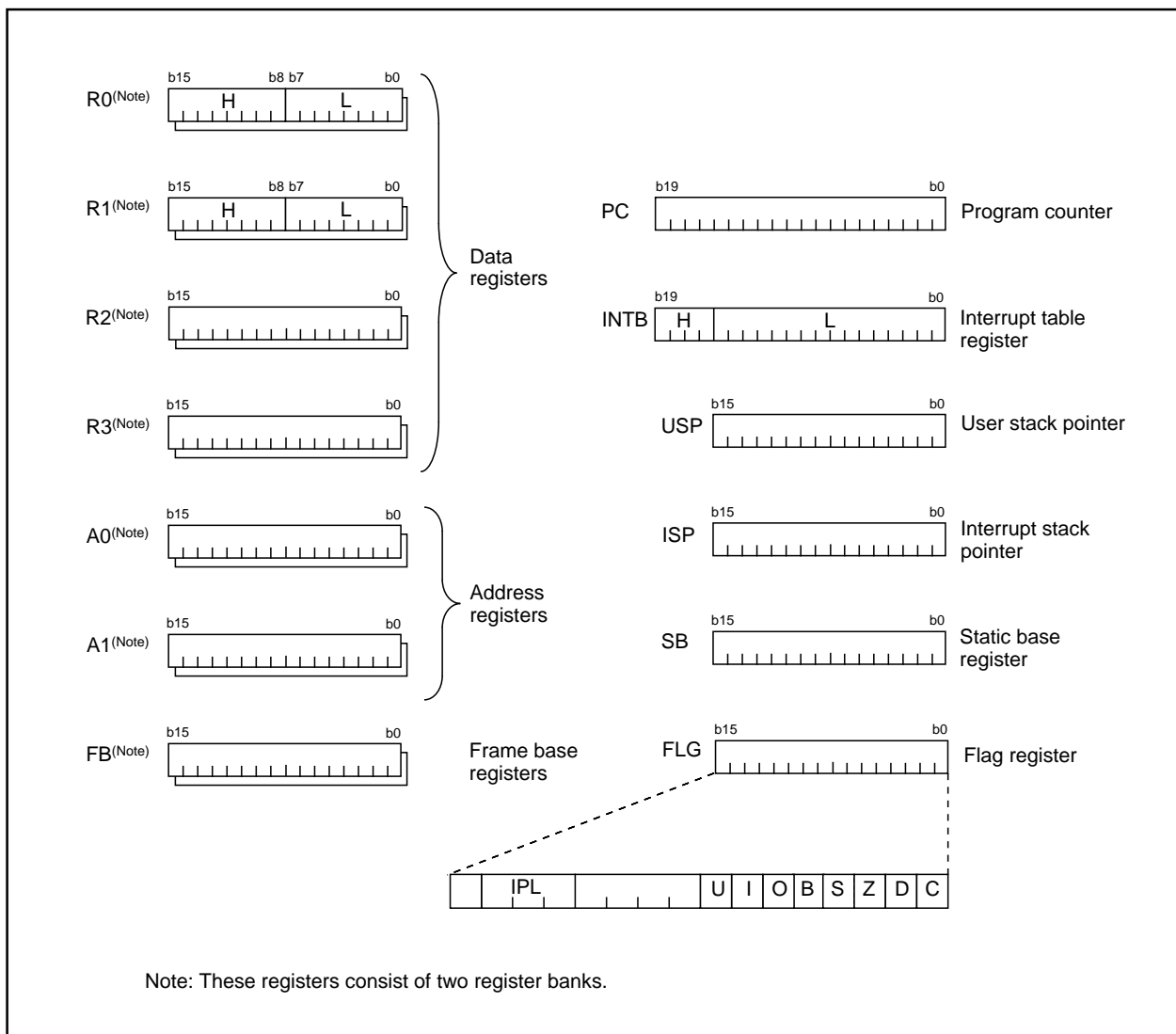


Figure 1.9. Central processing unit register

(1) Data registers (R0, R0H, R0L, R1, R1H, R1L, R2, and R3)

Data registers (R0, R1, R2, and R3) are configured with 16 bits, and are used primarily for transfer and arithmetic/logic operations.

Registers R0 and R1 each can be used as separate 8-bit data registers, high-order bits as (R0H, R1H), and low-order bits as (R0L, R1L). In some instructions, registers R2 and R0, as well as R3 and R1 can use as 32-bit data registers (R2R0, R3R1).

(2) Address registers (A0 and A1)

Address registers (A0 and A1) are configured with 16 bits, and have functions equivalent to those of data registers. These registers can also be used for address register indirect addressing and address register relative addressing.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

(3) Frame base register (FB)

Frame base register (FB) is configured with 16 bits, and is used for FB relative addressing.

(4) Program counter (PC)

Program counter (PC) is configured with 20 bits, indicating the address of an instruction to be executed.

(5) Interrupt table register (INTB)

Interrupt table register (INTB) is configured with 20 bits, indicating the start address of an interrupt vector table.

(6) Stack pointer (USP/ISP)

Stack pointer comes in two types: user stack pointer (USP) and interrupt stack pointer (ISP), each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by a stack pointer select flag (U flag).

This flag is located at the position of bit 7 in the flag register (FLG).

(7) Static base register (SB)

Static base register (SB) is configured with 16 bits, and is used for SB relative addressing.

(8) Flag register (FLG)

Flag register (FLG) is configured with 11 bits, each bit is used as a flag. Figure 1.10 shows the flag register (FLG). The following explains the function of each flag:

• Bit 0: Carry flag (C flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

• Bit 1: Debug flag (D flag)

This flag enables a single-step interrupt.

When this flag is "1", a single-step interrupt is generated after instruction execution. This flag is cleared to "0" when the interrupt is acknowledged.

• Bit 2: Zero flag (Z flag)

This flag is set to "1" when an arithmetic operation resulted in 0; otherwise, cleared to "0".

• Bit 3: Sign flag (S flag)

This flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, cleared to "0".

• Bit 4: Register bank select flag (B flag)

This flag chooses a register bank. Register bank 0 is selected when this flag is "0"; register bank 1 is selected when this flag is "1".

• Bit 5: Overflow flag (O flag)

This flag is set to "1" when an arithmetic operation resulted in overflow; otherwise, cleared to "0".

• Bit 6: Interrupt enable flag (I flag)

This flag enables a maskable interrupt.

An interrupt is disabled when this flag is "0", and is enabled when this flag is "1". This flag is cleared to "0" when the interrupt is acknowledged.

CPU

- **Bit 7: Stack pointer select flag (U flag)**

Interrupt stack pointer (ISP) is selected when this flag is “0” ; user stack pointer (USP) is selected when this flag is “1”.

This flag is cleared to “0” when a hardware interrupt is acknowledged or an INT instruction of software interrupt Nos. 0 to 31 is executed.

- **Bits 8 to 11: Reserved area**

- **Bits 12 to 14: Processor interrupt priority level (IPL)**

Processor interrupt priority level (IPL) is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than the processor interrupt priority level (IPL), the interrupt is enabled.

- **Bit 15: Reserved area**

The C, Z, S, and O flags are changed when instructions are executed. See the software manual for details.

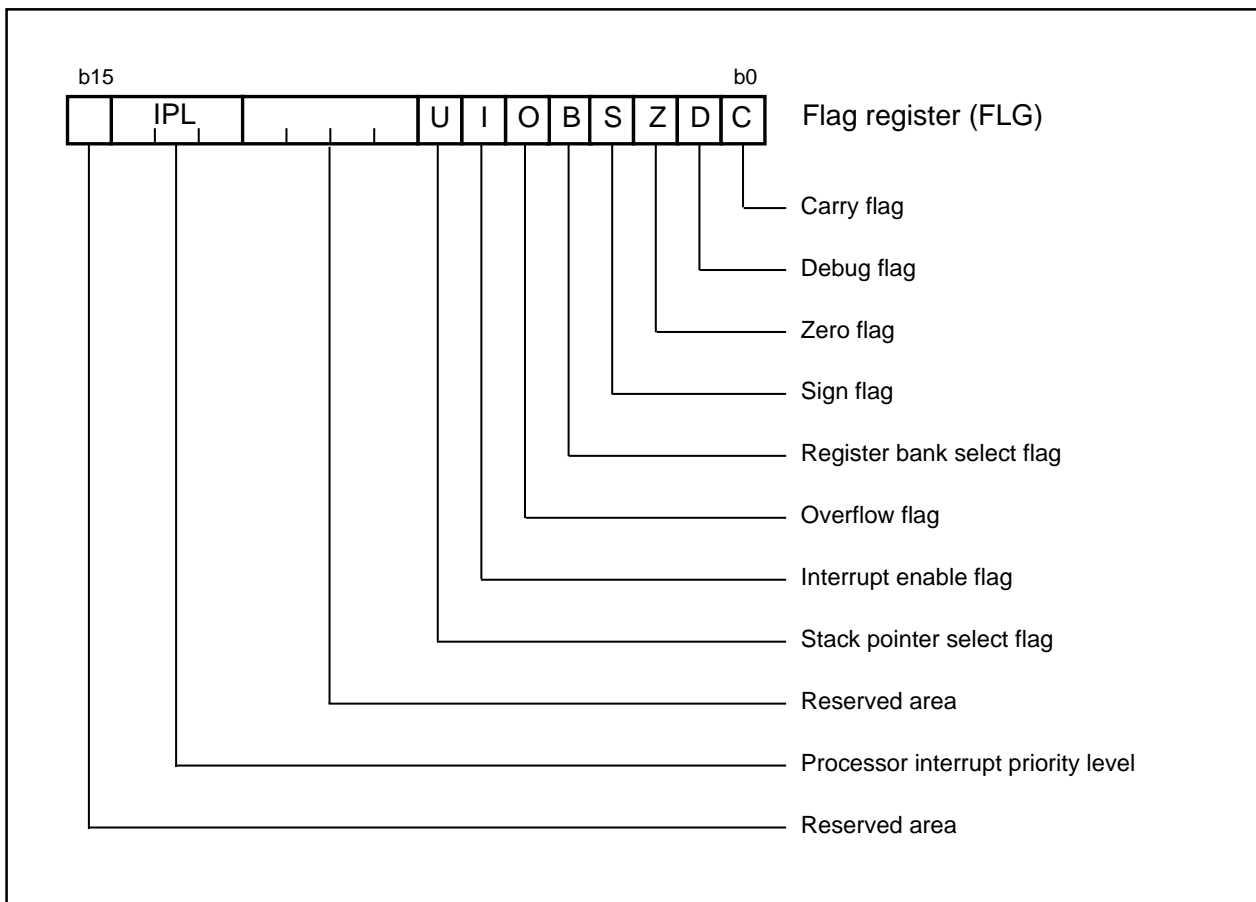


Figure 1.10. Flag register (FLG)

Reset

Reset

There are two kinds of resets; hardware and software. In both cases, operation is the same after the reset. (See "Software Reset" for details of software resets.) This section explains on hardware resets.

When the supply voltage is in the range where operation is guaranteed, a reset is effected by holding the reset pin level "L" (0.2V_{CC} max.) for at least 20 cycles. When the reset pin level is then returned to the "H" level while main clock is stable, the reset status is cancelled and program execution resumes from the address in the reset vector table.

Figure 1.11 shows the example reset circuit. Figure 1.12 shows the reset sequence.

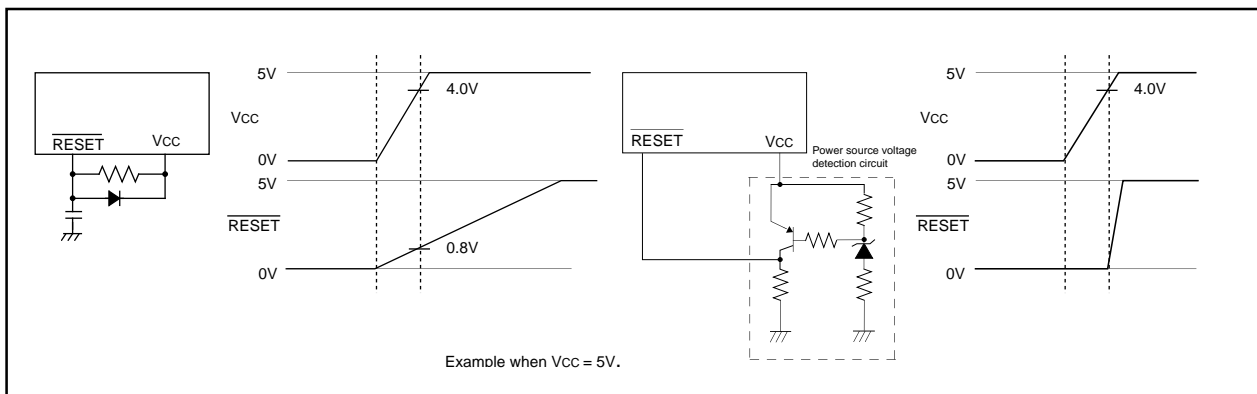


Figure 1.11. Example reset circuit

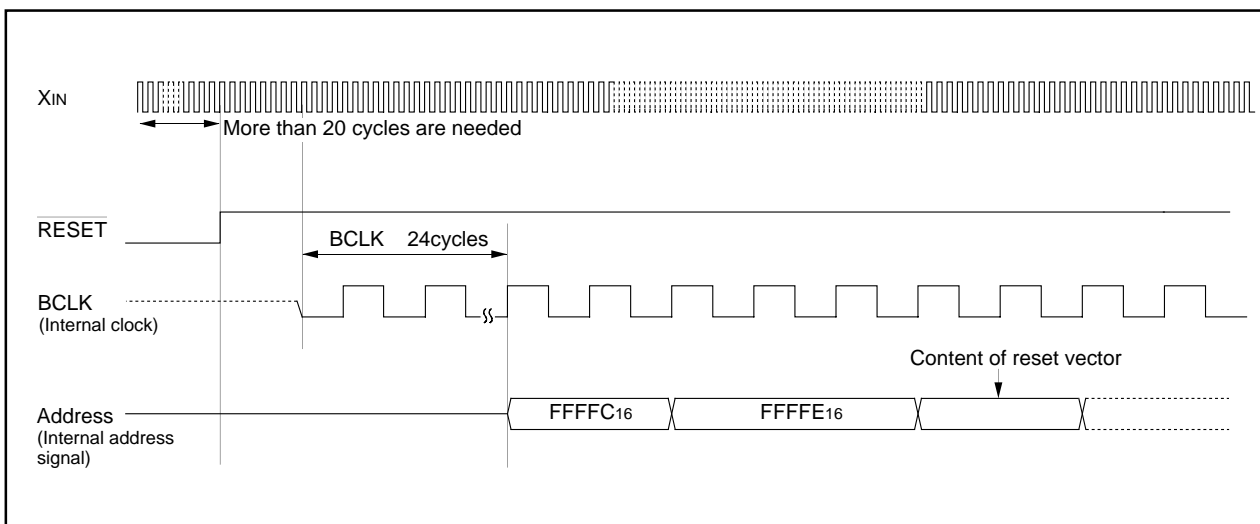


Figure 1.12. Reset sequence

Reset

(1) Processor mode register 0	(0004 ₁₆)...		(33) Timer B0 mode register	(039B ₁₆)...	
(2) Processor mode register 1	(0005 ₁₆)...		(34) Timer B1 mode register	(039C ₁₆)...	
(3) System clock control register 0	(0006 ₁₆)...		(35) UART0 transmit/receive mode register	(03A0 ₁₆)...	
(4) System clock control register 1	(0007 ₁₆)...		(36) UART0 transmit/receive control register 0	(03A4 ₁₆)...	
(5) Address match interrupt enable register	(0009 ₁₆)...		(37) UART0 transmit/receive control register 1	(03A5 ₁₆)...	
(6) Protect register	(000A ₁₆)...		(38) UART1 transmit/receive mode register	(03A8 ₁₆)...	
(7) Watchdog timer control register	(000F ₁₆)...		(39) UART1 transmit/receive control register 0	(03AC ₁₆)...	
(8) Address match interrupt register 0	(0010 ₁₆)...		(40) UART1 transmit/receive control register 1	(03AD ₁₆)...	
	(0011 ₁₆)...		(41) UART transmit/receive control register 2	(03B0 ₁₆)...	
	(0012 ₁₆)...		(42) Flash memory control register 0 (Note)	(03B4 ₁₆)...	
(9) Address match interrupt register 1	(0014 ₁₆)...		(43) Flash memory control register 1 (Note)	(03B5 ₁₆)...	
	(0015 ₁₆)...		(44) Flash command register	(03B6 ₁₆)...	
	(0016 ₁₆)...		(45) A-D control register 2	(03D4 ₁₆)...	
(10) Key input interrupt control register	(004D ₁₆)...		(46) A-D control register 0	(03D6 ₁₆)...	
(11) A-D conversion interrupt control register	(004E ₁₆)...		(47) A-D control register 1	(03D7 ₁₆)...	
(12) UART0 transmit interrupt control register	(0051 ₁₆)...		(48) Port P0 direction register	(03E2 ₁₆)...	
(13) UART0 receive interrupt control register	(0052 ₁₆)...		(49) Port P1 direction register	(03E3 ₁₆)...	
(14) UART1 transmit interrupt control register	(0053 ₁₆)...		(50) Port P2 direction register	(03E6 ₁₆)...	
(15) UART1 receive interrupt control register	(0054 ₁₆)...		(51) Port P3 direction register	(03E7 ₁₆)...	
(16) Timer A0 interrupt control register	(0055 ₁₆)...		(52) Port P4 direction register	(03EA ₁₆)...	
(17) Timer X0 interrupt control register	(0056 ₁₆)...		(53) Port P5 direction register	(03EB ₁₆)...	
(18) Timer X1 interrupt control register	(0057 ₁₆)...		(54) Port P6 direction register	(03EE ₁₆)...	
(19) Timer X2 interrupt control register	(0058 ₁₆)...		(55) Port P7 direction register	(03EF ₁₆)...	
(20) Timer B0 interrupt control register	(005A ₁₆)...		(56) Pull-up control register 0	(03FC ₁₆)...	
(21) Timer B1 interrupt control register	(005B ₁₆)...		(57) Pull-up control register 1	(03FD ₁₆)...	
(22) INT0 interrupt control register	(005D ₁₆)...		(58) Port P1 drive capacity control register	(03FE ₁₆)...	
(23) INT1 interrupt control register	(005E ₁₆)...		(59) Data registers (R0/R1/R2/R3)		
(24) Count start flag	(0380 ₁₆)...		(60) Address registers (A0/A1)		
(25) Clock prescaler reset flag	(0381 ₁₆)...		(61) Frame base register (FB)		
(26) One-shot start flag	(0382 ₁₆)...		(62) Interrupt table register (INTB)		
(27) Trigger select flag	(0383 ₁₆)...		(63) User stack pointer (USP)		
(28) Up-down flag	(0384 ₁₆)...		(64) Interrupt stack pointer (ISP)		
(29) Timer A0 mode register	(0396 ₁₆)...		(65) Static base register (SB)		
(30) Timer X0 mode register	(0397 ₁₆)...		(66) Flag register (FLG)		
(31) Timer X1 mode register	(0398 ₁₆)...				
(32) Timer X2 mode register	(0399 ₁₆)...				

x : Nothing is mapped to this bit
? : Undefined

The content of other registers and RAM is undefined when the microcomputer is reset. The initial values must therefore be set.

Note: This register is only exist in flash memory version.

Figure 1.13. Device's internal status after a reset is cleared

Software Reset

Software Reset

Writing "1" to bit 3 of the processor mode register 0 (address 0004₁₆) applies a (software) reset to the microcomputer. A software reset has almost the same effect as a hardware reset. The contents of internal RAM are preserved.

Figure 1.14 shows the processor mode register 0 and 1.

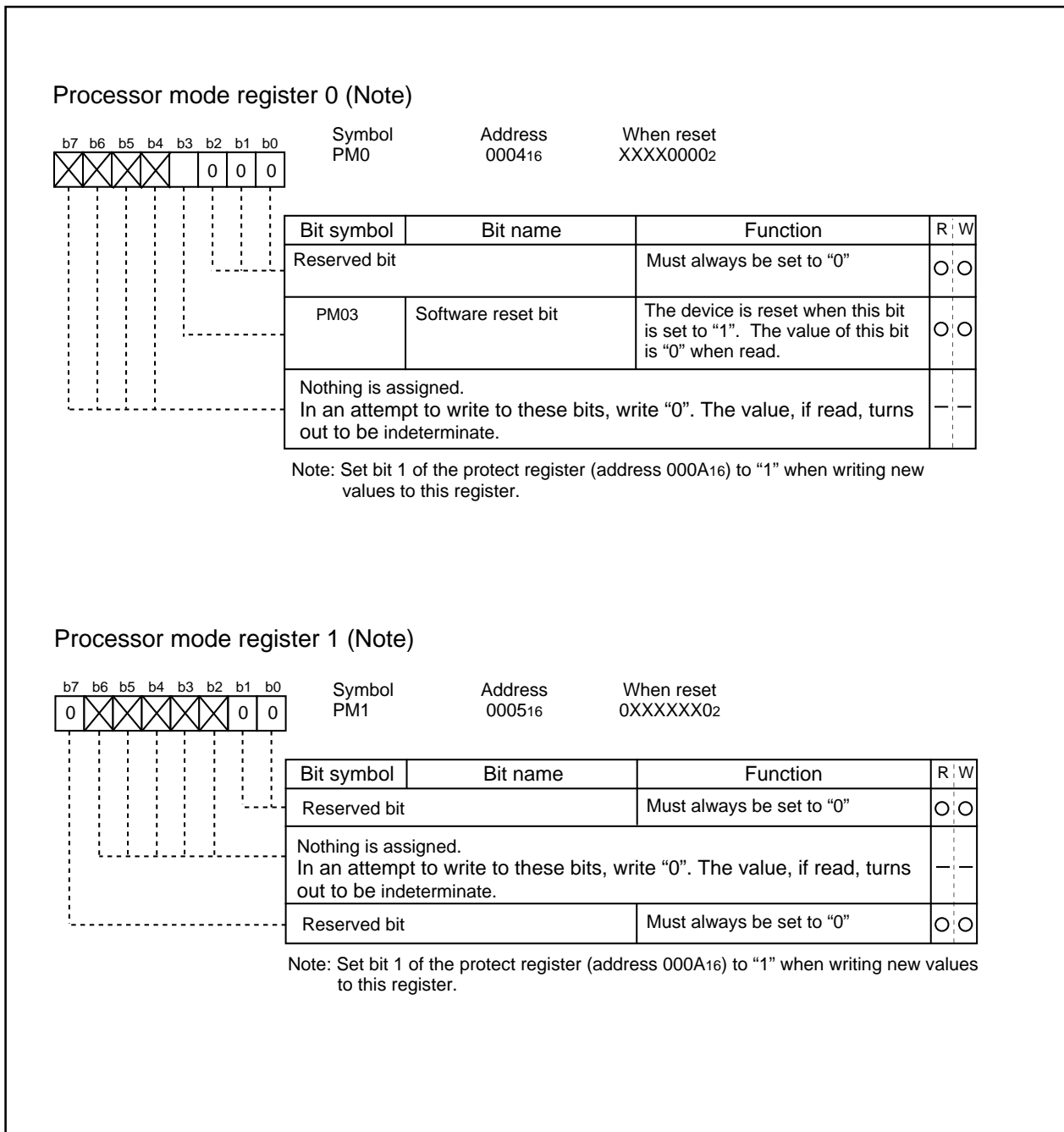


Figure 1.14. Processor mode register 0 and 1.

Clock Generating Circuit

Clock Generating Circuit

The clock generating circuit contains two oscillator circuits that supply the operating clock sources to the CPU and internal peripheral units.

Table 1.2. Main clock and sub-clock generating circuits

	Main clock generating circuit	Sub clock generating circuit
Use of clock	<ul style="list-style-type: none"> • CPU's operating clock source • Internal peripheral units' operating clock source 	<ul style="list-style-type: none"> • CPU's operating clock source • Timer A/B/X's count clock source
Usable oscillator	Ceramic or crystal oscillator	Crystal oscillator
Pins to connect oscillator	XIN, XOUT	XCIN, XCOUT
Oscillation stop/restart function	Available	Available
Oscillator status immediately after reset	Oscillating	Stopped
Other	Externally derived clock can be input	

Example of oscillator circuit

Figure 1.15 shows some examples of the main clock circuit, one using an oscillator connected to the circuit, and the other one using an externally derived clock for input. Figure 1.16 shows some examples of sub-clock circuits, one using an oscillator connected to the circuit, and the other one using an externally derived clock for input. Circuit constants in Figures 15 and 16 vary with each oscillator used. Use the values recommended by the manufacturer of your oscillator.

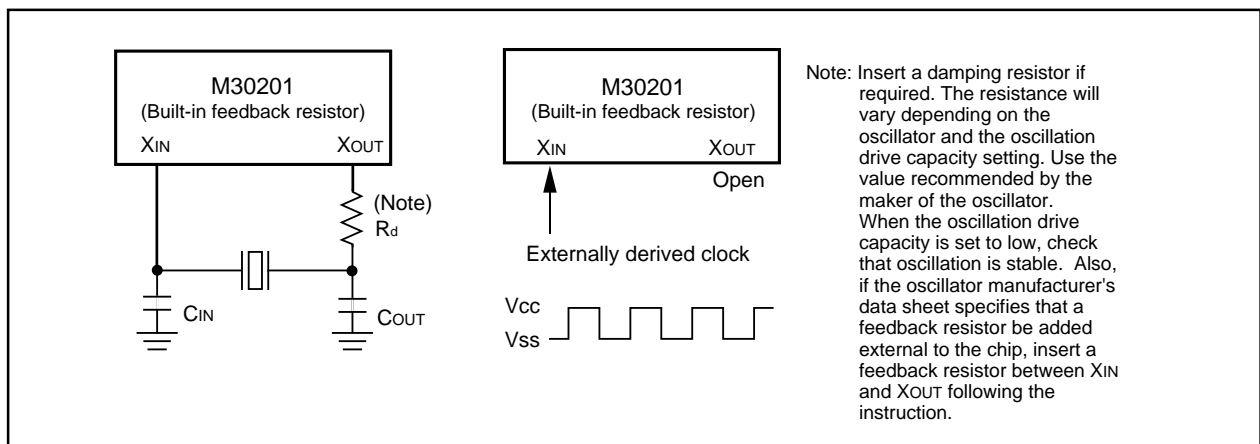


Figure 1.15. Examples of main clock

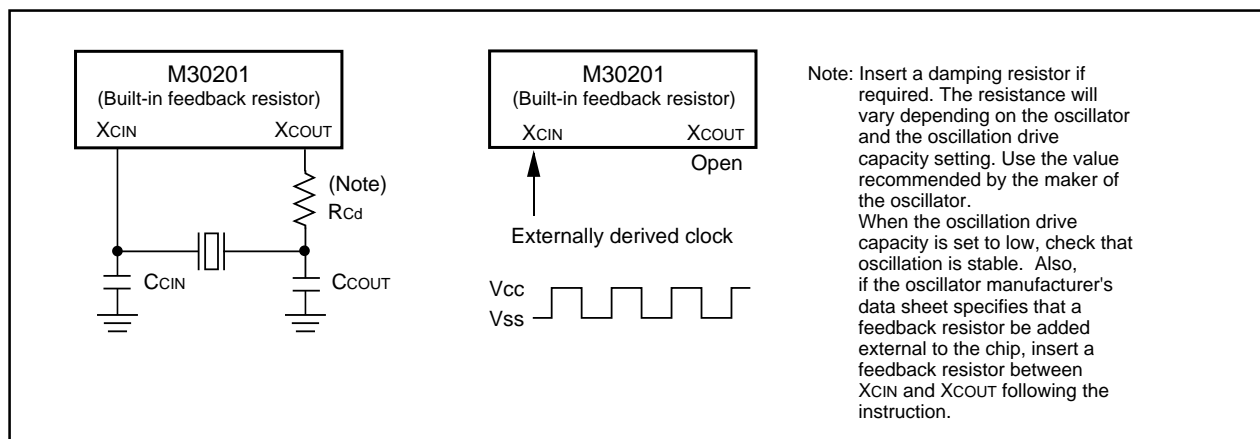


Figure 1.16. Examples of sub-clock

Clock Generating Circuit

Clock Control

Figure 1.17 shows the block diagram of the clock generating circuit.

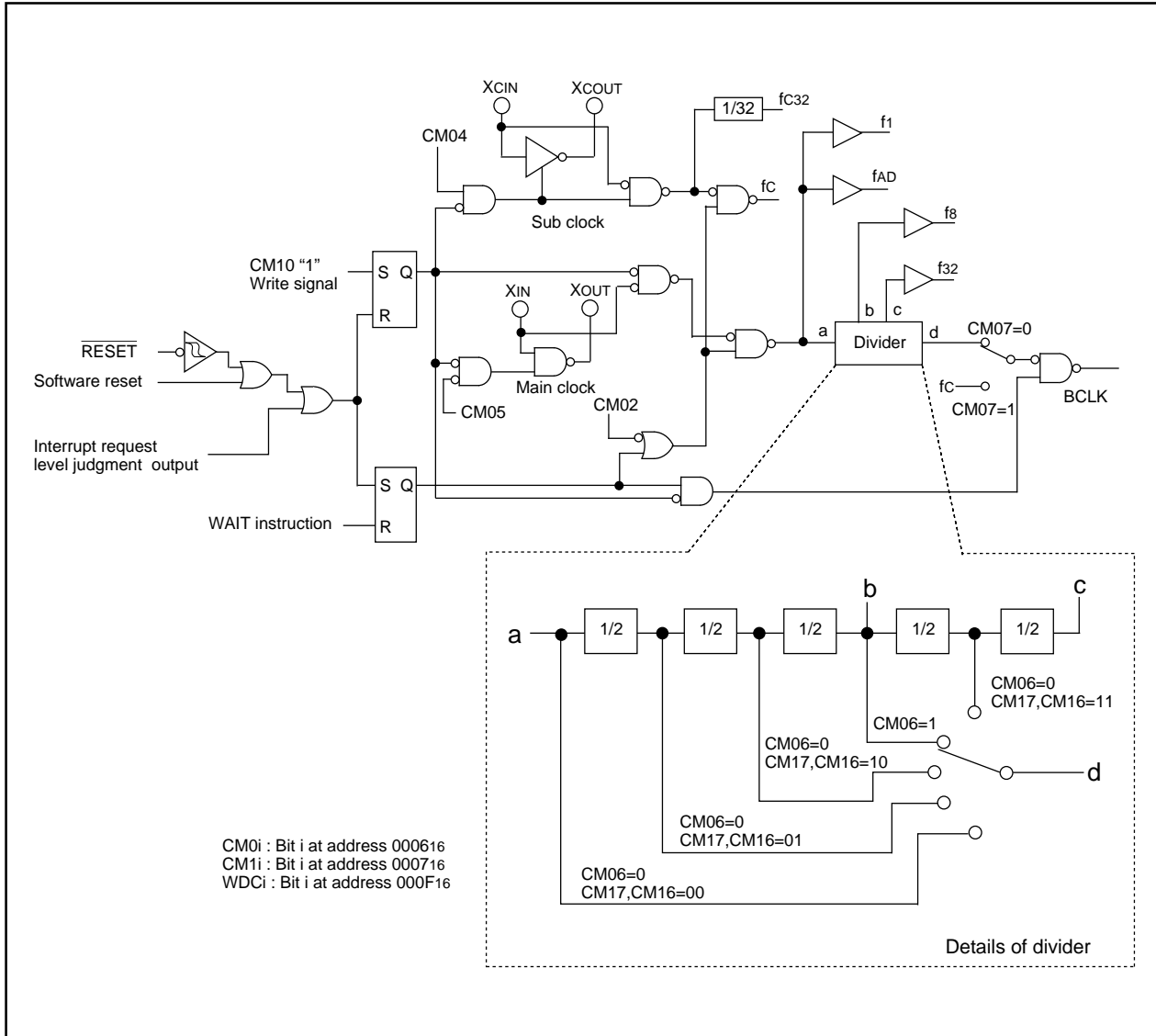


Figure 1.17. Clock generating circuit

Clock Generating Circuit

The following paragraphs describes the clocks generated by the clock generating circuit.

(1) Main clock

The main clock is generated by the main clock oscillation circuit. After a reset, the clock is divided by 8 to BCLK. The clock can be stopped using the main clock stop bit (bit 5 at address 0006₁₆). Stopping the clock, after switching the operating clock source of CPU to the sub-clock, reduces the power dissipation. After the oscillation of the main clock oscillation circuit has stabilized, the drive capacity of the main clock oscillation circuit can be reduced using the XIN-XOUT drive capacity select bit (bit 5 at address 0007₁₆). Reducing the drive capacity of the main clock oscillation circuit reduces the power dissipation. This bit changes to "1" when shifting from high-speed/medium-speed mode to stop mode and at a reset. When shifting from low-speed/low power dissipation mode to stop mode, the value before stop mode is retained.

(2) Sub-clock

The sub-clock is generated by the sub-clock oscillation circuit. No sub-clock is generated after a reset. After oscillation is started using the port Xc select bit (bit 4 at address 0006₁₆), the sub-clock can be selected as BCLK by using the system clock select bit (bit 7 at address 0006₁₆). However, be sure that the sub-clock oscillation has fully stabilized before switching.

After the oscillation of the sub-clock oscillation circuit has stabilized, the drive capacity of the sub-clock oscillation circuit can be reduced using the XCIN-XCOUT drive capacity select bit (bit 3 at address 0006₁₆). Reducing the drive capacity of the sub-clock oscillation circuit reduces the power dissipation. This bit changes to "1" when shifting to stop mode and at a reset.

(3) BCLK

The BCLK is the clock that drives the CPU, and is fc or the clock is derived by dividing the main clock by 1, 2, 4, 8, or 16. The BCLK is derived by dividing the main clock by 8 after a reset.

The main clock division select bit 0(bit 6 at address 0006₁₆) changes to "1" when shifting from high-speed/medium-speed to stop mode and at reset. When shifting from low-speed/low power dissipation mode to stop mode, the value before stop mode is retained.

(4) Peripheral function clock (f₁, f₈, f₃₂, f_{AD})

The clock for the peripheral devices is derived from the main clock or by dividing it by 8 or 32. The peripheral function clock is stopped by stopping the main clock or by setting the WAIT peripheral function clock stop bit (bit 2 at 0006₁₆) to "1" and then executing a WAIT instruction.

(5) fc₃₂

This clock is derived by dividing the sub-clock by 32. It is used for the timer A, timer B and timer X counts.

(6) fc

This clock has the same frequency as the sub-clock. It is used for BCLK and for the watchdog timer.

Clock Generating Circuit

Figure 1.18 shows the system clock control registers 0 and 1.

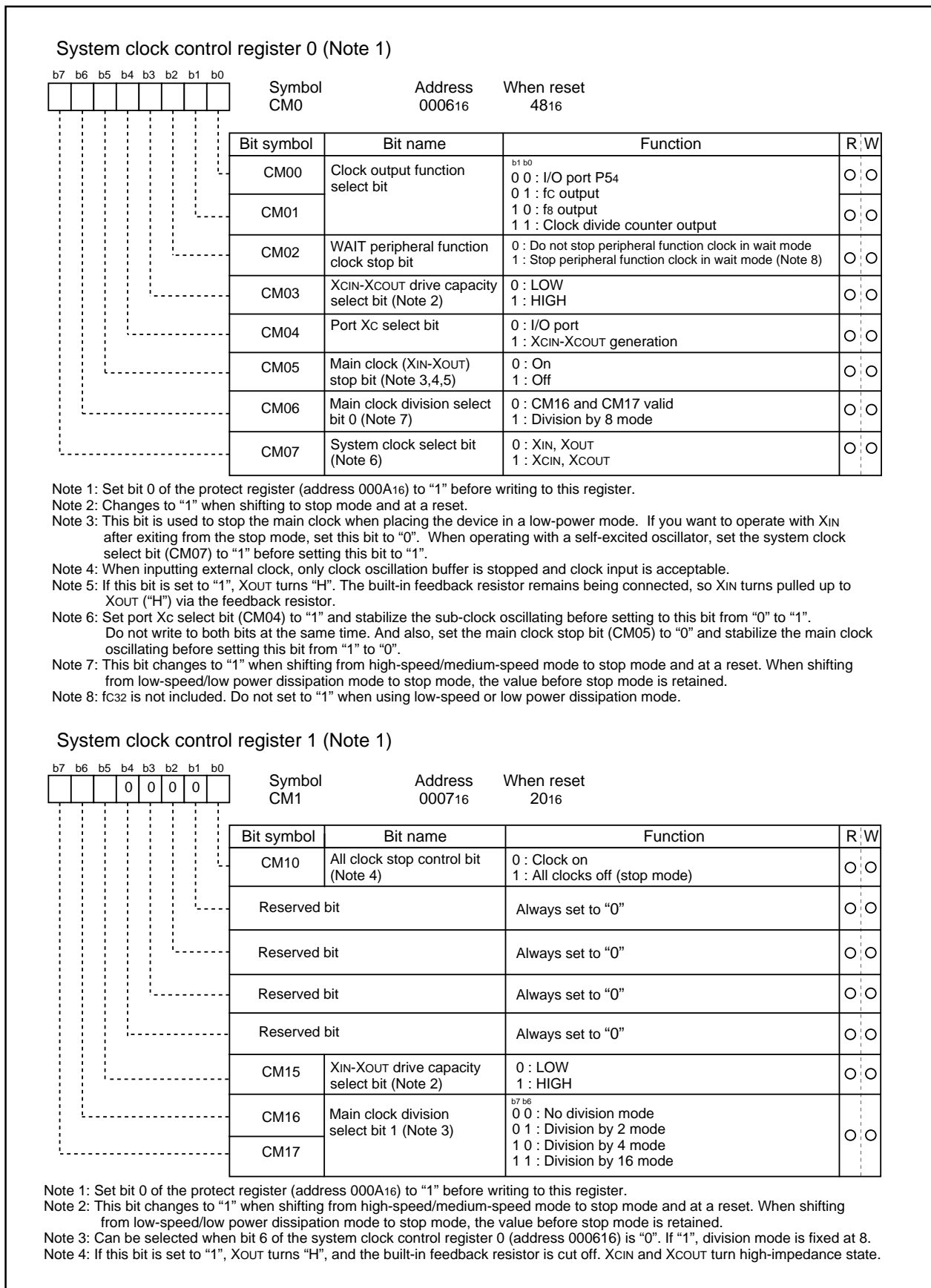


Figure 1.18. Clock control registers 0 and 1

Clock Generating Circuit

Clock Output

The clock output function select bit allows you to choose the clock from f8, fc, or a divide-by-n clock that is output from the P54/CKOUT pin. The clock divide counter is an 8-bit counter whose count source is f32, and its divide ratio can be set in the range of 0016 to FF16. Figure 1.19 shows a block diagram of clock output.

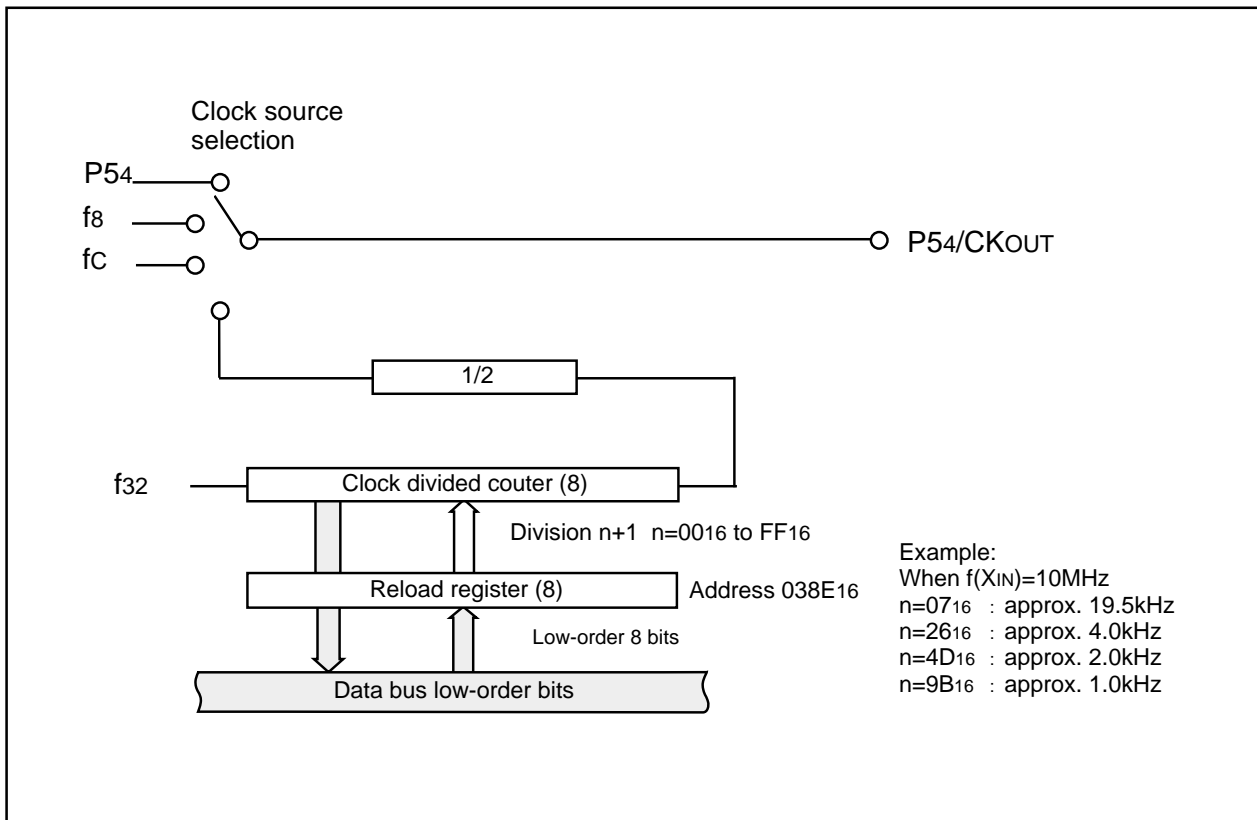


Figure 1.19. Block diagram of clock output

Stop Mode, Wait Mode

Stop Mode

Writing "1" to the all-clock stop control bit (bit 0 at address 0007₁₆) stops all oscillation and the microcomputer enters stop mode. In stop mode, the content of the internal RAM is retained provided that VCC remains above 2V.

Because the oscillation of BCLK, f₁ to f₃₂, f_c, f_{c32}, and f_{AD} stops in stop mode, peripheral functions such as the A-D converter and watchdog timer do not function. However, timer A, timer B and timer X operate provided that the event counter mode is set to an external pulse, and UART0 functions provided an external clock is selected. Table 1.3 shows the status of the ports in stop mode.

Stop mode is cancelled by a hardware reset or an interrupt. If an interrupt is to be used to cancel stop mode, that interrupt must first have been enabled. If returning by an interrupt, that interrupt routine is executed.

When shifting from high-speed/medium-speed mode to stop mode and at a reset, the main clock division select bit 0 (bit 6 at address 0006₁₆) is set to "1". When shifting from low-speed/low power dissipation mode to stop mode, the value before stop mode is retained.

Table 1.3. Port status during stop mode

Pin		States
Port		Retains status before stop mode
CLKOUT	When f _c selected	"H"
	When f ₈ , clock divided counter output selected	Retains status before stop mode

Wait Mode

When a WAIT instruction is executed, BCLK stops and the microcomputer enters the wait mode. In this mode, oscillation continues but BCLK and watchdog timer stop. Writing "1" to the WAIT peripheral function clock stop bit and executing a WAIT instruction stops the clock being supplied to the internal peripheral functions, allowing power dissipation to be reduced. However, peripheral function clock f_{c32} does not stop so that the peripherals using f_{c32} do not contribute to the power saving. When the MCU running in low-speed or low power dissipation mode, do not enter WAIT mode with this bit set to "1". Table 1.4 shows the status of the ports in wait mode.

Wait mode is cancelled by a hardware reset or interrupt. If an interrupt is used to cancel wait mode, the microcomputer restarts from the interrupt routine using as BCLK, the clock that had been selected when the WAIT instruction was executed.

Table 1.4. Port status during wait mode

Pin		States
Port		Retains status before wait mode
CLKOUT	When f _c selected	Does not stop
	When f ₈ , clock divided counter output selected	Does not stop when the WAIT peripheral function clock stop bit is "0". When the WAIT peripheral function clock stop bit is "1", the status immediately prior to entering wait mode is maintained.

Status Transition of BCLK

Status Transition of BCLK

Power dissipation can be reduced and low-voltage operation achieved by changing the count source for BCLK. Table 1.5 shows the operating modes corresponding to the settings of system clock control registers 0 and 1.

When reset, the device starts in division by 8 mode. The main clock division select bit 0(bit 6 at address 000616) changes to "1" when shifting from high-speed/medium-speed to stop mode and at a reset. When shifting from low-speed/low power dissipation mode to stop mode, the value before stop mode is retained. The following shows the operational modes of BCLK.

(1) Division by 2 mode

The main clock is divided by 2 to obtain the BCLK.

(2) Division by 4 mode

The main clock is divided by 4 to obtain the BCLK.

(3) Division by 8 mode

The main clock is divided by 8 to obtain the BCLK. When reset, the device starts operating from this mode. Before the user can go from this mode to no division mode, division by 2 mode, or division by 4 mode, the main clock must be oscillating stably. When going to low-speed or lower power consumption mode, make sure the sub-clock is oscillating stably.

(4) Division by 16 mode

The main clock is divided by 16 to obtain the BCLK.

(5) No-division mode

The main clock is divided by 1 to obtain the BCLK.

(6) Low-speed mode

fc is used as BCLK. Note that oscillation of both the main and sub-clocks must have stabilized before transferring from this mode to another or vice versa. At least 2 to 3 seconds are required after the sub-clock starts. Therefore, the program must be written to wait until this clock has stabilized immediately after powering up and after stop mode is cancelled.

(7) Low power dissipation mode

fc is the BCLK and the main clock is stopped.

Note : Before the count source for BCLK can be changed from XIN to XCIN or vice versa, the clock to which the count source is going to be switched must be oscillating stably. Allow a wait time in software for the oscillation to stabilize before switching over the clock.

Table 1.5. Operating modes dictated by settings of system clock control registers 0 and 1

CM17	CM16	CM07	CM06	CM05	CM04	Operating mode of BCLK
0	1	0	0	0	Invalid	Division by 2 mode
1	0	0	0	0	Invalid	Division by 4 mode
Invalid	Invalid	0	1	0	Invalid	Division by 8 mode
1	1	0	0	0	Invalid	Division by 16 mode
0	0	0	0	0	Invalid	No-division mode
Invalid	Invalid	1	Invalid	0	1	Low-speed mode
Invalid	Invalid	1	Invalid	1	1	Low power dissipation mode

Power Saving

Power Saving

There are three power save modes.

(1) Normal operating mode

- **High-speed mode**

In this mode, one main clock cycle forms BCLK. The CPU operates on the BCLK. The peripheral functions operate on the clocks specified for each respective function.

- **Medium-speed mode**

In this mode, the main clock is divided into 2, 4, 8, or 16 to form BCLK. The CPU operates on the BCLK. The peripheral functions operated on the clocks specified for each respective function.

- **Low-speed mode**

In this mode, fc forms BCLK. The CPU operates on the fc clock. fc is the clock supplied by the subclock. The peripheral functions operate on the clocks specified for each respective function.

- **Low power-dissipation mode**

This mode is selected when the main clock is stopped from low-speed mode. The CPU operates on the fc clock. fc is the clock supplied by the subclock. Only the peripheral functions for which the subclock was selected as the count source continue to run.

(2) Wait mode

CPU operation is halted in this mode. The oscillator continues to run.

(3) Stop mode

All oscillators stop in this mode. The CPU and internal peripheral functions all stop. Of all 3 power saving modes, power savings are greatest in this mode.

Figure 1.20 shows the transition between each of the three modes, (1), (2), and (3).

Power Saving

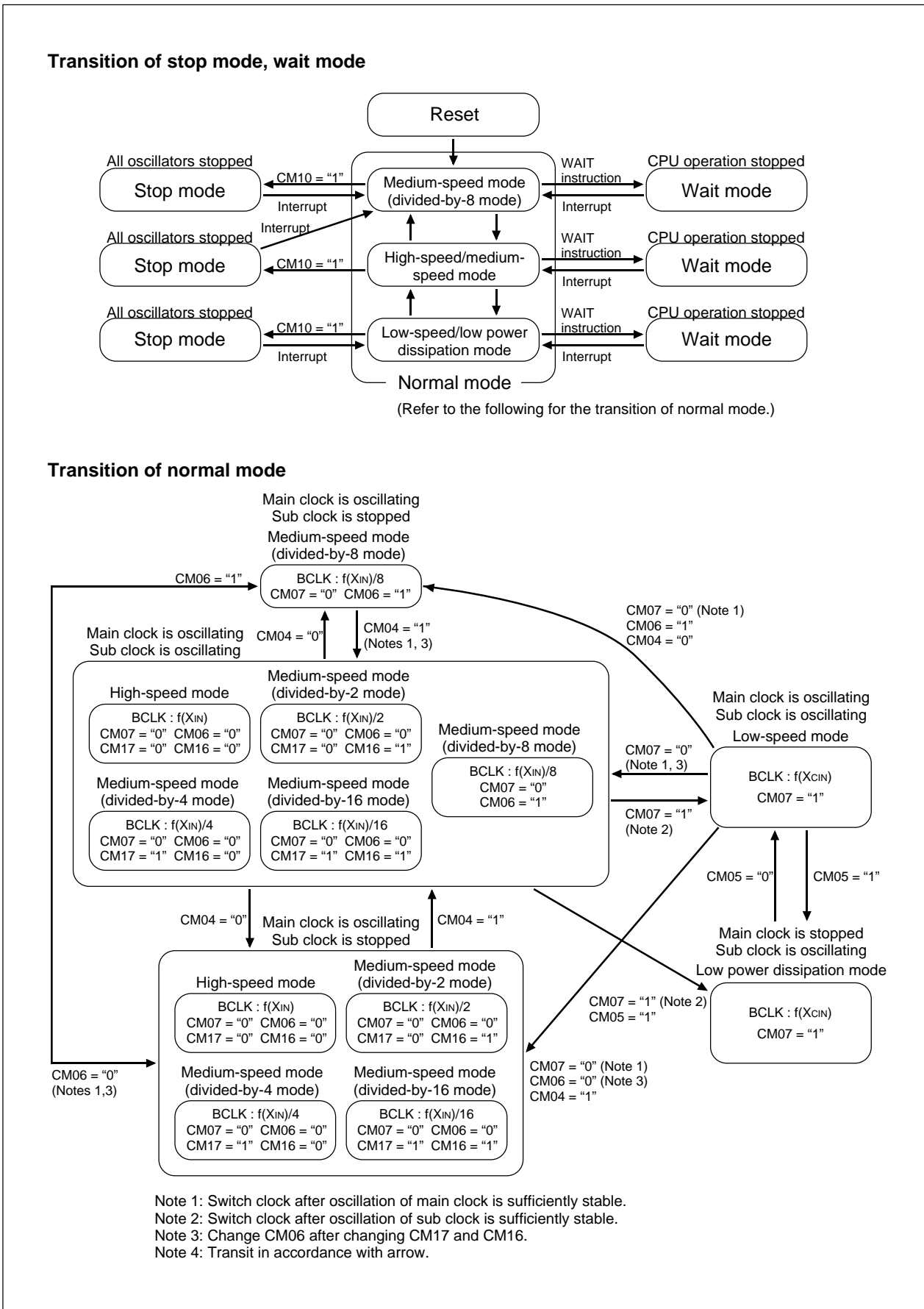


Figure 1.20. Clock transition

Protection

Protection

The protection function is provided so that the values in important registers cannot be changed in the event that the program runs out of control. Figure 1.21 shows the protect register. The values in the processor mode register 0 (address 0004₁₆), processor mode register 1 (address 0005₁₆), system clock control register 0 (address 0006₁₆), system clock control register 1 (address 0007₁₆) and port P4 direction register (address 03EA₁₆) can only be changed when the respective bit in the protect register is set to "1". Therefore, important outputs can be allocated to port P4.

If, after "1" (write-enabled) has been written to the port P4 direction register write-enable bit (bit 2 at address 000A₁₆), a value is written to any address, the bit automatically reverts to "0" (write-inhibited). However, the system clock control registers 0 and 1 write-enable bit (bit 0 at 000A₁₆) and processor mode register 0 and 1 write-enable bit (bit 1 at 000A₁₆) do not automatically return to "0" after a value has been written to an address. The program must therefore be written to return these bits to "0".

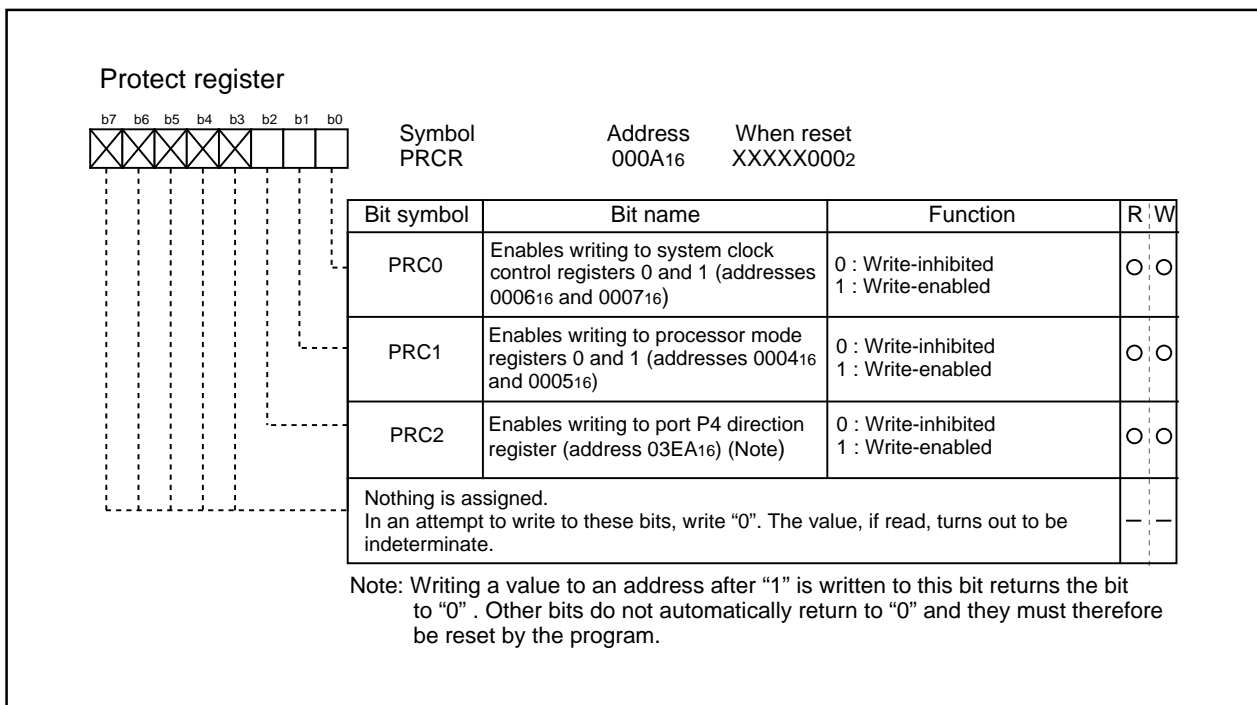


Figure 1.21. Protect register

Interrupts

Overview of Interrupt

Type of Interrupts

Figure 1.22 lists the types of interrupts.

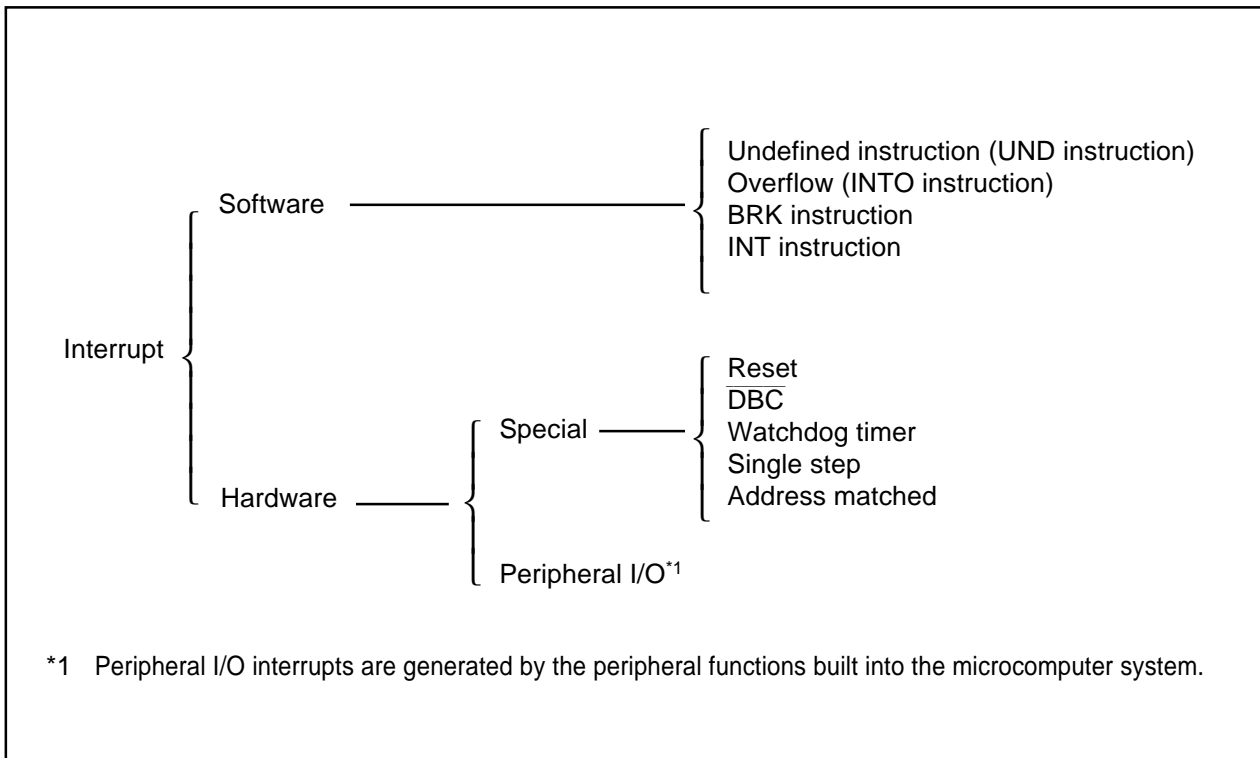


Figure 1.22. Classification of interrupts

- Maskable interrupt : An interrupt which can be enabled (disabled) by the interrupt enable flag (I flag) or whose interrupt priority can be changed by priority level.
- Non-maskable interrupt : An interrupt which cannot be enabled (disabled) by the interrupt enable flag (I flag) or whose interrupt priority cannot be changed by priority level.

Interrupts

Software Interrupts

A software interrupt occurs when executing certain instructions. Software interrupts are non-maskable interrupts.

- **Undefined instruction interrupt**

An undefined instruction interrupt occurs when executing the UND instruction.

- **Overflow interrupt**

An overflow interrupt occurs when executing the INTO instruction with the overflow flag (O flag) set to "1".

The following are instructions whose O flag changes by arithmetic:

ABS, ADC, ADCF, ADD, CMP, DIV, DIVU, DIVX, NEG, RMPA, SBB, SHA, SUB

- **BRK interrupt**

A BRK interrupt occurs when executing the BRK instruction.

- **INT interrupt**

An INT interrupt occurs when assigning one of software interrupt numbers 0 through 63 and executing the INT instruction. Software interrupt numbers 0 through 31 are assigned to peripheral I/O interrupts, so executing the INT instruction allows executing the same interrupt routine that a peripheral I/O interrupt does.

The stack pointer (SP) used for the INT interrupt is dependent on which software interrupt number is involved.

So far as software interrupt numbers 0 through 31 are concerned, the microcomputer saves the stack pointer assignment flag (U flag) when it accepts an interrupt request. If change the U flag to "0" and select the interrupt stack pointer (ISP), and then execute an interrupt sequence. When returning from the interrupt routine, the U flag is returned to the state it was before the acceptance of interrupt request. So far as software numbers 32 through 63 are concerned, the stack pointer does not make a shift.

Interrupts

Hardware Interrupts

Hardware interrupts are classified into two types — special interrupts and peripheral I/O interrupts.

(1) Special interrupts

Special interrupts are non-maskable interrupts.

- **Reset**

Reset occurs if an “L” is input to the RESET pin.

- **DBC interrupt**

This interrupt is exclusively for the debugger, do not use it in other circumstances.

- **Watchdog timer interrupt**

Generated by the watchdog timer.

- **Single-step interrupt**

This interrupt is exclusively for the debugger, do not use it in other circumstances. With the debug flag (D flag) set to “1”, a single-step interrupt occurs after one instruction is executed.

- **Address match interrupt**

An address match interrupt occurs immediately before the instruction held in the address indicated by the address match interrupt register is executed with the address match interrupt enable bit set to “1”. If an address other than the first address of the instruction in the address match interrupt register is set, no address match interrupt occurs.

(2) Peripheral I/O interrupts

A peripheral I/O interrupt is generated by one of built-in peripheral functions. The interrupt vector table is the same as the one for software interrupt numbers 0 through 31 the INT instruction uses. Peripheral I/O interrupts are maskable interrupts.

- **Key-input interrupt**

A key-input interrupt occurs if an “L” is input to the \overline{KI} pin.

- **A-D conversion interrupt**

This is an interrupt that the A-D converter generates.

- **UART0 and UART1 transmission interrupt**

These are interrupts that the serial I/O transmission generates.

- **UART0 and UART1 reception interrupt**

These are interrupts that the serial I/O reception generates.

- **Timer A0 interrupt**

This is an interrupts that timer A0 generates.

- **Timer B0 and timer B2 interrupt**

These are interrupts that timer B generates.

- **Timer X0 to timer X2 interrupt**

These are interrupts that timer X generates.

- **$\overline{INT0}$ and $\overline{INT1}$ interrupt**

An \overline{INT} interrupt occurs if either a rising edge or a falling edge is input to the \overline{INT} pin.

Interrupts

Interrupts and Interrupt Vector Tables

If an interrupt request is accepted, a program branches to the interrupt routine set in the interrupt vector table. Set the first address of the interrupt routine in each vector table. Figure 1.23 shows format for specifying interrupt vector addresses.

Two types of interrupt vector tables are available — fixed vector table in which addresses are fixed and variable vector table in which addresses can be varied by the setting.

	MSB	LSB
Vector address + 0	Low address	
Vector address + 1	Mid address	
Vector address + 2	0 0 0 0	High address
Vector address + 3	0 0 0 0	0 0 0 0

Figure 1.23. Format for specifying interrupt vector addresses

• Fixed vector tables

The fixed vector table is a table in which addresses are fixed. The vector tables are located in an area extending from FFFDC₁₆ to FFFFF₁₆. One vector table comprises four bytes. Set the first address of interrupt routine in each vector table. Table 1.6 shows the interrupts assigned to the fixed vector tables and addresses of vector tables.

Table 1.6. Interrupt and fixed vector address

Interrupt source	Vector table addresses Address (L) to address (H)	Remarks
Undefined instruction	FFFD _{C16} to FFFD _{F16}	Interrupt on UND instruction
Overflow	FFFE ₀₁₆ to FFFE ₃₁₆	Interrupt on INTO instruction
BRK instruction	FFFE ₄₁₆ to FFFE ₇₁₆	If the vector is filled with FF ₁₆ , program execution starts from the address shown by the vector in the variable vector table
Address match	FFFE ₈₁₆ to FFFE _{B16}	There is an address-matching interrupt enable bit
Single step (Note)	FFFE _{C16} to FFFE _{F16}	Do not use
Watchdog timer	FFFF ₀₁₆ to FFFF ₃₁₆	
DBC (Note)	FFFF ₄₁₆ to FFFF ₇₁₆	Do not use
-	FFFF ₈₁₆ to FFFF _{B16}	-
Reset	FFFF _{C16} to FFFF _{F16}	

Note: Interrupts used for debugging purposes only.

Interrupts

• Variable vector tables

The addresses in the variable vector table can be modified, according to the user's settings. Indicate the first address using the interrupt table register (INTB). The 256-byte area subsequent to the address the INTB indicates becomes the area for the variable vector tables. One vector table comprises four bytes. Set the first address of the interrupt routine in each vector table. Table 1.7 shows the interrupts assigned to the variable vector tables and addresses of vector tables.

Table 1.7. Interrupt causes (variable interrupt vector addresses)

Software interrupt number	Vector table address Address (L) to address (H)	Interrupt source	Remarks
Software interrupt number 0	+0 to +3 (Note)	BRK instruction	Cannot be masked by I flag
—		—	
Software interrupt number 11	+44 to +47 (Note)	—	
Software interrupt number 12	+48 to +51 (Note)	—	
Software interrupt number 13	+52 to +55 (Note)	Key input interrupt	
Software interrupt number 14	+56 to +59 (Note)	A-D	
—		—	
Software interrupt number 17	+68 to +71 (Note)	UART0 transmit	
Software interrupt number 18	+72 to +75 (Note)	UART0 receive	
Software interrupt number 19	+76 to +79 (Note)	UART1 transmit	
Software interrupt number 20	+80 to +83 (Note)	UART1 receive	
Software interrupt number 21	+84 to +87 (Note)	Timer A0	
Software interrupt number 22	+88 to +91 (Note)	Timer X0	
Software interrupt number 23	+92 to +95 (Note)	Timer X1	
Software interrupt number 24	+96 to +99 (Note)	Timer X2	
Software interrupt number 25	+100 to +103 (Note)	—	
Software interrupt number 26	+104 to +107 (Note)	Timer B0	
Software interrupt number 27	+108 to +111 (Note)	Timer B1	
Software interrupt number 28	+112 to +115 (Note)	—	
Software interrupt number 29	+116 to +119 (Note)	$\overline{\text{INT0}}$	
Software interrupt number 30	+120 to +123 (Note)	$\overline{\text{INT1}}$	
Software interrupt number 31	+124 to +127 (Note)	—	
Software interrupt number 32 to Software interrupt number 63	+128 to +131 (Note) to +252 to +255 (Note)	Software interrupt	Cannot be masked by I flag

Note : Address relative to address in interrupt table register (INTB).

Interrupts

Interrupt Control

Descriptions are given here regarding how to enable or disable maskable interrupts and how to set the priority to be accepted. What is described here does not apply to non-maskable interrupts.

Enable or disable a maskable interrupt using the interrupt enable flag (I flag), interrupt priority level select bit, and processor interrupt priority level (IPL). Whether an interrupt request is present or absent is indicated by the interrupt request bit. The interrupt request bit and the interrupt priority level selection bit are located in the interrupt control register of each interrupt. Also, the interrupt enable flag (I flag) and the IPL are located in the flag register (FLG).

Figure 1.24 shows the interrupt control registers.

Interrupts

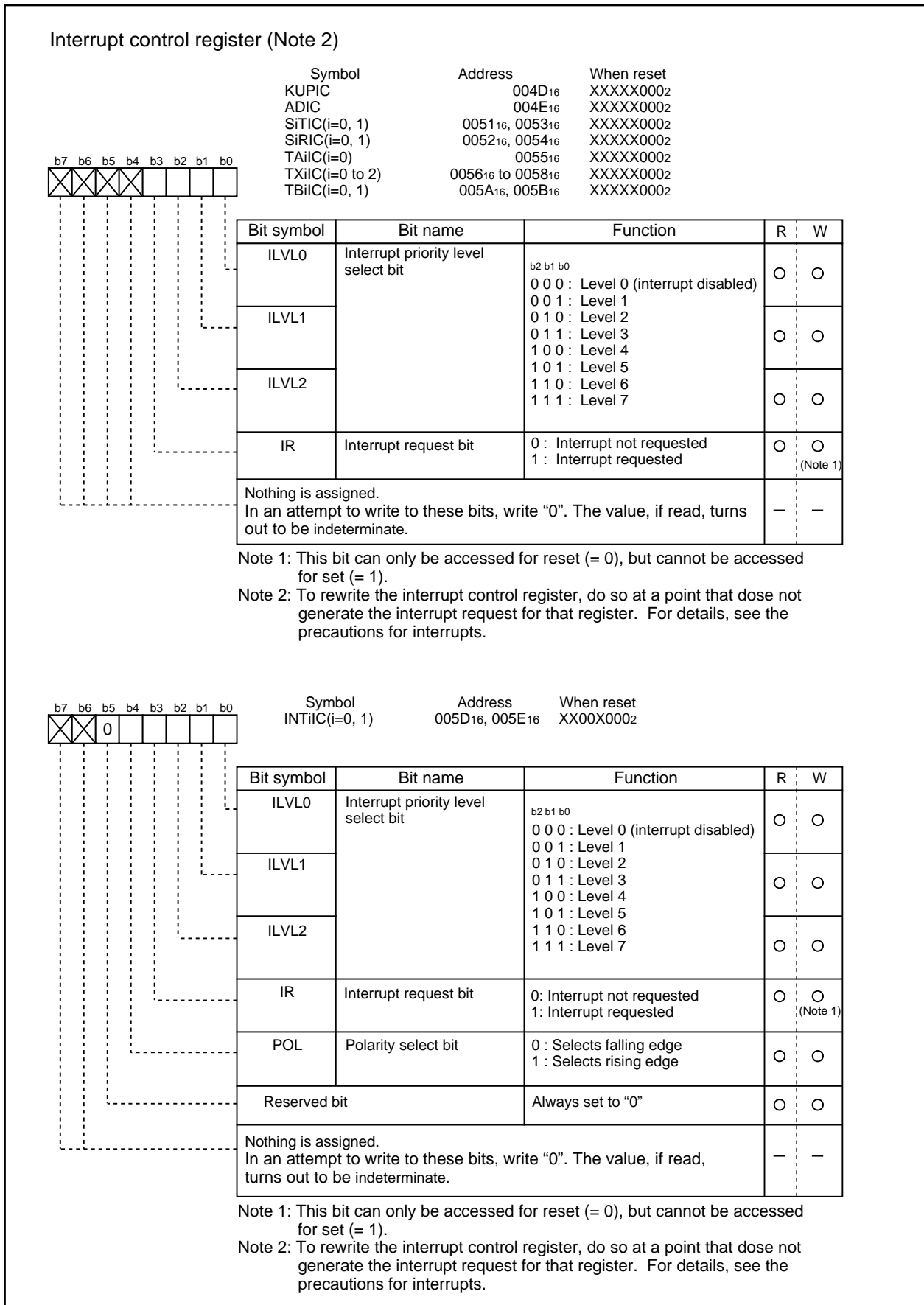


Figure 1.24. Interrupt control register

Interrupts

Interrupt Enable Flag

The interrupt enable flag (I flag) controls the enabling and disabling of maskable interrupts. Setting this flag to "1" enables all maskable interrupts; setting it to "0" disables all maskable interrupts. This flag is set to "0" after reset.

Interrupt Request Bit

The interrupt request bit is set to "1" by hardware when an interrupt is requested. After the interrupt is accepted and jumps to the corresponding interrupt vector, the request bit is set to "0" by hardware. The interrupt request bit can also be set to "0" by software. (Do not set this bit to "1").

Interrupt Priority Level Select Bit and Processor Interrupt Priority Level (IPL)

Set the interrupt priority level using the interrupt priority level select bit, which is one of the component bits of the interrupt control register. When an interrupt request occurs, the interrupt priority level is compared with the IPL. The interrupt is enabled only when the priority level of the interrupt is higher than the IPL. Therefore, setting the interrupt priority level to "0" disables the interrupt.

Table 1.8 shows the settings of interrupt priority levels and Table 1.9 shows the interrupt levels enabled, according to the contents of the IPL.

The following are conditions under which an interrupt is accepted:

- interrupt enable flag (I flag) = 1
- interrupt request bit = 1
- interrupt priority level > IPL

The interrupt enable flag (I flag), the interrupt request bit, the interrupt priority select bit, and the IPL are independent, and they are not affected by one another.

Table 1.8. Settings of interrupt priority levels

Interrupt priority level select bit	Interrupt priority level	Priority order
b2 b1 b0 0 0 0	Level 0 (interrupt disabled)	———
0 0 1	Level 1	Low ↓ High
0 1 0	Level 2	
0 1 1	Level 3	
1 0 0	Level 4	
1 0 1	Level 5	
1 1 0	Level 6	
1 1 1	Level 7	

Table 1.9. Interrupt levels enabled according to the contents of the IPL

IPL	Enabled interrupt priority levels
IPL ₂ IPL ₁ IPL ₀ 0 0 0	Interrupt levels 1 and above are enabled
0 0 1	Interrupt levels 2 and above are enabled
0 1 0	Interrupt levels 3 and above are enabled
0 1 1	Interrupt levels 4 and above are enabled
1 0 0	Interrupt levels 5 and above are enabled
1 0 1	Interrupt levels 6 and above are enabled
1 1 0	Interrupt levels 7 and above are enabled
1 1 1	All maskable interrupts are disabled

Interrupts

Changing the Interrupt Control Register

< Program examples >

The program examples are described as follow:

Example 1:

```
INT_SWITCH1:
  FCLR   I           ; Disable interrupts.
  AND.B  #00h, 0055h ; Clear TA0IC int. priority level and int. request bit.
  NOP                    ; Four NOP instructions are required when using HOLD function.
  NOP
  FSET   I           ; Enable interrupts.
```

Example 2:

```
INT_SWITCH2:
  FCLR   I           ; Disable interrupts.
  AND.B  #00h, 0055h ; Clear TA0IC int. priority level and int. request bit.
  MOV.W  MEM, R0     ; Dummy read.
  FSET   I           ; Enable interrupts.
```

Example 3:

```
INT_SWITCH3:
  PUSHC  FLG         ; Push Flag register onto stack
  FCLR   I           ; Disable interrupts.
  AND.B  #00h, 0055h ; Clear TA0IC int. priority level and int. request bit.
  POPC   FLG         ; Enable interrupts.
```

The reason why two NOP instructions or dummy read are inserted before FSET I in Examples 1 and 2 is to prevent the interrupt enable flag I from being set before the interrupt control register is rewritten due to effects of the instruction queue.

If changing the interrupt control register using an instruction other than the instructions listed here, and if an interrupt occurs associated with this register during execution of the instruction, there can be instances in which the interrupt request bit is not set. To avoid this problem, use one of the instructions given below to change the register.

Following instructions: AND, OR, BCLR or BSET

Interrupts

Interrupt Sequence

An interrupt sequence — what are performed over a period from the instant an interrupt is accepted to the instant the interrupt routine is executed — is described here.

If an interrupt occurs during execution of an instruction, the processor determines its priority when the execution of the instruction is completed, and transfers control to the interrupt sequence from the next cycle. If an interrupt occurs during execution of either the SMOVB, SMOVF, SSTR or RMPA instruction, the processor temporarily suspends the instruction being executed, and transfers control to the interrupt sequence.

In the interrupt sequence, the processor carries out the following in sequence given:

- (1) CPU gets the interrupt information (the interrupt number and interrupt request level) by reading address 0000016. After this, the corresponding interrupt request bit becomes "0".
- (2) Saves the content of the flag register (FLG) as it was immediately before the start of interrupt sequence in the temporary register (Note) within the CPU.
- (3) Sets the interrupt enable flag (I flag), the debug flag (D flag), and the stack pointer select flag (U flag) to "0" (the U flag, however, does not change if the INT instruction, in software interrupt numbers 32 through 63, is executed).
- (4) Saves the content of the temporary register (Note) within the CPU in the stack area.
- (5) Saves the content of the program counter (PC) in the stack area.
- (6) Sets the interrupt priority level of the accepted instruction in the IPL.

After the interrupt sequence is completed, the processor resumes executing instructions from the first address of the interrupt routine.

Note: This register cannot be utilized by the user.

Interrupt Response Time

'Interrupt response time' is the period between the instant an interrupt occurs and the instant the first instruction within the interrupt routine has been executed. This time comprises the period from the occurrence of an interrupt to the completion of the instruction under execution at that moment (a) and the time required for executing the interrupt sequence (b). Figure 1.25 shows the interrupt response time.

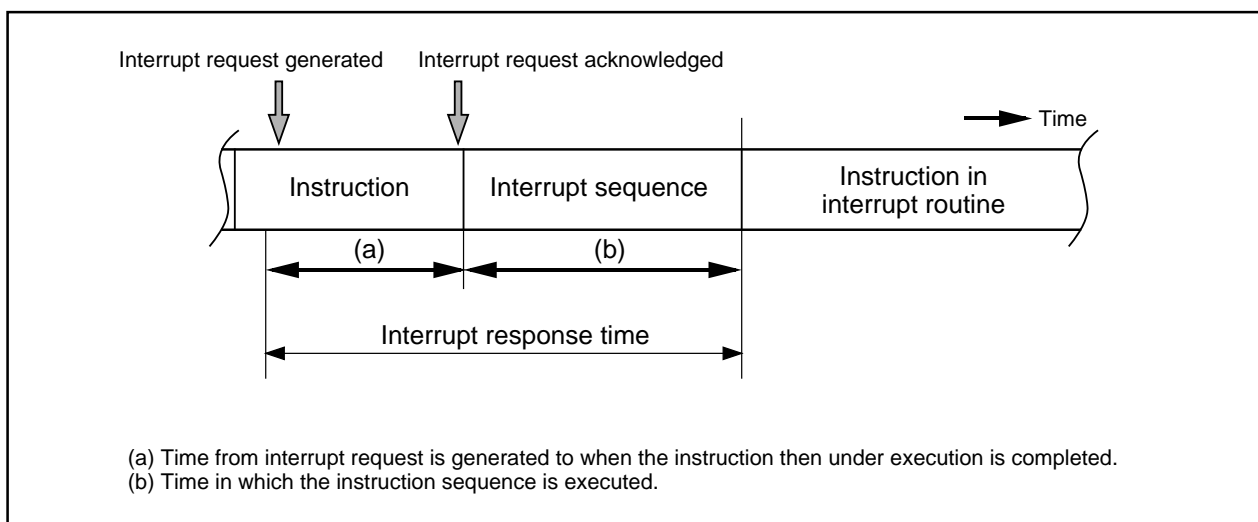


Figure 1.25. Interrupt response time

Interrupts

Time (a) is dependent on the instruction under execution. Thirty cycles is the maximum required for the DIVX instruction (without wait).

Time (b) is as shown in Table 1.10.

Table 1.10. Time required for executing the interrupt sequence

Interrupt vector address	Stack pointer (SP) value	16-bit bus, without wait	8-bit bus, without wait
Even	Even	18 cycles (Note 1)	20 cycles (Note 1)
Even	Odd	19 cycles (Note 1)	20 cycles (Note 1)
Odd (Note 2)	Even	19 cycles (Note 1)	20 cycles (Note 1)
Odd (Note 2)	Odd	20 cycles (Note 1)	20 cycles (Note 1)

Note 1: Add 2 cycles in the case of a \overline{DBC} interrupt; add 1 cycle in the case either of an address match interrupt or of a single-step interrupt.

Note 2: Locate an interrupt vector address in an even address, if possible.

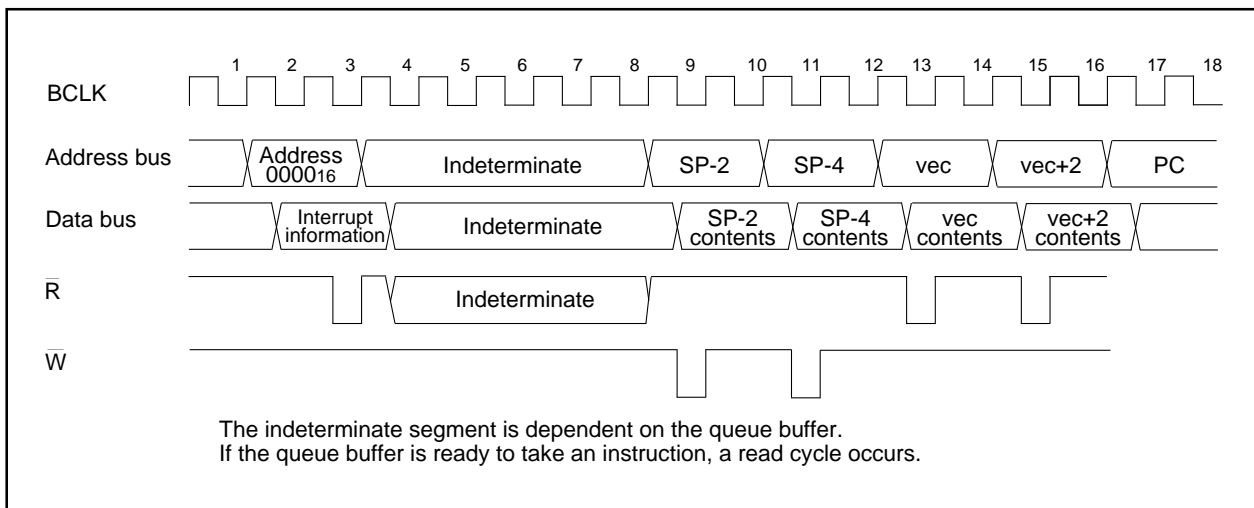


Figure 1.26. Time required for executing the interrupt sequence

Variation of IPL when Interrupt Request is Accepted

If an interrupt request is accepted, the interrupt priority level of the accepted interrupt is set in the IPL.

If an interrupt request, that does not have an interrupt priority level, is accepted, one of the values shown in Table 1.11 is set in the IPL.

Table 1.11. Relationship between interrupts without interrupt priority levels and IPL

Interrupt sources without priority levels	Value set in the IPL
Watchdog timer	7
Reset	0
Other	Not changed

Interrupts

Saving Registers

In the interrupt sequence, only the contents of the flag register (FLG) and that of the program counter (PC) are saved in the stack area.

First, the processor saves the 4 high-order bits of the program counter, and 4 high-order bits and 8 low-order bits of the FLG register, 16 bits in total, in the stack area, then saves 16 low-order bits of the program counter. Figure 1.27 shows the state of the stack as it was before the acceptance of the interrupt request, and the state the stack after the acceptance of the interrupt request.

Save other necessary registers at the beginning of the interrupt routine using software. Using the PUSHM instruction alone can save all the registers except the stack pointer (SP).

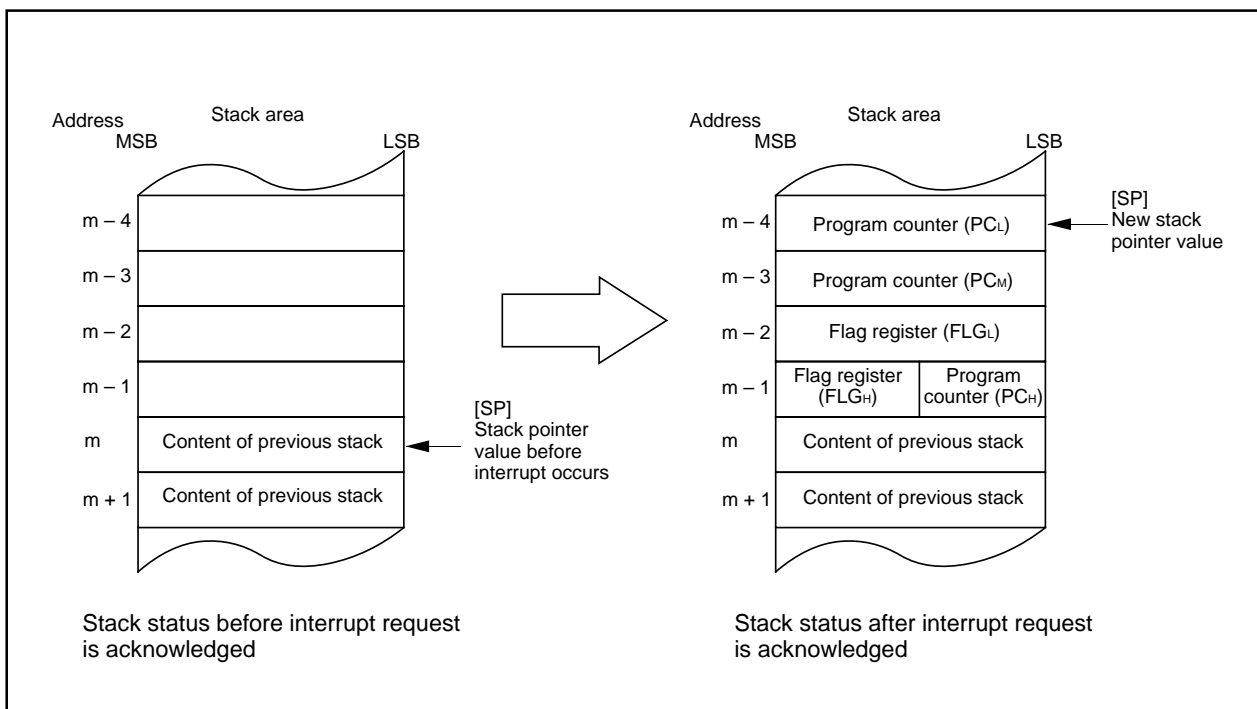


Figure 1.27. State of stack before and after acceptance of interrupt request

Interrupts

The operation of saving registers carried out in the interrupt sequence is dependent on whether the content of the stack pointer (Note), at the time of acceptance of an interrupt request, is even or odd. If the content of the stack pointer (Note) is even, the content of the flag register (FLG) and the content of the program counter (PC) are saved, 16 bits at a time. If odd, their contents are saved in two steps, 8 bits at a time. Figure 1.28 shows the operation of the saving registers.

Note: When any INT instruction in software numbers 32 to 63 has been executed, this is the stack pointer indicated by the U flag. Otherwise, it is the interrupt stack pointer (ISP).

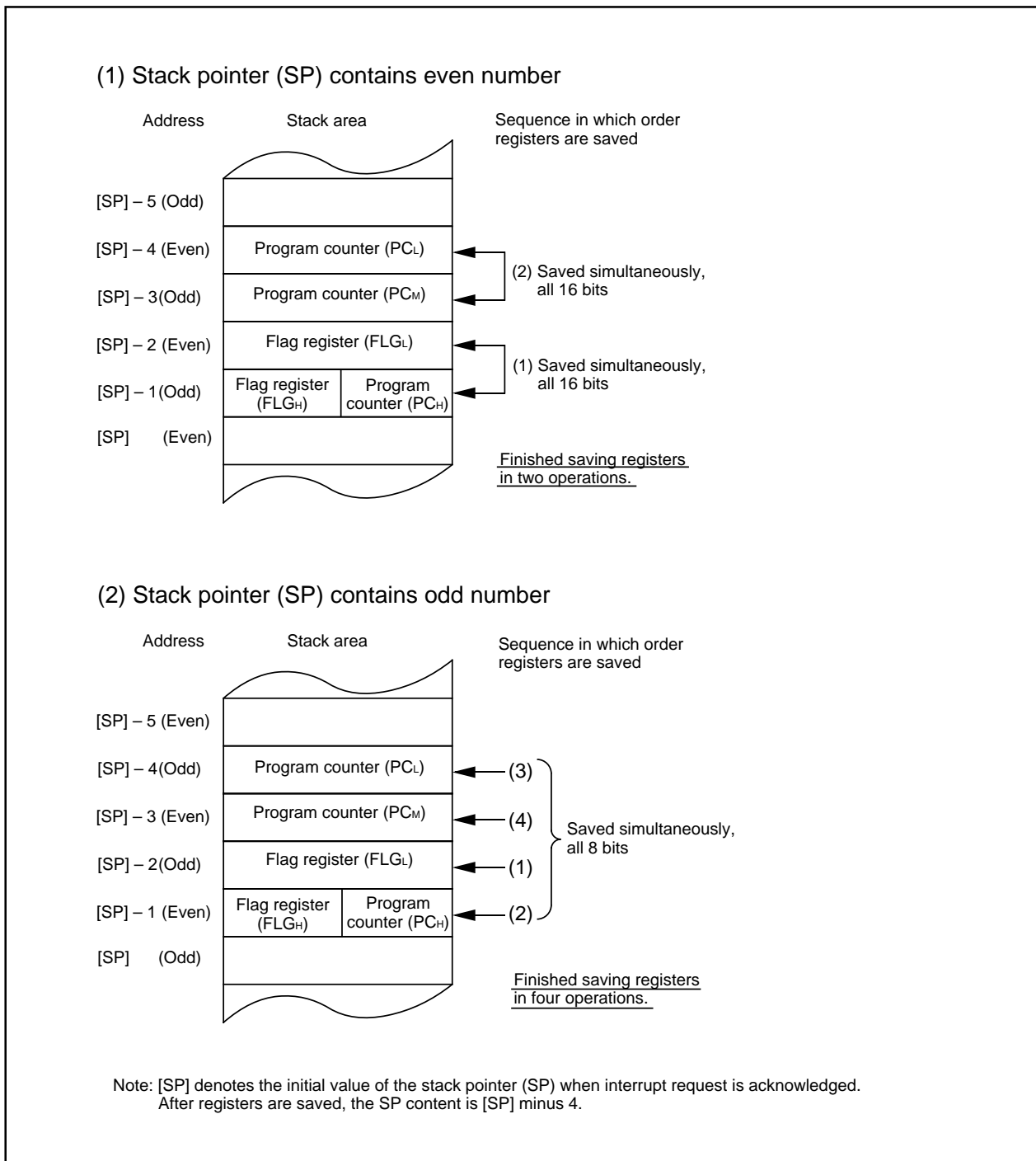


Figure 1.28. Operation of saving registers

Interrupts

Returning from an Interrupt Routine

Executing the REIT instruction at the end of an interrupt routine returns the contents of the flag register (FLG) as it was immediately before the start of interrupt sequence and the contents of the program counter (PC), both of which have been saved in the stack area. Then control returns to the program that was being executed before the acceptance of the interrupt request, so that the suspended process resumes.

Return the other registers saved by software within the interrupt routine using the POPM or similar instruction before executing the REIT instruction.

Interrupt Priority

If there are two or more interrupt requests occurring at a point in time within a single sampling (checking whether interrupt requests are made), the interrupt assigned a higher priority is accepted.

Assign an arbitrary priority to maskable interrupts (peripheral I/O interrupts) using the interrupt priority level select bit. If the same interrupt priority level is assigned, however, the interrupt assigned a higher hardware priority is accepted.

Priorities of the special interrupts, such as Reset (dealt with as an interrupt assigned the highest priority), watchdog timer interrupt, etc. are regulated by hardware.

Figure 1.29 shows the priorities of hardware interrupts.

Software interrupts are not affected by the interrupt priority. If an instruction is executed, control branches invariably to the interrupt routine.

Interrupt Priority Level Judge Circuit

This circuit selects the interrupt with the highest priority level when two or more interrupts are generated simultaneously.

Figure 1.30 shows the interrupt resolution circuit.

Interrupts

Reset > \overline{DBC} > Watchdog timer > Peripheral I/O > Single step > Address match

Figure 1.29. Hardware interrupts priorities

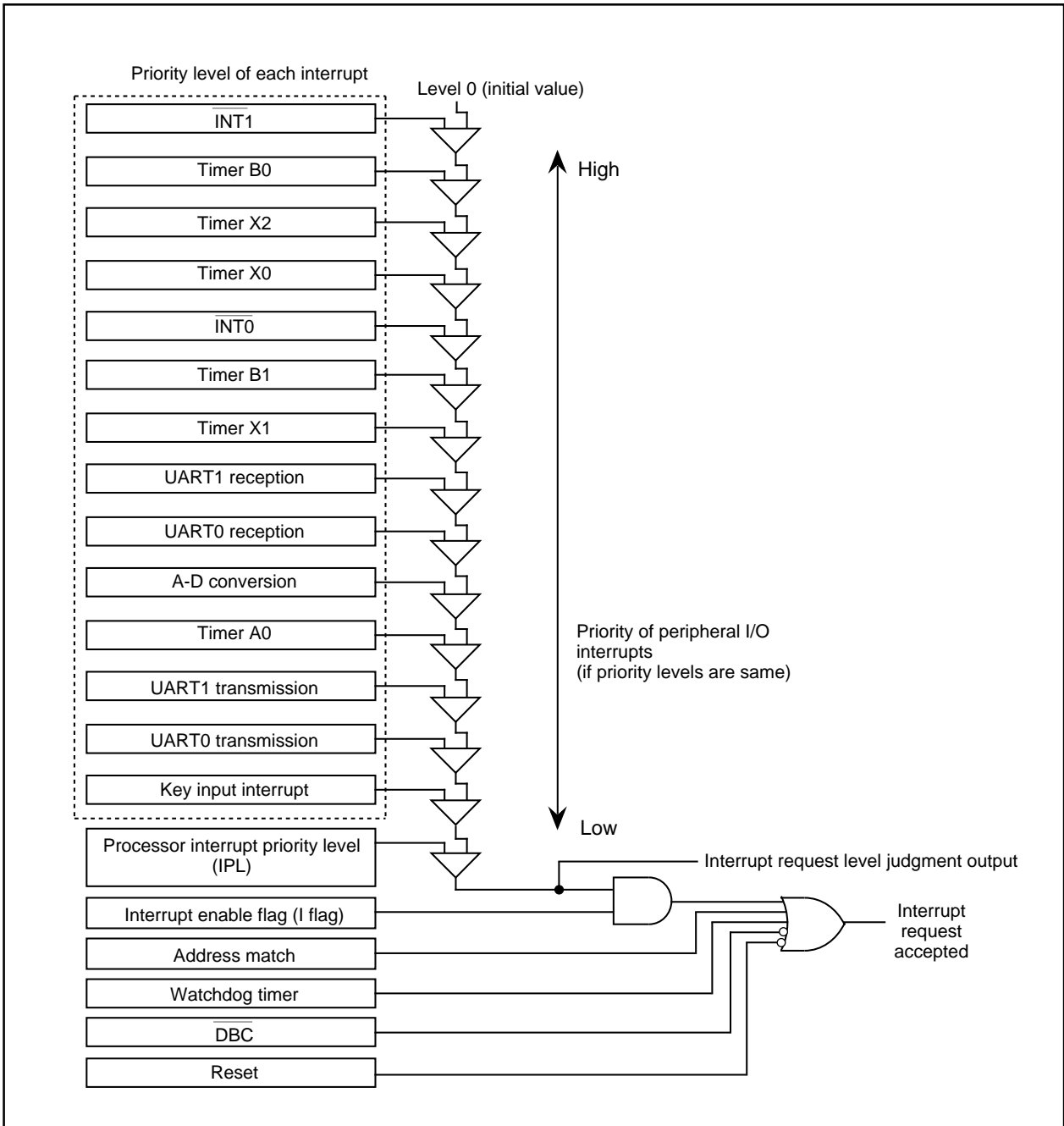


Figure 1.30. Interrupt resolution circuit

Key Input Interrupt

Key Input Interrupt

If the direction register of any of P00 to P07 is set for input and a falling edge is input to that port, a key input interrupt is generated. A key input interrupt can also be used as a key-on wakeup function for cancelling the wait mode or stop mode. Figure 1.31 shows the block diagram of the key input interrupt. Note that if an "L" level is input to any pin that has not been disabled for input, inputs to the other pins are not detected as an interrupt.

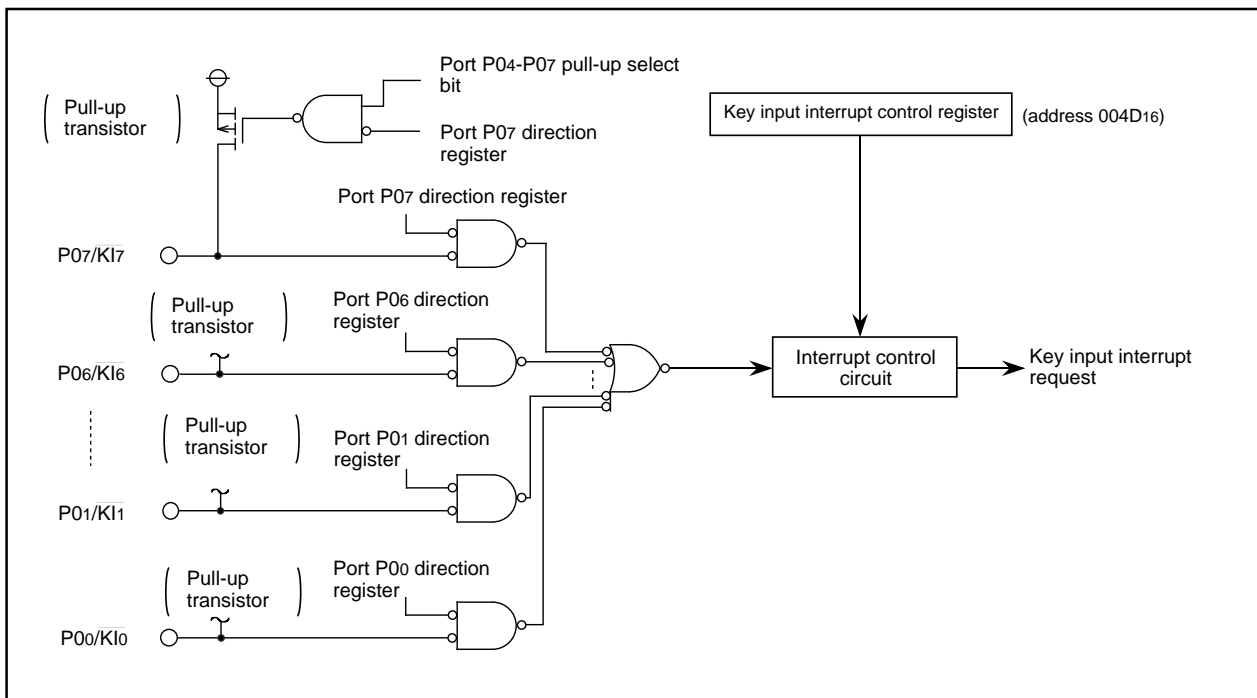


Figure 1.31. Block diagram of key input interrupt

Address Match Interrupt

Address Match Interrupt

An address match interrupt is generated when the address match interrupt address register contents match the program counter value. Two address match interrupts can be set, each of which can be enabled and disabled by an address match interrupt enable bit. Address match interrupts are not affected by the interrupt enable flag (I flag) and processor interrupt priority level (IPL). For an address match interrupt, the value of the program counter (PC) that is saved to the stack area varies depending on the instruction being executed.

Figure 1.32 shows the address match interrupt-related registers.

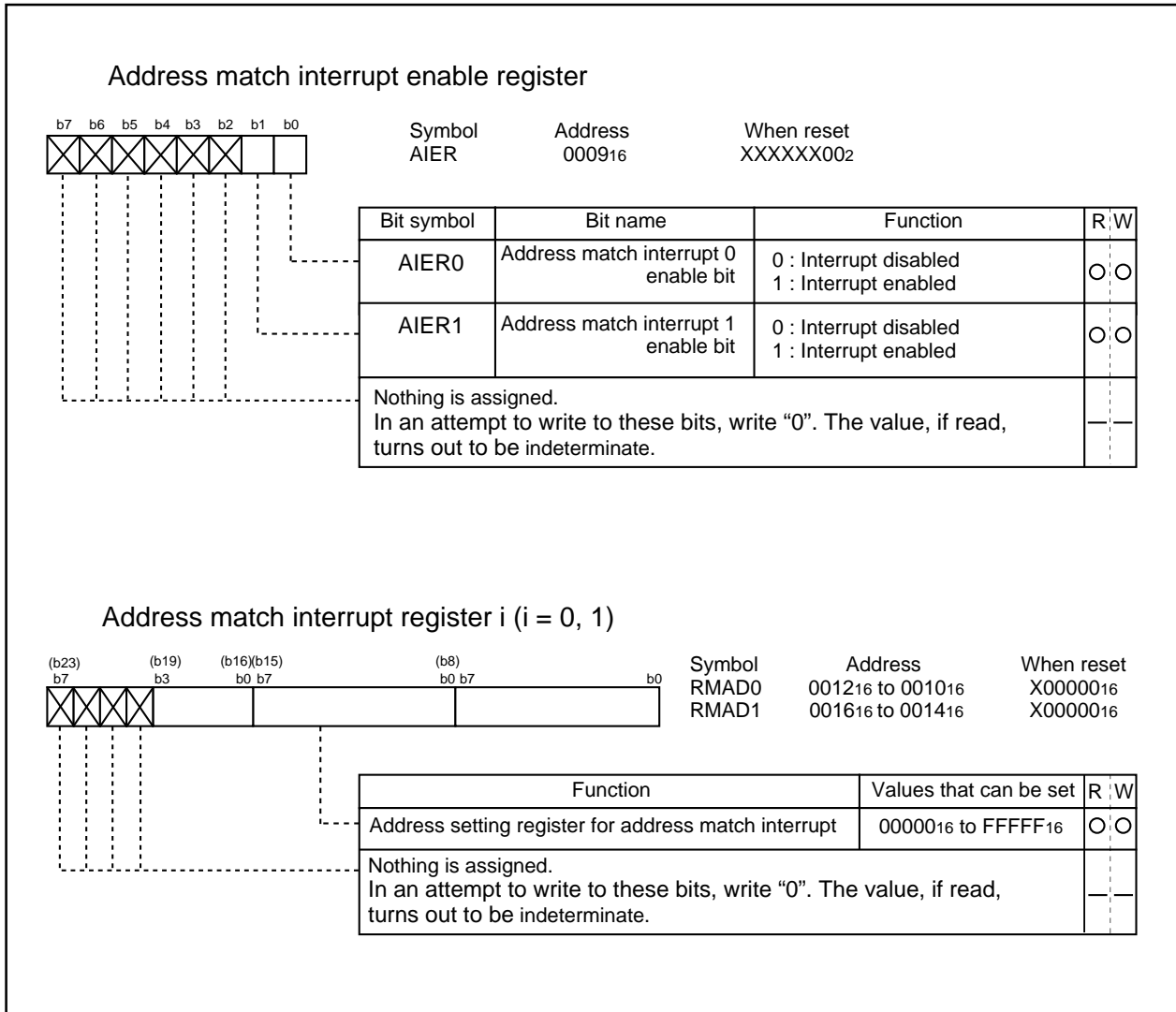


Figure 1.32. Address match interrupt-related registers

Interrupts

Precautions for Interrupts

(1) Reading address 00000₁₆

- When maskable interrupt is occurred, CPU read the interrupt information (the interrupt number and interrupt request level) in the interrupt sequence.

The interrupt request bit of the certain interrupt written in address 00000₁₆ will then be set to "0".

Reading address 00000₁₆ by software sets enabled highest priority interrupt source request bit to "0".

Though the interrupt is generated, the interrupt routine may not be executed.

Do not read address 00000₁₆ by software.

(2) Setting the stack pointer

- The value of the stack pointer immediately after reset is initialized to 0000₁₆. Accepting an interrupt before setting a value in the stack pointer may become a factor of runaway. Be sure to set a value in the stack pointer before accepting an interrupt. Concerning the first instruction immediately after reset, generating any interrupts is prohibited.

(3) External interrupt

- Either an "L" level or an "H" level of at least 250 ns width is necessary for the signal input to pins $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ regardless of the CPU operation clock.
- When changing a polarity of pins $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$, the interrupt request bit may become "1". Clear the interrupt request bit after changing the polarity. Figure 1.33 shows the switching condition of $\overline{\text{INT}}$ interrupt request.

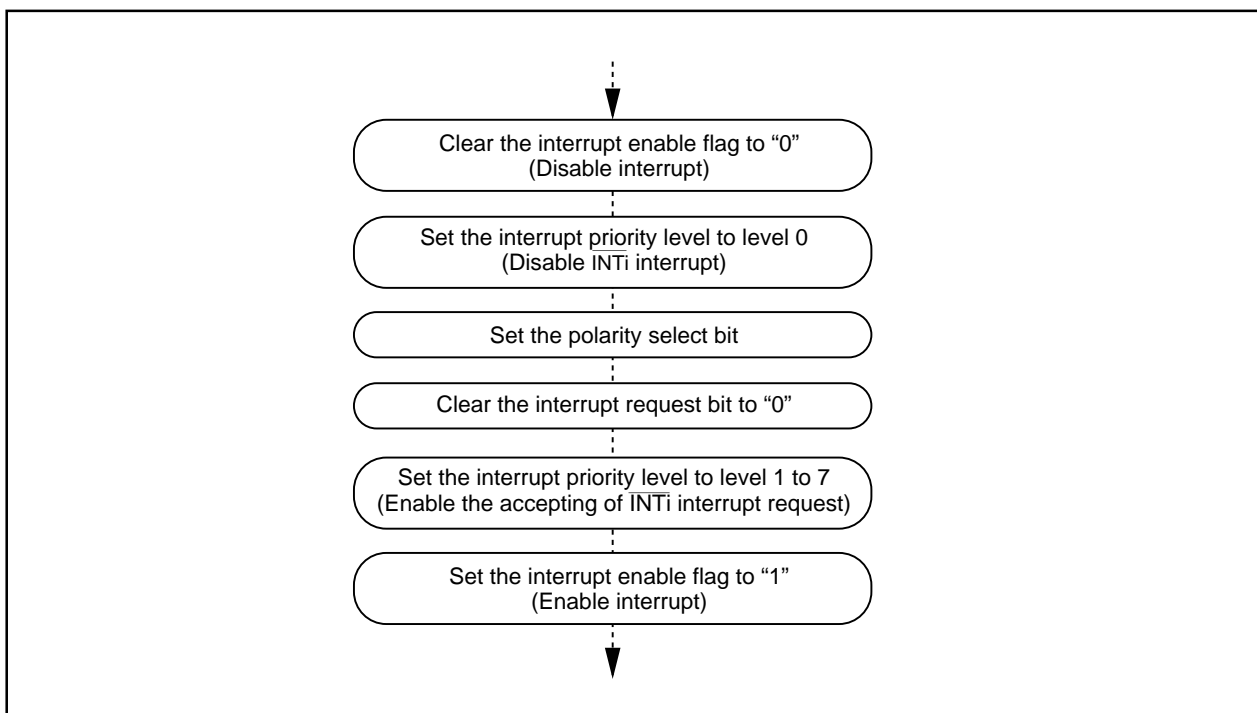


Figure 1.33. Switching condition of $\overline{\text{INT}}$ interrupt request

(4) Changing interrupt control register

See "Changing Interrupt Control Register".

Watchdog Timer

Watchdog Timer

The watchdog timer has the function of detecting when the program is out of control. The watchdog timer is a 15-bit counter which down-counts the clock derived by dividing the BCLK using the prescaler. A watchdog timer interrupt is generated when an underflow occurs in the watchdog timer. When XIN is selected for the BCLK, bit 7 of the watchdog timer control register (address 000F₁₆) selects the prescaler division ratio (by 16 or by 128). When XCIN is selected as the BCLK, the prescaler is set for division by 2 regardless of bit 7 of the watchdog timer control register (address 000F₁₆).

When XIN is selected in BCLK

$$\text{Watchdog timer cycle} = \frac{\text{Prescaler division ratio (16 or 128)} \times \text{watchdog timer count (32768)}}{\text{BCLK}}$$

When XCIN is selected in BCLK

$$\text{Watchdog timer cycle} = \frac{\text{Prescaler division ratio (2)} \times \text{watchdog timer count (32768)}}{\text{BCLK}}$$

For example, when BCLK is 10MHz and the prescaler division ratio is set to 16, the watchdog timer cycle is approximately 52.4 ms.

The watchdog timer is initialized by writing to the watchdog timer start register (address 000E₁₆) and when a watchdog timer interrupt request is generated. The prescaler is initialized only when the microcomputer is reset. After a reset is cancelled, the watchdog timer and prescaler are both stopped. The count is started by writing to the watchdog timer start register (address 000E₁₆). In stop mode and wait mode the watchdog timer and prescaler are stopped. Counting is resumed from the held value when the modes are released. Figure 1.34 shows the block diagram of the watchdog timer. Figure 1.35 shows the watchdog timer-related registers.

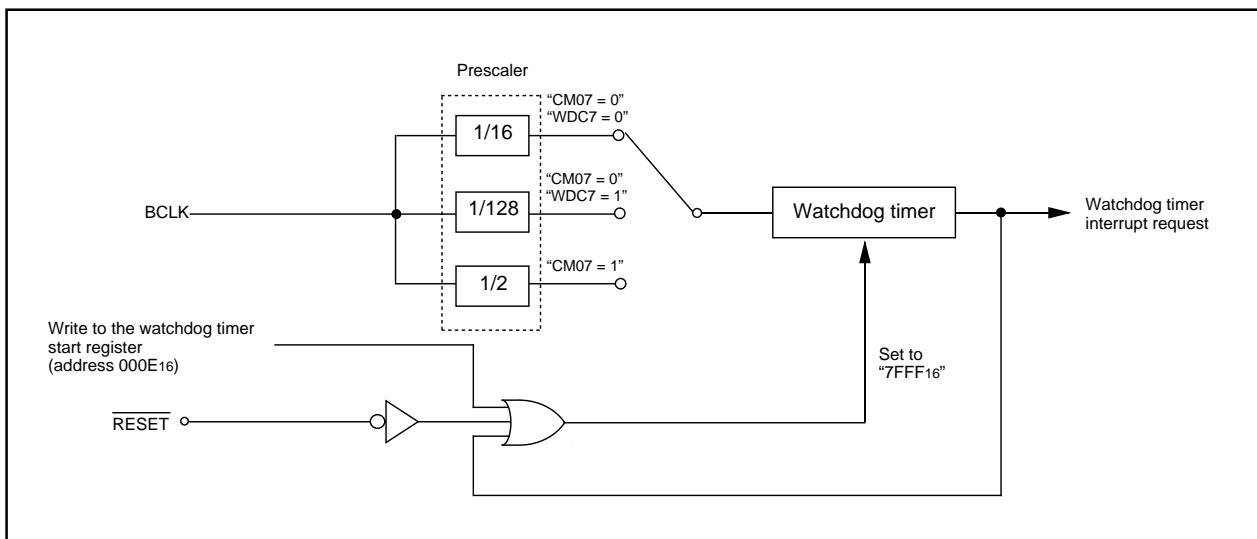


Figure 1.34. Block diagram of watchdog timer

Watchdog Timer

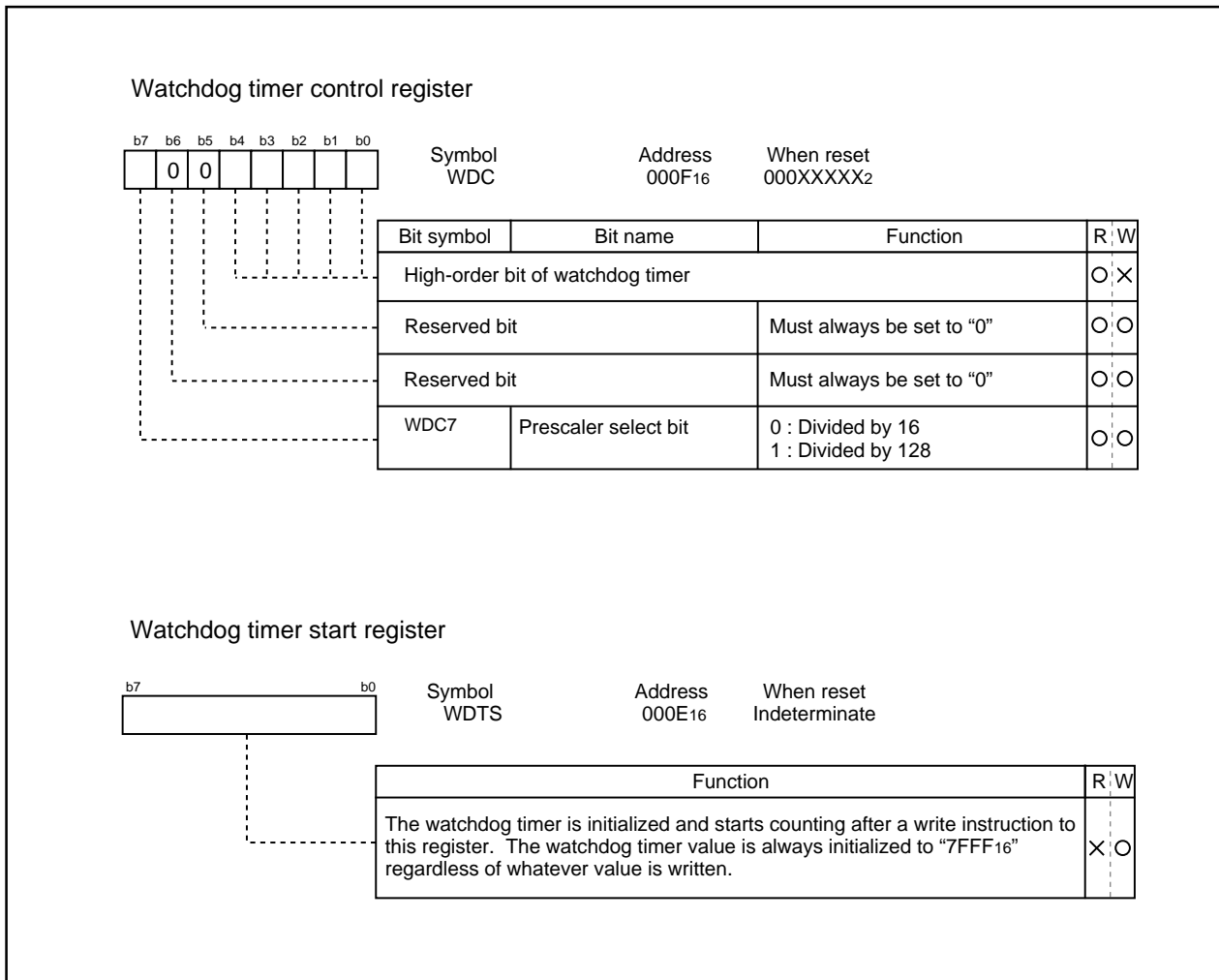


Figure 1.35. Watchdog timer control and start registers

Timer

Timer

There are six 16-bit timers. These timers can be classified by function into timer A (one), timers B (two) and timers X (three). All these timers function independently. Figure 1.36 show the block diagram of timers.

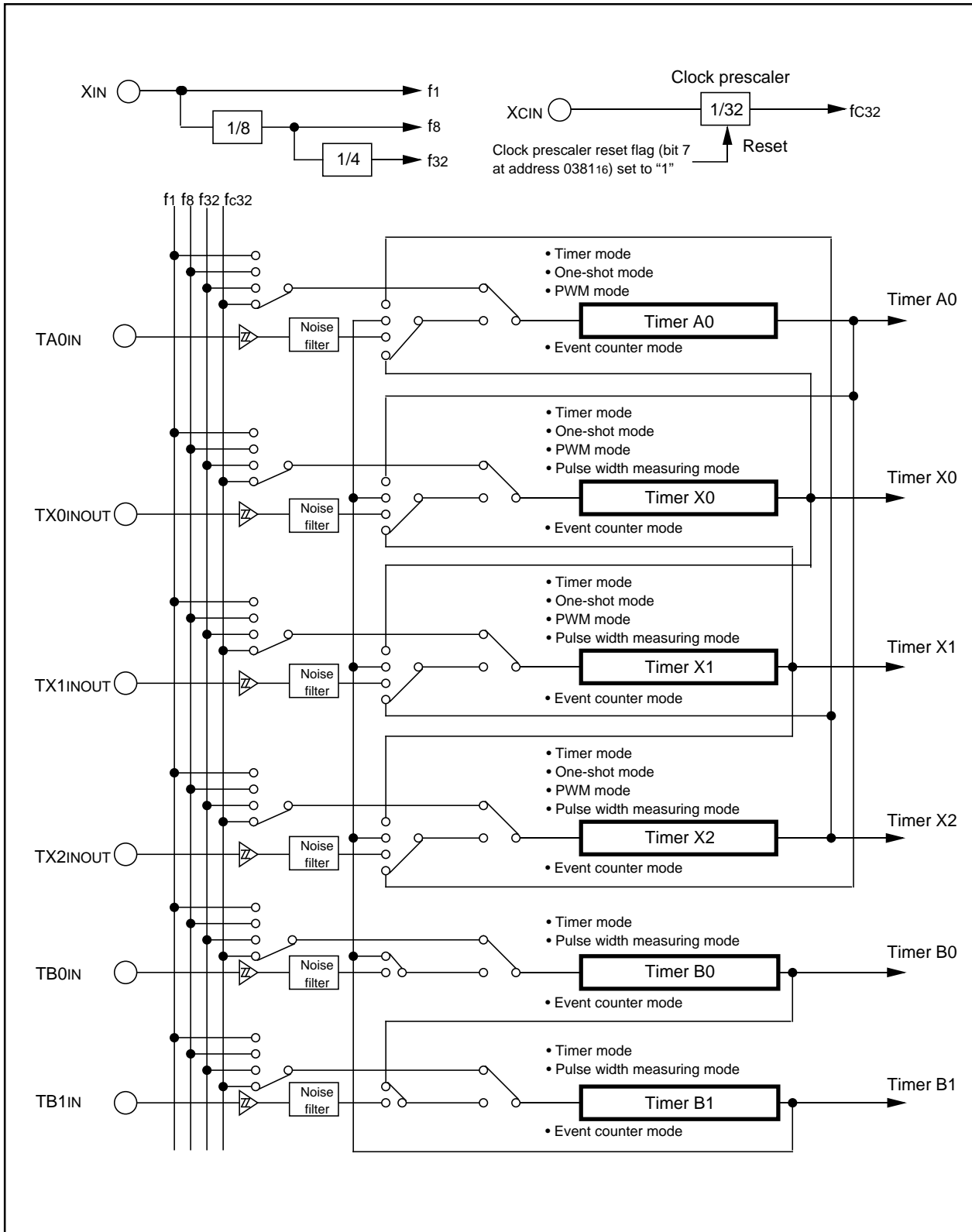


Figure 1.36. Timer block diagram

Timer A

Timer A

Figure 1.37 shows the block diagram of timer A. Figures 1.38 to 1.40 show the timer A-related registers. Use the timer A0 mode register bits 0 and 1 to choose the desired mode.

Timer A has the four operation modes listed as follows:

- Timer mode: The timer counts an internal count source.
- Event counter mode: The timer counts pulses from an external source or a timer overflow.
- One-shot timer mode: The timer stops counting when the count reaches "000016".
- Pulse width modulation (PWM) mode: The timer outputs pulses of a given width.

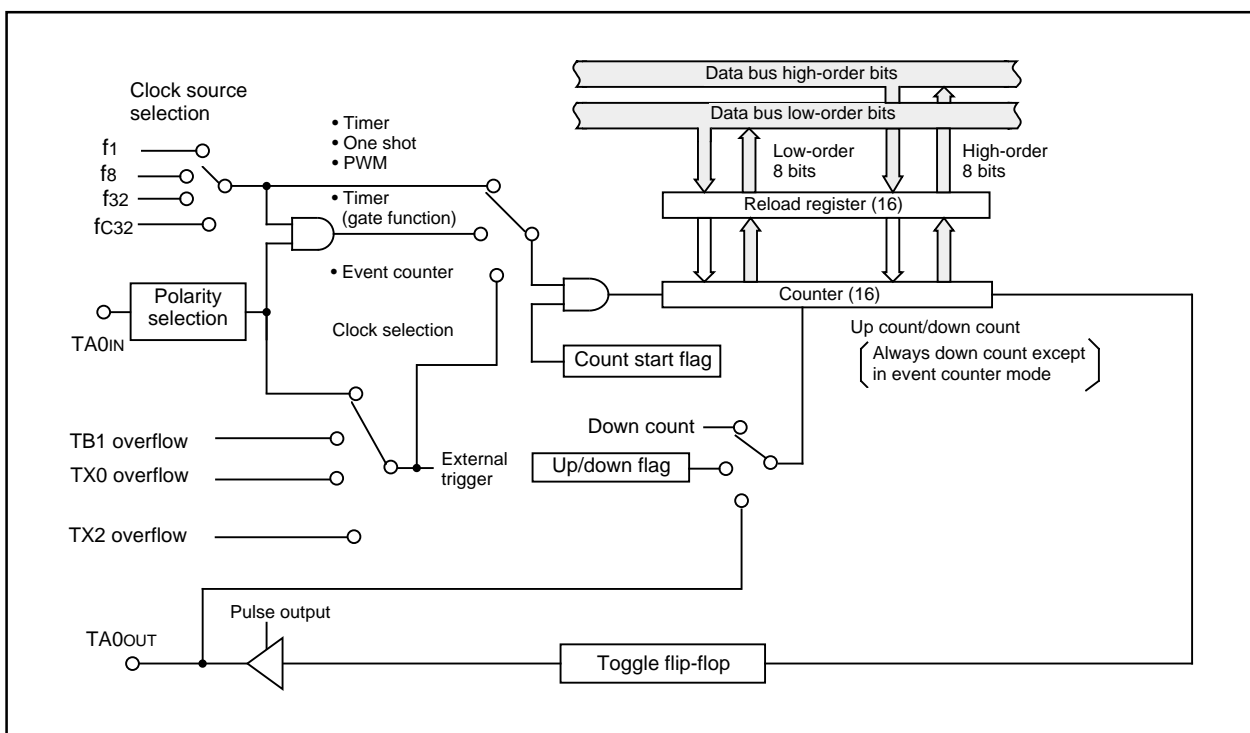


Figure 1.37. Block diagram of timer A

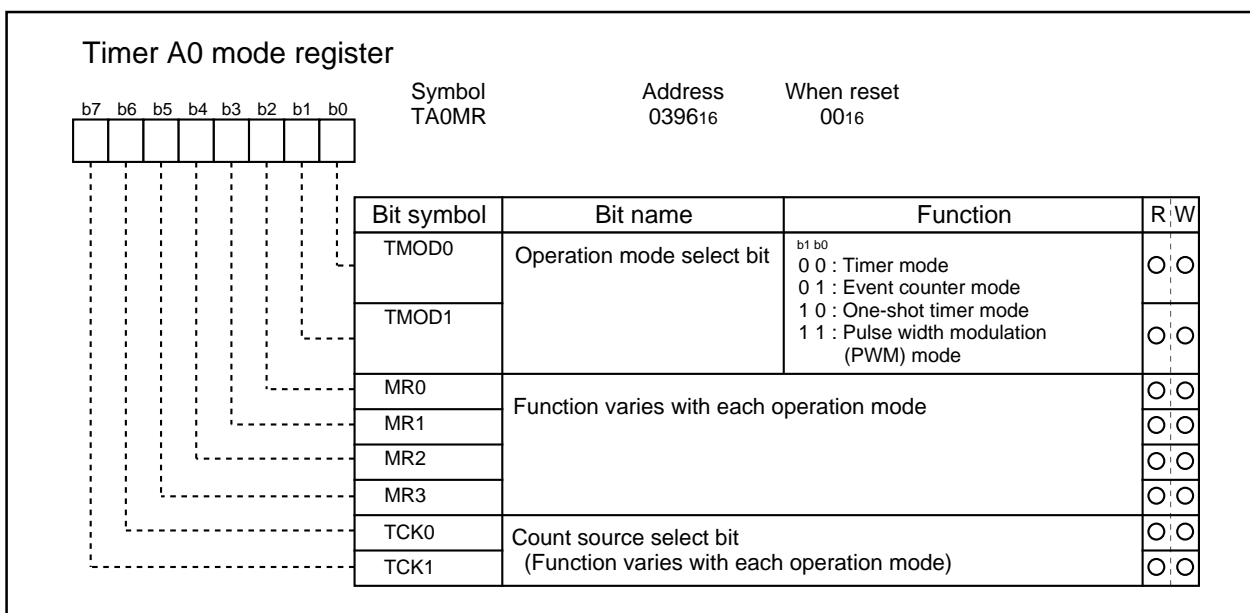


Figure 1.38. Timer A-related registers (1)

Timer A

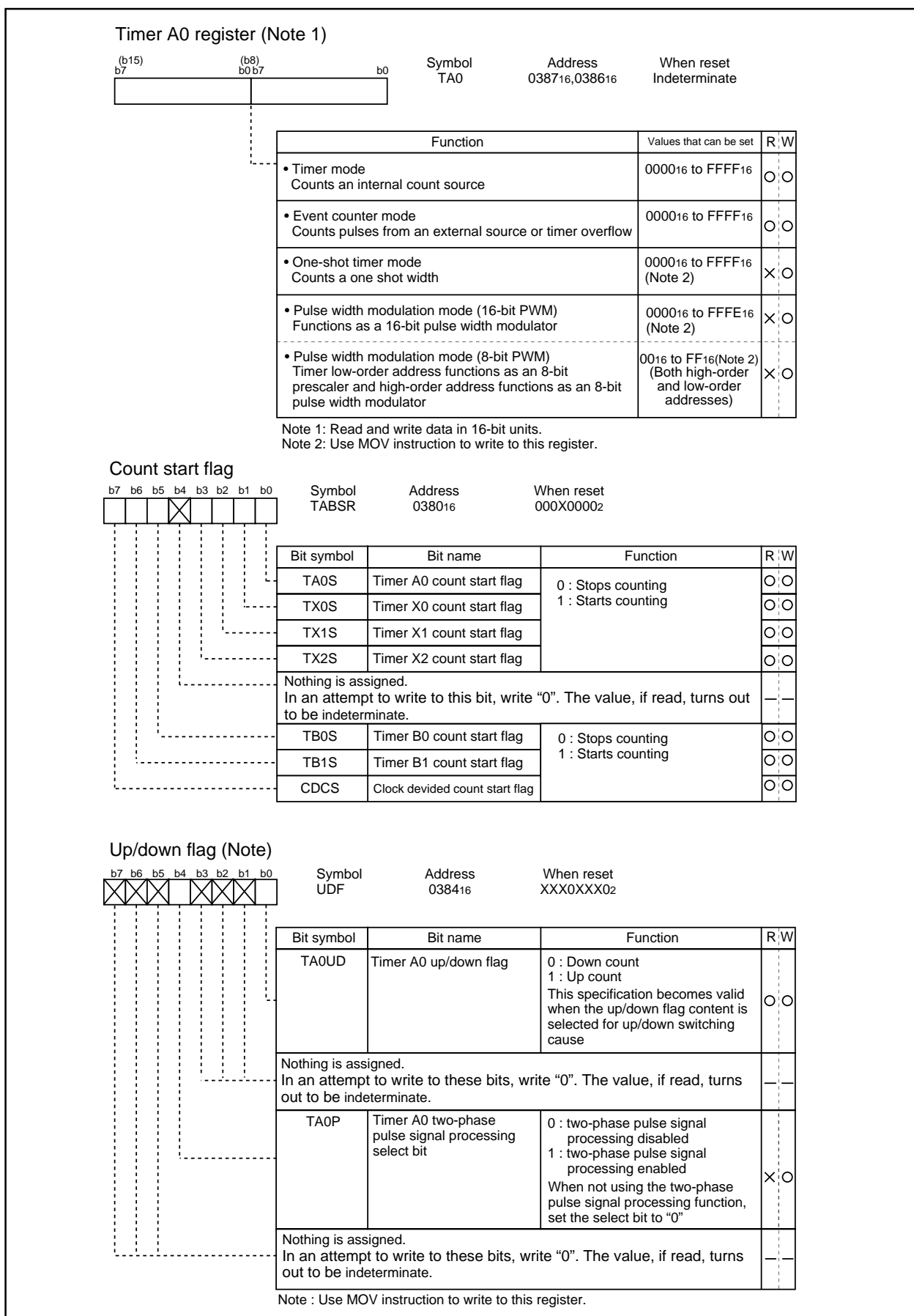


Figure 1.39. Timer A-related registers (2)

Timer A

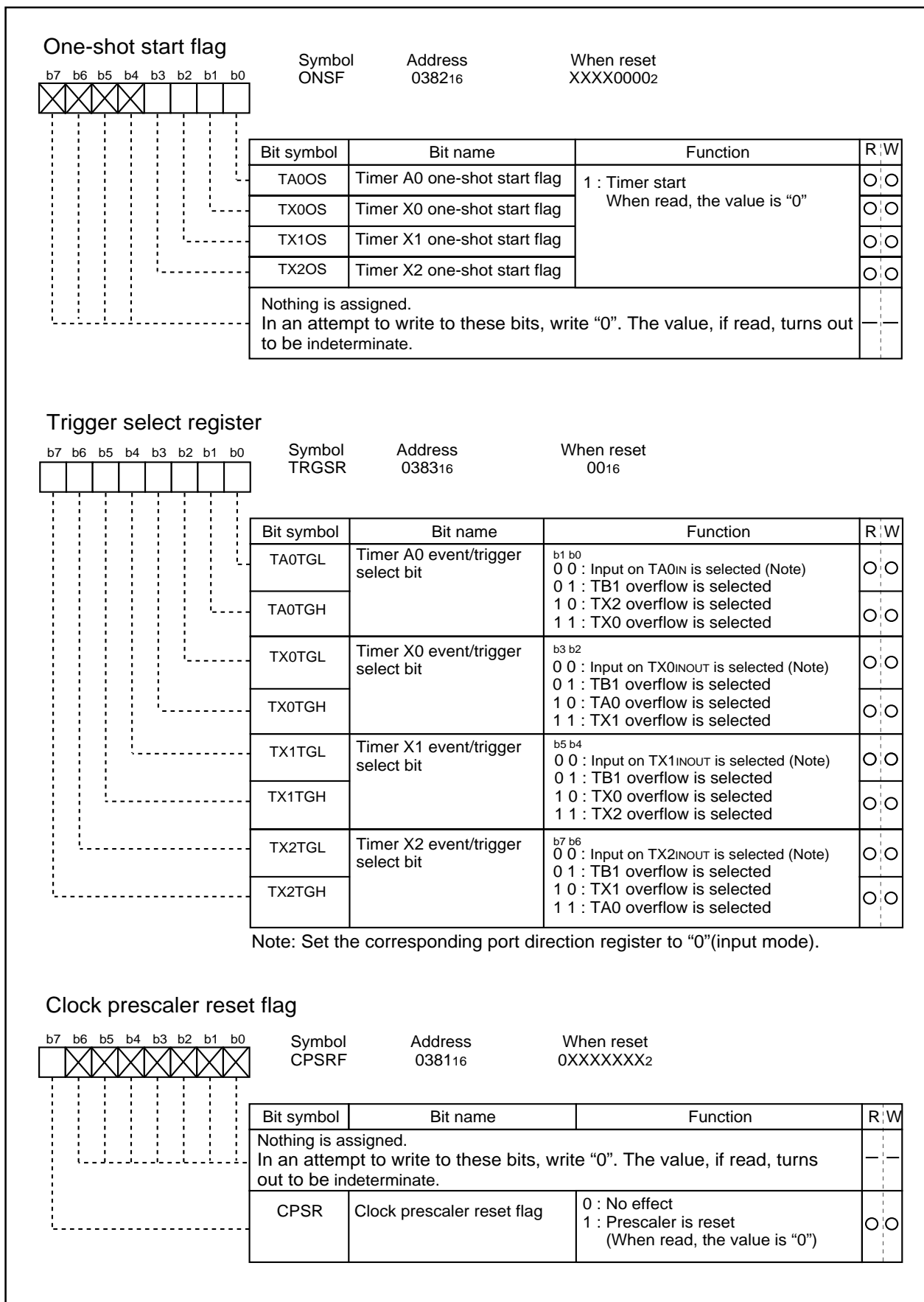


Figure 1.40. Timer A-related registers (3)

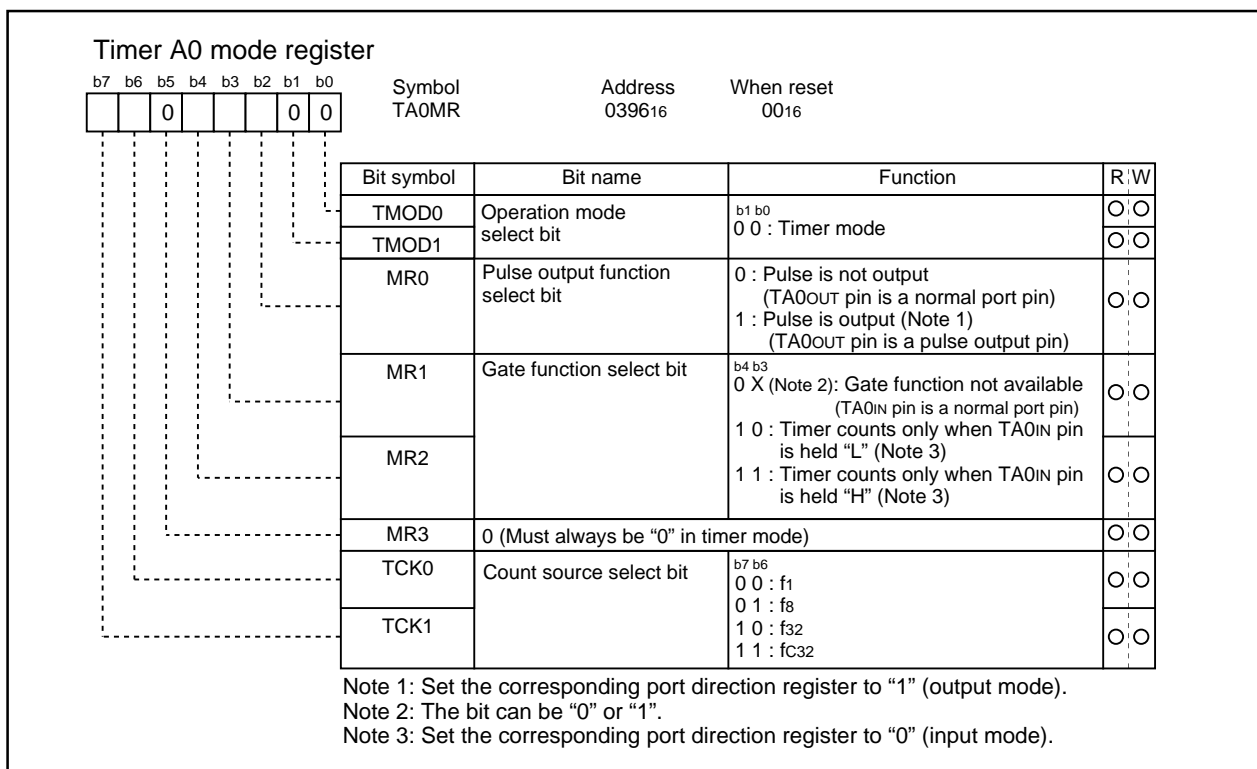
Timer A

(1) Timer mode

In this mode, the timer counts an internally generated count source. (See Table 1.12.) Figure 1.41 shows the timer A0 mode register in timer mode.

Table 1.12. Specifications of timer mode

Item	Specification
Count source	f1, f8, f32, fc32
Count operation	<ul style="list-style-type: none"> • Down count • When the timer underflows, it reloads the reload register contents before continuing counting
Divide ratio	1/(n+1) n : Set value
Count start condition	Count start flag is set (= 1)
Count stop condition	Count start flag is reset (= 0)
Interrupt request generation timing	When the timer underflows
TA0IN pin function	Programmable I/O port or gate input
TA0OUT pin function	Programmable I/O port or pulse output
Read from timer	Count value can be read out by reading timer A0 register
Write to timer	<ul style="list-style-type: none"> • When counting stopped When a value is written to timer A0 register, it is written to both reload register and counter • When counting in progress When a value is written to timer A0 register, it is written to only reload register (Transferred to counter at next reload time)
Select function	<ul style="list-style-type: none"> • Gate function Counting can be started and stopped by the TA0IN pin's input signal • Pulse output function Each time the timer underflows, the TA0OUT pin's polarity is reversed

**Figure 1.41. Timer A0 mode register in timer mode**

Timer A

(2) Event counter mode

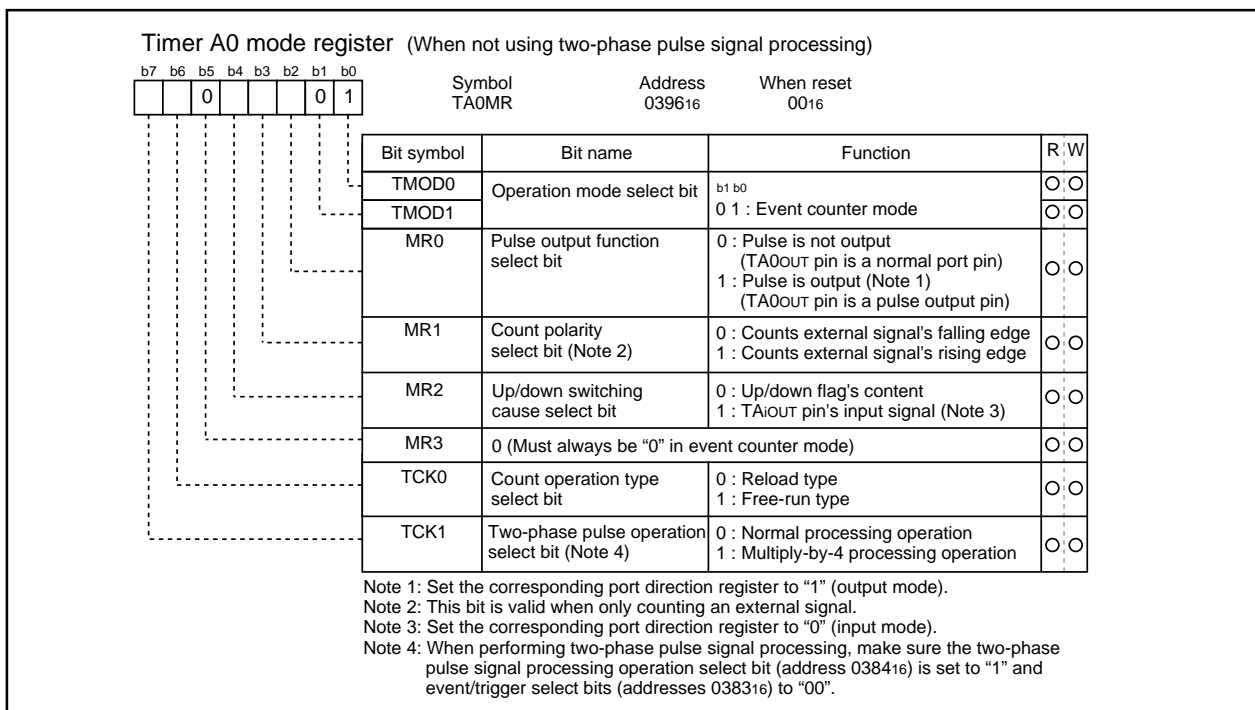
In this mode, the timer counts an external signal or an internal timer's overflow. Timer A0 can count a single-phase and a two-phase external signal. Table 1.13 lists timer specifications when counting a single-phase external signal. Figure 1.42 shows the timer A0 mode register in event counter mode.

Table 1.14 lists timer specifications when counting a two-phase external signal. Figure 1.43 shows the timer A0 mode register in event counter mode.

Table 1.13. Timer specifications in event counter mode (when not processing two-phase pulse signal)

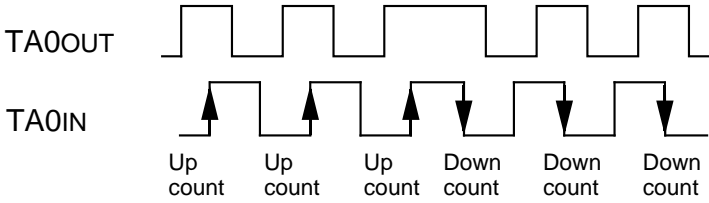
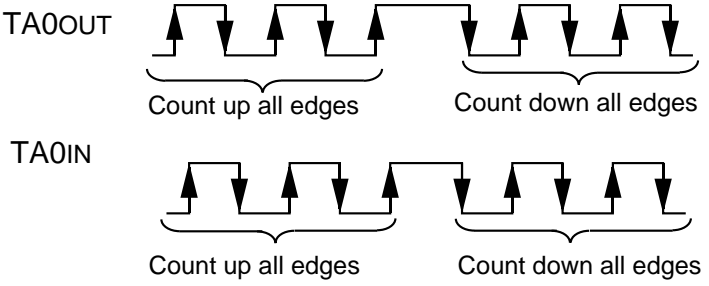
Item	Specification
Count source	<ul style="list-style-type: none"> External signals input to TA0IN pin (effective edge can be selected by software) TB1 overflow, TX0 overflow, TX2 overflow
Count operation	<ul style="list-style-type: none"> Up count or down count can be selected by external signal or software When the timer overflows or underflows, it reloads the reload register contents before continuing counting (Note)
Divide ratio	$1 / (FFFF_{16} - n + 1)$ for up count $1 / (n + 1)$ for down count n : Set value
Count start condition	Count start flag is set (= 1)
Count stop condition	Count start flag is reset (= 0)
Interrupt request generation timing	The timer overflows or underflows
TA0IN pin function	Programmable I/O port or count source input
TA0OUT pin function	Programmable I/O port, pulse output, or up/down count select input
Read from timer	Count value can be read out by reading timer A0 register
Write to timer	<ul style="list-style-type: none"> When counting stopped When a value is written to timer A0 register, it is written to both reload register and counter When counting in progress When a value is written to timer A0 register, it is written to only reload register (Transferred to counter at next reload time)
Select function	<ul style="list-style-type: none"> Free-run count function Even when the timer overflows or underflows, the reload register content is not reloaded to it Pulse output function Each time the timer overflows or underflows, the TA0OUT pin's polarity is reversed

Note: This does not apply when the free-run function is selected.

**Figure 1.42. Timer A0 mode register in event counter mode**

Timer A

Table 1.14. Timer specifications in event counter mode (when processing two-phase pulse signal)

Item	Specification
Count source	<ul style="list-style-type: none"> Two-phase pulse signals input to TA0IN or TA0OUT pin
Count operation	<ul style="list-style-type: none"> Up count or down count can be selected by two-phase pulse signal When the timer overflows or underflows, the reload register content is reloaded and the timer starts over again (Note)
Divide ratio	<ul style="list-style-type: none"> $1 / (FFFF_{16} - n + 1)$ for up count $1 / (n + 1)$ for down count <p style="text-align: right;">n : Set value</p>
Count start condition	Count start flag is set (= 1)
Count stop condition	Count start flag is reset (= 0)
Interrupt request generation timing	Timer overflows or underflows
TA0IN pin function	Two-phase pulse input
TA0OUT pin function	Two-phase pulse input
Read from timer	Count value can be read out by reading timer A0 register
Write to timer	<ul style="list-style-type: none"> When counting stopped When a value is written to timer A0 register, it is written to both reload register and counter When counting in progress When a value is written to timer A0 register, it is written to only reload register. (Transferred to counter at next reload time.)
Select function	<ul style="list-style-type: none"> Normal processing operation The timer counts up rising edges or counts down falling edges on the TA0IN pin when input signal on the TA0OUT pin is "H" <div style="text-align: center;">  </div> <ul style="list-style-type: none"> Multiply-by-4 processing operation If the phase relationship is such that the TA0IN pin goes "H" when the input signal on the TA0OUT pin is "H", the timer counts up rising and falling edges on the TA0OUT and TA0IN pins. If the phase relationship is such that the TA0IN pin goes "L" when the input signal on the TA0OUT pin is "H", the timer counts down rising and falling edges on the TA0OUT and TA0IN pins. <div style="text-align: center;">  </div>

Note: This does not apply when the free-run function is selected.

Timer A

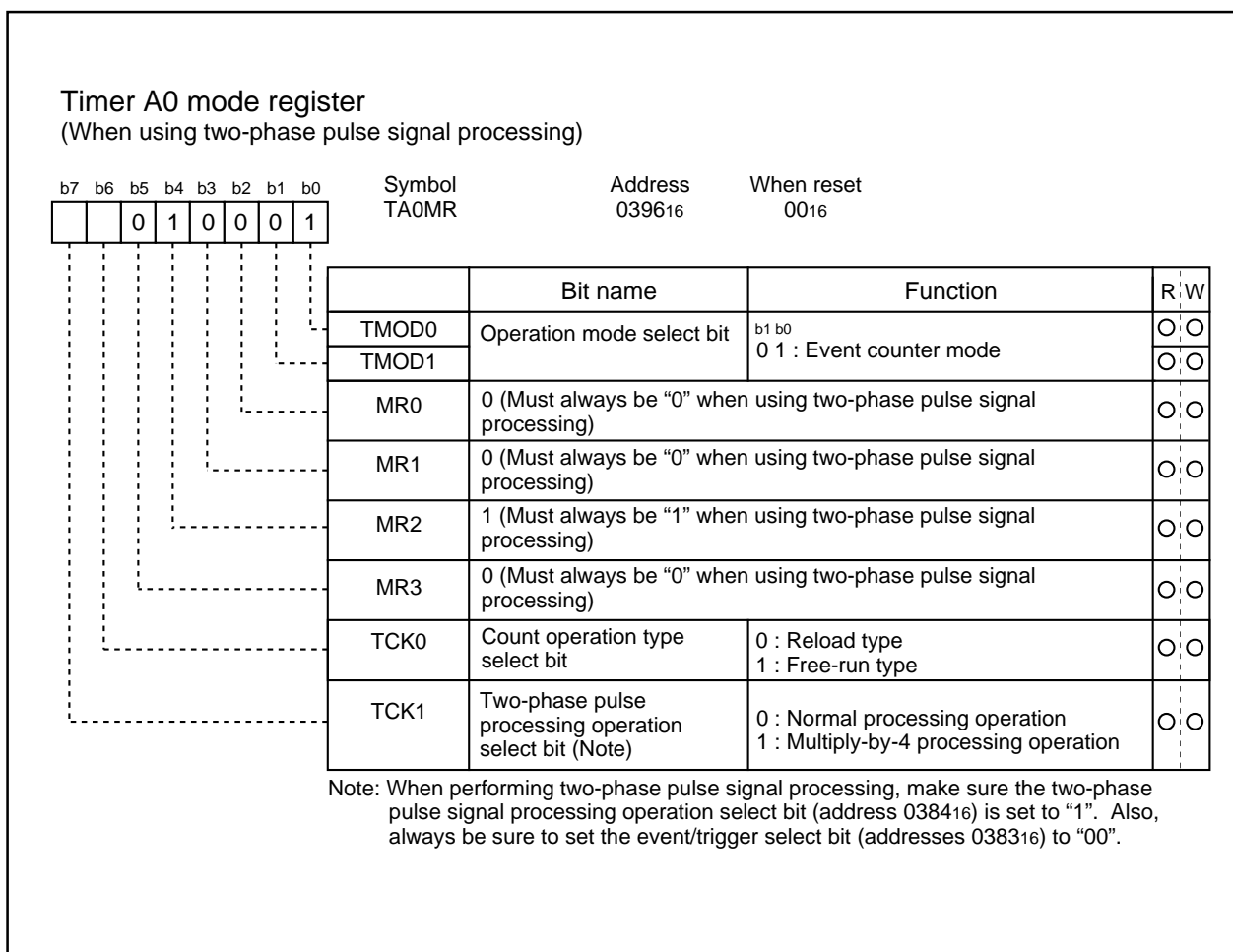


Figure 1.43. Timer A0 mode register in event counter mode

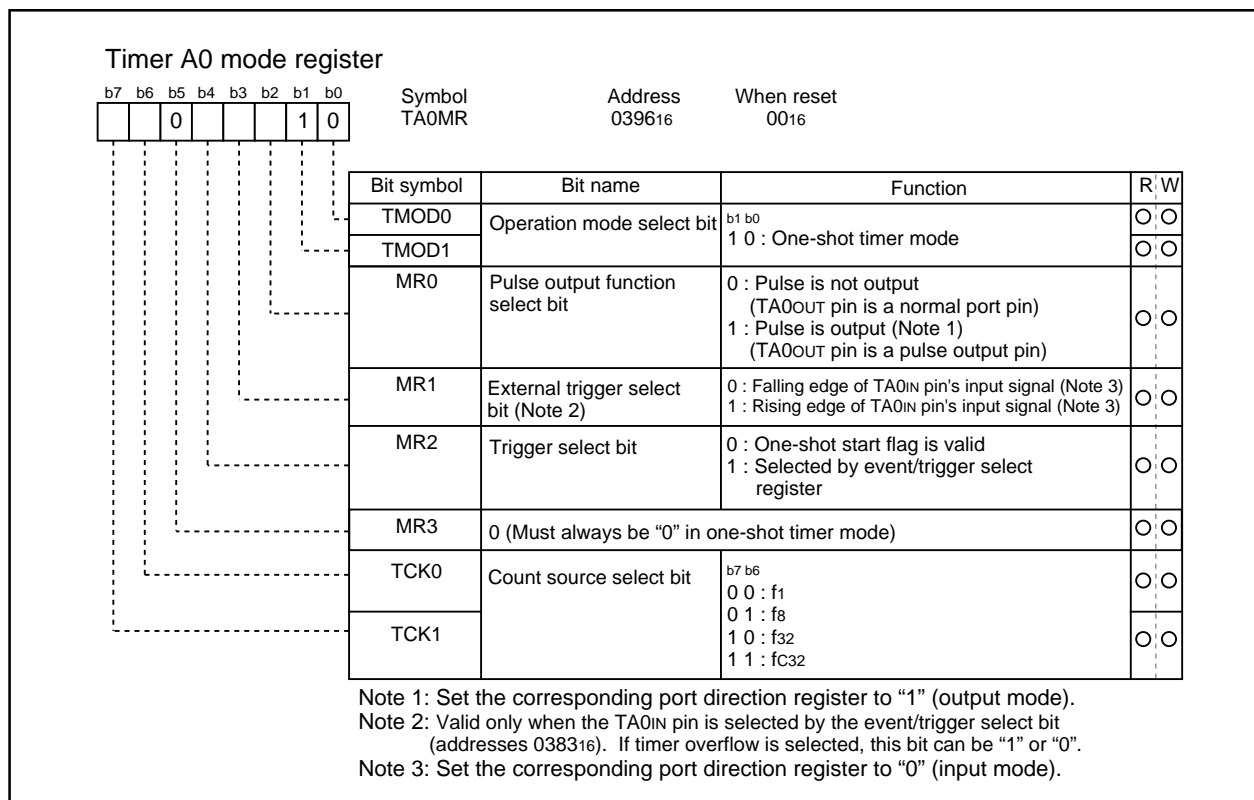
Timer A

(3) One-shot timer mode

In this mode, the timer operates only once. (See Table 1.15.) When a trigger occurs, the timer starts up and continues operating for a given period. Figure 1.44 shows the timer A0 mode register in one-shot timer mode.

Table 1.15. Timer specifications in one-shot timer mode

Item	Specification
Count source	f1, f8, f32, fc32
Count operation	<ul style="list-style-type: none"> The timer counts down When the count reaches 0000₁₆, the timer stops counting after reloading a new count If a trigger occurs when counting, the timer reloads a new count and restarts counting
Divide ratio	1/n n : Set value
Count start condition	<ul style="list-style-type: none"> An external trigger is input The timer overflows The one-shot start flag is set (= 1)
Count stop condition	<ul style="list-style-type: none"> A new count is reloaded after the count has reached 0000₁₆ The count start flag is reset (= 0)
Interrupt request generation timing	The count reaches 0000 ₁₆
TA0IN pin function	Programmable I/O port or trigger input
TA0OUT pin function	Programmable I/O port or pulse output
Read from timer	When timer A0 register is read, it indicates an indeterminate value
Write to timer	<ul style="list-style-type: none"> When counting stopped When a value is written to timer A0 register, it is written to both reload register and counter When counting in progress When a value is written to timer A0 register, it is written to only reload register (Transferred to counter at next reload time)

**Figure 1.44. Timer A0 mode register in one-shot timer mode**

Timer A

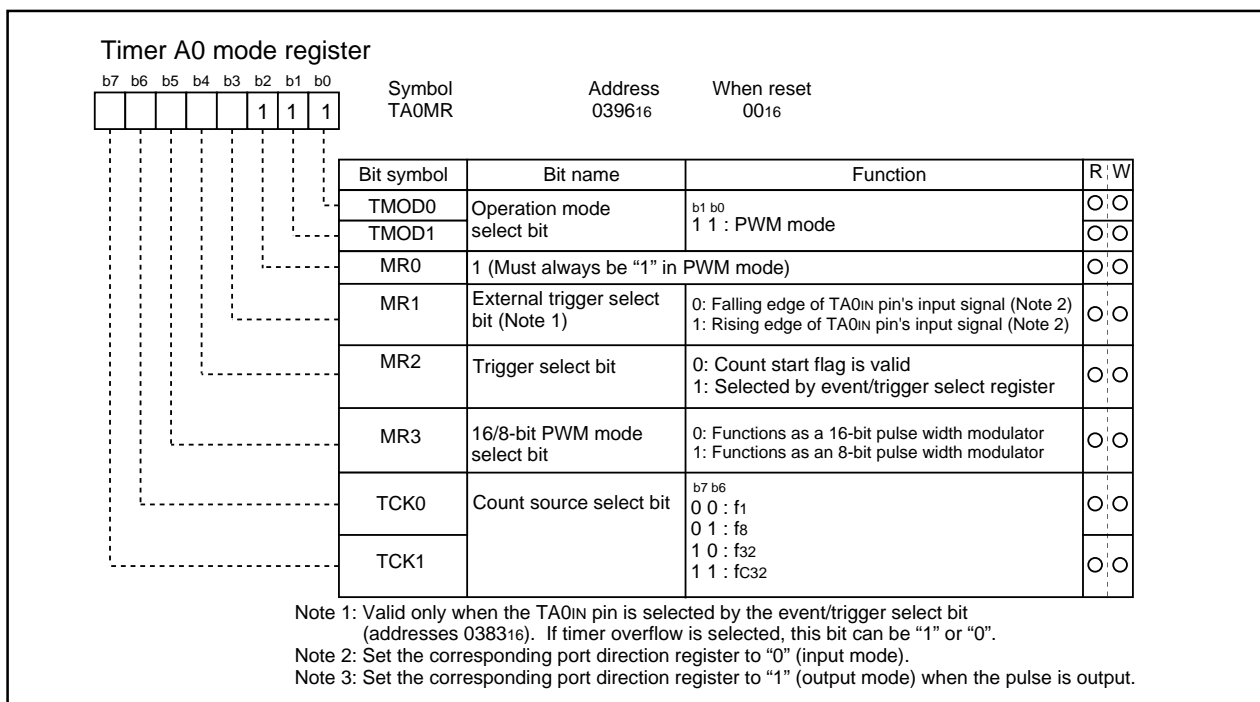
(4) Pulse width modulation (PWM) mode

In this mode, the timer outputs pulses of a given width in succession. (See Table 1.16.) In this mode, the counter functions as either a 16-bit pulse width modulator or an 8-bit pulse width modulator. Figure 1.45 shows the timer A0 mode register in pulse width modulation mode. Figure 1.46 shows the example of how a 16-bit pulse width modulator operates. Figure 1.47 shows the example of how an 8-bit pulse width modulator operates.

Table 1.16. Timer specifications in pulse width modulation mode

Item	Specification	
Count source	f ₁ , f ₈ , f ₃₂ , f _{C32}	
Count operation	<ul style="list-style-type: none"> The timer counts down (operating as an 8-bit or a 16-bit pulse width modulator) The timer reloads a new count at a rising edge of PWM pulse and continues counting The timer is not affected by a trigger that occurs when counting 	
16-bit PWM	<ul style="list-style-type: none"> High level width n / f_i n : Set value Cycle time $(2^{16}-1) / f_i$ fixed 	
8-bit PWM	<ul style="list-style-type: none"> High level width $n \times (m+1) / f_i$ n : values set to timer A0 register's high-order address Cycle time $(2^8-1) \times (m+1) / f_i$ m : values set to timer A0 register's low-order address 	
Count start condition	<ul style="list-style-type: none"> External trigger is input The timer overflows The count start flag is set (= 1) 	
Count stop condition	<ul style="list-style-type: none"> The count start flag is reset (= 0) 	
Interrupt request generation timing	8 bits PWM	<ul style="list-style-type: none"> Set value of "H" level width is except FF₁₆, 00₁₆ : PWM pulse goes "L" Set value of "H" level width is FF₁₆, 00₁₆ : Timing that count value goes to 01₁₆
	16 bits PWM	<ul style="list-style-type: none"> Set value of "H" level width is except FFFF₁₆, 0000₁₆ : PWM pulse goes "L" Set value of "H" level width is FFFF₁₆, 0000₁₆ : Timing that count value goes to 0001₁₆
TA0IN pin function	Programmable I/O port or trigger input	
TA0OUT pin function	Pulse output	
Read from timer	When timer A0 register is read, it indicates an indeterminate value	
Write to timer	<ul style="list-style-type: none"> When counting stopped : When a value is written to timer A0 register, it is written to both reload register and counter When counting in progress : When a value is written to timer A0 register, it is written to only reload register (Transferred to counter at next reload time) 	

Note: When set value of "H" level width is 00₁₆ or 0000₁₆, pulse outputs "L" level and inversion value, FF₁₆ or FFFF₁₆ is set to timer.

**Figure 1.45. Timer A0 mode register in pulse width modulation mode**

Timer A

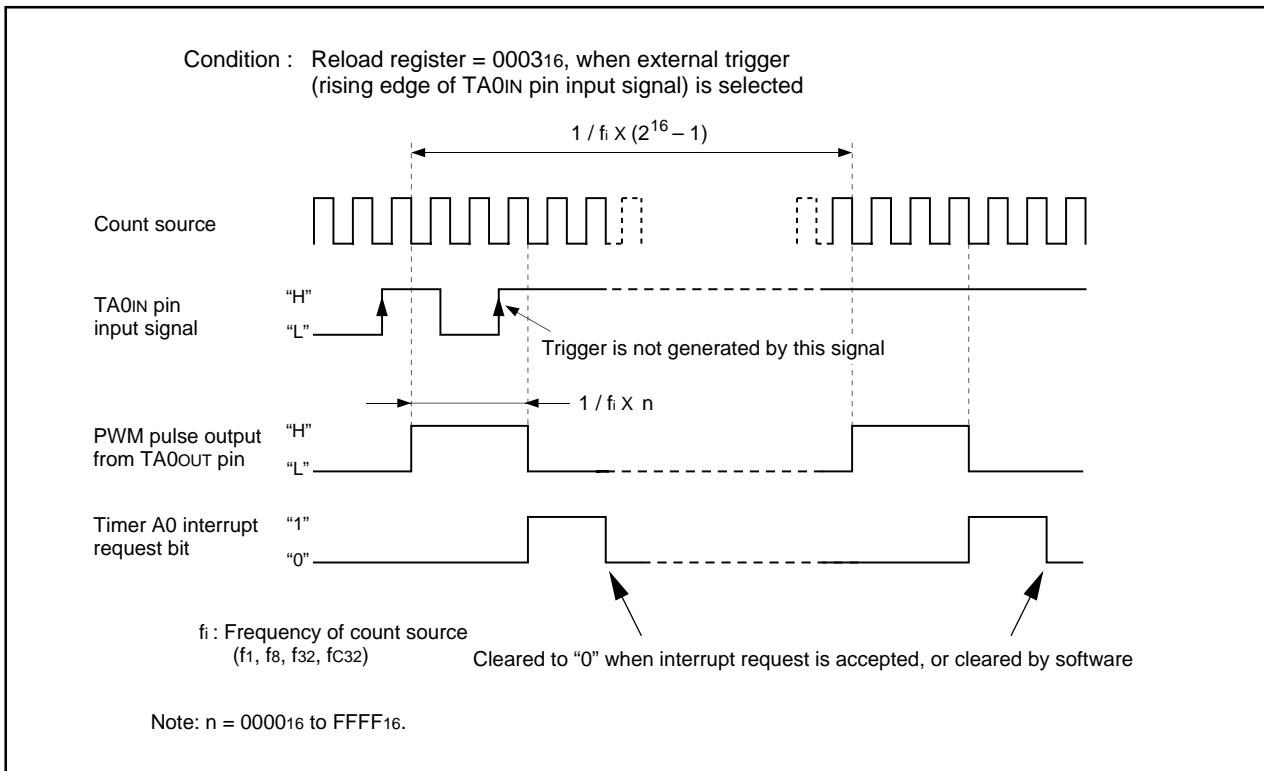


Figure 1.46. Example of how a 16-bit pulse width modulator operates

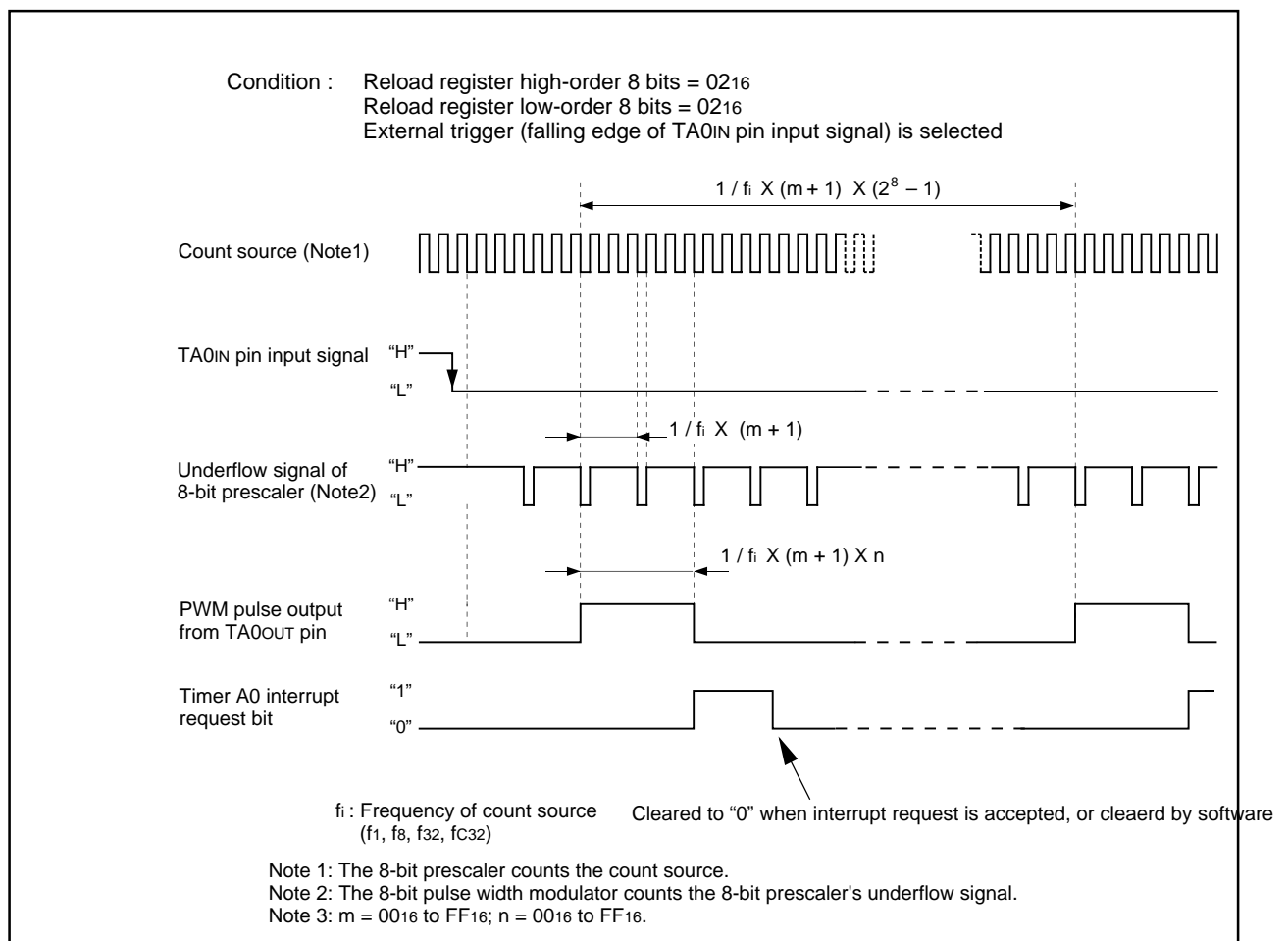


Figure 1.47. Example of how an 8-bit pulse width modulator operates

Timer B

Timer B

Figure 1.48 shows the block diagram of timer B. Figures 1.49 and 1.50 show the timer B-related registers. Use the timer Bi mode register (i = 0, 1) bits 0 and 1 to choose the desired mode.

Timer B has three operation modes listed as follows:

- Timer mode : The timer counts an internal count source.
- Event counter mode : The timer counts pulses from an external source or a timer overflow.
- Pulse period/pulse width measuring mode : The timer measures an external signal's pulse period or pulse width.

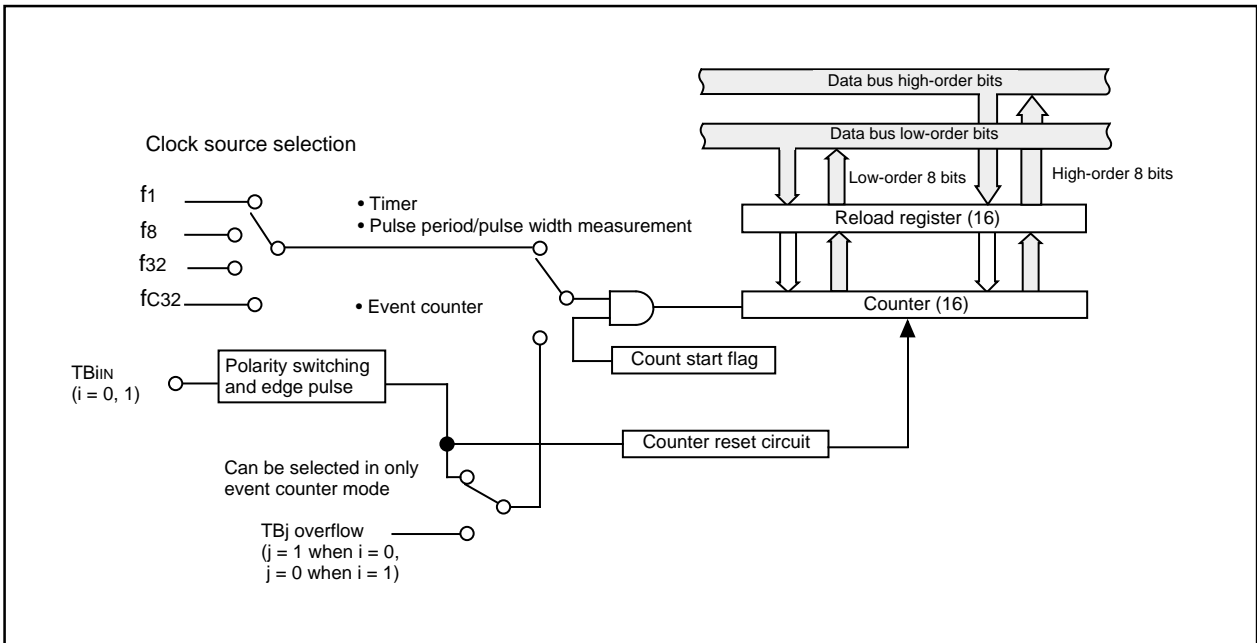


Figure 1.48. Block diagram of timer B

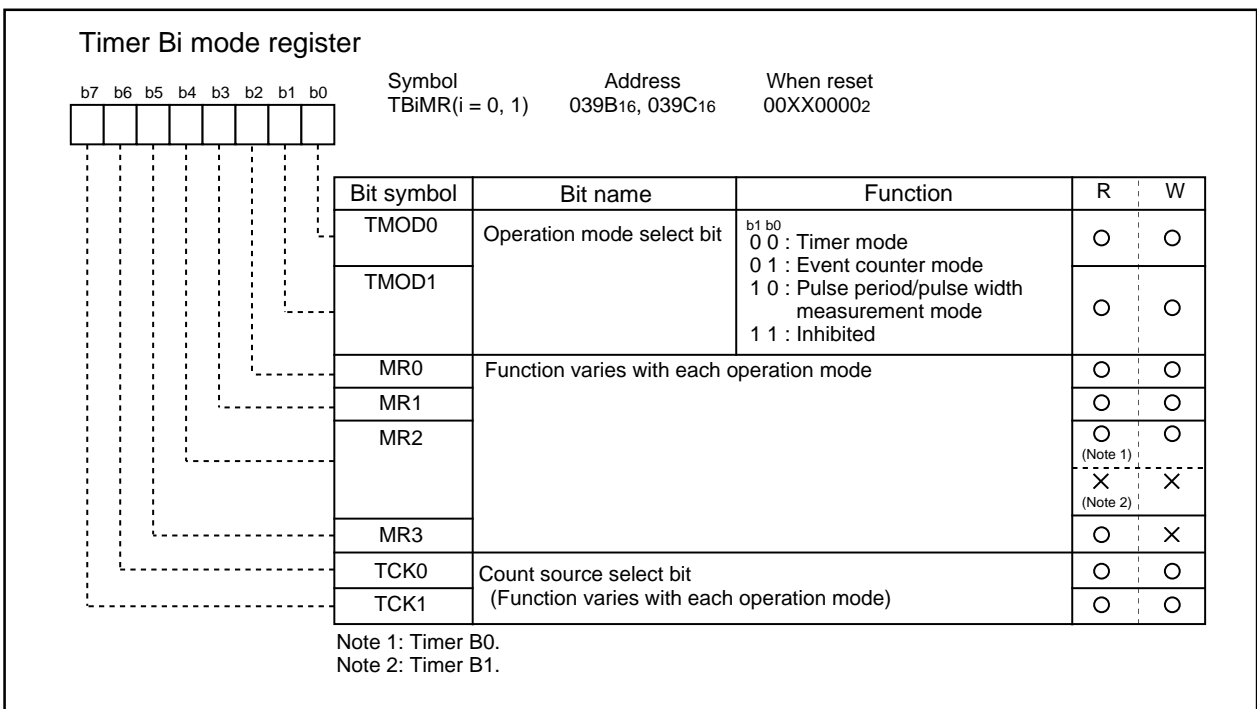


Figure 1.49. Timer B-related registers (1)

Timer B

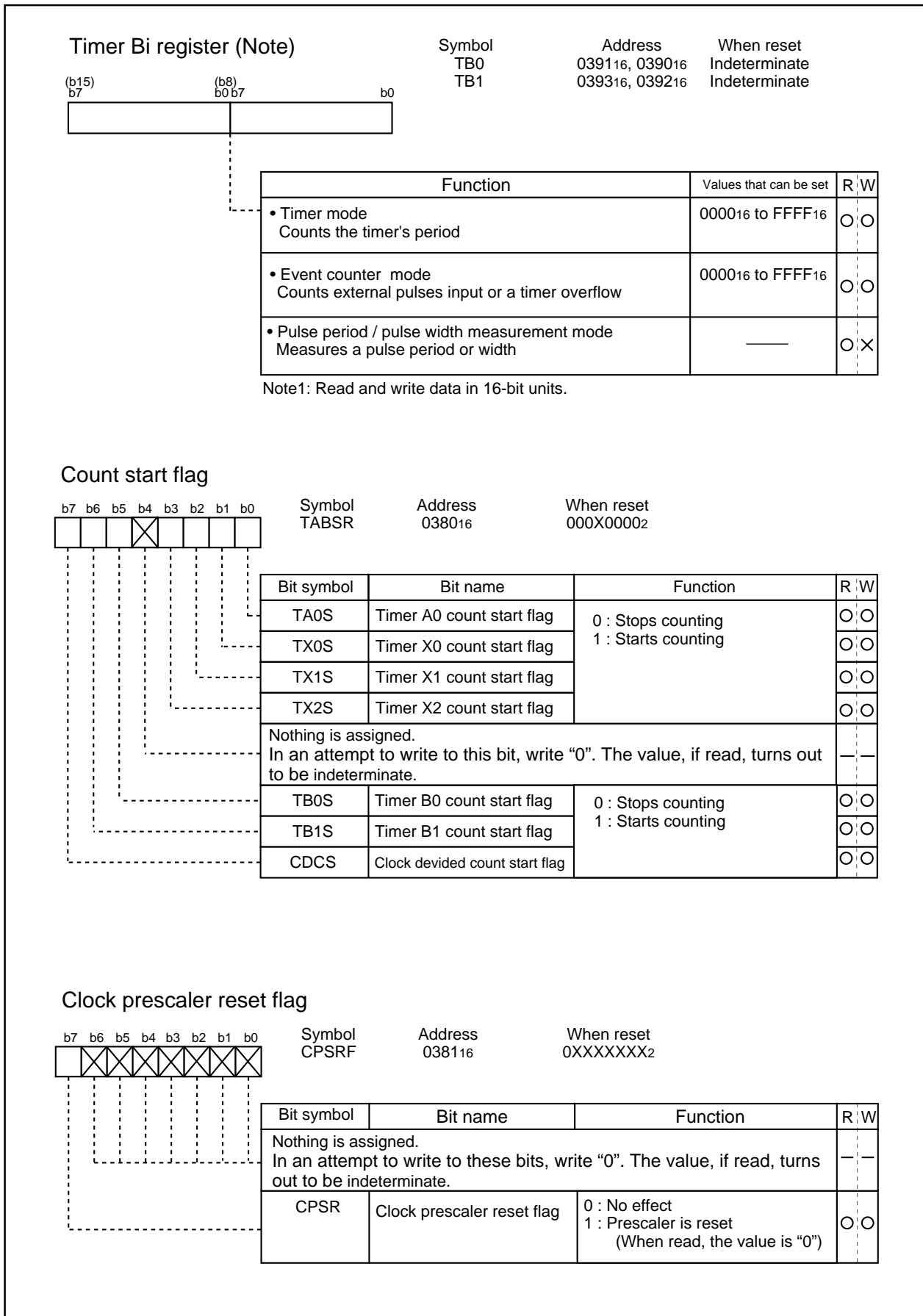


Figure 1.50. Timer B-related registers (2)

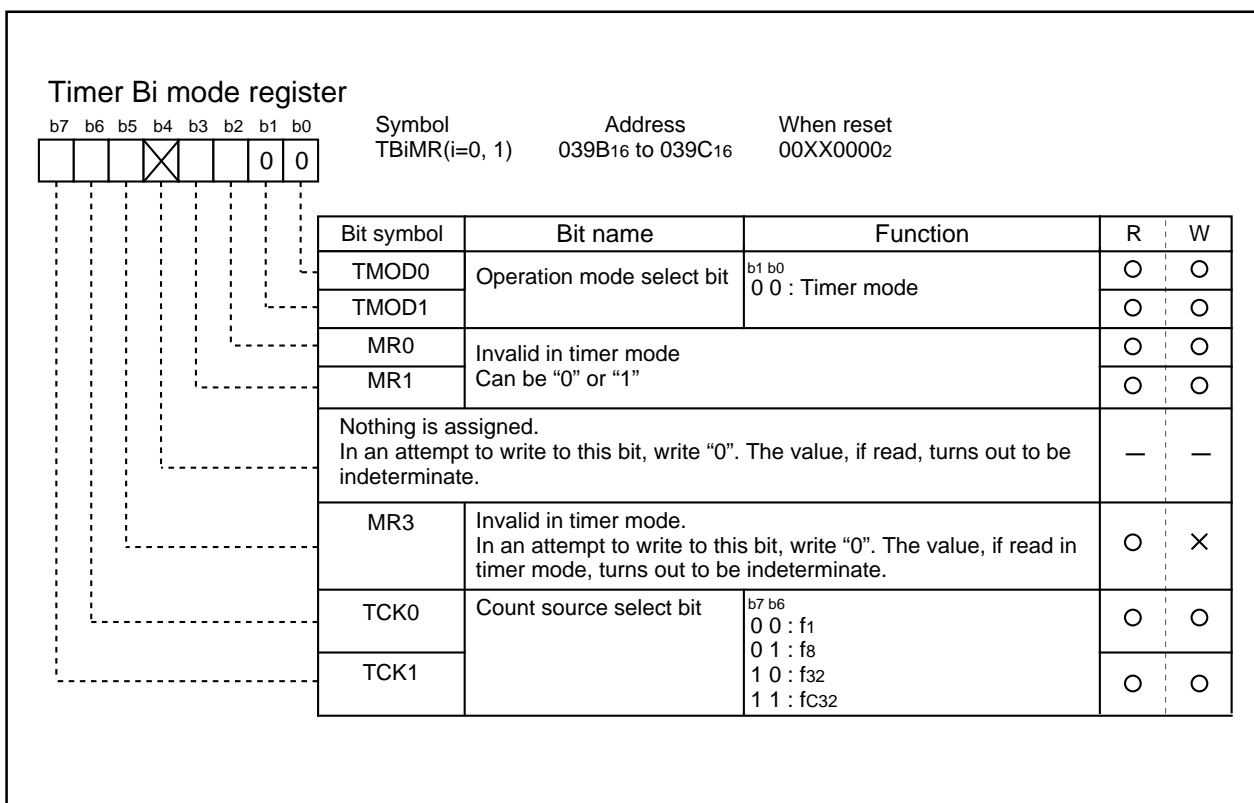
Timer B

(1) Timer mode

In this mode, the timer counts an internally generated count source. (See Table 1.17.) Figure 1.51 shows the timer Bi mode register in timer mode.

Table 1.17. Timer specifications in timer mode

Item	Specification
Count source	f1, f8, f32, fC32
Count operation	<ul style="list-style-type: none"> Counts down When the timer underflows, it reloads the reload register contents before continuing counting
Divide ratio	1/(n+1) n : Set value
Count start condition	Count start flag is set (= 1)
Count stop condition	Count start flag is reset (= 0)
Interrupt request generation timing	The timer underflows
TBiIN pin function	Programmable I/O port
Read from timer	Count value is read out by reading timer Bi register
Write to timer	<ul style="list-style-type: none"> When counting stopped When a value is written to timer Bi register, it is written to both reload register and counter When counting in progress When a value is written to timer Bi register, it is written to only reload register (Transferred to counter at next reload time)

**Figure 1.51. Timer Bi mode register in timer mode**

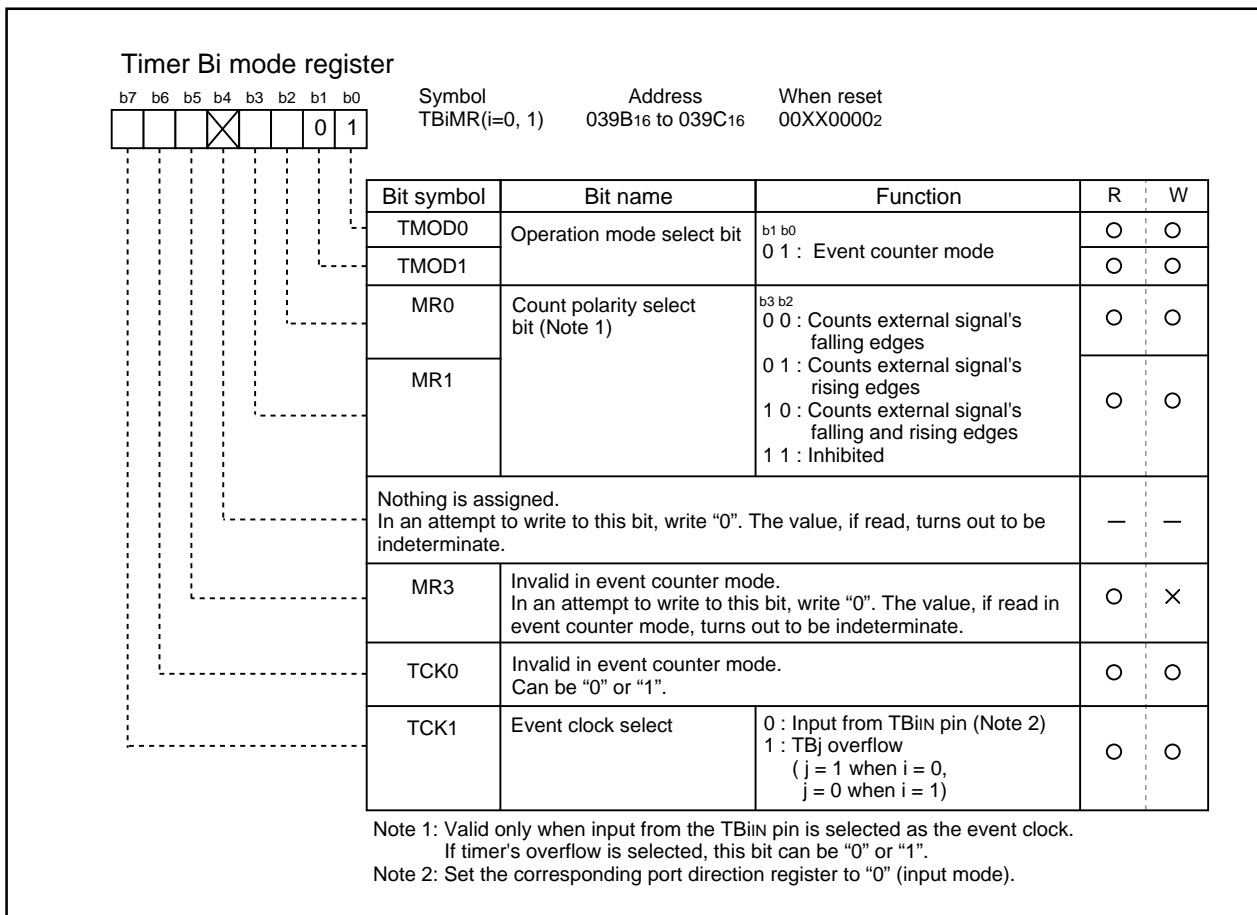
Timer B

(2) Event counter mode

In this mode, the timer counts an external signal or an internal timer's overflow. (See Table 1.18.) Figure 1.52 shows the timer Bi mode register in event counter mode.

Table 1.18. Timer specifications in event counter mode

Item	Specification
Count source	<ul style="list-style-type: none"> External signals input to TBIiN pin Effective edge of count source can be a rising edge, a falling edge, or falling and rising edges as selected by software
Count operation	<ul style="list-style-type: none"> Counts down When the timer underflows, it reloads the reload register contents before continuing counting
Divide ratio	$1/(n+1)$ n : Set value
Count start condition	Count start flag is set (= 1)
Count stop condition	Count start flag is reset (= 0)
Interrupt request generation timing	The timer underflows
TBIiN pin function	Count source input
Read from timer	Count value can be read out by reading timer Bi register
Write to timer	<ul style="list-style-type: none"> When counting stopped When a value is written to timer Bi register, it is written to both reload register and counter When counting in progress When a value is written to timer Bi register, it is written to only reload register (Transferred to counter at next reload time)

**Figure 1.52. Timer Bi mode register in event counter mode**

Timer B

(3) Pulse period/pulse width measurement mode

In this mode, the timer measures the pulse period or pulse width of an external signal. (See Table 1.19.)

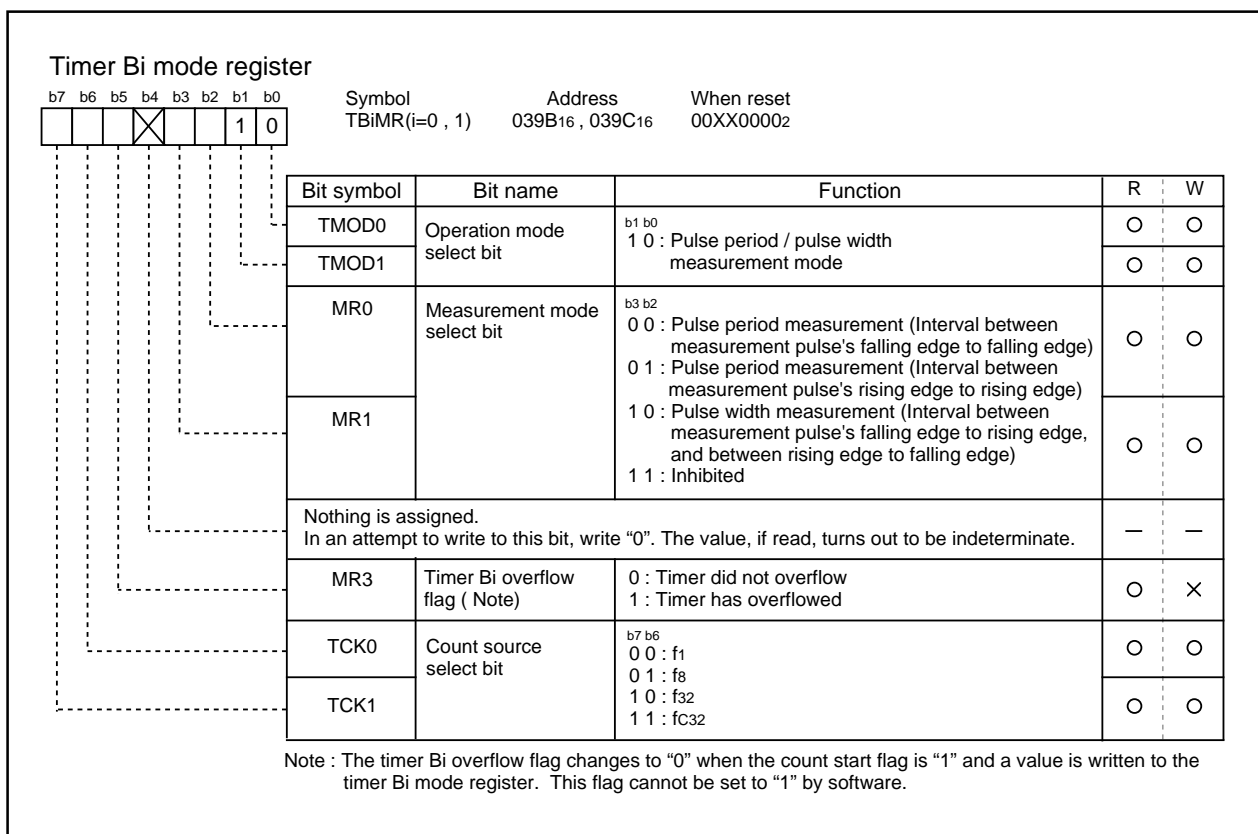
Figure 1.53 shows the timer Bi mode register in pulse period/pulse width measurement mode. Figure 1.54 shows the operation timing when measuring a pulse period. Figure 1.55 shows the operation timing when measuring a pulse width.

Table 1.19. Timer specifications in pulse period/pulse width measurement mode

Item	Specification
Count source	f1, f8, f32, fc32
Count operation	<ul style="list-style-type: none"> • Up count • Counter value "000016" is transferred to reload register at measurement pulse's effective edge and the timer continues counting
Count start condition	Count start flag is set (= 1)
Count stop condition	Count start flag is reset (= 0)
Interrupt request generation timing	<ul style="list-style-type: none"> • When measurement pulse's effective edge is input (Note 1) • When an overflow occurs. (Simultaneously, the timer Bi overflow flag changes to "1". The timer Bi overflow flag changes to "0" when the count start flag is "1" and a value is written to the timer Bi mode register.)
TBiIN pin function	Measurement pulse input
Read from timer	When timer Bi register is read, it indicates the reload register's content (measurement result) (Note 2)
Write to timer	Cannot be written to

Note 1: An interrupt request is not generated when the first effective edge is input after the timer has started counting.

Note 2: The value read out from the timer Bi register is indeterminate until the second effective edge is input after the timer.

**Figure 1.53. Timer Bi mode register in pulse period/pulse width measurement mode**

Timer B

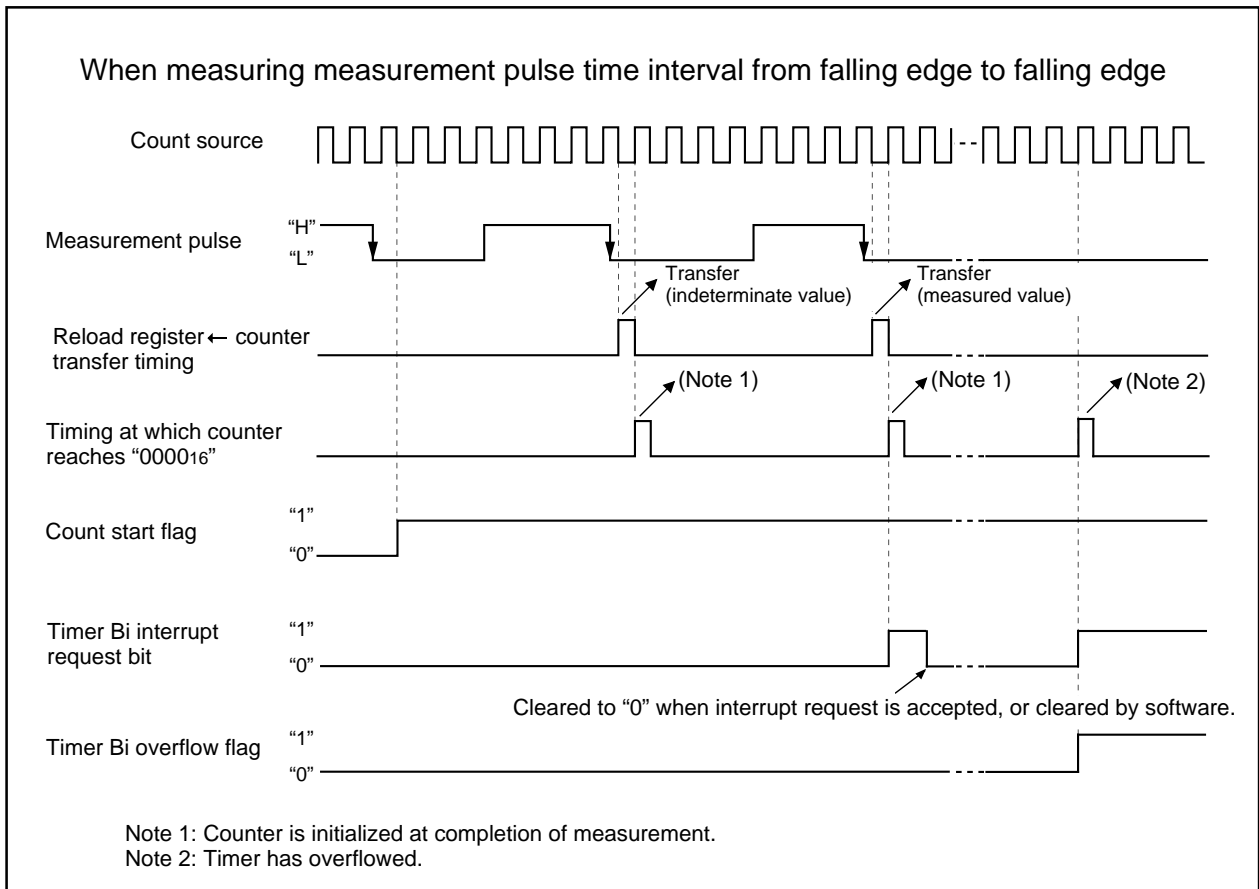


Figure 1.54. Operation timing when measuring a pulse period

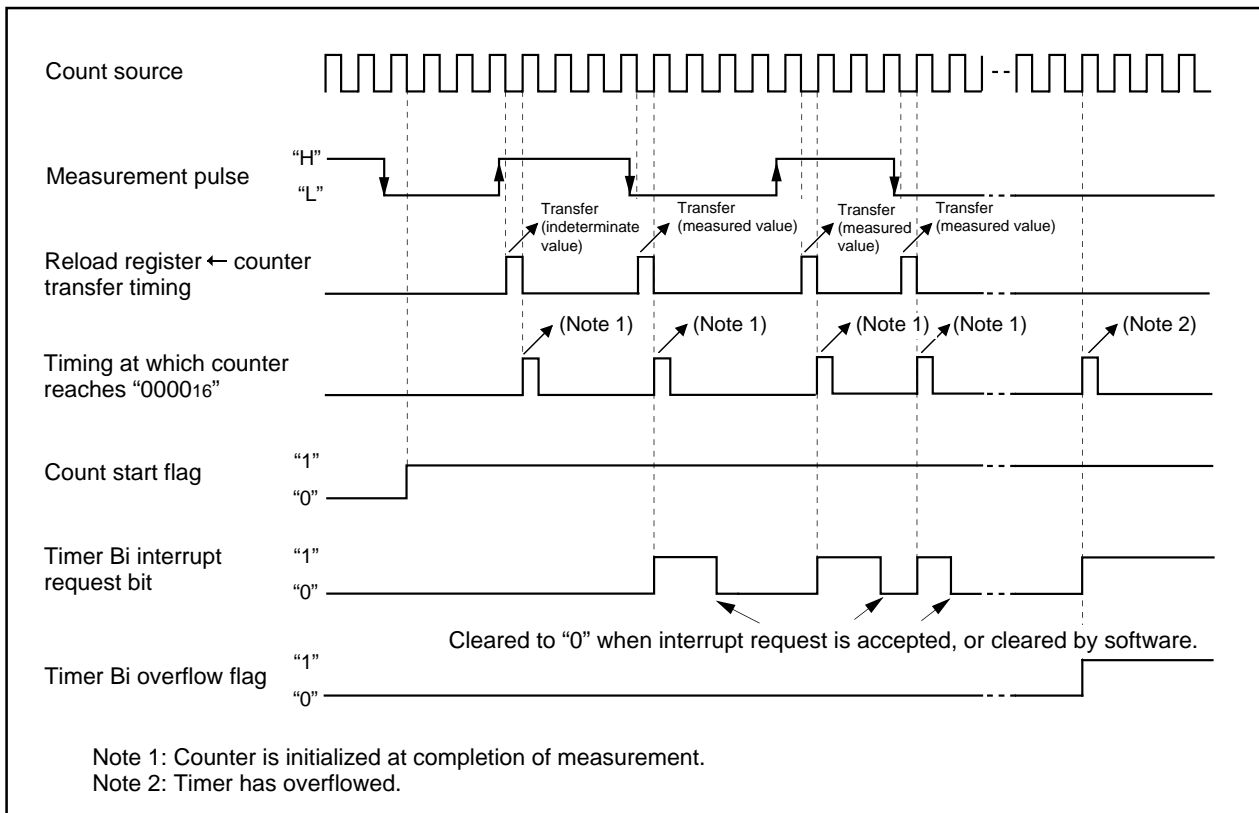


Figure 1.55. Operation timing when measuring a pulse width

Timer X

Timer X

Figure 1.56 shows the block diagram of timer X. Figures 1.57 to 1.59 show the timer X-related registers. Use the timer Xi mode register bits 0 and 1 to choose the desired mode.

Timer X has the five operation modes listed as follows:

- Timer mode : The timer counts an internal count source.
- Event counter mode : The timer counts pulses from an external source or a timer overflow.
- One-shot timer mode : The timer stops counting when the count reaches "0000₁₆".
- Pulse period/pulse width measuring mode : The timer measures an external signal's pulse period or pulse width.
- Pulse width modulation (PWM) mode : The timer outputs pulses of a given width.

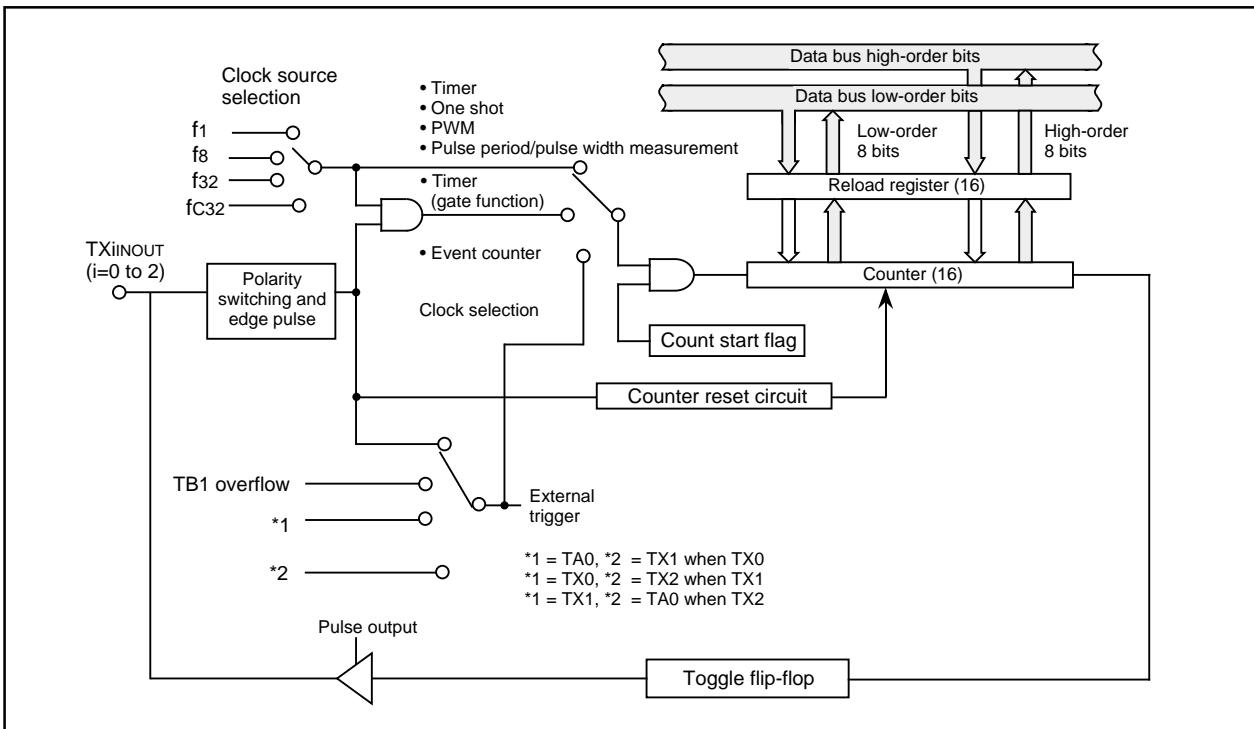


Figure 1.56. Block diagram of timer X

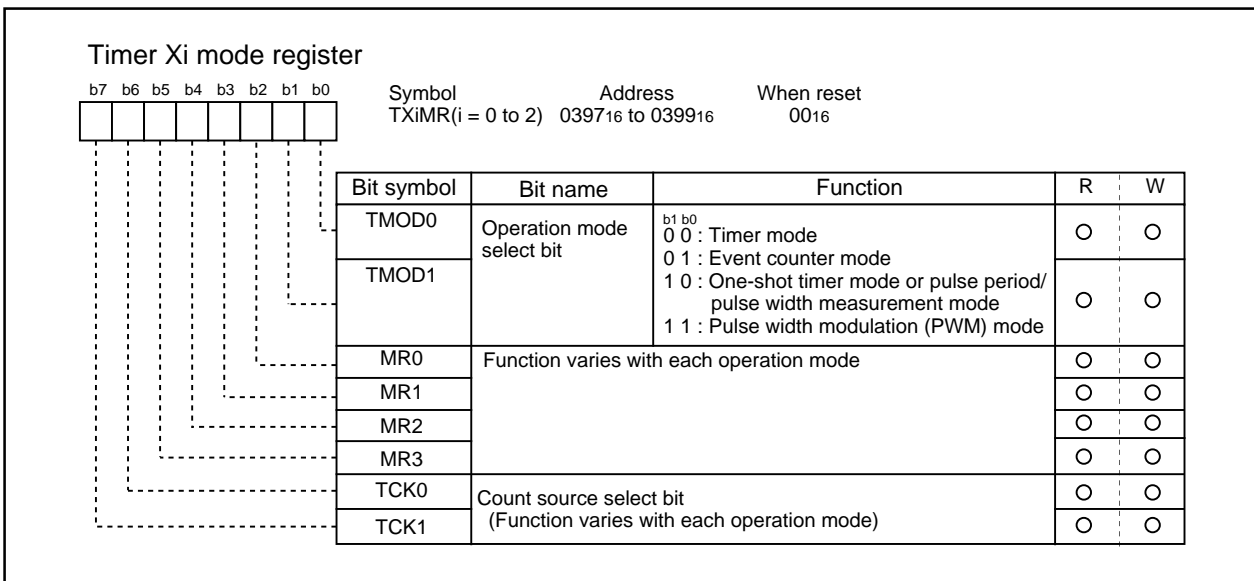


Figure 1.57. Timer X-related registers (1)

Timer X

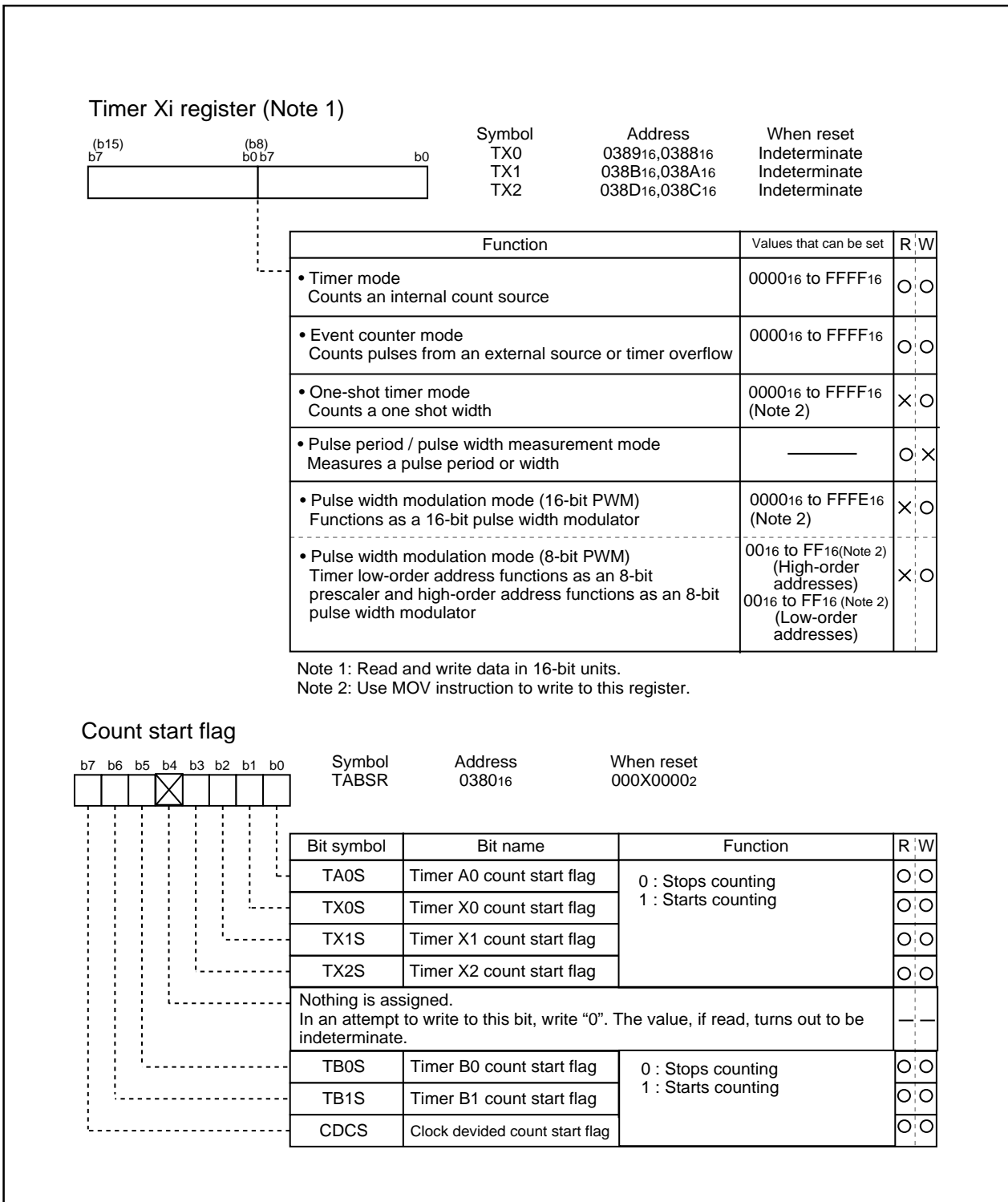


Figure 1.58. Timer X-related registers (2)

Timer X

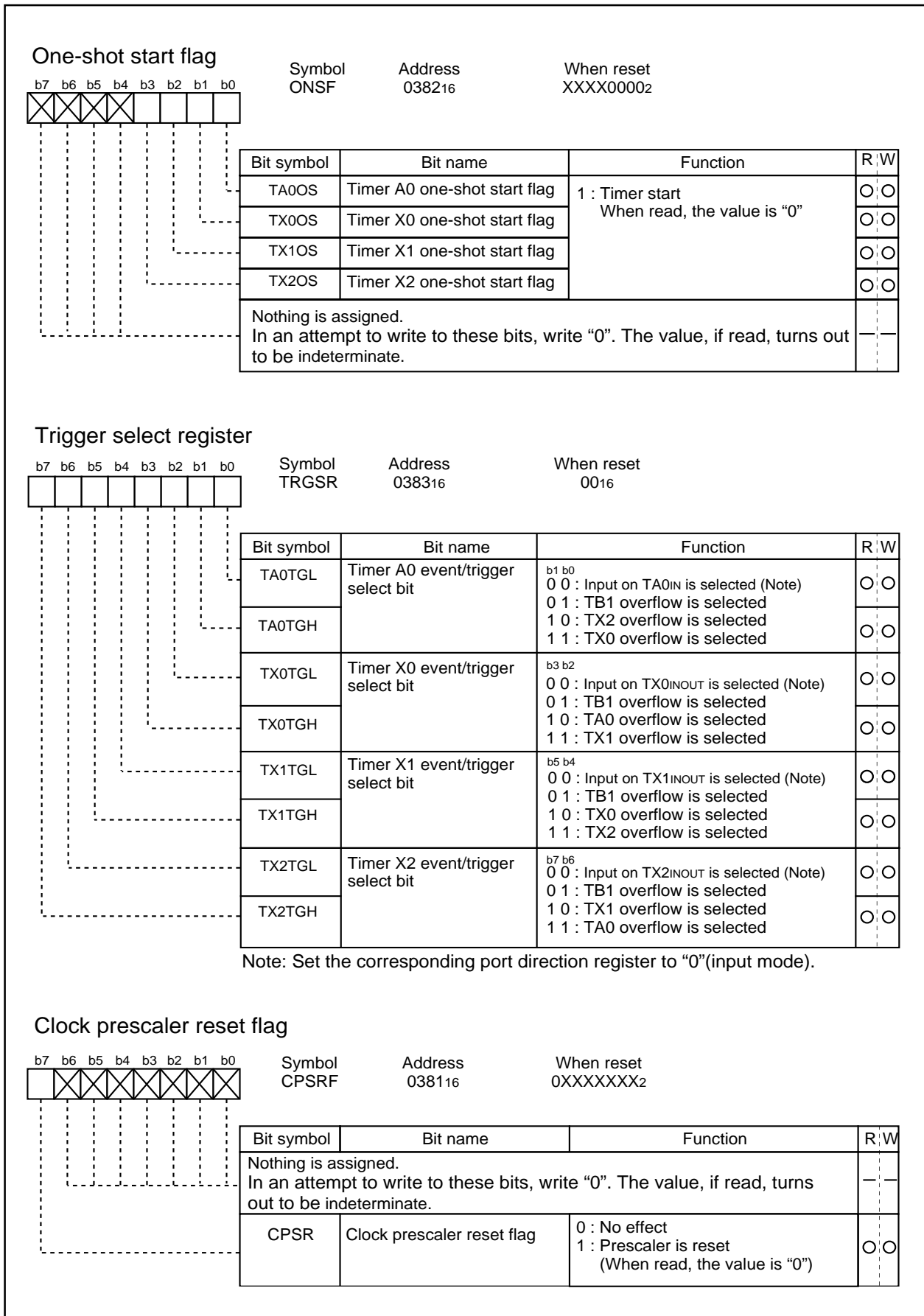


Figure 1.59. Timer X-related registers (3)

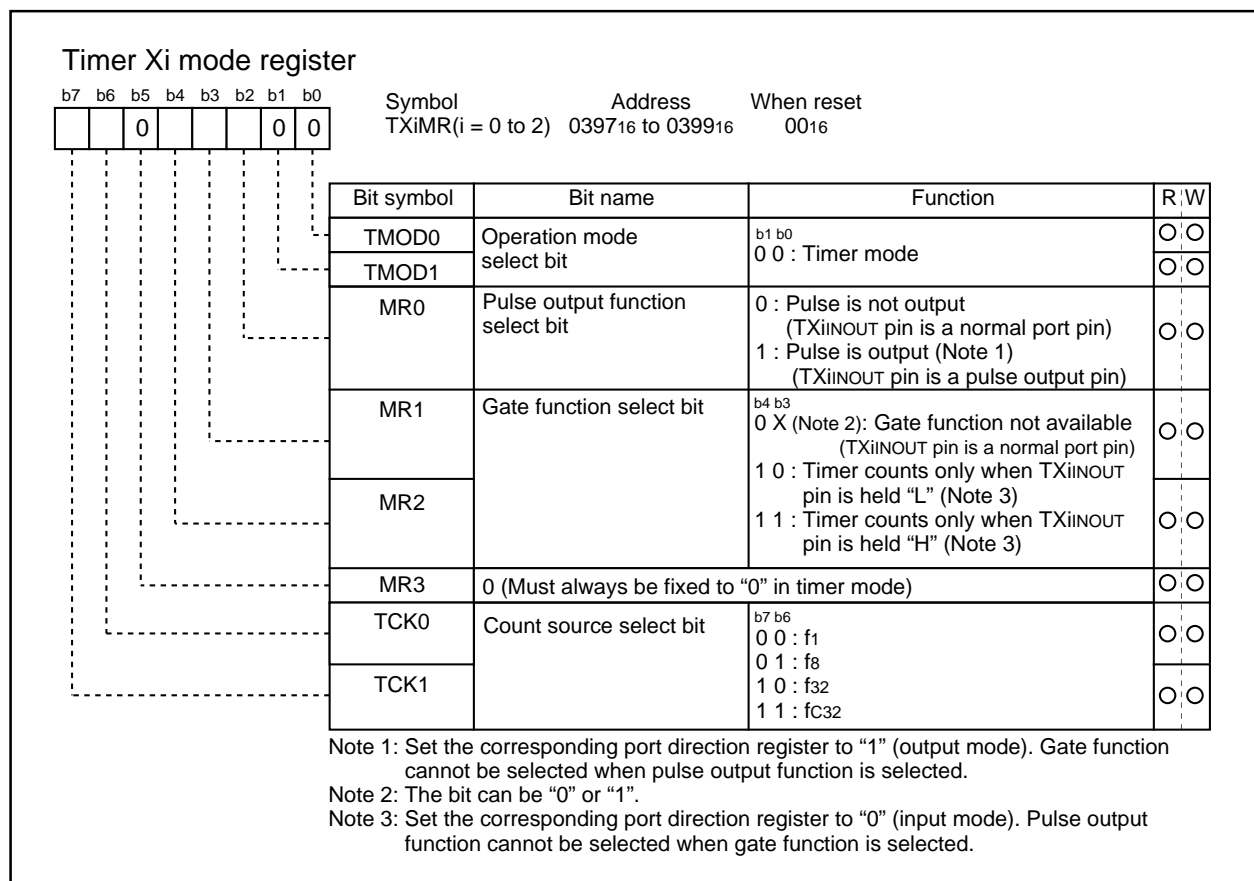
Timer X

(1) Timer mode

In this mode, the timer counts an internally generated count source. (See Table 1.20.) Figure 1.60 shows the timer Xi mode register in timer mode.

Table 1.20. Specifications of timer mode

Item	Specification
Count source	f1, f8, f32, fC32
Count operation	<ul style="list-style-type: none"> • Down count • When the timer underflows, it reloads the reload register contents before continuing counting
Divide ratio	1/(n+1) n : Set value
Count start condition	Count start flag is set (= 1)
Count stop condition	Count start flag is reset (= 0)
Interrupt request generation timing	When the timer underflows
TXiINOUT pin function	Programmable I/O port, gate input or pulse output
Read from timer	Count value can be read out by reading timer Xi register
Write to timer	<ul style="list-style-type: none"> • When counting stopped When a value is written to timer Xi register, it is written to both reload register and counter • When counting in progress When a value is written to timer Xi register, it is written to only reload register (Transferred to counter at next reload time)
Select function	<ul style="list-style-type: none"> • Gate function Counting can be started and stopped by the TXiINOUT pin's input signal • Pulse output function Each time the timer underflows, the TXiINOUT pin's polarity is reversed

**Figure 1.60. Timer Xi mode register in timer mode**

Timer X

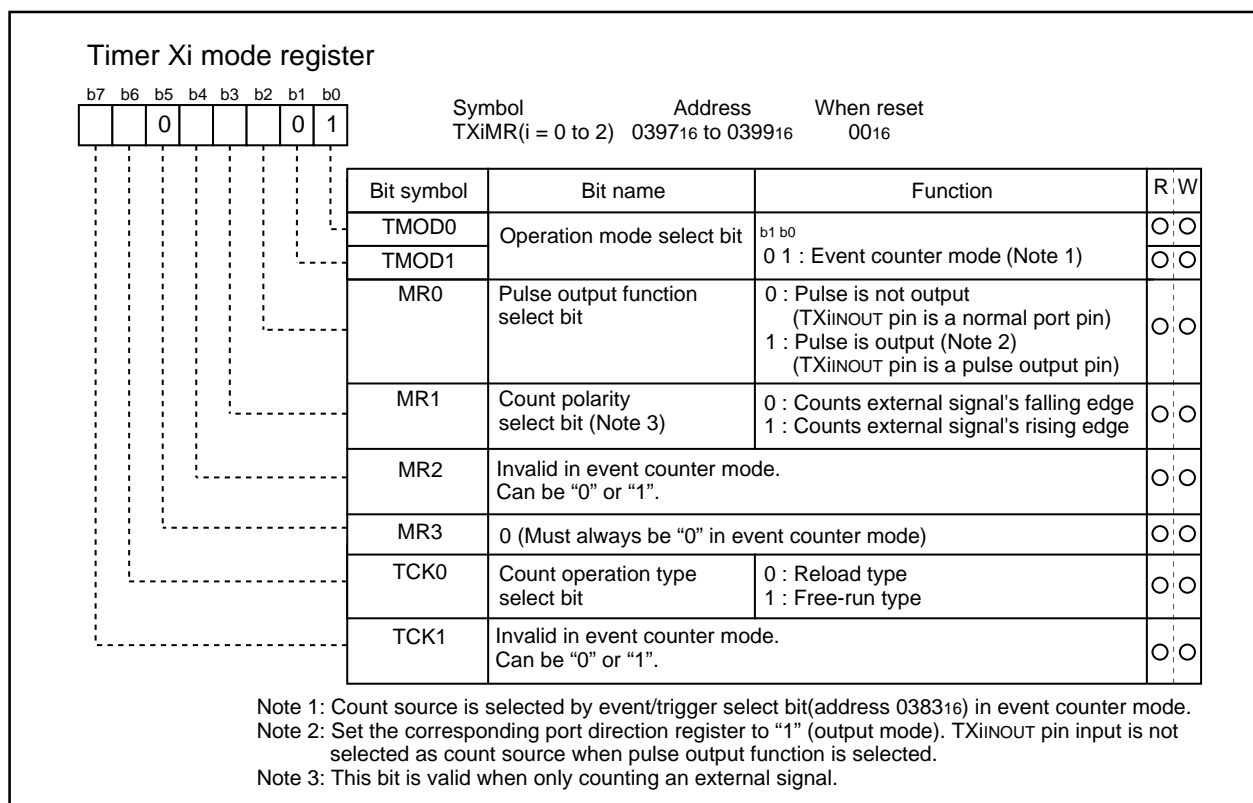
(2) Event counter mode

In this mode, the timer counts an external signal or an internal timer's overflow. (See Table 1.21.) Figure 1.61 shows the timer Xi mode register in event counter mode.

Table 1.21. Timer specifications in event counter mode (when not processing two-phase pulse signal)

Item	Specification
Count source	<ul style="list-style-type: none"> External signals input to TXiINOUT pin (effective edge can be selected by software) TB1 overflow, TA0 overflow, TXi overflow
Count operation	<ul style="list-style-type: none"> Down count When the timer underflows, it reloads the reload register contents before continuing counting (Note)
Divide ratio	$1/(n + 1)$ n : Set value
Count start condition	Count start flag is set (= 1)
Count stop condition	Count start flag is reset (= 0)
Interrupt request generation timing	The timer underflows
TXiINOUT pin function	Programmable I/O port, count source input or pulse output
Read from timer	Count value can be read out by reading timer Xi register
Write to timer	<ul style="list-style-type: none"> When counting stopped When a value is written to timer Xi register, it is written to both reload register and counter When counting in progress When a value is written to timer Xi register, it is written to only reload register (Transferred to counter at next reload time)
Select function	<ul style="list-style-type: none"> Free-run count function Even when the timer underflows, the reload register content is not reloaded to it Pulse output function Each time the timer underflows, the TXiINOUT pin's polarity is reversed

Note: This does not apply when the free-run function is selected.

**Figure 1.61. Timer Xi mode register in event counter mode**

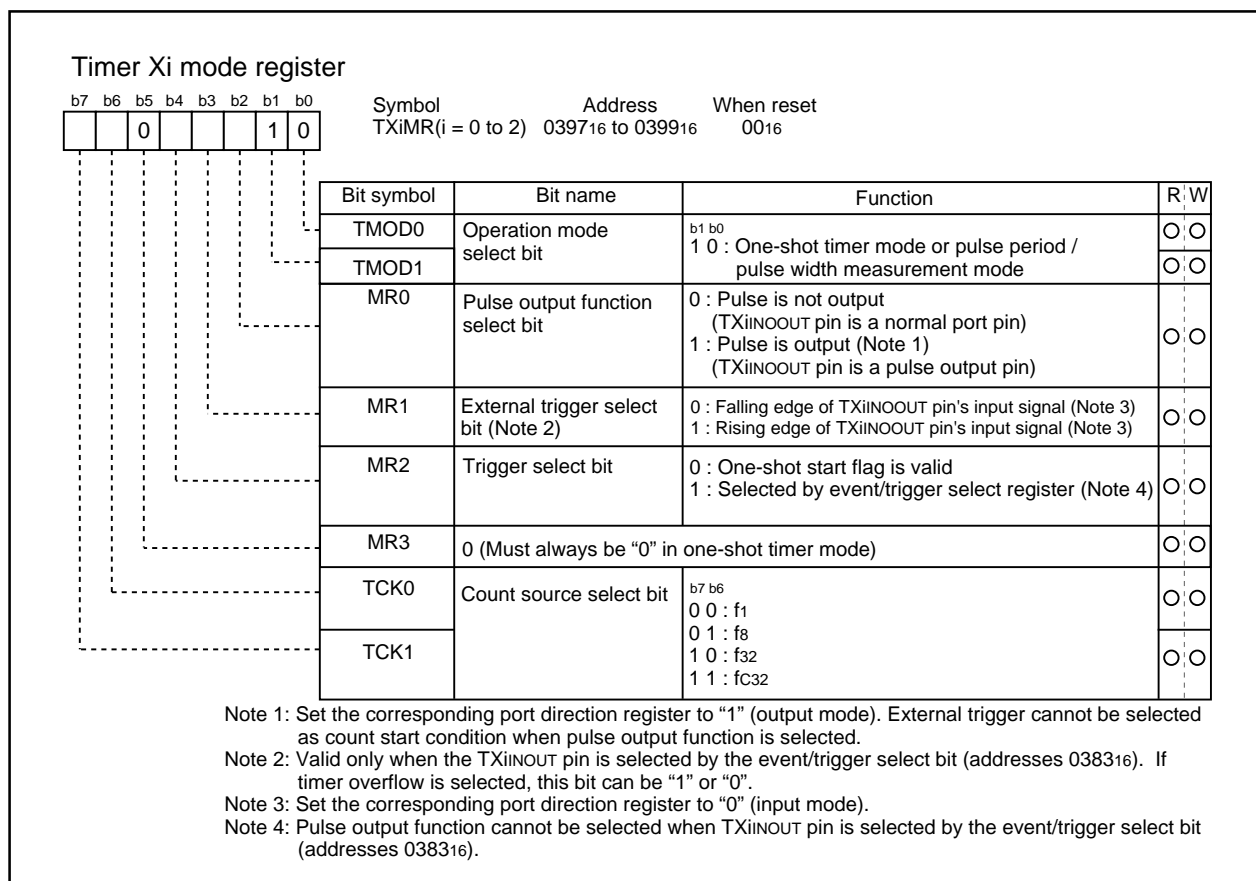
Timer X

(3) One-shot timer mode

In this mode, the timer operates only once. (See Table 1.22.) When a trigger occurs, the timer starts up and continues operating for a given period. Figure 1.62 shows the timer Xi mode register in one-shot timer mode.

Table 1.22. Timer specifications in one-shot timer mode

Item	Specification
Count source	f ₁ , f ₈ , f ₃₂ , f _{C32}
Count operation	<ul style="list-style-type: none"> The timer counts down When the count reaches 0000₁₆, the timer stops counting after reloading a new count If a trigger occurs when counting, the timer reloads a new count and restarts counting
Divide ratio	1/n n : Set value
Count start condition	<ul style="list-style-type: none"> An external trigger is input The timer overflows The one-shot start flag is set (= 1)
Count stop condition	<ul style="list-style-type: none"> A new count is reloaded after the count has reached 0000₁₆ The count start flag is reset (= 0)
Interrupt request generation timing	The count reaches 0000 ₁₆
TXiINOUT pin function	Programmable I/O port, trigger input or pulse output
Read from timer	When timer Xi register is read, it indicates an indeterminate value
Write to timer	<ul style="list-style-type: none"> When counting stopped When a value is written to timer Xi register, it is written to both reload register and counter When counting in progress When a value is written to timer Xi register, it is written to only reload register (Transferred to counter at next reload time)

**Figure 1.62. Timer Xi mode register in one-shot timer mode**

Timer X

(4) Pulse period/pulse width measurement mode

In this mode, the timer measures the pulse period or pulse width of an external signal. (See Table 1.23.)

Figure 1.63 shows the timer Xi mode register in pulse period/pulse width measurement mode. Figure

1.64 shows the operation timing when measuring a pulse period. Figure 1.65 shows the operation timing

when measuring a pulse width.

Table 1.23. Timer specifications in pulse period/pulse width measurement mode

Item	Specification
Count source	f1, f8, f32, fc32
Count operation	<ul style="list-style-type: none"> • Up count • Counter value "000016" is transferred to reload register at measurement pulse's effective edge and the timer continues counting
Count start condition	Count start flag is set (= 1)
Count stop condition	Count start flag is reset (= 0)
Interrupt request generation timing	<ul style="list-style-type: none"> • When measurement pulse's effective edge is input (Note 1) • When an overflow occurs. (Simultaneously, the timer Xi overflow flag changes to "1". The timer Xi overflow flag changes to "0" when the count start flag is "1" and a value is written to the timer Xi mode register.)
TXiINOUT pin function	Measurement pulse input
Read from timer	When timer Xi register is read, it indicates the reload register's content (measurement result) (Note 2)
Write to timer	Cannot be written to

Note 1: An interrupt request is not generated when the first effective edge is input after the timer has started counting.

Note 2: The value read out from the timer Xi register is indeterminate until the second effective edge is input after the timer.

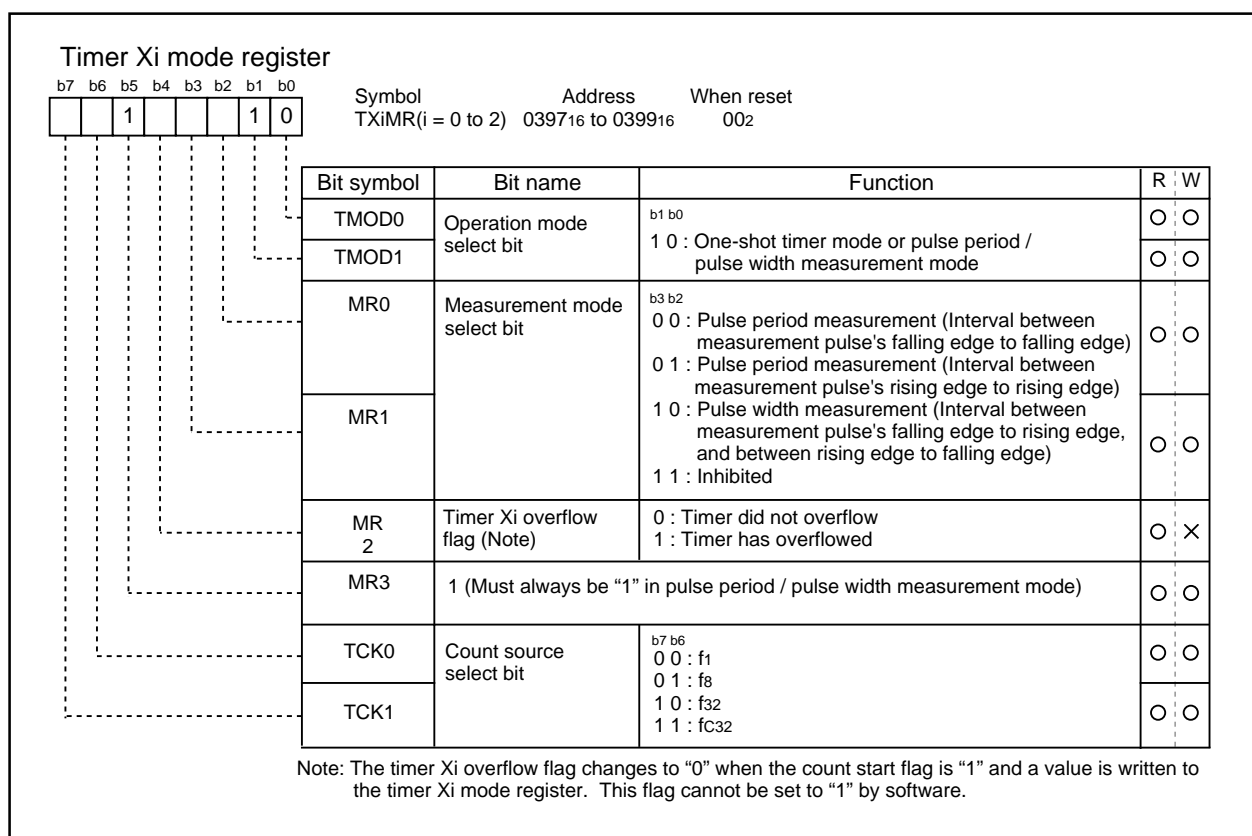


Figure 1.63. Timer Xi mode register in pulse period/pulse width measurement mode

Timer X

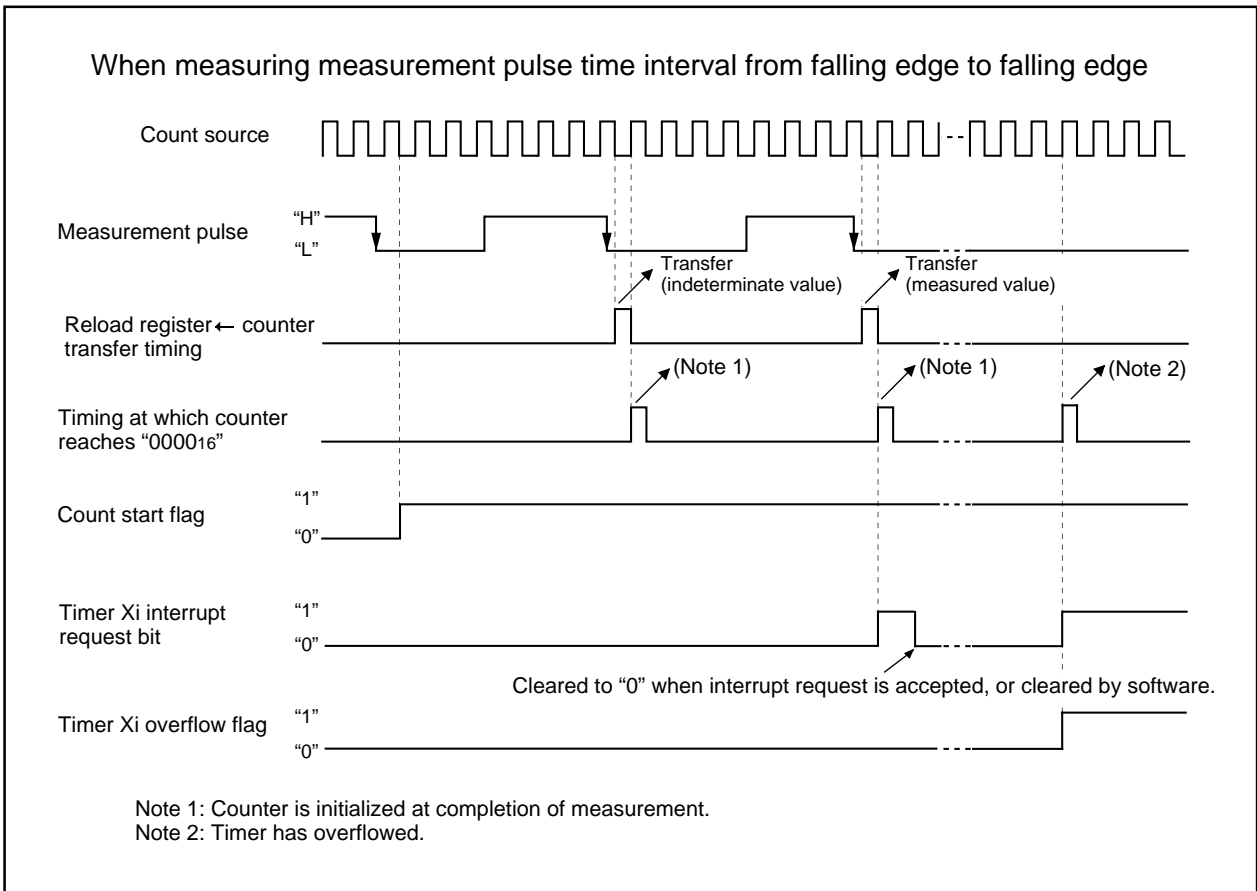


Figure 1.64. Operation timing when measuring a pulse period

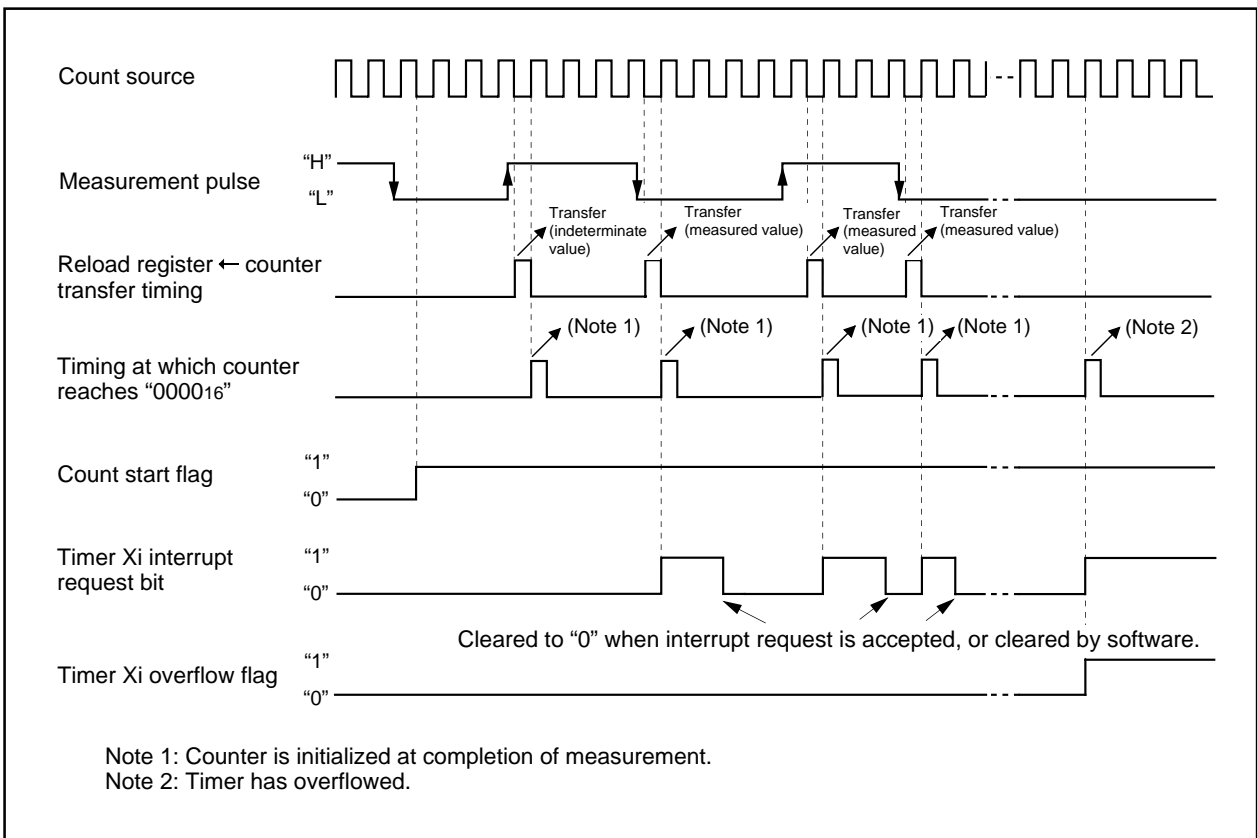


Figure 1.65. Operation timing when measuring a pulse width

Timer X

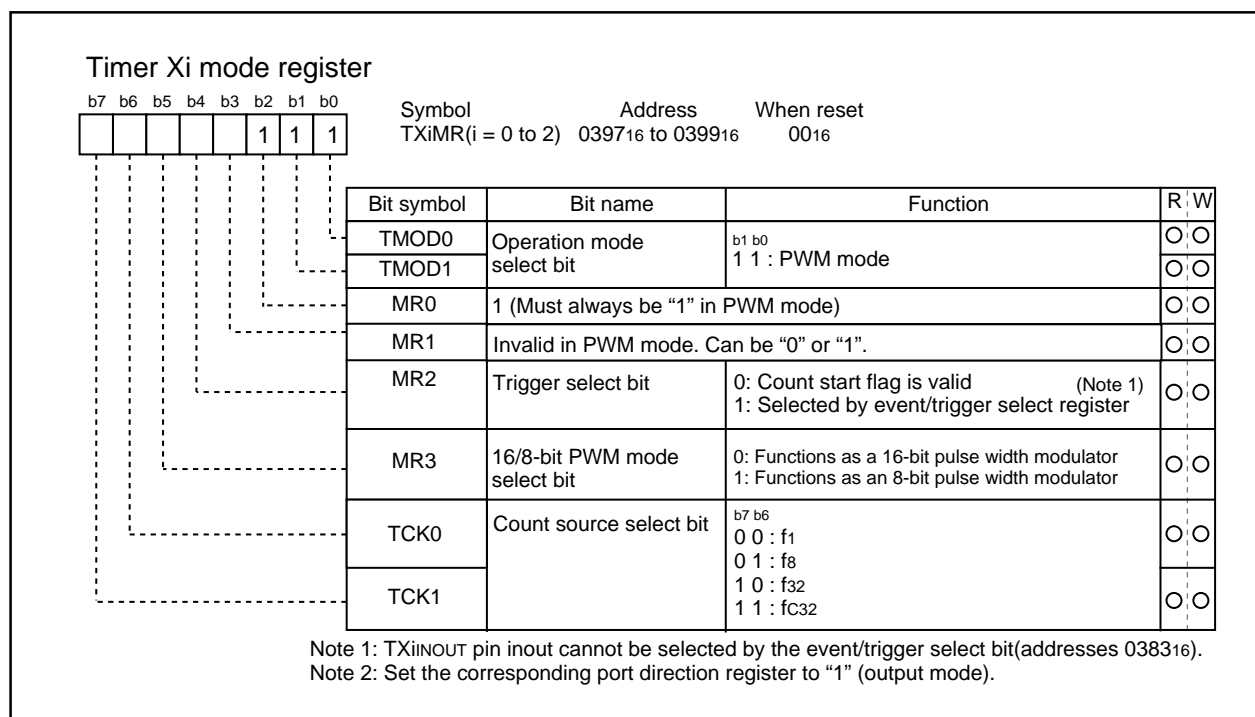
(5) Pulse width modulation (PWM) mode

In this mode, the timer outputs pulses of a given width in succession. (See Table 1.24.) In this mode, the counter functions as either a 16-bit pulse width modulator or an 8-bit pulse width modulator. Figure 1.66 shows the timer Xi mode register in pulse width modulation mode. Figure 1.67 shows the example of how a 16-bit pulse width modulator operates. Figure 1.68 shows the example of how an 8-bit pulse width modulator operates.

Table 1.24. Timer specifications in pulse width modulation mode

Item		Specification
Count source		f1, f8, f32, fc32
Count operation		<ul style="list-style-type: none"> Down counts (operating as an 8-bit or a 16-bit pulse width modulator) The timer reloads a new count at a rising edge of PWM pulse and continues counting The timer is not affected by a trigger that occurs when counting
16-bit PWM		<ul style="list-style-type: none"> "H" level width n / f_i n : Set value Cycle time $(2^{16}-1) / f_i$ fixed
8-bit PWM		<ul style="list-style-type: none"> "H" level width $n \times (m+1) / f_i$ n: values set to timer Xi register's high-order address Cycle time $(2^8-1) \times (m+1) / f_i$ m : values set to timer Xi register's low-order address
Count start condition		<ul style="list-style-type: none"> The timer overflows The count start flag is set (= 1)
Count stop condition		<ul style="list-style-type: none"> The count start flag is reset (= 0)
Interrupt request generation timing	8 bits PWM	<ul style="list-style-type: none"> Set value of "H" level width is except FF₁₆, 00₁₆ : PWM pulse goes "L" Set value of "H" level width is FF₁₆, 00₁₆ : Timing that count value goes to 01₁₆
	16 bits PWM	<ul style="list-style-type: none"> Set value of "H" level width is except FFFF₁₆, 0000₁₆ : PWM pulse goes "L" Set value of "H" level width is FFFF₁₆, 0000₁₆ : Timing that count value goes to 0001₁₆
TXiINOUT pin function		Pulse output
Read from timer		When timer Xi register is read, it indicates an indeterminate value
Write to timer		<ul style="list-style-type: none"> When counting stopped When a value is written to timer Xi register, it is written to both reload register and counter When counting in progress When a value is written to timer Xi register, it is written to only reload register (Transferred to counter at next reload time)

Note: When set value of "H" level width is 00₁₆ or 0000₁₆, pulse outputs "L" level and inversion value, FF₁₆ or FFFF₁₆ is set to timer.

**Figure 1.66. Timer Xi mode register in pulse width modulation mode**

Timer X

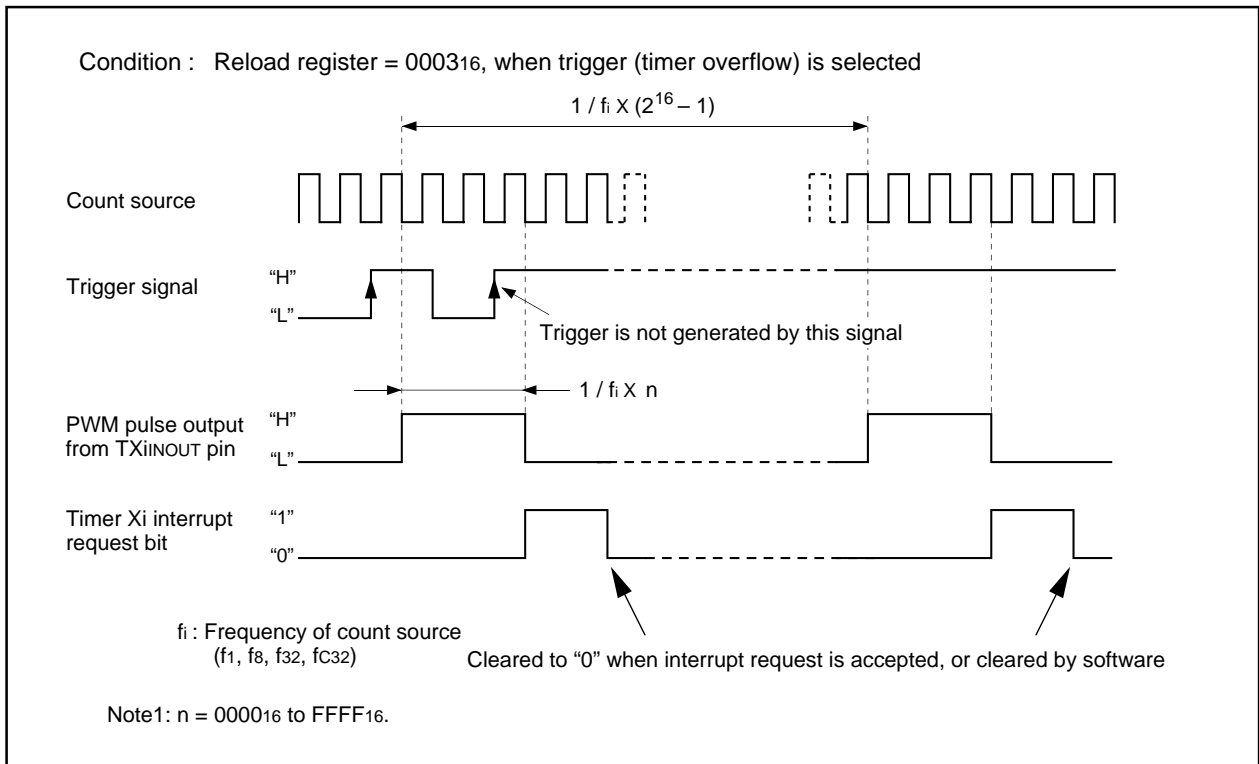


Figure 1.67. Example of how a 16-bit pulse width modulator operates

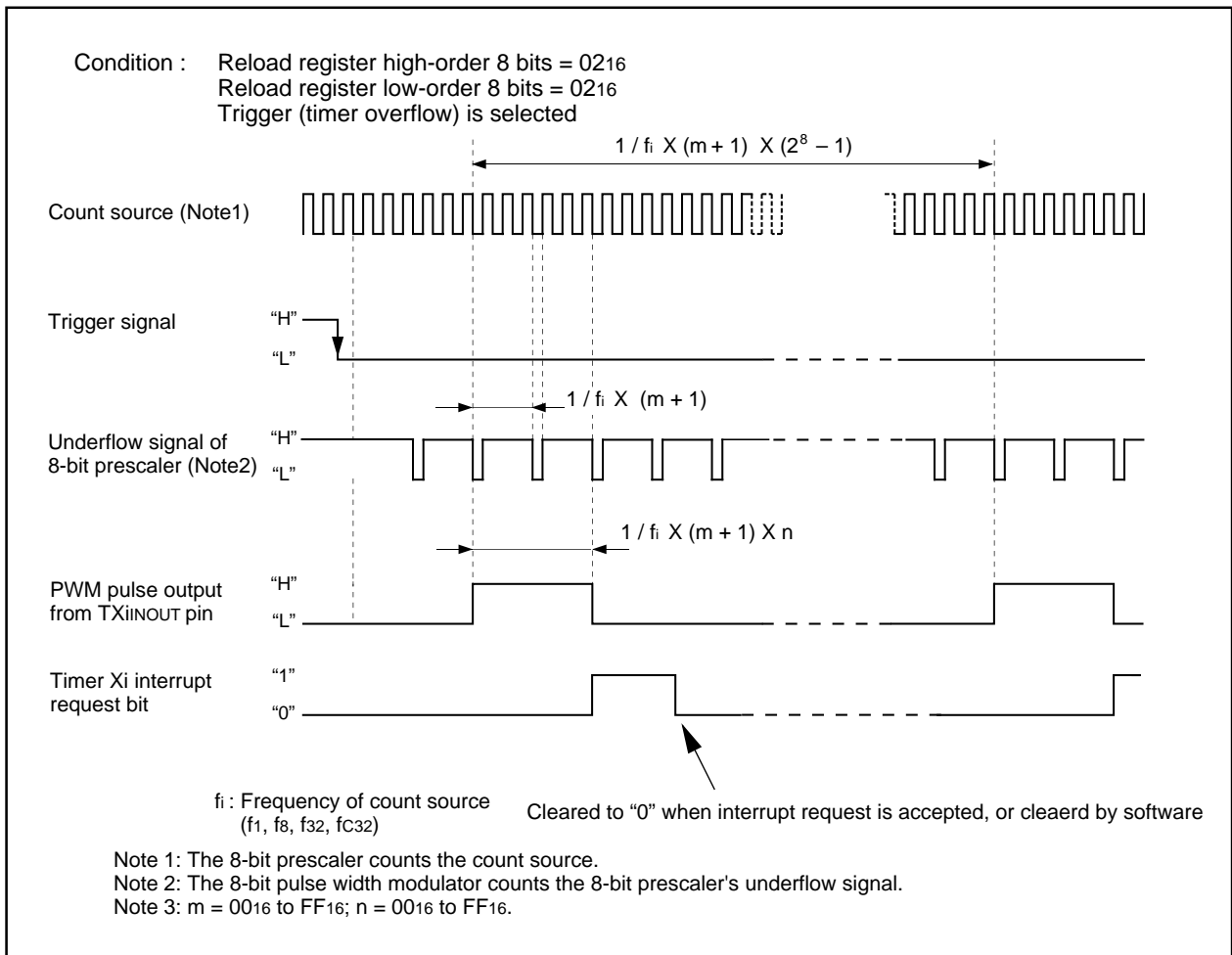


Figure 1.68. Example of how an 8-bit pulse width modulator operates

Serial I/O

Serial I/O

Serial I/O is configured as two channels: UART0 and UART1.

UART0 and UART1 each have an exclusive timer to generate a transfer clock, so they operate independently of each other.

Figure 1.69 shows the block diagram of UART0 and UART1. Figure 1.70 shows the block diagram of the transmit/receive unit.

UART0 has two operation modes: a clock synchronous serial I/O mode and a clock asynchronous serial I/O mode (UART mode). The contents of the serial I/O mode select bits (bits 0 to 2 at addresses 03A016 and 03A816) determine whether UART0 is used as a clock synchronous serial I/O or as a UART.

UART1 is used as a UART only.

Figures 1.71 through 1.73 show the registers related to UARTi.

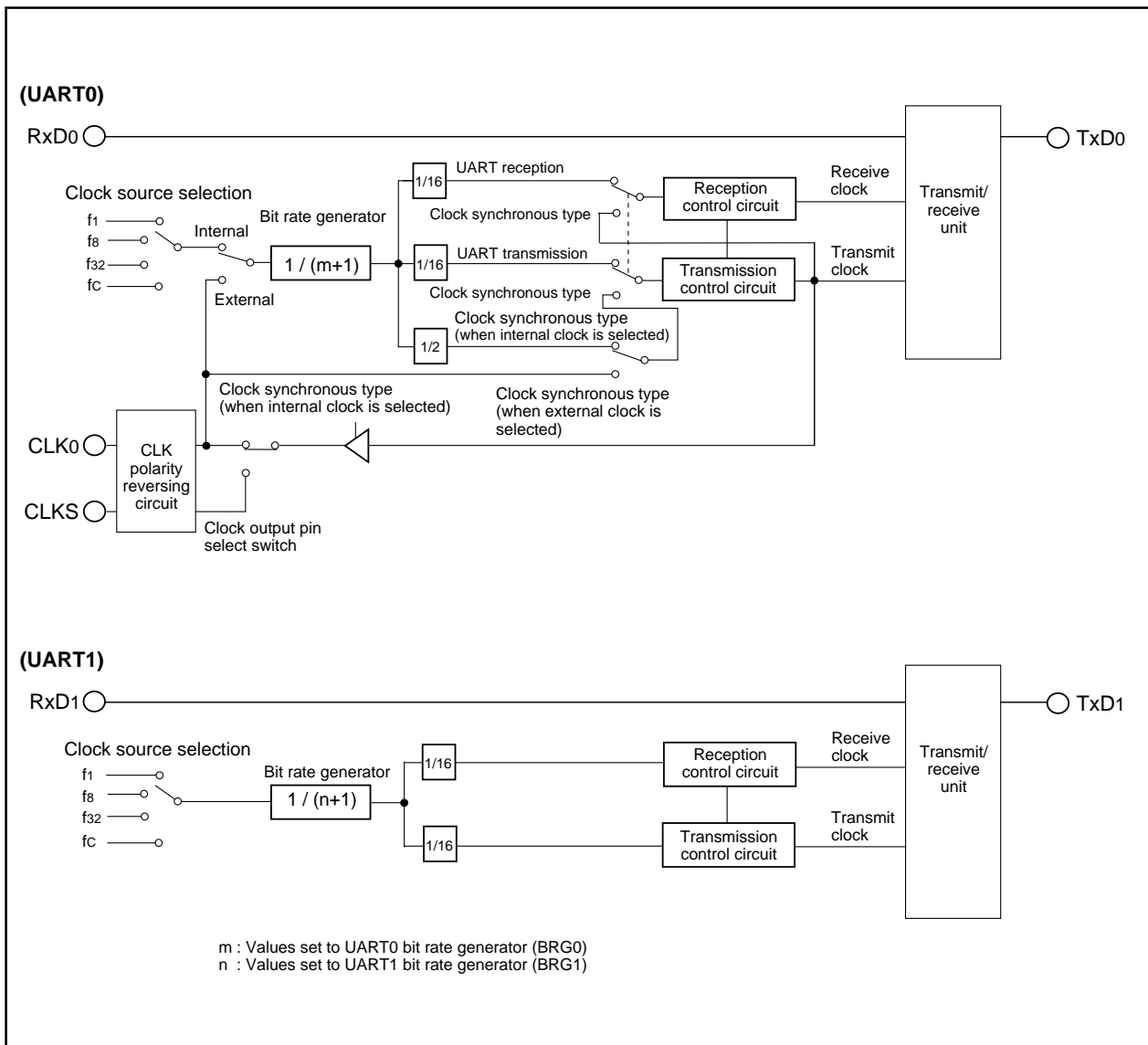


Figure 1.69. Block diagram of UARTi (i = 0, 1)

Serial I/O

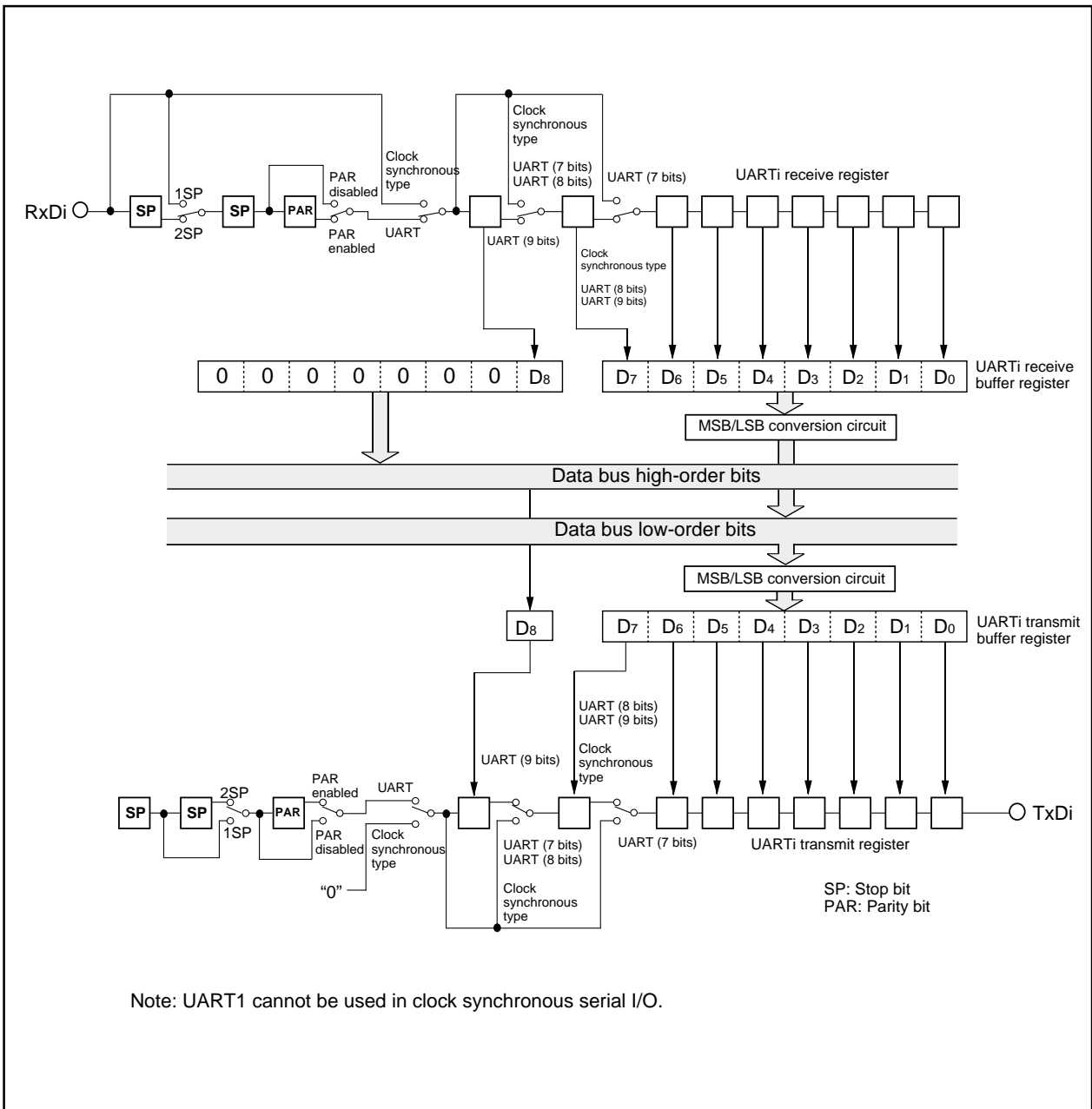


Figure 1.70. Block diagram of transmit/receive unit

Serial I/O

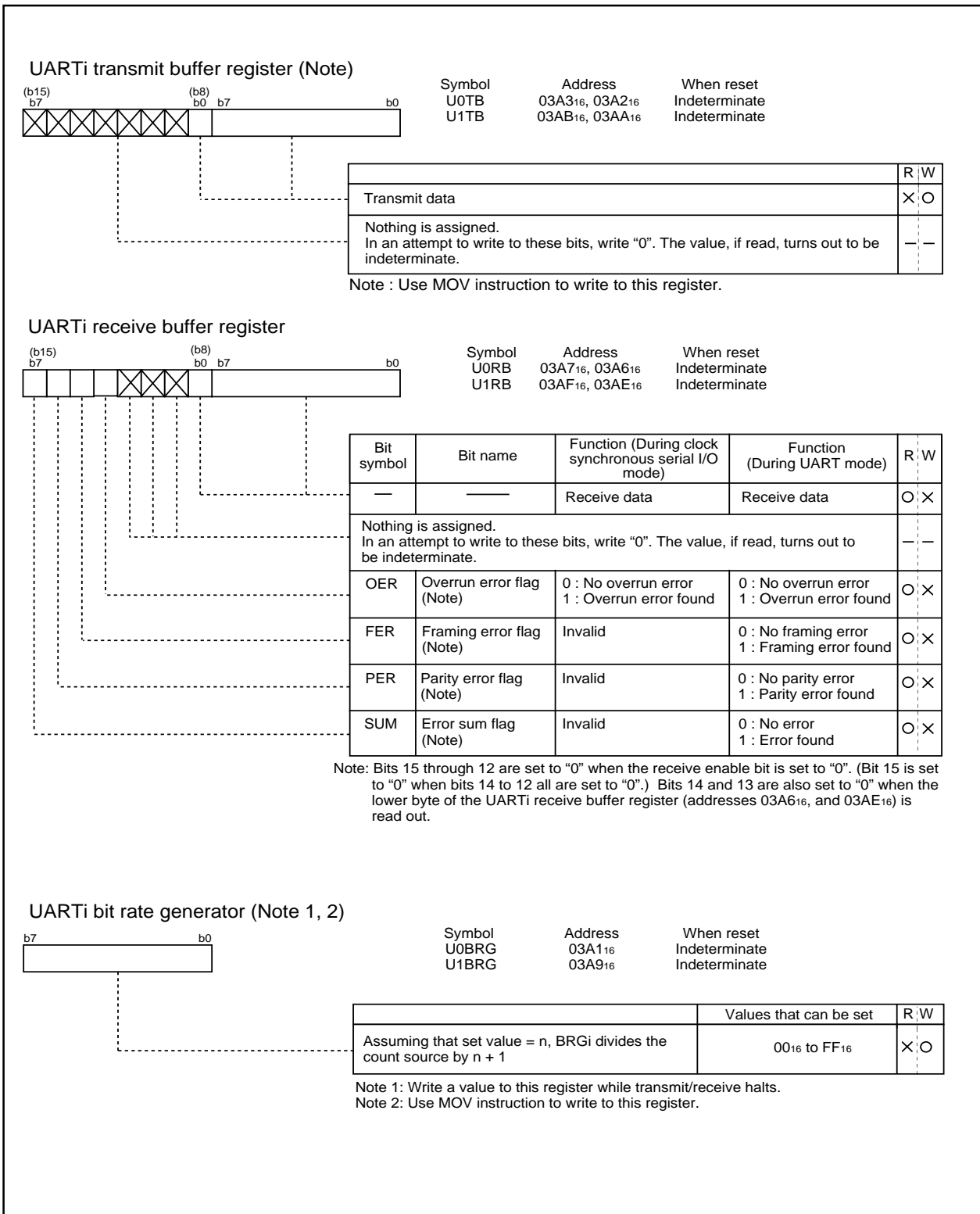


Figure 1.71. Serial I/O-related registers (1)

Serial I/O

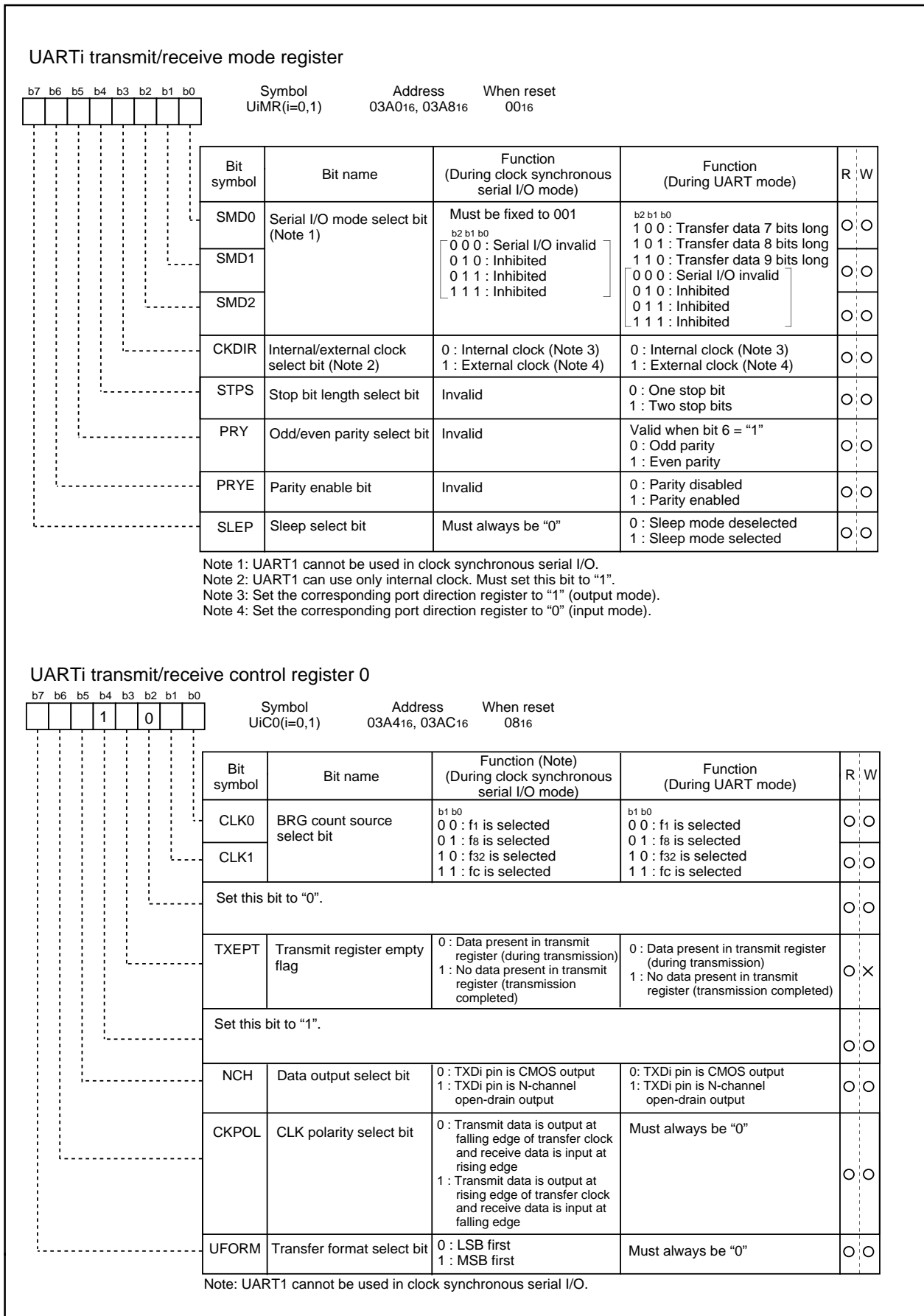


Figure 1.72. Serial I/O-related registers (2)

Serial I/O

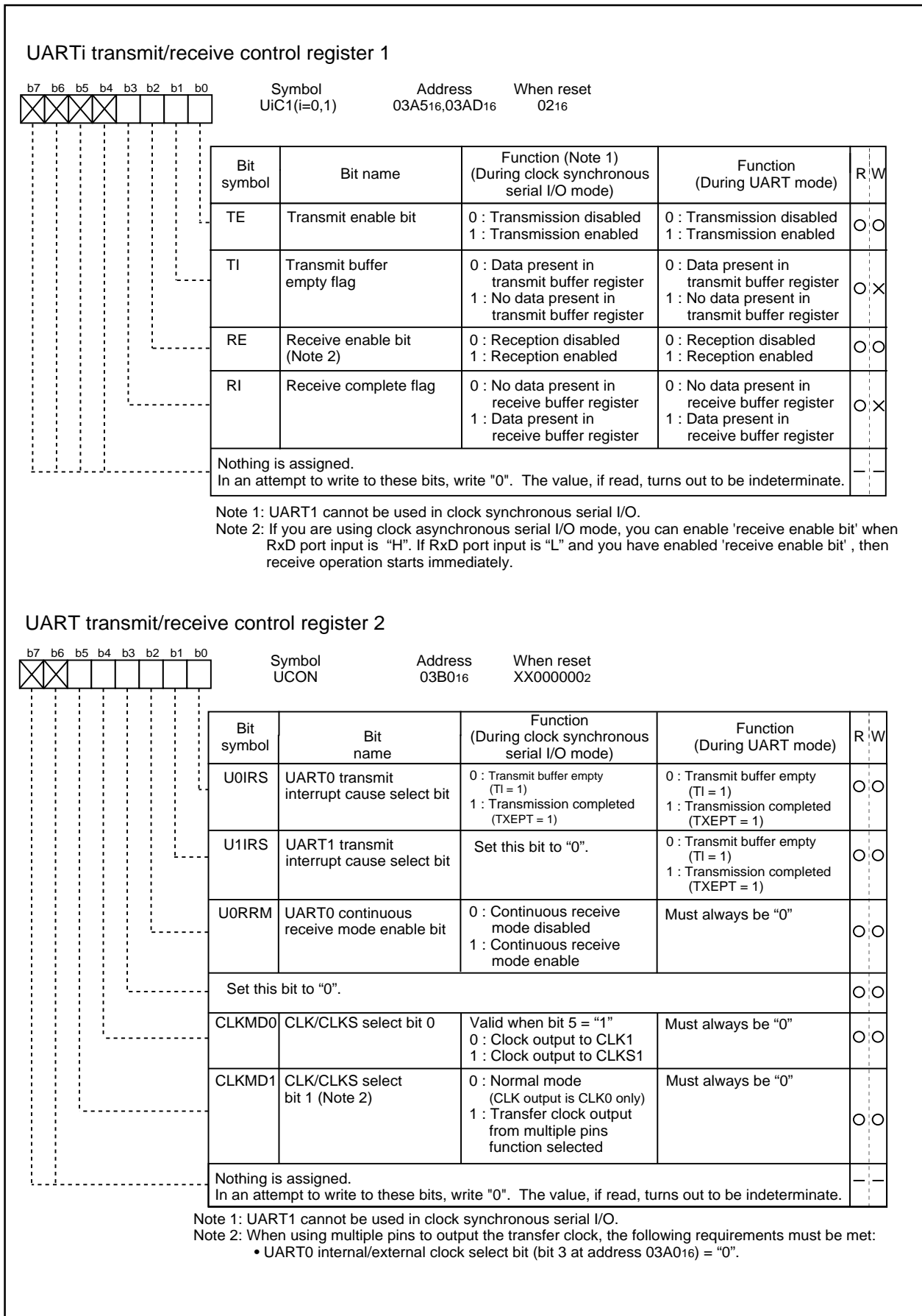


Figure 1.73. Serial I/O-related registers (3)

Clock synchronous serial I/O mode

(1) Clock synchronous serial I/O mode

The clock synchronous serial I/O mode uses a transfer clock to transmit and receive data. (See Table 1.25.) Figure 1.65 shows the UART0 transmit/receive mode register.

Table 1.25. Specifications of clock synchronous serial I/O mode

Item	Specification
Transfer data format	<ul style="list-style-type: none"> • Transfer data length: 8 bits
Transfer clock	<ul style="list-style-type: none"> • When internal clock is selected (bit 3 at address 03A0₁₆ = "0") : $f_i / 2^{(n+1)}$ (Note 1) $f_i = f_1, f_8, f_{32}, f_c$ • When external clock is selected (bit 3 at address 03A0₁₆ = "1") : Input from CLK0 pin
Transmission start condition	<ul style="list-style-type: none"> • To start transmission, the following requirements must be met: <ul style="list-style-type: none"> – Transmit enable bit (bit 0 at address 03A5₁₆) = "1" – Transmit buffer empty flag (bit 1 at addresses 03A5₁₆) = "0" • Furthermore, if external clock is selected, the following requirements must also be met: <ul style="list-style-type: none"> – CLK0 polarity select bit (bit 6 at address 03A4₁₆) = "0": CLK0 input level = "H" – CLK0 polarity select bit (bit 6 at address 03A4₁₆) = "1": CLK0 input level = "L"
Reception start condition	<ul style="list-style-type: none"> • To start reception, the following requirements must be met: <ul style="list-style-type: none"> – Receive enable bit (bit 2 at address 03A5₁₆) = "1" – Transmit enable bit (bit 0 at address 03A5₁₆) = "1" – Transmit buffer empty flag (bit 1 at address 03A5₁₆) = "0" • Furthermore, if external clock is selected, the following requirements must also be met: <ul style="list-style-type: none"> – CLK0 polarity select bit (bit 6 at address 03A4₁₆) = "0": CLK0 input level = "H" – CLK0 polarity select bit (bit 6 at address 03A4₁₆) = "1": CLK0 input level = "L"
Interrupt request generation timing	<ul style="list-style-type: none"> • When transmitting <ul style="list-style-type: none"> – Transmit interrupt cause select bit (bit 0 at address 03B0₁₆) = "0": Interrupts requested when data transfer from UART0 transfer buffer register to UART0 transmit register is completed – Transmit interrupt cause select bit (bit 0 at address 03B0₁₆) = "1": Interrupts requested when data transmission from UART0 transfer register is completed • When receiving <ul style="list-style-type: none"> – Interrupts requested when data transfer from UART0 receive register to UART0 receive buffer register is completed
Error detection	<ul style="list-style-type: none"> • Overrun error (Note 2) This error occurs when the next data is ready before contents of UART0 receive buffer register are read out
Select function	<ul style="list-style-type: none"> • CLK polarity selection Whether transmit data is output/input at the rising edge or falling edge of the transfer clock can be selected • LSB first/MSB first selection Whether transmission/reception begins with bit 0 or bit 7 can be selected • Continuous receive mode selection Reception is enabled simultaneously by a read from the receive buffer register • Transfer clock output from multiple pins selection UART0 transfer clock can be chosen by software to be output from one of the two pins set

Note 1: "n" denotes the value 00₁₆ to FF₁₆ that is set to the UART bit rate generator.

Note 2: If an overrun error occurs, the UART0 receive buffer will have the next data written in. Note also that the UART0 receive interrupt request bit does not change.

Clock synchronous serial I/O mode

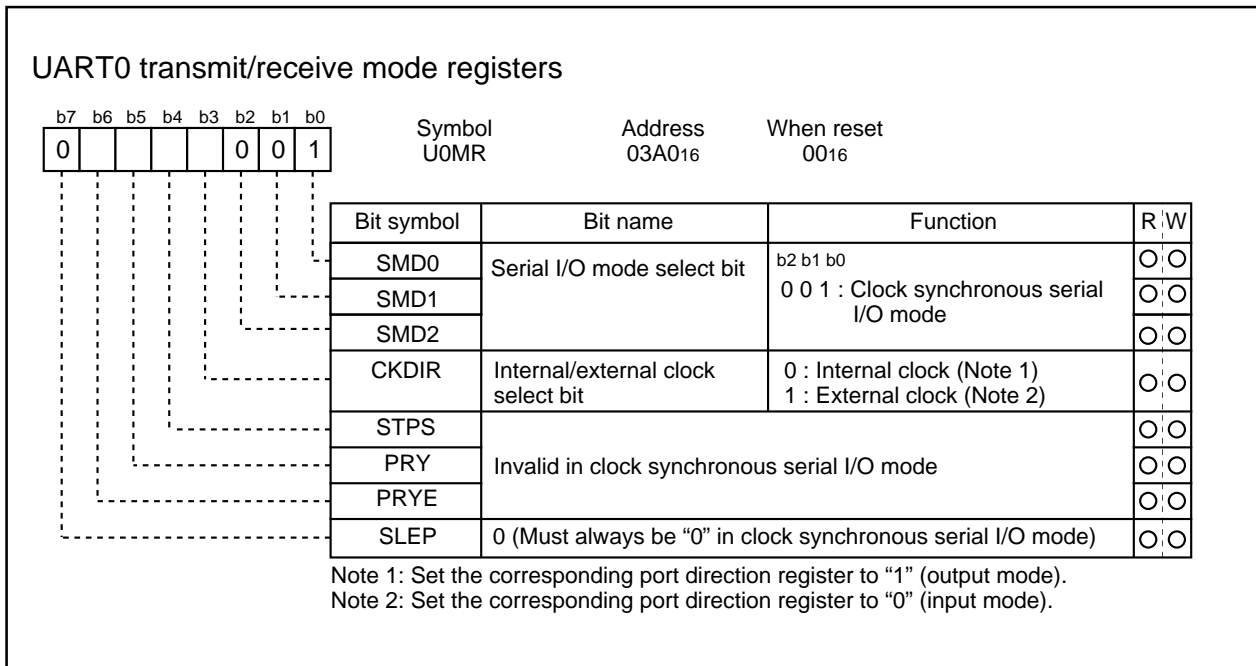


Figure 1.74. UART0 transmit/receive mode register in clock synchronous serial I/O mode

Table 1.26 lists the functions of the input/output pins during clock synchronous serial I/O mode. Note that for a period from when the UART0 operation mode is selected to when transfer starts, the TxD0 pin outputs a "H". (If the N-channel open-drain is selected, this pin is in floating state.)

Table 1.26. Input/output pin functions in clock synchronous serial I/O mode

Pin name	Function	Method of selection
TxD0 (P50)	Serial data output	Port P50 direction register (bit 0 at address 03EB ₁₆) = "1" (Outputs dummy data when performing reception only)
RxD0 (P51)	Serial data input	Port P51 direction register (bit 1 at address 03EB ₁₆) = "0" (Can be used as an input port when performing transmission only)
CLK0 (P52)	Transfer clock output	Internal/external clock select bit (bit 3 at address 03A0 ₁₆) = "0"
	Transfer clock input	Internal/external clock select bit (bit 3 at address 03A0 ₁₆) = "1" Port P52 direction register (bit 2 at address 03EB ₁₆) = "0"

Clock synchronous serial I/O mode

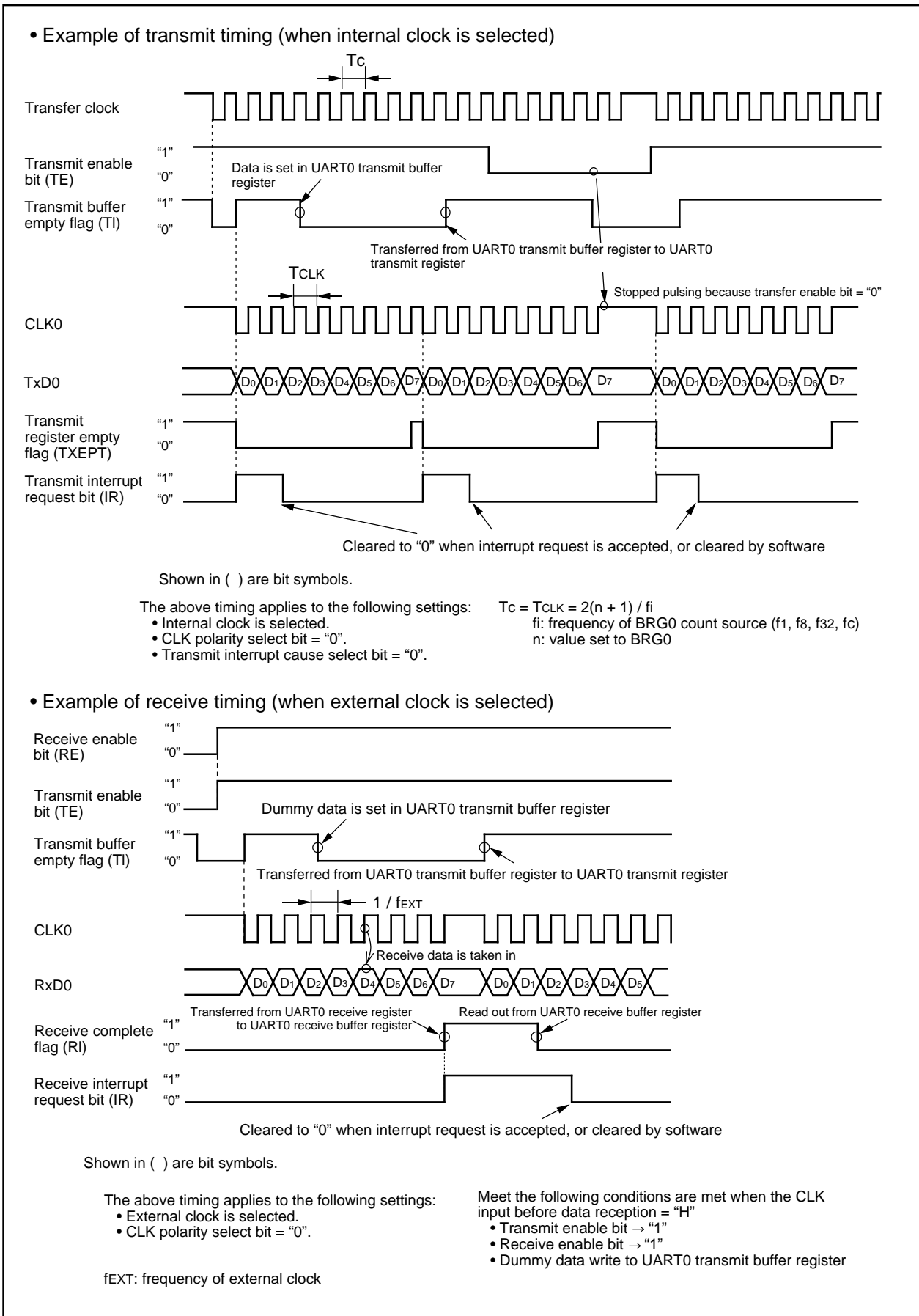


Figure 1.75. Typical transmit/receive timings in clock synchronous serial I/O mode

Clock synchronous serial I/O mode

(a) Polarity select function

As shown in Figure 1.76, the CLK polarity select bit (bit 6 at addresses 03A4₁₆) allows selection of the polarity of the transfer clock.

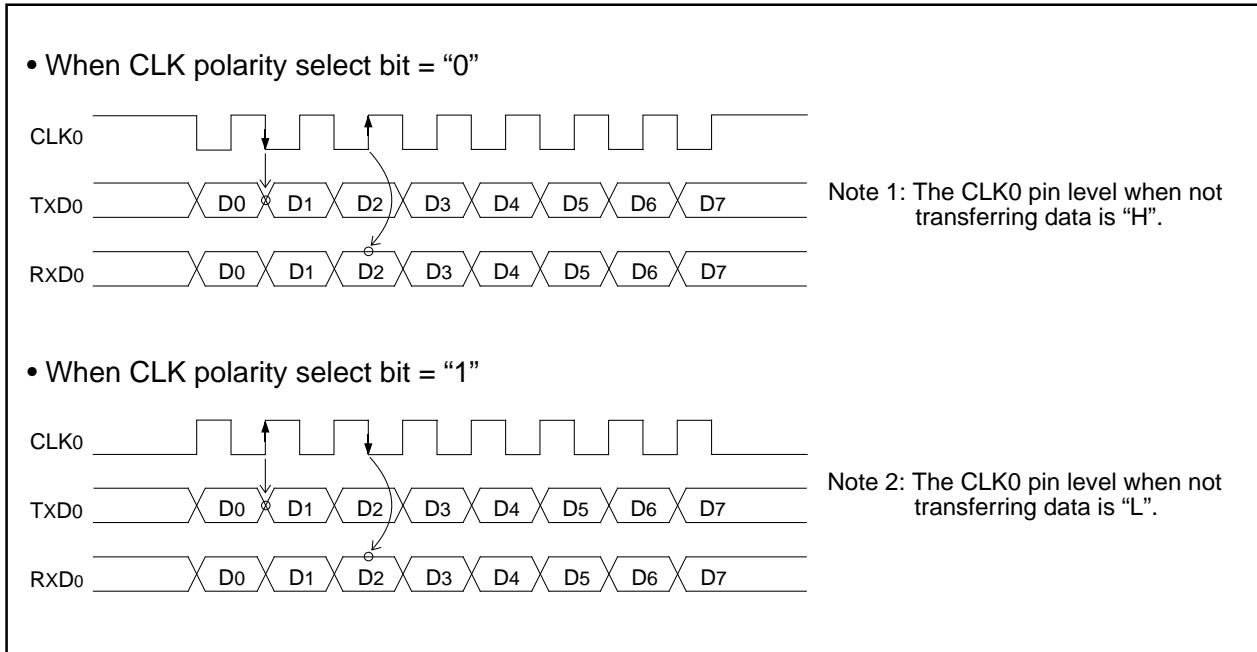


Figure 1.76. Polarity of transfer clock

(b) LSB first/MSB first select function

As shown in Figure 1.77, when the transfer format select bit (bit 7 at addresses 03A4₁₆) = "0", the transfer format is "LSB first"; when the bit = "1", the transfer format is "MSB first".

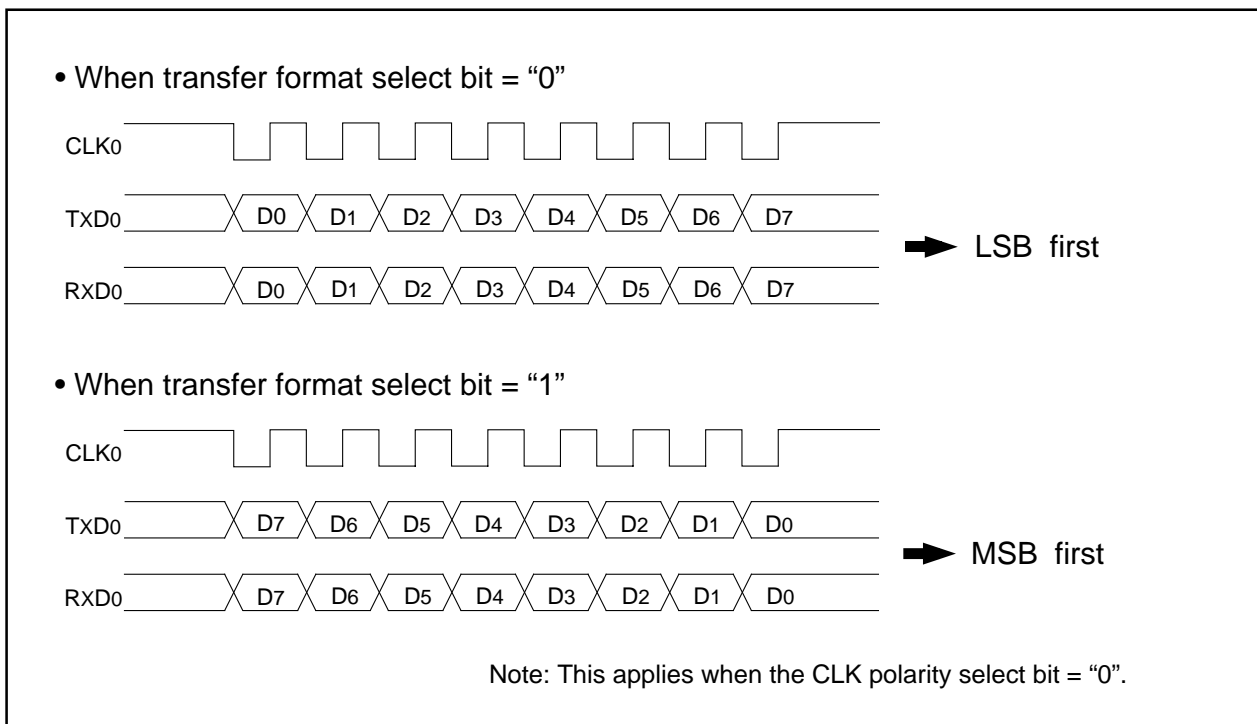


Figure 1.77. Transfer format

Clock synchronous serial I/O mode

(c) Transfer clock output from multiple pins function

This function allows the setting two transfer clock output pins and choosing one of the two to output a clock by using the CLK and CLKS select bit (bits 4 and 5 at address 03B016). (See Figure 1.78.) The multiple pins function is valid only when the internal clock is selected for UART0.

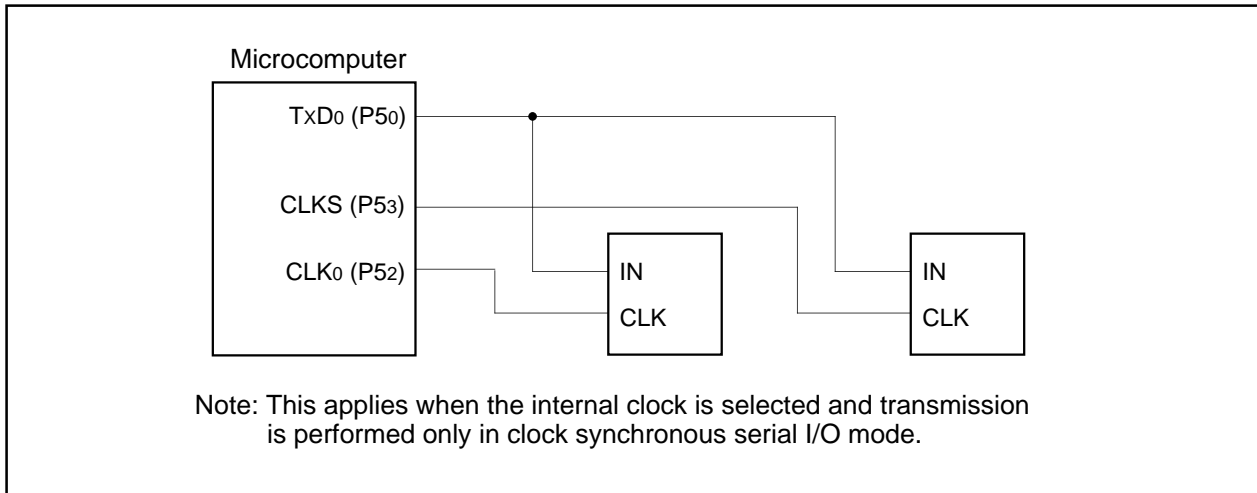


Figure 1.78. The transfer clock output from the multiple pins function usage

(d) Continuous receive mode

If the continuous receive mode enable bit (bits 2 and 3 at address 03B016) is set to "1", the unit is placed in continuous receive mode. In this mode, when the receive buffer register is read out, the unit simultaneously goes to a receive enable state without having to set dummy data to the transmit buffer register back again.

Clock asynchronous serial I/O (UART) mode

(2) Clock asynchronous serial I/O (UART) mode

The UART mode allows transmitting and receiving data after setting the desired transfer rate and transfer data format. (See Table 1.27.) Figure 1.79 shows the UARTi transmit/receive mode register.

Table 1.27. Specifications of UART Mode

Item	Specification
Transfer data format	<ul style="list-style-type: none"> • Character bit (transfer data): 7 bits, 8 bits, or 9 bits as selected • Start bit: 1 bit • Parity bit: Odd, even, or nothing as selected • Stop bit: 1 bit or 2 bits as selected
Transfer clock	<ul style="list-style-type: none"> • When internal clock is selected (bit 3 at addresses 03A0₁₆, 03A8₁₆ = "0") : $f_i/16(n+1)$ (Note 1) $f_i = f_1, f_8, f_{32}, f_c$ • When external clock is selected (bit 3 at addresses 03A0₁₆="1") : $f_{EXT}/16(n+1)$ (Note 1) (Note 2)
Transmission start condition	<ul style="list-style-type: none"> • To start transmission, the following requirements must be met: <ul style="list-style-type: none"> - Transmit enable bit (bit 0 at addresses 03A5₁₆, 03AD₁₆) = "1" - Transmit buffer empty flag (bit 1 at addresses 03A5₁₆, 03AD₁₆) = "0"
Reception start condition	<ul style="list-style-type: none"> • To start reception, the following requirements must be met: <ul style="list-style-type: none"> - Receive enable bit (bit 2 at addresses 03A5₁₆, 03AD₁₆) = "1" - Start bit detection
Interrupt request generation timing	<ul style="list-style-type: none"> • When transmitting <ul style="list-style-type: none"> - Transmit interrupt cause select bits (bits 0,1 at address 03B0₁₆) = "0": Interrupts requested when data transfer from UARTi transfer buffer register to UARTi transmit register is completed - Transmit interrupt cause select bits (bits 0, 1 at address 03B0₁₆) = "1": Interrupts requested when data transmission from UARTi transfer register is completed • When receiving <ul style="list-style-type: none"> - Interrupts requested when data transfer from UARTi receive register to UARTi receive buffer register is completed
Error detection	<ul style="list-style-type: none"> • Overrun error (Note 3) This error occurs when the next data is ready before contents of UARTi receive buffer register are read out • Framing error This error occurs when the number of stop bits set is not detected • Parity error This error occurs when if parity is enabled, the number of 1's in parity and character bits does not match the number of 1's set • Error sum flag This flag is set (= 1) when any of the overrun, framing, and parity errors is encountered
Select function	<ul style="list-style-type: none"> • Sleep mode selection This mode is used to transfer data to and from one of multiple slave micro-computers

Note 1: 'n' denotes the value 00₁₆ to FF₁₆ that is set to the UART bit rate generator.

Note 2: f_{EXT} is input from the CLK0 pin. Since UART1 does not have this pin, cannot select external clock.

Note 3: If an overrun error occurs, the UARTi receive buffer will have the next data written in. Note also that the UARTi receive interrupt request bit does not change.

Clock asynchronous serial I/O (UART) mode

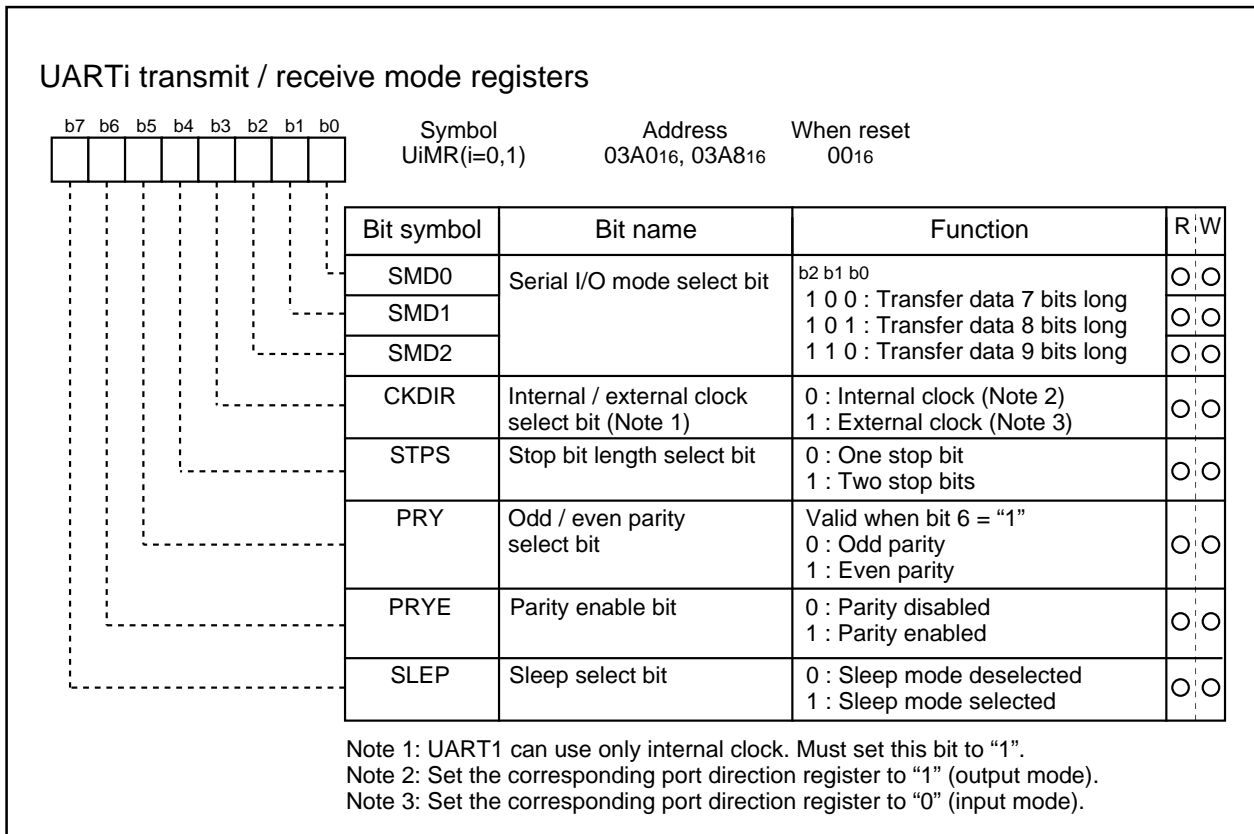
Figure 1.79. UART_i transmit/receive mode register in UART mode

Table 1.28 lists the functions of the input/output pins during UART mode. Note that for a period from when the UART_i operation mode is selected to when transfer starts, the TxDi pin outputs a "H". (If the N-channel open-drain is selected, this pin is in floating state.)

Table 1.28. Input/output pin functions in UART mode

Pin name	Function	Method of selection
TxDi (P50, P40)	Serial data output	Port P51 and P42 direction register (bit 0 at address 03EB16, bit 0 at address 03EA16) = "1" (Can be used as an input port when performing reception only)
RxDi (P51, P42)	Serial data input	Port P51 and P42 direction register (bit 1 at address 03EB16, bit 2 at address 03EA16) = "0" (Can be used as an input port when performing transmission only)
CLK0 (P52)	Programmable I/O port	Internal/external clock select bit (bit 3 at address 03A016) = "0"
	Transfer clock input	Internal/external clock select bit (bit 3 at address 03A016) = "1"

Clock asynchronous serial I/O (UART) mode

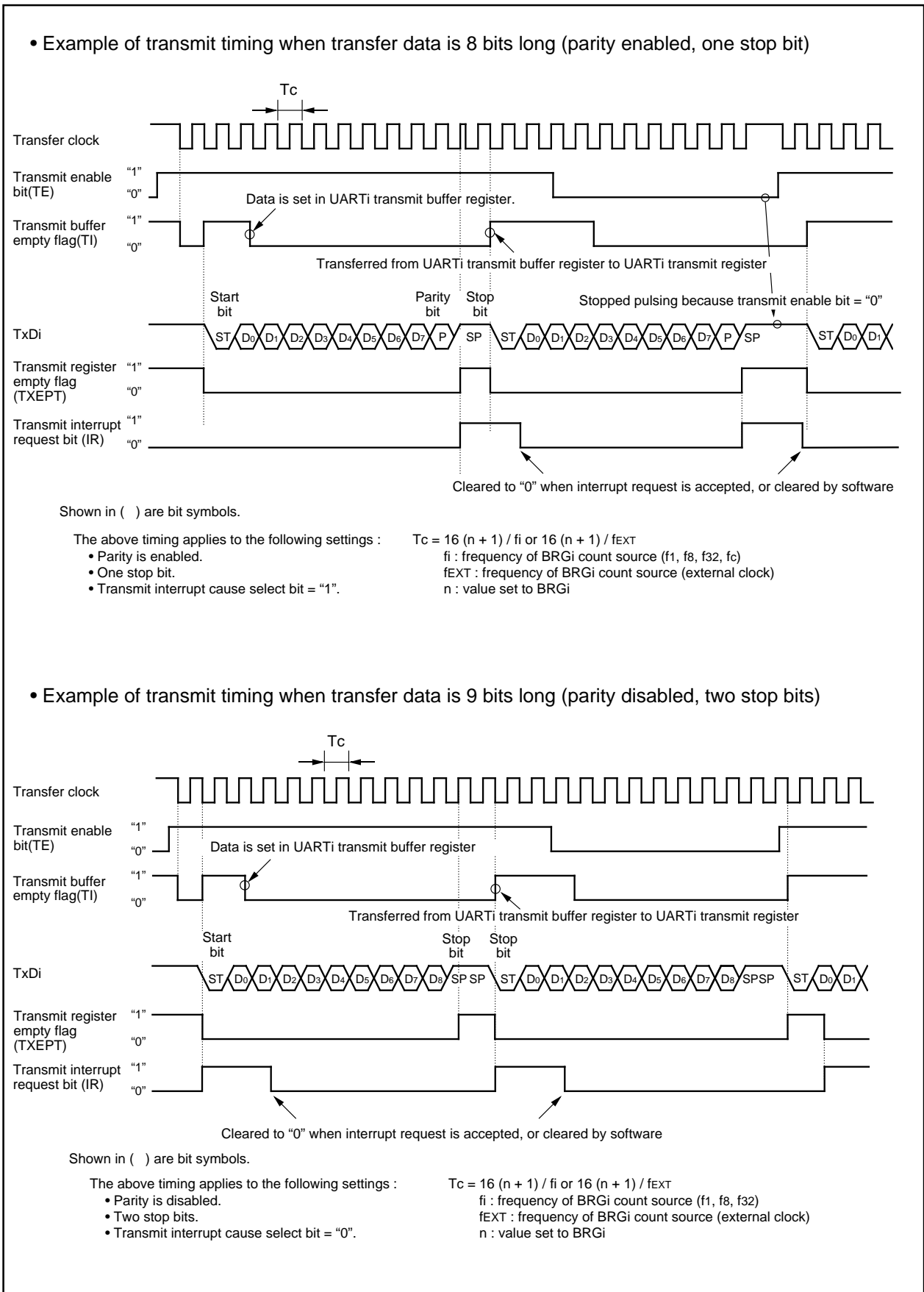


Figure 1.80. Typical transmit timings in UART mode

Clock asynchronous serial I/O (UART) mode

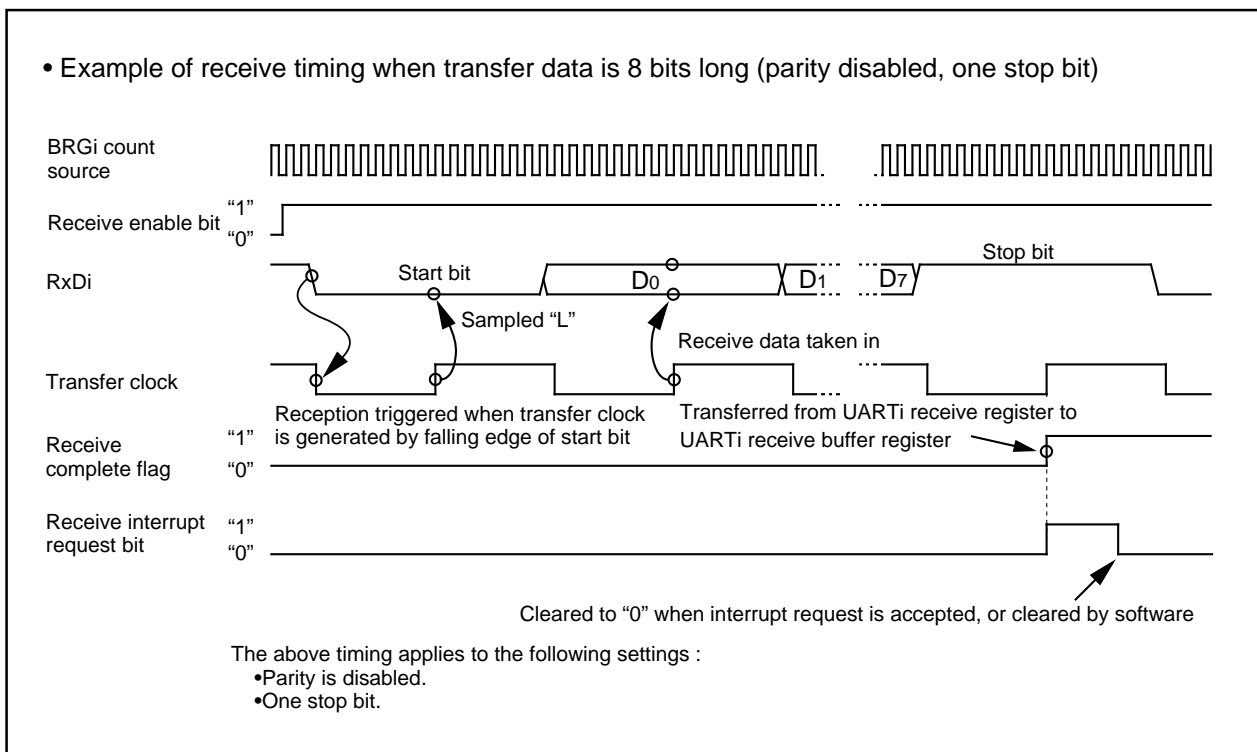


Figure 1.81. Typical receive timing in UART mode

(a) Sleep mode

This mode is used to transfer data between specific microcomputers among multiple microcomputers connected using UARTi. The sleep mode is selected when the sleep select bit (bit 7 at addresses 03A016, 03A816) is set to "1" during reception. In this mode, the unit performs receive operation when the MSB of the received data = "1" and does not perform receive operation when the MSB = "0".

A-D Converter

A-D Converter

The A-D converter consists of one 10-bit successive approximation A-D converter circuit with a capacitive coupling amplifier. Pins P60 to P67, and P50 to P54 also function as the analog signal input pins. The direction registers of these pins for A-D conversion must therefore be set to input. The Vref connect bit (bit 5 at address 03D716) can be used to isolate the resistance ladder of the A-D converter from the reference voltage input pin (VREF) when the A-D converter is not used. Doing so stops any current flowing into the resistance ladder from VREF, reducing the power dissipation. When using the A-D converter, start A-D conversion only after setting bit 5 of 03D716 to connect VREF.

The result of A-D conversion is stored in the A-D registers of the selected pins. When set to 10-bit precision, the low 8 bits are stored in the even addresses and the high 2 bits in the odd addresses. When set to 8-bit precision, the low 8 bits are stored in the even addresses.

Table 1.29 shows the performance of the A-D converter. Figure 1.82 shows the block diagram of the A-D converter, and Figures 1.83 and 1.84 show the A-D converter-related registers.

Table 1.29. Performance of A-D converter

Item	Performance
Method of A-D conversion	Successive approximation (capacitive coupling amplifier)
Analog input voltage (Note 1)	0V to AVCC (VCC)
Operating clock ϕ_{AD} (Note 2)	VCC = 5V f_{AD} , divide-by-2 of f_{AD} , divide-by-4 of f_{AD} , $f_{AD}=f(XIN)$ VCC = 3V divide-by-2 of f_{AD} , divide-by-4 of f_{AD} , $f_{AD}=f(XIN)$
Resolution	8-bit or 10-bit (selectable)
Absolute precision	VCC = 5V • Without sample and hold function $\pm 3\text{LSB}$ • With sample and hold function (8-bit resolution) $\pm 2\text{LSB}$ • With sample and hold function (10-bit resolution) $\pm 3\text{LSB}$ VCC = 3V • Without sample and hold function (8-bit resolution) $\pm 2\text{LSB}$
Operating modes	One-shot mode, repeat mode, single sweep mode, repeat sweep mode 0, and repeat sweep mode 1
Analog input pins	8 pins (AN0 to AN7) + 5 pins (AN50 to AN54)
A-D conversion start condition	• Software trigger A-D conversion starts when the A-D conversion start flag changes to "1"
Conversion speed per pin	• Without sample and hold function 8-bit resolution: 49 ϕ_{AD} cycles, 10-bit resolution: 59 ϕ_{AD} cycles • With sample and hold function 8-bit resolution: 28 ϕ_{AD} cycles, 10-bit resolution: 33 ϕ_{AD} cycles

Note 1: Does not depend on use of sample and hold function.

Note 2: Without sample and hold function, set the ϕ_{AD} frequency to 250kHz min.

With the sample and hold function, set the ϕ_{AD} frequency to 1MHz min.

A-D Converter

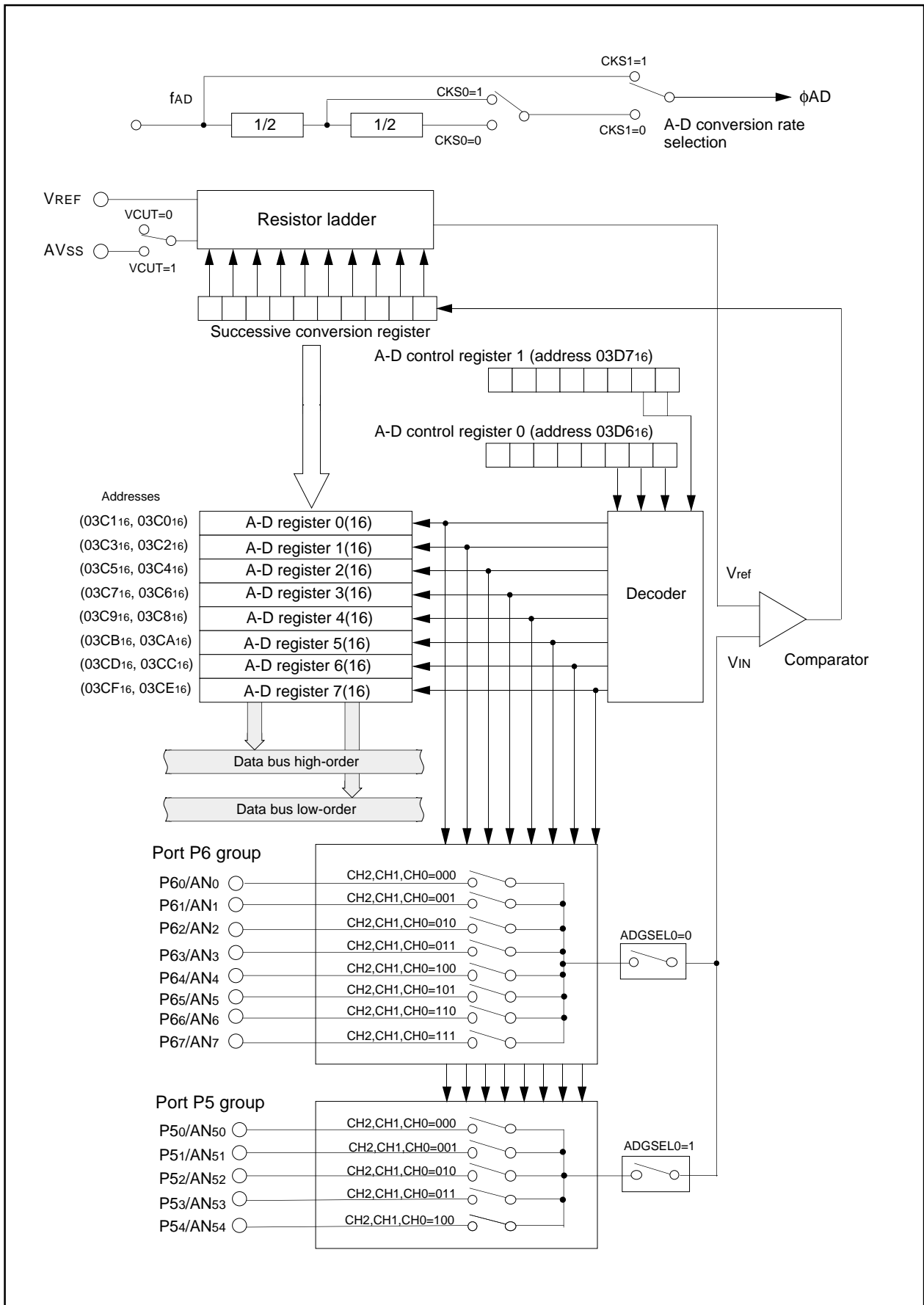


Figure 1.82. Block diagram of A-D converter

A-D Converter

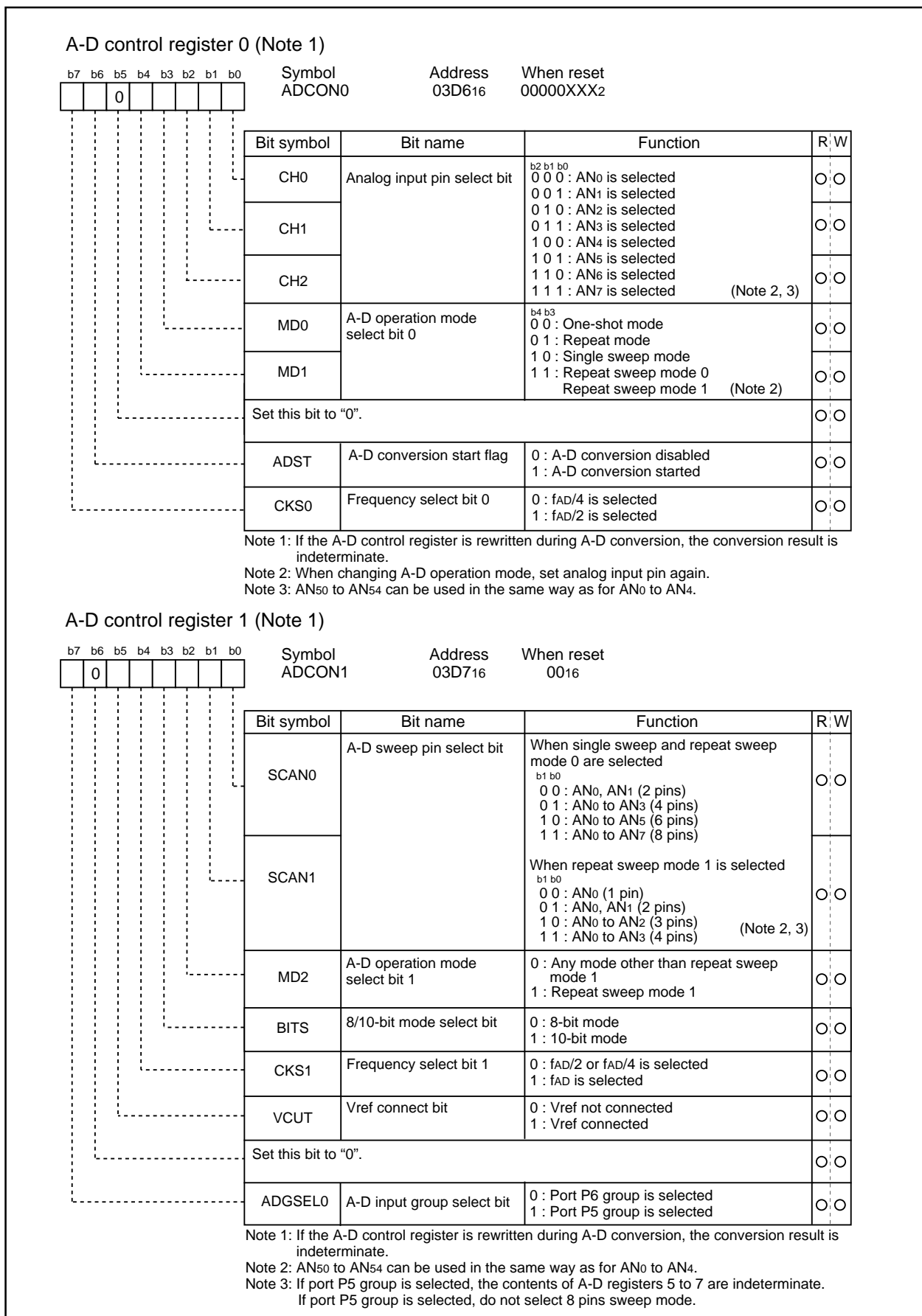


Figure 1.83. A-D converter-related registers (1)

A-D Converter

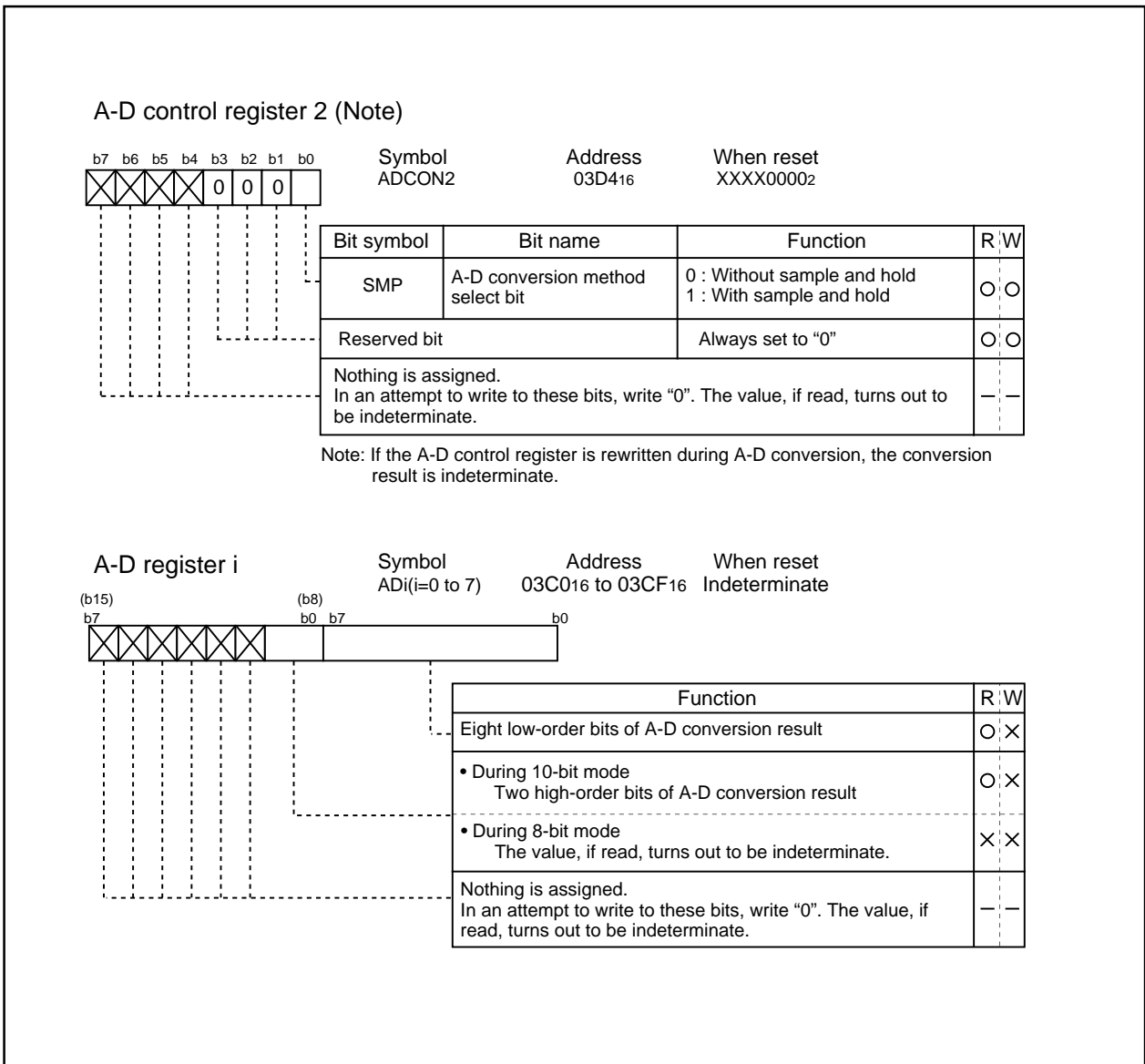


Figure 1.84. A-D converter-related registers (2)

A-D Converter

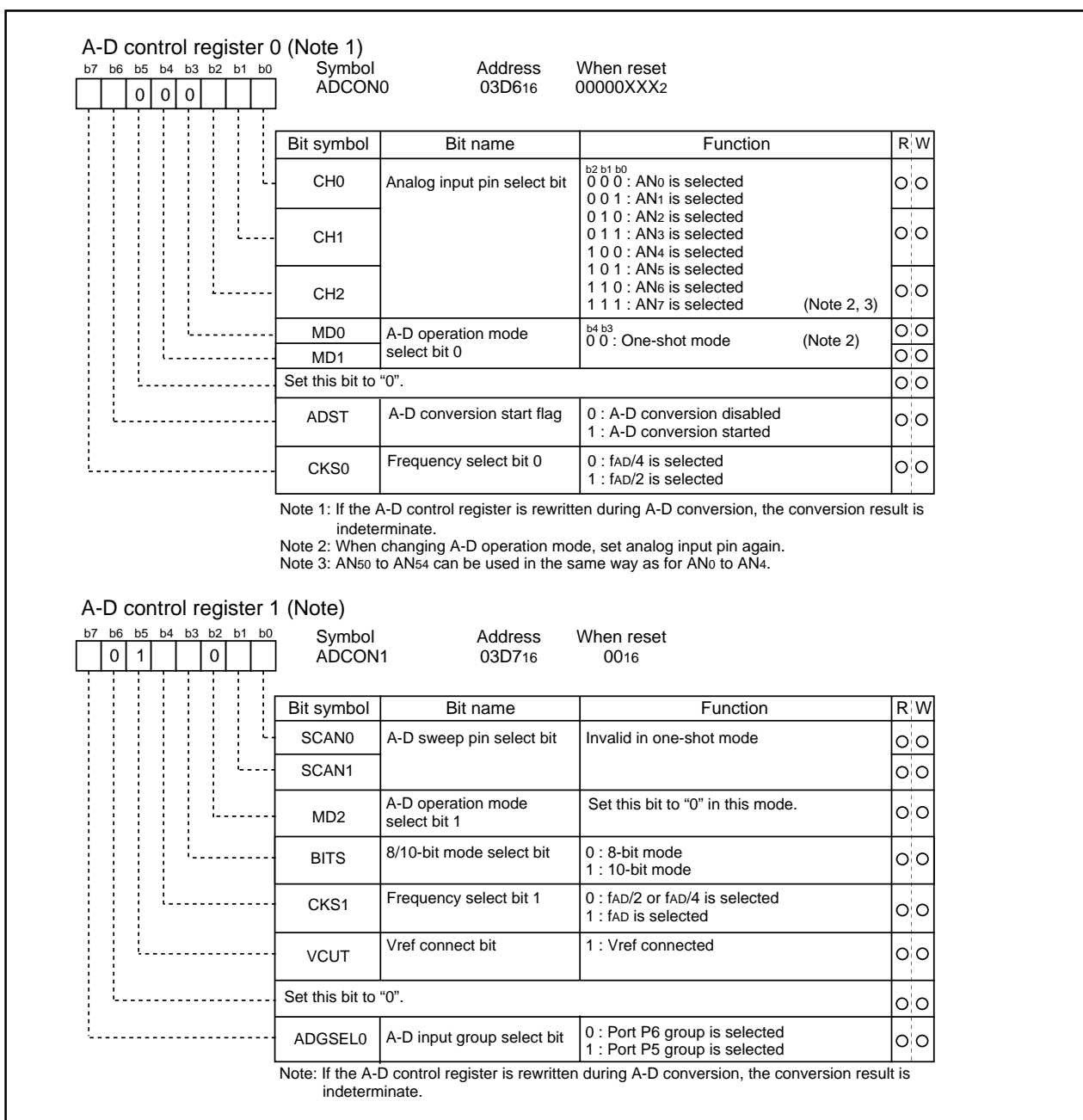
(1) One-shot mode

In one-shot mode, the pin selected using the analog input pin select bit is used for one-shot A-D conversion. (See Table 1.30.) Figure 1.85 shows the A-D control register in one-shot mode.

Table 1.30. One-shot mode specifications

Item	Specification
Function	The pin selected by the analog input pin select bit is used for one A-D conversion
Start condition	Writing "1" to A-D conversion start flag
Stop condition	<ul style="list-style-type: none"> • End of A-D conversion (A-D conversion start flag changes to "0") • Writing "0" to A-D conversion start flag
Interrupt request generation timing	End of A-D conversion
Input pin	One of AN ₀ to AN ₇ , as selected (Note)
Reading of result of A-D converter	Read A-D register corresponding to selected pin

Note : AN₅₀ to AN₅₄ can be used in the same way as for AN₀ to AN₄.

**Figure 1.85. A-D conversion register in one-shot mode**

A-D Converter

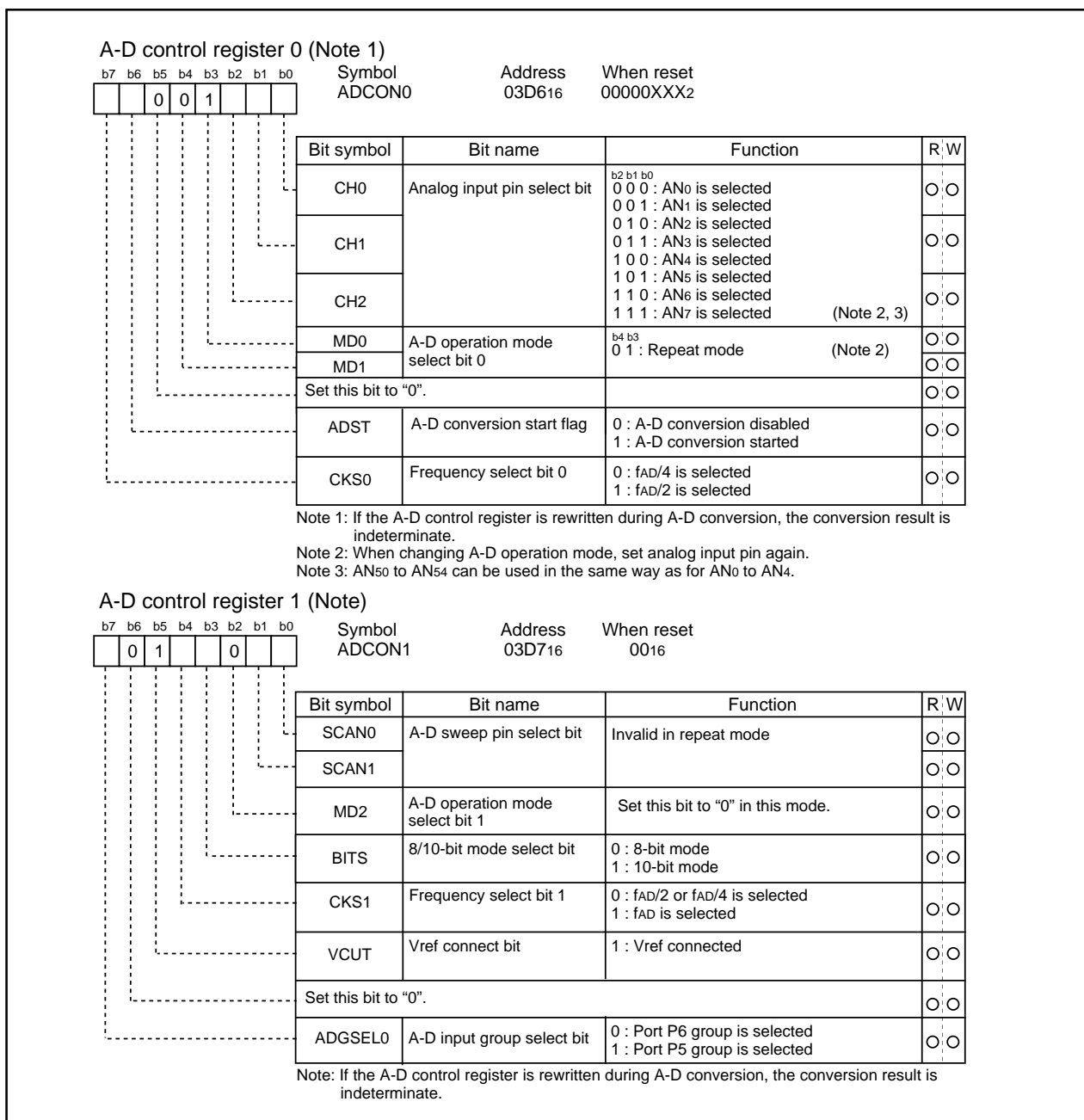
(2) Repeat mode

In repeat mode, the pin selected using the analog input pin select bit is used for repeated A-D conversion. (See Table 1.31.) Figure 1.86 shows the A-D control register in repeat mode.

Table 1.31. Repeat mode specifications

Item	Specification
Function	The pin selected by the analog input pin select bit is used for repeated A-D conversion
Start condition	Writing "1" to A-D conversion start flag
Stop condition	Writing "0" to A-D conversion start flag
Interrupt request generation timing	None generated
Input pin	One of AN0 to AN7, as selected (Note)
Reading of result of A-D converter	Read A-D register corresponding to selected pin (at any time)

Note : AN50 to AN54 can be used in the same way as for AN0 to AN4.

**Figure 1.86. A-D conversion register in repeat mode**

A-D Converter

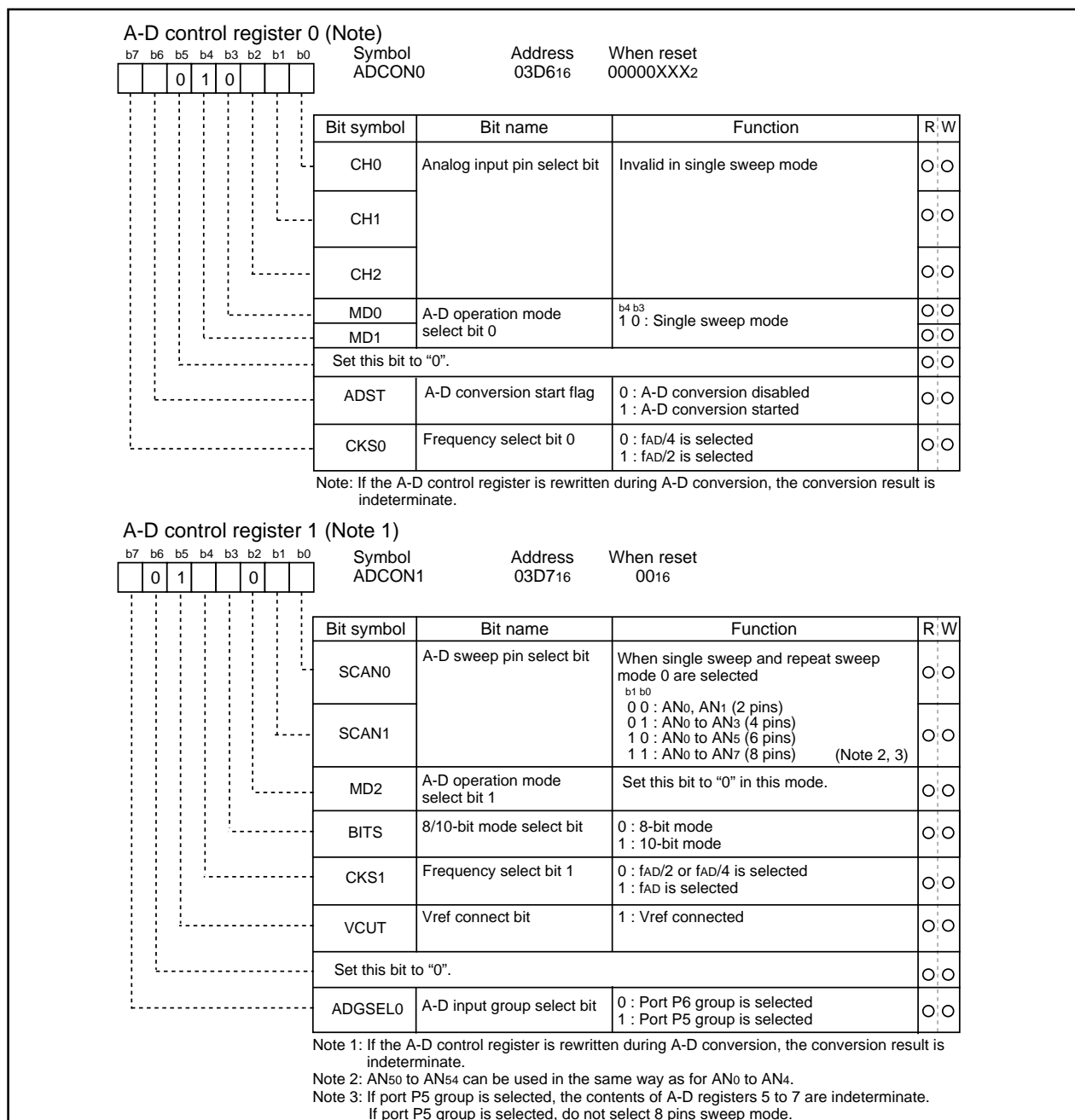
(3) Single sweep mode

In single sweep mode, the pins selected using the A-D sweep pin select bit are used for one-by-one A-D conversion. (See Table 1.32.) Figure 1.87 shows the A-D control register in single sweep mode.

Table 1.32. Single sweep mode specifications

Item	Specification
Function	The pins selected by the A-D sweep pin select bit are used for one-by-one A-D conversion
Start condition	Writing "1" to A-D converter start flag
Stop condition	<ul style="list-style-type: none"> • End of A-D conversion (A-D conversion start flag changes to "0".) • Writing "0" to A-D conversion start flag
Interrupt request generation timing	End of A-D conversion
Input pin	AN ₀ and AN ₁ (2 pins), AN ₀ to AN ₃ (4 pins), AN ₀ to AN ₅ (6 pins), or AN ₀ to AN ₇ (8 pins)(Note)
Reading of result of A-D converter	Read A-D register corresponding to selected pin

Note : AN₅₀ to AN₅₄ can be used in the same way as for AN₀ to AN₄.

**Figure 1.87. A-D conversion register in single sweep mode**

A-D Converter

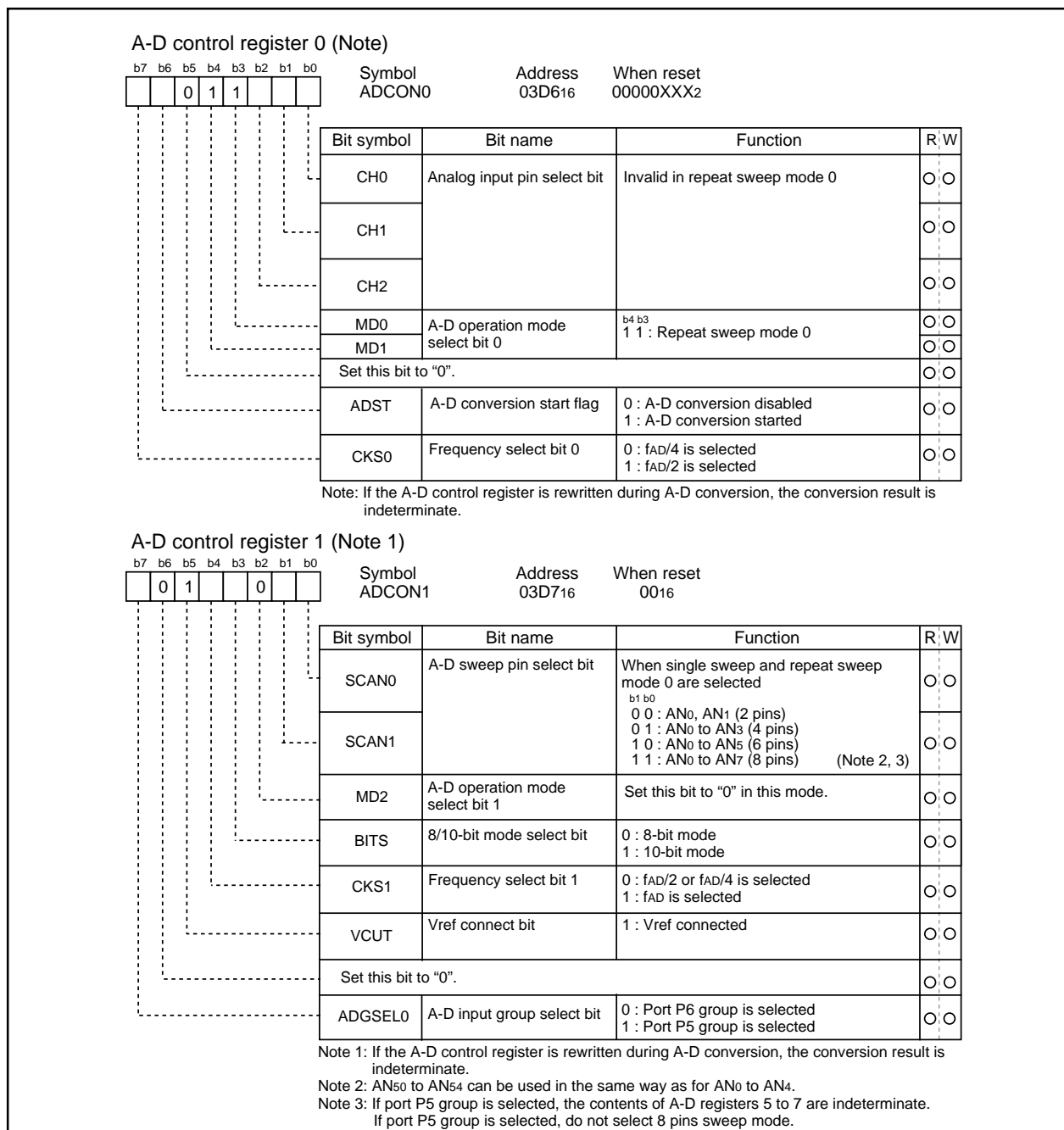
(4) Repeat sweep mode 0

In repeat sweep mode 0, the pins selected using the A-D sweep pin select bit are used for repeat sweep A-D conversion. (See Table 1.33.) Figure 1.88 shows the A-D control register in repeat sweep mode 0.

Table 1.33. Repeat sweep mode 0 specifications

Item	Specification
Function	The pins selected by the A-D sweep pin select bit are used for repeat sweep A-D conversion
Start condition	Writing "1" to A-D conversion start flag
Stop condition	Writing "0" to A-D conversion start flag
Interrupt request generation timing	None generated
Input pin	AN ₀ and AN ₁ (2 pins), AN ₀ to AN ₃ (4 pins), AN ₀ to AN ₅ (6 pins), or AN ₀ to AN ₇ (8 pins)(Note)
Reading of result of A-D converter	Read A-D register corresponding to selected pin (at any time)

Note : AN₅₀ to AN₅₄ can be used in the same way as for AN₀ to AN₄.

**Figure 1.88. A-D conversion register in repeat sweep mode 0**

A-D Converter

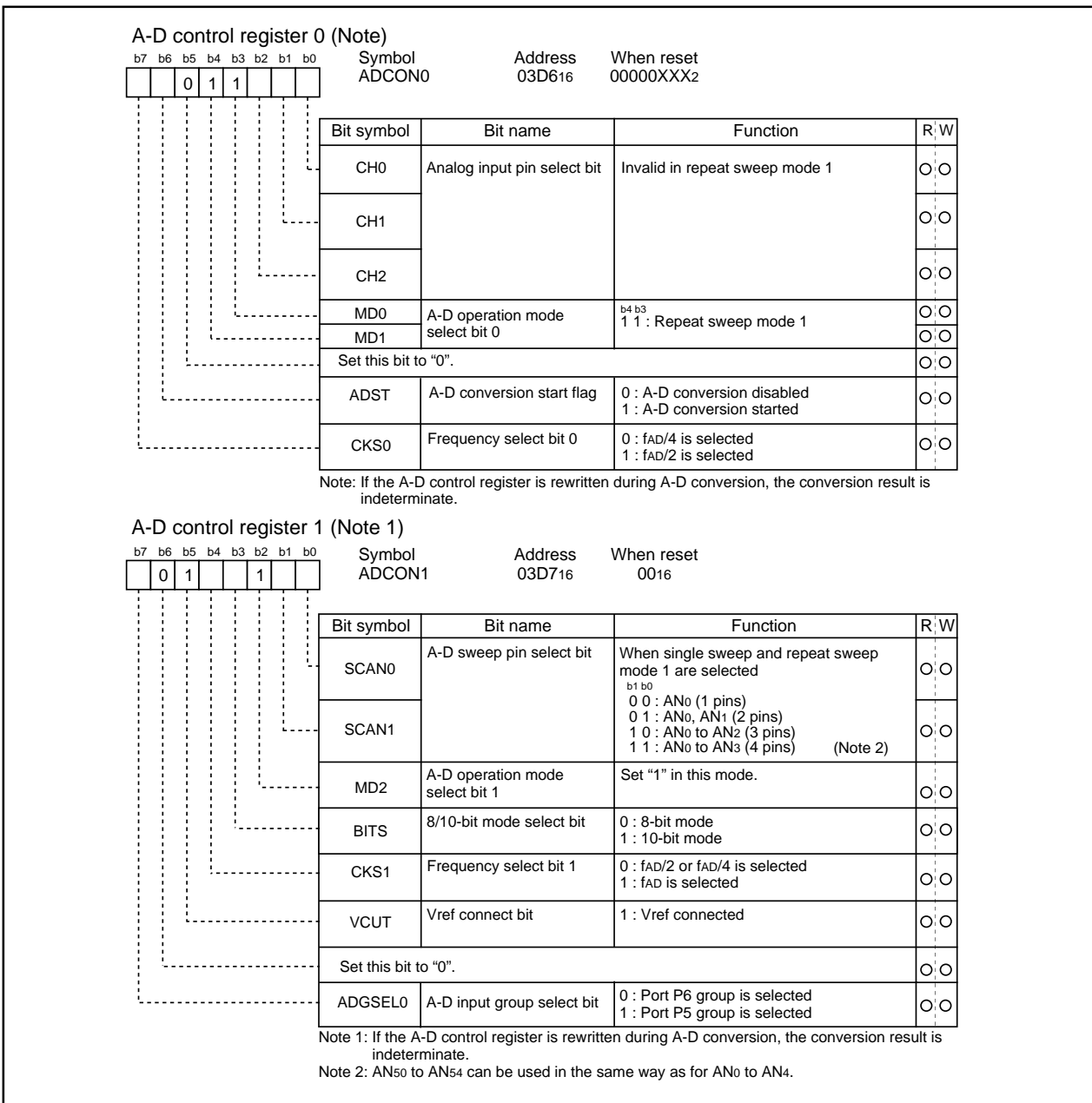
(5) Repeat sweep mode 1

In repeat sweep mode 1, all pins are used for A-D conversion with emphasis on the pin or pins selected using the A-D sweep pin select bit. (See Table 1.34.) Figure 1.89 shows the A-D control register in repeat sweep mode 1.

Table 1.34. Repeat sweep mode 1 specifications

Item	Specification
Function	All pins perform repeat sweep A-D conversion, with emphasis on the pin or pins selected by the A-D sweep pin select bit Example : AN ₀ selected AN ₀ → AN ₁ → AN ₀ → AN ₂ → AN ₀ → AN ₃ , etc
Start condition	Writing "1" to A-D conversion start flag
Stop condition	Writing "0" to A-D conversion start flag
Interrupt request generation timing	None generated
Input pin	AN ₀ (1 pin), AN ₀ and AN ₁ (2 pins), AN ₀ to AN ₂ (3 pins), AN ₀ to AN ₃ (4 pins) (Note)
Reading of result of A-D converter	Read A-D register corresponding to selected pin (at any time)

Note : AN₅₀ to AN₅₄ can be used in the same way as for AN₀ to AN₄.

**Figure 1.89. A-D conversion register in repeat sweep mode 1**

A-D Converter

- **Sample and hold**

Sample and hold is selected by setting bit 0 of the A-D control register 2 (address 03D4₁₆) to "1". When sample and hold is selected, the rate of conversion of each pin increases. As a result, a 28 ϕ_{AD} cycle is achieved with 8-bit resolution and 33 ϕ_{AD} with 10-bit resolution. Sample and hold can be selected in all modes. However, in all modes, be sure to specify before starting A-D conversion whether sample and hold is to be used.

Programmable I/O Ports

There are 43 programmable I/O ports: P0 to P7. Each port can be set independently for input or output using the direction register. A pull-up resistance for each block of 4 ports can be set. The port P1 allows the drive capacity of its N-channel output transistor to be set as necessary.

Figures 1.90 to 1.92 show the programmable I/O ports.

Each pin functions as a programmable I/O port and as the I/O for the built-in peripheral devices.

To use the pins as the inputs for the built-in peripheral devices, set the direction register of each pin to input mode. When the pins are used as the outputs for the built-in peripheral devices, they function as outputs regardless of the contents of the direction registers. See the descriptions of the respective functions for how to set up the built-in peripheral devices.

(1) Direction registers

Figure 1.93 shows the direction registers.

These registers are used to choose the direction of the programmable I/O ports. Each bit in these registers corresponds one for one to each I/O pin.

(2) Port registers

Figure 1.94 shows the port registers.

These registers are used to write and read data for input and output to and from an external device. A port register consists of a port latch to hold output data and a circuit to read the status of a pin. Each bit in port registers corresponds one for one to each I/O pin.

(3) Pull-up control registers

Figure 1.95 shows the pull-up control registers.

The pull-up control register can be set to apply a pull-up resistance to each block of 4 ports. When ports are set to have a pull-up resistance, the pull-up resistance is connected only when the direction register is set for input.

(4) Port P1 drive capacity control register

Figure 1.95 shows a structure of the port P1 drive capacity control register.

This register is used to control the drive capacity of the port P1's N-channel output transistor. Each bit in this register corresponds one for one to the port pins.

Programmable I/O Port

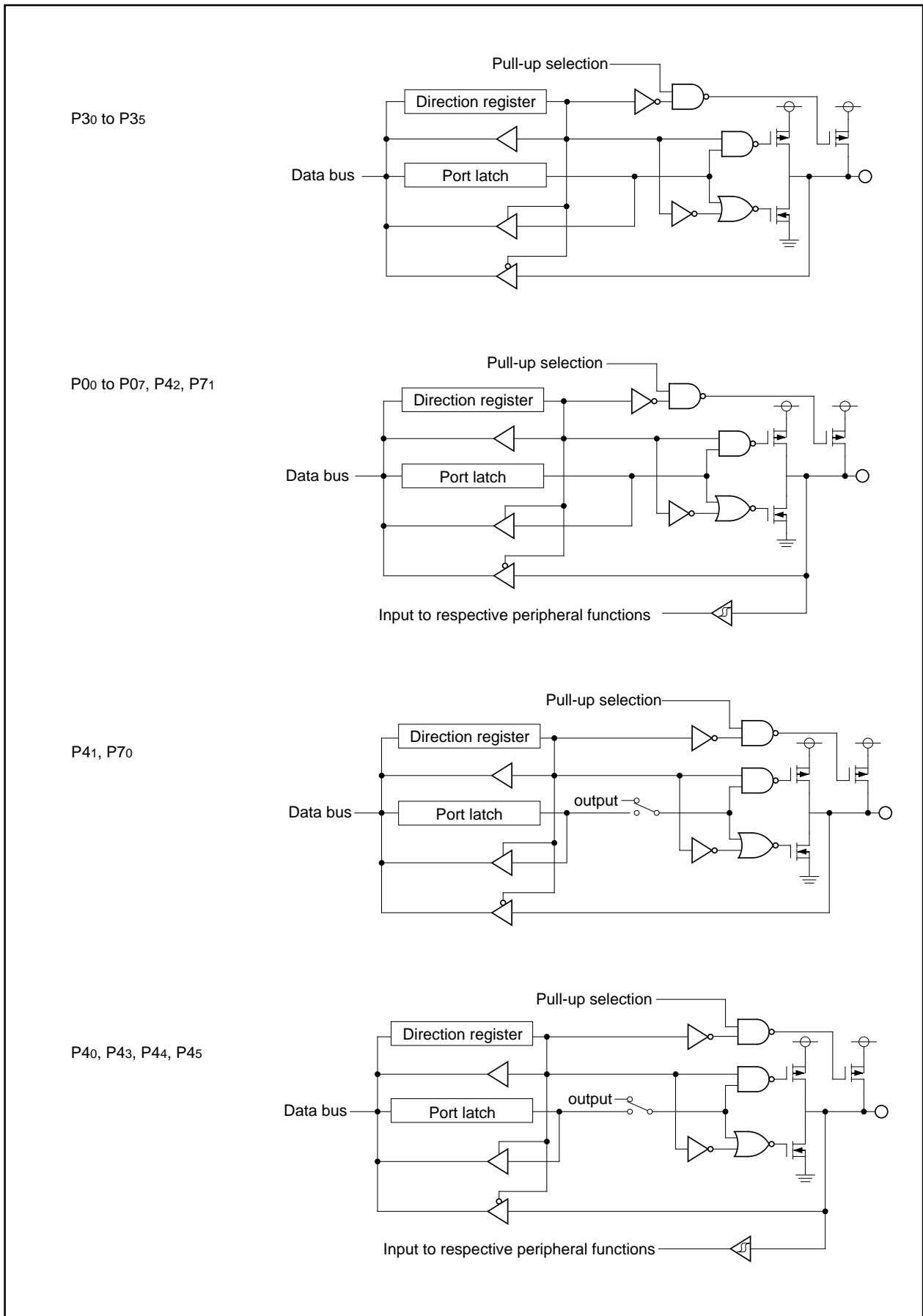


Figure 1.90. Programmable I/O ports (1)

Programmable I/O Port

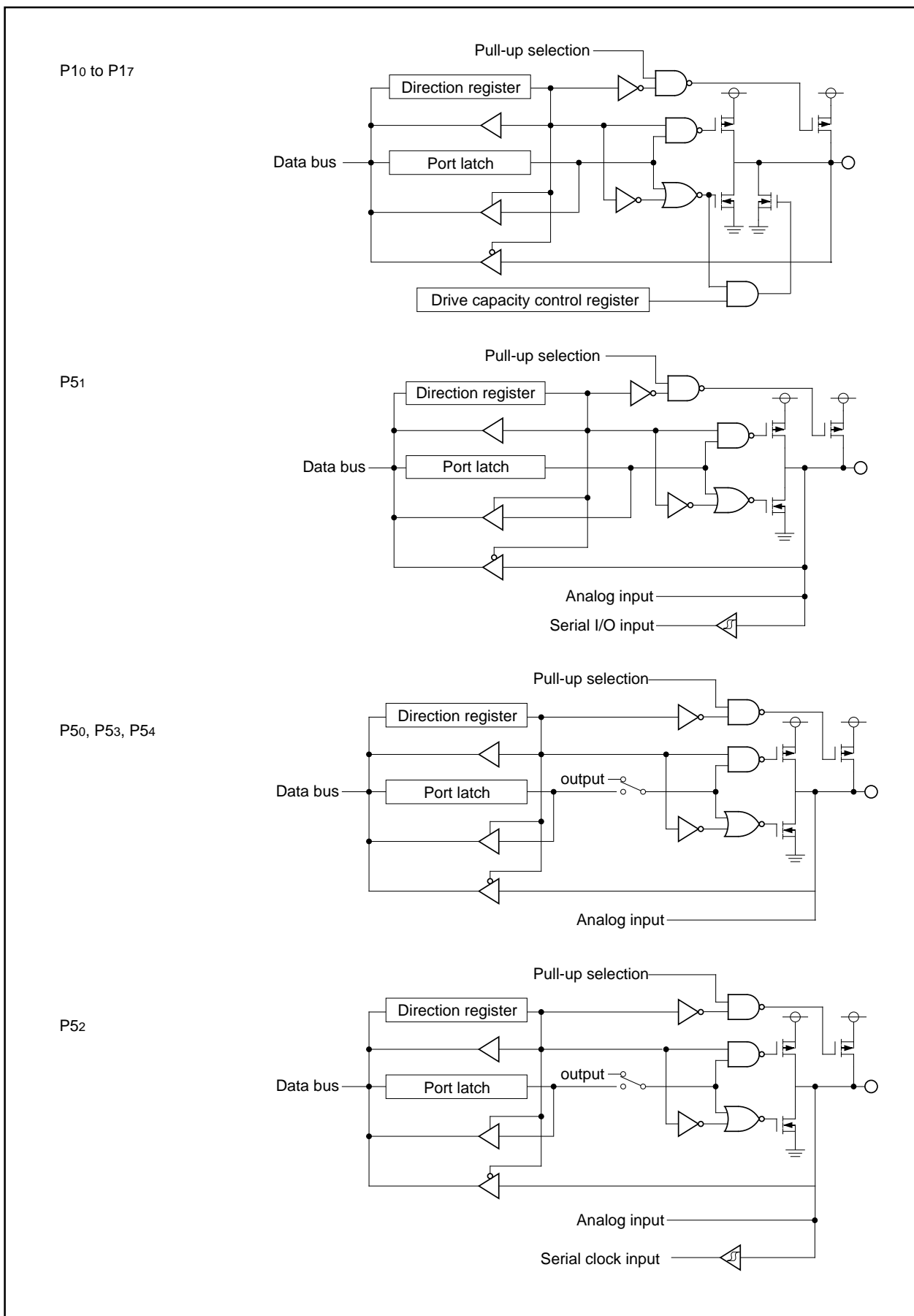


Figure 1.91. Programmable I/O ports (2)

Programmable I/O Port

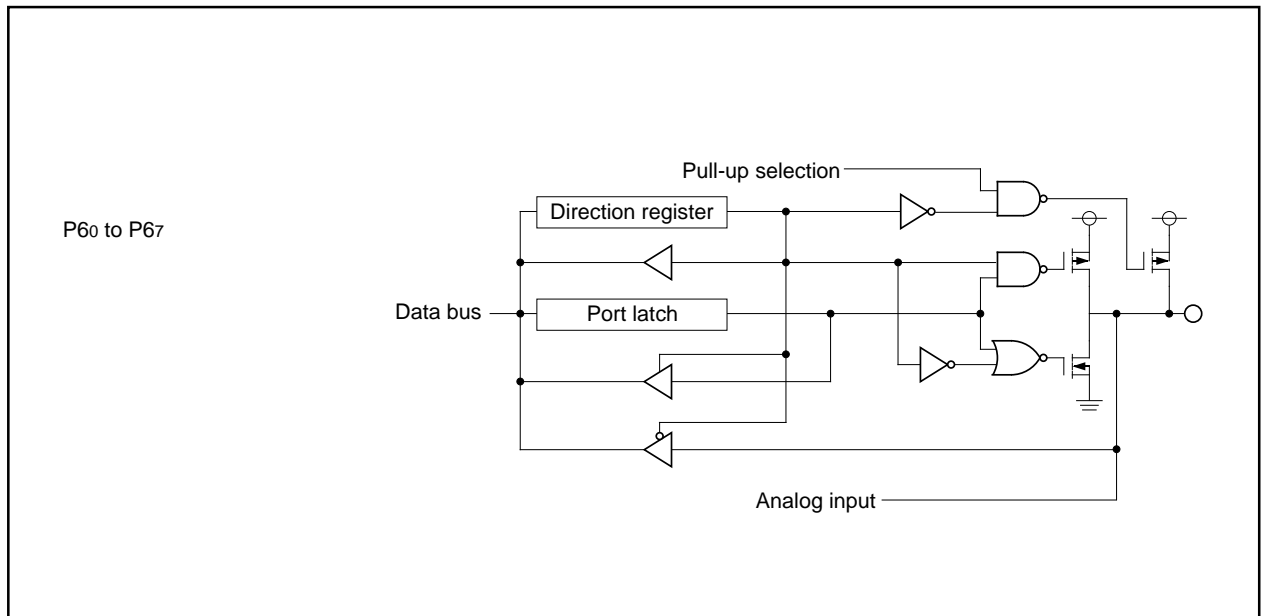


Figure 1.92. Programmable I/O ports (3)

Programmable I/O Port

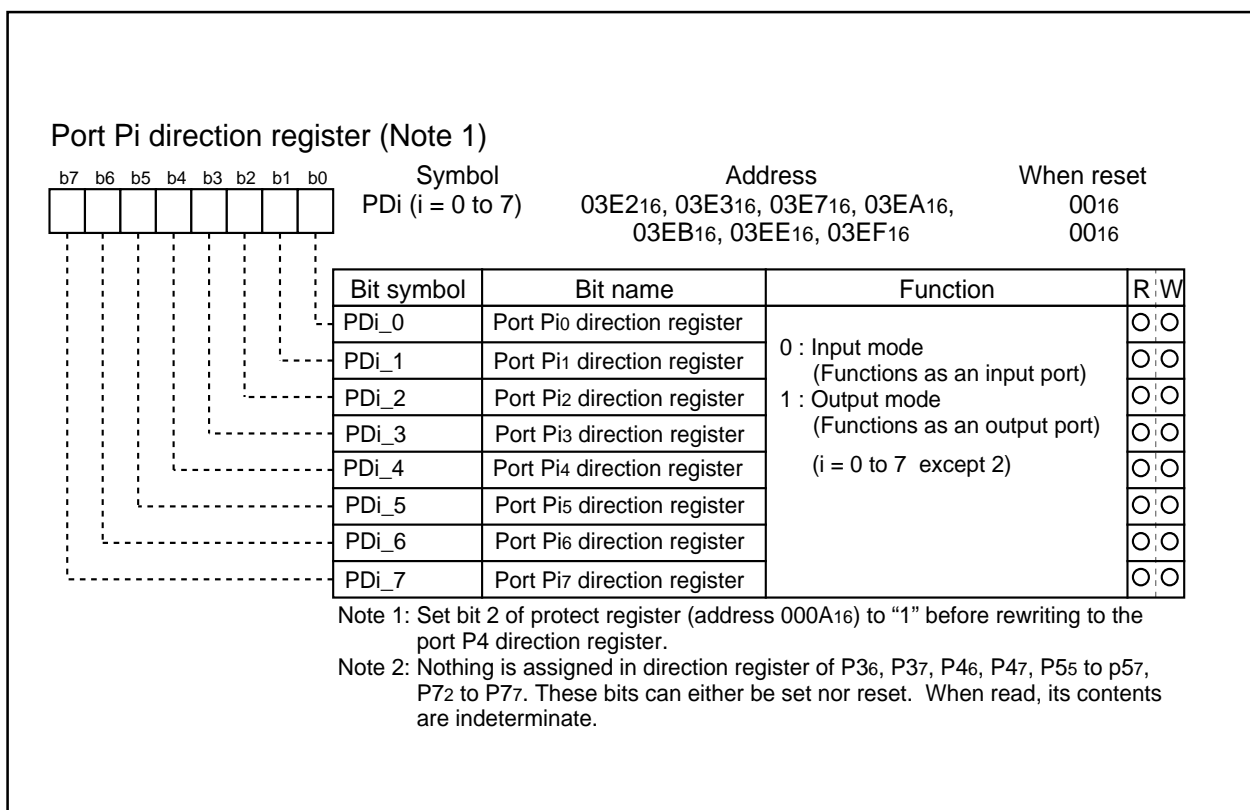


Figure 1.93. Direction register

Programmable I/O Port

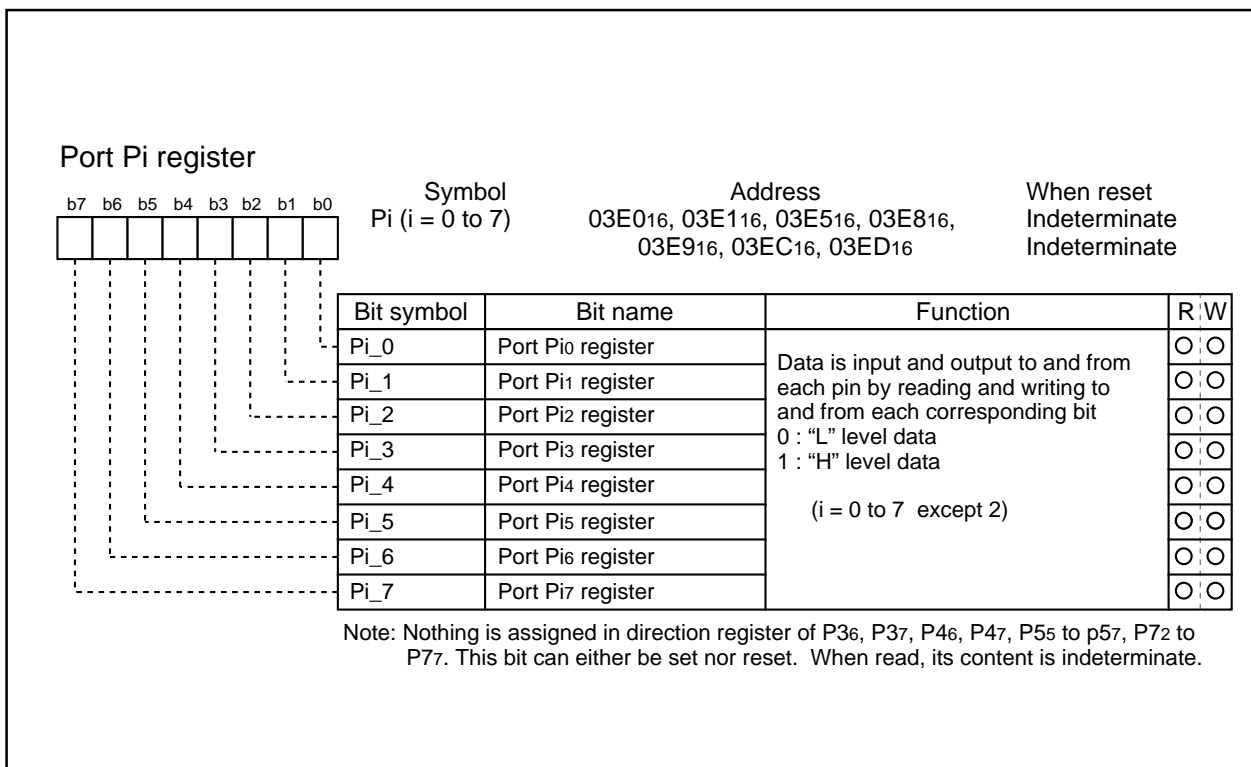


Figure 1.94. Port register

Programmable I/O Port

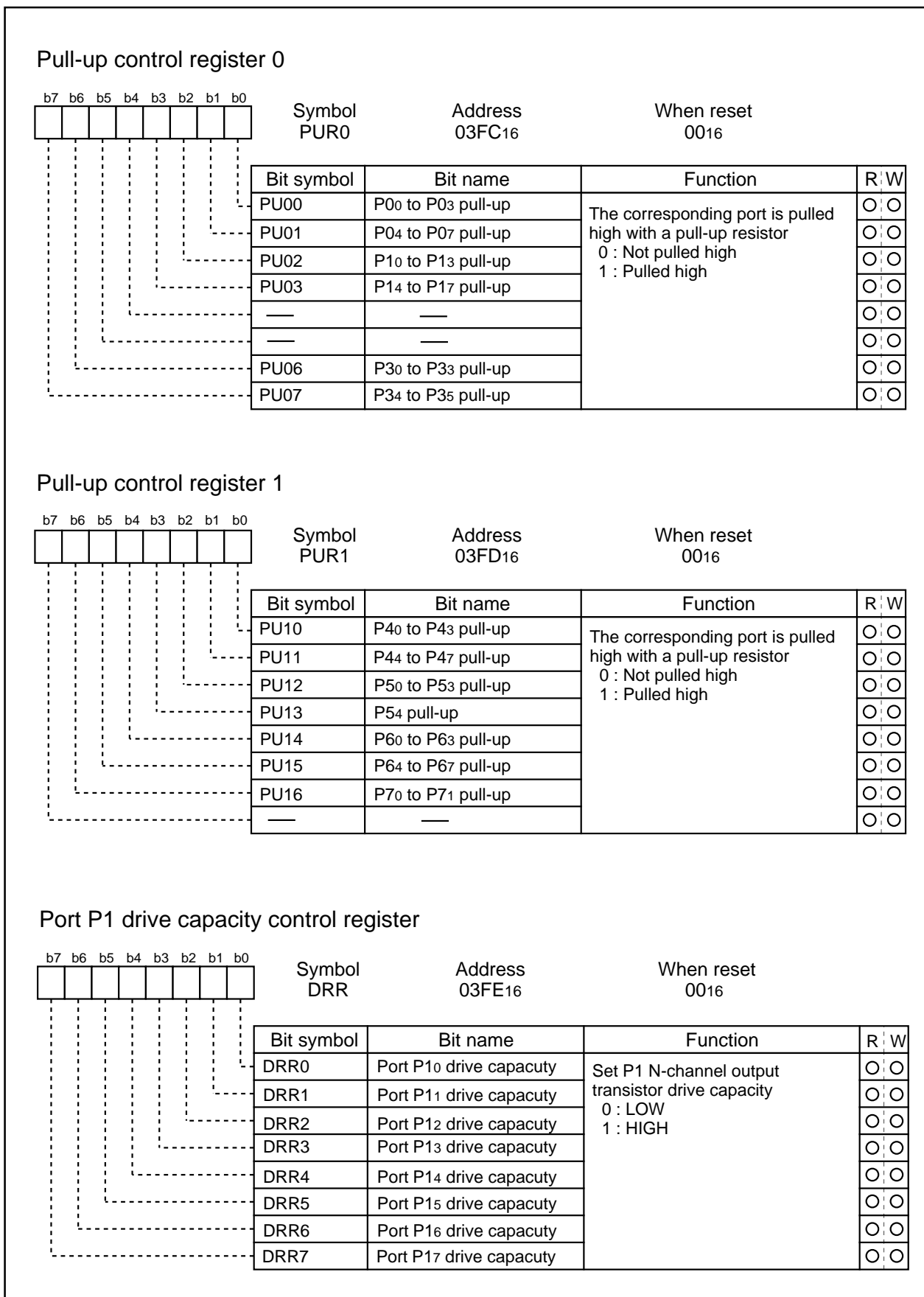


Figure 1.95. Pull-up control register

Programmable I/O Port

Example connection of unused pins**Table 1.36. Example connection of unused pins**

Pin name	Connection
Ports P0, P1, P3 to P7	After setting for input mode, connect every pin to Vss (pull-down); or after setting for output mode, leave these pins open.
XOUT (Note)	Open
AVcc	Connect to Vcc
AVss, VREF	Connect to Vss

Note: With external clock input to XIN pin.

Usage precaution

Usage Precaution**Timer A (timer mode)**

- (1) Reading the timer A0 register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the timer A0 register with the reload timing gets "FFFF₁₆". Reading the timer A0 register after setting a value in the timer A0 register with a count halted but before the counter starts counting gets a proper value.

Timer A (event counter mode)

- (1) Reading the timer A0 register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the timer A0 register with the reload timing gets "FFFF₁₆" by under-flow or "0000₁₆" by overflow. Reading the timer A0 register after setting a value in the timer A0 register with a count halted but before the counter starts counting gets a proper value.
- (2) When stop counting in free run type, set timer again.

Timer A (one-shot timer mode)

- (1) Setting the count start flag to "0" while a count is in progress causes as follows:
- The counter stops counting and a content of reload register is reloaded.
 - The TA0OUT pin outputs "L" level.
 - The interrupt request generated and the timer A0 interrupt request bit goes to "1".
- (2) The timer A0 interrupt request bit goes to "1" if the timer's operation mode is set using any of the following procedures:
- Selecting one-shot timer mode after reset.
 - Changing operation mode from timer mode to one-shot timer mode.
 - Changing operation mode from event counter mode to one-shot timer mode.

Therefore, to use timer A0 interrupt (interrupt request bit), set timer A0 interrupt request bit to "0" after the above listed changes have been made.

Timer A (pulse width modulation mode)

- (1) The timer A0 interrupt request bit becomes "1" if setting operation mode of the timer in compliance with any of the following procedures:
- Selecting PWM mode after reset.
 - Changing operation mode from timer mode to PWM mode.
 - Changing operation mode from event counter mode to PWM mode.

Therefore, to use timer A0 interrupt (interrupt request bit), set timer A0 interrupt request bit to "0" after the above listed changes have been made.

- (2) Setting the count start flag to "0" while PWM pulses are being output causes the counter to stop counting. If the TA0OUT pin is outputting an "H" level in this instance, the output level goes to "L", and the timer A0 interrupt request bit goes to "1". If the TA0OUT pin is outputting an "L" level in this instance, the level does not change, and the timer A0 interrupt request bit does not becomes "1".

Usage precaution

Timer B (timer mode, event counter mode)

- (1) Reading the timer Bi register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the timer Bi register with the reload timing gets "FFFF16". Reading the timer Bi register after setting a value in the timer Bi register with a count halted but before the counter starts counting gets a proper value.

Timer B (pulse period/pulse width measurement mode)

- (1) If changing the measurement mode select bit is set after a count is started, the timer Bi interrupt request bit goes to "1".
- (2) When the first effective edge is input after a count is started, an indeterminate value is transferred to the reload register. At this time, timer Bi interrupt request is not generated.

Timer X (timer mode)

- (1) Reading the timer Xi register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the timer Xi register with the reload timing gets "FFFF16". Reading the timer A0 register after setting a value in the timer Xi register with a count halted but before the counter starts counting gets a proper value.

Timer X (event counter mode)

- (1) Reading the timer Xi register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the timer Xi register with the reload timing gets "FFFF16" by underflow or "000016" by overflow. Reading the timer Xi register after setting a value in the timer Xi register with a count halted but before the counter starts counting gets a proper value.
- (2) When stop counting in free run type, set timer again.

Timer X (one-shot timer mode)

- (1) Setting the count start flag to "0" while a count is in progress causes as follows:
 - The counter stops counting and a content of reload register is reloaded.
 - The TXiINOUT pin outputs "L" level.
 - The interrupt request generated and the timer Xi interrupt request bit goes to "1".
- (2) The timer Xi interrupt request bit goes to "1" if the timer's operation mode is set using any of the following procedures:
 - Selecting one-shot timer mode after reset.
 - Changing operation mode from timer mode to one-shot timer mode.
 - Changing operation mode from event counter mode to one-shot timer mode.

Therefore, to use timer Xi interrupt (interrupt request bit), set timer Xi interrupt request bit to "0" after the above listed changes have been made.

Usage precaution

Timer X (pulse width modulation mode)

(1) The timer Xi interrupt request bit becomes "1" if setting operation mode of the timer in compliance with any of the following procedures:

- Selecting PWM mode after reset.
- Changing operation mode from timer mode to PWM mode.
- Changing operation mode from event counter mode to PWM mode.

Therefore, to use timer Xi interrupt (interrupt request bit), set timer Xi interrupt request bit to "0" after the above listed changes have been made.

(2) Setting the count start flag to "0" while PWM pulses are being output causes the counter to stop counting. If the TXiINOUT pin is outputting an "H" level in this instance, the output level goes to "L", and the timer Xi interrupt request bit goes to "1". If the TXiINOUT pin is outputting an "L" level in this instance, the level does not change, and the timer Xi interrupt request bit does not become "1".

Timer X (pulse period/pulse width measurement mode)

- (1) If changing the measurement mode select bit is set after a count is started, the timer Xi interrupt request bit goes to "1".
- (2) When the first effective edge is input after a count is started, an indeterminate value is transferred to the reload register. At this time, timer Xi interrupt request is not generated.

A-D Converter

(1) Write to each bit (except bit 6) of A-D control register 0, to each bit of A-D control register 1, and to bit 0 of A-D control register 2 when A-D conversion is stopped (before a trigger occurs).

In particular, when the Vref connection bit is changed from "0" to "1", start A-D conversion after an elapse of 1 μ s or longer.

(2) When changing A-D operation mode, select analog input pin again.

(3) Using one-shot mode or single sweep mode

Read the correspondence A-D register after confirming A-D conversion is finished. (It is known by A-D conversion interrupt request bit.)

(4) Using repeat mode, repeat sweep mode 0 or repeat sweep mode 1

Use the undivided main clock as the internal CPU clock.

Stop Mode and Wait Mode

(1) When returning from stop mode by hardware reset, $\overline{\text{RESET}}$ pin must be set to "L" level until main clock oscillation is stabilized.

(2) When shifting to WAIT mode or STOP mode, the program stops after reading 8 bytes from the WAIT instruction and the instruction that sets all clock stop bits to "1" in the instruction queue. Therefore, insert a minimum of 8 NOPs after the WAIT instruction and the instruction that sets all clock stop bits to "1".

(3) When the MCU running in low-speed or low power dissipation mode, do not enter WAIT mode with WAIT peripheral function clock stop bit set to "1".

Interrupts

(1) Reading address 00000₁₆

- When maskable interrupt is occurred, CPU read the interrupt information (the interrupt number and interrupt request level) in the interrupt sequence.

The interrupt request bit of the certain interrupt written in address 00000₁₆ will then be set to "0".

Reading address 00000₁₆ by software sets enabled highest priority interrupt source request bit to "0".

Though the interrupt is generated, the interrupt routine may not be executed.

Do not read address 00000₁₆ by software.

(2) Setting the stack pointer

- The value of the stack pointer immediately after reset is initialized to 0000₁₆. Accepting an interrupt before setting a value in the stack pointer may become a factor of runaway. Be sure to set a value in the stack pointer before accepting an interrupt.

Concerning the first instruction immediately after reset, generating any interrupt is prohibited.

(3) External interrupt

- When changing a polarity of pins $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$, the interrupt request bit may become "1". Clear the interrupt request bit after changing the polarity.

(4) Changing interrupt control register

See "Changing Interrupt Control Register".

Electrical characteristics

Electrical characteristics

Table 1.36. Absolute maximum ratings

Symbol	Parameter	Condition	Rated value	Unit
V _{cc}	Supply voltage		- 0.3 to 6.5 (Note 1)	V
AV _{cc}	Analog supply voltage		- 0.3 to 6.5 (Note 1)	V
V _I	Input voltage RESET, CNV _{ss} , P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P3 ₀ to P3 ₅ , P4 ₀ to P4 ₅ , P5 ₀ to P5 ₄ , P6 ₀ to P6 ₇ , P7 ₀ , P7 ₁ , VREF, XIN		- 0.3 to V _{cc} + 0.3 (Note 2)	V
V _O	Output voltage P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P3 ₀ to P3 ₅ , P4 ₀ to P4 ₅ , P5 ₀ to P5 ₄ , P6 ₀ to P6 ₇ , P7 ₀ , P7 ₁ , VREF, XIN		- 0.3 to V _{cc} + 0.3	V
P _d	Power dissipation	T _a = 25 °C	1000 (Note 3)	mW
T _{opr}	Operating ambient temperature		- 20 to 85 (Note 4)	°C
T _{stg}	Storage temperature		- 40 to 150 (Note 5)	°C

Note 1: Flash memory version: -0.3 to 7 (V) .

Note 2: When writing to flash MCU, CNV_{ss} is -0.3 to 13 (V) .

Note 3: Flat package (56P6S-A) is 300 mW.

Note 4: Extended operating temperature version: -40 to 85 °C. When flash memory version is program/erase mode: 25±5 °C.

Note 5: Extended operating temperature version: -65 to 150 °C.

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Table 1.37. Recommended operating conditions (Note 1)

Symbol	Parameter		Standard			Unit
			Min	Typ.	Max.	
V _{CC}	Supply voltage	Mask ROM version	2.7	5.0	5.5	V
		Flash memory version	4.0	5.0	5.5	
A _V CC	Analog supply voltage			V _{CC}		V
V _{SS}	Supply voltage			0		V
A _V SS	Analog supply voltage			0		V
V _{IH}	HIGH input voltage	P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P3 ₀ to P3 ₅ , P4 ₀ to P4 ₅ , P5 ₀ to P5 ₄ , P6 ₀ to P6 ₇ , P7 ₀ , P7 ₁ , X _{IN} , RESET, CNV _{SS} ,	0.8V _{CC}		V _{CC}	V
V _{IL}	LOW input voltage	P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P3 ₀ to P3 ₅ , P4 ₀ to P4 ₅ , P5 ₀ to P5 ₄ , P6 ₀ to P6 ₇ , P7 ₀ , P7 ₁ , X _{IN} , RESET, CNV _{SS}	0		0.2V _{CC}	V
I _{OH (peak)}	HIGH peak output current	P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P3 ₀ to P3 ₅ , P4 ₀ to P4 ₅ , P5 ₀ to P5 ₄ , P6 ₀ to P6 ₇ , P7 ₀ , P7 ₁			- 10.0	mA
I _{OL (peak)}	LOW peak output current	P0 ₀ to P0 ₇ , P3 ₀ to P3 ₅ , P4 ₀ to P4 ₅ , P5 ₀ to P5 ₄ , P6 ₀ to P6 ₇ , P7 ₀ , P7 ₁			10.0	mA
I _{OL (peak)}	LOW peak output current	P1 ₀ to P1 ₇	HIGHPOWER		30.0	mA
			LOWPOWER		10.0	
I _{OH (avg)}	HIGH average output current	P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P3 ₀ to P3 ₅ , P4 ₀ to P4 ₅ , P5 ₀ to P5 ₄ , P6 ₀ to P6 ₇ , P7 ₀ , P7 ₁			- 5.0	mA
I _{OL (avg)}	LOW average output current	P0 ₀ to P0 ₇ , P3 ₀ to P3 ₅ , P4 ₀ to P4 ₅ , P5 ₀ to P5 ₄ , P6 ₀ to P6 ₇ , P7 ₀ , P7 ₁			5.0	mA
I _{OL (avg)}	LOW average output current	P1 ₀ to P1 ₇	HIGHPOWER		15.0	mA
			LOWPOWER		5.0	
f (X _{IN})	Main clock input oscillation frequency	Mask ROM version	V _{CC} =4.0V to 5.5V	0	10	MHz
			V _{CC} =2.7V to 4.0V	0	5 x V _{CC} - 10.000	MHz
		Flash memory version	V _{CC} =4.0V to 5.5V	0	10	MHz
f (X _{CIN})	Subclock oscillation frequency			32.768	50	kHz

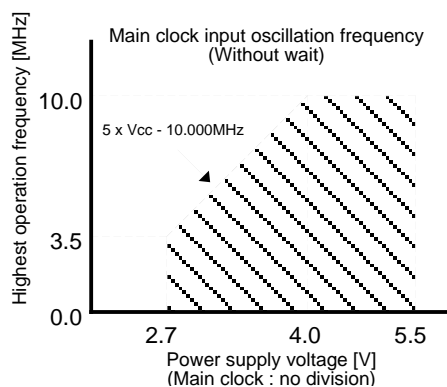
Note 1: Unless otherwise noted: V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 20 to 85°C (Extended operating temperature version:- 40 to 85°C). Flash version: V_{CC} = 4.0V to 5.5V, V_{SS} = 0V, T_a = - 20 to 85°C (Extended operating temperature version:- 40 to 85°C.)

Note 2: The average output current is an average value measured over 100ms.

Note 3: Keep output current as follows:

The sum of port P3 and P4 I_{OL} (peak) is under 40 mA. The sum of port P1 I_{OL} (peak) is under 60 mA. The sum of port P1, P3 and P4 I_{OH} (peak) is under 40 mA. The sum of port P0, P5, P6 and P7 I_{OL} (peak) is under 80 mA. The sum of port P0, P5, P6 and P7 I_{OH} (peak) is under 80 mA.

Note 4: Relationship between main clock oscillation frequency and supply voltage.



Electrical characteristics (V_{CC} = 5V)

V_{CC} = 5V

Table 1.38. Electrical characteristics (Note1)

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
V _{OH}	HIGH output voltage	P00 to P07,P10 to P17,P30 to P35, P40 to P45,P50 to P54,P60 to P67,P70,P71	I _{OH} = - 5 mA	3.0			V
V _{OH}	HIGH output voltage	P00 to P07,P10 to P17,P30 to P35, P40 to P45,P50 to P54,P60 to P67,P70,P71	I _{OH} = - 200 μA	4.7			V
V _{OH}	HIGH output voltage	X _{OUT}	HIGHPOWER	I _{OH} = - 1 mA	3.0		V
			LOWPOWER	I _{OH} = - 0.5 mA	3.0		
V _{OH}	HIGH output voltage	X _{COU} T	HIGHPOWER	No load		3.0	V
			LOWPOWER	No load		1.6	
V _{OL}	LOW output voltage	P00 to P07,P30 to P35,P40 to P45 P50 to P54,P60 to P67,P70,P71	I _{OL} = 5 mA			2.0	V
V _{OL}	LOW output voltage	P00 to P07,P30 to P35,P40 to P45 P50 to P54,P60 to P67,P70,P71	I _{OL} = 200 μA			0.45	V
V _{OL}	LOW output voltage	P10 to P17	HIGHPOWER	I _{OL} = 15mA		2.0	V
			LOWPOWER	I _{OL} = 5 mA		2.0	
V _{OL}	LOW output voltage	P10 to P17	HIGHPOWER	I _{OL} = 200 μA		0.3	V
			LOWPOWER	I _{OL} = 200 μA		0.45	
V _{OL}	LOW output voltage	X _{OUT}	HIGHPOWER	I _{OH} = 1 mA		2.0	V
			LOWPOWER	I _{OH} = 0.5 mA		2.0	
V _{OL}	LOW output voltage	X _{OUT}	HIGHPOWER	No load		0	V
			LOWPOWER	No load		0	
V _{T+} -V _{T-}	Hysteresis	TA0IN,TX0INOUT,TX1INOUT,TX2INOUT TB0IN,TB1IN INT0,INT1,CLK0,KT0 to KT7 RxD0, RxD1		0.2		0.8	V
V _{T+} -V _{T-}	Hysteresis	RESET		0.2		1.8	V
I _{IH}	HIGH input current	P00 to P07,P10 to P17,P30 to P35, P40 to P45,P50 to P54,P60 to P67 P70,P71, RESET, CNVss	V _I = 5V			5.0	μA
I _{IL}	LOW input current	P00 to P07,P10 to P17,P30 to P35, P40 to P45,P50 to P54,P60 to P67, P70,P71, RESET, CNVss	V _I = 0V			-5.0	μA
R _{PULLUP}	Pull-up resistor	P00 to P07,P10 to P17,P30 to P35, P40 to P45,P50 to P54,P60 to P67,P70,P71	V _I = 0V	30.0	50.0	167.0	kΩ
R _{XIN}	Feedback resistor	X _{IN}			1.0		MΩ
R _{X_{CIN}}	Feedback resistor	X _{CIN}			6.0		MΩ
V _{RAM}	RAM retention voltage		When clock is stopped	2.0			V
I _{CC}	Power supply current	I/O pin has no load	f(X _{IN})=10MHz Square wave, no division		19.0	38.0	mA
			f(X _{CIN})=32kHz Square wave		90.0		μA
			f(X _{CIN})=32kHz When a WAIT instruction is executed (Note 2)		4.0		μA
			T _a =25°C when clock is stopped			1.0	μA
			T _a =85°C when clock is stopped			20.0	

Note 1: Unless otherwise noted: V_{CC} = 5V, V_{SS} = 0V at T_a = -20 to 85°C, f(X_{IN}) = 10MHz

(Extended operating temperature version; -40 to 85°C)

Note 2: With one timer operated using fc32.

Electrical characteristics ($V_{CC} = 5V$)

$V_{CC} = 5V$

Table 1.39. A-D conversion characteristics (Note)

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		$V_{REF} = V_{CC}$			10	Bits
–	Absolute accuracy	Sample & hold function not available	$V_{REF} = V_{CC} = 5V$			± 3	LSB
		Sample & hold function available(10bit)	$V_{REF} = V_{CC} = 5V$			± 3	LSB
		Sample & hold function available(8bit)	$V_{REF} = V_{CC} = 5V$			± 2	LSB
R_{LADDER}	Ladder resistance		$V_{REF} = V_{CC}$	10		40	kohm
t_{CONV}	Conversion time(10bit)			3.3			μs
t_{CONV}	Conversion time(8bit)			2.8			μs
t_{SAMP}	Sampling time			0.3			μs
V_{REF}	Reference voltage			2		V_{CC}	V
V_{IA}	Analog input voltage			0		V_{REF}	V

Note : Unless otherwise noted: $V_{CC} = AV_{CC} = V_{REF} = 5V$, $V_{SS} = AV_{SS} = 0V$ at $T_a = -25^{\circ}C$, $f(X_{IN}) = 10MHz$

Electrical characteristics ($V_{CC} = 5V$)

$V_{CC} = 5V$

Timing requirements (referenced to $V_{CC} = 5V$, $V_{SS} = 0V$ at $T_a = -20$ to $85^{\circ}C^{(*)}$ unless otherwise specified)

* Extended operating temperature version; -40 to $85^{\circ}C$

Table 1.40. External clock input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	100		ns
$t_{w(H)}$	External clock input HIGH pulse width	40		ns
$t_{w(L)}$	External clock input LOW pulse width	40		ns
t_r	External clock rise time		15	ns
t_f	External clock fall time		15	ns

Table 1.41. Timer A input (counter input in event counter mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TA0IN input cycle time	100		ns
$t_{w(TAH)}$	TA0IN input HIGH pulse width	40		ns
$t_{w(TAL)}$	TA0IN input LOW pulse width	40		ns

Table 1.42. Timer A input (gating input in timer mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TA0IN input cycle time	400		ns
$t_{w(TAH)}$	TA0IN input HIGH pulse width	200		ns
$t_{w(TAL)}$	TA0IN input LOW pulse width	200		ns

Table 1.43. Timer A input (external trigger input in one-shot timer mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TA0IN input cycle time	200		ns
$t_{w(TAH)}$	TA0IN input HIGH pulse width	100		ns
$t_{w(TAL)}$	TA0IN input LOW pulse width	100		ns

Table 1.44. Timer A input (external trigger input in pulse width modulation mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TA0IN input HIGH pulse width	100		ns
$t_{w(TAL)}$	TA0IN input LOW pulse width	100		ns

Table 1.45. Timer A input (up/down input in event counter mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TA0OUT input cycle time	2000		ns
$t_{w(UPH)}$	TA0OUT input HIGH pulse width	1000		ns
$t_{w(UPL)}$	TA0OUT input LOW pulse width	1000		ns
$t_{su(UP-TIN)}$	TA0OUT input setup time	400		ns
$t_{h(TIN-UP)}$	TA0OUT input hold time	400		ns

Electrical characteristics ($V_{CC} = 5V$)

$V_{CC} = 5V$

Timing requirements (referenced to $V_{CC} = 5V$, $V_{SS} = 0V$ at $T_a = -20$ to $85^{\circ}C^{(*)}$ unless otherwise specified)

* Extended operating temperature version; -40 to $85^{\circ}C$

Table 1.46. Timer B input (counter input in event counter mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on both edges)	80		ns

Table 1.47. Timer B input (pulse period measurement mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	200		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	200		ns

Table 1.48. Timer B input (pulse width measurement mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	200		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	200		ns

Table 1.49. Timer X input (counter input in event counter mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TX)}$	TXiINOUT input cycle time	100		ns
$t_{w(TXH)}$	TXiINOUT input HIGH pulse width	40		ns
$t_{w(TXL)}$	TXiINOUT input LOW pulse width	40		ns

Table 1.50. Timer X input (gate input in timer mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TX)}$	TXiINOUT input cycle time	400		ns
$t_{w(TXH)}$	TXiINOUT input HIGH pulse width	200		ns
$t_{w(TXL)}$	TXiINOUT input LOW pulse width	200		ns

Table 1.51. Timer X input (external trigger input in one-shot timer mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TX)}$	TXiINOUT input cycle time	200		ns
$t_{w(TXH)}$	TXiINOUT input HIGH pulse width	100		ns
$t_{w(TXL)}$	TXiINOUT input LOW pulse width	100		ns

Electrical characteristics ($V_{CC} = 5V$)

$V_{CC} = 5V$

Timing requirements (referenced to $V_{CC} = 5V$, $V_{SS} = 0V$ at $T_a = -20$ to $85^{\circ}C^{(*)}$ unless otherwise specified)

* Extended operating temperature version; -40 to $85^{\circ}C$

Table 1.52. Timer X input (pulse period measurement mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TX)}$	TXiINOUT input cycle time	400		ns
$t_{w(TXH)}$	TXiINOUT input HIGH pulse width	200		ns
$t_{w(TXL)}$	TXiINOUT input LOW pulse width	200		ns

Table 1.53. Timer X input (pulse width measurement mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TX)}$	TXiINOUT input cycle time	400		ns
$t_{w(TXH)}$	TXiINOUT input HIGH pulse width	200		ns
$t_{w(TXL)}$	TXiINOUT input LOW pulse width	200		ns

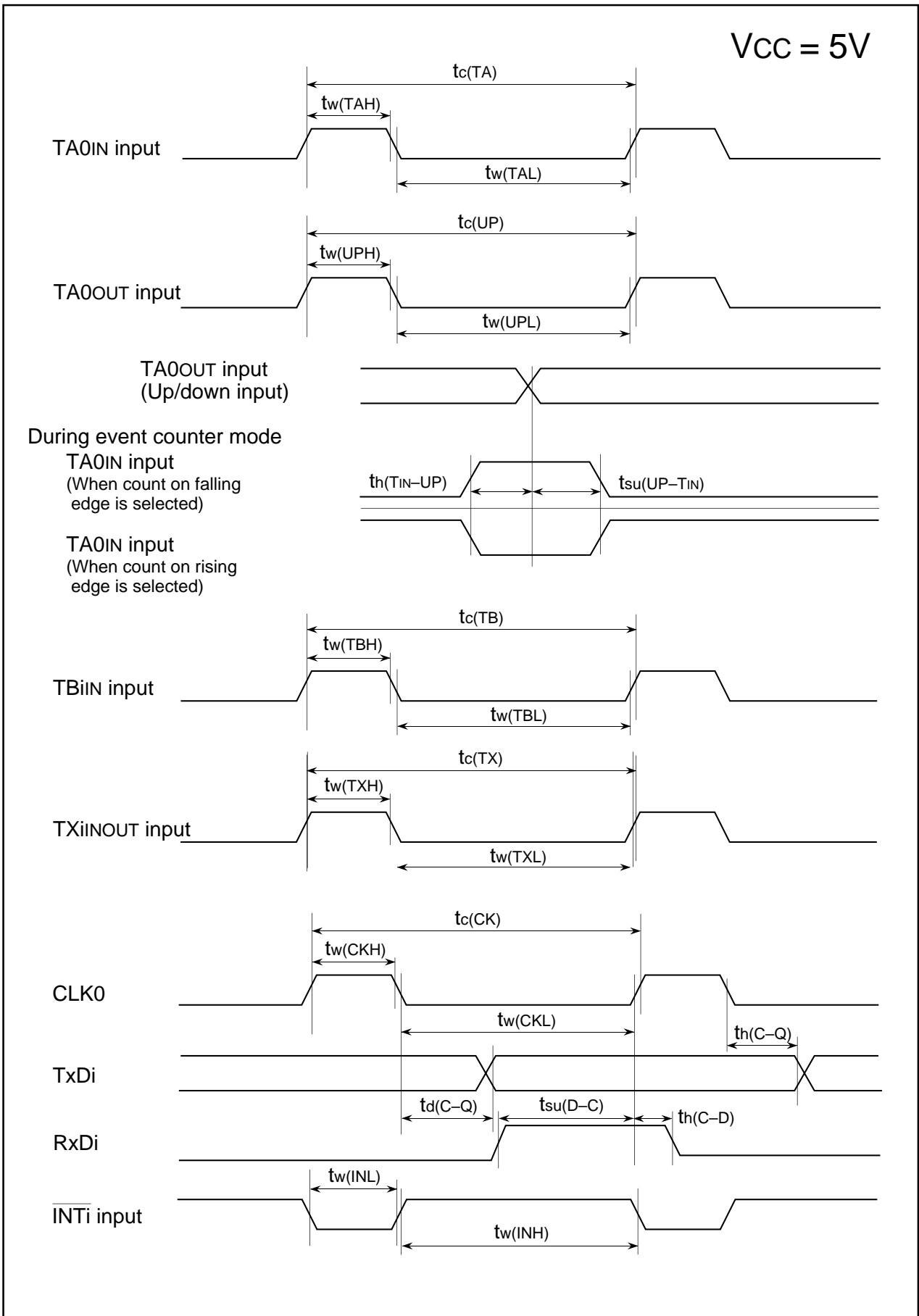
Table 1.54. Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	200		ns
$t_{w(CKH)}$	CLK0 input HIGH pulse width	100		ns
$t_{w(CKL)}$	CLK0 input LOW pulse width	100		ns
$t_{d(C-Q)}$	TxDi output delay time		80	ns
$t_{h(C-Q)}$	TxDi hold time	0		ns
$t_{su(D-C)}$	RxDi input setup time	30		ns
$t_{h(C-D)}$	RxDi input hold time	90		ns

Table 1.55. External interrupt \overline{INTi} inputs

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	\overline{INTi} input HIGH pulse width	250		ns
$t_{w(INL)}$	\overline{INTi} input LOW pulse width	250		ns

Electrical characteristics ($V_{CC} = 5V$)



Electrical characteristics (V_{CC} = 3V)V_{CC} = 3V

Table 1.56. Electrical characteristics (Note 1)

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
V _{OH}	HIGH output voltage	P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P3 ₀ to P3 ₅ , P4 ₀ to P4 ₅ , P5 ₀ to P5 ₄ , P6 ₀ to P6 ₇ , P7 ₀ , P7 ₁	I _{OH} = - 1 mA	2.5			V
V _{OH}	HIGH output voltage	X _{OUT}	HIGHPOWER	I _{OH} = - 1 mA	2.5		V
			LOWPOWER	I _{OH} = - 50 μA	2.5		
V _{OH}	HIGH output voltage	X _{COU} T	HIGHPOWER	No load		3.0	V
			LOWPOWER	No load		1.6	
V _{OL}	LOW output voltage	P0 ₀ to P0 ₇ , P3 ₀ to P3 ₅ , P4 ₀ to P4 ₅ P5 ₀ to P5 ₄ , P6 ₀ to P6 ₇ , P7 ₀ , P7 ₁	I _{OL} = 1 mA			0.5	V
V _{OL}	LOW output voltage	P1 ₀ to P1 ₇	HIGHPOWER	I _{OL} = 3 mA		0.5	V
			LOWPOWER	I _{OL} = 1 mA		0.5	
V _{OL}	LOW output voltage	X _{OUT}	HIGHPOWER	I _{OH} = 0.1 mA		0.5	V
			LOWPOWER	I _{OH} = 50 μA		0.5	
V _{OL}	LOW output voltage	X _{OUT}	HIGHPOWER	No load		0	V
			LOWPOWER	No load		0	
V _{T+} -V _{T-}	Hysteresis	TA0 _{IN} , TX0 _{INOUT} , TX1 _{INOUT} , TX2 _{INOUT} TB0 _{IN} , TB1 _{IN} INT ₀ , INT ₁ , CLK ₀ , KI ₀ to KI ₇ RxD ₀ , RxD ₁		0.2		0.8	V
V _{T+} -V _{T-}	Hysteresis	RESET		0.2		1.8	V
I _{IH}	HIGH input current	P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P3 ₀ to P3 ₅ , P4 ₀ to P4 ₅ , P5 ₀ to P5 ₄ , P6 ₀ to P6 ₇ , P7 ₀ , P7 ₁ , RESET, CNV _{SS}	V _I = 3V			4.0	μA
I _{IL}	LOW input current	P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P3 ₀ to P3 ₅ , P4 ₀ to P4 ₅ , P5 ₀ to P5 ₄ , P6 ₀ to P6 ₇ , P7 ₀ , P7 ₁ , RESET, CNV _{SS}	V _I = 0V			-4.0	μA
R _{PULLUP}	Pull-up resistor	P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P3 ₀ to P3 ₅ , P4 ₀ to P4 ₅ , P5 ₀ to P5 ₄ , P6 ₀ to P6 ₇ , P7 ₀ , P7 ₁	V _I = 0V	66.0	120.0	500.0	kΩ
R _{XIN}	Feedback resistor	X _{IN}			3.0		MΩ
R _{XIN}	Feedback resistor	X _{IN}			10.0		MΩ
V _{RAM}	RAM retention voltage		When clock is stopped	2.0			V
I _{CC}	Power supply current	I/O pin has no load	f(X _{IN})=3.5MHz Square wave, no division		3.5	7.0	mA
			f(X _{CIN})=32kHz Square wave		40.0		μA
			f(X _{CIN})=32kHz When a WAIT instruction is executed Oscillation capacity HIGH (Note 2)		2.8		μA
			f(X _{CIN})=32kHz When a WAIT instruction is executed Oscillation capacity LOW (Note 2)		0.9		μA
			Ta=25°C when clock is stopped			1.0	μA
			Ta=85°C when clock is stopped			20.0	

Note 1: Unless otherwise noted: V_{CC} = 3V, V_{SS} = 0V at Ta = -20 to 85°C, f(X_{IN}) = 3.5MHz)
(Extended operating temperature version; -40 to 85°C)

Note 2: With one timer operated using fc32.

Electrical characteristics ($V_{CC} = 3V$)

$V_{CC} = 3V$

Table 1.57. A-D conversion characteristics (Note)

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		$V_{REF} = V_{CC}$			10	Bits
–	Absolute accuracy	Sample & hold function not available (8bit)	$V_{REF} = V_{CC} = 3V$, $\emptyset_{AD} = f_{AD}$			± 2	LSB
R_{LADDER}	Ladder resistance		$V_{REF} = V_{CC}$	10		40	kohm
t_{CONV}	Conversion time(8bit)			14.0			μs
V_{REF}	Reference voltage			2.7		V_{CC}	V
V_{IA}	Analog input voltage			0		V_{REF}	V

Note : Unless otherwise noted: $V_{CC} = AV_{CC} = V_{REF} = 3V$, $V_{SS} = AV_{SS} = 0V$ at $T_a = 25^\circ C$, $f(XIN) = 3.5MHz$.

Electrical characteristics ($V_{CC} = 3V$) $V_{CC} = 3V$

Timing requirements (referenced to $V_{CC} = 3V$, $V_{SS} = 0V$ at $T_a = -20$ to $85^{\circ}C^{(*)}$ unless otherwise specified)

* Extended operating temperature version; -40 to $85^{\circ}C$

Table 1.58. External clock input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	286		ns
$t_{w(H)}$	External clock input HIGH pulse width	120		ns
$t_{w(L)}$	External clock input LOW pulse width	120		ns
t_r	External clock rise time		18	ns
t_f	External clock fall time		18	ns

Table 1.59. Timer A input (counter input in event counter mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(TA)$	TA0IN input cycle time	300		ns
$t_{w(TAH)}$	TA0IN input HIGH pulse width	120		ns
$t_{w(TAL)}$	TA0IN input LOW pulse width	120		ns

Table 1.60. Timer A input (gating input in timer mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(TA)$	TA0IN input cycle time	1200		ns
$t_{w(TAH)}$	TA0IN input HIGH pulse width	600		ns
$t_{w(TAL)}$	TA0IN input LOW pulse width	600		ns

Table 1.61. Timer A input (external trigger input in one-shot timer mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(TA)$	TA0IN input cycle time	600		ns
$t_{w(TAH)}$	TA0IN input HIGH pulse width	300		ns
$t_{w(TAL)}$	TA0IN input LOW pulse width	300		ns

Table 1.62. Timer A input (external trigger input in pulse width modulation mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TA0IN input HIGH pulse width	300		ns
$t_{w(TAL)}$	TA0IN input LOW pulse width	300		ns

Table 1.63. Timer A input (up/down input in event counter mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(UP)$	TA0OUT input cycle time	6000		ns
$t_{w(UPH)}$	TA0OUT input HIGH pulse width	3000		ns
$t_{w(UPL)}$	TA0OUT input LOW pulse width	3000		ns
$t_{su}(UP-TIN)$	TA0OUT input setup time	1200		ns
$t_h(TIN-UP)$	TA0OUT input hold time	1200		ns

Electrical characteristics ($V_{CC} = 3V$) $V_{CC} = 3V$

Timing requirements (referenced to $V_{CC} = 3V$, $V_{SS} = 0V$ at $T_a = -20$ to $85^{\circ}C^{(*)}$ unless otherwise specified)

* Extended operating temperature version; -40 to $85^{\circ}C$

Table 1.64. Timer B input (counter input in event counter mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	300		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on one edge)	120		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on one edge)	120		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	600		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on both edges)	320		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on both edges)	320		ns

Table 1.65. Timer B input (pulse period measurement mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	1200		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	600		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	600		ns

Table 1.66. Timer B input (pulse width measurement mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	1200		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	600		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	600		ns

Table 1.67. Timer X input (counter input in event counter mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TX)}$	TXiINOUT input cycle time	300		ns
$t_{w(TXH)}$	TXiINOUT input HIGH pulse width	120		ns
$t_{w(TXL)}$	TXiINOUT input LOW pulse width	120		ns

Table 1.68. Timer X input (gate input in timer mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TX)}$	TXiINOUT input cycle time	1200		ns
$t_{w(TXH)}$	TXiINOUT input HIGH pulse width	600		ns
$t_{w(TXL)}$	TXiINOUT input LOW pulse width	600		ns

Table 1.69. Timer X input (external trigger input in one-shot timer mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TX)}$	TXiINOUT input cycle time	600		ns
$t_{w(TXH)}$	TXiINOUT input HIGH pulse width	300		ns
$t_{w(TXL)}$	TXiINOUT input LOW pulse width	300		ns

Electrical characteristics ($V_{CC} = 3V$) $V_{CC} = 3V$

Timing requirements (referenced to $V_{CC} = 3V$, $V_{SS} = 0V$ at $T_a = -20$ to $85^{\circ}C^{(*)}$ unless otherwise specified)

* Extended operating temperature version; -40 to $85^{\circ}C$

Table 1.70. Timer X input (pulse period measurement mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(TX)$	TXiINOUT input cycle time	1200		ns
$t_w(TXH)$	TXiINOUT input HIGH pulse width	600		ns
$t_w(TXL)$	TXiINOUT input LOW pulse width	600		ns

Table 1.71. Timer X input (pulse width measurement mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(TX)$	TXiINOUT input cycle time	1200		ns
$t_w(TXH)$	TXiINOUT input HIGH pulse width	600		ns
$t_w(TXL)$	TXiINOUT input LOW pulse width	600		ns

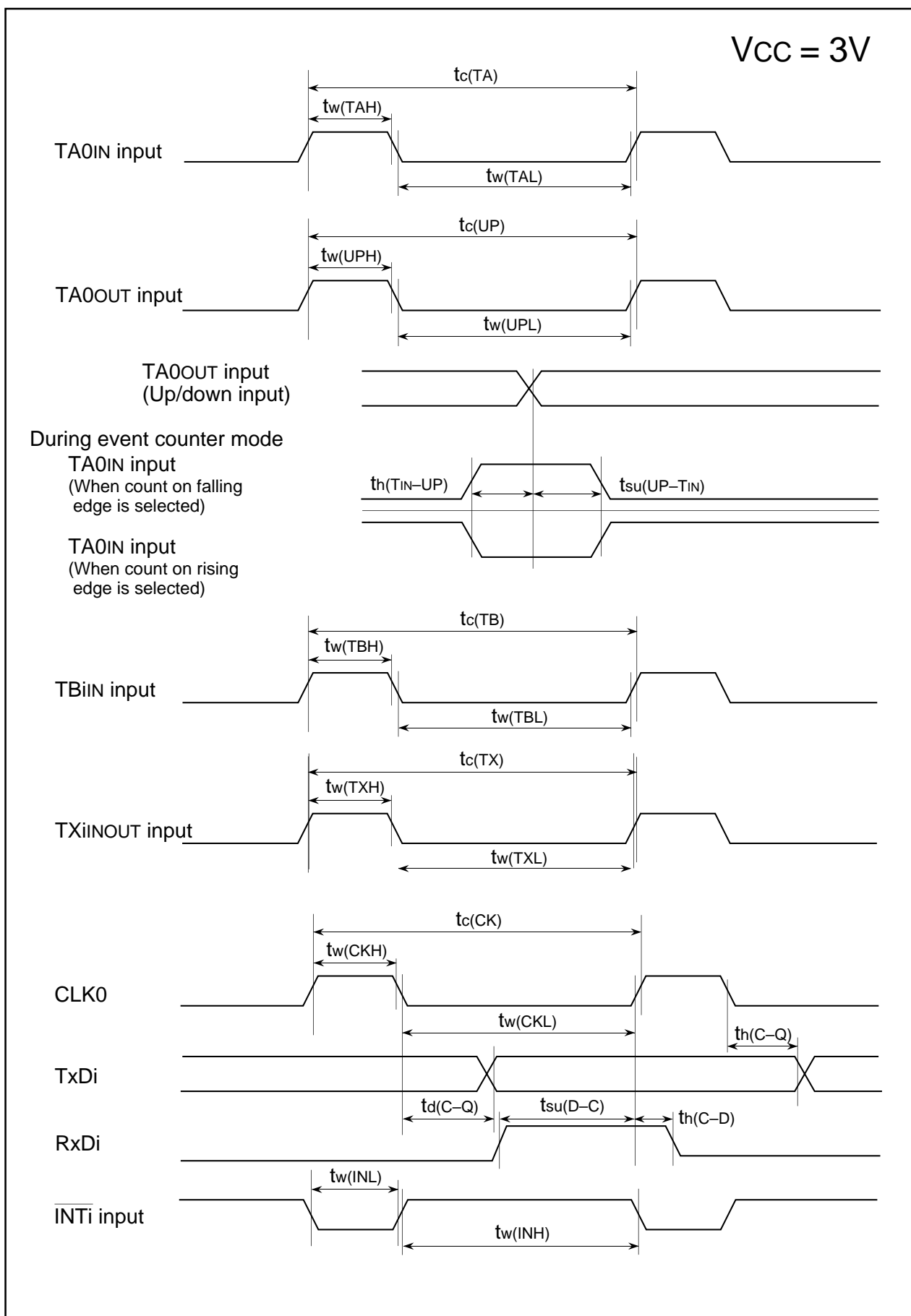
Table 1.72. Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(CK)$	CLK0 input cycle time	300		ns
$t_w(CKH)$	CLK0 input HIGH pulse width	150		ns
$t_w(CKL)$	CLK0 input LOW pulse width	150		ns
$t_d(C-Q)$	TxDi output delay time		160	ns
$t_h(C-Q)$	TxDi hold time	0		ns
$t_{su}(D-C)$	RxDi input setup time	50		ns
$t_h(C-D)$	RxDi input hold time	90		ns

Table 1.73. External interrupt \overline{INT}_i inputs

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_w(INH)$	\overline{INT}_i input HIGH pulse width	380		ns
$t_w(INL)$	\overline{INT}_i input LOW pulse width	380		ns

Electrical characteristics ($V_{CC} = 3V$)



Description (Flash memory version)

Outline Performance

Table 1.74 shows the outline performance of the M30201 (flash memory version).

Table 1.74. Outline Performance of the M30201 (flash memory version)

Item		Performance
Power supply voltage		4.0V to 5.5 V (f(XIN)=10MHz)
Program/erase voltage		VPP=12V \pm 5% (f(XIN)=10MHz, Ta=25 \pm 5°C)
		VCC=5V \pm 10% (f(XIN)=10MHz, Ta=25 \pm 5°C)
Flash memory operation mode		Three modes (parallel I/O, standard serial I/O, CPU rewrite)
Erase block division	User ROM area	See Figure 1.96
	Boot ROM area	One division (3.5 Kbytes) (Note)
Program method		In units of byte
Erase method		Collective erase
Program/erase control method		Program/erase control by software command
Number of commands		6 commands
Program/erase count		100 times
ROM code protect		Parallel I/O mode is supported.

Note: The boot ROM area contains a standard serial I/O mode control program which is stored in it when shipped from the factory. This area can be erased and programmed in only parallel I/O mode.

Description (Flash memory version)

Flash Memory

The M30201 (flash memory version) contains the NOR type of flash memory that requires a high-voltage VPP power supply for program/erase operations, in addition to the VCC power supply for device operation. For this flash memory, three flash memory modes are available in which to read, program, and erase: parallel I/O and standard serial I/O modes in which the flash memory can be manipulated using a programmer and a CPU rewrite mode in which the flash memory can be manipulated by the Central Processing Unit (CPU). Each mode is detailed in the pages to follow.

In addition to the ordinary user ROM area to store a microcomputer operation control program, the flash memory has a boot ROM area that is used to store a program to control rewriting in CPU rewrite and standard serial I/O modes. This boot ROM area has had a standard serial I/O mode control program stored in it when shipped from the factory. However, the user can write a rewrite control program in this area that suits the user's application system. This boot ROM area can be rewritten in only parallel I/O mode.

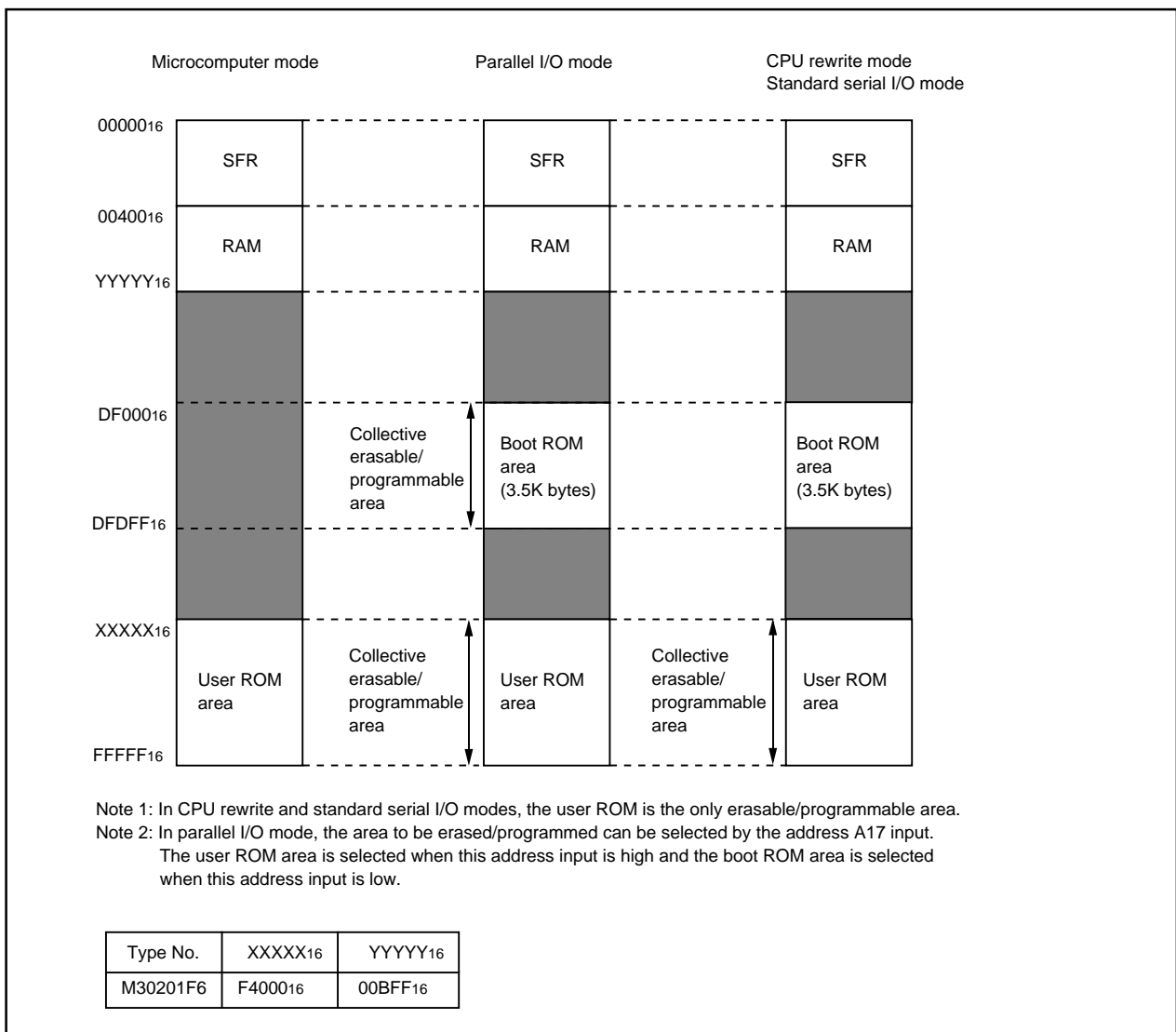


Figure 1.96. Block diagram of flash memory version

CPU Rewrite Mode (Flash memory version)

CPU Rewrite Mode

In CPU rewrite mode, the on-chip flash memory can be operated on (read, program, or erase) under control of the Central Processing Unit (CPU). In CPU rewrite mode, the flash memory can be operated on by reading or writing to the flash memory control register and flash command register. Figure 1.97, Figure 1.98 show the flash memory control register, and flash command register respectively.

Also, in CPU rewrite mode, the CNVSS pin is used as the VPP power supply pin. Apply the power supply voltage, VPPH, from an external source to this pin.

In CPU rewrite mode, only the user ROM area shown in Figure 1.96 can be rewritten; the boot ROM area cannot be rewritten. Make sure the program and block commands are issued for only the user ROM area. The control program for CPU rewrite mode can be stored in either user ROM or boot ROM area. In the CPU rewrite mode, because the flash memory cannot be read from the CPU, the rewrite control program must be transferred to internal RAM before it can be executed.

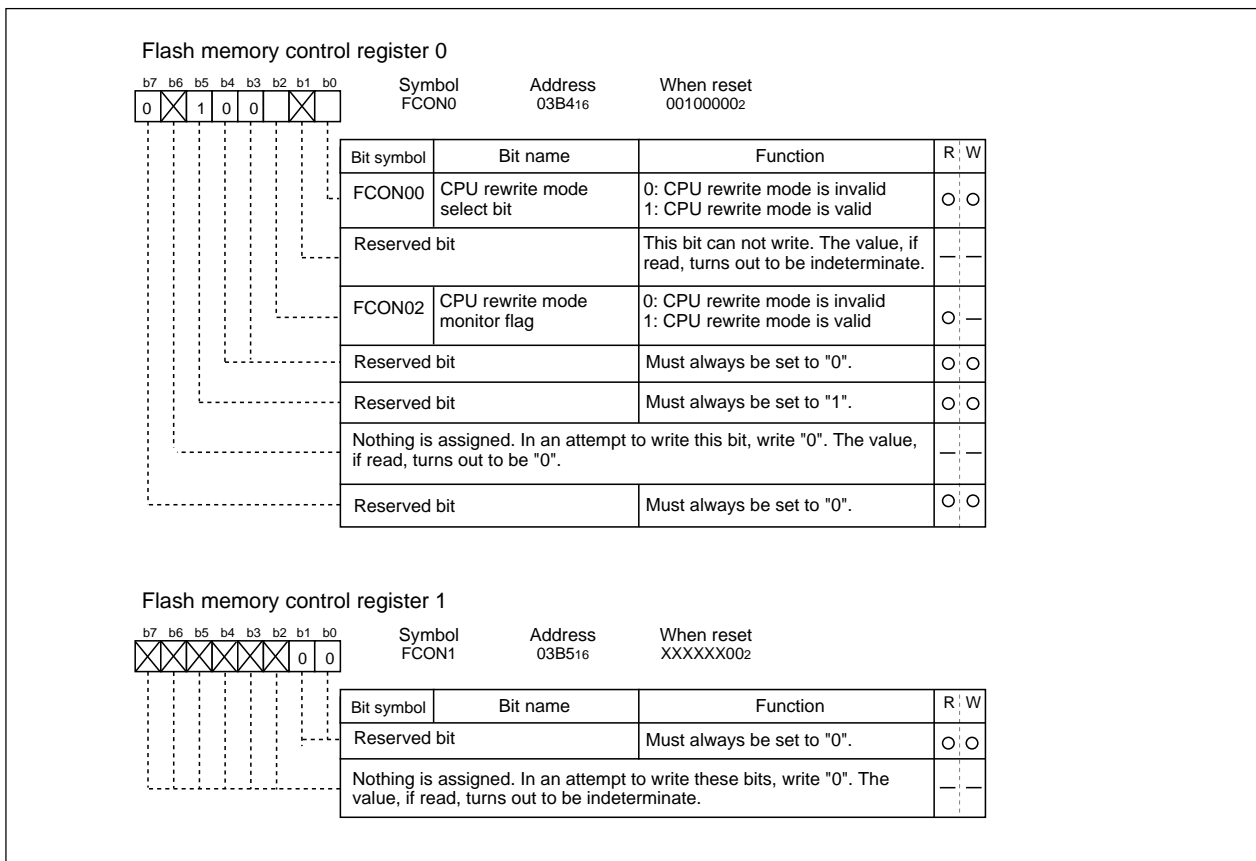


Figure 1.97. Flash memory control register

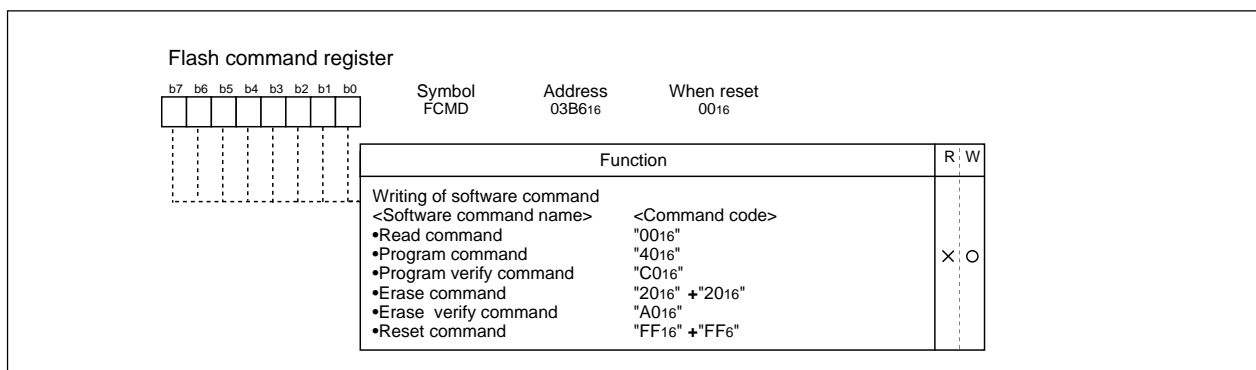


Figure 1.98. Flash command register

CPU Rewrite Mode (Flash memory version)

Microcomputer Mode and Boot Mode

The control program for CPU rewrite mode must be written into the user ROM or boot ROM area in parallel I/O mode beforehand. (If the control program is written into the boot ROM area, the standard serial I/O mode becomes unusable.)

See Figure 1.96 for details about the boot ROM area.

Normal microcomputer mode is entered when the microcomputer is reset with pulling CNVSS pin low (Vss). In this case, the CPU starts operating using the control program in the user ROM area.

When the microcomputer is reset by pulling the P52 pin high (VCC), the CNVSS pin high (VPPH), the CPU starts operating using the control program in the boot ROM area. This mode is called the "boot" mode.

The control program in the boot ROM area can also be used to rewrite the user ROM area.

CPU rewrite mode operation procedure

The internal flash memory can be operated on to program, read, verify, or erase it while being placed on-board by writing commands from the CPU to the flash memory control register (addresses 03B416, 03B516) and flash command register (address 03B616). Note that when in CPU rewrite mode, the boot ROM area cannot be accessed for program, read, verify, or erase operations. Before this can be accomplished, a CPU write control program must be written into the boot ROM area in parallel input/output mode. The following shows a CPU rewrite mode operation procedure.

<Start procedure (Note 1)>

- (1) Apply VPPH to the CNVSS/VPP pin and VCC to the port P52 pin for reset release. Or the user can jump from the user ROM area to the boot ROM area using the JMP instruction and execute the CPU write control program. In this case, set the CPU write mode select bit of the flash memory control register to "1" before applying VPPH to the CNVSS/VPP pin.
- (2) After transferring the CPU write control program from the boot ROM area to the internal RAM, jump to this control program in RAM. (The operations described below are controlled by this program.)
- (3) Set the CPU rewrite mode select bit to "1".
- (4) Read the CPU rewrite mode monitor flag to see that the CPU rewrite mode is enabled.
- (5) Execute operation on the flash memory by writing software commands to the flash command register.

Note 1: In addition to the above, various other operations need to be performed, such as for entering the data to be written to flash memory from an external source (e.g., serial I/O), initializing the ports, and writing to the watchdog timer.

<Clearing procedure>

- (1) Apply VSS to the CNVSS/VPP pin.
- (2) Set the CPU rewrite mode select bit to "0".

CPU Rewrite Mode (Flash memory version)

Precautions on CPU Rewrite Mode

Described below are the precautions to be observed when rewriting the flash memory in CPU rewrite mode.

(1) Operation speed

During erase/program mode, set BCLK to 5 MHz or less by changing the divide ratio.

(2) Instructions inhibited against use

The instructions listed below cannot be used during CPU rewrite mode because they refer to the internal data of the flash memory:

UND instruction, INTO instruction, JMPS instruction, JSRS instruction, and BRK instruction

(3) Interrupts inhibited against use

No interrupts can be used that look up the fixed vector table in the flash memory area. Maskable interrupts may be used by setting the interrupt vector table in a location outside the flash memory area.

CPU Rewrite Mode (Flash memory version)

Software Commands

Table 1.75 lists the software commands available with the M30201 (flash memory version).

When CPU rewrite mode is enabled, write software commands to the flash command register to specify the operation to erase or program.

The content of each software command is explained below.

Table 1.75. List of Software Commands (CPU Rewrite Mode)

Command	First bus cycle			Second bus cycle		
	Mode	Address	Data (D ₀ to D ₇)	Mode	Address	Data (D ₀ to D ₇)
Read	Write	03B6 ₁₆	00 ₁₆			
Program	Write	03B6 ₁₆	40 ₁₆	Write	Program address	Program data
Program verify	Write	03B6 ₁₆	C0 ₁₆	Read	Verify address	Verify data
Erase	Write	03B6 ₁₆	20 ₁₆	Write	03B6 ₁₆	20 ₁₆
Erase verify	Write	03B6 ₁₆	A0 ₁₆	Read	Verify address	Verify data
Reset	Write	03B6 ₁₆	FF ₁₆	Write	03B6 ₁₆	FF ₁₆

Read Command (00₁₆)

The read mode is entered by writing the command code “00₁₆” to the flash command register in the first bus cycle. When an address to be read is input in one of the bus cycles that follow, the content of the specified address is read out at the data bus (D₀–D₇), 8 bits at a time.

The read mode is retained intact until another command is written.

After reset and after the reset command is executed, the read mode is set.

Program Command (40₁₆)

The program mode is entered by writing the command code “40₁₆” to the flash command register in the first bus cycle. When the user execute an instruction to write byte data to the desired address (e.g., STE instruction) in the second bus cycle, the flash memory control circuit executes the program operation. The program operation requires approximately 20 μs. Wait for 20 μs or more before the user go to the next processing.

During program operation, the watchdog timer remains idle, with the value “7FFF₁₆” set in it.

Note 1: The write operation is not completed immediately by writing a program command once. The user must always execute a program-verify command after each program command executed. And if verification fails, the user need to execute the program command repeatedly until the verification passes. See Figure 1.99 for an example of a programming flowchart.

CPU Rewrite Mode (Flash memory version)

Program-verify command (C0₁₆)

The program-verify mode is entered by writing the command code "C0₁₆" to the flash command register in the first bus cycle. When the user execute an instruction (e.g., LDE instruction) to read byte data from the address to be verified (the previously programmed address) in the second bus cycle, the content that has actually been written to the address is read out from the memory.

The CPU compares this read data with the data that it previously wrote to the address using the program command. If the compared data do not match, the user need to execute the program and program-verify operations one more time.

Erase command (20₁₆ + 20₁₆)

The flash memory control circuit executes an erase operation by writing command code "20₁₆" to the flash command register in the first bus cycle and the same command code to the flash command register again in the second bus cycle. The erase operation requires approximately 20 ms. Wait for 20 ms or more before the user go to the next processing.

Before this erase command can be performed, all memory locations to be erased must have had data "00₁₆" written to by using the program and program-verify commands. During erase operation, the watchdog timer remains idle, with the value "7FFF₁₆ set in it.

Note 1: The erase operation is not completed immediately by writing an erase command once. The user must always execute an erase-verify command after each erase command executed. And if verification fails, the user need to execute the erase command repeatedly until the verification passes. See Figure 1.99 for an example of an erase flowchart.

Erase-verify command (A0₁₆)

The erase-verify mode is entered by writing the command code "A0₁₆" to the flash command register in the first bus cycle. When the user execute an instruction to read byte data from the address to be verified (e.g., LDE instruction) in the second bus cycle, the content of the address is read out.

The CPU must sequentially erase-verify memory contents one address at a time, over the entire area erased. If any address is encountered whose content is not "FF₁₆" (not erased), the CPU must stop erase-verify at that point and execute erase and erase-verify operations one more time.

Note 1: If any unerased memory location is encountered during erase-verify operation, be sure to execute erase and erase-verify operations one more time. In this case, however, the user does not need to write data "00₁₆" to memory before erasing.

CPU Rewrite Mode (Flash memory version)

Reset command (FF16 + FF16)

The reset command is used to stop the program command or the erase command in the middle of operation. After writing command code "4016" or "2016" twice to the flash command register, write command code "FF16" to the flash command register in the first bus cycle and the same command code to the flash command register again in the second bus cycle. The program command or erase command is disabled, with the flash memory placed in read mode.

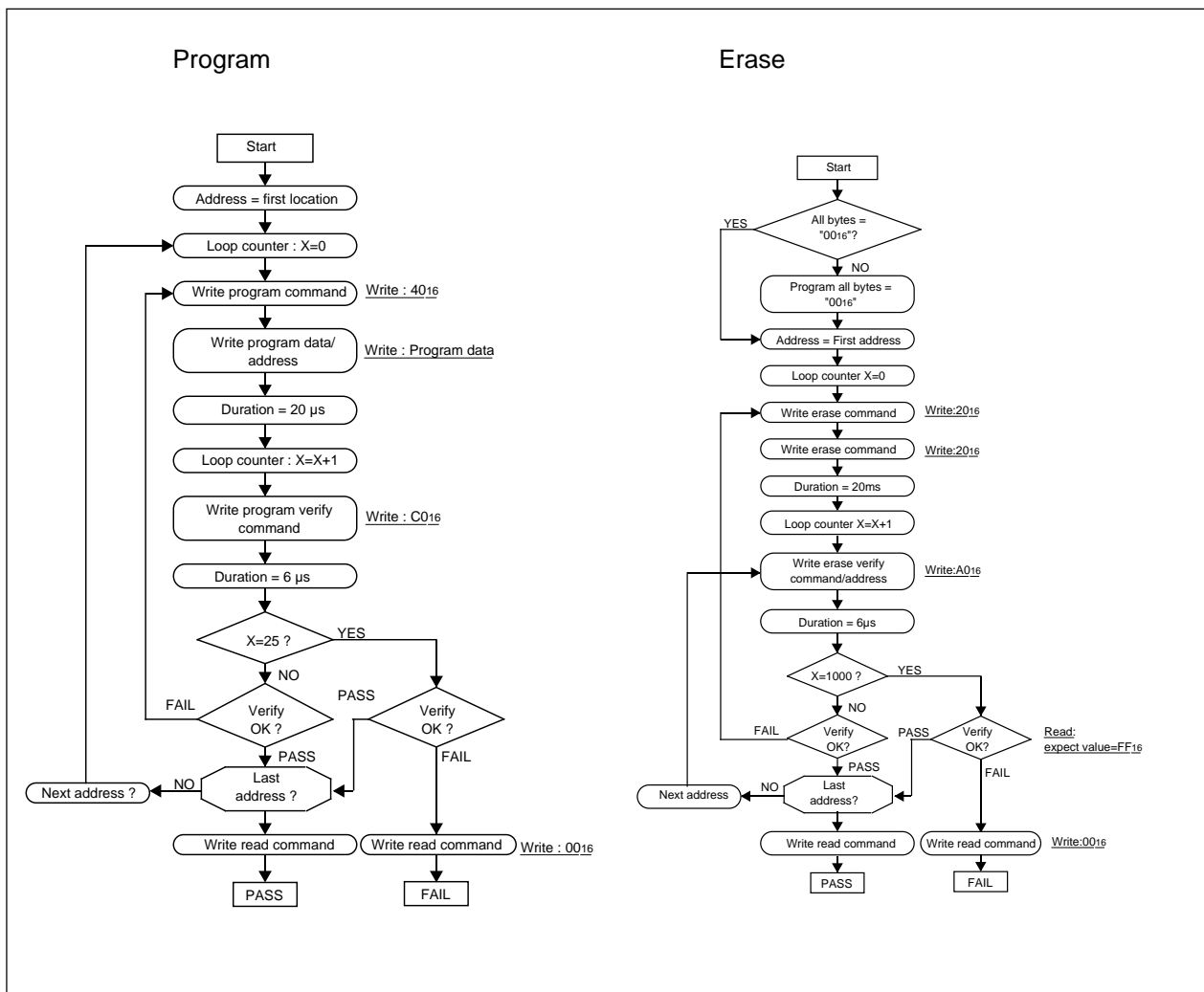


Figure 1.99. Program and erase execution flowchart in the CPU rewrite mode

Appendix Parallel I/O Mode (Flash memory version)

Description of Pin Function (Flash Memory Parallel I/O Mode)

Pin name	Signal name	I/O	Function
Vcc, Vss	Power supply input		Apply 5 V \pm 10 % to the Vcc pin and 0 V to the Vss pin.
CNVss	CNVss	I	Apply 12 V \pm 5 % to the CNVss pin.
RESET	Reset input	I	Connect this pin to Vss.
XIN	Clock input	I	Connect a ceramic or crystal resonator between the XIN and XOUT pins. When entering an externally derived clock, enter it from XIN and leave XOUT open.
XOUT	Clock output	O	
AVcc, AVss	Analog power supply input		Connect AVss to Vss and AVcc to Vcc, respectively.
VREF	Reference voltage input	I	Connect this pin to Vss.
P00 to P07	Data I/O D0 to D7	I/O	These are data D0–D7 input/output pins.
P10 to P17	Address input A8 to A15	I	These are address A8–A15 input pins.
P30 to P33	Address input A4 to A7	I	These are address A4–A7 input pins.
P34 to P35	Input port P3	I	Enter low signals to these pins.
P40	\overline{WE} input	I	This is a \overline{WE} input pin.
P41	\overline{OE} input	I	This is a \overline{OE} input pin.
P43	\overline{CE} input	I	This is a \overline{CE} input pin.
P42, P44, P45	Input port P4	I	Enter high signals or low signals to these pins.
P50	Address input A17	I	This is address A17 input pin.
P51	VRFY input	I	Apply V _{IH} (5 V) to this pin when V _{PP} = V _{PPH} (12 V), or V _{IL} (0 V) when V _{PP} = V _{PLL} (5 V).
P52	Input port P5	I	Enter low signal to this pin.
P53, P54	Input port P5	I	Enter high signals or low signals to these pins.
P60 to P63	Address input A0 to A3	I	These are address A0–A3 input pins.
P64 to P67	Input port P6	I	Enter high signals or low signals to these pins.
P70 to P71	Input port P7	I	Enter high signals or low signals to these pins.

Appendix Parallel I/O Mode (Flash memory version)

Parallel I/O Mode

The parallel I/O mode is entered by making connections shown in Figures 1.101 and 1.102 and then turning the VPPH power supply on. In this mode, the M30201 (flash memory version) operates in a manner similar to the NOR flash memory M5M28F101 from Mitsubishi. Note, however, that there are some differences with regard to the functions not available with the microcomputer (function of read device identification code) and matters related to memory capacity.

Table 1.76 shows pin relationship between the M30201 and M5M28F101 in parallel I/O mode.

Table 1.76. Pin relationship in parallel I/O mode

	M30201(flash memory version)	M5M28F101
Vcc	Vcc	Vcc
Vss	Vss	Vss
Address input	P60 to P63, P30 to P33, P10 to P17, P50	A0 to A15, A17
Data I/O	P00 to P07	D0 to D7
OE input	P41	\overline{OE}
CE input	P43	\overline{CE}
WE input	P40	\overline{WE}
VERFY input (Note)	P51	—

Note: The VRFY input only selects read-only or read/write mode, and does not have any pin associated with it on the M5M28F101.

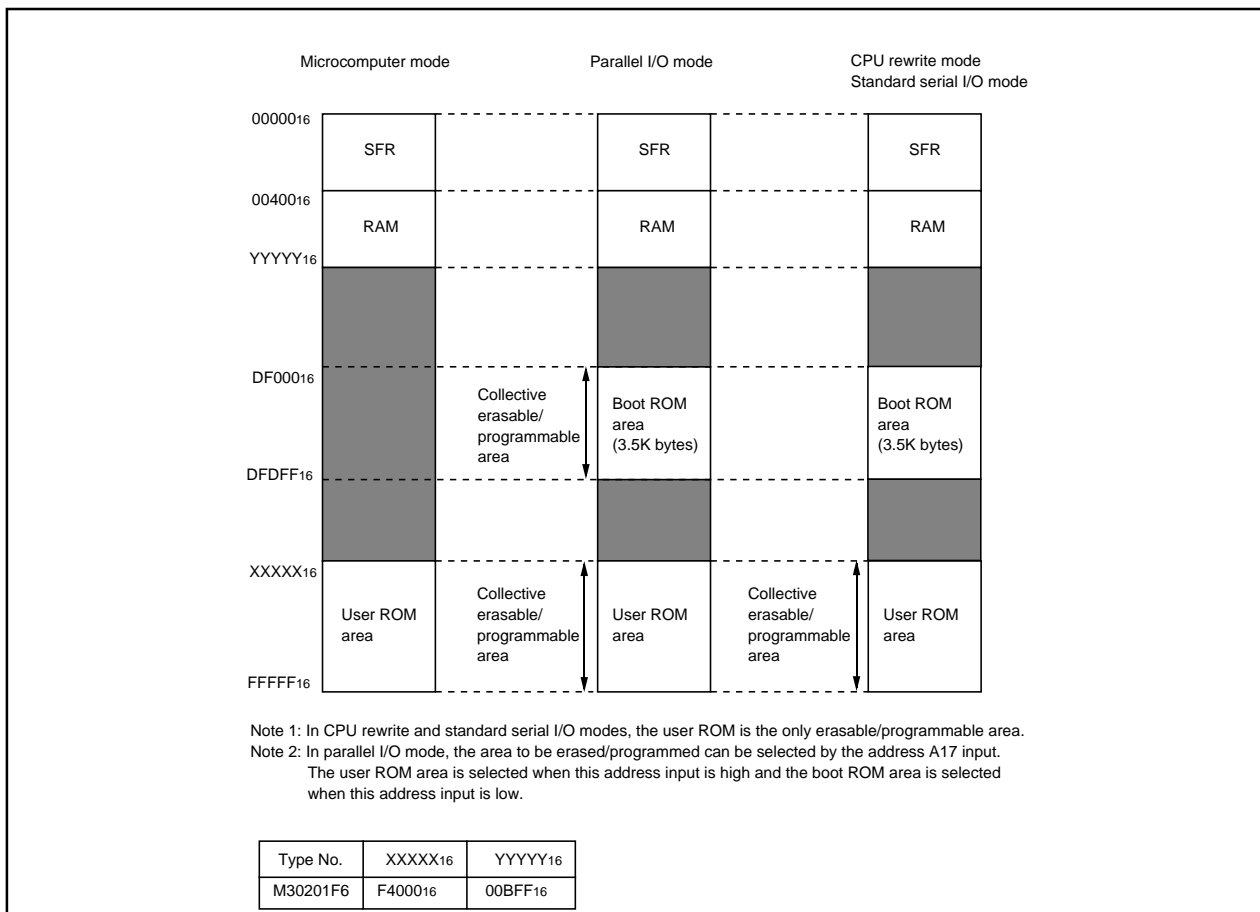


Figure 1.100. Block diagram of flash memory version

Appendix Parallel I/O Mode (Flash memory version)

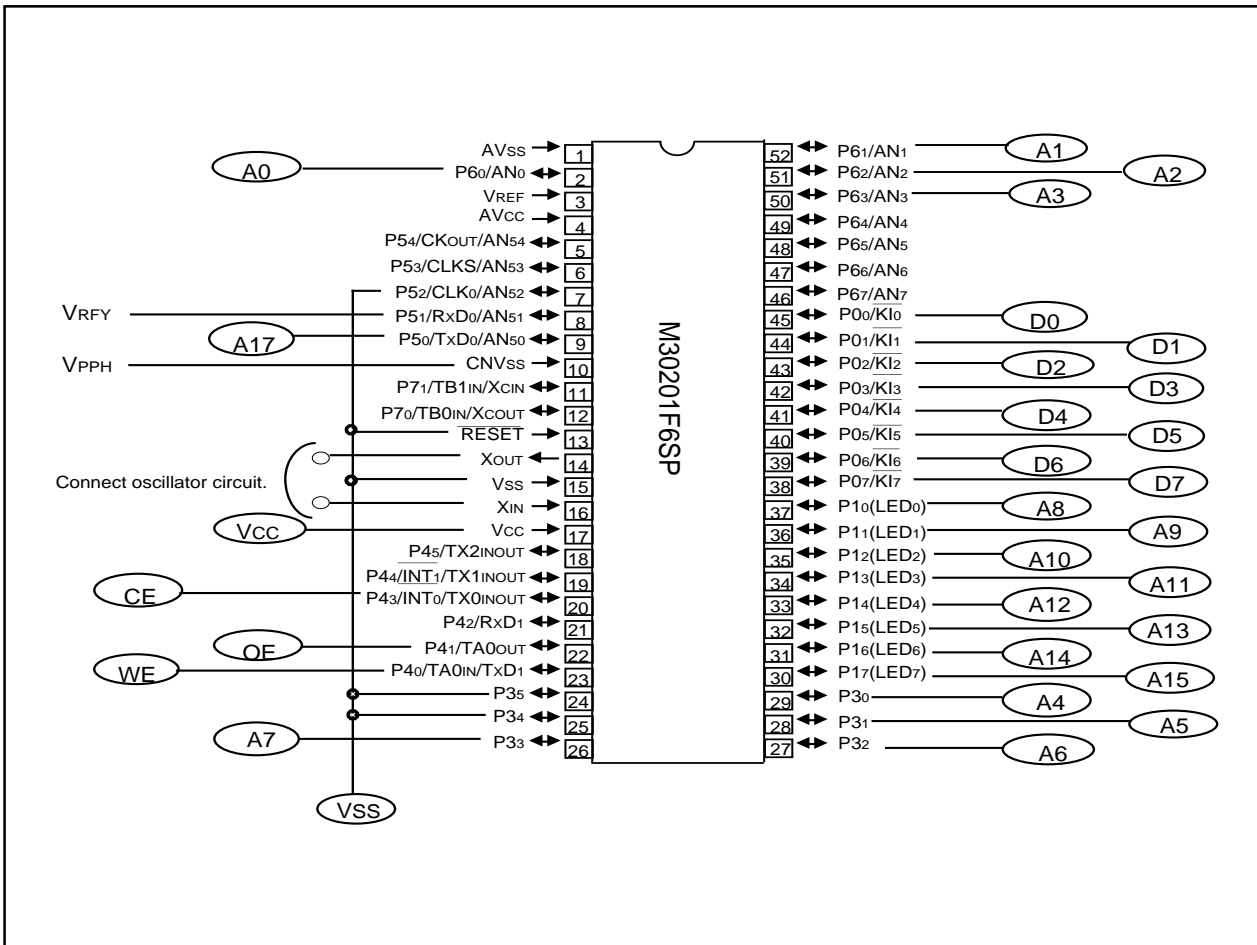


Figure 1.101. Pin connection diagram in parallel I/O mode (1)

Appendix Parallel I/O Mode (Flash memory version)

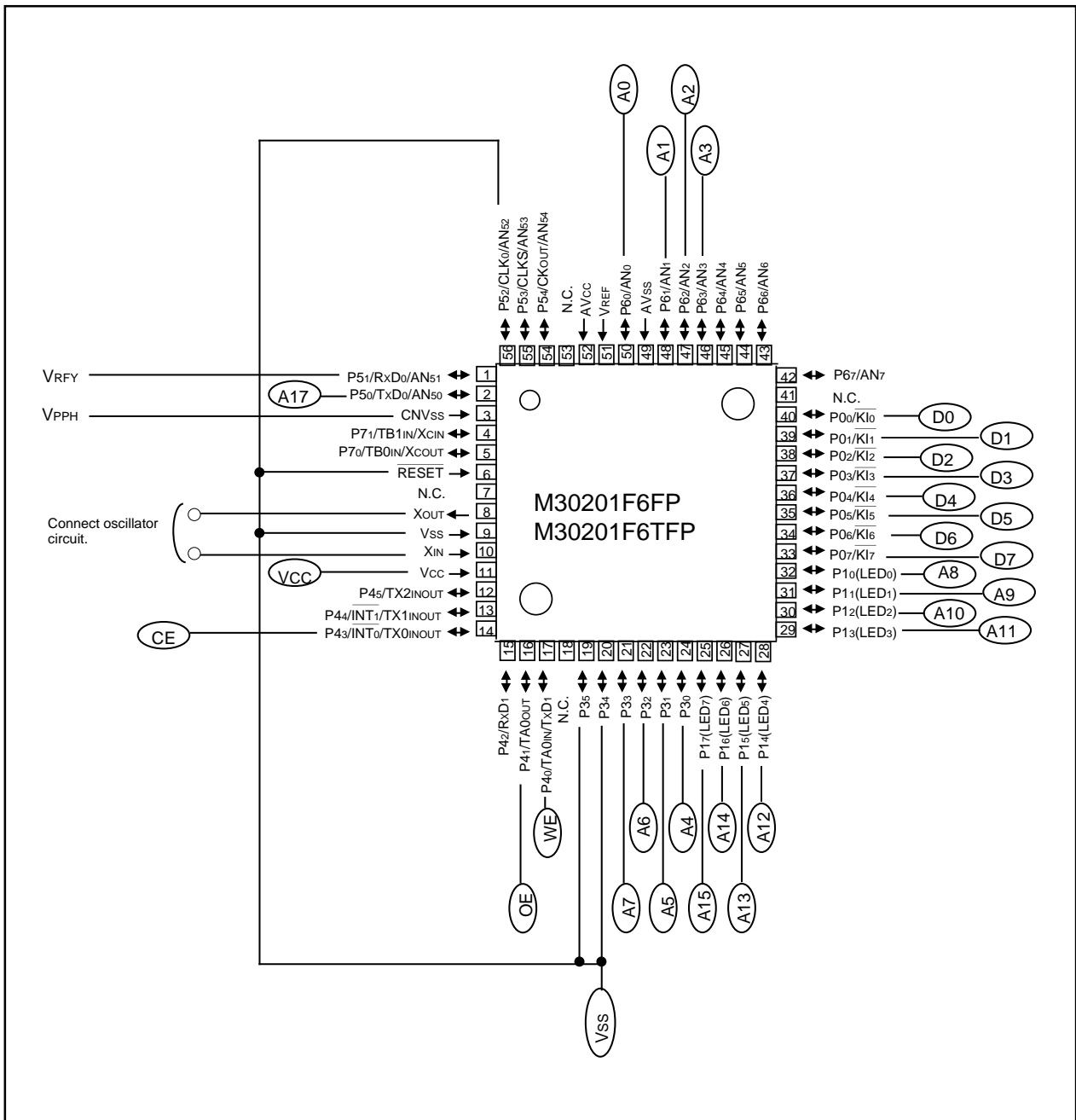


Figure 1.102. Pin connection diagram in parallel I/O mode (2)

Appendix Parallel I/O Mode (Flash memory version)

User ROM and Boot ROM Areas

In parallel I/O mode, the user ROM and boot ROM areas shown in Figure 1.100 can be rewritten.

In the boot ROM area, an erase block operation is applied to only one 3.5 K byte block. The boot ROM area has had a standard serial I/O mode control program stored in it when shipped from the Mitsubishi factory. Therefore, using the device in standard serial input/output mode, the user does not need to write to the boot ROM area.

Functional Outline (Parallel I/O Mode)

In parallel I/O mode, bus operation modes—Read, Output Disable, Standby, and Write—are selected by the status of the \overline{CE} , \overline{OE} , \overline{WE} , V_{RFY} , and $CNVSS$ input pins.

The contents of erase, program, and other operations are selected by writing a software command. The data in memory can only be read out by a read after software command input.

Program and erase operations are controlled using software commands.

Table 1.77. Relationship between control signals and bus operation modes

Mode \ Pin name		\overline{CE}	\overline{OE}	\overline{WE}	V_{RFY}	V_{PP}	D ₀ to D ₇
Read only	Read	V _{IL}	V _{IL}	V _{IH}	V _{IL}	V _{PPH}	Data output
	Output disabled	V _{IL}	V _{IH}	V _{IH}	V _{IL}	V _{PPH}	Hi-Z
	Stand by	V _{IH}	X	X	V _{IL}	V _{PPH}	Hi-Z
Read/Write	Read	V _{IL}	V _{IL}	V _{IH}	V _{IH}	V _{PPH}	Data output
	Output disabled	V _{IL}	V _{IH}	V _{IH}	V _{IH}	V _{PPH}	Hi-Z
	Stand by	V _{IH}	X	X	V _{IH}	V _{PPH}	Hi-Z
	Write	V _{IL}	V _{IH}	V _{IL}	V _{IH}	V _{PPH}	Data input

Note: X can be V_{IL} or V_{IH}.

Appendix Parallel I/O Mode (Flash memory version)

The following explains about bus operation modes, software commands, and status register.

Bus Operation Modes

Read-only mode is entered by applying V_{PPH} to the CNVSS pin and a low voltage to the VRFY pin. Read-only mode has three states: Read, Output Disable, and Standby which are selected by setting the \overline{CE} , \overline{OE} , and \overline{WE} pins high or low.

Read-write mode is entered by applying V_{PPH} to the CNVSS pin and a high voltage to the VRFY pin. Read-write mode has four states: Read, Output Disable, Standby, and Write which are selected by setting the \overline{CE} , \overline{OE} , and \overline{WE} pins high or low.

Read

The Read mode is entered by pulling the \overline{WE} pin high when the \overline{CE} and \overline{OE} pins are low. In Read mode, the data corresponding to each software command entered is output from the data I/O pins D₀–D₇.

Output Disable

The Output Disable mode is entered by pulling the \overline{CE} pin low and the \overline{WE} and \overline{OE} pins high. Also, the data I/O pins are placed in the high-impedance state.

Standby

The Standby mode is entered by driving the \overline{CE} pin high. Also, the data I/O pins are placed in the high-impedance state.

Write

The Write mode is entered by applying V_{PPH} to the CNVSS pin and a high voltage to the VRFY pin and then pulling the \overline{WE} pin low when the \overline{CE} pin is low and \overline{OE} pin is high. In this mode, the device accepts the software commands or write data entered from the data I/O pins. A program, erase, or some other operation is initiated depending on the content of the software command entered here. The input data such as address is latched at the falling edge of \overline{WE} pin. The input data such as software command is latched at the rising edge of \overline{WE} pin.

Appendix Parallel I/O Mode (Flash memory version)

Software Commands

Table 1.78 lists the software commands available with the M30201 (flash memory version). By entering a software command from the data I/O pins (D₀–D₇) in Write mode, specify the content of the operation, such as erase or program operation, to be performed.

The following explains the content of each software command.

Table 1.78. Software command list (parallel I/O mode)

Command	First bus cycle			Second bus cycle		
	Mode	Address	Data (D ₀ to D ₇)	Mode	Address	Data (D ₀ to D ₇)
Read	Write	x	00 ₁₆			
Program	Write	x	40 ₁₆	Write	Program address	Program data
Program verify	Write	x	C0 ₁₆	Read	x	Verify data
Erase	Write	x	20 ₁₆	Write	x	20 ₁₆
Erase verify	Write	Verify address	A0 ₁₆	Read	x	Verify data
Reset	Write	x	FF ₁₆	Write	x	FF ₁₆

Read Command (00₁₆)

The read mode is entered by writing the command code “00₁₆” in the first bus cycle. When an address to be read is input in one of the bus cycles that follow, the content of the specified address is read out at the data I/O pins (D₀–D₇).

The read mode is retained intact until another command is written.

After reset and after the reset command is executed, the read mode is set.

Program Command (40₁₆)

The program mode is entered by writing the command code “40₁₆” in the first bus cycle. When an address and data to be program is write in the second bus cycle, the flash memory control circuit executes the program operation. The program operation requires approximately 20 μs. Wait for 20 μs or more before the user go to the next processing.

Note 1: The write operation is not completed immediately by writing a program command once. The user must always execute a program-verify command after each program command executed. And if verification fails, the user need to execute the program command repeatedly until the verification passes. See Figure 1.103 for an example of a programming flowchart.

Appendix Parallel I/O Mode (Flash memory version)

Program-verify command (C0₁₆)

The program-verify mode is entered by writing the command code "C0₁₆" in the first bus cycle and the verify data is output from the data I/O pins (D₀–D₇) in the second bus cycle.

Erase command (20₁₆ + 20₁₆)

The flash memory control circuit executes an erase operation by writing command code "20₁₆" in the first bus cycle and the same command code again in the second bus cycle. The erase operation requires approximately 20 ms. Wait for 20 ms or more before the user go to the next processing. Before this erase command can be performed, all memory locations to be erased must have had data "00₁₆" written to by using the program and program-verify commands.

Note 1: The erase operation is not completed immediately by writing an erase command once. The user must always execute an erase-verify command after each erase command executed. And if verification fails, the user need to execute the erase command repeatedly until the verification passes. See Figure 1.103 for an example of an erase flowchart.

Erase-verify command (A0₁₆)

The erase-verify mode is entered by writing the command code "A0₁₆" in the first bus cycle and the verify data is output from the data I/O pins (D₀–D₇) in the second bus cycle.

Note 1: If any unerased memory location is encountered during erase-verify operation, be sure to execute erase and erase-verify operations one more time. In this case, however, the user does not need to write data "00₁₆" to memory before erasing.

Appendix Parallel I/O Mode (Flash memory version)

Reset command (FF₁₆ + FF₁₆)

The reset command is used to stop the program command or the erase command in the middle of operation. After writing command code "40₁₆" or "20₁₆" twice, write command code "FF₁₆" in the first bus cycle and the same command code again in the second bus cycle. The program command or erase command is disabled, with the flash memory placed in read mode.

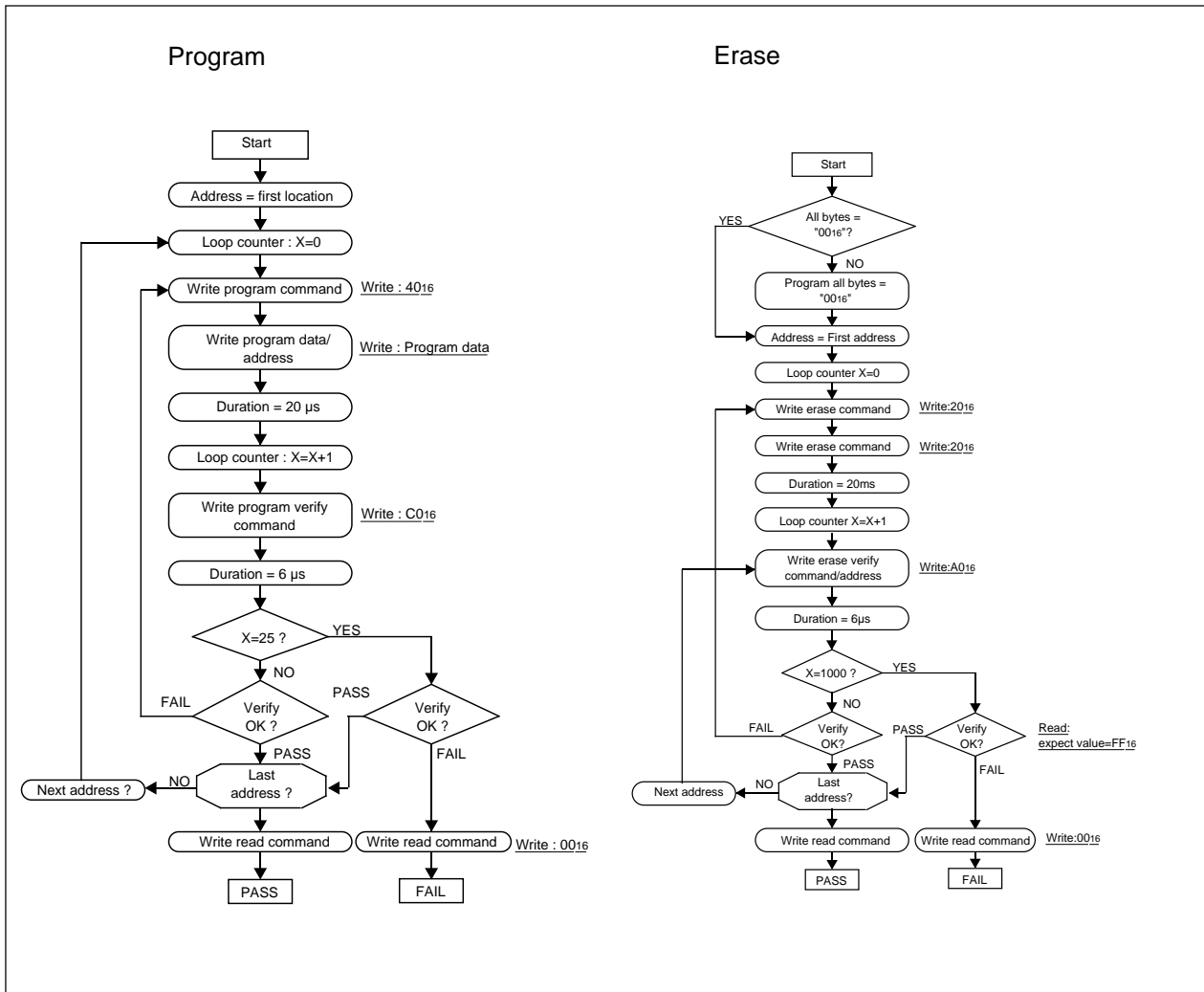


Figure 1.103. Program and erase execution flowchart in the CPU rewrite mode

Appendix Parallel I/O Mode (Flash memory version)

Protect function

In parallel I/O mode, the internal flash memory has the "protect function" available. This function protects the flash memory contents from being read or rewritten easily.

Depending on the content at the protect control address (FFFFF₁₆) in parallel I/O mode, this function inhibits the flash memory contents against read or modification. The protect control address (FFFFF₁₆) is shown in Figure 1.104. (This address exists in the user ROM area.)

The protect function is enabled by setting one of the two protect set bits to "0", so that the internal flash memory contents are inhibited against read or modification. The protect function is disabled by setting both of the two protect reset bits to "00", so that the internal flash memory contents can be read or modified. Once the protect function is set, the user cannot change settings of the protect clear bits while in parallel I/O mode. Settings of the protect reset bits can only be changed in CPU rewrite mode.

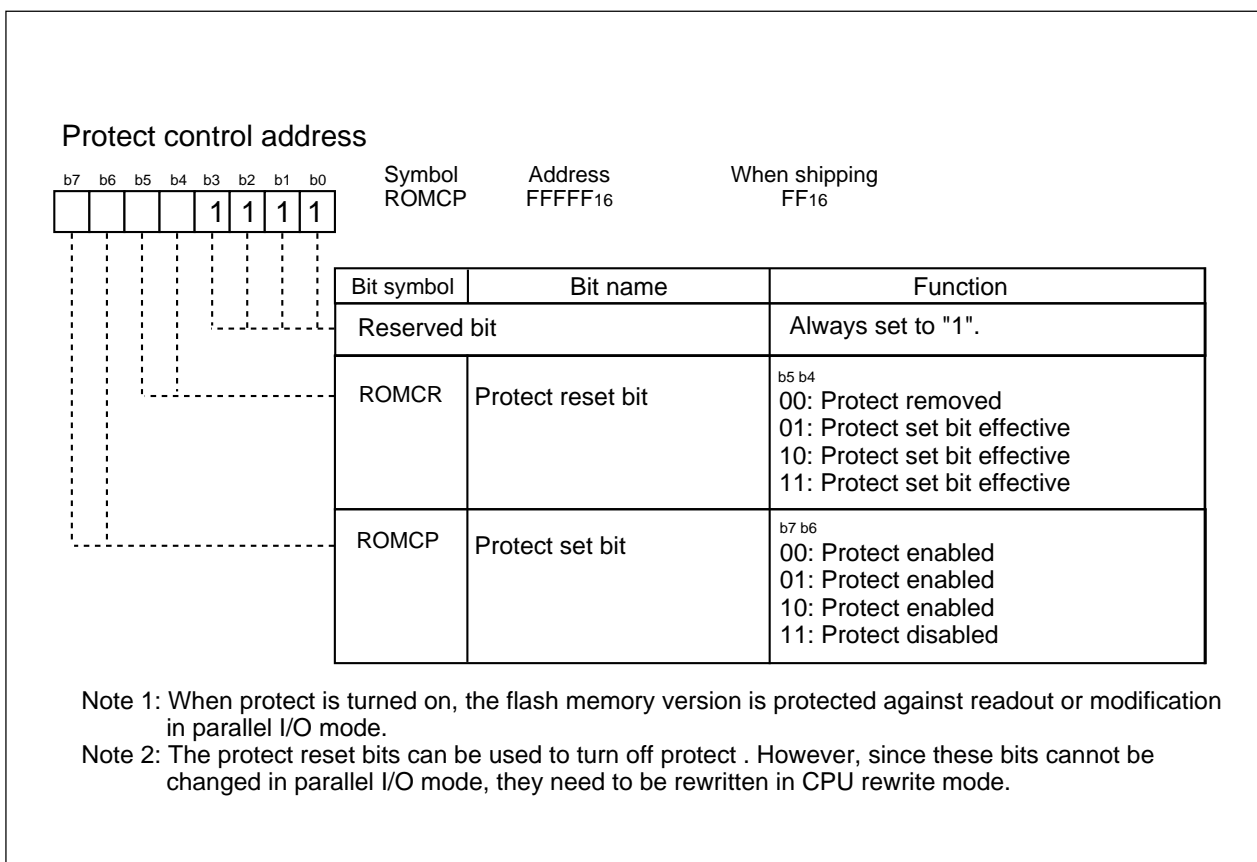


Figure 1.104. Protect control address

Appendix Standard Serial I/O Mode (Flash Memory Version)

Pin functions (Flash memory standard serial I/O mode)

Pin	Name	I/O	Description
Vcc, Vss	Power input		Apply 5V \pm 10 % to Vcc pin and 0 V to Vss pin.
CNVss	CNVss	I	Mode entry pin. Apply 12V \pm 5 % to this pin.
RESET	Reset input	I	Reset input pin. While reset is "L" level, a 20 cycle or longer clock must be input to XIN pin.
XIN	Clock input	I	Connect a ceramic resonator or crystal oscillator between XIN and XOUT pins. To input an externally generated clock, input it to XIN pin and open XOUT pin.
XOUT	Clock output	O	
AVcc, AVss	Analog power supply input		Connect AVss to Vss and AVcc to Vcc, respectively.
VREF	Reference voltage input	I	Enter the reference voltage for AD from this pin.
P00 to P07	Input port P0	I	Input "H" or "L" level signal or open.
P10 to P17	Input port P1	I	Input "H" or "L" level signal or open.
P30 to P35	Input port P3	I	Input "H" or "L" level signal or open.
P40 to P45	Input port P4	I	Input "H" or "L" level signal or open.
P54	Input port P5	I	Input "H" or "L" level signal or open.
P50	TxD output	O	Serial data output pin.
P51	RxD input	I	Serial data input pin.
P52	SCLK input	I	Mode entry pin. Supply "H" level when powering on MCU. When startup is completed this pin serves the serial input clock.
P53	BUSY	I \rightarrow O	This pin sets the type of serial flash programming mode. <ul style="list-style-type: none"> •An "H" level input (mode 1) sets the mode to clock synchronous. •An "L" level input (mode 2) sets the mode to clock asynchronous. This pin changes to "output" after entry into standard serial I/O mode.
P60 to P67	Input port P6	I	Input "H" or "L" level signal or open.
P70 to P71	Input port P7	I	Input "H" or "L" level signal or open.

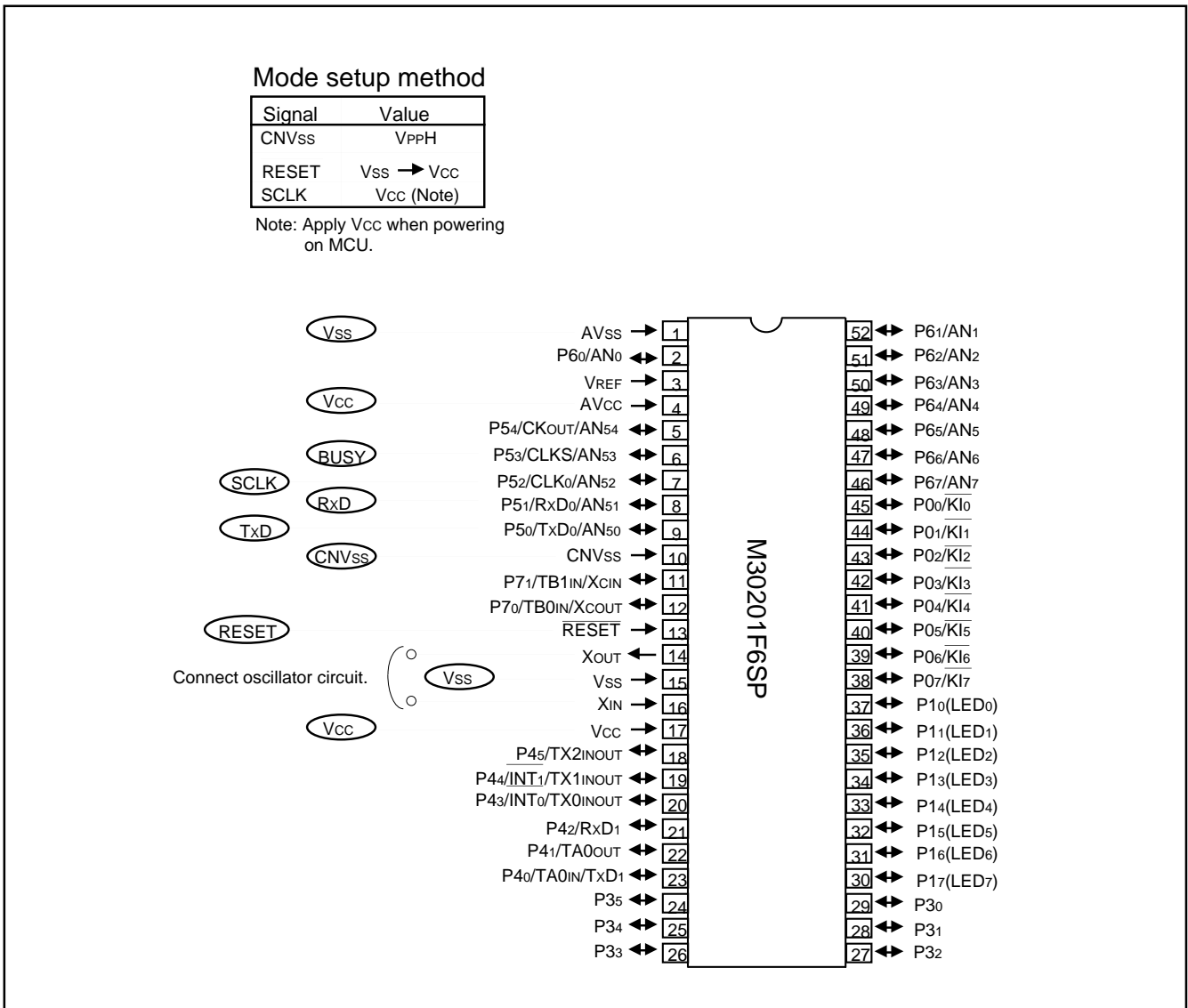


Figure 1.105. Pin connections for standard serial I/O mode (1)

Appendix Standard Serial I/O Mode (Flash Memory Version)

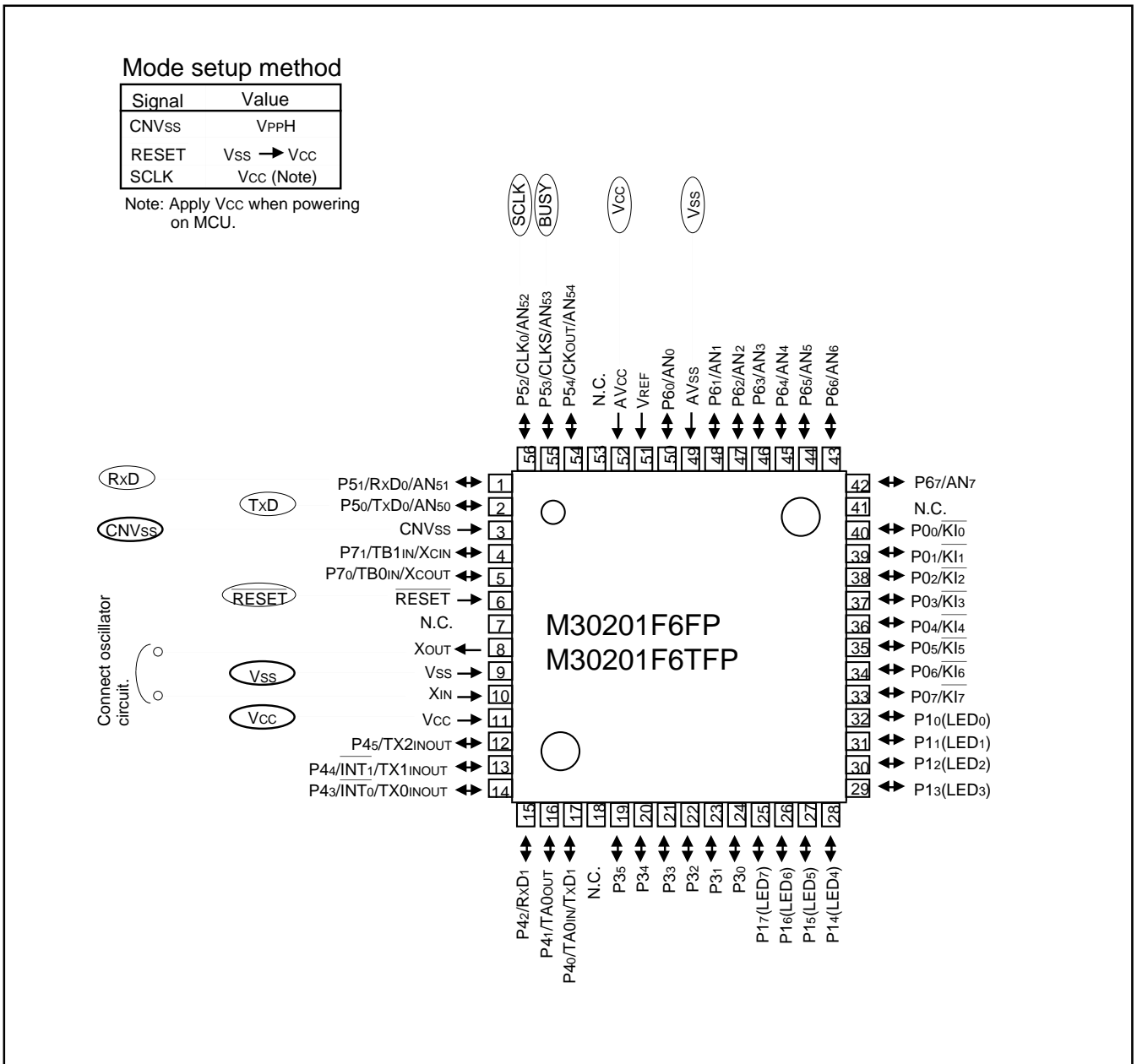


Figure 1.106. Pin connections for serial I/O mode (2)

Standard serial I/O mode

The standard serial I/O mode inputs and outputs the software commands, addresses and data needed to operate (read, program, erase, etc.) the internal flash memory. This I/O is serial. There are actually two standard serial I/O modes: mode 1, which is clock synchronized, and mode 2, which is asynchronous. Both modes require a purpose-specific peripheral unit.

The standard serial I/O mode is different from the parallel I/O mode in that the CPU controls flash memory rewrite (uses the CPU's rewrite mode), rewrite data input and so forth. It is started when the reset is released, which is done when the P52 (SCLK) pin is "H" level, the CNVss pin "VppH" level. (In the ordinary command mode, set CNVss pin to "L" level.)

This control program is written in the boot ROM area when the product is shipped from Mitsubishi. Accordingly, make note of the fact that the standard serial I/O mode cannot be used if the boot ROM area is rewritten in the parallel I/O mode. Figures 1.105 and 1.106 show the pin connections for the standard serial I/O mode. Serial data I/O uses UART0 and transfers the data serially in 8-bit units. Standard serial I/O switches between mode 1 (clock synchronized) and mode 2 (clock asynchronous) according to the level of P53 (BUSY) pin when the reset is released.

To use standard serial I/O mode 1 (clock synchronized), set the P53 (BUSY) pin to "H" level and release the reset. The operation uses the four UART0 pins CLK0, RxD0, TxD0 and P53 (BUSY). The CLK0 pin is the transfer clock input pin through which an external transfer clock is input. The TxD0 pin is for CMOS output. The P53 (BUSY) pin outputs an "L" level when ready for reception and an "H" level when reception starts.

To use standard serial I/O mode 2 (clock asynchronous), set the P53 (BUSY) pin to "L" level and release the reset. The operation uses the two UART0 pins RxD0 and TxD0.

In the standard serial I/O mode, only the user ROM area indicated in Figure 1.96 can be rewritten. The boot ROM cannot.

In the standard serial I/O mode, a 7-byte ID code is used. When there is data in the flash memory, commands sent from the peripheral unit are not accepted unless the ID code matches.

Overview of standard serial I/O mode 1 (clock synchronized)

In standard serial I/O mode 1, software commands, addresses and data are input and output between the MCU and peripheral units (serial programmer, etc.) using clock-synchronized serial I/O (UART0) and P53 (BUSY). Standard serial I/O mode 1 is engaged by releasing the reset with the P53 (BUSY) pin "H" level. In reception, software commands, addresses and program data are synchronized with the rise of the transfer clock that is input to the CLK0 pin, and are then input to the MCU via the RxD0 pin. In transmission, the read data and status are synchronized with the fall of the transfer clock, and output from the TxD0 pin.

The TxD0 pin is for CMOS output. Transfer is in 8-bit units with LSB first.

When busy, such as during transmission, reception, erasing or program execution, the P53 (BUSY) pin is "H" level. Accordingly, always start the next transfer after the P53 (BUSY) pin is "L" level.

Also, data and status registers in memory can be read after inputting software commands. Status, such as the operating state of the flash memory or whether a program or erase operation ended successfully or not, can be checked by reading the status register. Here following are explained software commands, status registers, etc.

Appendix Standard Serial I/O Mode 1 (Flash Memory Version)

Software Commands

Table 1.79 lists software commands. In the standard serial I/O mode 1, erase operations, programs and reading are controlled by transferring software commands via the RxD0 pin. Software commands are explained here below.

Table 1.79. Software commands (Standard serial I/O mode 1)

	Control command		2nd byte	3rd byte	4th byte	5th byte	6th byte		When ID is not verificate
1	Page read	FF ₁₆	Address (middle)	Address (high)	Data output	Data output	Data output	Data output to 259th byte	Not acceptable
2	Page program	41 ₁₆	Address (middle)	Address (high)	Data input	Data input	Data input	Data input to 259th byte	Not acceptable
3	Erase all unlocked blocks	A7 ₁₆	D0 ₁₆						Not acceptable
4	Read status register	70 ₁₆	SRD output	SRD1 output					Acceptable
5	Clear status register	50 ₁₆							Not acceptable
6	Read lockbit status	71 ₁₆	Address (middle)	Address (high)	Lock bit data output				Not acceptable
7	ID check function	F5 ₁₆	Address (low)	Address (middle)	Address (high)	ID size	ID1	To ID7	Acceptable
8	Download function	FA ₁₆	Size (low)	Size (high)	Check-sum	Data input	To required number of times		Not acceptable
9	Version data output function	FB ₁₆	Version data output	Version data output	Version data output	Version data output	Version data output	Version data output to 9th byte	Acceptable
10	Boot area output function	FC ₁₆	Address (middle)	Address (high)	Data output	Data output	Data output	Data output to 259th byte	Not acceptable

Note 1: Shading indicates transfer from flash memory microcomputer to peripheral unit. All other data is transferred from the peripheral unit to the flash memory microcomputer.

Note 2: SRD refers to status register data. SRD1 refers to status register 1 data.

Note 3: All commands can be accepted when the flash memory is totally blank.

Page Read Command

This command reads the specified page (256 bytes) in the flash memory sequentially one byte at a time. Execute the page read command as explained here following.

- (1) Transfer the "FF16" command code with the 1st byte.
- (2) Transfer addresses A8 to A15 and A16 to A23 with the 2nd and 3rd bytes respectively.
- (3) From the 4th byte onward, data (D0–D7) for the page (256 bytes) specified with addresses A8 to A23 will be output sequentially from the smallest address first in sync with the rise of the clock.

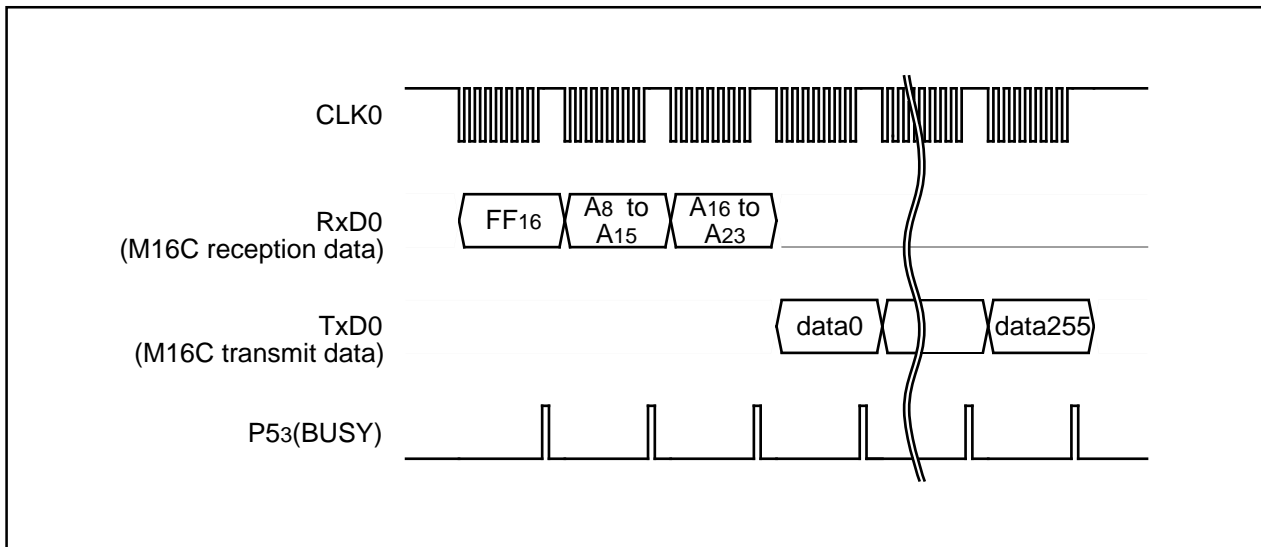


Figure 1.107. Timing for page read

Read Status Register Command

This command reads status information. When the "7016" command code is sent with the 1st byte, the contents of the status register (SRD) specified with the 2nd byte and the contents of status register 1 (SRD1) specified with the 3rd byte are read.

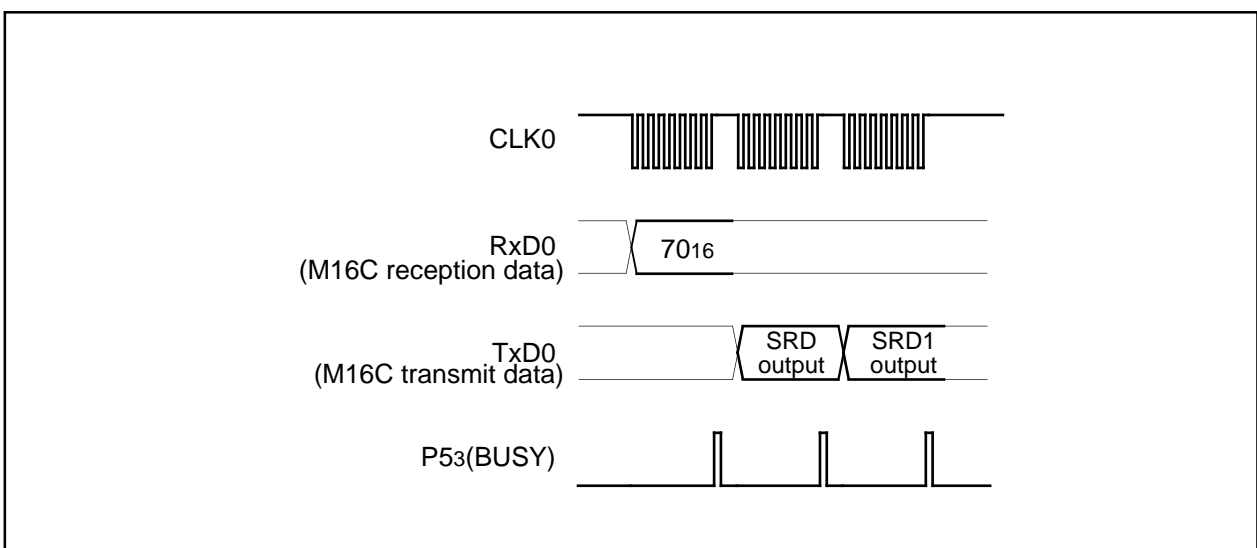


Figure 1.108. Timing for reading the status register

Clear Status Register Command

This command clears the bits (SR3–SR4) which are set when the status register operation ends in error. When the “5016” command code is sent with the 1st byte, the aforementioned bits are cleared. When the clear status register operation ends, the P53 (BUSY) signal changes from the “H” to the “L” level.

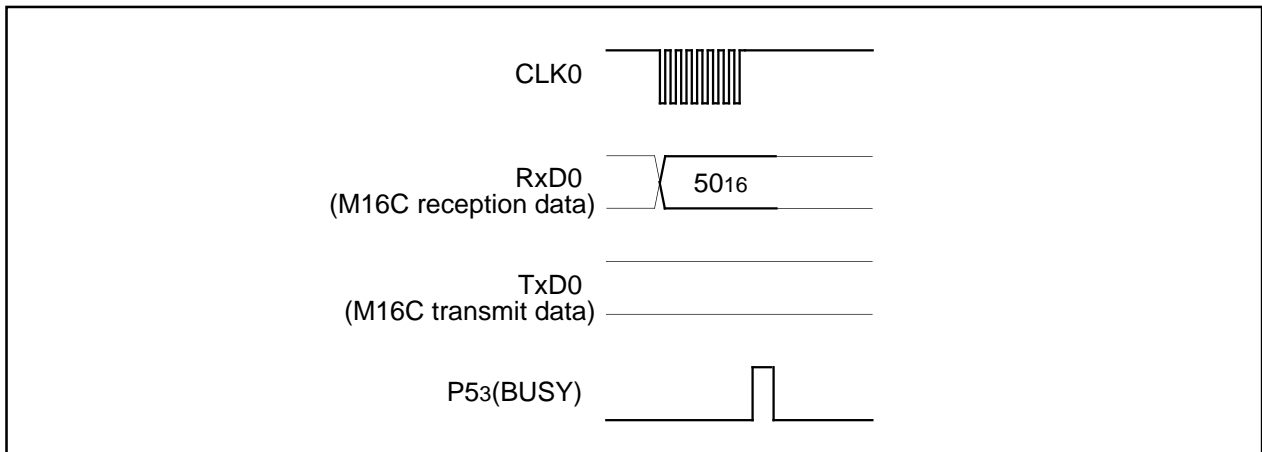


Figure 1.109. Timing for clearing the status register

Page Program Command

This command writes the specified page (256 bytes) in the flash memory sequentially one byte at a time. Execute the page program command as explained here following.

- (1) Transfer the “4116” command code with the 1st byte.
- (2) Transfer addresses A8 to A15 and A16 to A23 with the 2nd and 3rd bytes respectively.
- (3) From the 4th byte onward, as write data (D0–D7) for the page (256 bytes) specified with addresses A8 to A23 is input sequentially from the smallest address first, that page is automatically written.

When reception setup for the next 256 bytes ends, the P53 (BUSY) signal changes from the “H” to the “L” level. The result of the page program can be known by reading the status register. For more information, see the section on the status register.

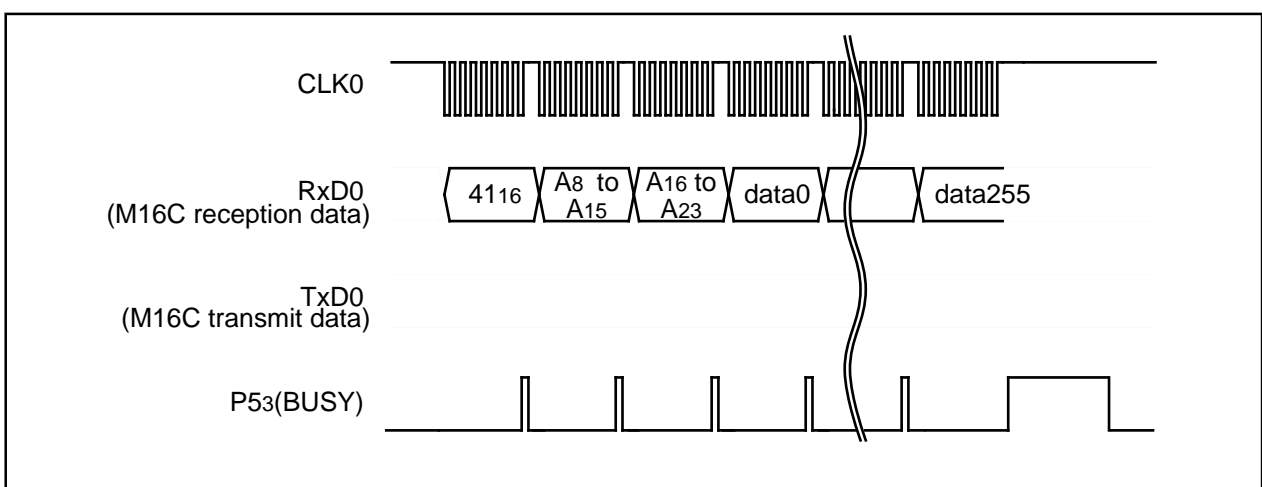


Figure 1.110. Timing for the page program

Erase All Unlocked Blocks Command

This command erases the content of all blocks. Execute the erase all unlocked blocks command as explained here following.

- (1) Transfer the "A716" command code with the 1st byte.
- (2) Transfer the verify command code "D016" with the 2nd byte. With the verify command code, the erase operation will start and continue for all blocks in the flash memory.

When block erasing ends, the P53 (BUSY) signal changes from the "H" to the "L" level. The result of the erase operation can be known by reading the status register.

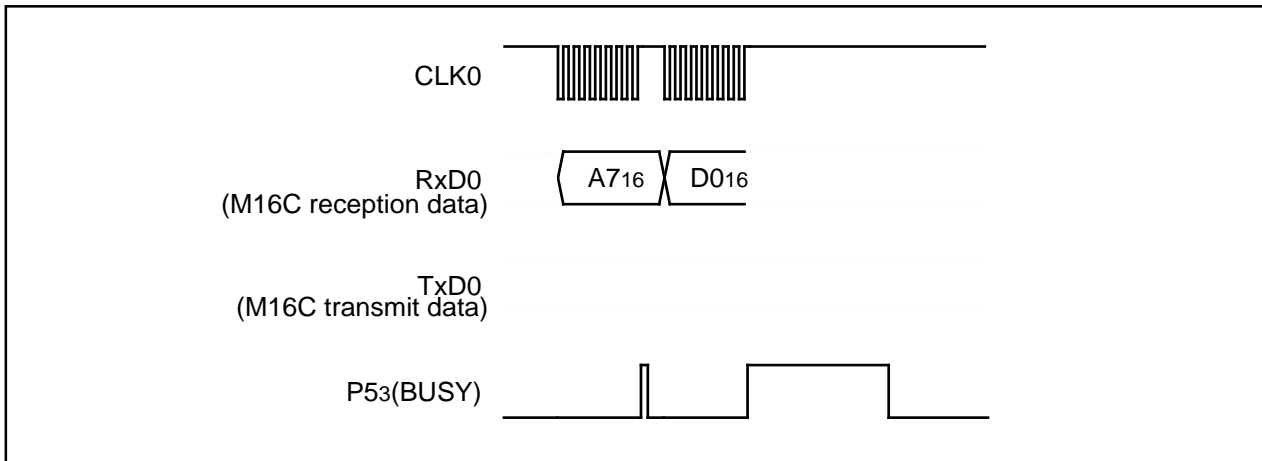


Figure 1.111. Timing for erasing all unlocked blocks

Read Lock Bit Status Command

This command reads the lock bit status of the specified block. Execute the read lock bit status command as explained here following.

- (1) Transfer the "7116" command code with the 1st byte.
- (2) Transfer addresses A8 to A15 and A16 to A23 with the 2nd and 3rd bytes respectively.
- (3) The lock bit data of the specified block is output with the 4th byte. Write the highest address of the specified block for addresses A8 to A23.

The M30201 (flash memory version) does not have the lock bit, so the read value is always "1" (block unlock).

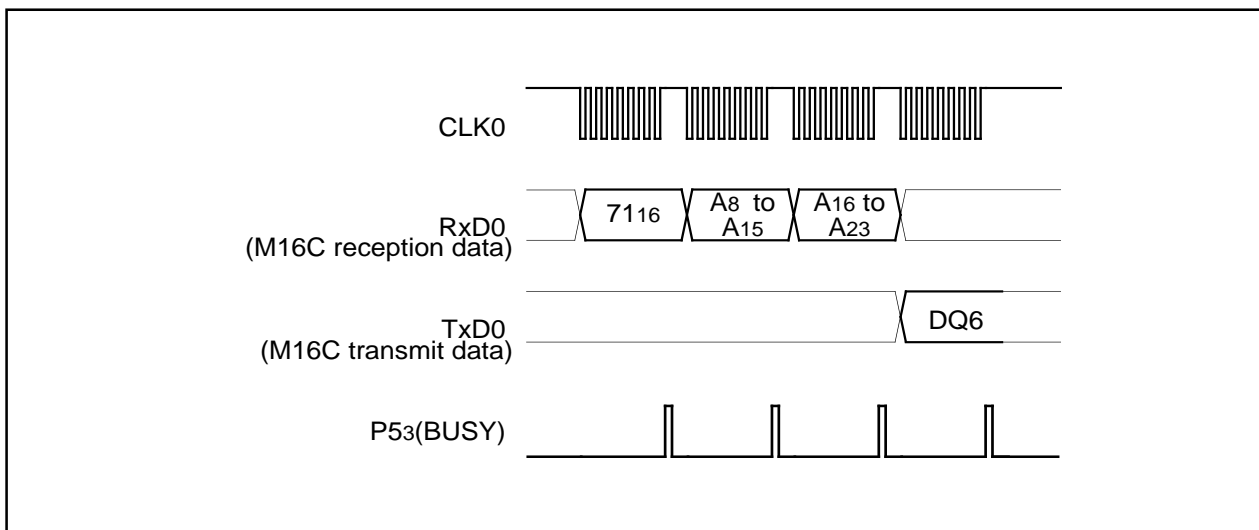


Figure 1.112. Timing for reading lock bit status

Download Command

This command downloads a program to the RAM for execution. Execute the download command as explained here following.

- (1) Transfer the "FA16" command code with the 1st byte.
- (2) Transfer the program size with the 2nd and 3rd bytes.
- (3) Transfer the check sum with the 4th byte. The check sum is added to all data sent with the 5th byte onward.
- (4) The program to execute is sent with the 5th byte onward.

When all data has been transmitted, if the check sum matches, the downloaded program is executed. The size of the program will vary according to the internal RAM.

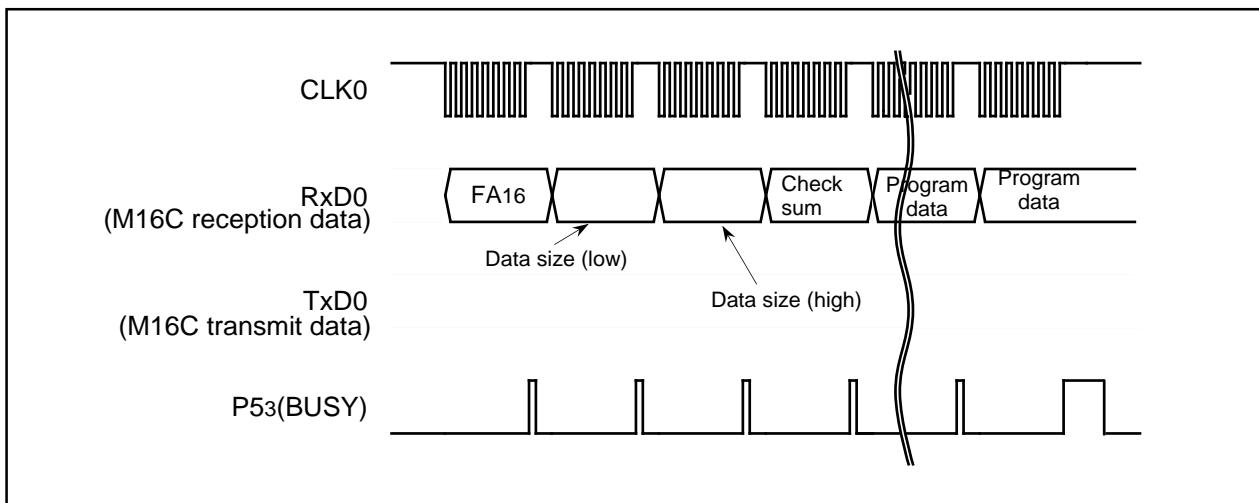


Figure 1.113. Timing for download

Version Information Output Command

This command outputs the version information of the control program stored in the boot area. Execute the version information output command as explained here following.

- (1) Transfer the "FB16" command code with the 1st byte.
- (2) The version information will be output from the 2nd byte onward. This data is composed of 8 ASCII code characters.

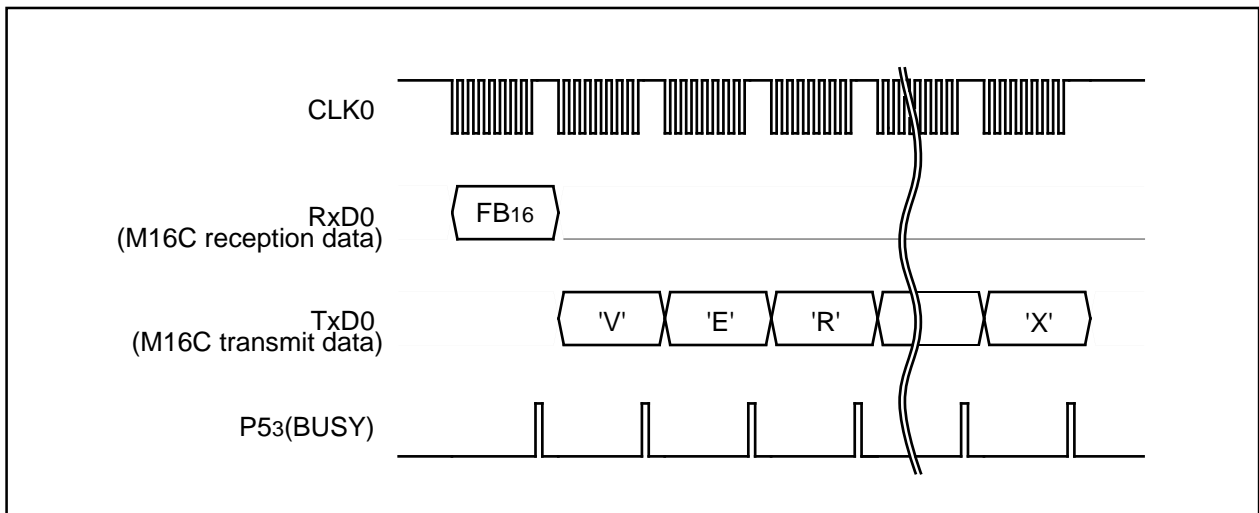


Figure 1.114. Timing for version information output

Boot ROM Area Output Command

This command outputs the control program stored in the boot ROM area in one page blocks (256 bytes). Execute the boot ROM area output command as explained here following.

- (1) Transfer the "FC16" command code with the 1st byte.
- (2) Transfer addresses A8 to A15 and A16 to A23 with the 2nd and 3rd bytes respectively.
- (3) From the 4th byte onward, data (D0–D7) for the page (256 bytes) specified with addresses A8 to A23 will be output sequentially from the smallest address first, in sync with the fall of the clock.

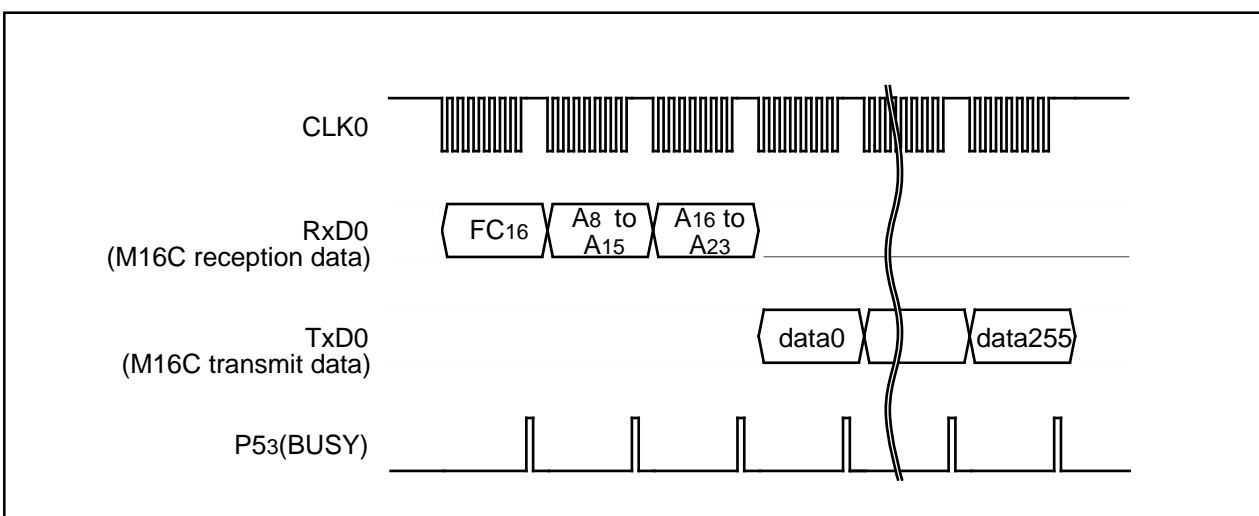


Figure 1.115. Timing for boot ROM area output

ID Check

This command checks the ID code. Execute the boot ID check command as explained here following.

- (1) Transfer the "F5₁₆" command code with the 1st byte.
- (2) Transfer addresses A₀ to A₇, A₈ to A₁₅ and A₁₆ to A₂₃ of the 1st byte of the ID code with the 2nd, 3rd and 4th bytes respectively.
- (3) Transfer the number of data sets of the ID code with the 5th byte.
- (4) The ID code is sent with the 6th byte onward, starting with the 1st byte of the code.

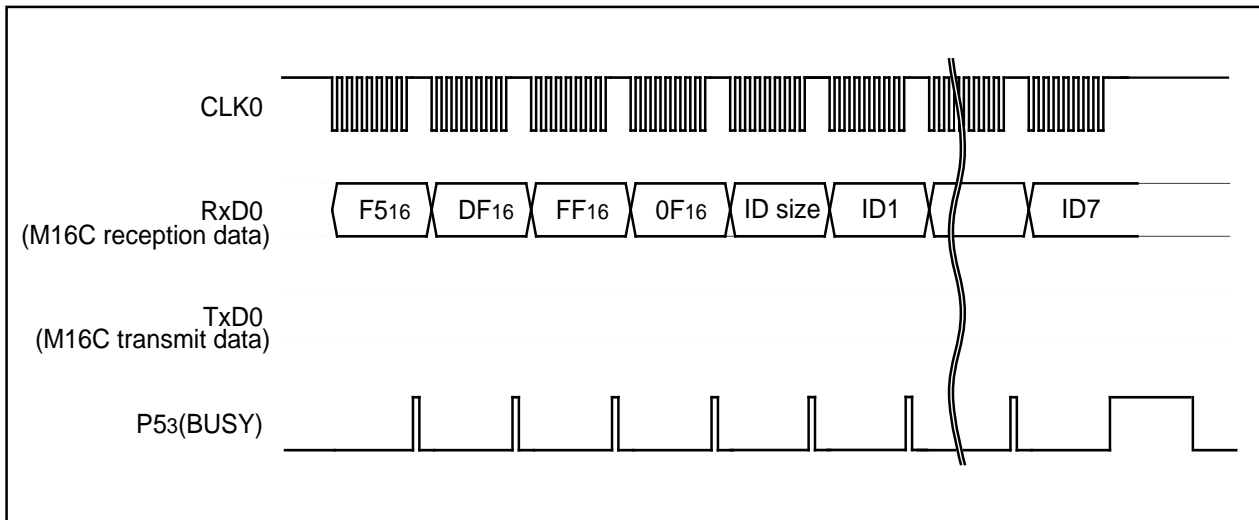


Figure 1.116. Timing for the ID check

ID Code

When the flash memory is not blank, the ID code sent from the peripheral units and the ID code written in the flash memory are compared to see if they match. If the codes do not match, the command sent from the peripheral units is not accepted. An ID code contains 8 bits of data. Area is, from the 1st byte, addresses 0FFFD₁₆, 0FFFE₃₁₆, 0FFFE_{B16}, 0FFFE_{F16}, 0FFFF₃₁₆, 0FFFF₇₁₆ and 0FFFF_{B16}. Write a program into the flash memory, which already has the ID code set for these addresses.

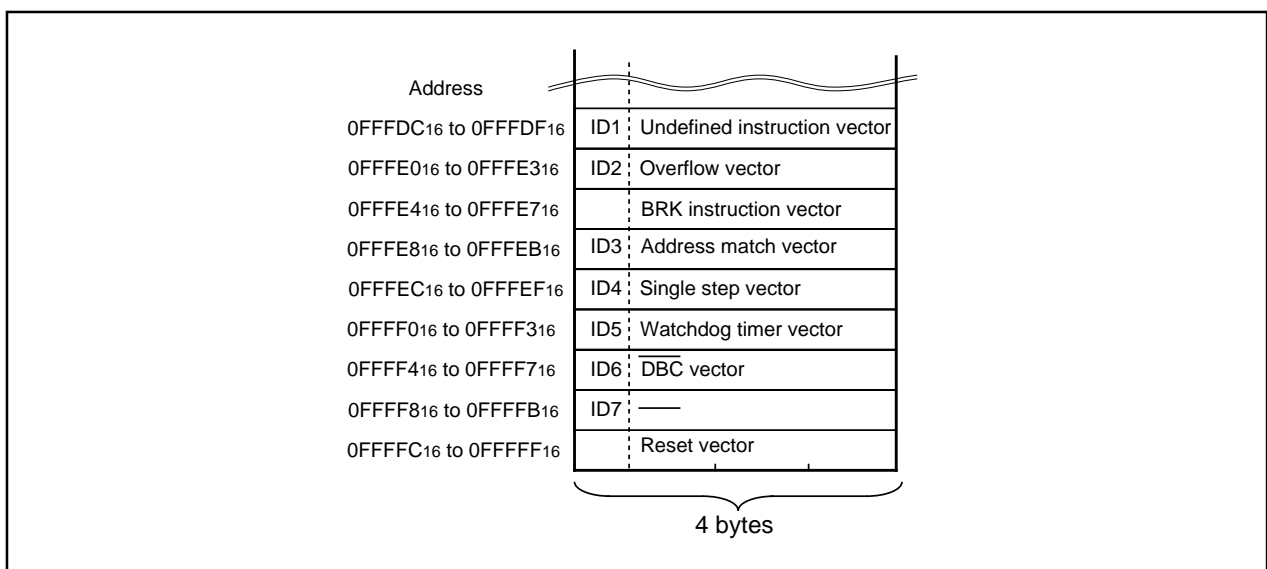


Figure 1.117. ID code storage addresses

Status Register (SRD)

The status register indicates operating status of the flash memory and status such as whether an erase operation or a program ended successfully or in error. It can be read by writing the read status register command (70₁₆). Also, the status register is cleared by writing the clear status register command (50₁₆). Table 1.80 gives the definition of each status register bit. After clearing the reset, the status register outputs "80₁₆".

Table 1.80. Status register (SRD)

SRD0 bits	Status name	Definition	
		"1"	"0"
SR7 (bit7)	Status bit	Ready	Busy
SR6 (bit6)	Reserved	-	-
SR5 (bit5)	Erase bit	Terminated in error	Terminated normally
SR4 (bit4)	Program bit	Terminated in error	Terminated normally
SR3 (bit3)	Reserved	-	-
SR2 (bit2)	Reserved	-	-
SR1 (bit1)	Reserved	-	-
SR0 (bit0)	Reserved	-	-

Status bit (SR7)

The status bit indicates the operating status of the flash memory. When power is turned on, "1" (ready) is set for it. The bit is set to "0" (busy) during an auto write or auto erase operation, but it is set back to "1" when the operation ends.

Erase Status (SR5)

The erase status reports the operating status of the auto erase operation. If an erase error occurs, it is set to "1". When the erase status is cleared, it is set to "0".

Program Status (SR4)

The program status reports the operating status of the auto write operation. If a write error occurs, it is set to "1". When the program status is cleared, it is set to "0".

Status Register 1 (SRD1)

Status register 1 indicates the status of serial communications, results from ID checks and results from check sum comparisons. It can be read after the SRD by writing the read status register command (7016). Also, status register 1 is cleared by writing the clear status register command (5016).

Table 1.81 gives the definition of each status register 1 bit. "0016" is output when power is turned ON and the flag status is maintained even after the reset.

Table 1.81. Status register 1 (SRD1)

SRD1 bits	Status name	Definition	
		"1"	"0"
SR15 (bit7)	Boot update completed bit	Update completed	Not update
SR14 (bit6)	Reserved	-	-
SR13 (bit5)	Reserved	-	-
SR12 (bit4)	Checksum match bit	Match	Mismatch
SR11 (bit3) SR10 (bit2)	ID check completed bits	00 01 10 11	Not verified Verification mismatch Reserved Verified
SR9 (bit1)	Data receive time out	Time out	Normal operation
SR8 (bit0)	Reserved	-	-

Boot Update Completed Bit (SR15)

This flag indicates whether the control program was downloaded to the RAM or not, using the download function.

Check Sum Consistency Bit (SR12)

This flag indicates whether the check sum matches or not when a program, is downloaded for execution using the download function.

ID Check Completed Bits (SR11 and SR10)

These flags indicate the result of ID checks. Some commands cannot be accepted without an ID check.

Data Reception Time Out (SR9)

This flag indicates when a time out error is generated during data reception. If this flag is attached during data reception, the received data is discarded and the microcomputer returns to the command wait state.

Example Circuit Application for The Standard Serial I/O Mode 1

The below figure shows a circuit application for the standard serial I/O mode 1. Control pins will vary according to programmer, therefore see the peripheral unit manual for more information.

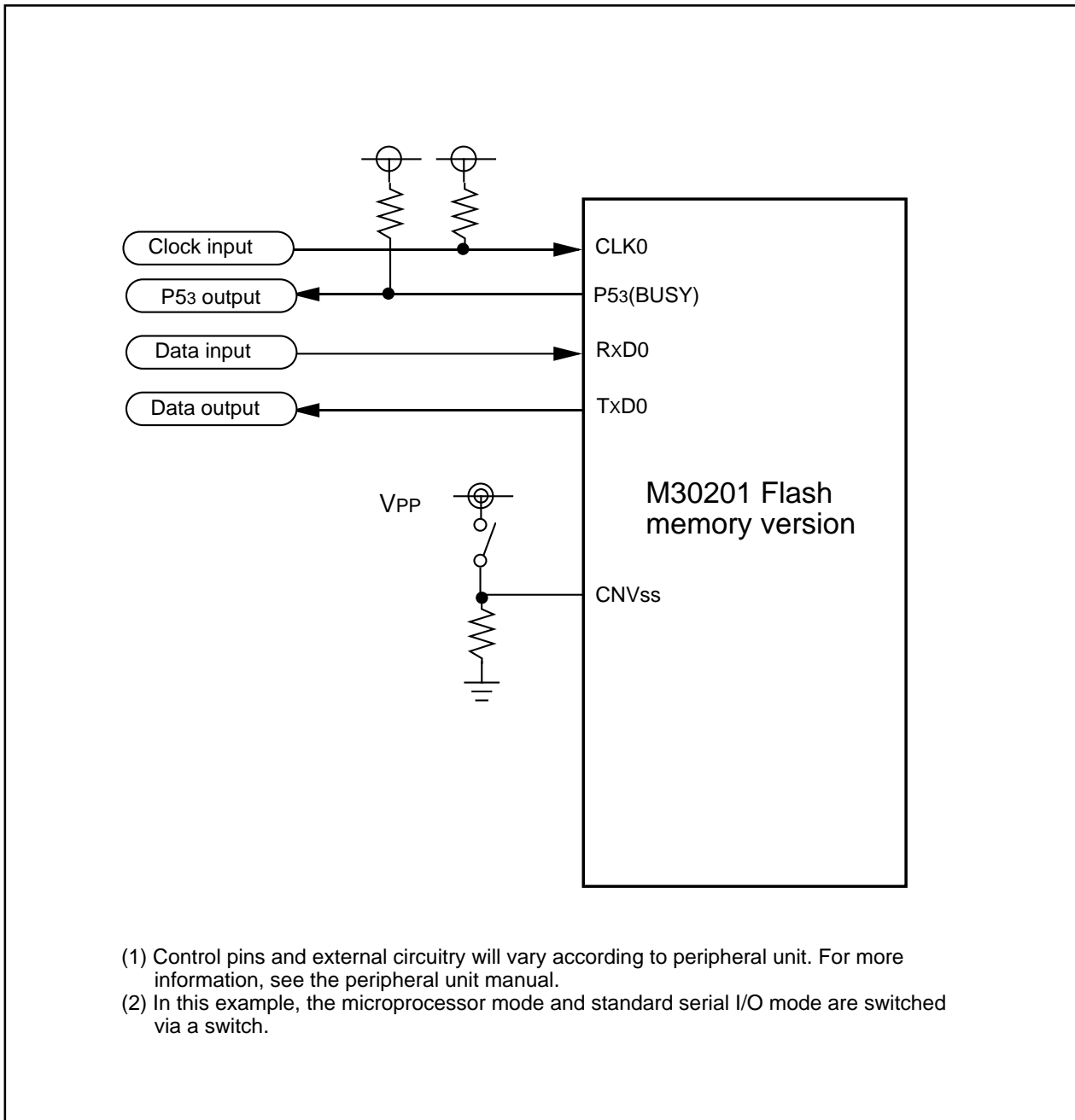


Figure 1.118. Example circuit application for the standard serial I/O mode 1

Overview of standard serial I/O mode 2 (clock asynchronous)

In standard serial I/O mode 2, software commands, addresses and data are input and output between the MCU and peripheral units (serial programmer, etc.) using 2-wire clock-asynchronized serial I/O (UART0). Standard serial I/O mode 2 is engaged by releasing the reset with the P5₃ (BUSY) pin "L" level.

The TxD₀ pin is for CMOS output. Data transfer is in 8-bit units with LSB first, 1 stop bit and parity OFF.

After the reset is released, connections can be established at 9,600 bps when initial communications (Figure 1.119) are made with a peripheral unit. However, this requires a main clock with a minimum 2 MHz input oscillation frequency. Baud rate can also be changed from 9,600 bps to 19,200, 38,400 or 57,600 bps by executing software commands. However, communication errors may occur because of the oscillation frequency of the main clock. If errors occur, change the main clock's oscillation frequency and the baud rate. After executing commands from a peripheral unit that requires time to erase and write data, as with erase and program commands, allow a sufficient time interval or execute the read status command and check how processing ended, before executing the next command.

Data and status registers in memory can be read after transmitting software commands. Status, such as the operating state of the flash memory or whether a program or erase operation ended successfully or not, can be checked by reading the status register. Here following are explained initial communications with peripheral units, how frequency is identified and software commands.

Initial communications with peripheral units

After the reset is released, the bit rate generator is adjusted to 9,600 bps to match the oscillation frequency of the main clock, by sending the code as prescribed by the protocol for initial communications with peripheral units (Figure 1.119).

- (1) Transmit "B0₁₆" from a peripheral unit. If the oscillation frequency input by the main clock is 10 MHz, the MCU with internal flash memory outputs the "B0₁₆" check code. If the oscillation frequency is anything other than 10 MHz, the MCU does not output anything.
- (2) Transmit "00₁₆" from a peripheral unit 16 times. (The MCU with internal flash memory sets the bit rate generator so that "00₁₆" can be successfully received.)
- (3) The MCU with internal flash memory outputs the "B0₁₆" check code and initial communications end successfully *1. Initial communications must be transmitted at a speed of 9,600 bps and a transfer interval of a minimum 15 ms. Also, the baud rate at the end of initial communications is 9,600 bps.

*1. If the peripheral unit cannot receive "B0₁₆" successfully, change the oscillation frequency of the main clock.

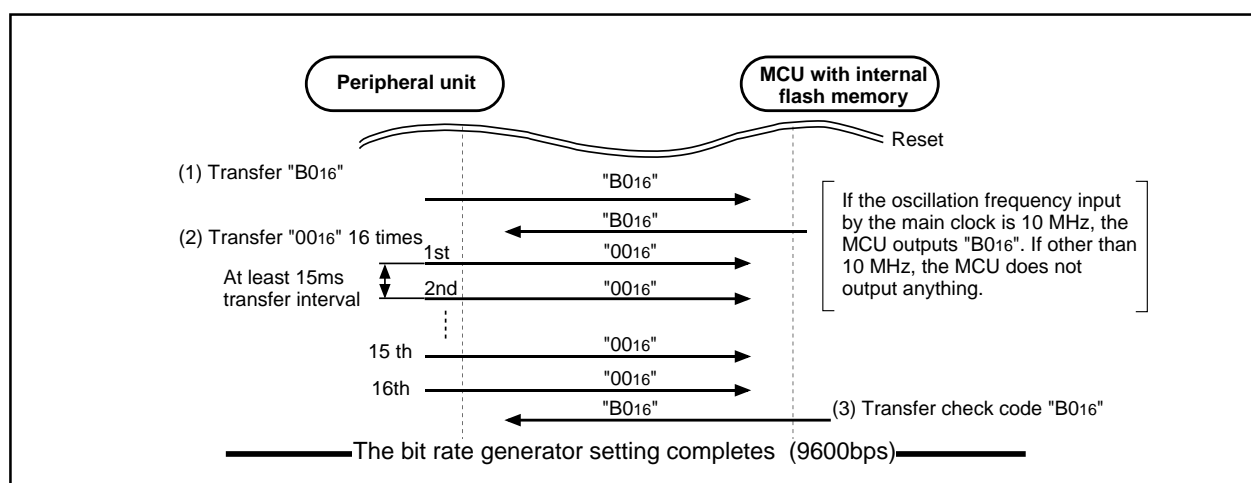


Figure 1.119. Peripheral unit and initial communication

How frequency is identified

When "0016" data is received 16 times from a peripheral unit at a baud rate of 9,600 bps, the value of the bit rate generator is set to match the operating frequency (2 - 10 MHz). The highest speed is taken from the first 8 transmissions and the lowest from the last 8. These values are then used to calculate the bit rate generator value for a baud rate of 9,600 bps.

Baud rate cannot be attained with some operating frequencies. Table 1.82 gives the operation frequency and the baud rate that can be attained for.

Table 1.82 Operation frequency and the baud rate

Operation frequency (MHz)	Baud rate 9,600bps	Baud rate 19,200bps	Baud rate 38,400bps	Baud rate 57,600bps
10MHz	√	√	—	√
8MHz	√	√	—	√
7.3728MHz	√	√	√	√
6MHz	√	√	√	—
5MHz	√	√	—	—
4.5MHz	√	√	—	√
4.194304MHz	√	√	√	—
4MHz	√	√	—	—
3.58MHz	√	√	√	√
3MHz	√	√	√	—
2MHz	√	—	—	—

√ : Communications possible

— : Communications not possible

Appendix Standard Serial I/O Mode 2 (Flash Memory Version)

Software Commands

Table 1.83 lists software commands. In the standard serial I/O mode 2, erase operations, programs and reading are controlled by transferring software commands via the RxD₀ pin. Standard serial I/O mode 2 adds four transmission speed commands - 9,600, 19,200, 38,400 and 57,600 bps - to the software commands of standard serial I/O mode 1. Software commands are explained here below.

Table 1.83. Software commands (Standard serial I/O mode 2)

	Control command	1st byte transfer	2nd byte	3rd byte	4th byte	5th byte	6th byte		When ID is not verified
1	Page read	FF ₁₆	Address (middle)	Address (high)	Data output	Data output	Data output	Data output to 259th byte	Not acceptable
2	Page program	41 ₁₆	Address (middle)	Address (high)	Data input	Data input	Data input	Data input to 259th byte	Not acceptable
3	Erase all unlocked blocks	A7 ₁₆	D0 ₁₆						Not acceptable
4	Read status register	70 ₁₆	SRD output	SRD1 output					Acceptable
5	Clear status register	50 ₁₆							Not acceptable
6	Read lock bit status	71 ₁₆	Address (middle)	Address (high)	Lock bit data output				Not acceptable
7	Code processing function	F5 ₁₆	Address (low)	Address (middle)	Address (high)	ID size	ID1	To ID7	Acceptable
8	Download function	FA ₁₆	Size (low)	Size (high)	Check-sum	Data input	To required number of times		Not acceptable
9	Version data output function	FB ₁₆	Version data output	Version data output	Version data output	Version data output	Version data output	Version data output to 9th byte	Acceptable
10	Boot ROM area output function	FC ₁₆	Address (middle)	Address (high)	Data output	Data output	Data output	Data output to 259th byte	Not acceptable
11	Baud rate 9600	B0 ₁₆	B0 ₁₆						Acceptable
12	Baud rate 19200	B1 ₁₆	B1 ₁₆						Acceptable
13	Baud rate 38400	B2 ₁₆	B2 ₁₆						Acceptable
14	Baud rate 57600	B3 ₁₆	B3 ₁₆						Acceptable

Note 1: Shading indicates transfer from flash memory microcomputer to peripheral unit. All other data is transferred from the peripheral unit to the flash memory microcomputer.

Note 2: SRD refers to status register data. SRD1 refers to status register 1 data.

Note 3: All commands can be accepted when the flash memory is totally blank.

Page Read Command

This command reads the specified page (256 bytes) in the flash memory sequentially one byte at a time. Execute the page read command as explained here following.

- (1) Transfer the "FF16" command code with the 1st byte.
- (2) Transfer addresses A8 to A15 and A16 to A23 with the 2nd and 3rd bytes respectively.
- (3) From the 4th byte onward, data (D0–D7) for the page (256 bytes) specified with addresses A8 to A23 will be output sequentially from the smallest address first in sync with the fall of the clock.

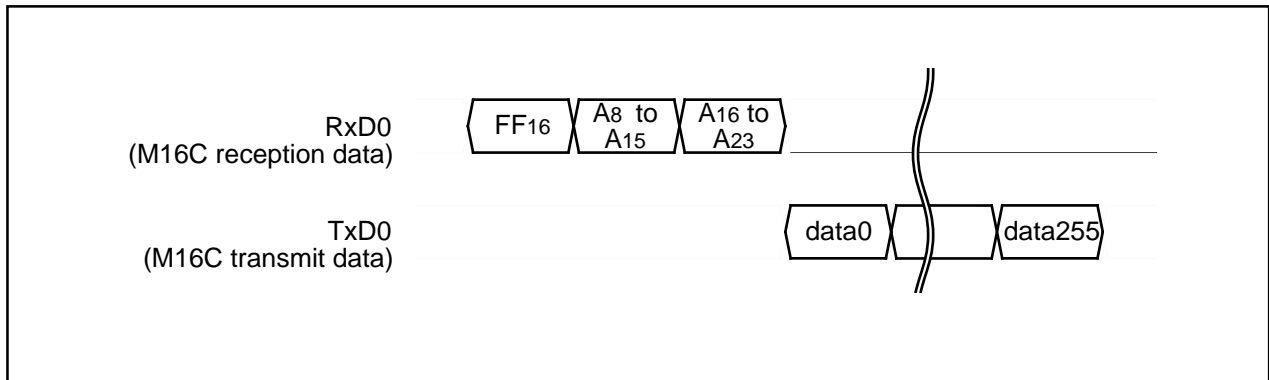


Figure 1.120. Timing for page read

Read Status Register Command

This command reads status information. When the "7016" command code is sent with the 1st byte, the contents of the status register (SRD) specified with the 2nd byte and the contents of status register 1 (SRD1) specified with the 3rd byte are read.

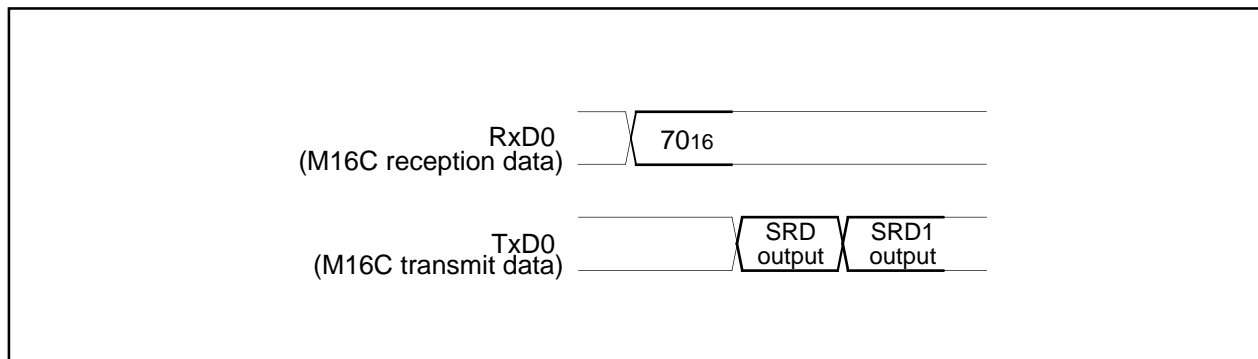


Figure 1.121. Timing for reading the status register

Clear Status Register Command

This command clears the bits (SR3–SR4) which are set when the status register operation ends in error. When the “5016” command code is sent with the 1st byte, the aforementioned bits are cleared. When the clear status register operation ends, the RTS₁ (BUSY) signal changes from the “H” to the “L” level.

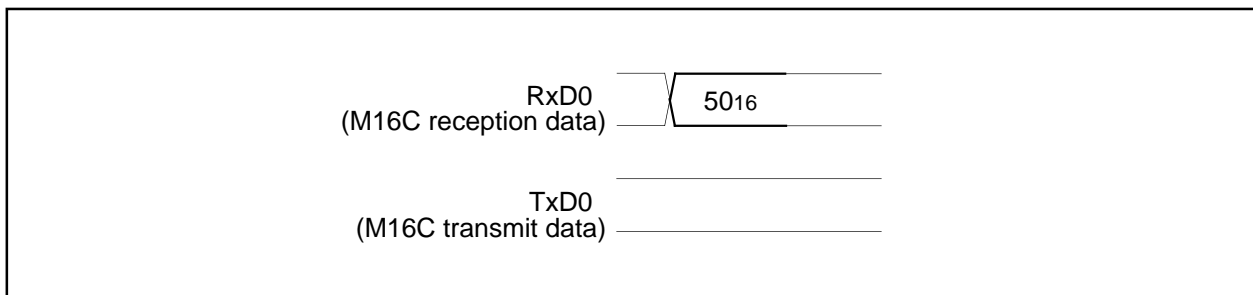


Figure 1.122. Timing for clearing the status register

Page Program Command

This command writes the specified page (256 bytes) in the flash memory sequentially one byte at a time. Execute the page program command as explained here following.

- (1) Transfer the “4116” command code with the 1st byte.
- (2) Transfer addresses A₈ to A₁₅ and A₁₆ to A₂₃ with the 2nd and 3rd bytes respectively.
- (3) From the 4th byte onward, as write data (D₀–D₇) for the page (256 bytes) specified with addresses A₈ to A₂₃ is input sequentially from the smallest address first, that page is automatically written.

When reception setup for the next 256 bytes ends, the RTS₁ (BUSY) signal changes from the “H” to the “L” level. The result of the page program can be known by reading the status register. For more information, see the section on the status register.

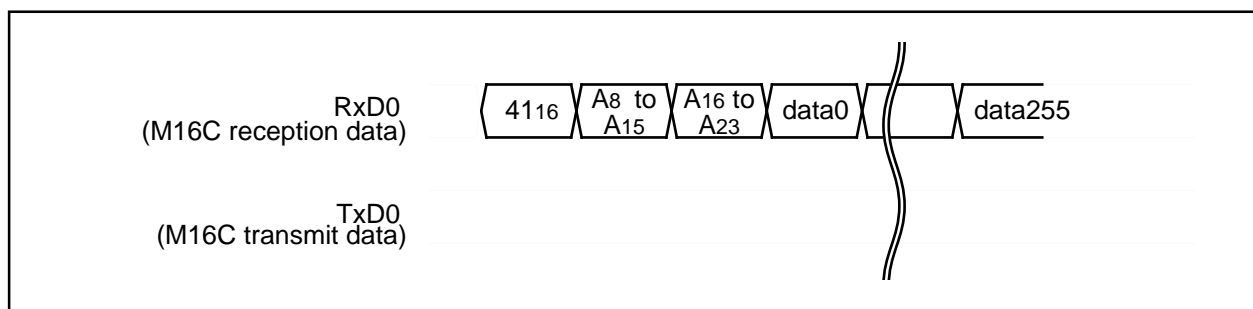


Figure 1.123. Timing for the page program

Appendix Standard Serial I/O Mode 2 (Flash Memory Version)

Erase All Unlocked Blocks Command

This command erases the content of all blocks. Execute the erase all unlocked blocks command as explained here following.

- (1) Transfer the "A716" command code with the 1st byte.
- (2) Transfer the verify command code "D016" with the 2nd byte. With the verify command code, the erase operation will start and continue for all blocks in the flash memory.

When block erasing ends, the RTS₁ (BUSY) signal changes from the "H" to the "L" level. The result of the erase operation can be known by reading the status register.



Figure 1.124. Timing for erasing all unlocked blocks

Read Lock Bit Status Command

This command reads the lock bit status of the specified block. Execute the read lock bit status command as explained here following.

- (1) Transfer the "7116" command code with the 1st byte.
- (2) Transfer addresses A8 to A15 and A16 to A23 with the 2nd and 3rd bytes respectively.
- (3) The lock bit data of the specified block is output with the 4th byte. Write the highest address of the specified block for addresses A8 to A23.

The M30201 (flash memory version) does not have the lock bit, so the read value is always "1" (block unlock).

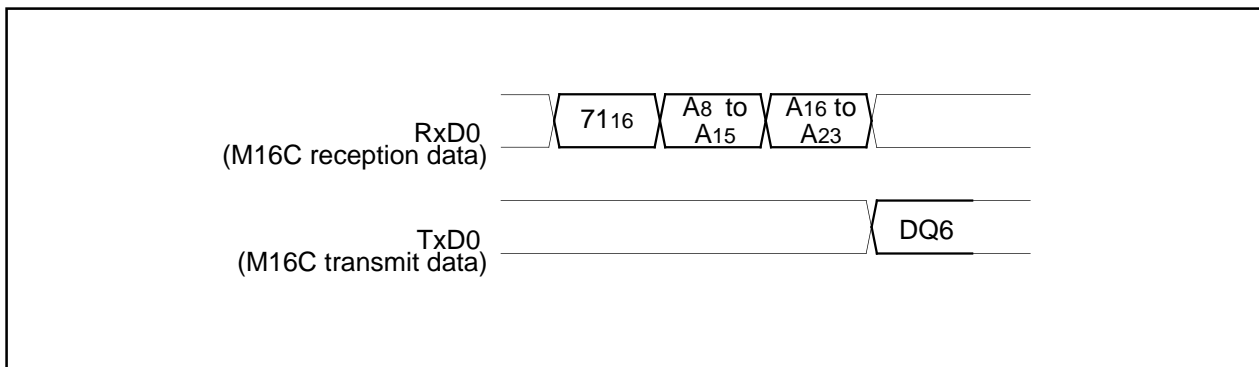


Figure 1.125. Timing for reading lock bit status

Download Command

This command downloads a program to the RAM for execution. Execute the download command as explained here following.

- (1) Transfer the "FA16" command code with the 1st byte.
- (2) Transfer the program size with the 2nd and 3rd bytes.
- (3) Transfer the check sum with the 4th byte. The check sum is added to all data sent with the 5th byte onward.
- (4) The program to execute is sent with the 5th byte onward.

When all data has been transmitted, if the check sum matches, the downloaded program is executed. The size of the program will vary according to the internal RAM.

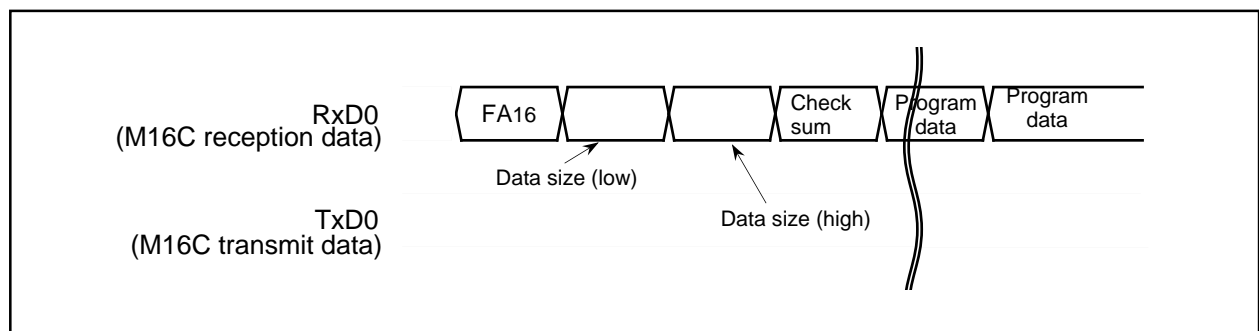


Figure 1.126. Timing for download

Version Information Output Command

This command outputs the version information of the control program stored in the boot area. Execute the version information output command as explained here following.

- (1) Transfer the "FB16" command code with the 1st byte.
- (2) The version information will be output from the 2nd byte onward. This data is composed of 8 ASCII code characters.

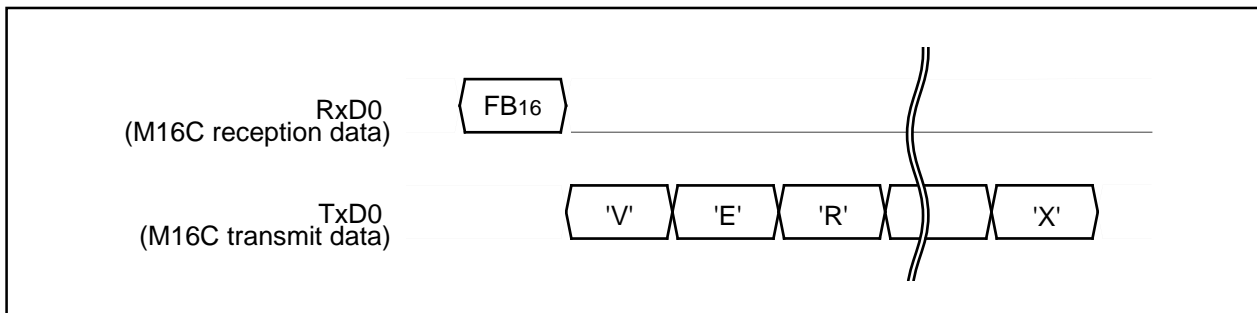


Figure 1.127. Timing for version information output

Boot ROM Area Output Command

This command outputs the control program stored in the boot ROM area in one page blocks (256 bytes). Execute the boot ROM area output command as explained here following.

- (1) Transfer the "FC16" command code with the 1st byte.
- (2) Transfer addresses A8 to A15 and A16 to A23 with the 2nd and 3rd bytes respectively.
- (3) From the 4th byte onward, data (D0–D7) for the page (256 bytes) specified with addresses A8 to A23 will be output sequentially from the smallest address first.

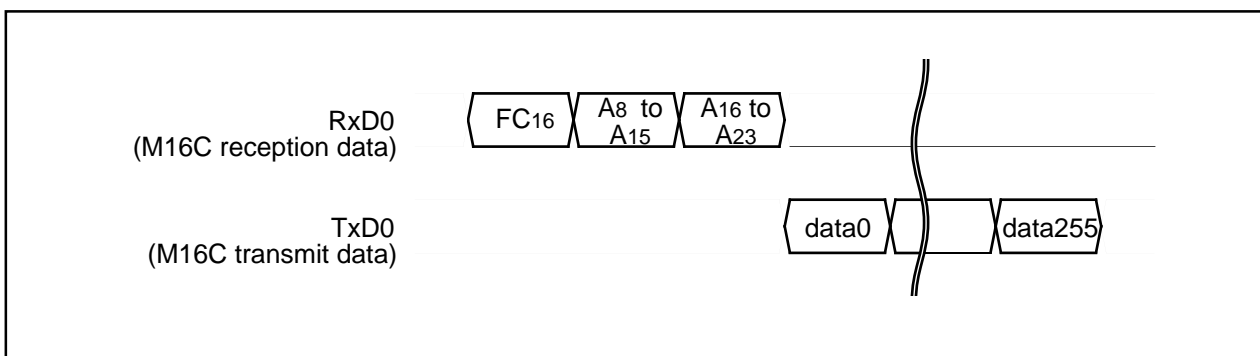


Figure 1.128. Timing for boot ROM area output

Appendix Standard Serial I/O Mode 2 (Flash Memory Version)

ID Check

This command checks the ID code. Execute the boot ID check command as explained here following.

- (1) Transfer the "F5₁₆" command code with the 1st byte.
- (2) Transfer addresses A₀ to A₇, A₈ to A₁₅ and A₁₆ to A₂₃ of the 1st byte of the ID code with the 2nd, 3rd and 4th bytes respectively.
- (3) Transfer the number of data sets of the ID code with the 5th byte.
- (4) The ID code is sent with the 6th byte onward, starting with the 1st byte of the code.

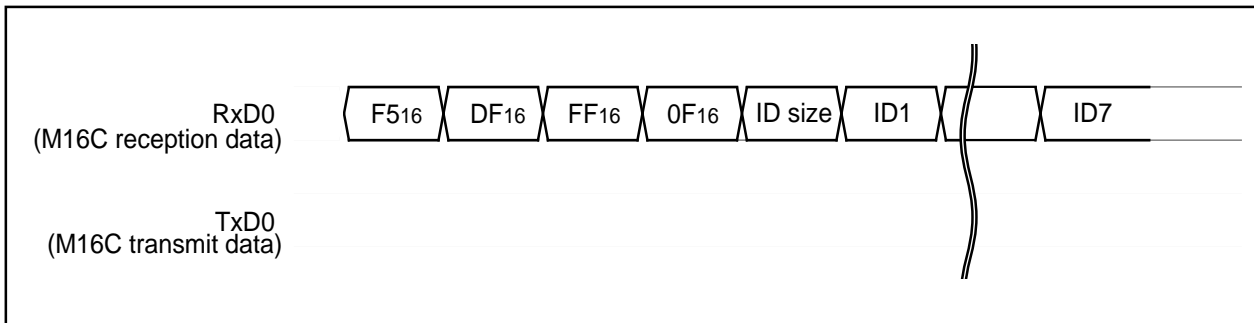


Figure 1.129. Timing for the ID check

ID Code

When the flash memory is not blank, the ID code sent from the peripheral units and the ID code written in the flash memory are compared to see if they match. If the codes do not match, the command sent from the peripheral units is not accepted. An ID code contains 8 bits of data. Area is, from the 1st byte, addresses 0FFFD₁₆, 0FFFE₃₁₆, 0FFFE_{B16}, 0FFFE_{F16}, 0FFFF₃₁₆, 0FFFF₇₁₆ and 0FFFF_{B16}. Write a program into the flash memory, which already has the ID code set for these addresses.

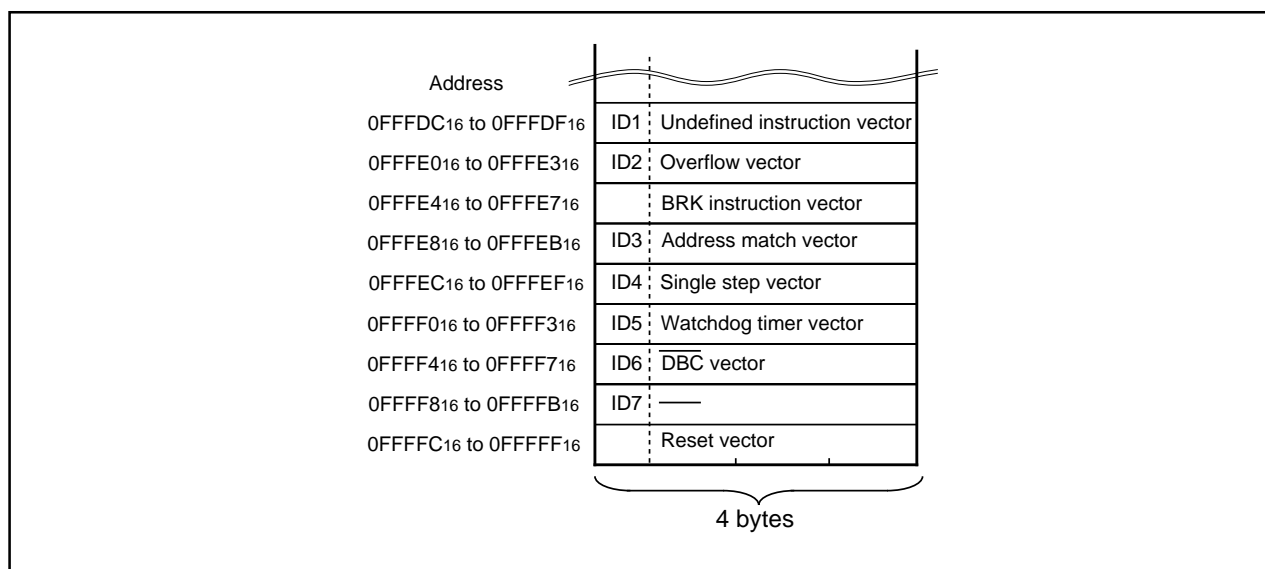


Figure 1.130. ID code storage addresses

Appendix Standard Serial I/O Mode 2 (Flash Memory Version)

Baud Rate 9600

This command changes baud rate to 9,600 bps. Execute it as follows.

- (1) Transfer the "B016" command code with the 1st byte.
- (2) After the "B016" check code is output with the 2nd byte, change the baud rate to 9,600 bps.

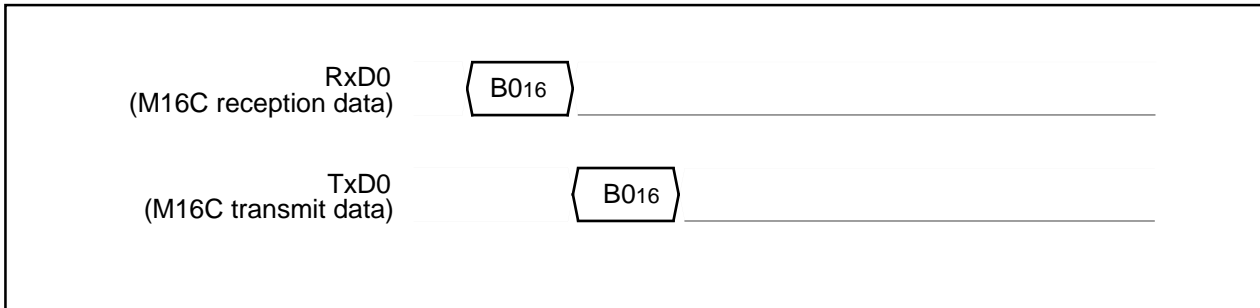


Figure 1.131. Timing of baud rate 9600

Baud Rate 19200

This command changes baud rate to 19,200 bps. Execute it as follows.

- (1) Transfer the "B116" command code with the 1st byte.
- (2) After the "B116" check code is output with the 2nd byte, change the baud rate to 19,200 bps.



Figure 1.132. Timing of baud rate 19200

Baud Rate 38400

This command changes baud rate to 38,400 bps. Execute it as follows.

- (1) Transfer the "B216" command code with the 1st byte.
- (2) After the "B216" check code is output with the 2nd byte, change the baud rate to 38,400 bps.

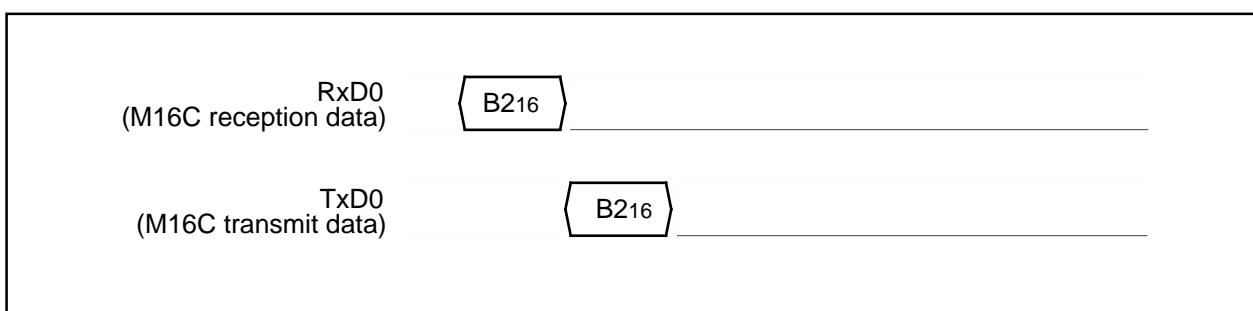


Figure 1.133. Timing of baud rate 38400

Baud Rate 57600

This command changes baud rate to 57,600 bps. Execute it as follows.

- (1) Transfer the "B316" command code with the 1st byte.
- (2) After the "B316" check code is output with the 2nd byte, change the baud rate to 57,600 bps.

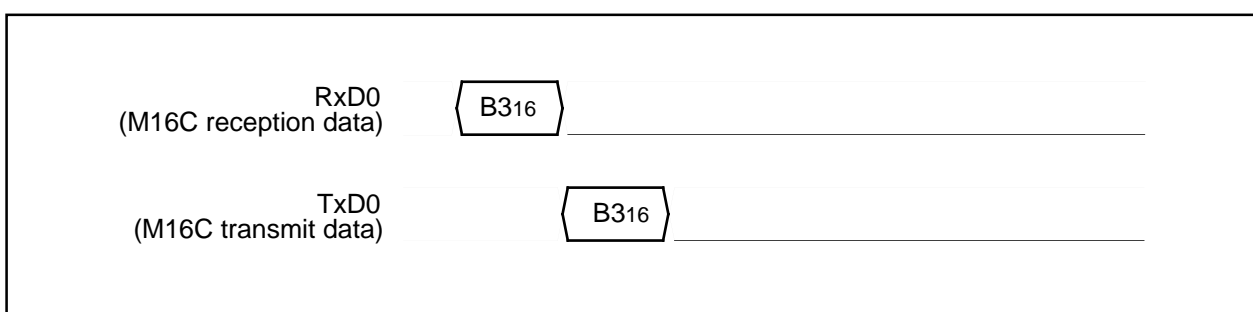


Figure 1.134. Timing of baud rate 57600

Example Circuit Application for The Standard Serial I/O Mode 2

The below figure shows a circuit application for the standard serial I/O mode 2.

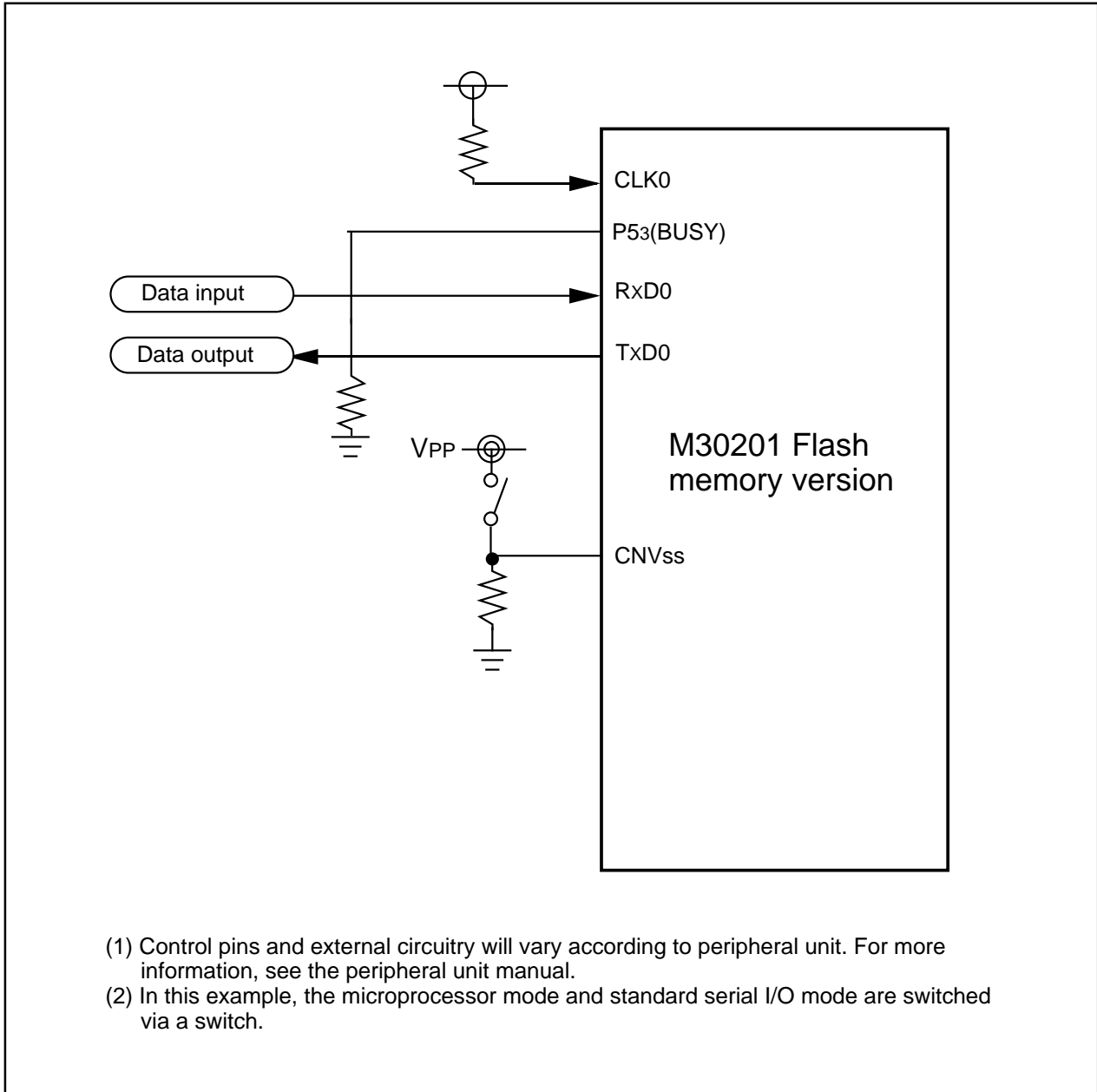


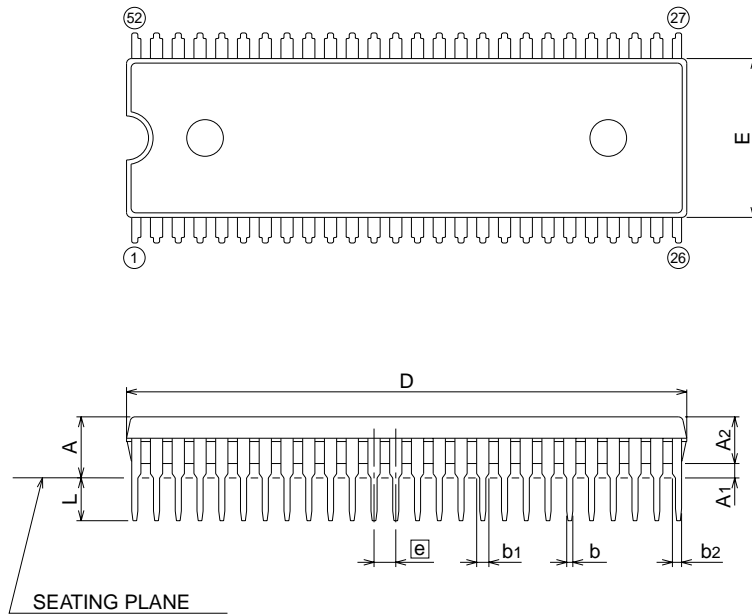
Figure 1.135. Example circuit application for the standard serial I/O mode 2

52P4B

(MMP)

Plastic 52pin 600mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP52-P-600-1.78	-	5.1	Alloy 42/Cu Alloy

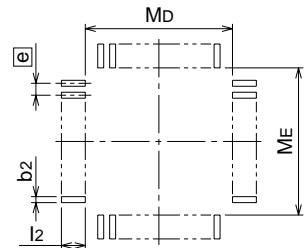
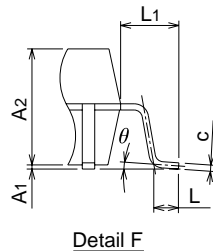
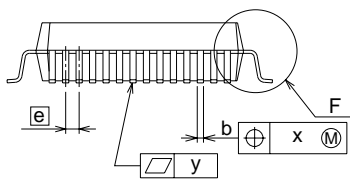
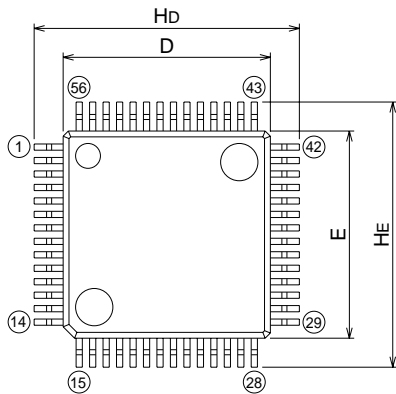


Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	5.5
A1	0.51	-	-
A2	-	3.8	-
b	0.4	0.5	0.59
b1	0.9	1.0	1.3
b2	0.65	0.75	1.05
c	0.22	0.27	0.34
D	45.65	45.85	46.05
E	12.85	13.0	13.15
e	-	1.778	-
e1	-	15.24	-
L	3.0	-	-
θ	0°	-	15°

56P6S-A

Plastic 56pin 10X10mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP56-P-1010-0.65	-	0.59	Alloy 42



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	3.05
A1	0	0.1	0.2
A2	-	2.8	-
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	9.8	10.0	10.2
E	9.8	10.0	10.2
e	-	0.65	-
Hd	12.5	12.8	13.1
HE	12.5	12.8	13.1
L	0.4	0.6	0.8
L1	-	1.4	-
x	-	-	0.13
y	-	-	0.1
θ	0°	-	10°
b2	-	0.35	-
l2	1.3	-	-
Md	-	10.6	-
ME	-	10.6	-

Chapter 2

Peripheral Functions Usage

Protect

2.1 Protect

2.1.1 Overview

'Protect' is a function that causes a value held in a register to be unchanged even when a program runs away. The following is an overview of the protect function:

(1) Registers affected by the protect function

The registers affected by the protect function are:

- (a) System clock control registers 0, 1 (addresses 0006₁₆ and 0007₁₆)
- (b) Processor mode registers 0, 1 (addresses 0004₁₆ and 0005₁₆)
- (c) Port P4 direction register (address 03EA₁₆)

The values in registers (1) through (3) cannot be changed in write-protect state. To change values in the registers, put the individual registers in write-enabled state.

(2) Protect register

Figure 2.1.1 shows protect register.

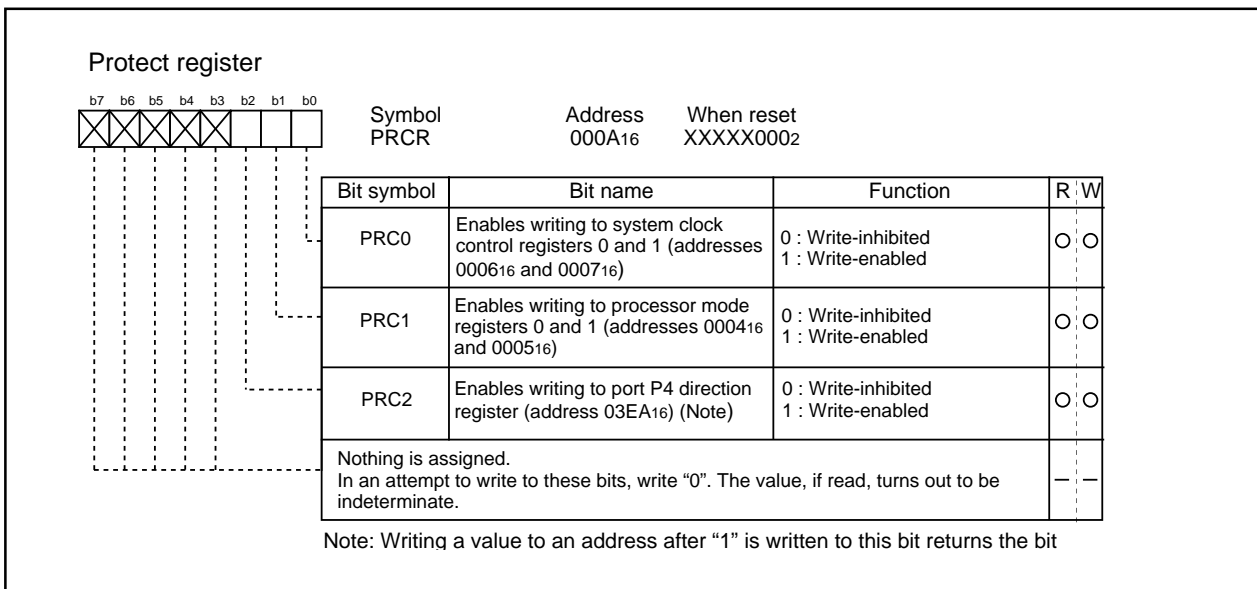


Figure 2.1.1. Protect register

2.1.2 Protect Operation

The following explains the protect operation. Figure 2.1.2 shows the set-up procedure.

- Operation
- (1) Setting "1" in the write-enable bit of system clock control registers 0 and 1 causes system clock control register 0 and system clock control register 1 to be in write-enabled state.
 - (2) The contents of system clock control register 0 and that of system clock control register 1 are changed.
 - (3) Setting "0" in the write-enable bit of system control registers 0 and 1 causes system clock control register 0 and system control register 1 to be in write-inhibited state.
 - (4) To change the contents of processor mode register 0 and that of processor mode register 1, follow the same steps as in dealing with system clock control registers.
 - (5) The write-enable bit of port P4 direction register goes to "0" when the next write instruction is executed after write-enabled state is readied. Make changes in input/output immediately after the instruction that sets "1" in the write-enable bit of port P4 direction register (avoid causing an interrupt).

Protect

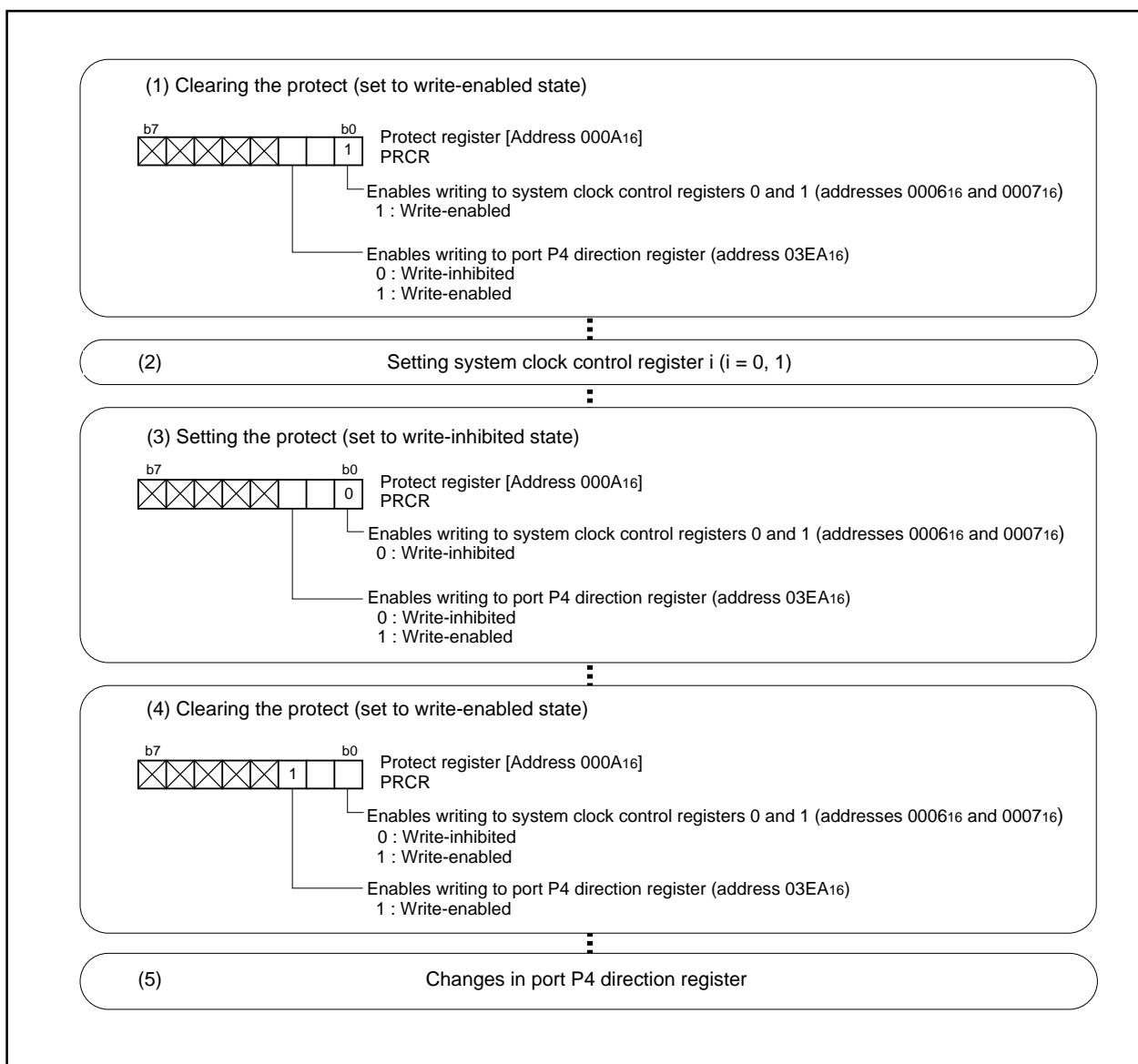


Figure 2.1.2. Set-up procedure for protect function

2.1.3 Precaution for Protect

- (1) The write-enable bit of port P4 direction register goes to “0” when the next write instruction is executed after write-enabled state is readied. Make changes in input/output immediately after the instruction that sets “1” in the write-enable bit of port P4 direction register (avoid causing an interrupt).

2.2 Timer A

2.2.1 Overview

The following is an overview for timer A, a 16-bit timer.

(1) Mode

Timer A operates in one of the four modes:

(a) Timer mode

In this mode, the internal count source is counted. Two functions can be selected: the pulse output function that reverses output from a port every time an overflow occurs, or the gate function which controls the count start/stop according to the input signal from a port.

- Timer mode operation P180
- Timer mode, gate function operation P182
- Timer mode, pulse output function operation P184

(b) Event counter mode

This mode counts the pulses from the outside and the number of overflows in other timers. The free-run type, in which nothing is reloaded from the reload register, can be selected when an underflow occurs. The pulse output function can also be selected. Please refer to the timer mode explanation for details, as the operation is identical.

- Event counter mode operation P186
- Event counter mode, free run type operation P188

Furthermore, Timer A has a 2-phase pulse signal processing function which generates an up count or down count in the event counter mode, depending on the phase of the two input signals.

- Operation of the 2-phase pulse signal processing function in normal event counter mode P190
- Operation of the 2-phase pulse signal processing function in 4-multiplication mode P192

(c) One-shot timer mode

In this mode, the timer is started by the trigger and stops when the timer goes to "0". The trigger can be selected from the following 3 types: an external input signal, an overflow of the timer, or a software trigger. The pulse output function can also be selected. Please refer to the timer mode explanation for details, as the operation is identical.

- Operation in one-shot timer mode effected by software P194
- Operation in one-shot timer mode effected by an external trigger P196

(d) Pulse width modulation (PWM) mode

In this mode, the arbitrary pulses are successively output. Either a 16-bit fixed-period PWM mode or 8-bit variable-period mode can be selected. The trigger for initiating output can also be selected. Please refer to the one-shot timer mode explanation for details, as the operation is identical.

- 16-bit PWM mode operation P198
- 8-bit PWM mode operation P200

Timer A

(2) Count source

The internal count source can be selected from f1, f8, f32, and fc32. Clocks f1, f8, and f32 are derived by dividing the CPU's main clock by 1, 8, and 32 respectively. Clock fc32 is derived by dividing the CPU's secondary clock by 32.

(3) Frequency division ratio

In timer mode or pulse width modulation mode, [the value set in the timer register + 1] becomes the frequency division ratio. In event counter mode, [the set value + 1] becomes the frequency division ratio when a down count is performed, or [FFFF₁₆ - the set value + 1] becomes the frequency division ratio when an up count is performed. In one-shot timer mode, the value set in the timer register becomes the frequency division ratio.

The counter overflows (or underflows) when a count source equal to a frequency division ratio is input, and an interrupt occurs. For the pulse output function, the output from the port varies (the value in the port register does not vary).

(4) Reading the timer

Either in timer mode or in event counter mode, reading the timer register takes out the count at that moment. Read it in 16-bit units. The data either in one-shot timer mode or in pulse width modulation mode is indeterminate.

(5) Writing to the timer

To write to the timer register when a count is in progress, the value is written only to the reload register. When writing to the timer register when a count is stopped, the value is written both to the reload register and to the counter. Write a value in 16-bit units.

(6) Relation between the input/output to/from the timer and the direction register

With the output function of the timer, set the direction register of the relevant port to input. To input an external signal to the timer, set the direction register of the relevant port to input.

(7) Pins related to timer A

- (a) TA0IN Input pins to timer A.
- (b) TA0OUT Output pins from timer A. They become input pins to timer A when event counter mode is active.

Timer A

(8) Registers related to timer A

Figure 2.2.1 shows the memory map of timer A-related registers. Figures 2.2.2 through 2.2.5 show timer A-related registers.

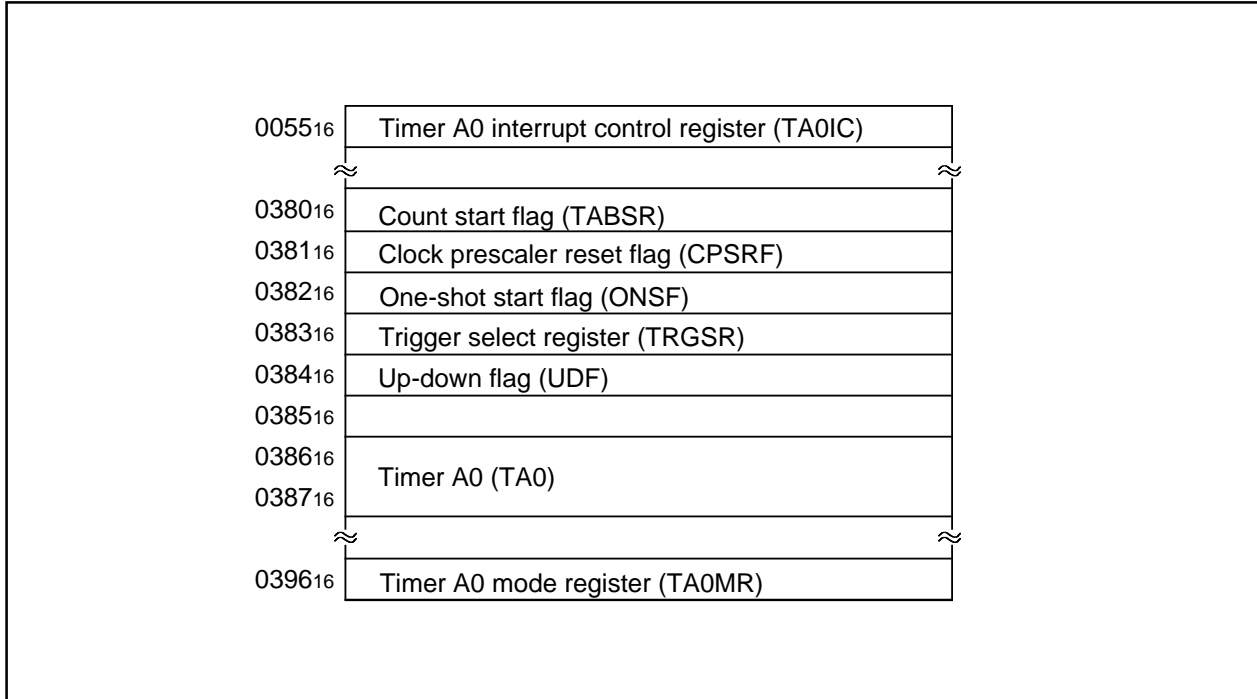


Figure 2.2.1. Memory map of timer A-related registers

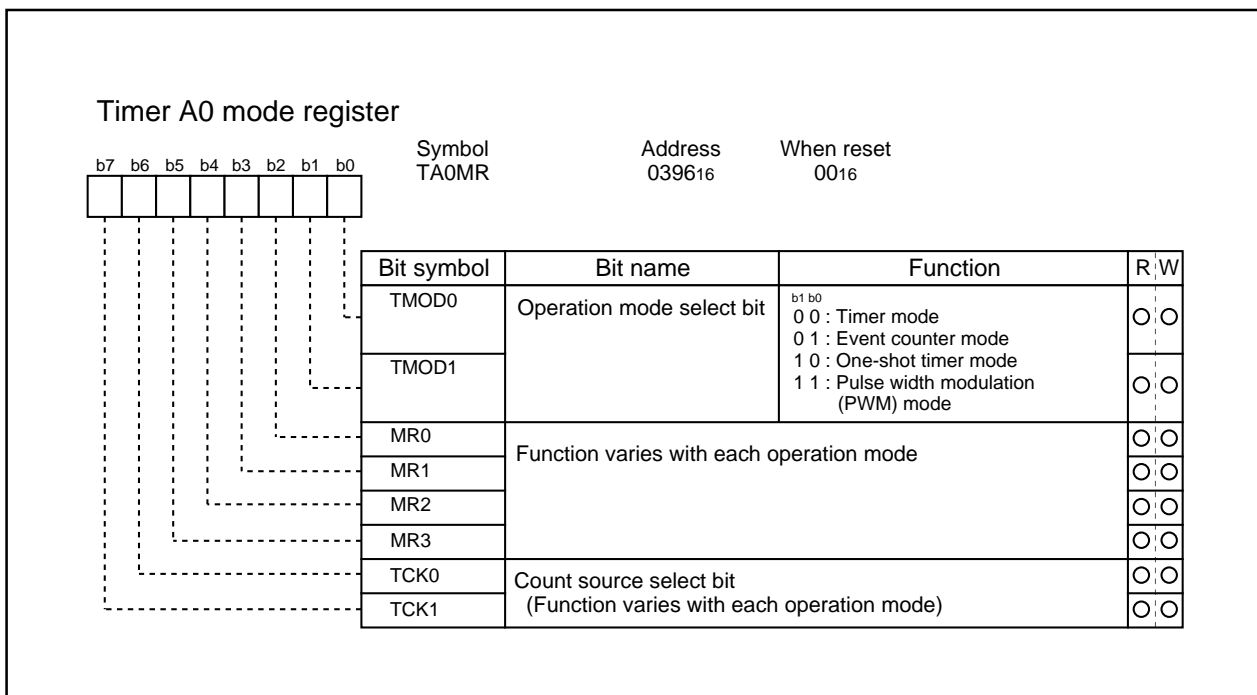


Figure 2.2.2. Timer A-related registers (1)

Timer A

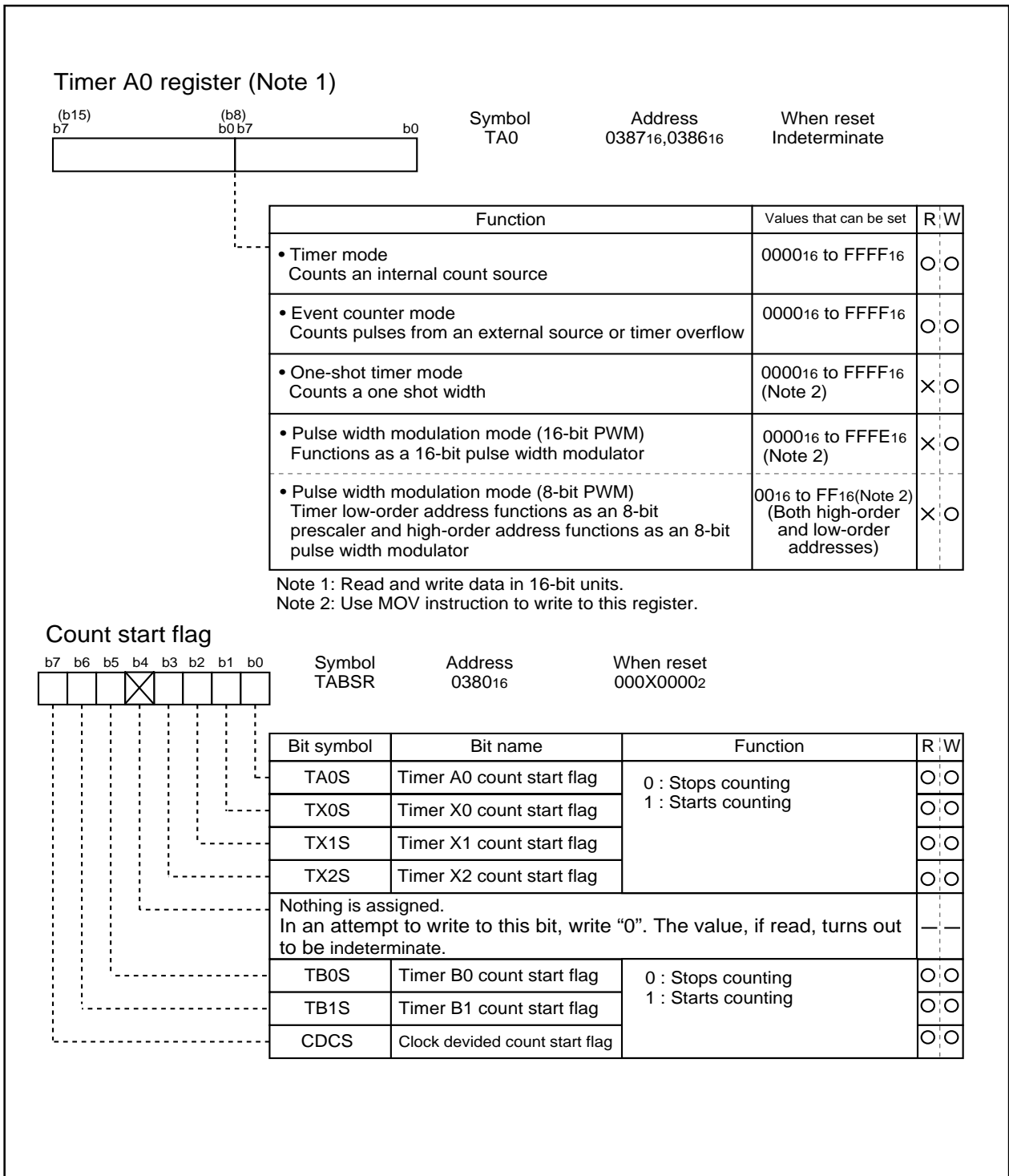


Figure 2.2.3. Timer A-related registers (2)

Timer A

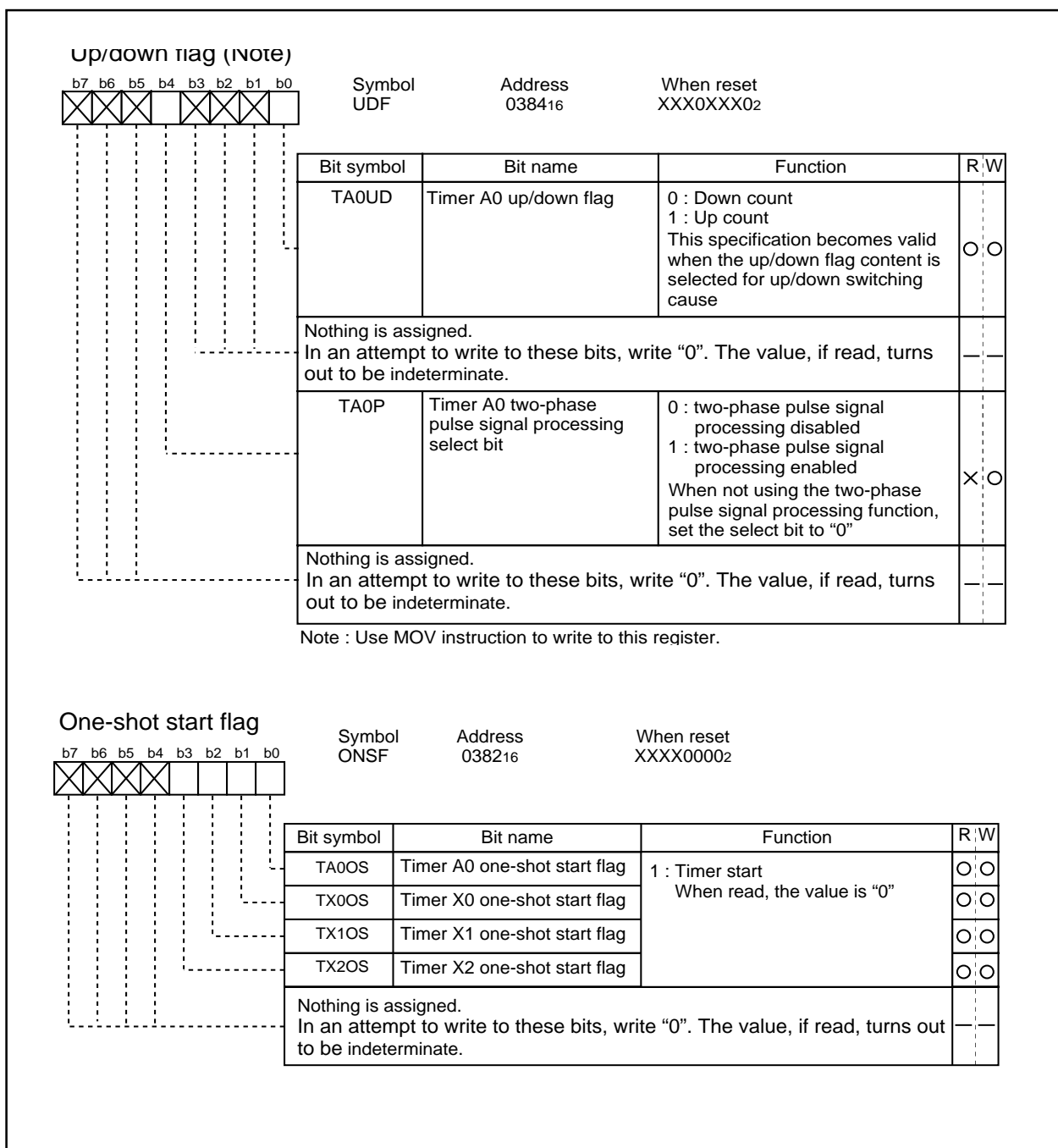


Figure 2.2.4. Timer A-related registers (3)

Timer A

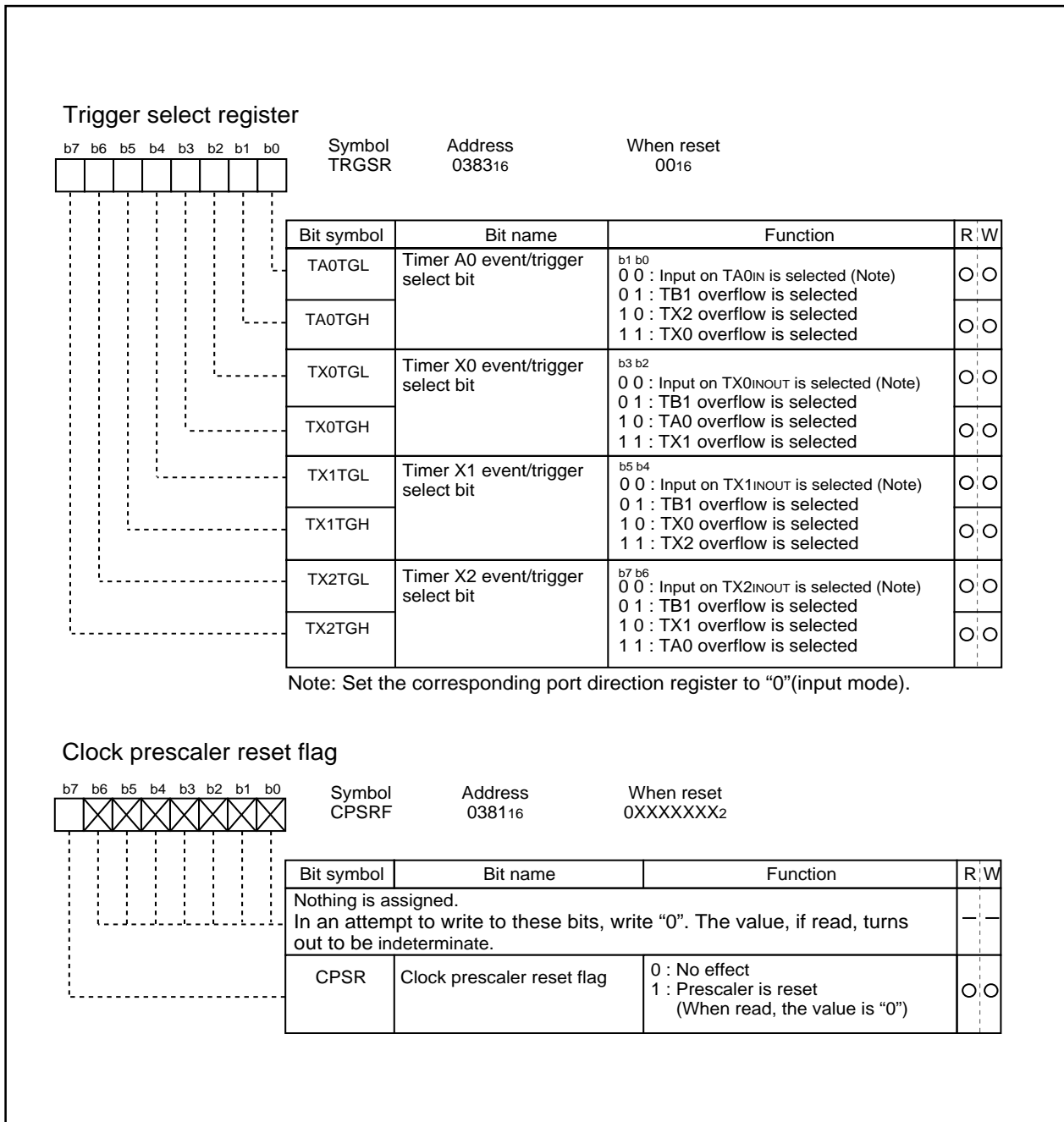


Figure 2.2.5. Timer A-related registers (4)

2.2.2 Operation of Timer A (timer mode)

In timer mode, choose functions from those listed in Table 2.2.1. Operations of the circled items are described below. Figure 2.2.6 shows the operation timing, and Figure 2.2.7 shows the set-up procedure.

Table 2.2.1. Chosed functions

Item	Set-up
Count source	○ Internal count source (f ₁ / f ₈ / f ₃₂ / f _{c32})
Pulse output function	○ No pulses output
	Pulses output
Gate function	○ No gate function
	Performs count only for the period in which the TA0IN pin is at "L" level
	Performs count only for the period in which the TA0IN pin is at "H" level

- Operation
- (1) Setting the count start flag to "1" causes the counter to perform a down count on the count source.
 - (2) If an underflow occurs, the content of the reload register is reloaded, and the count continues. At this time, the timer A0 interrupt request bit goes to "1".
 - (3) Setting the count start flag to "0" causes the counter to hold its value and to stop.

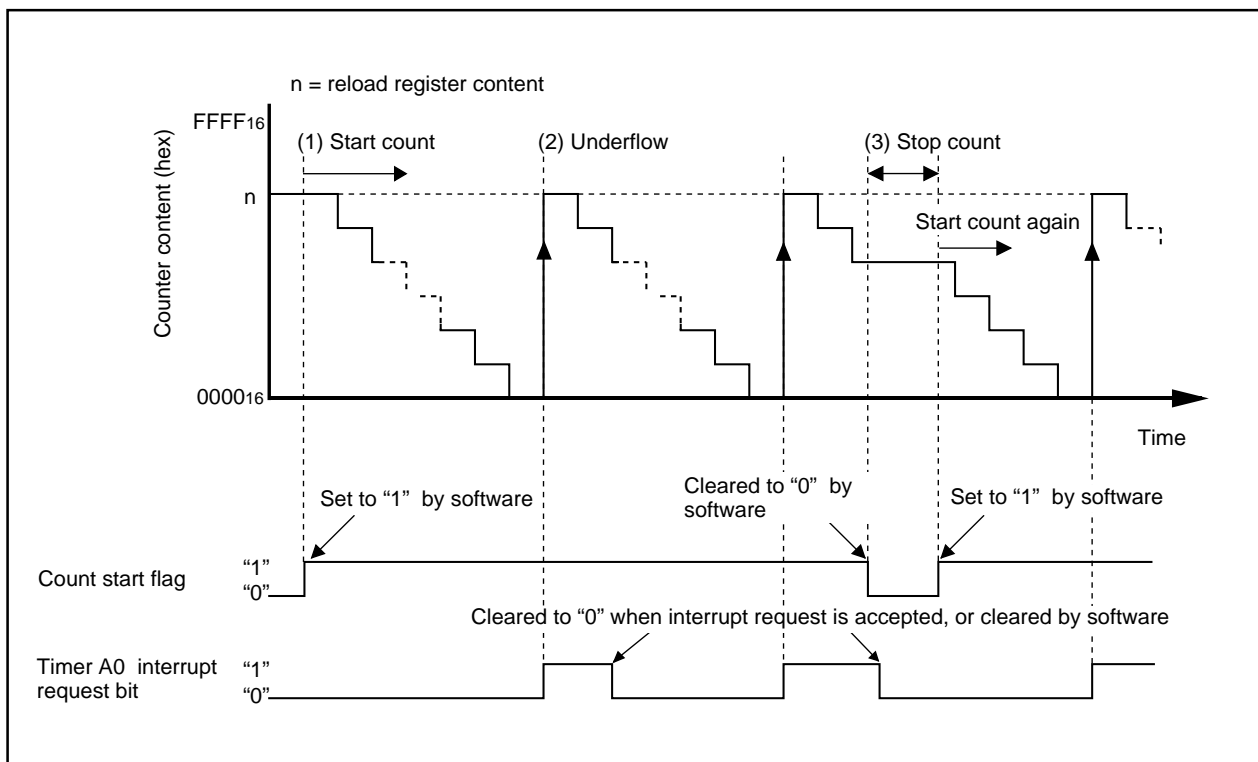


Figure 2.2.6. Operation timing of timer mode

Timer A

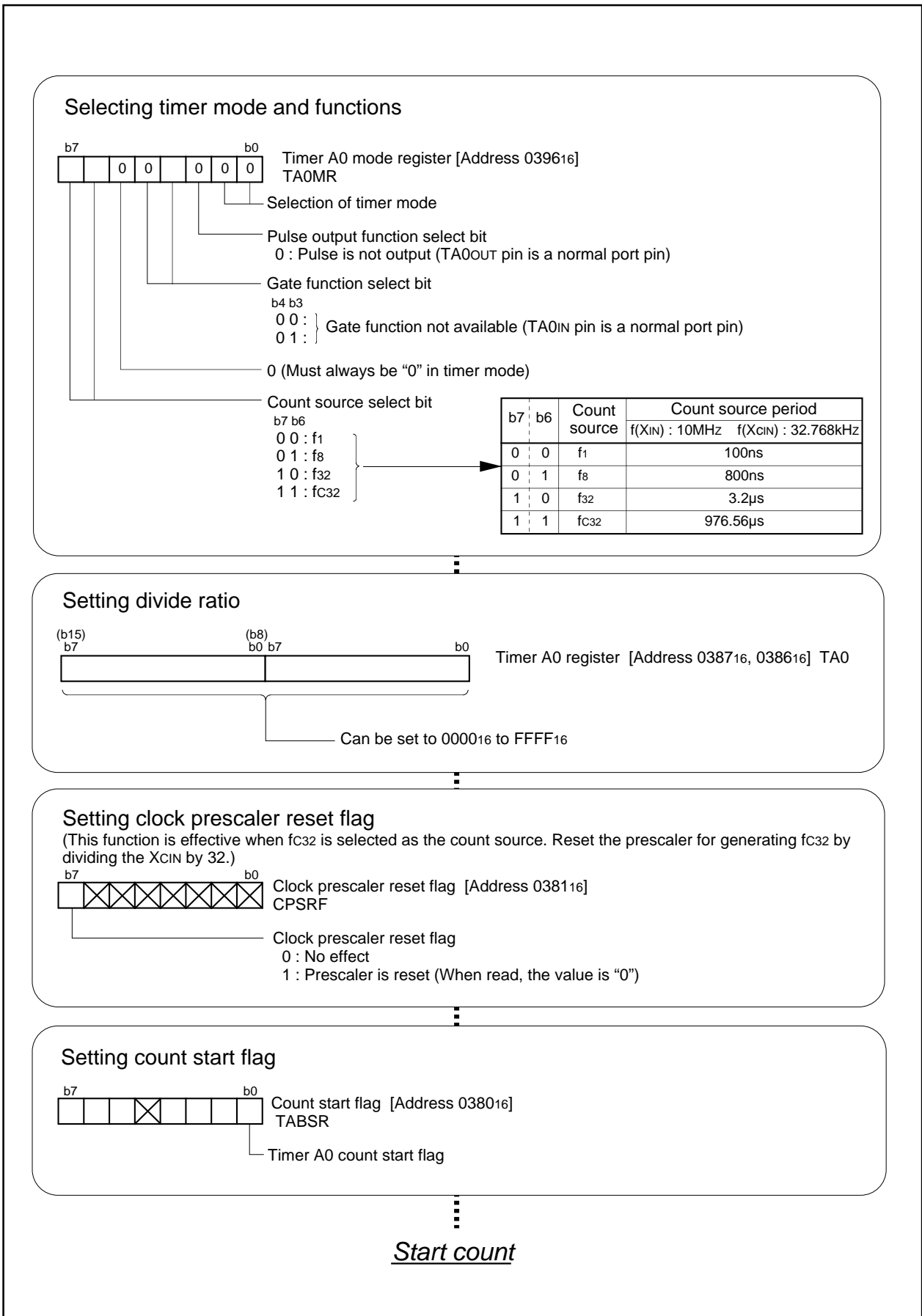


Figure 2.2.7. Set-up procedure of timer mode

Timer A

2.2.3 Operation of Timer A (timer mode, gate function selected)

In timer mode, choose functions from those listed in Table 2.2.2. Operations of the circled items are described below. Figure 2.2.8 shows the operation timing, and Figure 2.2.9 shows the set-up procedure.

Table 2.2.2. Chosed functions

Item	Set-up	
Count source	<input type="radio"/>	Internal count source($f_1 / f_8 / f_{32} / f_{c32}$)
Pulse output function	<input type="radio"/>	No pulses output
	<input type="radio"/>	Pulses output
Gate function	<input type="radio"/>	No gate function
	<input type="radio"/>	Performs count only for the period in which the TA0IN pin is at "L" level
	<input type="radio"/>	Performs count only for the period in which the TA0IN pin is at "H" level

- Operation
- (1) When the count start flag is set to "1" and the TA0IN pin inputs at "H" level, the counter performs a down count on the count source.
 - (2) When the TA0IN pin inputs at "L" level, the counter holds its value and stops.
 - (3) If an underflow occurs, the content of the reload register is reloaded and the count continues. At this time, the timer A0 interrupt request bit goes to "1".
 - (4) Setting the count start flag to "0" causes the counter to hold its value and to stop.

Note

- Make the pulse width of the signal input to the TA0IN pin not less than two cycles of the count source.

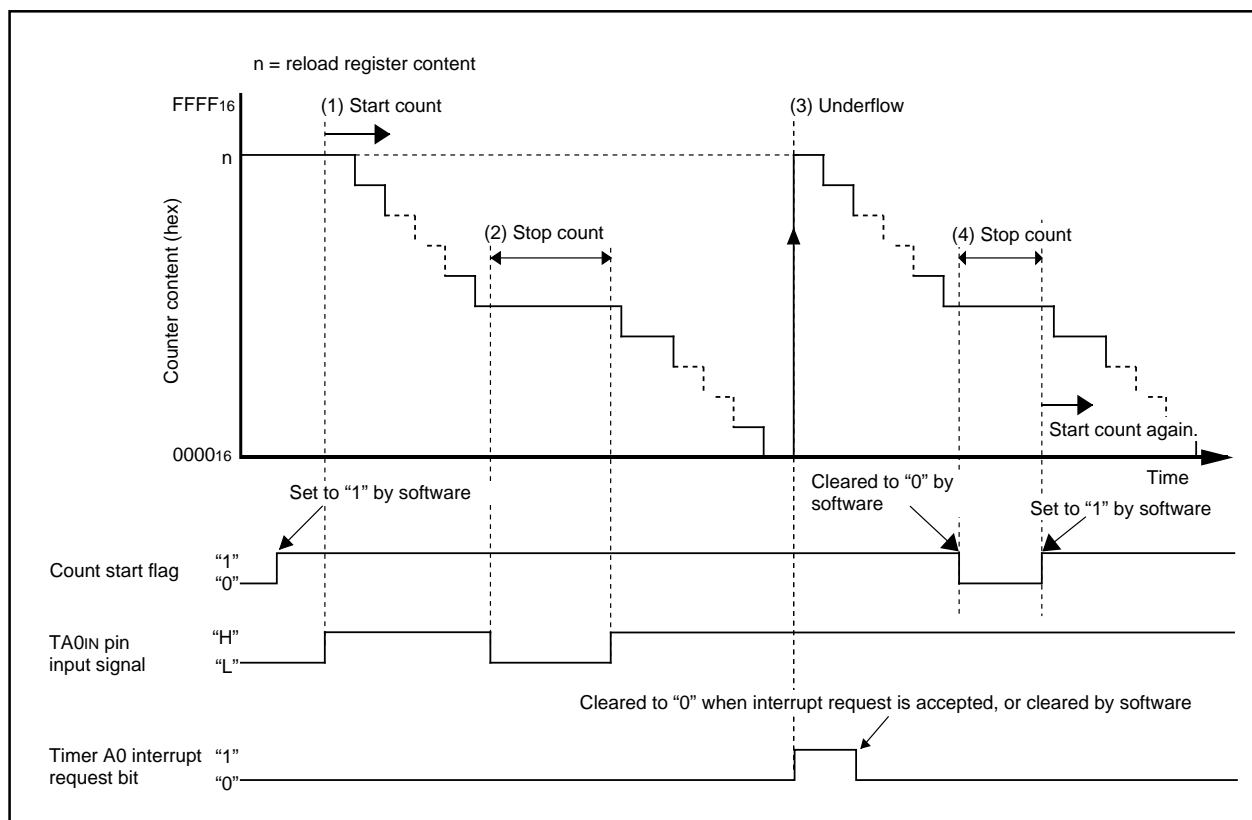


Figure 2.2.8. Operation timing of timer mode, gate function selected

Timer A

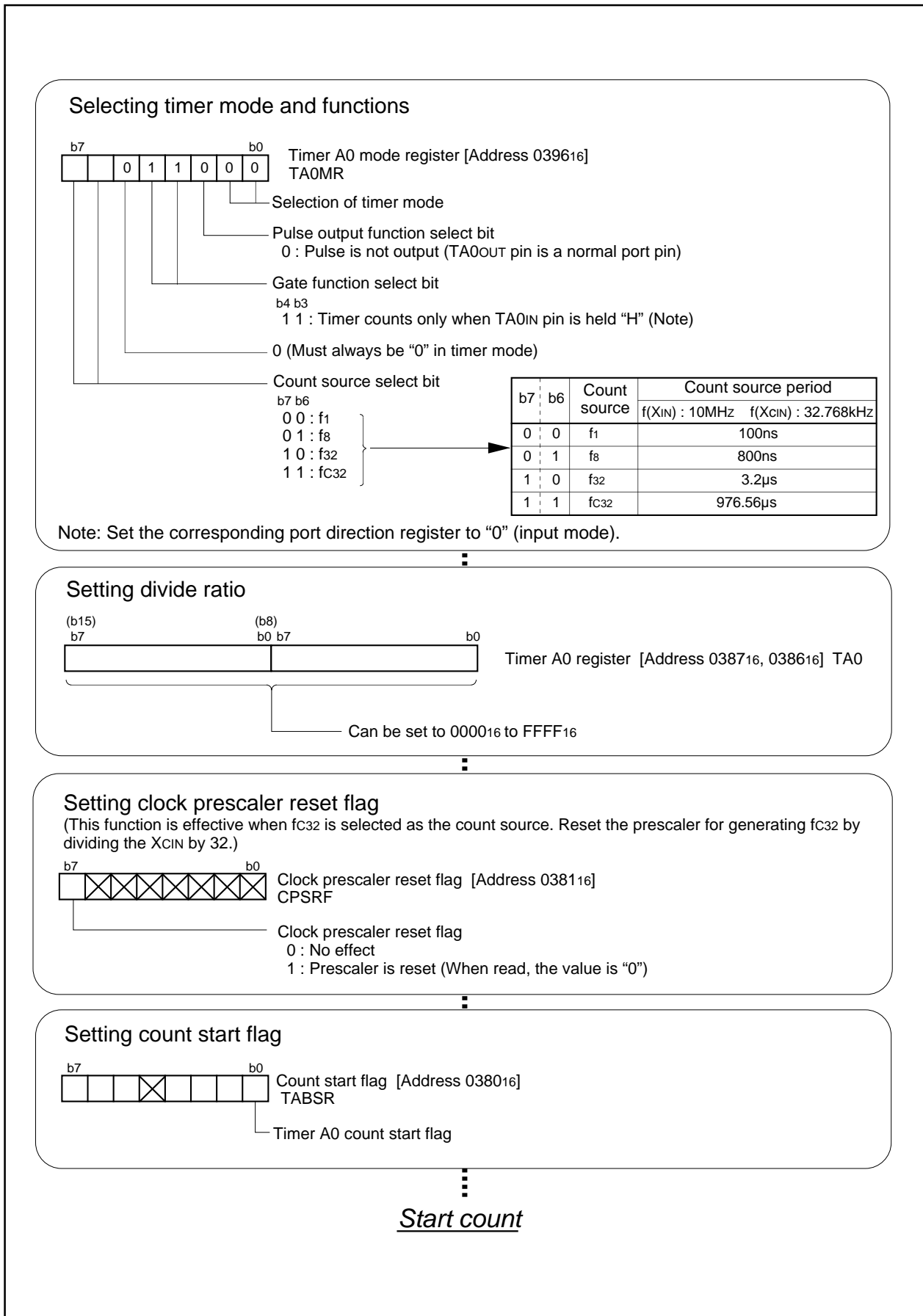


Figure 2.2.9. Set-up procedure of timer mode, gate function selected

2.2.4 Operation of Timer A (timer mode, pulse output function selected)

In timer mode, choose functions from those listed in Table 2.2.3. Operations of the circled items are described below. Figure 2.2.10 shows the operation timing, and Figure 2.2.11 shows the set-up procedure.

Table 2.2.3. Chosed functions

Item	Set-up	
Count source	O	Internal count source($f_1 / f_8 / f_{32} / f_{c32}$)
Pulse output function		No pulses output
	O	Pulses output
Gate function	O	No gate function
		Performs count only for the period in which the TA0IN pin is at "L" level
		Performs count only for the period in which the TA0IN pin is at "H" level

- Operation
- (1) Setting the count start flag to "1" causes the counter to perform a down count on the count source.
 - (2) If an underflow occurs, the content of the reload register is reloaded and the count continues. At this time, the timer A0 interrupt request bit goes to "1". Also, the output polarity of the TA0OUT pin reverses.
 - (3) Setting the count start flag to "0" causes the counter to hold its value and to stop. Also, the TA0OUT pin outputs an "L" level.

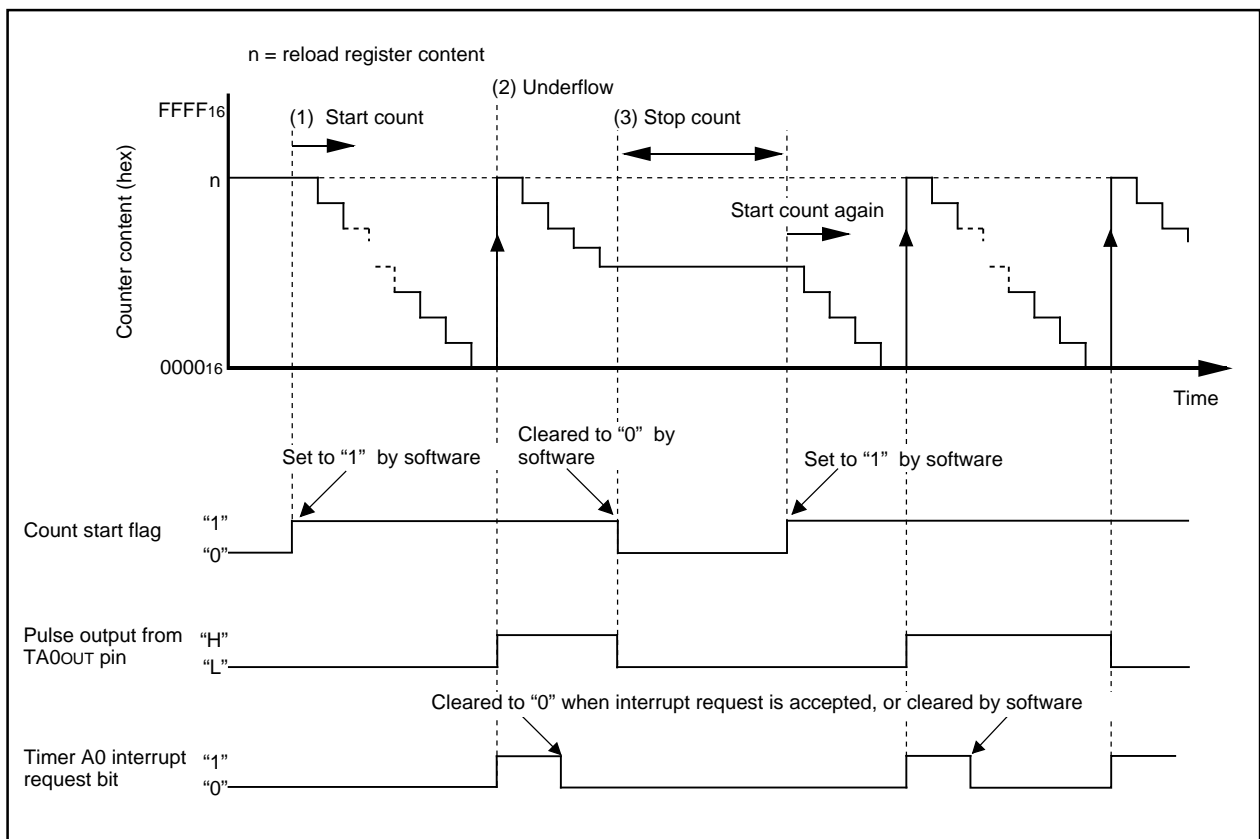


Figure 2.2.10. Operation timing of timer mode, pulse output function selected

Timer A

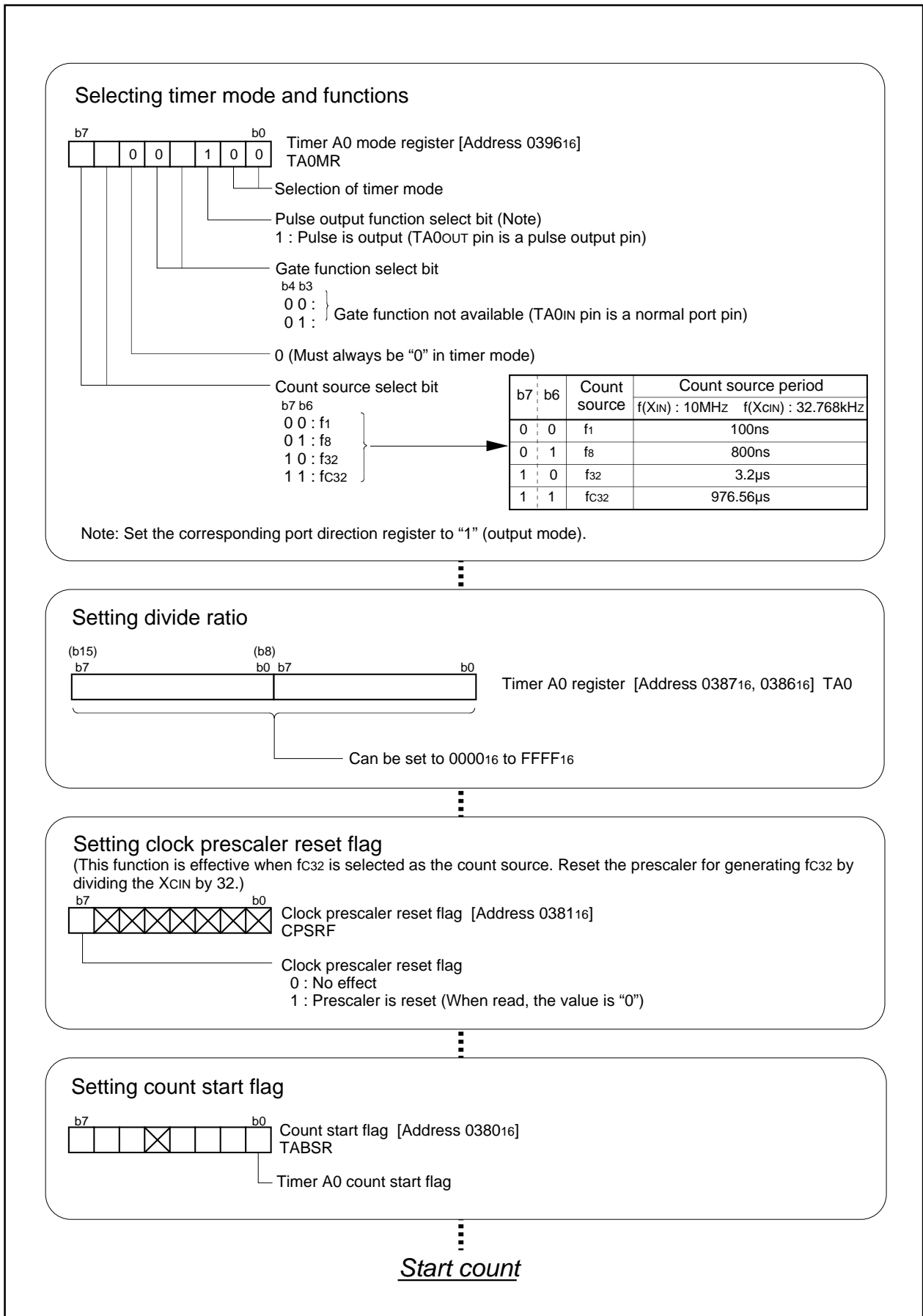


Figure 2.2.11. Set-up procedure of timer mode, pulse output function selected

2.2.5 Operation of Timer A (event counter mode, reload type selected)

In event counter mode, choose functions from those listed in Table 2.2.4. Operations of the circled items are described below. Figure 2.2.12 shows the operation timing, and Figure 2.2.13 shows the set-up procedure.

Table 2.2.4. Chosed functions

Item	Set-up	Item	Set-up
Count source	○ Input signal to TA0IN (counting falling edges)	Pulse output function	○ No pulses output
	Input signal to TA0IN (counting rising edges)		Pulses output
	Timer overflow (TB1/TX0/TX2 overflow)	Count operation type	○ Reload type
			Free-run type
		Factor for switching between up and down	○ Content of up/down flag
			Input signal to TA0out

- Operation
- (1) Setting the count start flag to "1" causes the counter to count the falling edges of the count source.
 - (2) If an underflow occurs, the content of the reload register is reloaded, and the count continues. At this time, the timer A0 interrupt request bit goes to "1".
 - (3) If switching from an up count to a down count or vice versa while a count is in progress, the switch takes effect from the next effective edge of the count source.
 - (4) Setting the count start flag to "0" causes the counter to hold its value and to stop.
 - (5) If an overflow occurs, the content of the reload register is reloaded, and the count continues. At this time, the timer A0 interrupt request bit goes to "1".

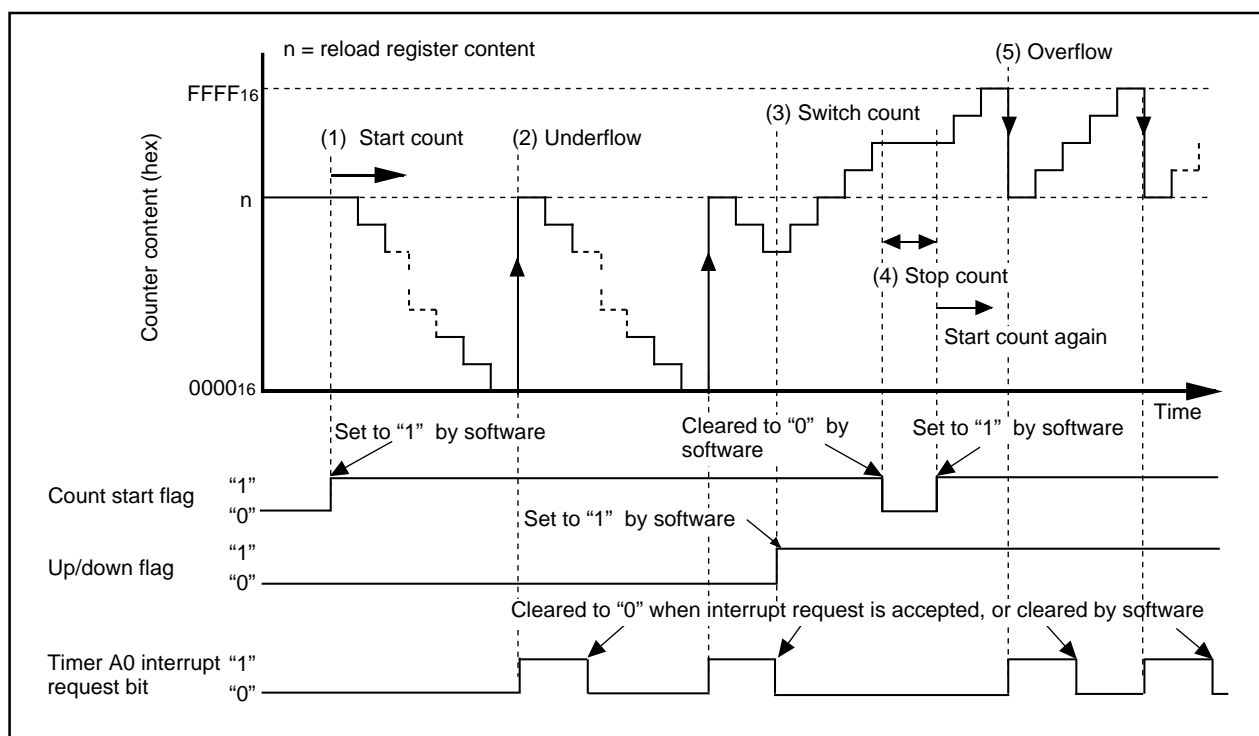


Figure 2.2.12. Operation timing of event counter mode, reload type selected

Timer A

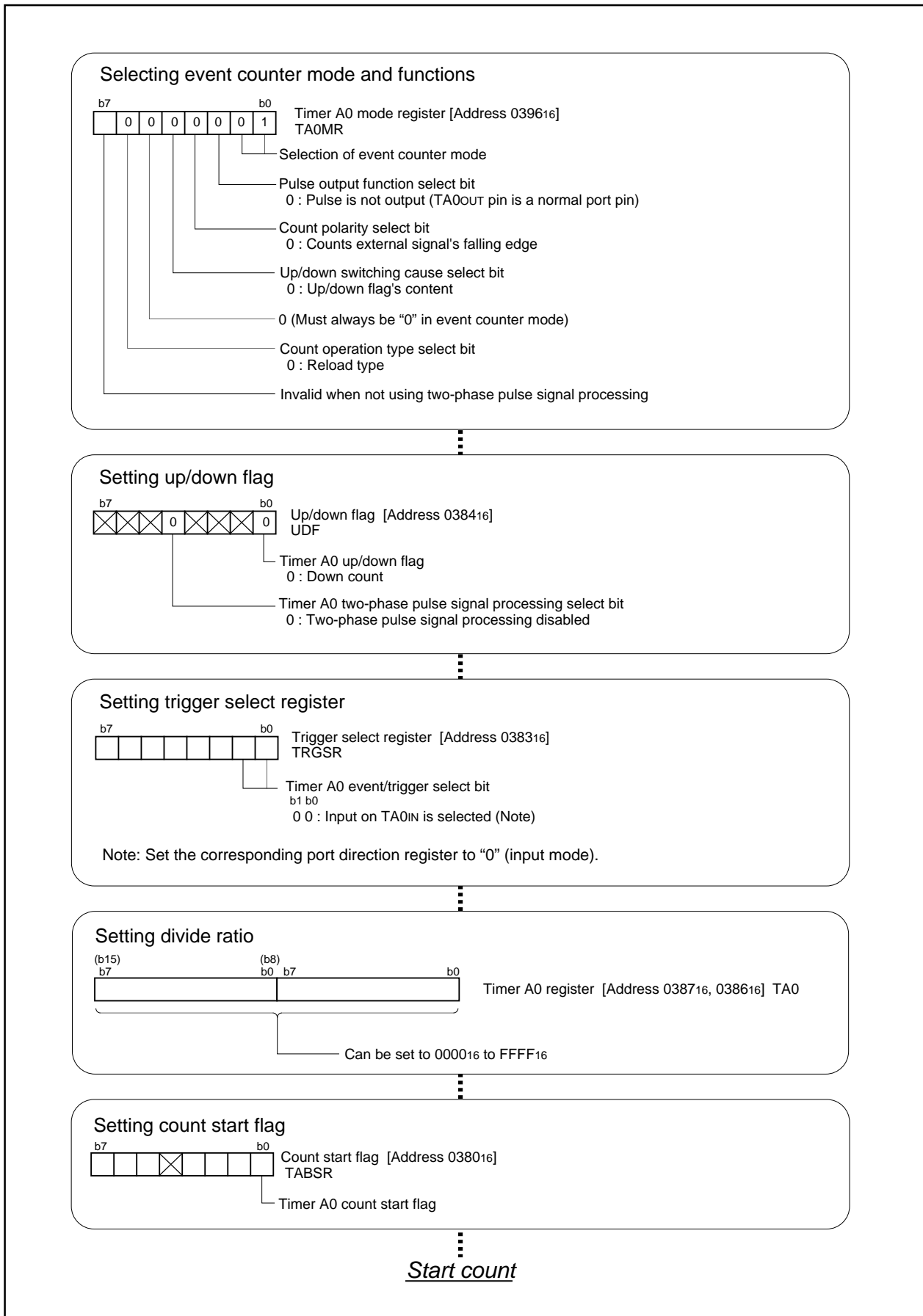


Figure 2.2.13. Set-up procedure of event counter mode, reload type selected

2.2.6 Operation of Timer A (event counter mode, free run type selected)

In event counter mode, choose functions from those listed in Table 2.2.5. Operations of the circled items are described below. Figure 2.2.14 shows the operation timing, and Figure 2.2.15 shows the set-up procedure.

Table 2.2.5. Chosed functions

Item	Set-up	Item	Set-up
Count source	○ Input signal to TA0IN (counting falling edges)	Pulse output function	○ No pulses output
			Pulses output
	Input signal to TA0IN (counting rising edges)	Count operation type	Reload type
		○ Free-run type	
Timer overflow (TB1/TX0/TX2 overflow)		Factor for switching between up and down	○ Content of up/down flag
			Input signal to TA0OUT

- Operation
- (1) Setting the count start flag to "1" causes the counter to count the falling edges of the count source.
 - (2) Even if an underflow occurs, the content of the reload register is not reloaded, but the count continues. At this time, the timer A0 interrupt request bit goes to "1".
 - (3) If switching from an up count to a down count or vice versa while a count is in progress, the switch takes effect from the next effective edge of the count source.
 - (4) Even if an overflow occurs, the content of the reload register is not reloaded, but the count continues. At this time, the timer A0 interrupt request bit goes to "1".

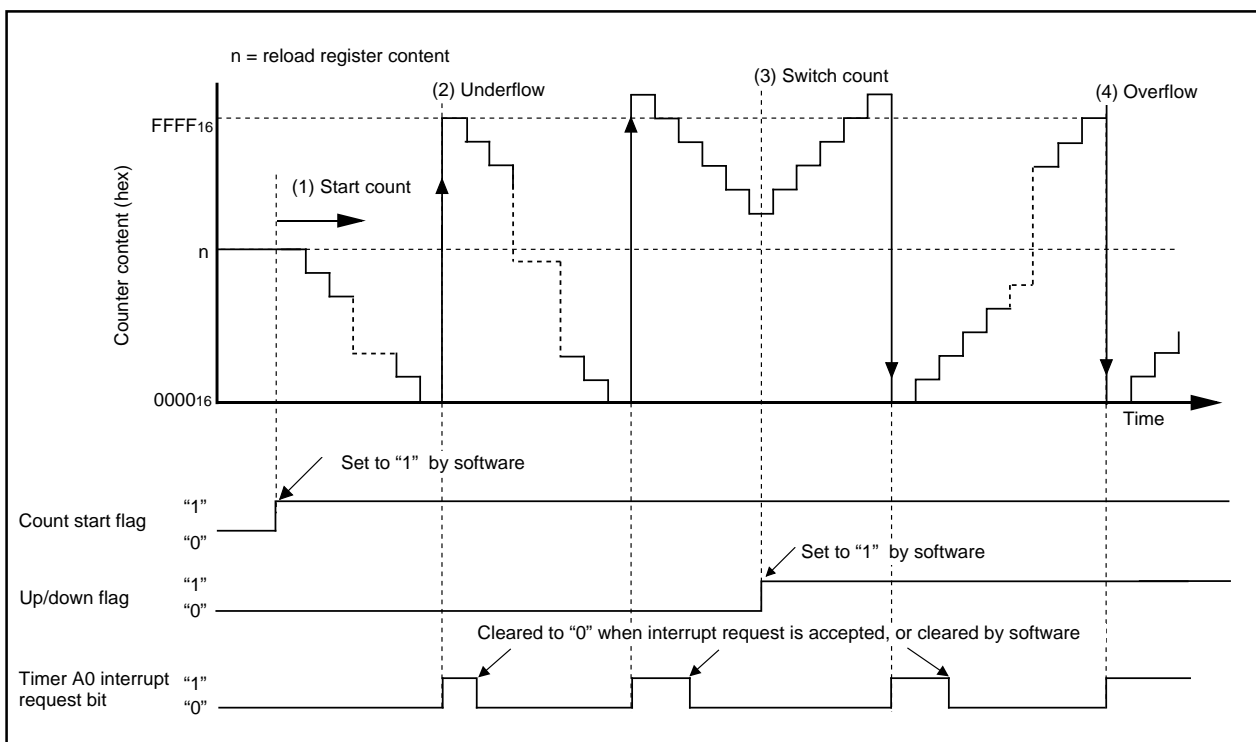


Figure 2.2.14. Operation timing of event counter mode, free run type selected

Timer A

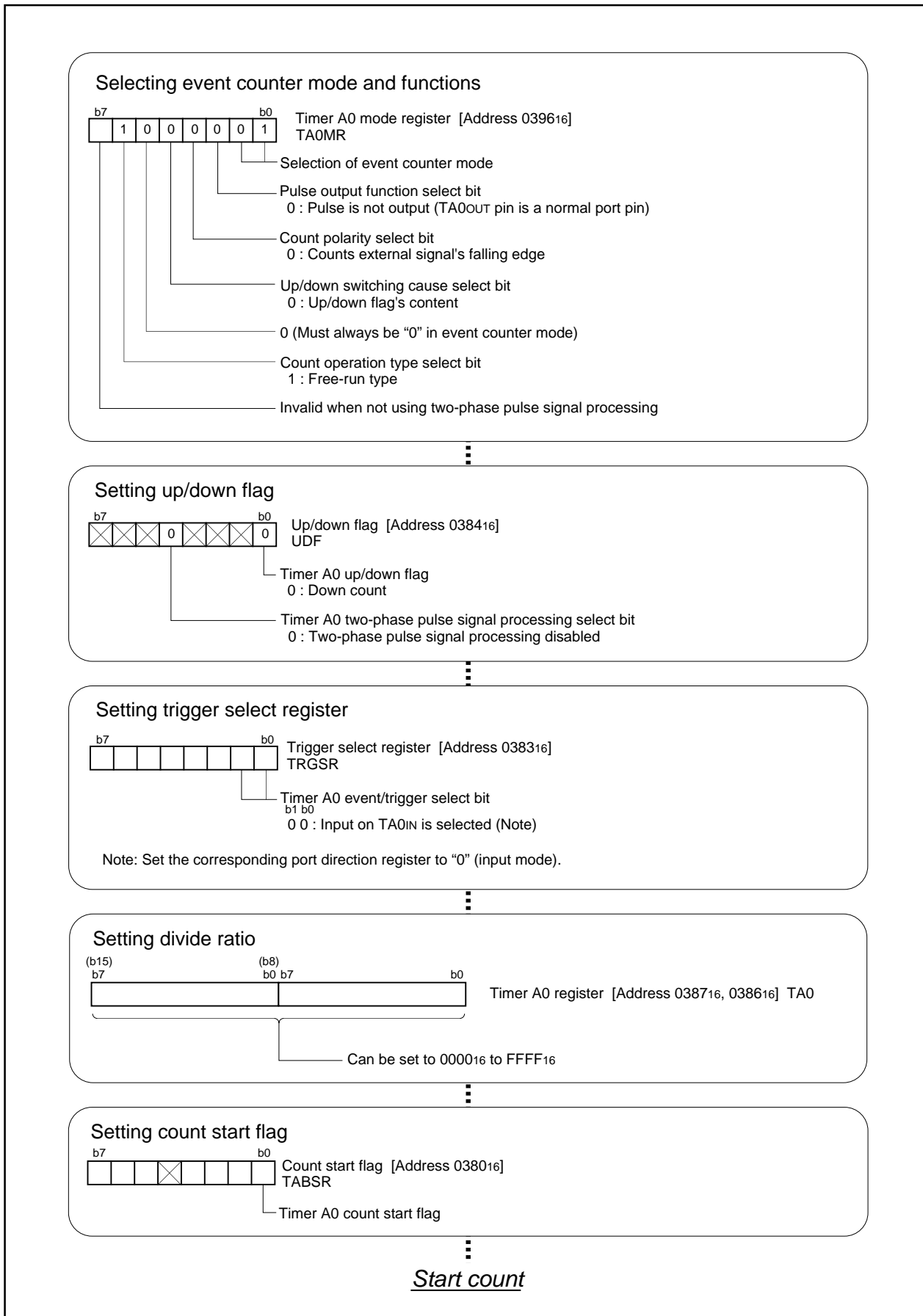


Figure 2.2.15. Set-up procedure of event counter mode, free run type selected

2.2.7 Operation of timer A (2-phase pulse signal process in event counter mode, normal mode selected)

In processing 2-phase pulse signals in event counter mode, choose functions from those listed in Table 2.2.6. Operations of the circled items are described below. Figure 2.2.16 shows the operation timing, and Figure 2.2.17 shows the set-up procedure.

Table 2.2.6. Chosen functions

Item	Set-up
Count operation type	Reload type
	○ Free run type
2-phase pulses process	○ Normal processing
	4-multiplication processing

- Operation
- (1) Setting the count start flag to "1" causes the counter to count effective edges of the count source.
 - (2) Even if an underflow occurs, the content of the reload register is not reloaded, but the count continues. At this time, the timer A0 interrupt request bit goes to "1".
 - (3) Even if an overflow occurs, the content of the reload register is not reloaded, but the count continues. At this time, the timer A0 interrupt request bit goes to "1".

- Note
- The up count or down count conditions are as follows:
 - If a rising edge is present at the TA0IN pin when the input signal level to the TA0OUT pin is "H", an up count is performed.
 - If a falling edge is present at the TA0IN pin when the input signal level to the TA0OUT pin is "H", a down count is performed.

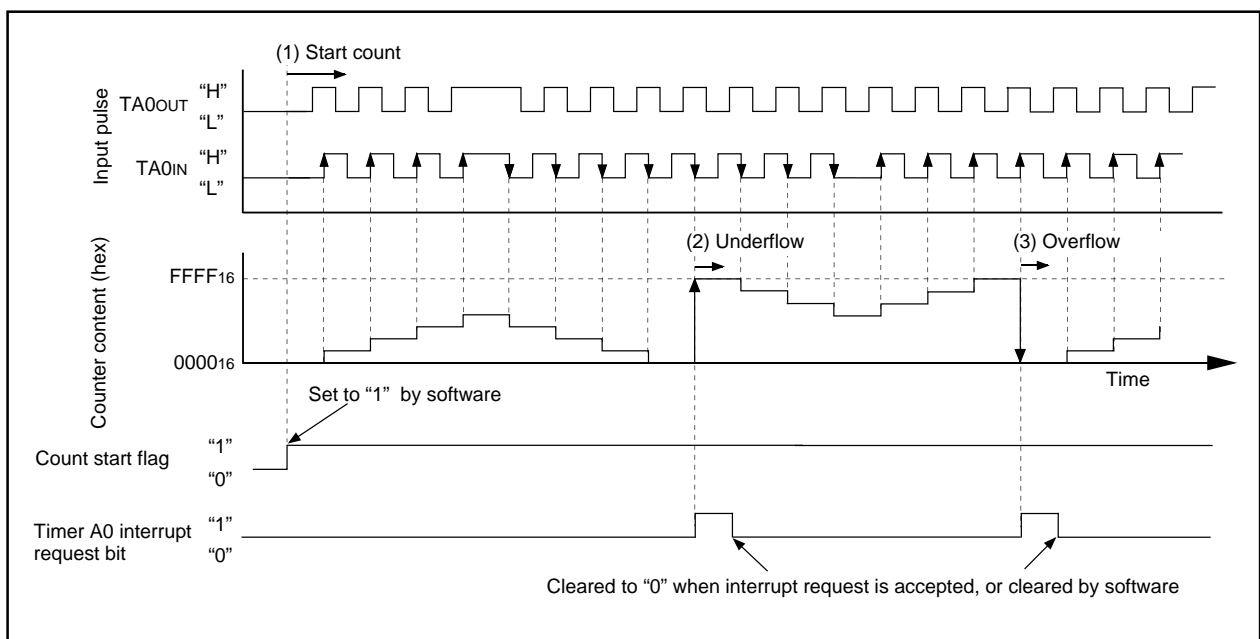


Figure 2.2.16. Operation timing of 2-phase pulse signal process in event counter mode, normal mode selected

Timer A

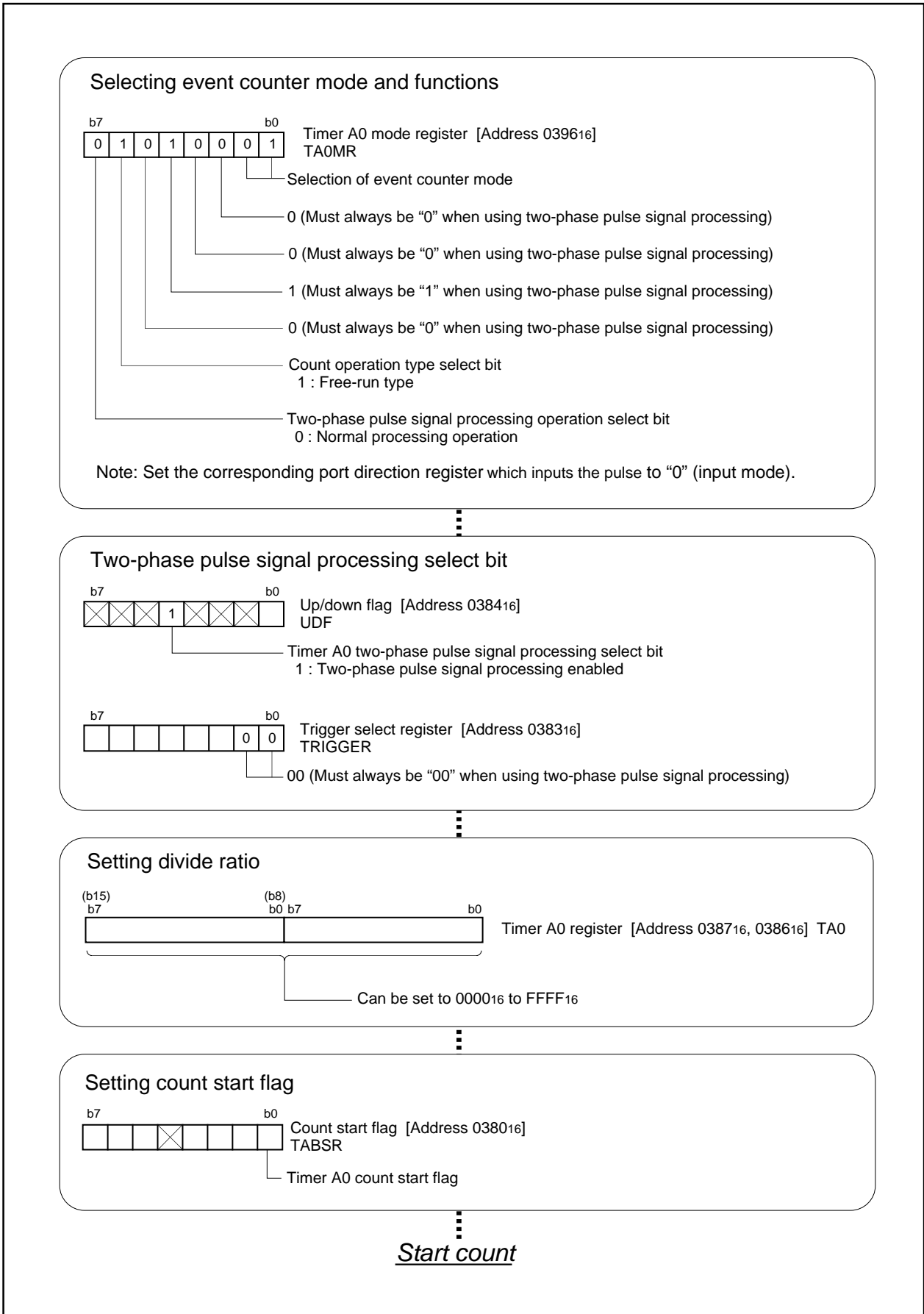


Figure 2.2.17. Set-up procedure of 2-phase pulse signal process in event counter mode, normal mode selected

2.2.8 Operation of timer A (2-phase pulse signal process in event counter mode, multiply-by-4 mode selected)

In processing 2-phase pulse signals in event counter mode, choose functions from those listed in Table 2.2.7. Operations of the circled items are described below. Figure 2.2.18 shows the operation timing, and Figure 2.2.19 shows the set-up procedure.

Table 2.2.7. Chosed functions

Item	Set-up		Item	Set-up	
Count operation type		Reload type	Processing 2 phase pulses		Normal processing
	○	Free run type		○	4-multiplication processing

- Operation
- (1) Setting the count start flag to "1" causes the counter to count effective edges of the count source.
 - (2) Even if an underflow occurs, the content of the reload register is not reloaded, but the count continues. At this time, the timer A0 interrupt request bit goes to "1".
 - (3) Even if an overflow occurs, the content of the reload register is not reloaded, but the count continues. At this time, the timer A0 interrupt request bit goes to "1".

Note • The up count or down count conditions are as follows:

Table 2.2.8. The up count or down count conditions

	Input signal to the TA0OUT pin	Input signal to the TA0IN pin		Input signal to the TA0OUT pin	Input signal to the TA0IN pin
Up count	"H" level	Rising	Down count	"H" level	Falling
	"L" level	Falling		"L" level	Rising
	Rising	"L" level		Rising	"H" level
	Falling	"H" level		Falling	"L" level

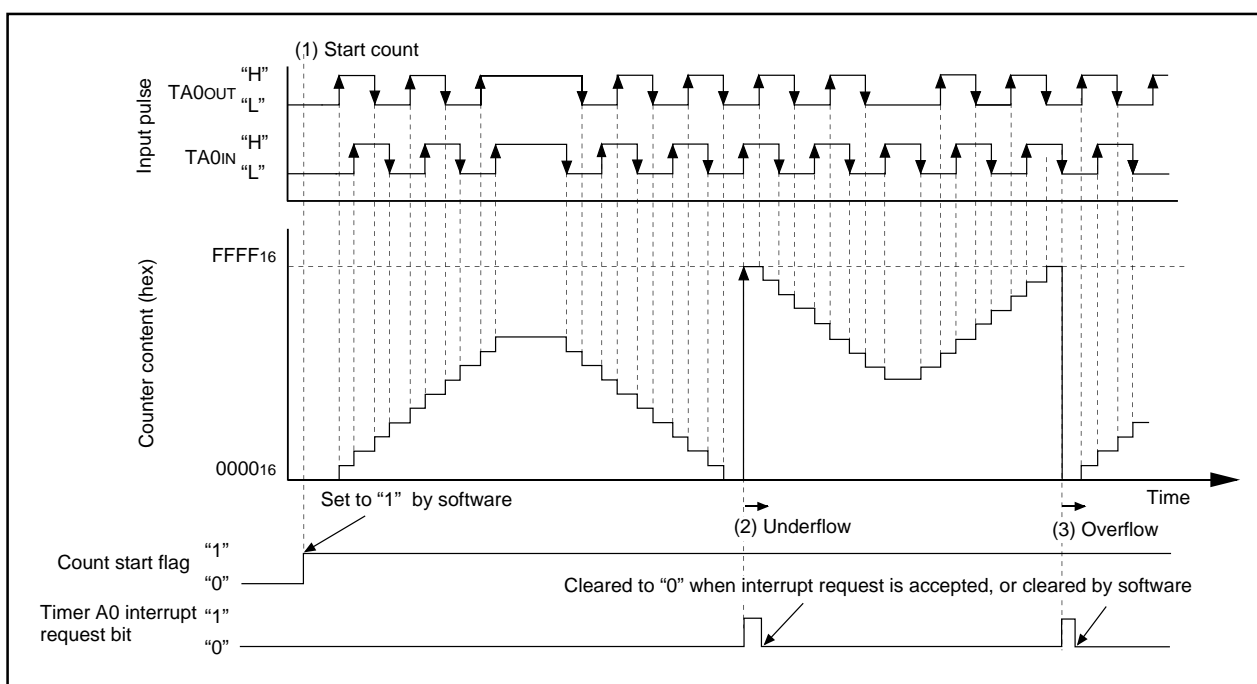
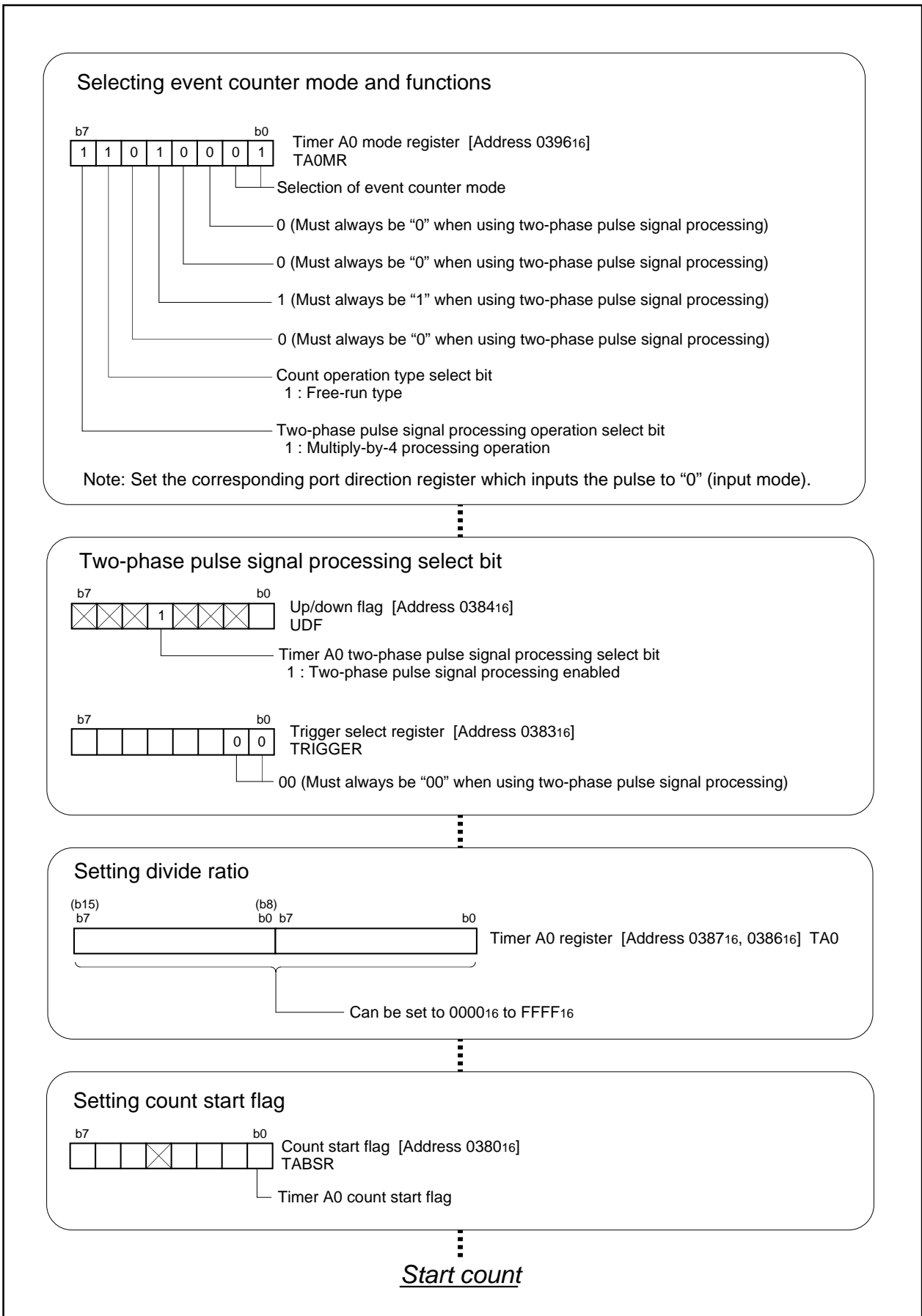


Figure 2.2.18. Operation timing of 2-phase pulse signal process in event counter mode, multiply-by-4 mode selected

Timer A



Timer A

2.2.9 Operation of Timer A (one-shot timer mode)

In one-shot timer mode, choose functions from those listed in Table 2.2.9. Operations of the circled items are described below. Figure 2.2.20 shows the operation timing, and Figure 2.2.21 shows the set-up procedure.

Table 2.2.9. Chosed functions

Item	Set-up	
Count source	○	Internal count source ($f_1 / f_8 / f_{32} / f_{c32}$)
Pulse output function		No pulses output
	○	Pulses output
Count start condition		External trigger input (falling edge of input signal to the TA0IN pin)
		External trigger input (rising edge of input signal to the TA0IN pin)
		Timer overflow (TB1/TX0/TX2 overflow)
	○	Writing "1" to the one-shot start flag

- Operation
- (1) Setting the one-shot start flag to "1" with the count start flag set to "1" causes the counter to perform a down count on the count source. At this time, the TA0OUT pin outputs an "H" level.
 - (2) The instant the value of the counter becomes "0000₁₆", the TA0OUT pin outputs an "L" level, and the counter reloads the content of the reload register and stops counting. At this time, the timer A0 interrupt request bit goes to "1".
 - (3) If a trigger occurs while a count is in progress, the counter reloads the value in the reload register again and continues counting. The reload timing is in step with the next count source input after the trigger.
 - (4) Setting the count start flag to "0" causes the counter to stop and to reload the content of the reload register. Also, the TA0OUT pin outputs an "L" level. At this time, the timer A0 interrupt request bit goes to "1".

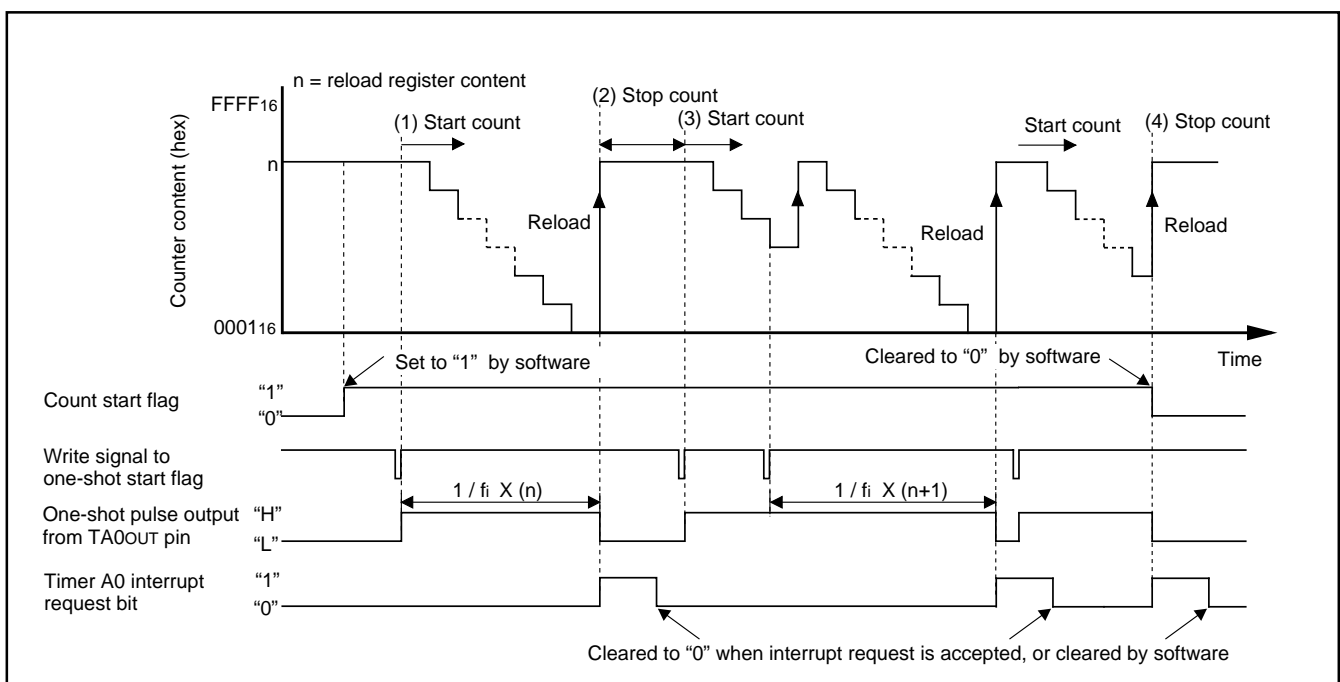
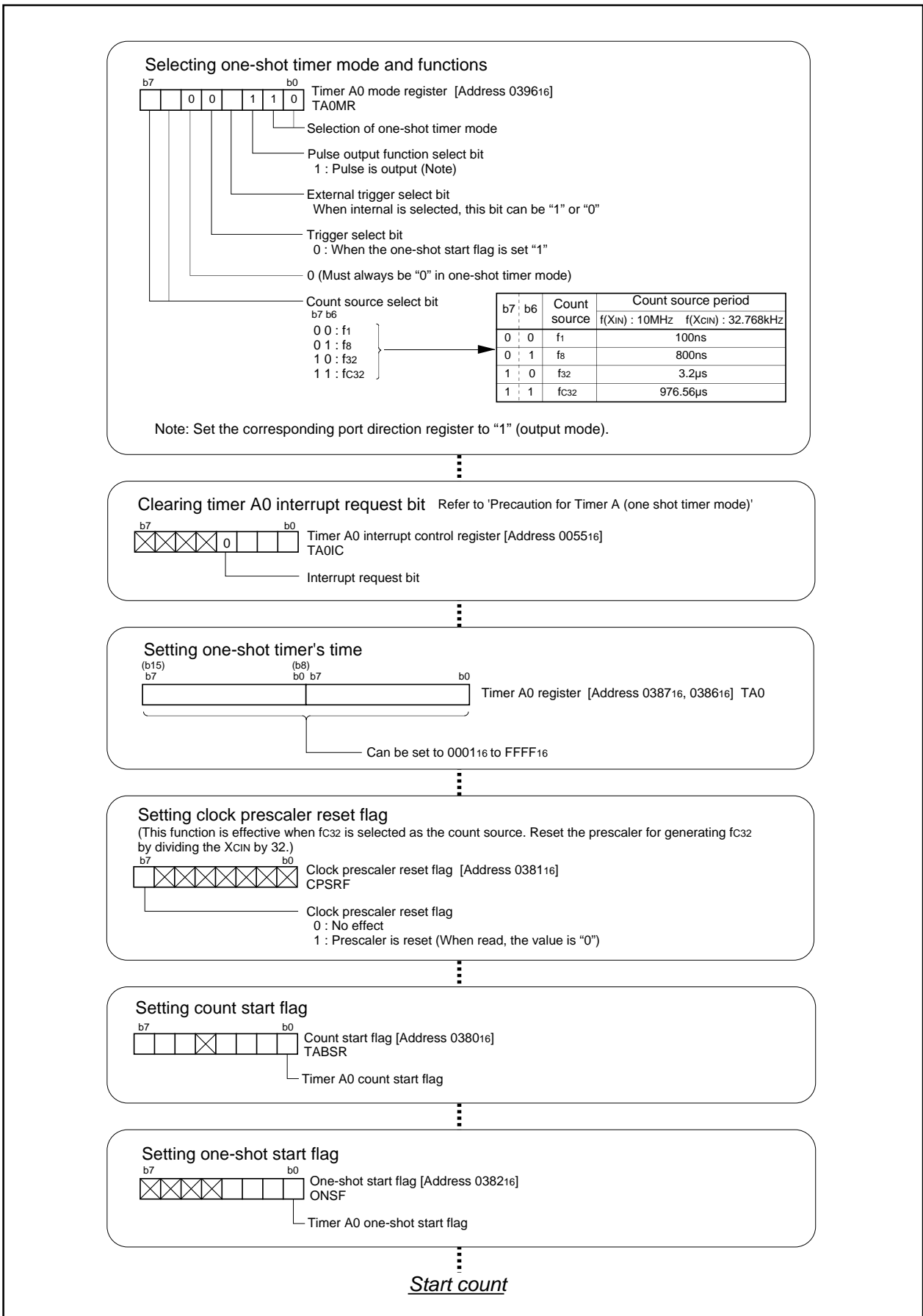


Figure 2.2.20. Operation timing of one-shot mode

Timer A



2.2.10 Operation of Timer A (one-shot timer mode, external trigger selected)

In one-shot timer mode, choose functions from those listed in Table 2.2.10. Operations of the circled items are described below. Figure 2.2.22 shows the operation timing, and Figure 2.2.23 shows the set-up procedure.

Table 2.2.10. Chosed functions

Item	Set-up	
Count source	○	Internal count source ($f_1 / f_8 / f_{32} / f_{c32}$)
Pulse output function		No pulses output
	○	Pulses output
Count start condition		External trigger input (falling edge of input signal to the TA0IN pin)
	○	External trigger input (rising edge of input signal to the TA0IN pin)
		Timer overflow (TB1/TX0/TX2 overflow)
		Writing "1" to the one-shot start flag

- Operation
- (1) If the TA0IN pin input level changes from "L" to "H" with the count start flag set to "1", the counter performs a down count on the count source. At this time, the TA0OUT pin output level goes to "H" level.
 - (2) If the value of the counter becomes "0000₁₆", the TA0OUT pin outputs an "L" level, and the counter reloads the content of the reload register and stops counting. At this time, the timer A0 interrupt request bit goes to "1".
 - (3) If a trigger occurs while a count is in progress, the counter reloads the value of the reload register again and continues counting. The reload timing is in step with the next count source input after the trigger.
 - (4) Setting the count start flag to "0" causes the counter to stop and to reload the content of the reload register. Also, the TA0OUT pin outputs an "L" level. At this time, the timer A0 interrupt request bit goes to "1".

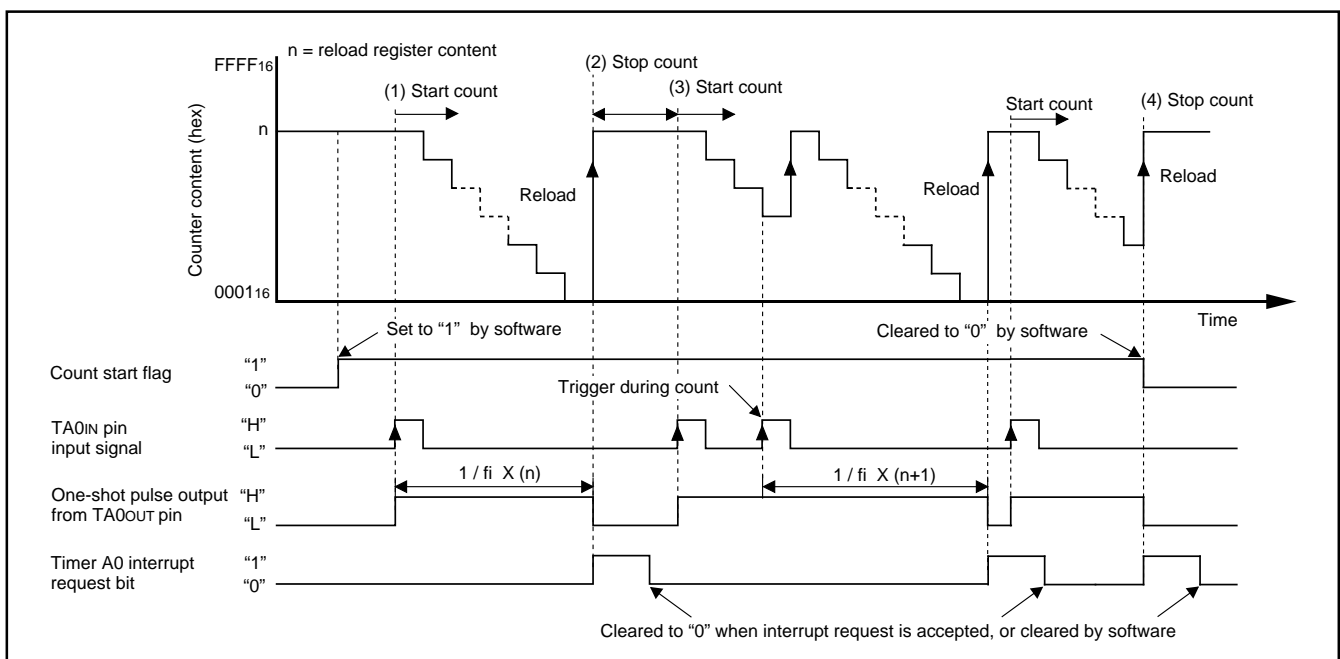


Figure 2.2.22. Operation timing of one-shot mode, external trigger selected

Timer A

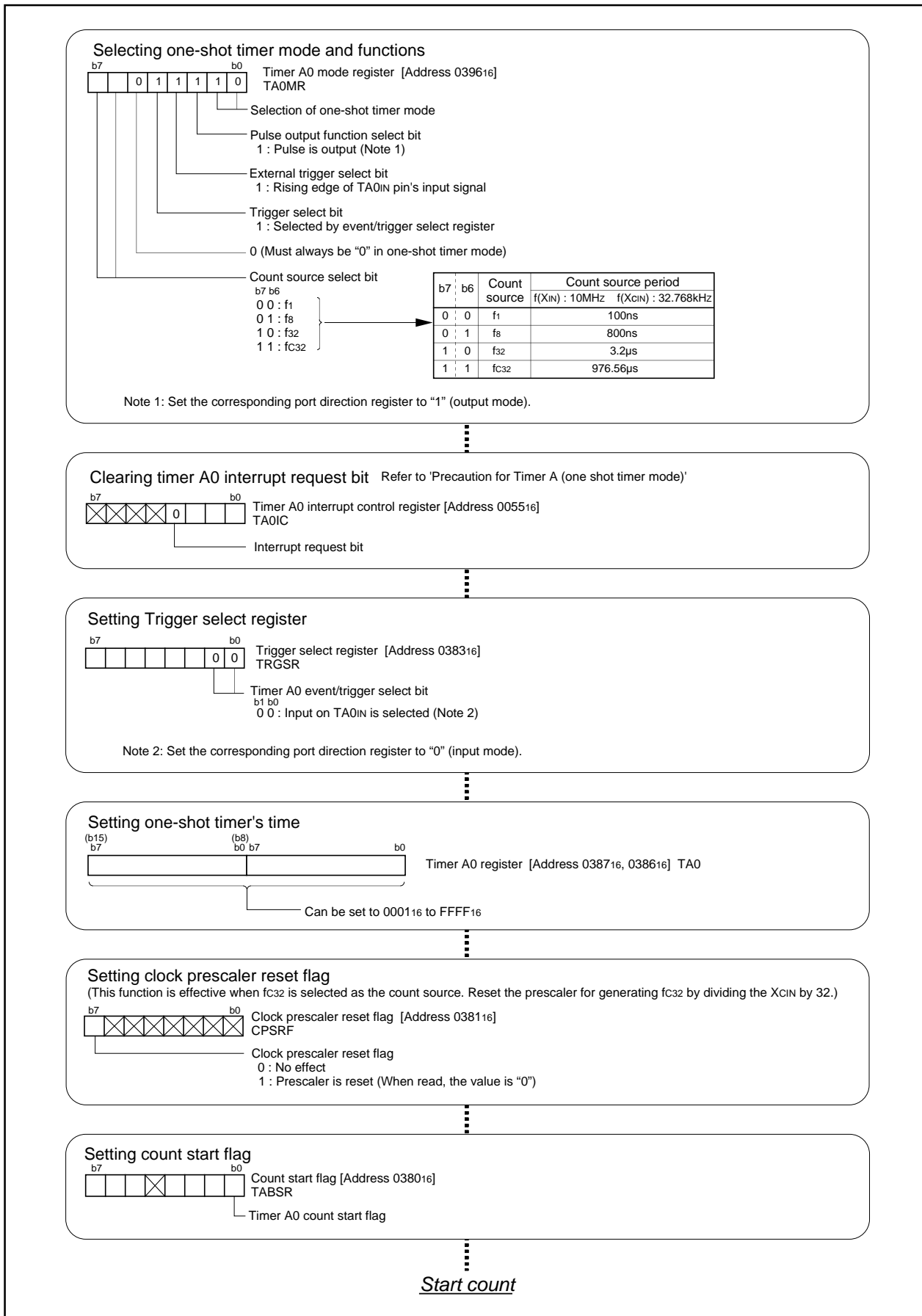


Figure 2.2.23. Set-up procedure of one-shot mode, external trigger selected

2.2.11 Operation of Timer A (pulse width modulation mode, 16-bit PWM mode selected)

In pulse width modulation mode, choose functions from those listed in Table 2.2.11. Operations of the circled items are described below. Figure 2.2.24 shows the operation timing, and Figure 2.2.25 shows the set-up procedure.

Table 2.2.11. Chosed functions

Item	Set-up	
Count source	○	Internal count source ($f_1 / f_8 / f_{32} / f_{c32}$)
PWM mode	○	16-bit PWM
		8-bit PWM
Count start condition		External trigger input (falling edge of input signal to the TA0IN pin)
	○	External trigger input (rising edge of input signal to the TA0IN pin)
		Timer overflow (TB1/TX0/TX2 overflow)

- Operation
- (1) If the TA0IN pin input level changes from "L" to "H" with the count start flag set to "1", the counter performs a down count on the count source. Also, the TA0OUT pin outputs an "H" level.
 - (2) The TA0OUT pin output level changes from "H" to "L" when a set time period elapses. At this time, the timer A0 interrupt request bit goes to "1".
 - (3) The counter reloads the content of the reload register every time PWM pulses are output for one cycle, and continues counting.
 - (4) Setting the count start flag to "0" causes the counter to hold its value and to stop. Also, the TA0OUT outputs an "L" level.

- Note
- PWM pulse cycle is $(2^{16} - 1)/f_i$, whereas H level duration is n/f_i . However, when "0000₁₆" is set for the timer A0 register, the PWM output is "L" level for the entire period, and an interrupt request is generated for every PWM output cycle. Also, when "FFFF₁₆" is set for the timer A0 register, the PWM output is "H" level for the entire period, and an interrupt request is generated for every PWM output cycle.
- (f_i : Count source frequency $f_1, f_8, f_{32}, f_{c32}$ n : Timer value)

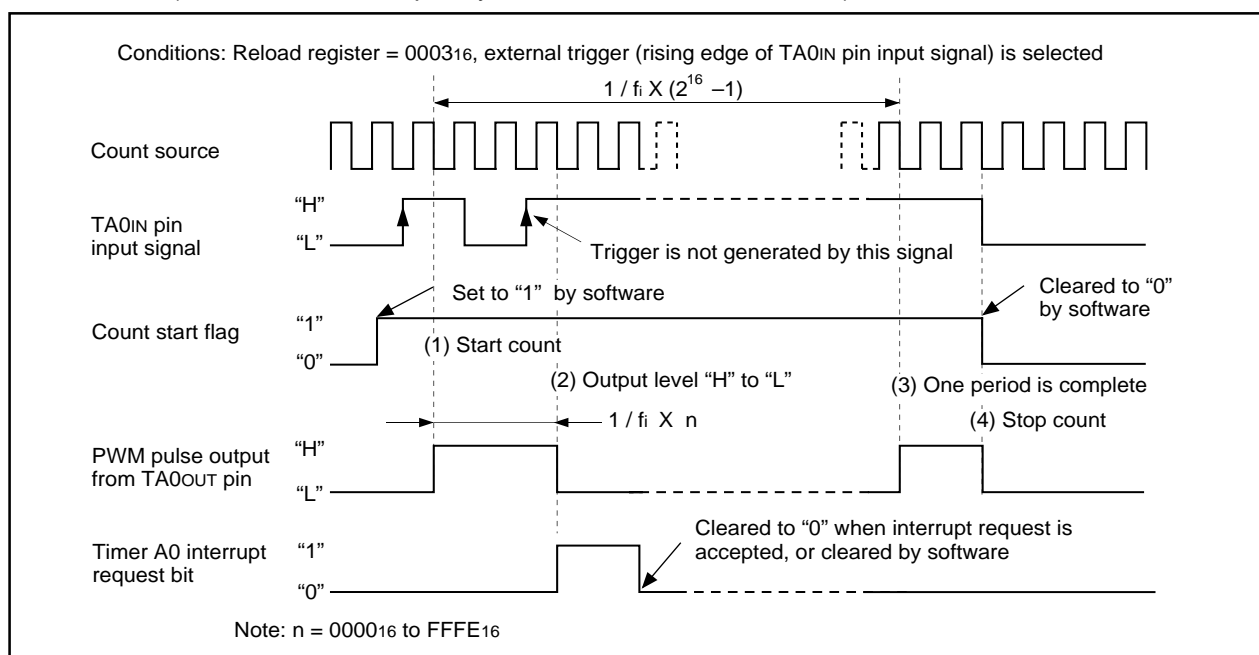


Figure 2.2.24. Operation timing of pulse width modulation mode, 16-bit PWM mode selected

Timer A

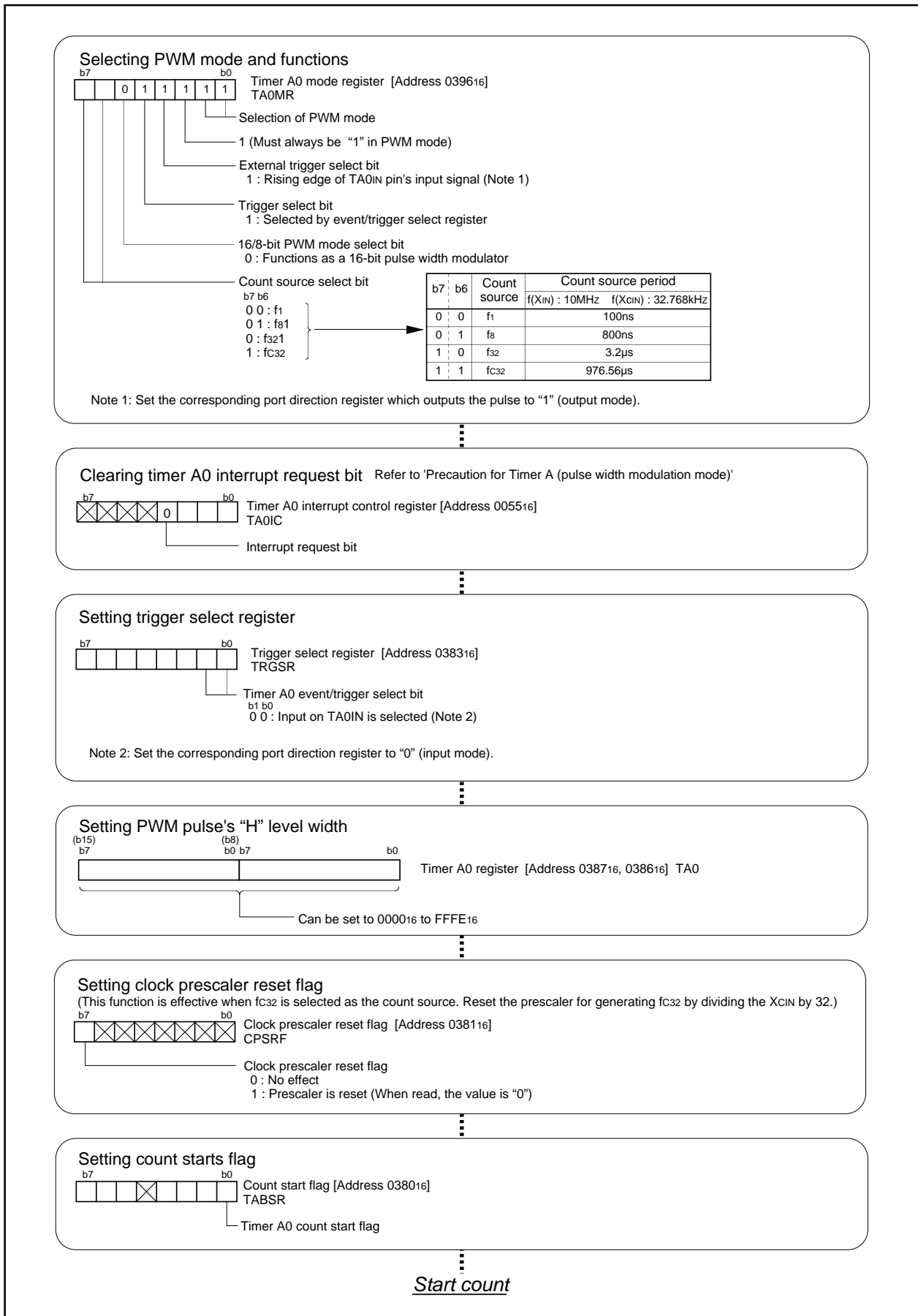


Figure 2.2.25. Set-up procedure of pulse width modulation mode, 16-bit PWM mode selected

2.2.12 Operation of Timer A (pulse width modulation mode, 8-bit PWM mode selected)

In pulse width modulation mode, choose functions from those listed in Table 2.2.12. Operations of the circled items are described below. Figure 2.2.26 shows the operation timing, and Figure 2.2.27 shows the set-up procedure.

Table 2.2.12. Chosed functions

Item	Set-up	
Count source	○	Internal count source ($f_1 / f_8 / f_{32} / f_{c32}$)
PWM mode		16-bit PWM
	○	8-bit PWM
Count start condition	○	External trigger input (falling edge of input signal to the TA0IN pin)
		External trigger input (rising edge of input signal to the TA0IN pin)
		Timer overflow (TB1/TX0/TX2 overflow)

- Operation
- (1) If the TA0IN pin input level changes from "H" to "L" with the count start flag set to "1", the counter performs a down count on the count source. Also, the TA0OUT pin outputs an "H" level.
 - (2) The TA0OUT pin output level changes from "H" to "L" when a set time period elapses. At this time, the timer A0 interrupt request bit goes to "1".
 - (3) The counter reloads the content of the reload register every time PWM pulses are output for one cycle, and continues counting.
 - (4) Setting the count start flag to "0" causes the counter to hold its value and to stop. Also, the TA0OUT pin outputs an "L" level.

- Note
- PWM pulse cycle is $(m + 1) \times (2^8 - 1) / f_i$, whereas "H" level duration is $n \times (m + 1) / f_i$. However, when "0016" is set for the significant 8 bits of the timer A0 register, the PWM output is "L" level for the entire period, and an interrupt request is generated for every PWM output cycle. Also, when "FF16" is set for the significant 8 bits of the timer A0 register, the PWM output is "H" level for the entire period, and an interrupt request is generated for every PWM output cycle. (f_i : Count source frequency $f_1, f_8, f_{32}, f_{c32}$ n : Timer value)

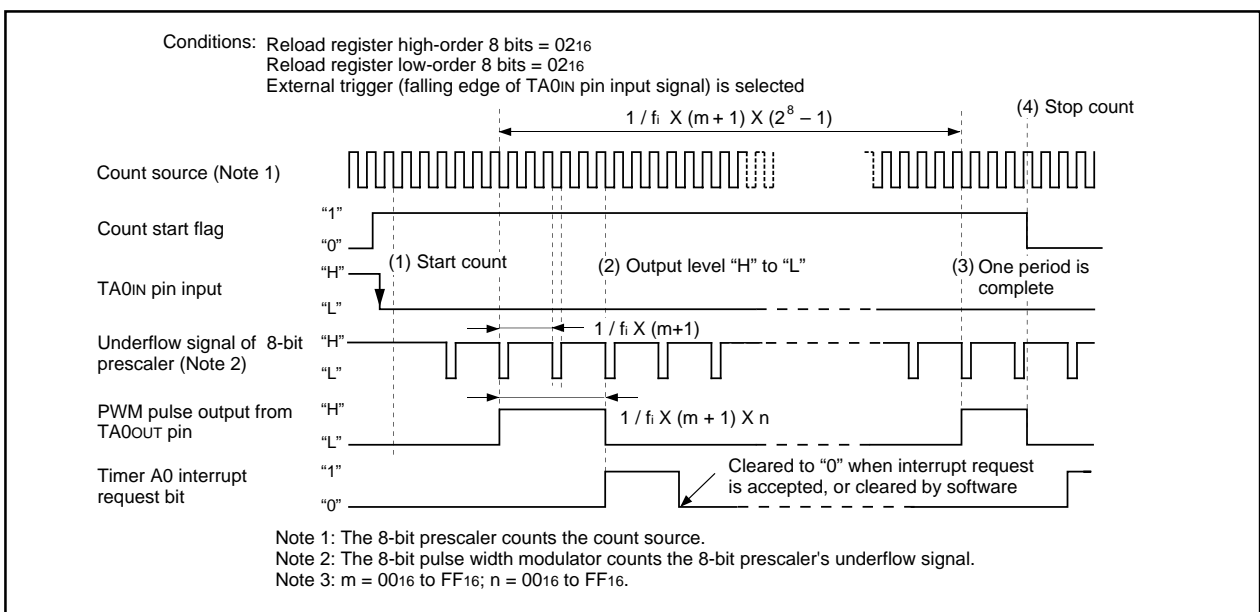
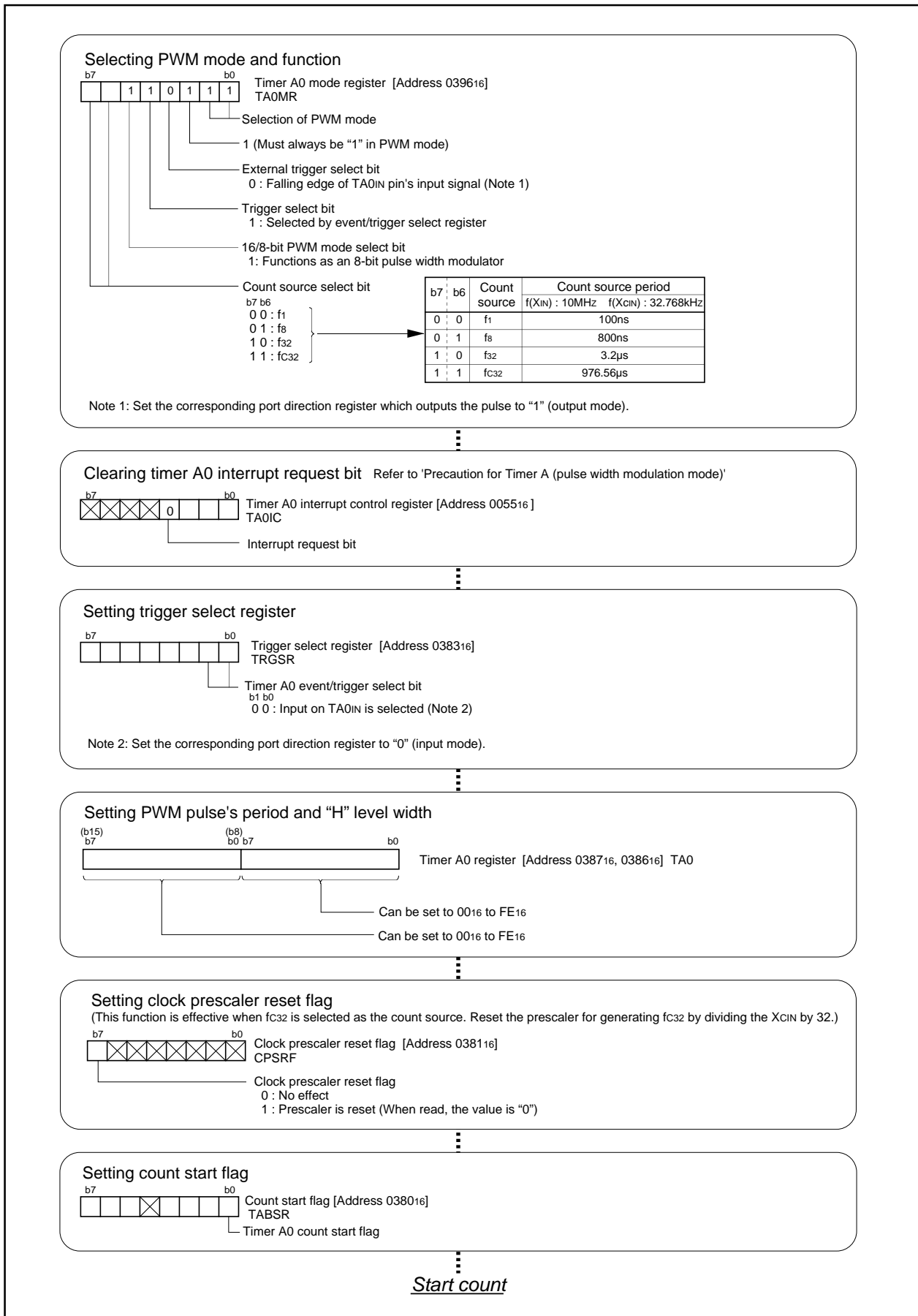


Figure 2.2.26. Operation timing of pulse width modulation mode, with 8-bit PWM mode selected

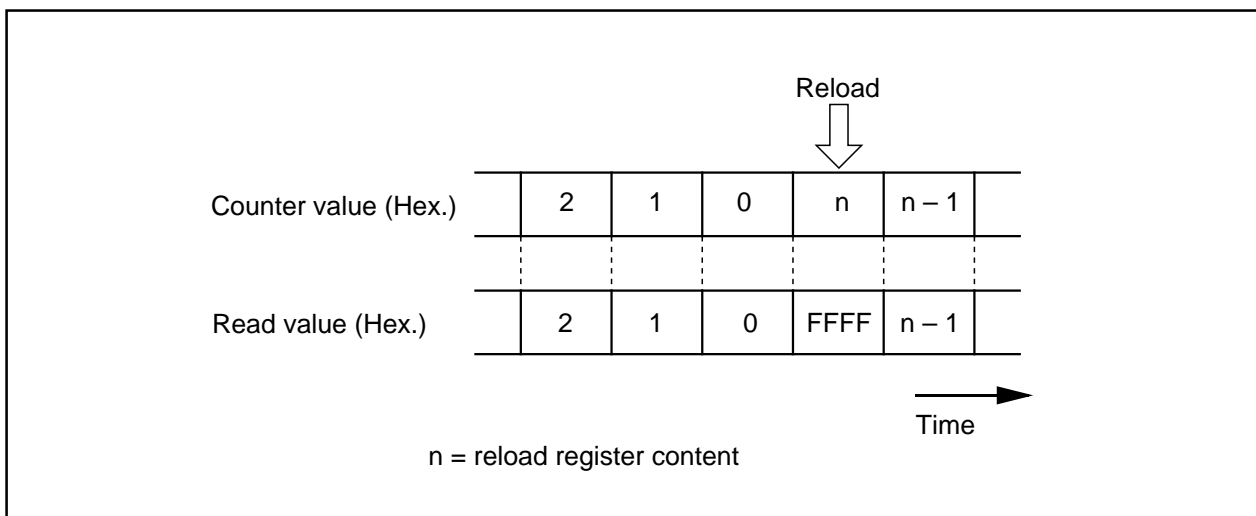
Timer A



Timer A

2.2.13 Precautions for Timer A (timer mode)

- (1) To clear reset, the count start flag is set to "0". Set a value in the timer A0 register, then set the flag to "1".
- (2) Reading the timer A0 register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the timer A0 register with the reload timing shown in Figure 2.2.28 gets "FFFF16". Reading the timer A0 register after setting a value in the timer A0 register with a count halted but before the counter starts counting gets a proper value.

**Figure 2.2.28. Reading timer A0 register**

Timer A

2.2.14 Precautions for Timer A (event counter mode)

- (1) To clear reset, the count start flag is set to "0". Set a value in the timer A0 register, then set the flag to "1".
- (2) Reading the timer A0 register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the timer A0 register with the reload timing shown in Figure 2.2.29 gets "FFFF₁₆" by underflow or "0000₁₆" by overflow. Reading the timer A0 register after setting a value in the timer A0 register with a count halted but before the counter starts counting gets a proper value.
- (3) Please note the standards for the differences between the 2 pulses used in the 2-phase pulse signals input signals to the TA0IN pin and TA0OUT pin as shown in Figure 2.2.30.
- (4) When free run type is selected, if count is stopped, set a value in the timer A0 register again.

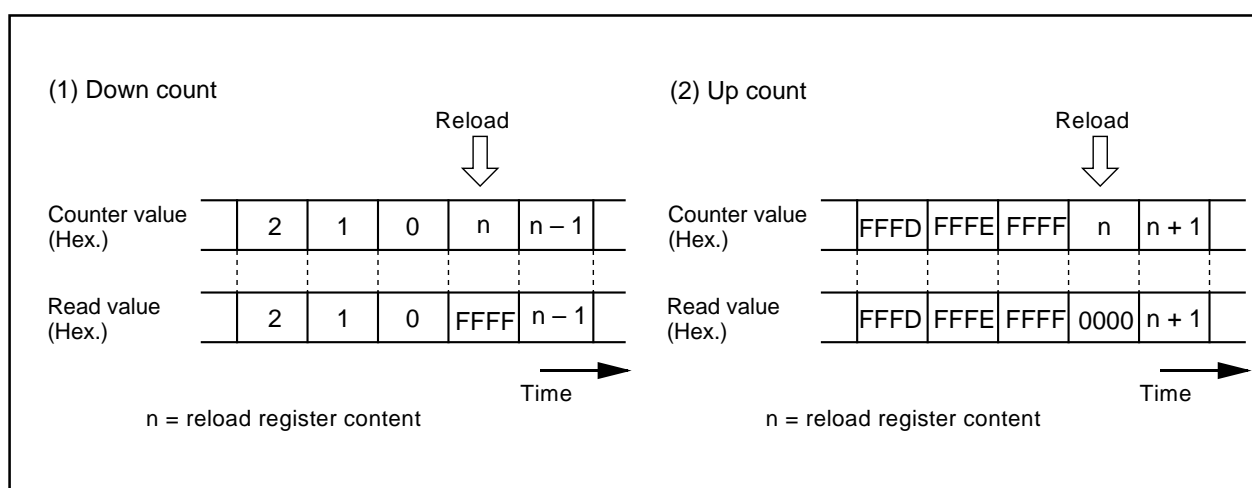


Figure 2.2.29. Reading timer A0 register

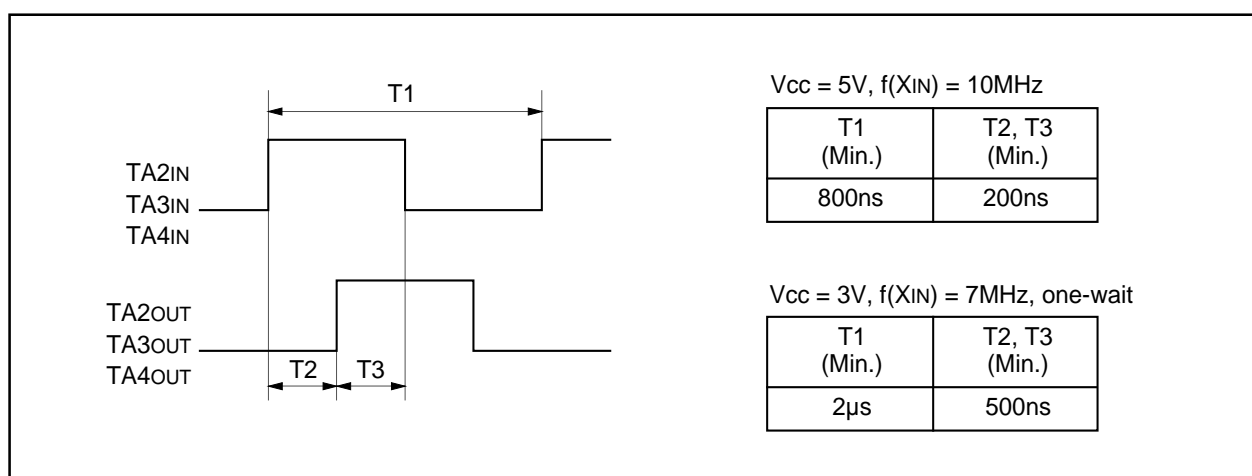


Figure 2.2.30. Standard of 2-phase pulses

2.2.15 Precautions for Timer A (one-shot timer mode)

- (1) To clear reset, the count start flag is set to "0". Set a value in the timer A0 register, then set the flag to "1".
- (2) Setting the count start flag to "0" while a count is in progress causes as follows:
 - The counter stops counting and a content of reload register is reloaded.
 - The TA0OUT pin outputs "L" level.
 - The interrupt request generated and the timer A0 interrupt request bit goes to "1".
- (3) The output from the one-shot timer synchronizes with the count source generated internally. Therefore, when an external trigger has been selected, a delay of one cycle of count source as a maximum occurs between the trigger input to the TA0IN pin and the one-shot timer output.
- (4) The timer A0 interrupt request bit goes to "1" if the timer's operation mode is set using any of the following procedures:
 - Selecting one-shot timer mode after reset.
 - Changing operation mode from timer mode to one-shot timer mode.
 - Changing operation mode from event counter mode to one-shot timer mode.
 Therefore, to use timer A0 interrupt (interrupt request bit), set timer A0 interrupt request bit to "0" after the above listed changes have been made.
- (5) If a trigger occurs while a count is in progress, after the counter performs one down count following the reoccurrence of a trigger, the reload register contents are reloaded, and the count continues. To generate a trigger while a count is in progress, generate the second trigger after an elapse longer than one cycle of the timer's count source after the previous trigger occurred.

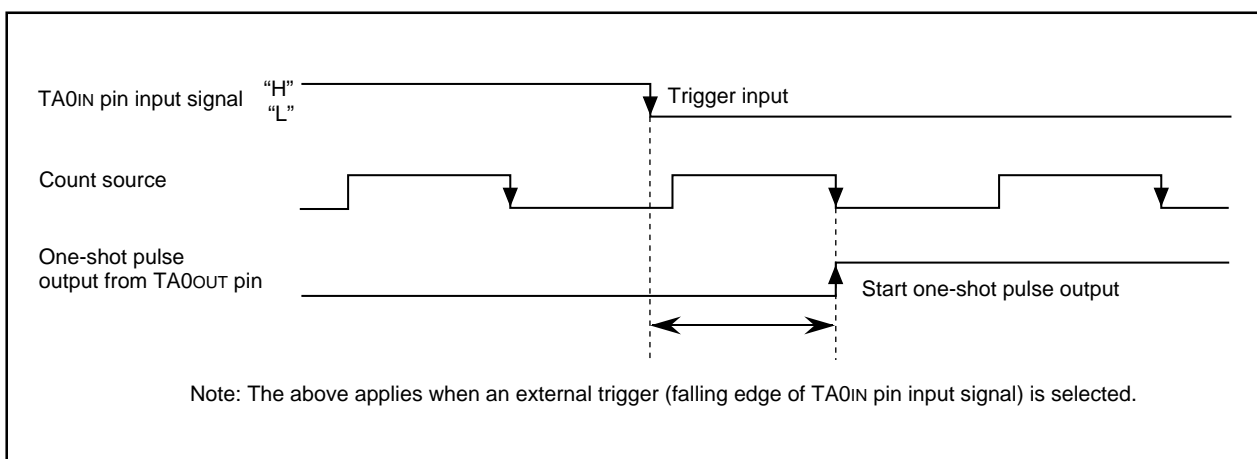
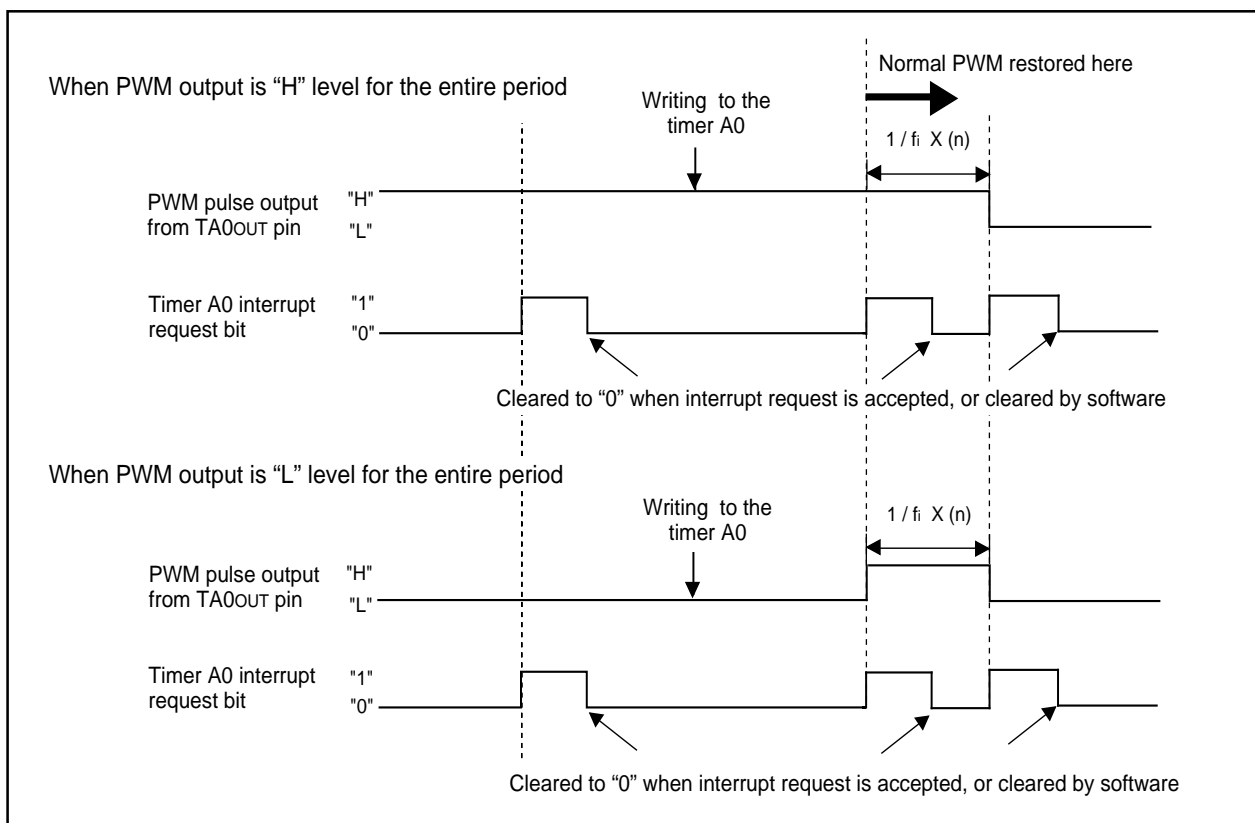


Figure 2.2.31. One-shot timer delay

Timer A

2.2.16 Precautions for Timer A (pulse width modulation mode)

- (1) To clear reset, the count start flag is set to "0". Set a value in the timer A0 register, then set the flag to "1".
- (2) The timer A0 interrupt request bit becomes "1" if setting operation mode of the timer in compliance with any of the following procedures:
 - Selecting PWM mode after reset.
 - Changing operation mode from timer mode to PWM mode.
 - Changing operation mode from event counter mode to PWM mode.Therefore, to use timer A0 interrupt (interrupt request bit), set timer A0 interrupt request bit to "0" after the above listed changes have been made.
- (3) Setting the count start flag to "0" while PWM pulses are being output causes the counter to stop counting. If the TA0OUT pin is outputting an "H" level in this instance, the output level goes to "L", and the timer A0 interrupt request bit goes to "1". If the TA0OUT pin is outputting an "L" level in this instance, the level does not change, and the timer A0 interrupt request bit does not become "1".
- (4) Normal PWM output is restored according to the interrupt request generate timing, both in the case of 16-bit PWM and 8-bit PWM, when PWM output is either "H" or "L" level for the entire period. This holds only when a value other than "0000₁₆" or "FFFF₁₆" is set during 16-bit PWM, or a value other than "00₁₆" or "FF₁₆" is set during 8-bit PWM.

**Figure 2.2.32. Operation timing of PWM output mode**

2.3 Timer B

2.3.1 Overview

The following is an overview for timer B, a 16-bit timer.

(1) Mode

Timer B operates in one of three modes:

(a) Timer mode

The internal count source is counted.

- Operation in timer mode P210

(b) Event counter mode

The number of pulses coming from outside and the number of the timer overflows are counted.

- Operation in event counter mode P212

(c) Pulse period measurement/pulse width measurement mode

External pulse period or external pulse widths are measured. If pulse period measurement mode is selected, the periods of input pulses are continuously measured. If pulse width measurement mode is selected, widths of "H" level pulses and those of "L" level pulses are continuously measured.

- Operation in pulse period measurement mode P214
- Operation in pulse width measurement mode P216

(2) Count source

An internal count source can be selected from f₁, f₈, f₃₂, and fc₃₂. f₁, f₈, and f₃₂ are clocks obtained by dividing the CPU main clock by 1, 8, and 32 respectively. fc₃₂ is the clock obtained by dividing the CPU secondary clock by 32.

(3) Frequency division ratio

The frequency division ratio equals [the value set in the timer register + 1]. The counter underflows when a count source equal to a frequency division ratio is input, and an interrupt request occurs.

(4) Reading the timer

In timer mode or event counter mode, the count value at the time of reading the timer register will be read. Read the register in 16-bit increments. In both the pulse period measurement mode and pulse width measurement mode, an indeterminate value is read until the second effective edge is input after a count is started, otherwise, the measurement results are read.

(5) Writing to the timer

When writing to the timer register while a count is in progress, the value is written only to the reload register. When writing to the timer register while a count has stopped, the value is written both to the reload register and the count. Write the value in 16-bit increments. The timer register cannot be written to in either the pulse period measurement mode or the pulse width measurement mode.

Timer B

(6) Input to the timer and the direction register

To input an external signal to the timer, set the direction register of the relevant port to input.

(7) Pins related to timer B

(a) TB0IN, TB1IN Input pins to timer B.

(8) Registers related to timer B

Figure 2.3.1 shows the memory map of timer B-related registers. Figures 2.3.2 and 2.3.3 show timer B-related registers.

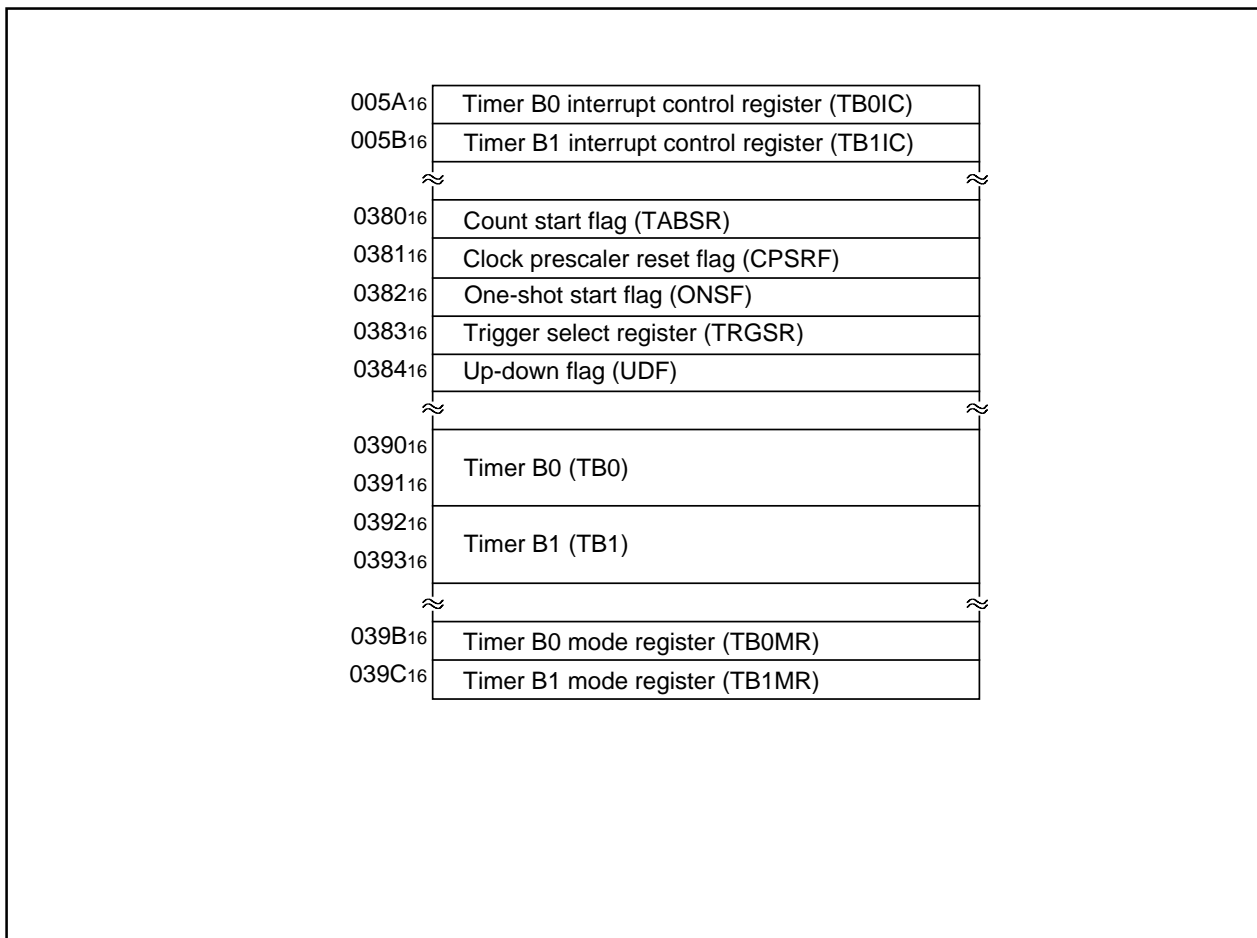


Figure 2.3.1. Memory map of timer B-related registers

Timer B

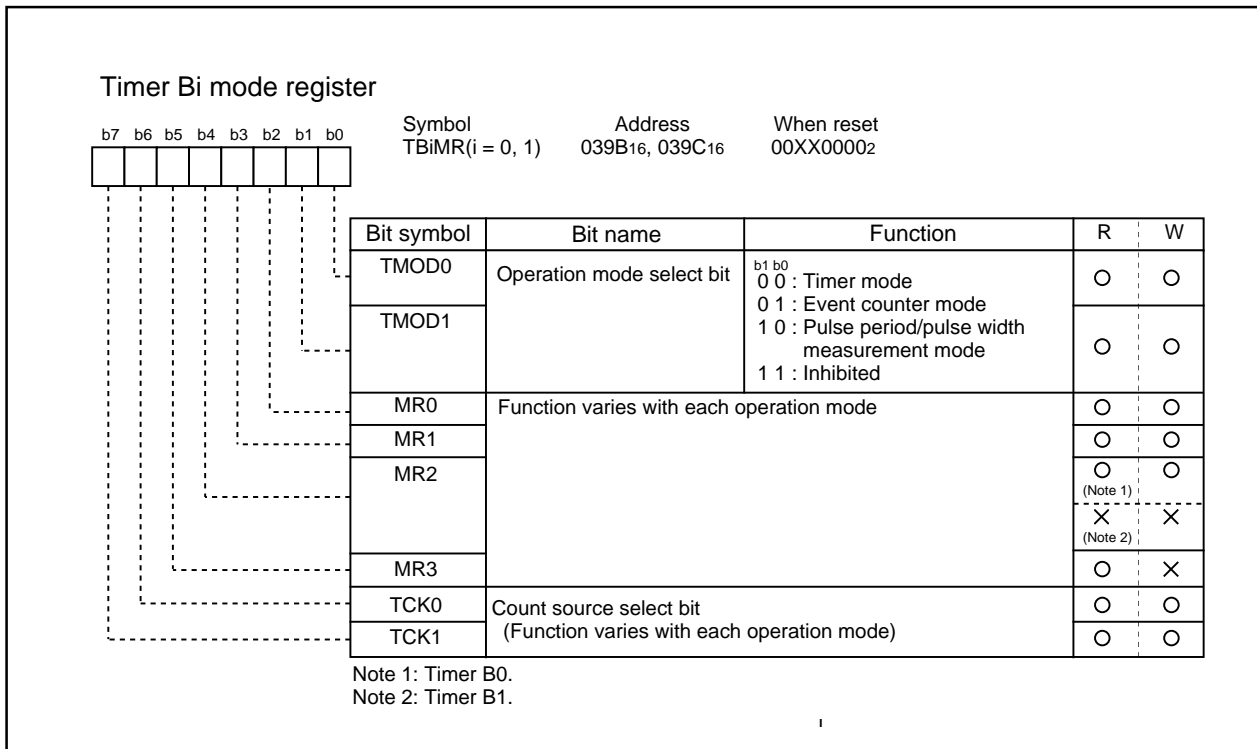
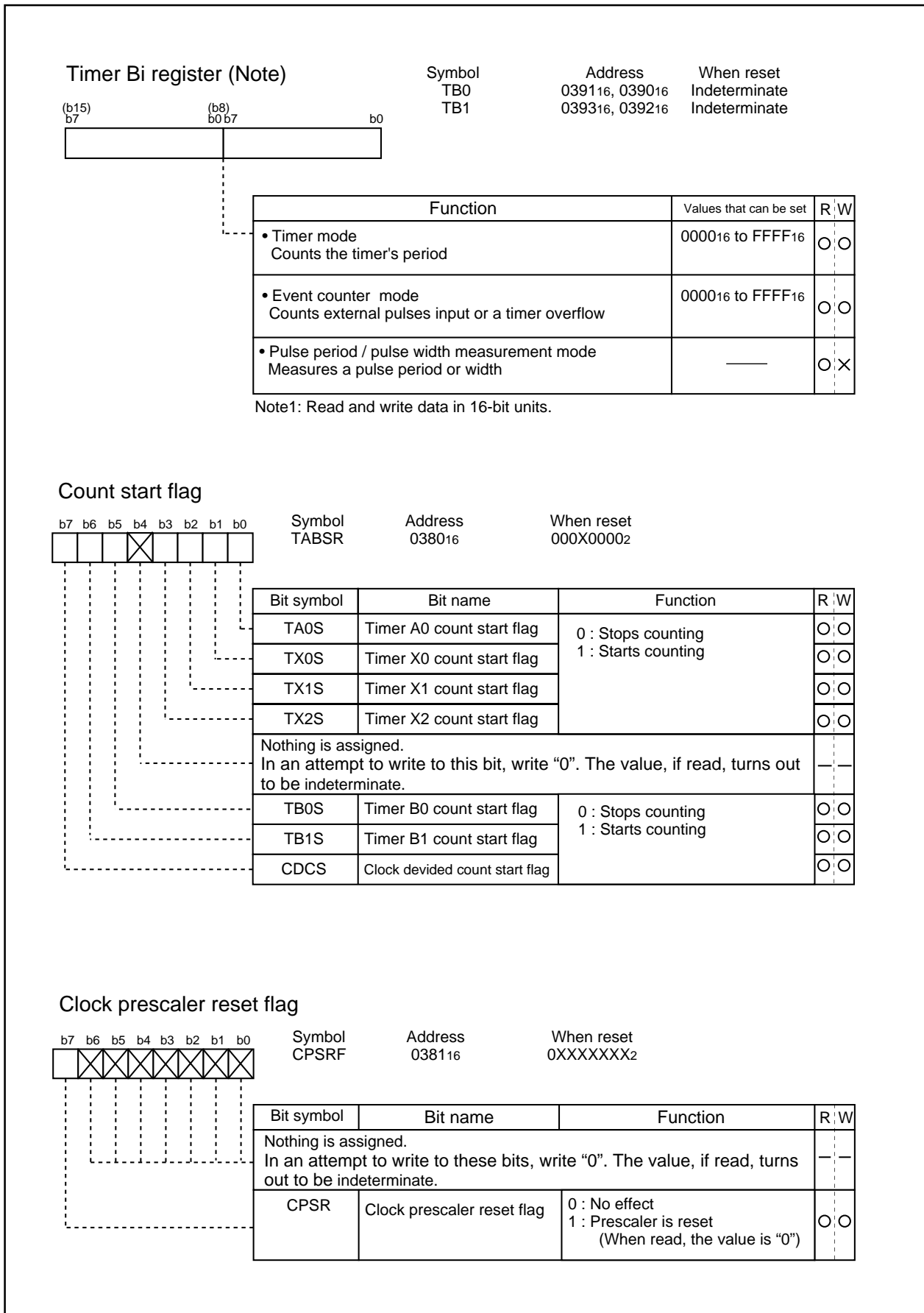


Figure 2.3.2. Timer B-related registers (1)

Timer B



Timer B

2.3.2 Operation of Timer B (timer mode)

In timer mode, choose functions from those listed in Table 2.3.1. Operations of the circled items are described below. Figure 2.3.4 shows the operation timing, and Figure 2.3.5 shows the set-up procedure.

Table 2.3.1. Chosed functions

Item	Set-up	
Count source	○	Internal count source (f1 / f8 / f32 / fc32)

- Operation
- (1) Setting the count start flag to "1" causes the counter to perform a down count on the count source.
 - (2) If an underflow occurs, the content of the reload register is reloaded, and the counter continues counting. At this time, the timer Bi interrupt request bit goes to "1".
 - (3) Setting the count start flag to "0" causes the counter to hold its value and to stop.

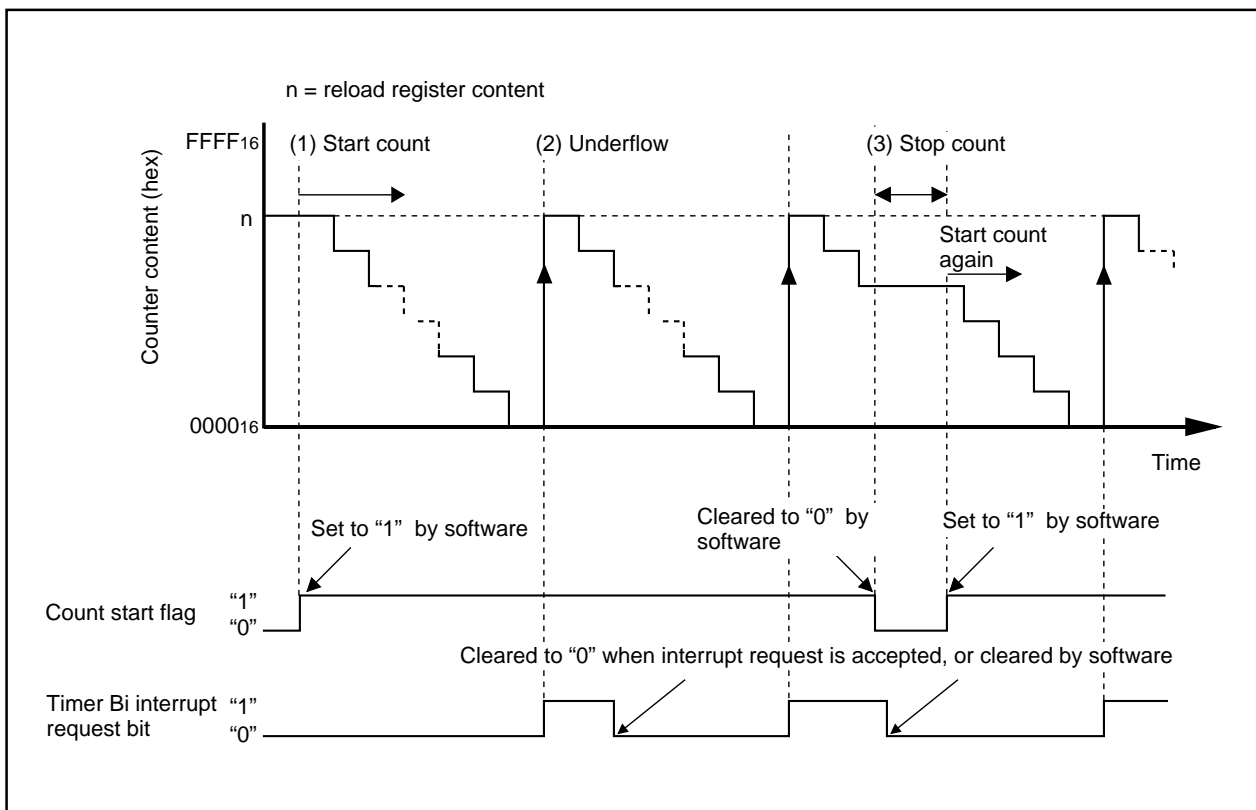
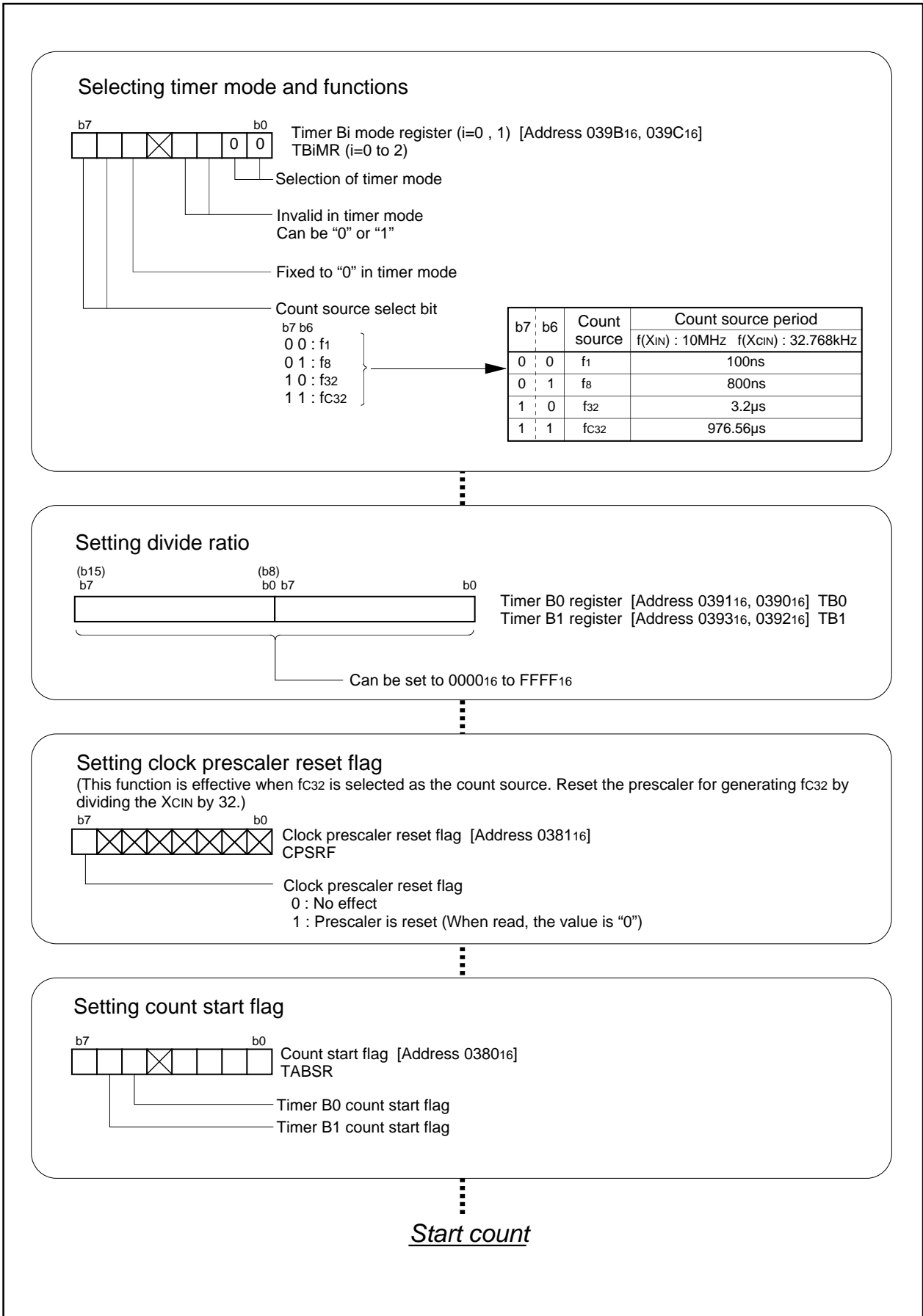


Figure 2.3.4. Operation timing of timer mode

Timer B



Timer B

2.3.3 Operation of Timer B (event counter mode)

In event counter mode, choose functions from those listed in Table 2.3.2. Operations of the circled items are described below. Figure 2.3.6 shows the operation timing, and Figure 2.3.7 shows the set-up procedure.

Table 2.3.2. Chosed functions

Item	Set-up
Count source	0 Input signal to the TBiIN pin (counting falling edges)
	Input signal to the TBiIN pin (counting rising edges)
	Input signal to the TBiIN pin (counting rising edges and falling edges)
	Timer overflow(TBj overflow)

- Operation
- (1) Setting the count start flag to "1" causes the counter to count the falling edges of the count source.
 - (2) If an underflow occurs, the content of the reload register is reloaded, and the count continues. At this time, the timer Bi interrupt request bit goes to "1".
 - (3) Setting the count start flag to "0" causes the counter to hold its value and to stop.

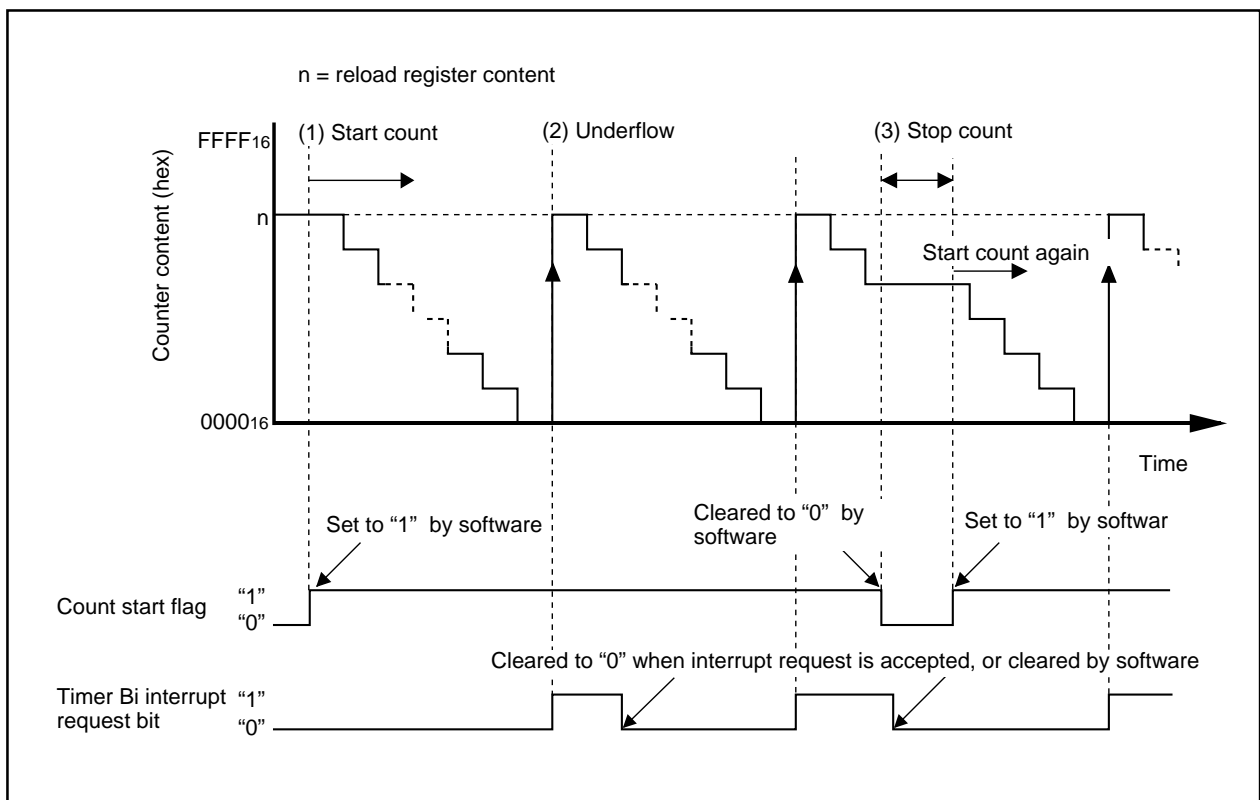


Figure 2.3.6. Operation timing of event counter mode

Timer B

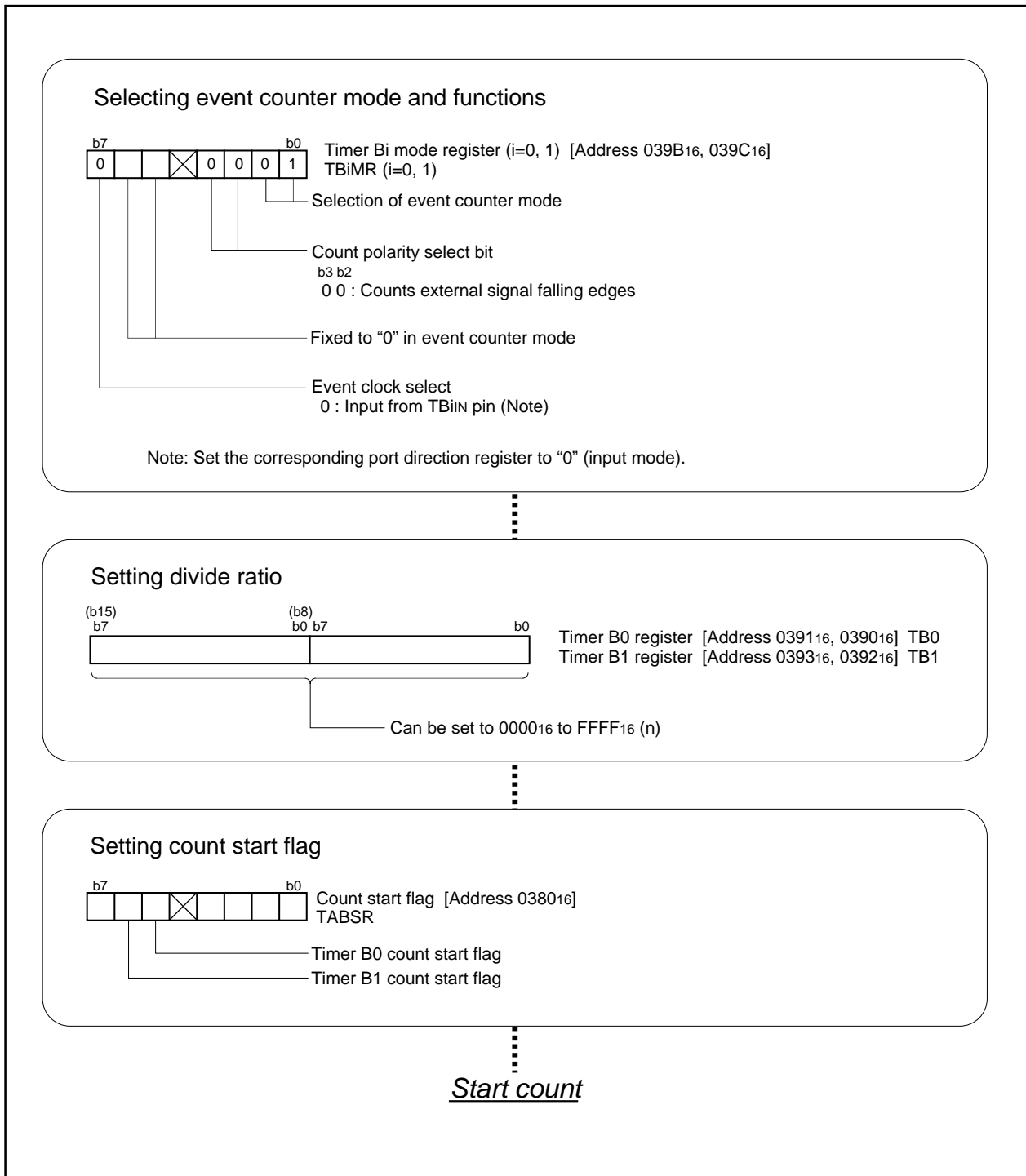


Figure 2.3.7. Set-up procedure of event counter mode

Timer B

2.3.4 Operation of Timer B (pulse period measurement mode)

In pulse period/pulse width measurement mode, choose functions from those listed in Table 2.3.3. Operations of the circled items are described below. Figure 2.3.8 shows the operation timing, and Figure 2.3.9 shows the set-up procedure.

Table 2.3.3. Chosed functions

Item	Set-up
Count source	○ Internal count source ($f_1 / f_8 / f_{32} / f_{c32}$)
Measurement mode	○ Pulse period measurement (interval between measurement pulse falling edge to falling edge)
	○ Pulse period measurement (interval between measurement pulse rising edge to rising edge)
	○ Pulse width measurement (interval between measurement pulse falling edge to rising edge, and between rising edge to falling edge)

- Operation
- (1) Setting the count start flag to "1" causes the counter to start counting the count source.
 - (2) If a measurement pulse changes from "H" to "L", the value of the counter goes to "0000₁₆", and measurement is started. In this instance, an indeterminate value is transferred to the reload register. The timer Bi interrupt request does not generate.
 - (3) If a measurement pulse changes from "H" to "L" again, the value of the counter is transferred to the reload register, and the timer Bi interrupt request bit goes to "1". Then the value of the counter becomes "0000₁₆", and the measurement is started again.

- Note
- The timer Bi interrupt request bit goes to "1" when an effective edge of a measurement pulse is input or timer Bi is overflowed. The factor of interrupt request can be determined by use of the timer Bi overflow flag within the interrupt routine.
 - The value of the counter at the beginning of a count is indeterminate. Thus there can be instances in which the timer Bi overflow flag goes to "1" immediately after a count is performed.
 - The timer Bi overflow flag goes to "0" if timer Bi mode register is written to when the count start flag is "1". This flag cannot be set to "1" by software.

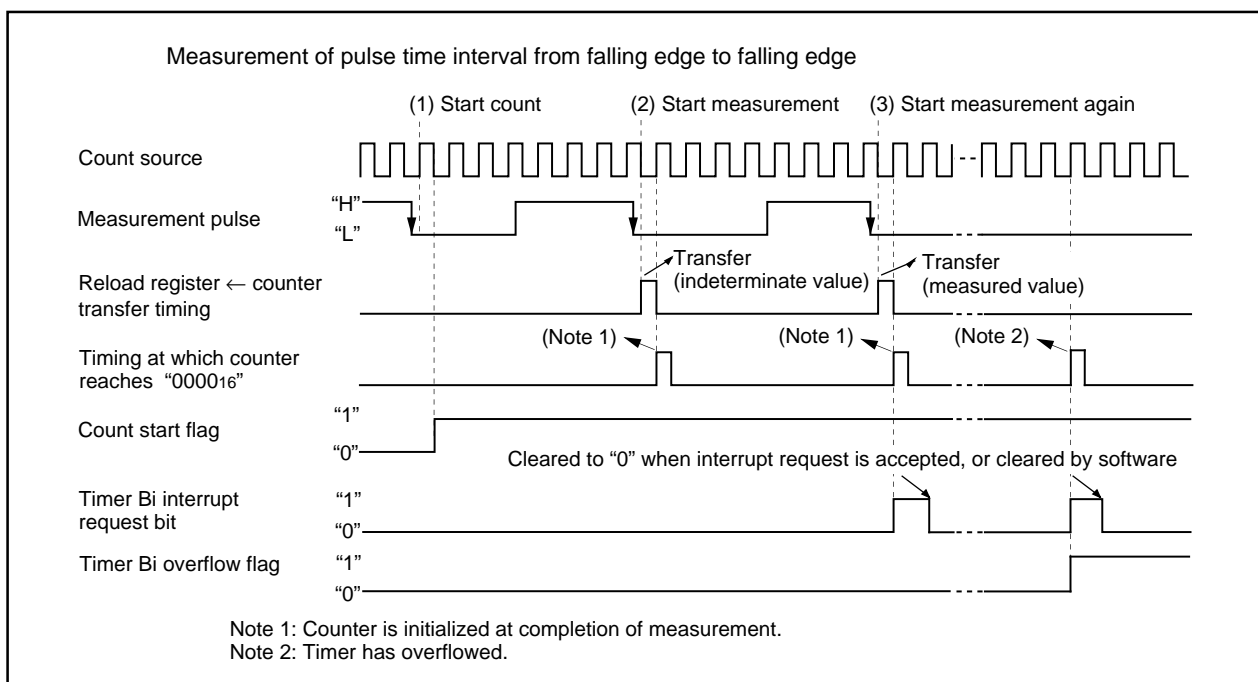


Figure 2.3.8. Operation timing of pulse period measurement mode

Timer B

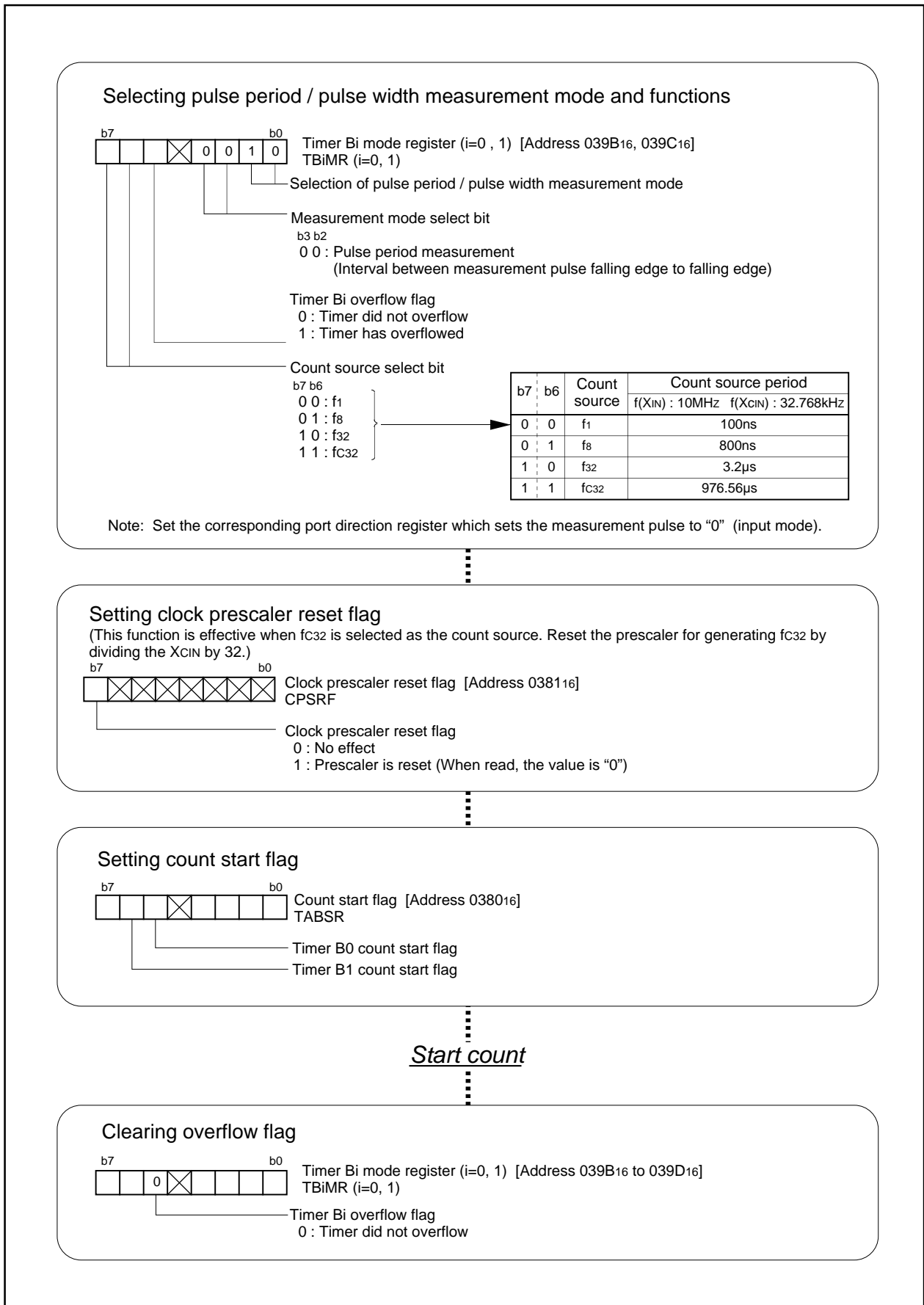


Figure 2.3.9. Set-up procedure of pulse period measurement mode

Timer B

2.3.5 Operation of Timer B (pulse width measurement mode)

In pulse period/pulse width measurement mode, choose functions from those listed in Table 2.3.4. Operations of the circled items are described below. Figure 2.3.10 shows the operation timing, and Figure 2.3.11 shows the set-up procedure.

Table 2.3.4. Chosed functions

Item	Set-up
Count source	○ Internal count source ($f_1 / f_8 / f_{32} / f_{c32}$)
Measurement mode	Pulse period measurement (interval between measurement pulse falling edge to falling edge)
	Pulse period measurement (interval between measurement pulse rising edge to rising edge)
	○ Pulse width measurement (interval between measurement pulse falling edge to rising edge, and between rising edge to falling edge)

- Operation
- (1) Setting the count start flag to "1" causes the counter to start counting the count source.
 - (2) If an effective edge of a pulse to be measured is input, the value of the counter goes to "0000₁₆", and measurement is started. In this instance, an indeterminate value is transferred to the reload register. The timer Bi interrupt request does not generate.
 - (3) If an effective edge of a pulse to be measured is input again, the value of the counter is transferred to the reload register, and the timer Bi interrupt request bit goes to "1". Then the value of the counter becomes "0000₁₆", and measurement is started again.

- Note
- The timer Bi interrupt request bit goes to "1" when an effective edge of a pulse to be measured is input or timer Bi is overflows. The factor of interrupt request can be determined by use of the timer Bi overflow flag within the interrupt routine.
 - The value of the counter at the beginning of a count is indeterminate. Thus there can be instances in which the timer Bi overflow flag goes to "1" immediately after a count is performed.
 - The timer Bi overflow flag goes to "0" if timer Bi mode register is written to when the count start flag is "1". This flag cannot be set to "1" by software.

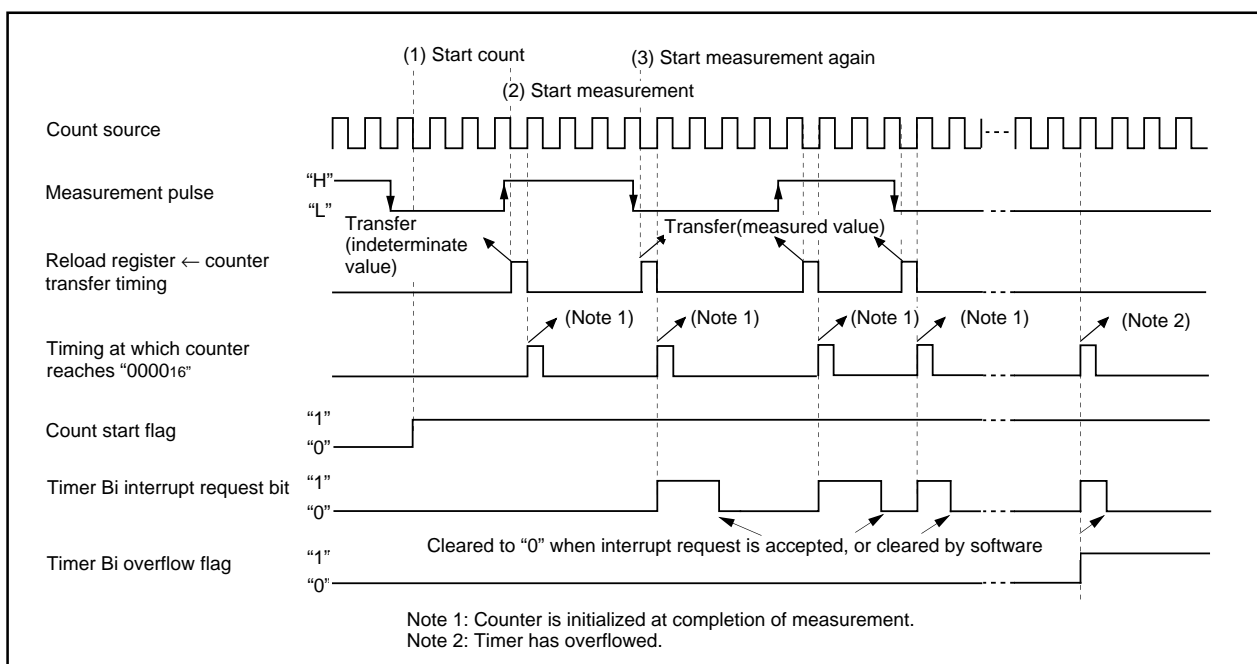


Figure 2.3.10. Operation timing of pulse width measurement mode

Timer B

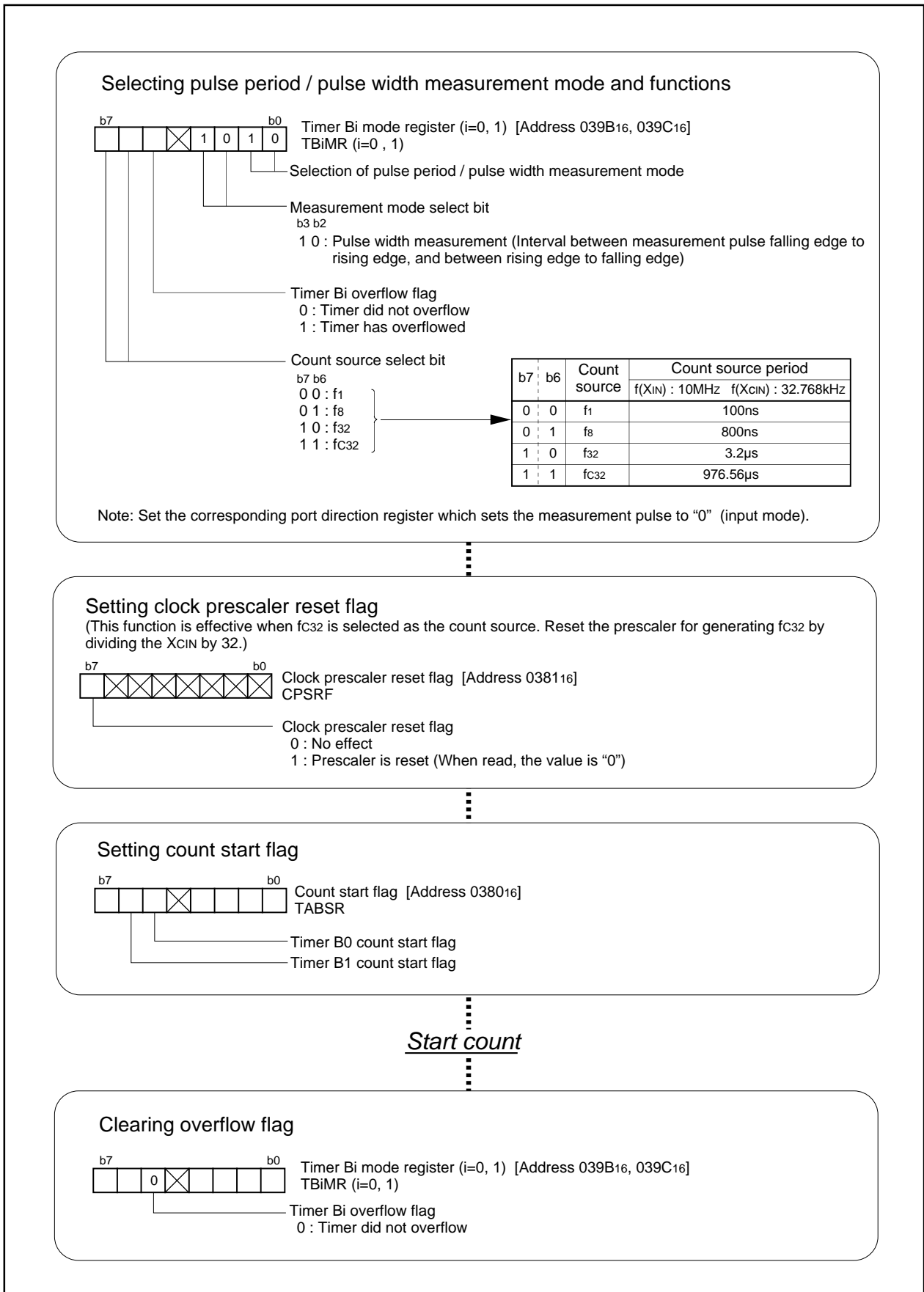


Figure 2.3.11. Set-up procedure of pulse width measurement mode

Timer B

2.3.6 Precautions for Timer B (timer mode, event counter mode)

- (1) To clear reset, the count start flag is set to "0". Set a value in the timer Bi register, then set the flag to "1".
- (2) Reading the timer Bi register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the timer Bi register with the reload timing shown in Figure 2.3.12 gets "FFFF₁₆". Reading the timer Bi register after setting a value in the timer Bi register with a count halted but before the counter starts counting gets a proper value.

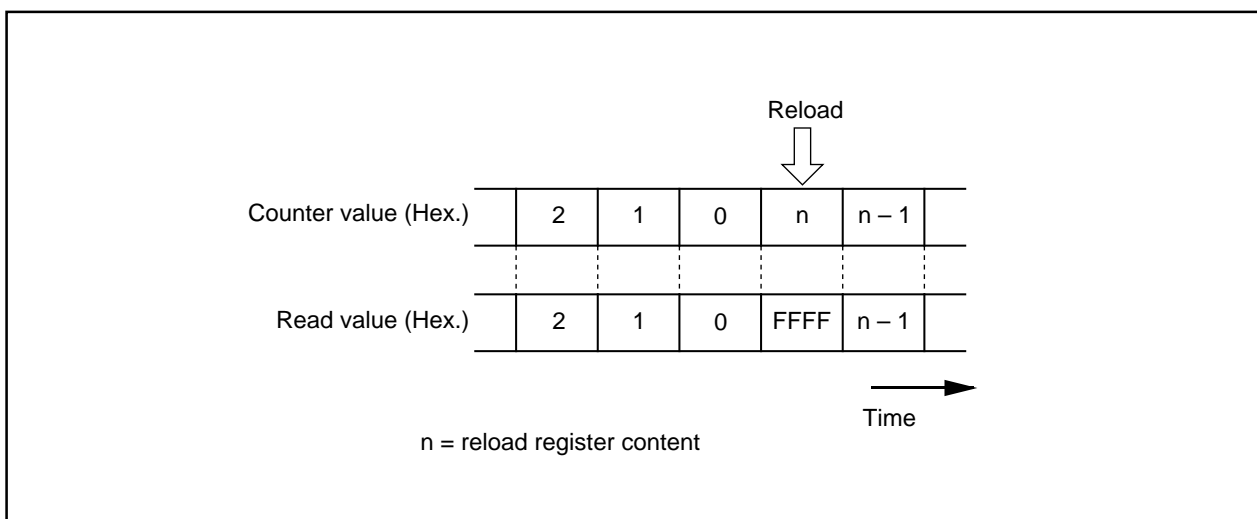


Figure 2.3.12. Reading timer Bi register

2.3.7 Precautions for Timer B (pulse period/pulse width measurement mode)

- (1) The timer Bi interrupt request bit goes to "1" when an effective edge of a measurement pulse is input or timer Bi is overflowed. The factor of interrupt request can be determined by use of the timer Bi overflow flag within the interrupt routine.
- (2) If the timer overflow occurs simultaneously with the input of a measurement pulse, and if the interrupt factor cannot be determined from the timer Bi overflow flag, connect the timers and count the number of overflows.
- (3) When reset, the timer Bi overflow flag goes to "1". This flag can be set to "0" by writing to the timer Bi mode register when the count start flag is "1".
- (4) Use the timer Bi interrupt request bit to detect only overflows. Use the timer Bi overflow flag only to determine the interrupt factor within the interrupt routine.
- (5) When the first effective edge is input after a count is started, an indeterminate value is transferred to the reload register. At this time, timer Bi interrupt request is not generated.
- (6) The value of the counter is indeterminate at the beginning of a count. Therefore the timer Bi overflow flag may go to "1" immediately after a count is started.
- (7) If changing the measurement mode select bit is set after a count is started, the timer Bi interrupt request bit goes to "1".
- (8) If the input signal to the TBiIN pin is affected by noise, precise measurement may not be performed in some cases. It is recommended to see that measurements fall within a specific range by use of software.
- (9) For pulse width measurement, pulse widths are successively measured. Use software to check whether the measurement result is an "H" level width or an "L" level width.

2.4 Timer X

2.4.1 Overview

The following is an overview for timer X, a 16-bit timer.

(1) Mode

Timer X operates in one of the four modes:

(a) Timer mode

In this mode, the internal count source is counted. Two functions can be selected: the pulse output function that reverses output from a port every time an overflow occurs, or the gate function which controls the count start/stop according to the input signal from a port.

- Timer mode operation P224
- Timer mode, gate function operation P226
- Timer mode, pulse output function operation P228

(b) Event counter mode

This mode counts the pulses from the outside and the number of overflows in other timers. The free-run type, in which nothing is reloaded from the reload register, can be selected when an underflow occurs. The pulse output function can also be selected.

- Event counter mode operation P230
- Event counter mode, free run type operation P232

(c) One-shot timer mode

In this mode, the timer is started by the trigger and stops when the timer goes to "0". The trigger can be selected from the following 3 types: an external input signal, an overflow of the timer, or a software trigger.

- One-shot timer mode operation P234

(d) Pulse period measurement/pulse width measurement mode

External pulse period or external pulse widths are measured. If pulse period measurement mode is selected, the periods of input pulses are continuously measured. If pulse width measurement mode is selected, widths of "H" level pulses and those of "L" level pulses are continuously measured.

- Operation in pulse period measurement mode P236
- Operation in pulse width measurement mode P238

(d) Pulse width modulation (PWM) mode

In this mode, the arbitrary pulses are successively output. Either a 16-bit fixed-period PWM mode or 8-bit variable-period mode can be selected. The trigger for initiating output can also be selected.

- 16-bit PWM mode operation P240
- 8-bit PWM mode operation P242

(2) Count source

The internal count source can be selected from f1, f8, f32, and fc32. Clocks f1, f8, and f32 are derived by dividing the CPU's main clock by 1, 8, and 32 respectively. Clock fc32 is derived by dividing the CPU's secondary clock by 32.

Timer X

(3) Frequency division ratio

In timer mode or pulse width modulation mode, [the value set in the timer register + 1] becomes the frequency division ratio. In event counter mode, [the set value + 1] becomes the frequency division ratio when a down count is performed, or $[FFFF_{16} - \text{the set value} + 1]$ becomes the frequency division ratio when an up count is performed. In one-shot timer mode, the value set in the timer register becomes the frequency division ratio.

The counter overflows (or underflows) when a count source equal to a frequency division ratio is input, and an interrupt occurs. For the pulse output function, the output from the port varies (the value in the port register does not vary).

(4) Reading the timer

Either in timer mode or in event counter mode, reading the timer register takes out the count at that moment. Read it in 16-bit units. The data either in one-shot timer mode or in pulse width modulation mode is indeterminate. In both the pulse period measurement mode and pulse width measurement mode, an indeterminate value is read until the second effective edge is input after a count is started, otherwise, the measurement results are read.

(5) Writing to the timer

When writing to the timer register while a count is in progress, the value is written only to the reload register. When writing to the timer register while a count has stopped, the value is written both to the reload register and the count. Write the value in 16-bit increments. The timer register cannot be written to in either the pulse period measurement mode or the pulse width measurement mode.

(6) Relation between the input/output to/from the timer and the direction register

With the output function of the timer, set the direction register of the relevant port to input. To input an external signal to the timer, set the direction register of the relevant port to input. However, pulse output cannot be selected when inputting an external signal to the timer, and vice-versa.

(7) Pins related to timer X

(a) TX0INOUT, TX1INOUT, TX2INOUT Input/output pins to timer X.

(8) Registers related to timer X

Figure 2.4.1 shows the memory map of timer X-related registers. Figures 2.4.2 and 2.4.3 show timer X-related registers.

0056 ₁₆	Timer X0 interrupt control register (TX0IC)
0057 ₁₆	Timer X1 interrupt control register (TX1IC)
0058 ₁₆	Timer X2 interrupt control register (TX2IC)
~	~
0380 ₁₆	Count start flag (TABSR)
0381 ₁₆	Clock prescaler reset flag (CPSRF)
0382 ₁₆	One-shot start flag (ONSF)
0383 ₁₆	Trigger select register (TRGSR)
0384 ₁₆	Up-down flag (UDF)
~	~
0388 ₁₆	Timer X0 (TX0)
0389 ₁₆	
038A ₁₆	
038B ₁₆	
038C ₁₆	Timer X1 (TX1)
038D ₁₆	
038E ₁₆	
038F ₁₆	
~	~
0397 ₁₆	Timer X0 mode register (TX0MR)
0398 ₁₆	Timer X1 mode register (TX1MR)
0399 ₁₆	Timer X2 mode register (TX2MR)

Figure 2.4.1. Memory map of timer X-related registers

Timer X

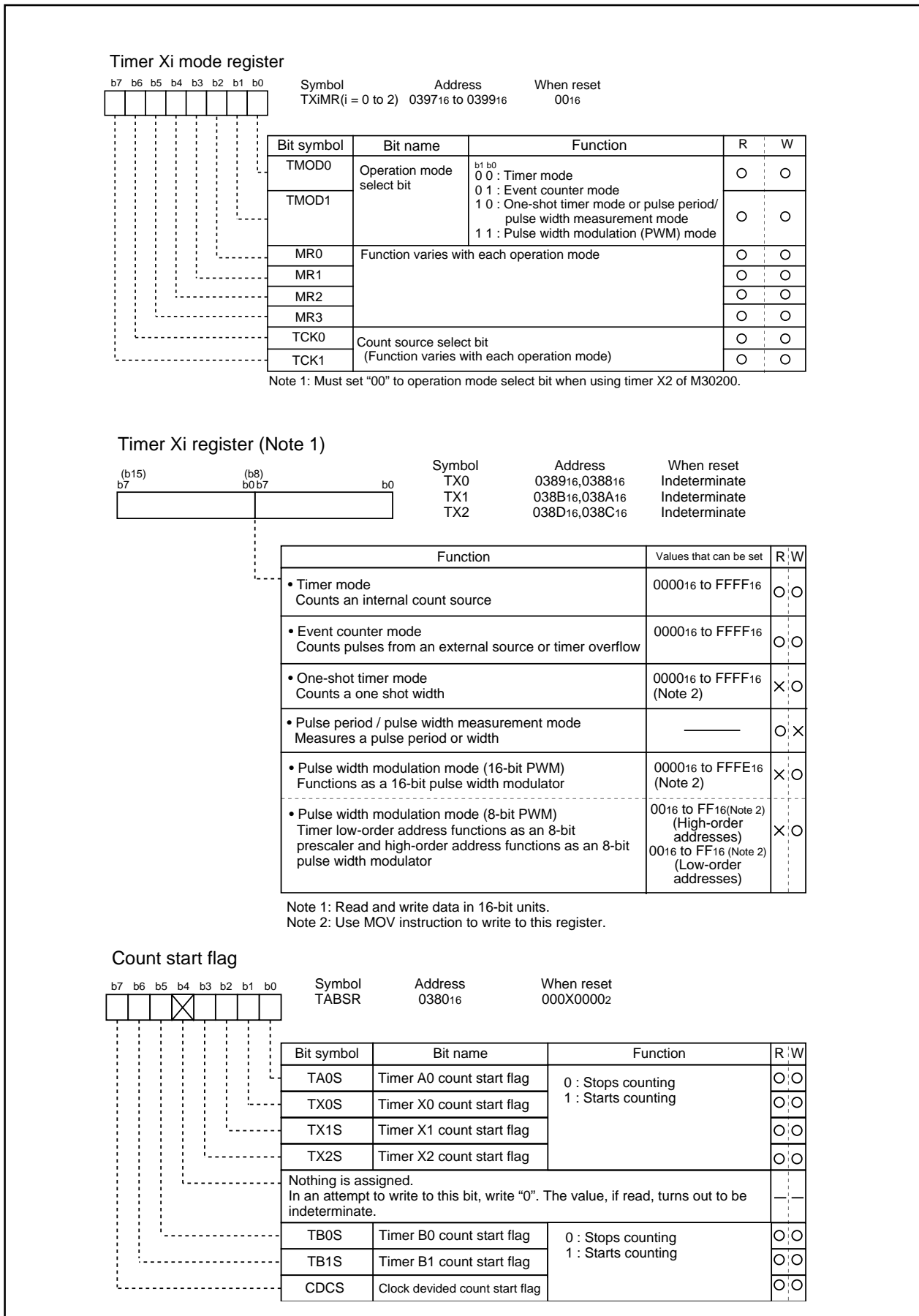


Figure 2.4.2. Timer X-related registers (1)

Timer X

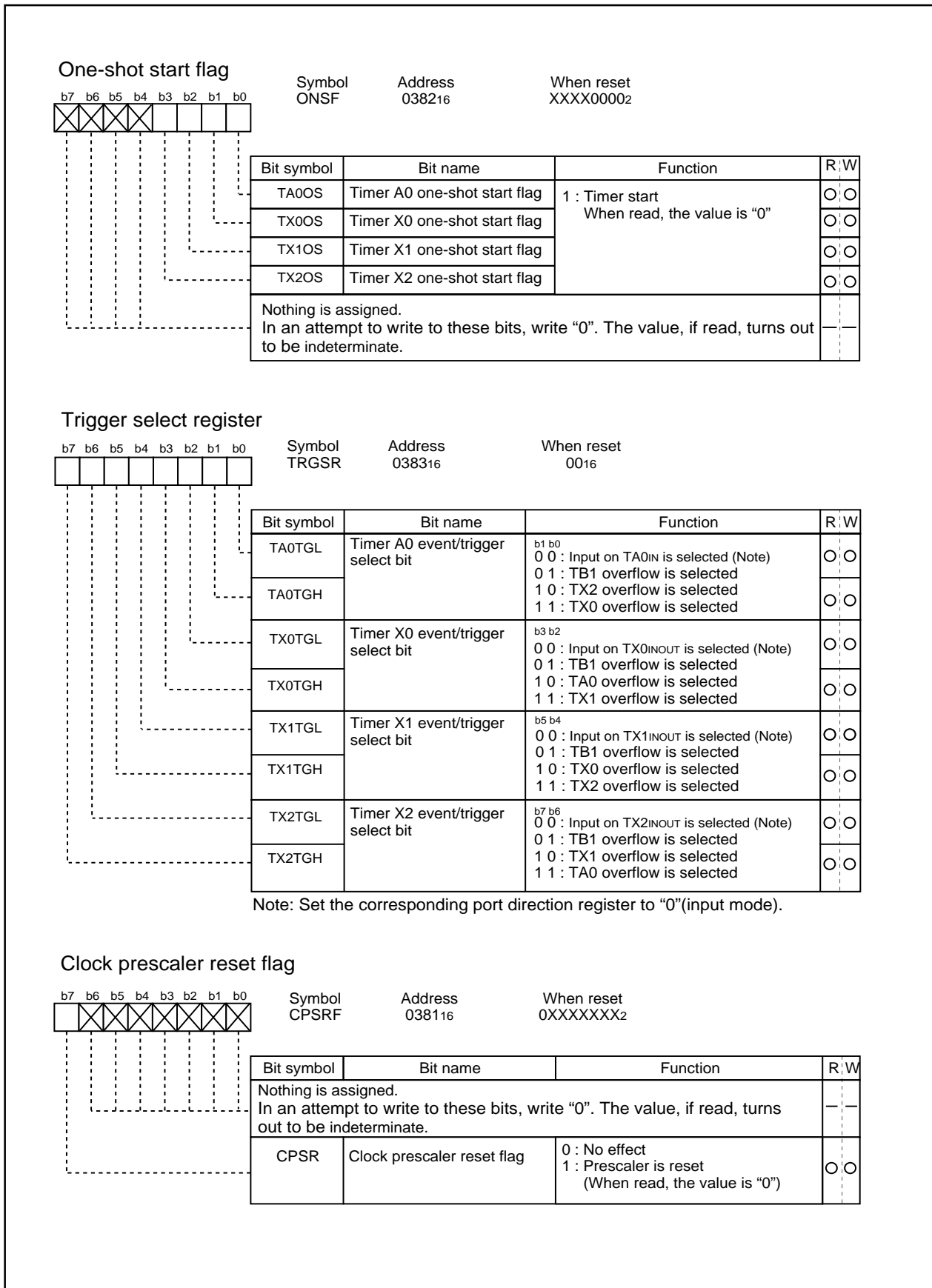


Figure 2.4.3. Timer X-related registers (2)

Timer X

2.4.2 Operation of Timer X (timer mode)

In timer mode, choose functions from those listed in Table 2.4.1. Operations of the circled items are described below. Figure 2.4.4 shows the operation timing, and Figure 2.4.5 shows the set-up procedure.

Table 2.4.1. Chosed functions

Item	Set-up
Count source	○ Internal count source (f ₁ / f ₈ / f ₃₂ / f _{c32})
Pulse output function	○ No pulses output
	Pulses output
Gate function	○ No gate function
	Performs count only for the period in which the TXiINOUT pin is at "L" level
	Performs count only for the period in which the TXiINOUT pin is at "H" level

- Operation
- (1) Setting the count start flag to "1" causes the counter to perform a down count on the count source.
 - (2) If an underflow occurs, the content of the reload register is reloaded, and the count continues. At this time, the timer Xi interrupt request bit goes to "1".
 - (3) Setting the count start flag to "0" causes the counter to hold its value and to stop.

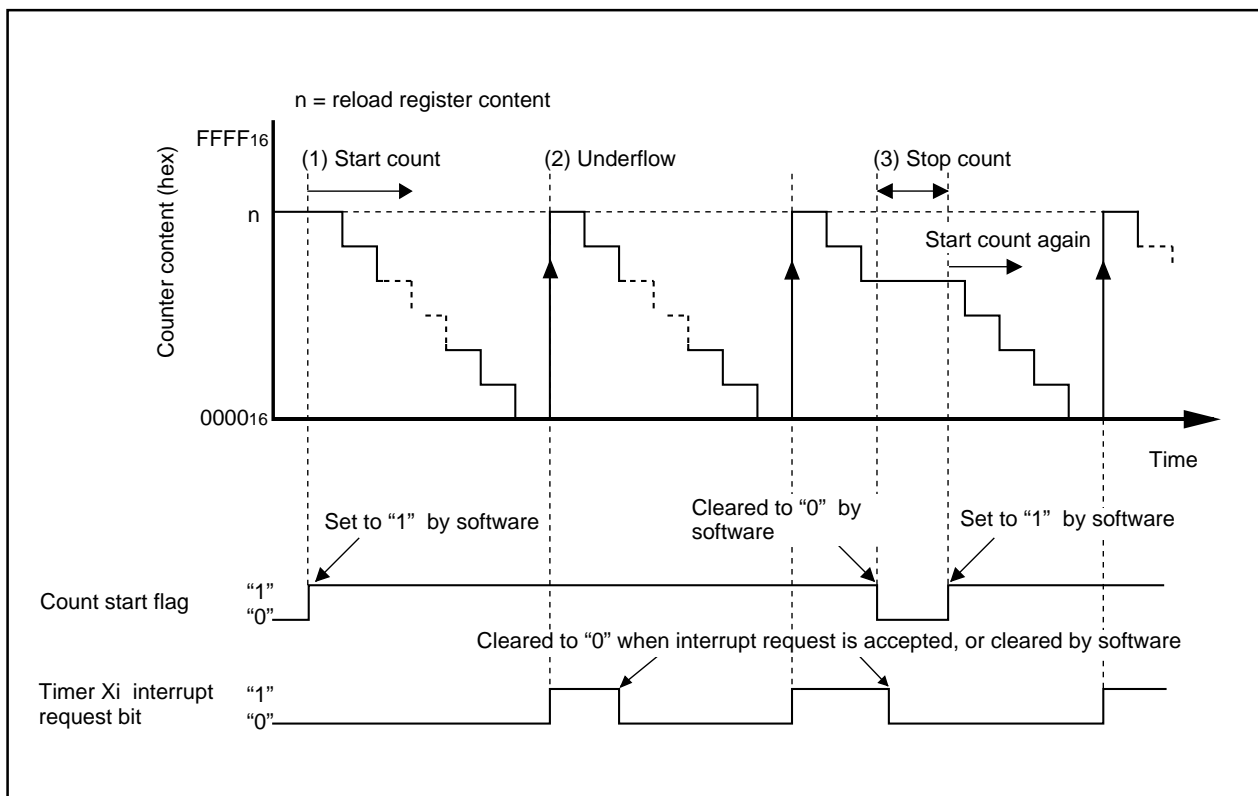


Figure 2.4.4. Operation timing of timer mode

Timer X

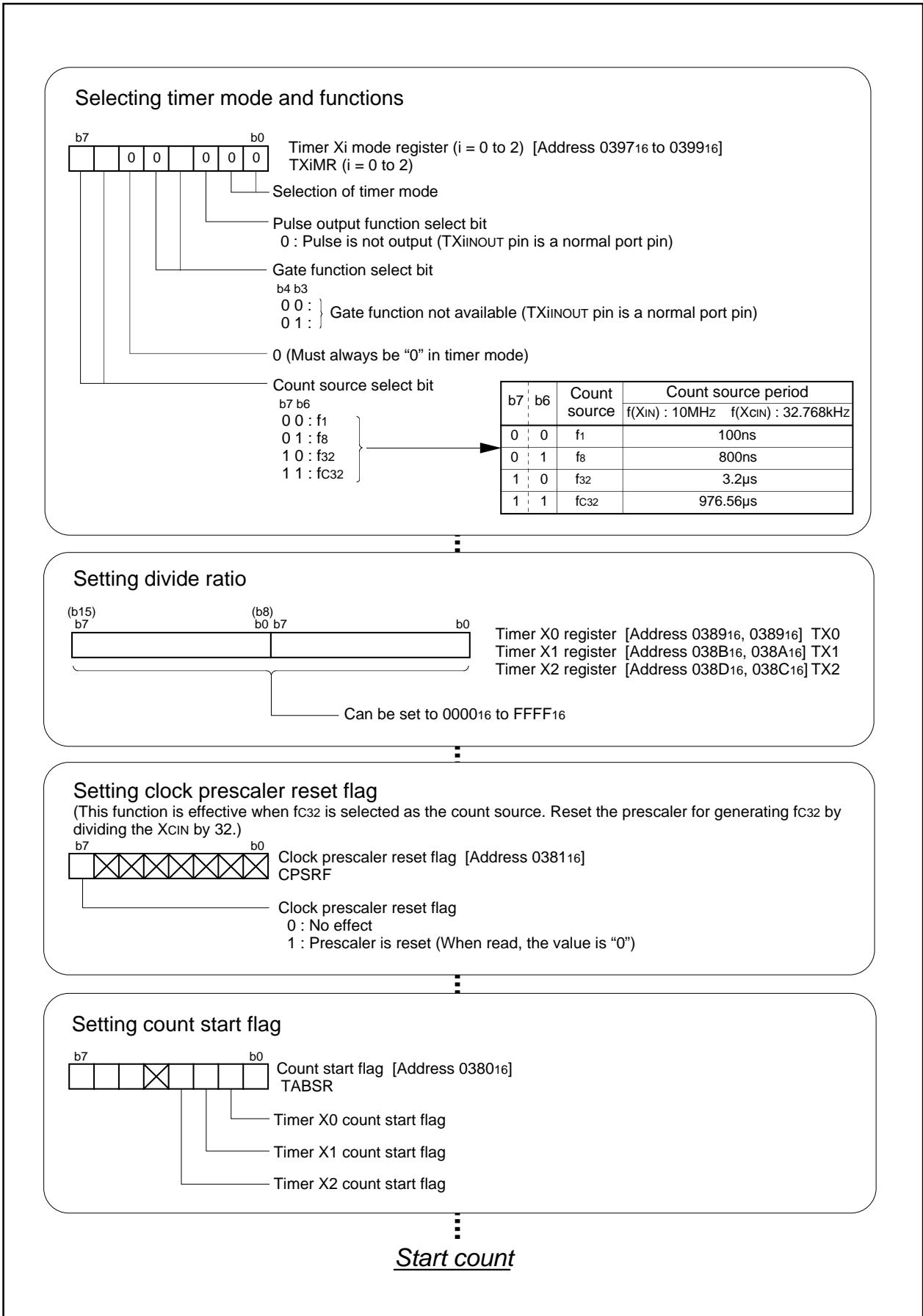


Figure 2.4.5. Set-up procedure of timer mode

2.4.3 Operation of Timer X (timer mode, gate function selected)

In timer mode, choose functions from those listed in Table 2.4.2. Operations of the circled items are described below. Figure 2.4.6 shows the operation timing, and Figure 2.4.7 shows the set-up procedure.

Table 2.4.2. Chosed functions

Item	Set-up	
Count source	○	Internal count source (f1 / f8 / f32 / fc32)
Pulse output function	○	No pulses output
		Pulses output
Gate function		No gate function
		Performs count only for the period in which the TXiINOUT pin is at "L" level
	○	Performs count only for the period in which the TXiINOUT pin is at "H" level

- Operation
- (1) When the count start flag is set to "1" and the TXiINOUT pin inputs at "H" level, the counter performs a down count on the count source.
 - (2) When the TXiINOUT pin inputs at "L" level, the counter holds its value and stops.
 - (3) If an underflow occurs, the content of the reload register is reloaded and the count continues. At this time, the timer Xi interrupt request bit goes to "1".
 - (4) Setting the count start flag to "0" causes the counter to hold its value and to stop.

Note

- Make the pulse width of the signal input to the TXiINOUT pin not less than two cycles of the count source.

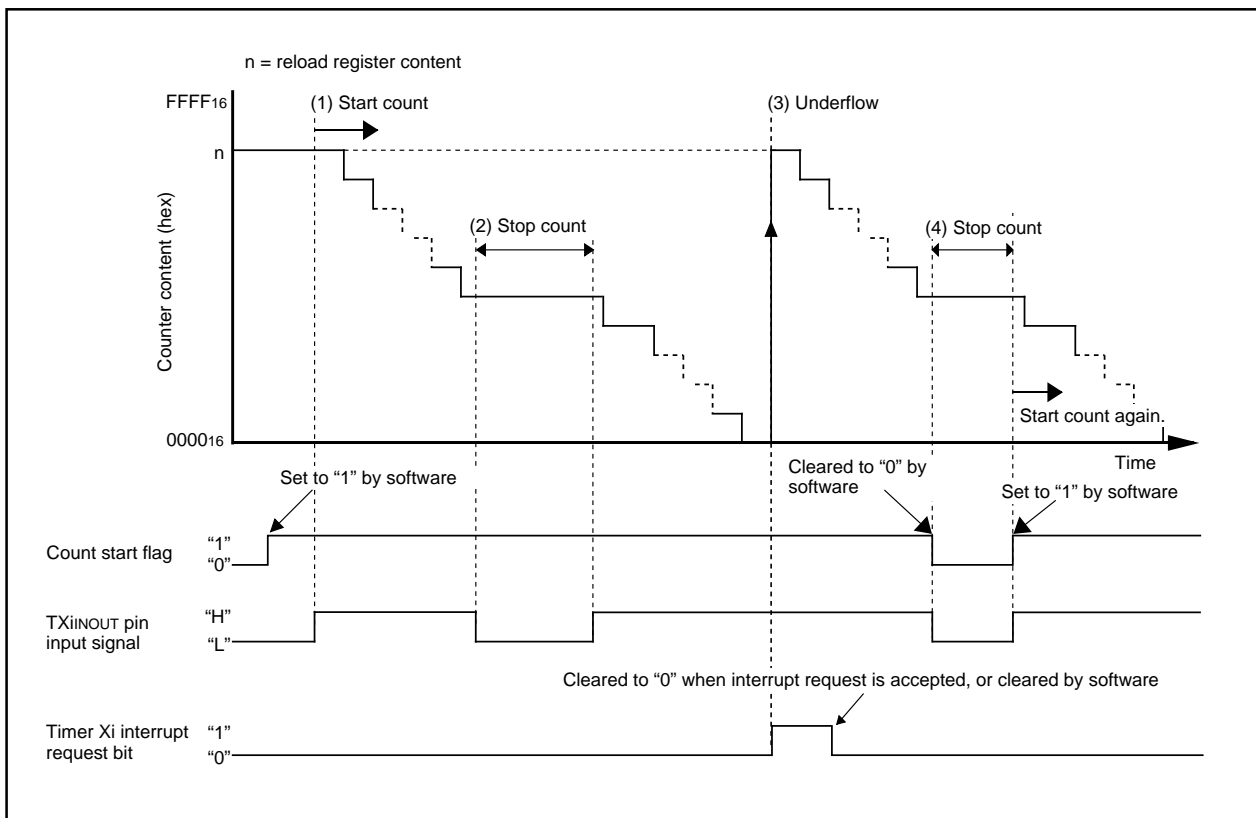
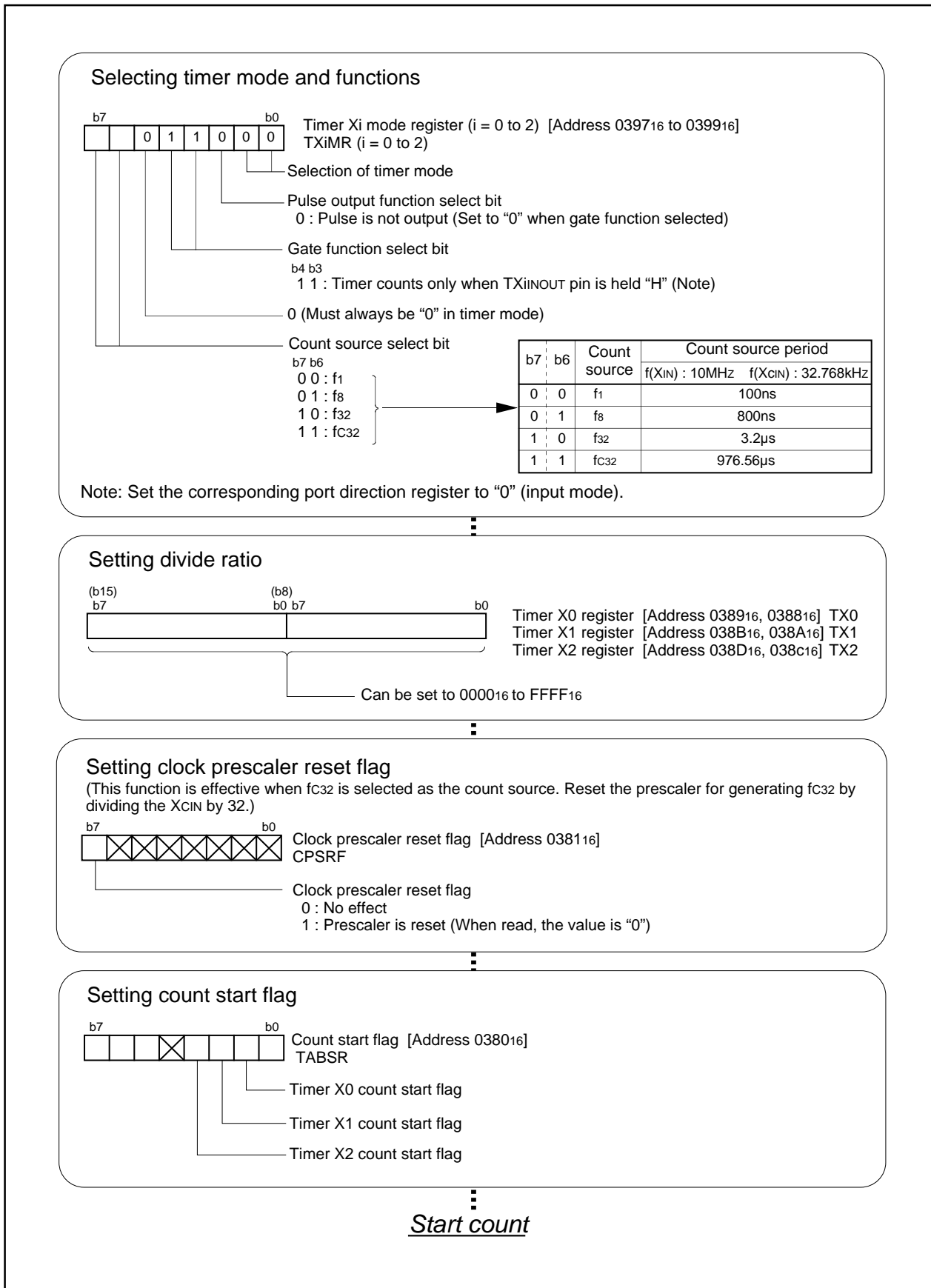


Figure 2.4.6. Operation timing of timer mode, gate function selected

Timer X



Timer X

2.4.4 Operation of Timer X (timer mode, pulse output function selected)

In timer mode, choose functions from those listed in Table 2.4.3. Operations of the circled items are described below. Figure 2.4.8 shows the operation timing, and Figure 2.4.9 shows the set-up procedure.

Table 2.4.3. Chosed functions

Item	Set-up
Count source	<input type="radio"/> Internal count source ($f_1 / f_8 / f_{32} / f_{c32}$)
Pulse output function	<input type="radio"/> No pulses output
	<input type="radio"/> Pulses output
Gate function	<input type="radio"/> No gate function
	<input type="radio"/> Performs count only for the period in which the TXiINOUT pin is at "L" level
	<input type="radio"/> Performs count only for the period in which the TXiINOUT pin is at "H" level

- Operation
- (1) Setting the count start flag to "1" causes the counter to perform a down count on the count source.
 - (2) If an underflow occurs, the content of the reload register is reloaded and the count continues. At this time, the timer Xi interrupt request bit goes to "1". Also, the output polarity of the TXiINOUT pin reverses.
 - (3) Setting the count start flag to "0" causes the counter to hold its value and to stop. Also, the TXiINOUT pin outputs an "L" level.

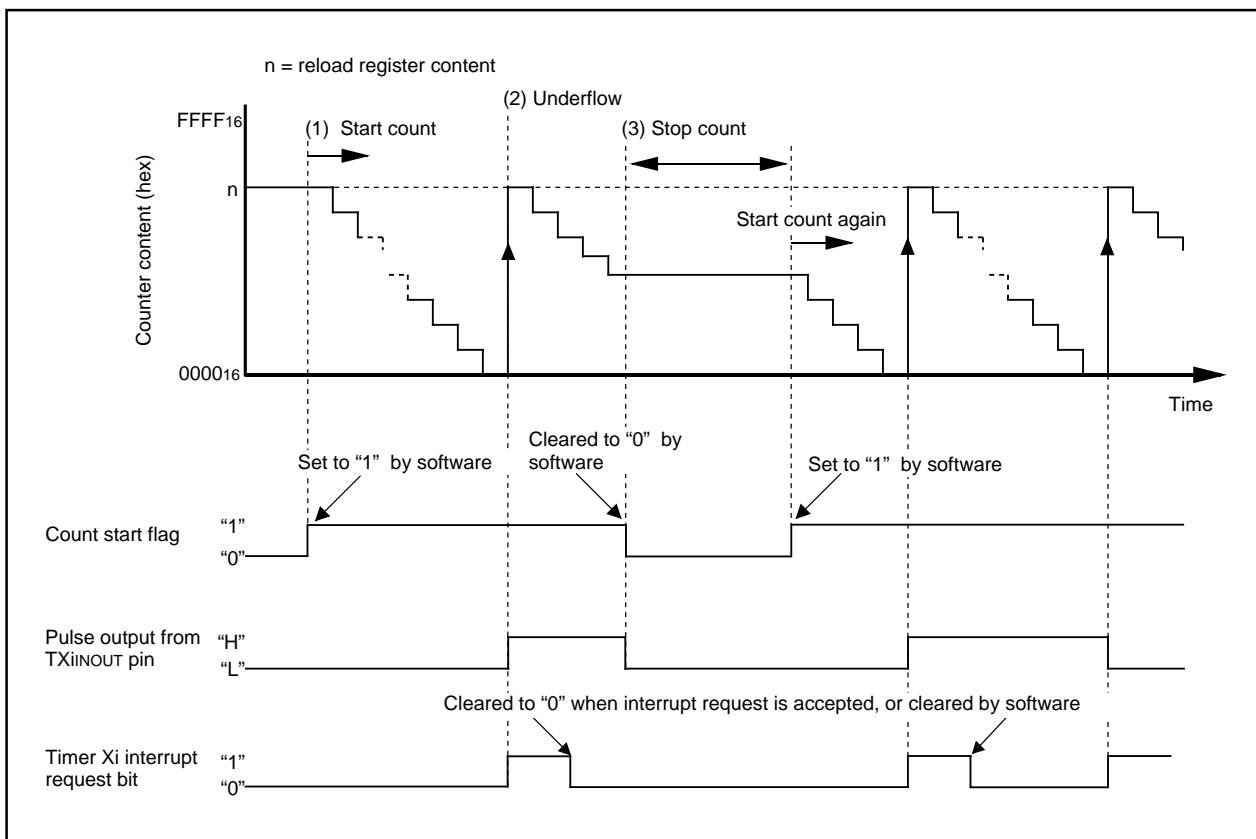


Figure 2.4.8. Operation timing of timer mode, pulse output function selected

Timer X

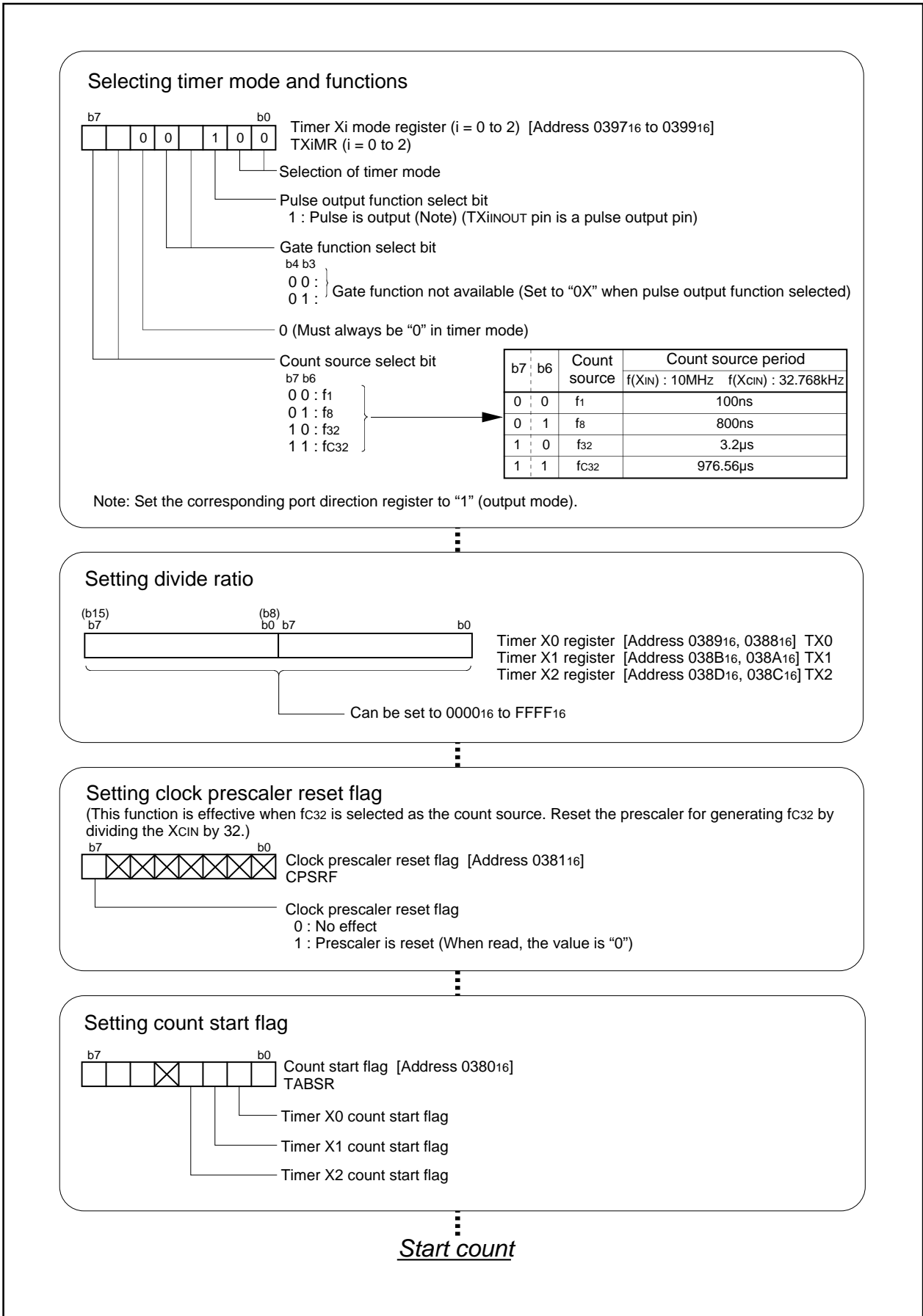


Figure 2.4.9. Set-up procedure of timer mode, pulse output function selected

Timer X

2.4.5 Operation of Timer X (event counter mode, reload type selected)

In event counter mode, choose functions from those listed in Table 2.4.4. Operations of the circled items are described below. Figure 2.4.10 shows the operation timing, and Figure 2.4.11 shows the set-up procedure.

Table 2.4.4. Chosed functions

Item	Set-up
Count source	Input signal to TXiINOUT(counting falling edges)
	Input signal to TXiINOUT(counting rising edges)
	○ Timer overflow(TB1/TA0/TXi overflow)
Pulse output function	No pulses output
	○ Pulses output
Count operation type	○ Reload type
	Free-run type

- Operation
- (1) Setting the count start flag to "1" causes the counter to count the falling edges of the count source.
 - (2) If an underflow occurs, the content of the reload register is reloaded, and the count continues. At this time, the timer Xi interrupt request bit goes to "1".
 - (3) Setting the count start flag to "0" causes the counter to hold its value and to stop.

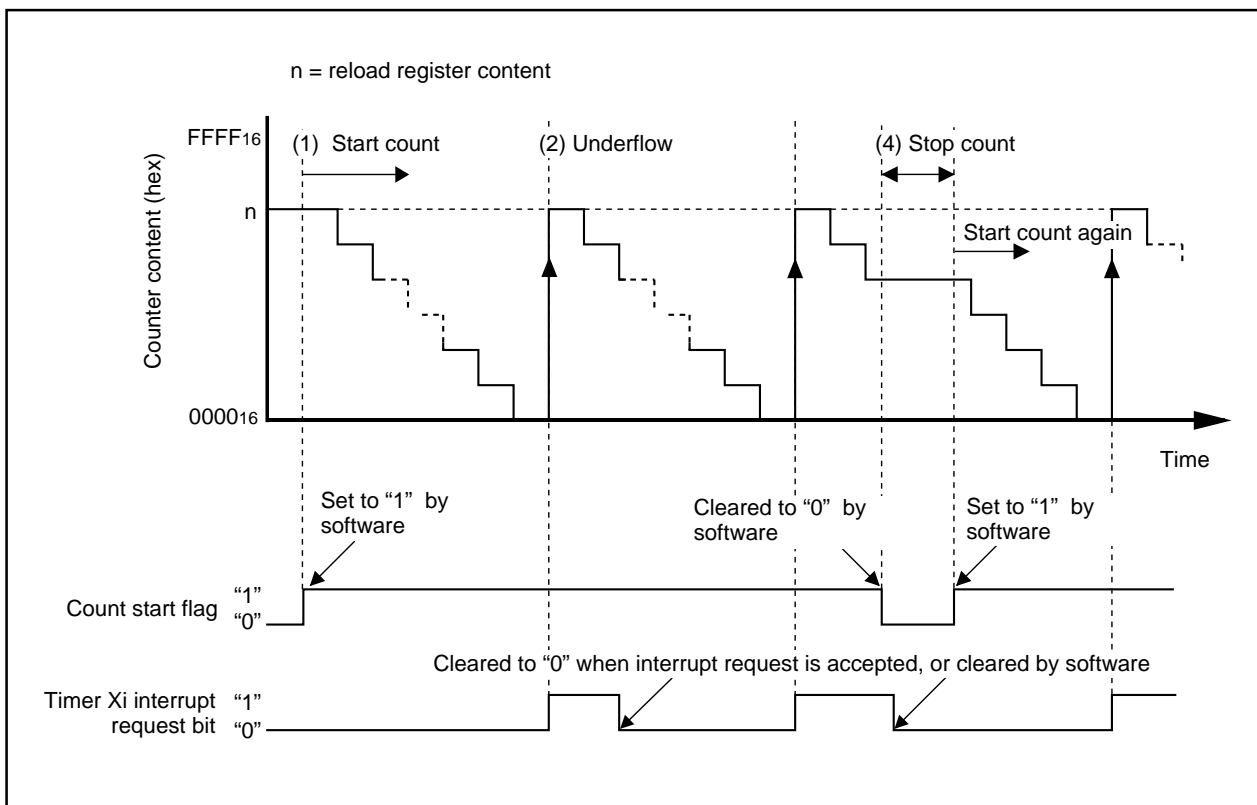
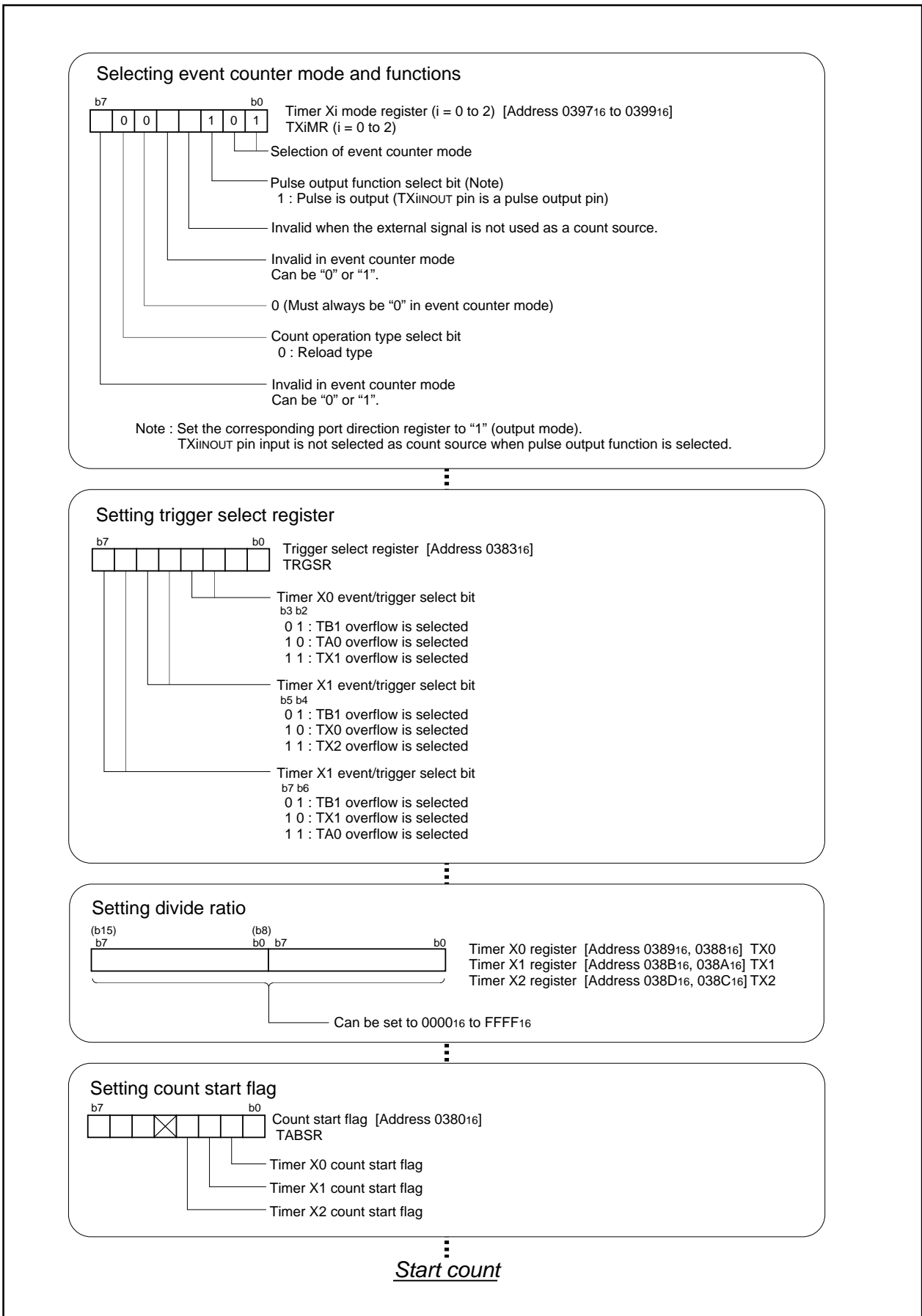


Figure 2.4.10. Operation timing of event counter mode, reload type selected

Timer X



2.4.6 Operation of Timer X (event counter mode, free run type selected)

In event counter mode, choose functions from those listed in Table 2.4.5. Operations of the circled items are described below. Figure 2.4.12 shows the operation timing, and Figure 2.4.13 shows the set-up procedure.

Table 2.4.5. Chosed functions

Item	Set-up
Count source	<input type="radio"/> Input signal to TXiINOUT(counting falling edges)
	<input type="radio"/> Input signal to TXiINOUT(counting rising edges)
	<input type="radio"/> Timer overflow(TB1/TA0/TXi overflow)
Pulse output function	<input type="radio"/> No pulses output
	<input type="radio"/> Pulses output
Count operation type	<input type="radio"/> Reload type
	<input type="radio"/> Free-run type

- Operation
- (1) Setting the count start flag to "1" causes the counter to count the falling edges of the count source.
 - (2) Even if an underflow occurs, the content of the reload register is not reloaded, but the count continues. At this time, the timer Xi interrupt request bit goes to "1".
 - (3) Setting the count start flag to "0" causes the counter to hold its value and to stop.

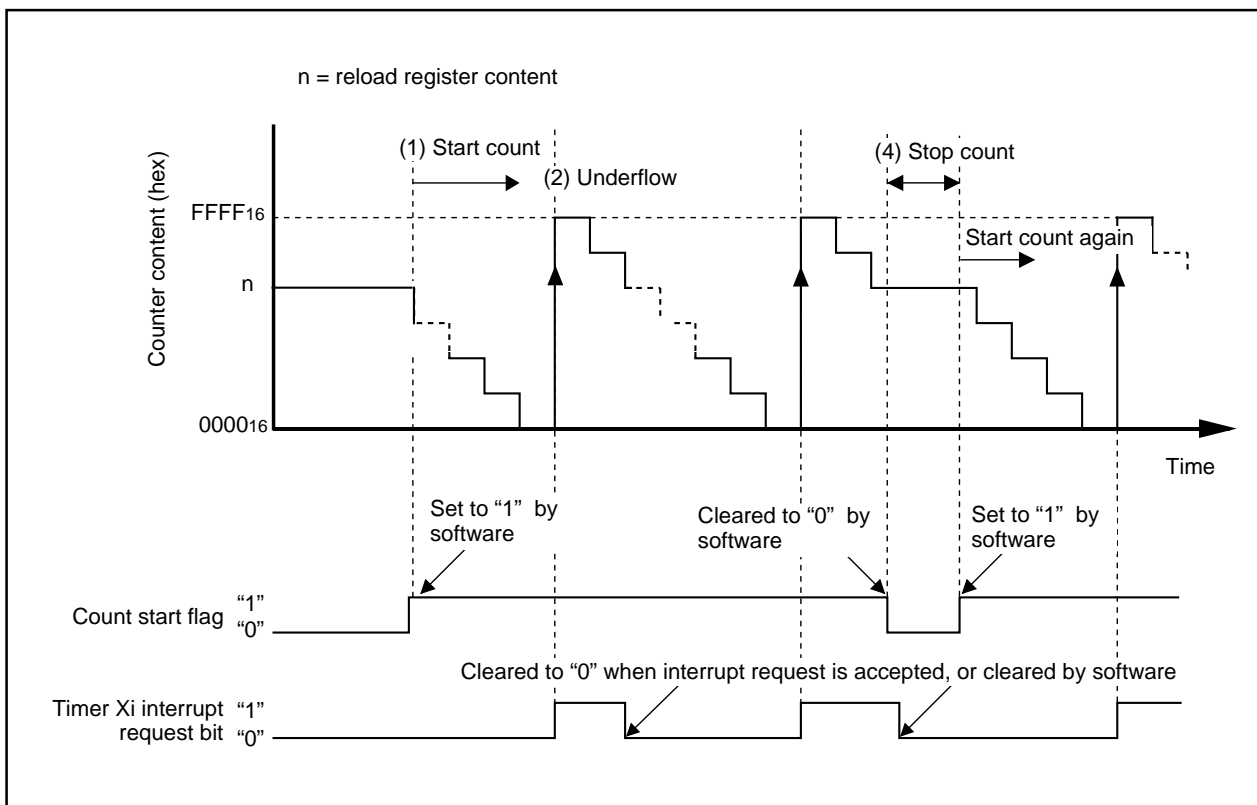


Figure 2.4.12. Operation timing of event counter mode, free run type selected

Timer X

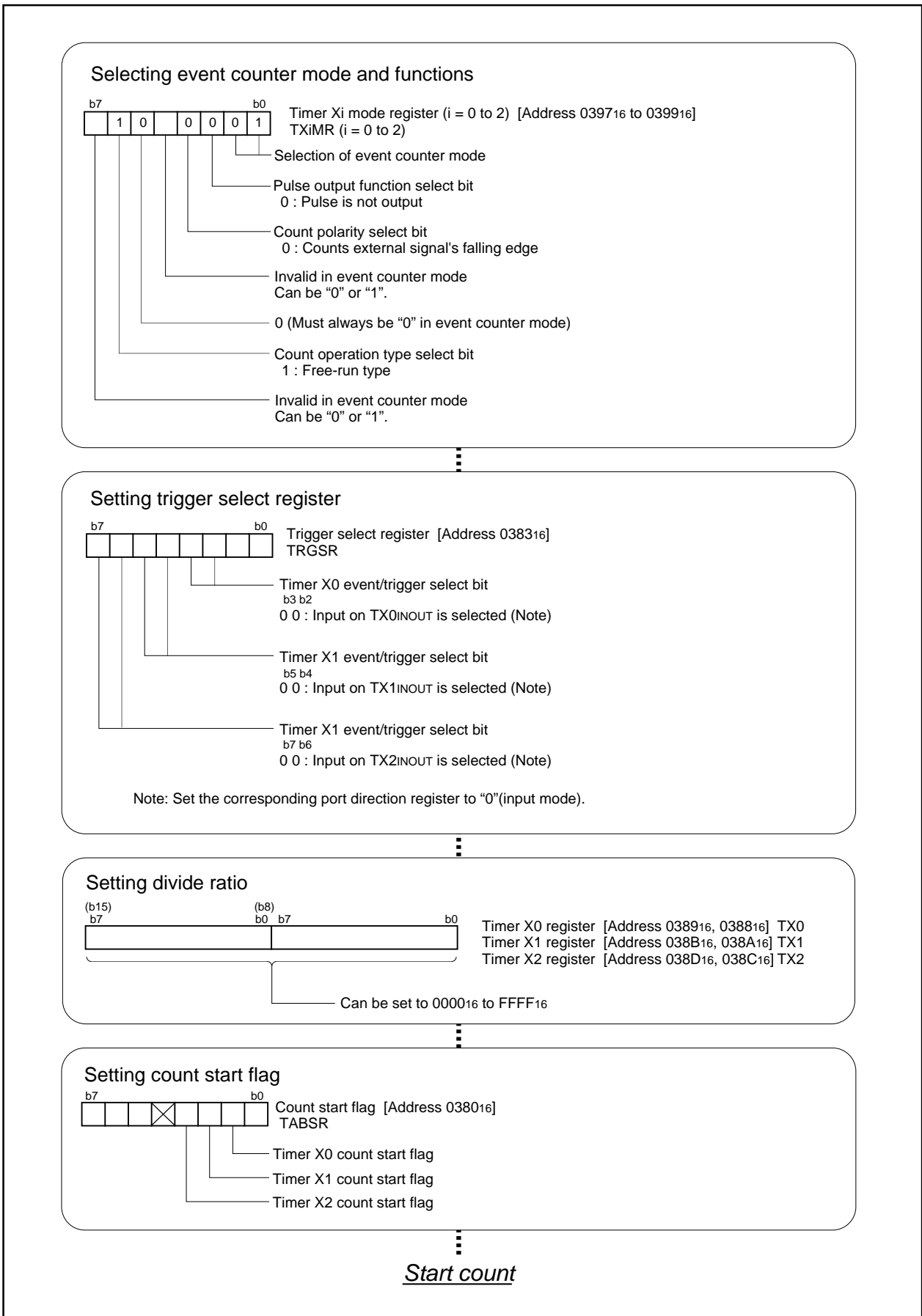


Figure 2.4.13. Set-up procedure of event counter mode, free run type selected

2.4.7 Operation of Timer X (one-shot timer mode)

In one-shot timer mode, choose functions from those listed in Table 2.4.6. Operations of the circled items are described below. Figure 2.4.14 shows the operation timing, and Figure 2.4.15 shows the set-up procedure.

Table 2.4.6. Chosed functions

Item	Set-up	
Count source	○	Internal count source ($f_1 / f_8 / f_{32} / f_{c32}$)
Pulse output function		No pulses output
	○	Pulses output
Count start condition		External trigger input (falling edge of input signal to the TXiINOUT pin)
		External trigger input (rising edge of input signal to the TXiINOUT pin)
		Timer overflow (TB1/TX0/TXi overflow)
	○	Writing "1" to the one-shot start flag

- Operation
- (1) Setting the one-shot start flag to "1" with the count start flag set to "1" causes the counter to perform a down count on the count source. At this time, the TXiINOUT pin outputs an "H" level.
 - (2) The instant the value of the counter becomes "0000₁₆", the TXiINOUT pin outputs an "L" level, and the counter reloads the content of the reload register and stops counting. At this time, the timer Xi interrupt request bit goes to "1".
 - (3) If a trigger occurs while a count is in progress, the counter reloads the value in the reload register again and continues counting. The reload timing is in step with the next count source input after the trigger.
 - (4) Setting the count start flag to "0" causes the counter to stop and to reload the content of the reload register. Also, the TXiINOUT pin outputs an "L" level. At this time, the timer Xi interrupt request bit goes to "1".

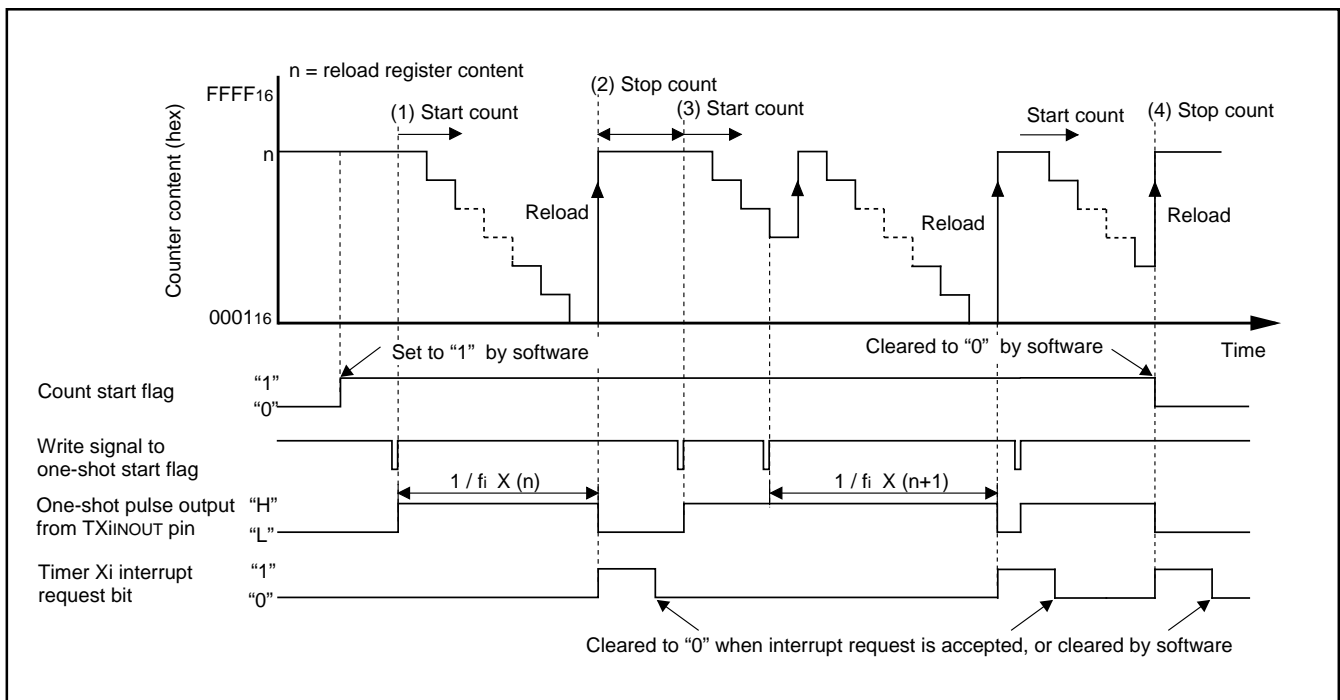


Figure 2.4.14. Operation timing of one-shot mode

Timer X

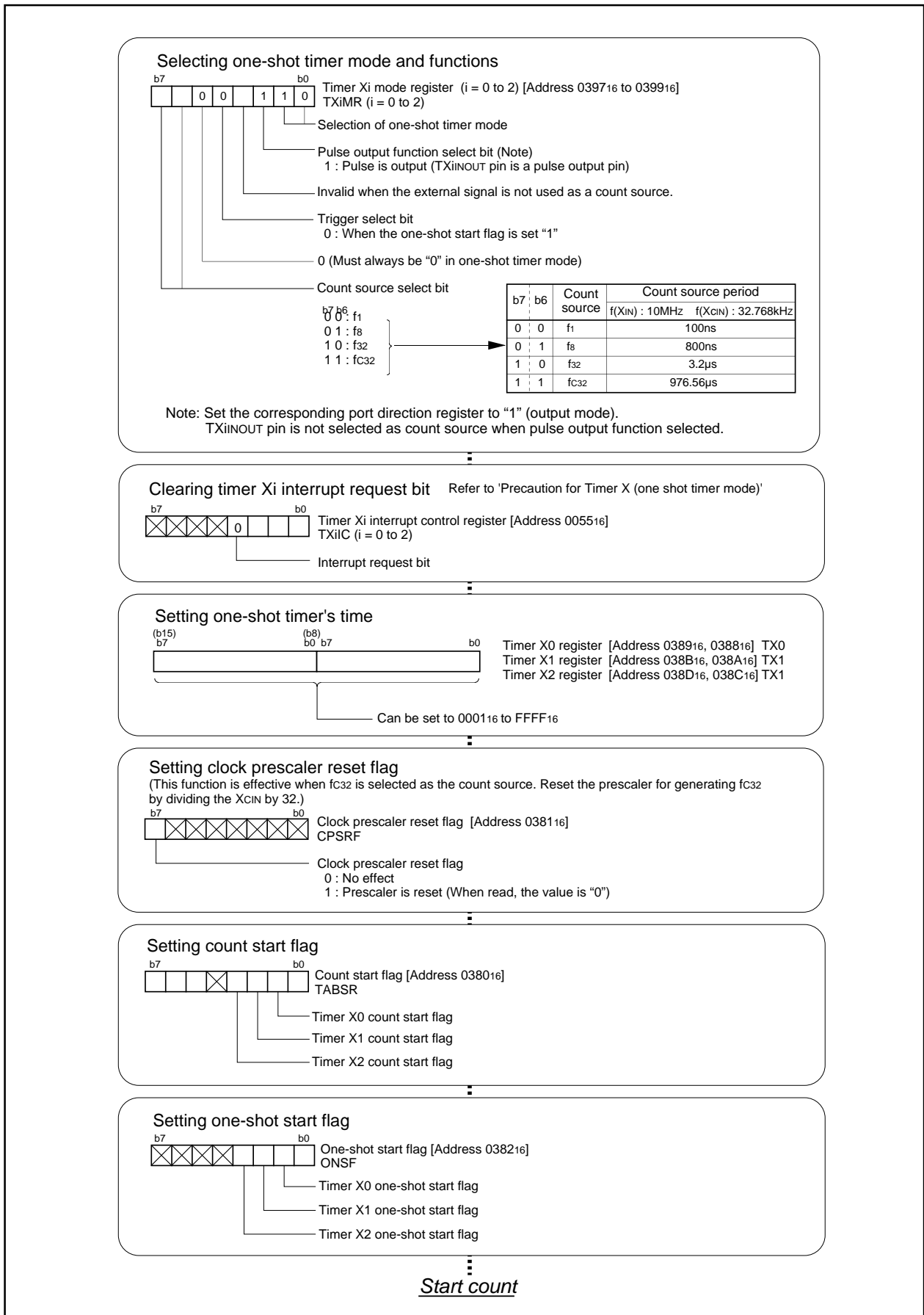


Figure 2.4.15. Set-up procedure of one-shot mode

2.4.8 Operation of Timer X (pulse period measurement mode)

In pulse period/pulse width measurement mode, choose functions from those listed in Table 2.4.7. Operations of the circled items are described below. Figure 2.4.16 shows the operation timing, and Figure 2.4.17 shows the set-up procedure.

Table 2.4.7. Chosed functions

Item	Set-up
Count source	○ Internal count source ($f_1 / f_8 / f_{32} / f_{c32}$)
Measurement mode	○ Pulse period measurement (interval between measurement pulse falling edge to falling edge)
	Pulse period measurement (interval between measurement pulse rising edge to rising edge)
	Pulse width measurement (interval between measurement pulse falling edge to rising edge, and between rising edge to falling edge)

- Operation
- (1) Setting the count start flag to "1" causes the counter to start counting the count source.
 - (2) If a measurement pulse changes from "H" to "L", the value of the counter goes to "0000₁₆", and measurement is started. In this instance, an indeterminate value is transferred to the reload register. The timer Xi interrupt request does not generate.
 - (3) If a measurement pulse changes from "H" to "L" again, the value of the counter is transferred to the reload register, and the timer Xi interrupt request bit goes to "1". Then the value of the counter becomes "0000₁₆", and the measurement is started again.

- Note
- The timer Xi interrupt request bit goes to "1" when an effective edge of a measurement pulse is input or timer Xi is overflowed. The factor of interrupt request can be determined by use of the timer Xi overflow flag within the interrupt routine.
 - The value of the counter at the beginning of a count is indeterminate. Thus there can be instances in which the timer Xi overflow flag goes to "1" immediately after a count is performed.
 - The timer Xi overflow flag goes to "0" if timer Xi mode register is written to when the count start flag is "1". This flag cannot be set to "1" by software.

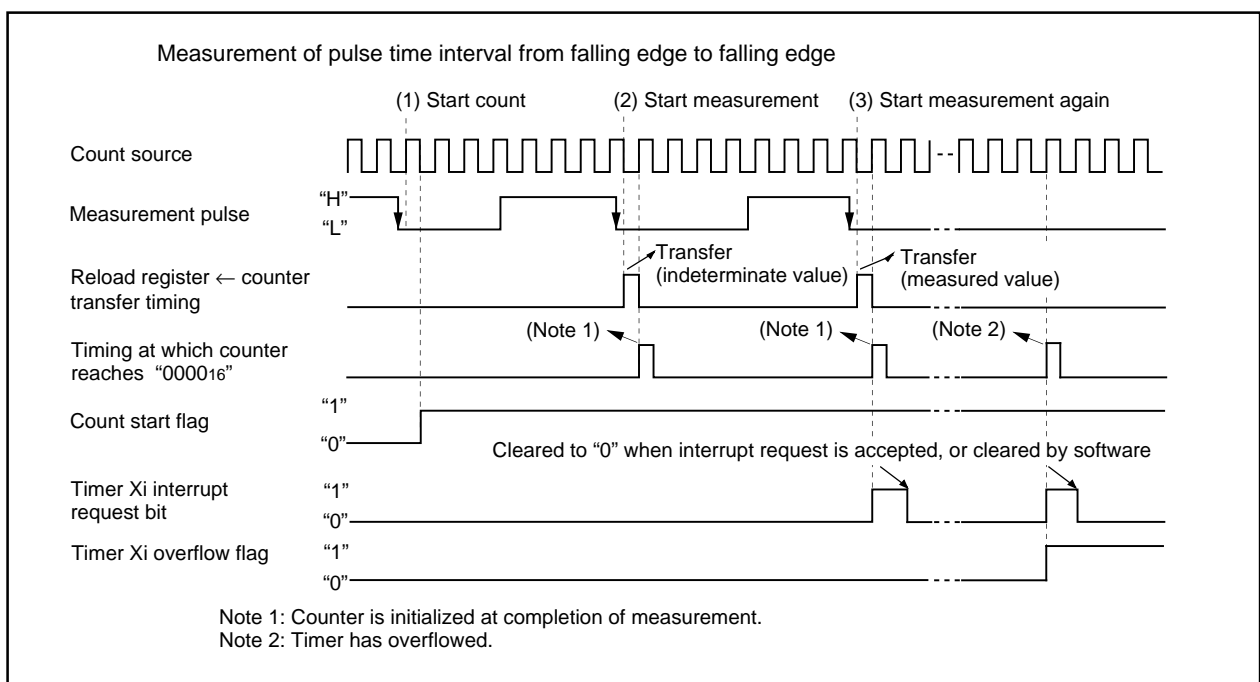
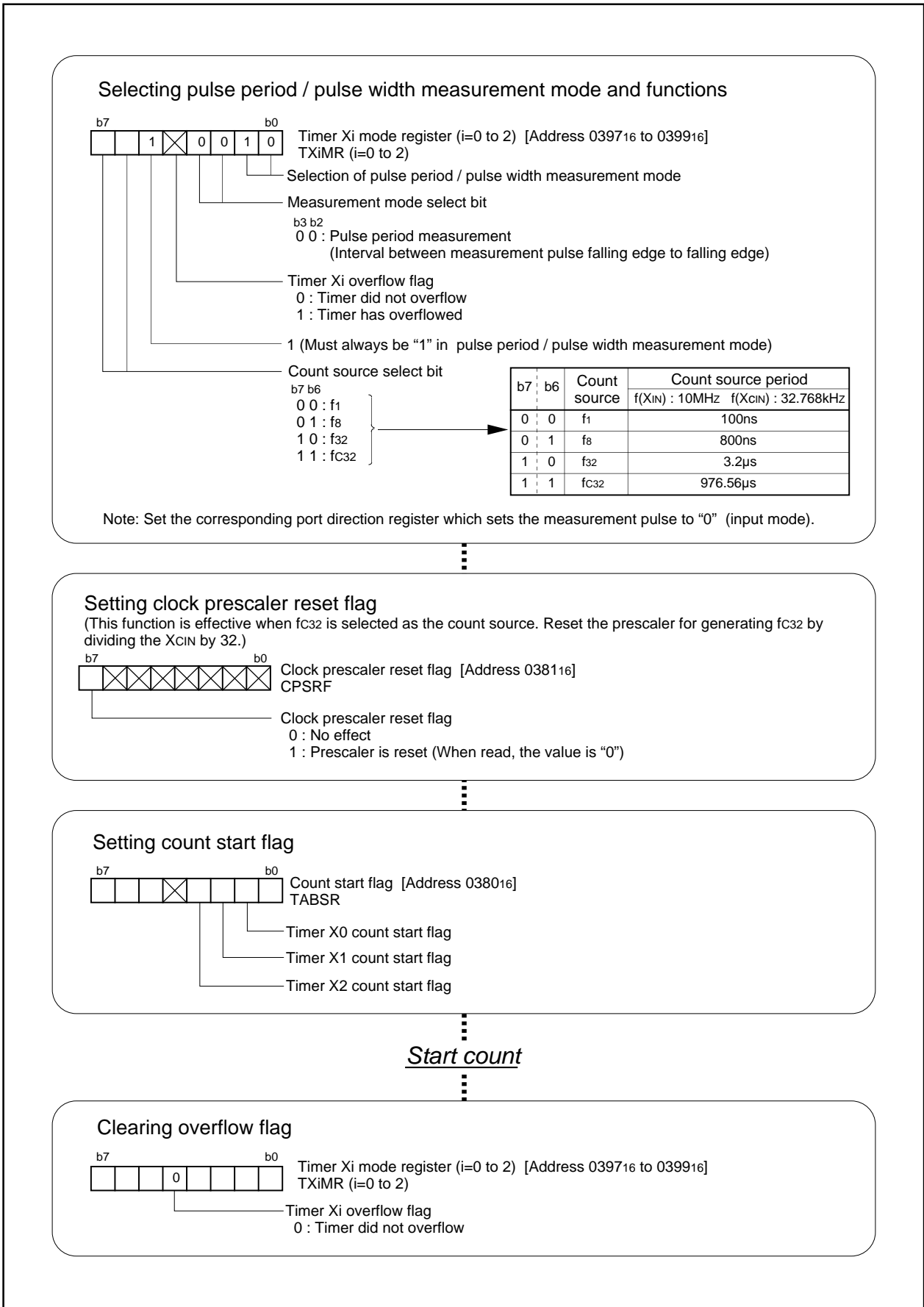


Figure 2.4.16. Operation timing of pulse period measurement mode

Timer X



2.4.9 Operation of Timer X (pulse width measurement mode)

In pulse period/pulse width measurement mode, choose functions from those listed in Table 2.4.8. Operations of the circled items are described below. Figure 2.4.18 shows the operation timing, and Figure 2.4.19 shows the set-up procedure.

Table 2.4.8. Chosed functions

Item	Set-up	
Count source	○	Internal count source ($f_1 / f_8 / f_{32} / f_{c32}$)
Measurement mode		Pulse period measurement (interval between measurement pulse falling edge to falling edge)
		Pulse period measurement (interval between measurement pulse rising edge to rising edge)
	○	Pulse width measurement (interval between measurement pulse falling edge to rising edge, and between rising edge to falling edge)

- Operation
- (1) Setting the count start flag to "1" causes the counter to start counting the count source.
 - (2) If an effective edge of a pulse to be measured is input, the value of the counter goes to "000016", and measurement is started. In this instance, an indeterminate value is transferred to the reload register. The timer Xi interrupt request does not generate.
 - (3) If an effective edge of a pulse to be measured is input again, the value of the counter is transferred to the reload register, and the timer Xi interrupt request bit goes to "1". Then the value of the counter becomes "000016", and measurement is started again.

- Note
- The timer Xi interrupt request bit goes to "1" when an effective edge of a pulse to be measured is input or timer Xi is overflows. The factor of interrupt request can be determined by use of the timer Xi overflow flag within the interrupt routine.
 - The value of the counter at the beginning of a count is indeterminate. Thus there can be instances in which the timer Xi overflow flag goes to "1" immediately after a count is performed.
 - The timer Xi overflow flag goes to "0" if timer Xi mode register is written to when the count start flag is "1". This flag cannot be set to "1" by software.

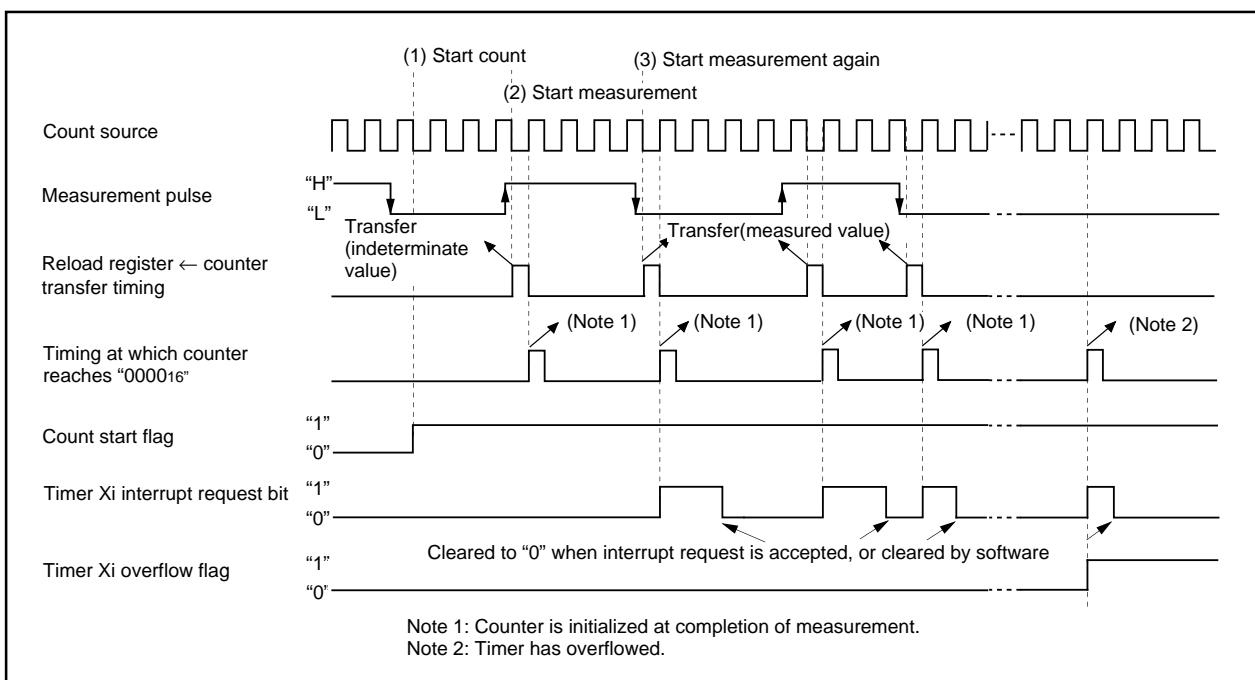
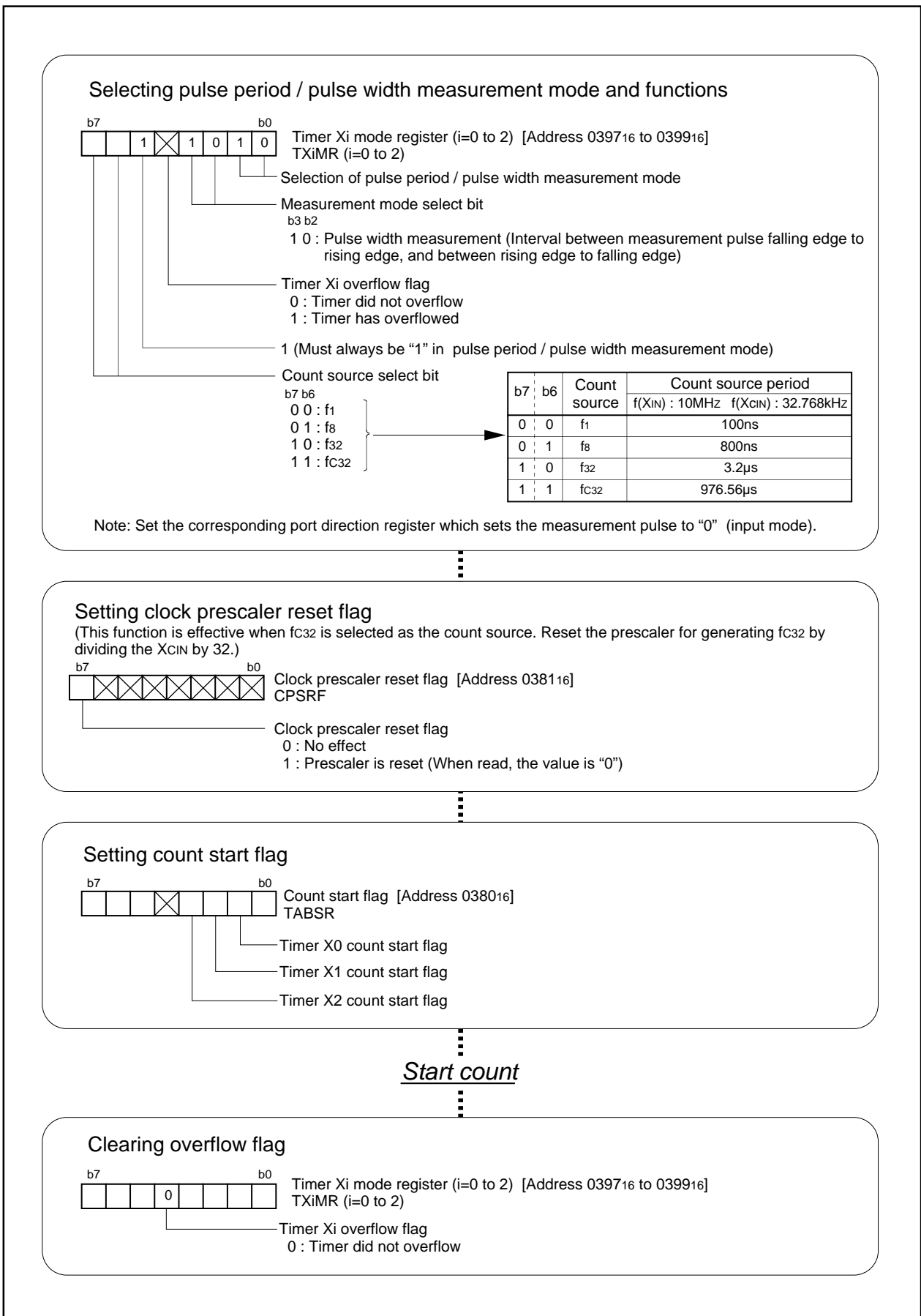


Figure 2.4.18. Operation timing of pulse width measurement mode

Timer X



2.4.10 Operation of Timer X (pulse width modulation mode, 16-bit PWM mode selected)

In pulse width modulation mode, choose functions from those listed in Table 2.4.9. Operations of the circled items are described below. Figure 2.4.20 shows the operation timing, and Figure 2.4.21 shows the set-up procedure.

Table 2.4.9. Chosed functions

Item	Set-up	
Count source	○	Internal count source (f ₁ / f ₈ / f ₃₂ / f _{c32})
PWM mode	○	16-bit PWM
		8-bit PWM
Count start condition	○	Timer overflow (TB1/TA0/TXi overflow)

- Operation
- (1) Selected timer overflow is generated with the count start flag set to "1", the counter performs a down count on the count source. Also, the TXiINOUT pin outputs an "H" level.
 - (2) The TXiINOUT pin output level changes from "H" to "L" when a set time period elapses. At this time, the timer Xi interrupt request bit goes to "1".
 - (3) The counter reloads the content of the reload register every time PWM pulses are output for one cycle, and continues counting.
 - (4) Setting the count start flag to "0" causes the counter to hold its value and to stop. Also, the TXiINOUT outputs an "L" level.

- Note
- PWM pulse cycle is $(2^{16} - 1)/f_i$, whereas "H" level duration is n/f_i . However, when "0000₁₆" is set for the timer A0 register, the PWM output is "L" level for the entire period, and an interrupt request is generated for every PWM output cycle. Also, when "FFFF₁₆" is set for the timer A0 register, the PWM output is "H" level for the entire period, and an interrupt request is generated for every PWM output cycle.
 (f_i: Count source frequency f₁, f₈, f₃₂, f_{c32} n: Timer value)

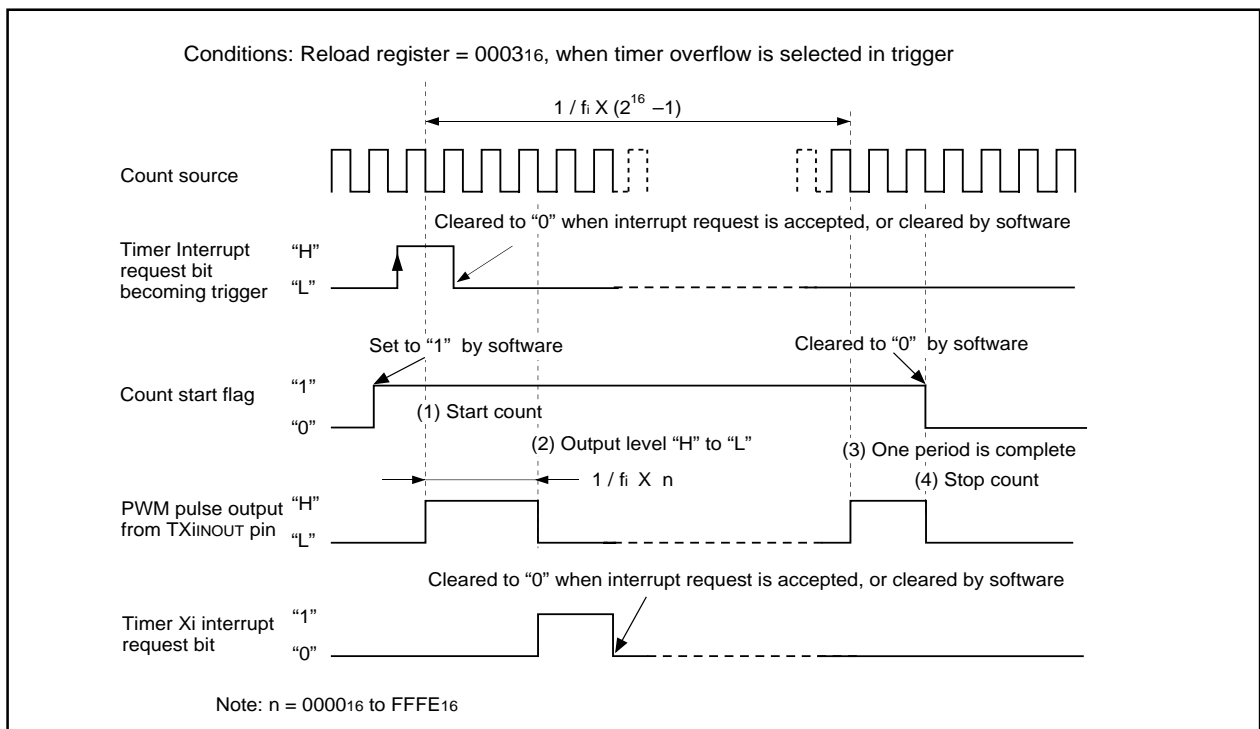


Figure 2.4.20. Operation timing of pulse width modulation mode, 16-bit PWM mode selected

Timer X

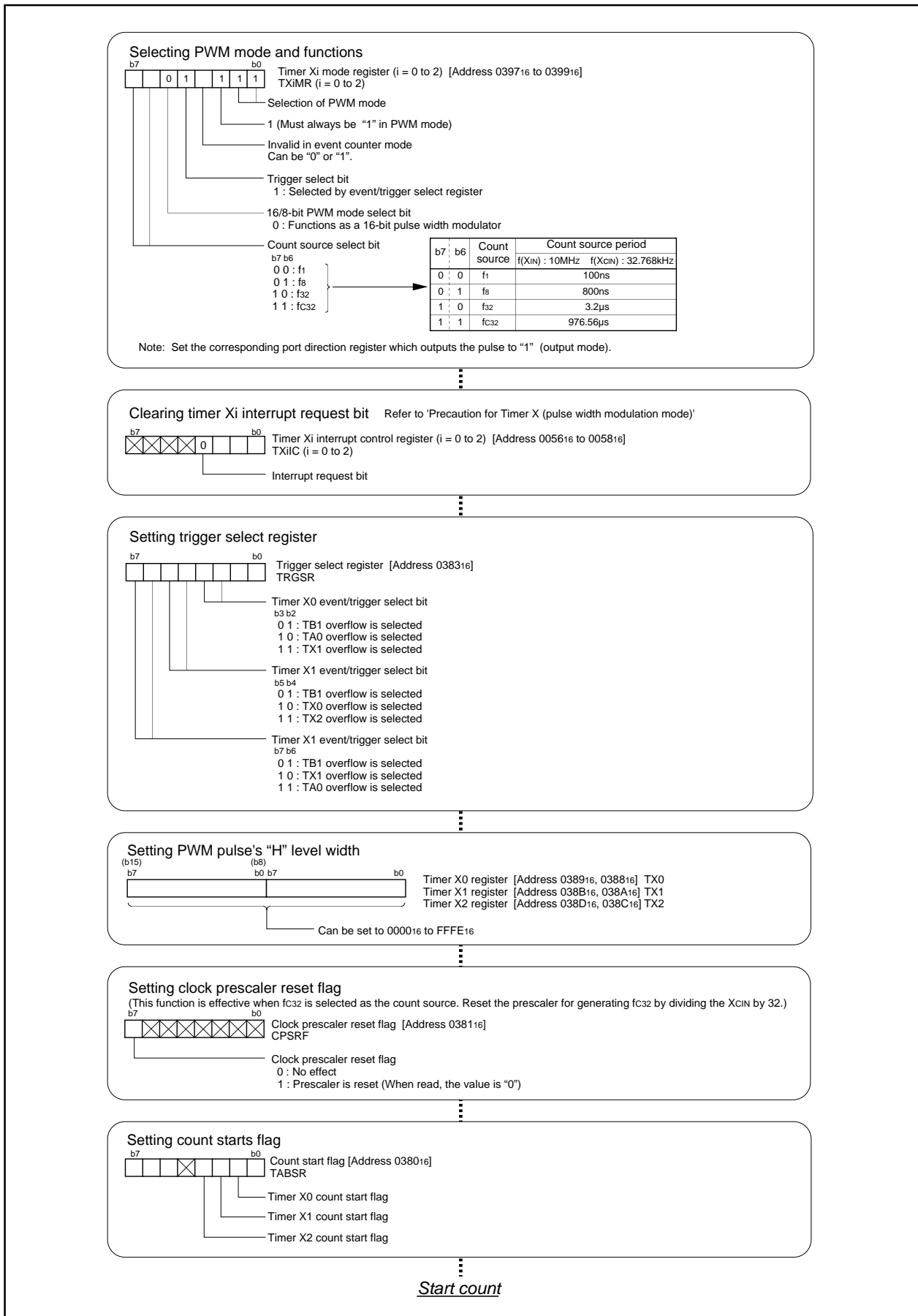


Figure 2.4.21. Set-up procedure of pulse width modulation mode, 16-bit PWM mode selected

2.4.11 Operation of Timer X (pulse width modulation mode, 8-bit PWM mode selected)

In pulse width modulation mode, choose functions from those listed in Table 2.4.10. Operations of the circled items are described below. Figure 2.4.22 shows the operation timing, and Figure 2.4.22 shows the set-up procedure.

Table 2.4.10. Chosed functions

Item	Set-up	
Count source	○	Internal count source ($f_1 / f_8 / f_{32} / f_{c32}$)
PWM mode		16-bit PWM
	○	8-bit PWM
Count start condition	○	Timer overflow (TB1/TA0/TXi overflow)

- Operation
- (1) Selected timer overflow is generated with the count start flag set to "1", the counter performs a down count on the count source. Also, the TXiINOUT pin outputs an "H" level.
 - (2) The TXiINOUT pin output level changes from "H" to "L" when a set time period elapses. At this time, the timer Xi interrupt request bit goes to "1".
 - (3) The counter reloads the content of the reload register every time PWM pulses are output for one cycle, and continues counting.
 - (4) Setting the count start flag to "0" causes the counter to hold its value and to stop. Also, the TXiOUT pin outputs an "L" level.

- Note
- PWM pulse cycle is $(m + 1) \times (2^8 - 1) / f_i$, whereas "H" level duration is $n \times (m + 1) / f_i$. However, when "0016" is set for the significant 8 bits of the timer A0 register, the PWM output is "L" level for the entire period, and an interrupt request is generated for every PWM output cycle. Also, when "FF16" is set for the significant 8 bits of the timer A0 register, the PWM output is "H" level for the entire period, and an interrupt request is generated for every PWM output cycle. (f_i : Count source frequency $f_1, f_8, f_{32}, f_{c32}$ n : Timer value)

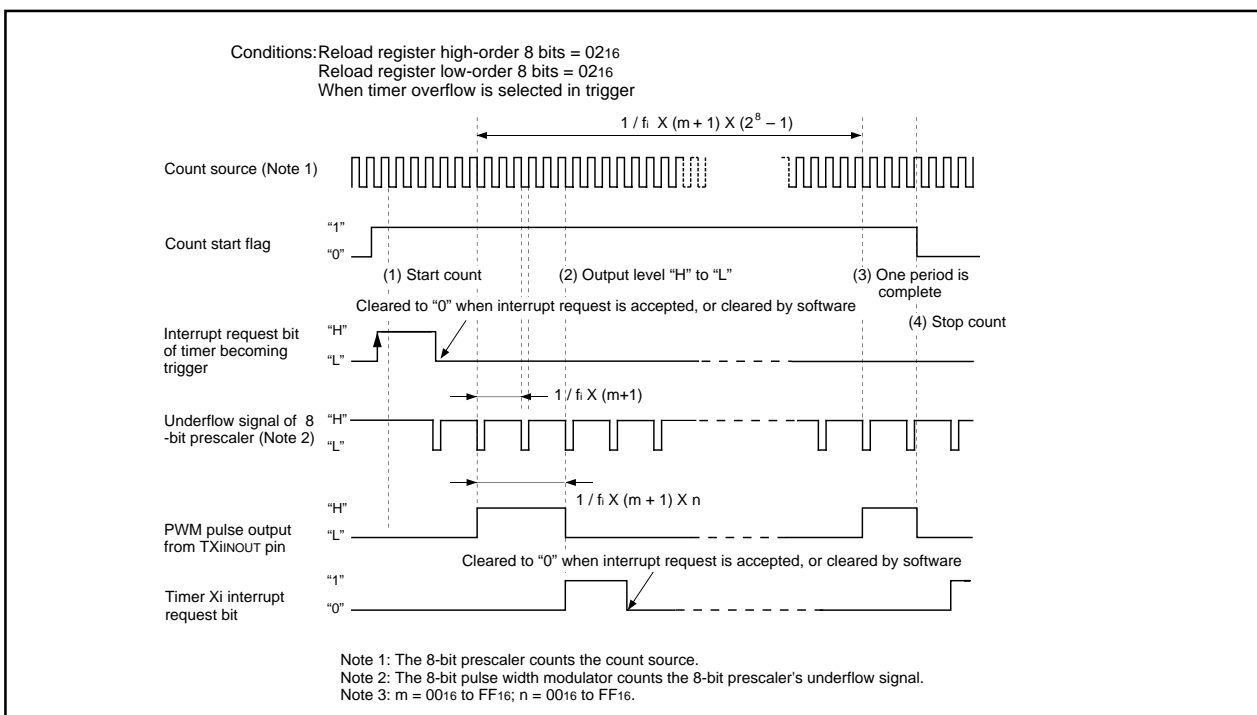


Figure 2.4.22. Operation timing of pulse width modulation mode, with 8-bit PWM mode selected

Timer X

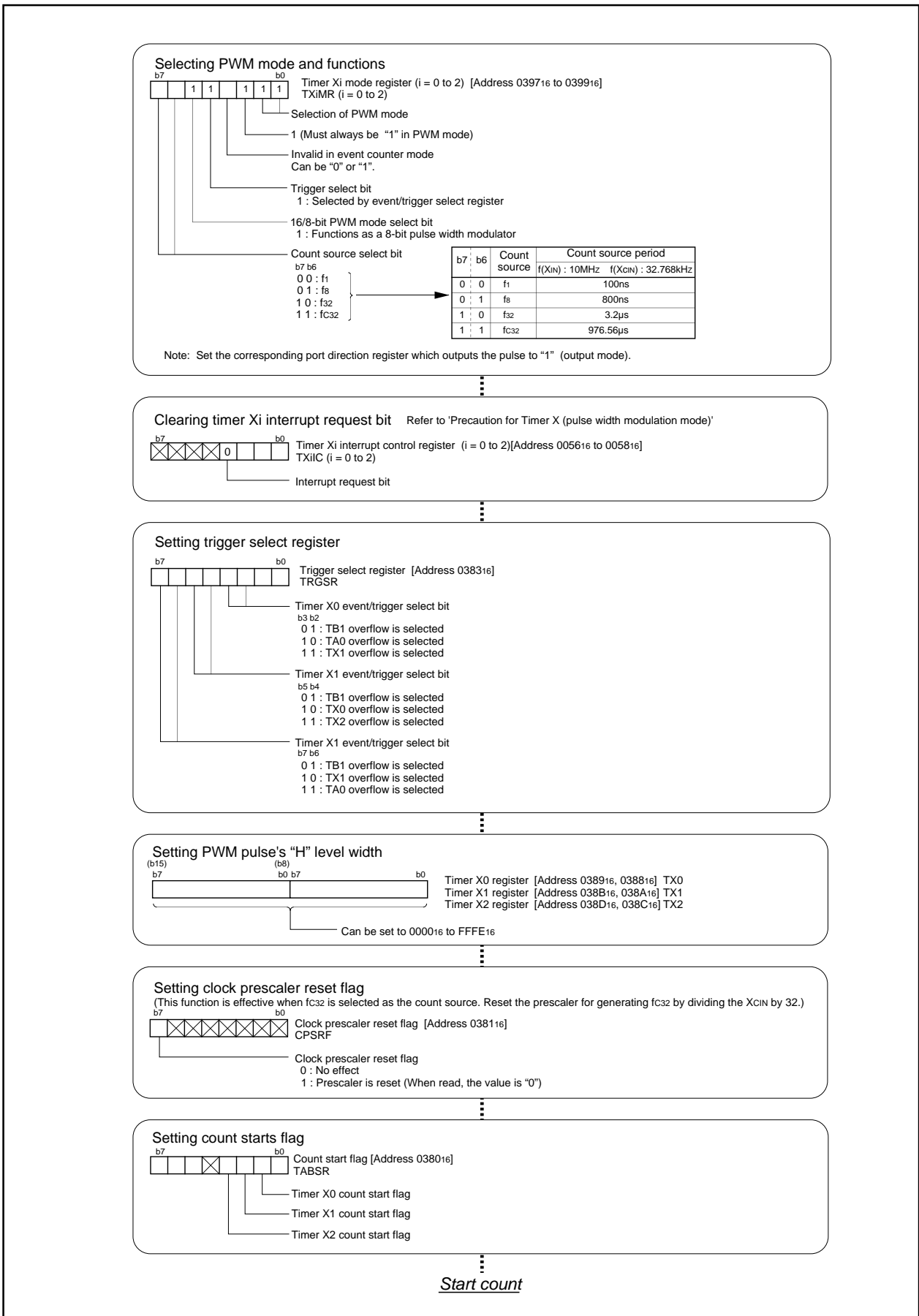


Figure 2.4.23. Set-up procedure of pulse width modulation mode, 8-bit PWM mode selected

Timer X

2.4.12 Precautions for Timer X (timer mode, event counter mode)

- (1) To clear reset, the count start flag is set to "0". Set a value in the timer Xi register, then set the flag to "1".
- (2) Reading the timer Xi register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the timer Xi register with the reload timing shown in Figure 2.4.24 gets "FFFF₁₆". Reading the timer Xi register after setting a value in the timer Xi register with a count halted but before the counter starts counting gets a proper value.

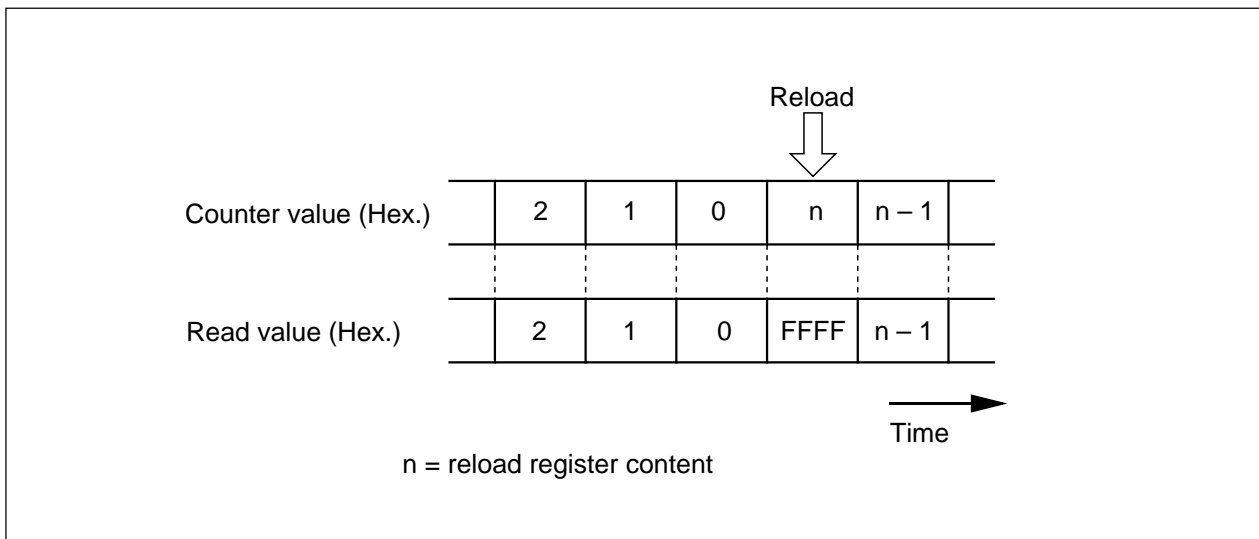


Figure 2.4.24. Reading timer Xi register

2.4.13 Precautions for Timer X (one-shot timer mode)

- (1) To clear reset, the count start flag is set to "0". Set a value in the timer Xi register, then set the flag to "1".

- (2) Setting the count start flag to "0" while a count is in progress causes as follows:
 - The counter stops counting and a content of reload register is reloaded.
 - The TXiINOUT pin outputs "L" level.
 - The interrupt request generated and the timer Xi interrupt request bit goes to "1".

- (3) The timer Xi interrupt request bit goes to "1" if the timer's operation mode is set using any of the following procedures:
 - Selecting one-shot timer mode after reset.
 - Changing operation mode from timer mode to one-shot timer mode.
 - Changing operation mode from event counter mode to one-shot timer mode.Therefore, to use timer Xi interrupt (interrupt request bit), set timer Xi interrupt request bit to "0" after the above listed changes have been made.

- (4) If a trigger occurs while a count is in progress, after the counter performs one down count following the reoccurrence of a trigger, the reload register contents are reloaded, and the count continues. To generate a trigger while a count is in progress, generate the second trigger after an elapse longer than one cycle of the timer's count source after the previous trigger occurred.

2.4.14 Precautions for Timer X (pulse period/pulse width measurement mode)

- (1) The timer Xi interrupt request bit goes to "1" when an effective edge of a measurement pulse is input or timer Xi is overflowed. The factor of interrupt request can be determined by use of the timer Xi overflow flag within the interrupt routine.
- (2) If the timer overflow occurs simultaneously with the input of a measurement pulse, and if the interrupt factor cannot be determined from the timer Xi overflow flag, connect the timers and count the number of overflows.
- (3) When reset, the timer Xi overflow flag goes to "1". This flag cannot be set to "0" by writing to the timer Xi mode register when the count start flag is "1".
- (4) Use the timer Xi interrupt request bit to detect only overflows. Use the timer Xi overflow flag only to determine the interrupt factor within the interrupt routine.
- (5) When the first effective edge is input after a count is started, an indeterminate value is transferred to the reload register. At this time, timer Xi interrupt request is not generated.
- (6) The value of the counter is indeterminate at the beginning of a count. Therefore the timer Xi overflow flag may go to "1" immediately after a count is started.
- (7) If changing the measurement mode select bit is set after a count is started, the timer Xi interrupt request bit goes to "1".
- (8) If the input signal to the TXiINOUT pin is affected by noise, precise measurement may not be performed in some cases. It is recommended to see that measurements fall within a specific range by use of software.
- (9) For pulse width measurement, pulse widths are successively measured. Use software to check whether the measurement result is an "H" level width or an "L" level width.

2.4.15 Precautions for Timer X (pulse width modulation mode)

- (1) To clear reset, the count start flag is set to "0". Set a value in the timer Xi register, then set the flag to "1".
- (2) The timer Xi interrupt request bit becomes "1" if setting operation mode of the timer in compliance with any of the following procedures:
 - Selecting PWM mode after reset.
 - Changing operation mode from timer mode to PWM mode.
 - Changing operation mode from event counter mode to PWM mode.
 Therefore, to use timer Xi interrupt (interrupt request bit), set timer Xi interrupt request bit to "0" after the above listed changes have been made.
- (3) Setting the count start flag to "0" while PWM pulses are being output causes the counter to stop counting. If the TXiINOUT pin is outputting an "H" level in this instance, the output level goes to "L", and the timer Xi interrupt request bit goes to "1". If the TXiINOUT pin is outputting an "L" level in this instance, the level does not change, and the timer Xi interrupt request bit does not become "1".
- (4) Normal PWM output is restored according to the interrupt request generate timing, both in the case of 16-bit PWM and 8-bit PWM, when PWM output is either "H" or "L" level for the entire period. This holds only when a value other than "0000₁₆" or "FFFF₁₆" is set during 16-bit PWM, or a value other than "00₁₆" or "FF₁₆" is set during 8-bit PWM.

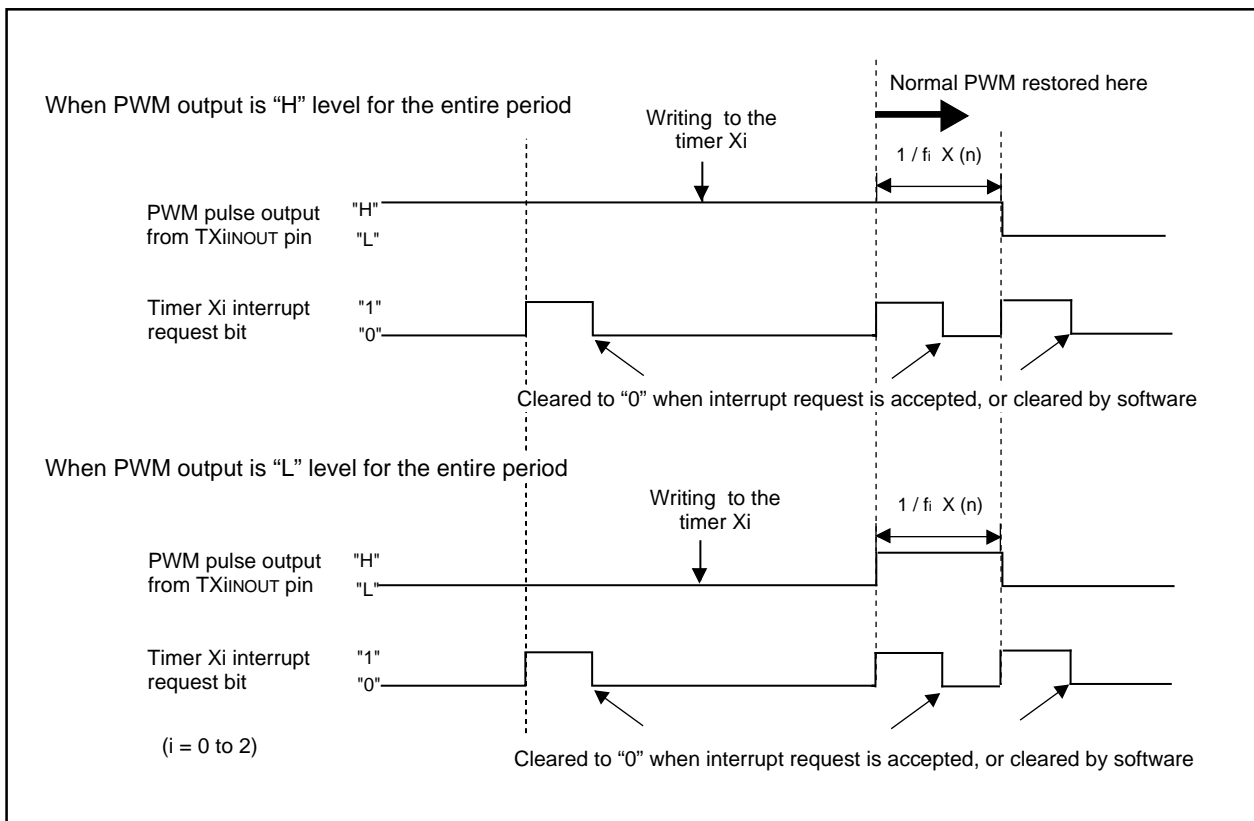


Figure 2.4.25. Operation timing of PWM output mode

2.5 Clock-Synchronous Serial I/O

2.5.1 Overview

Clock-synchronous serial I/O carries out 8-bit data communications in synchronization with the clock. The following is an overview of the clock-synchronous serial I/O.

(1) Transmission/reception format

8-bit data

(2) Transfer rate

If the internal clock is selected as the transfer clock, the divide-by-2 frequency, resulting from the bit rate generator division, becomes the transfer rate. The bit rate generator count source can be selected from the following: f1, f8, f32, and fc. Clocks f1, f8 and f32 are derived by dividing the CPU's main clock by 1, 8, and 32 respectively. Clock fc is derived by dividing the CPU's sub clock by 1 respectively.

Furthermore, if an external clock is selected as the transfer clock, the clock frequency input to the CLK pin becomes the transfer rate.

(3) Error detection

Only overrun error can be detected. Overrun error is an error that occurs when the next data is made ready before the reception buffer register is read.

(4) How to deal with an error

When receiving data, read an error flag and reception data simultaneously to determine which error has occurred. If the data read is erroneous, initialize the error flag and the UART0 receive buffer register, then receive the data again.

To initialize the UART0 receive buffer register

1. Set the receive enable bit to "0" (disable reception).
2. Set the serial I/O mode select bit to "0002" (invalid serial I/O).
3. Set the serial I/O mode select bit.
4. Set the receive enable bit to "1" again (enable reception).

To transmit data again due to an error on the reception side when external clock is selected, clear the UART0 transmit buffer register, then transmit the data again.

To clear the UART0 transmit buffer register

1. Set the port P52 (CLK0 pin) direction register to "0" (input mode).
2. Set the port P50 (TxD0 pin) direction register to "0" (input mode).
3. Set the internal/external clock select bit to "0" (internal clock).
4. Checking completion of transmission (no data present in transmit register).
5. Set the internal/external clock select bit to "1" (external clock).
6. Set the port P50 (TxD0 pin) direction register to "1" (output mode), then set transmission data in the UART0 transmit buffer register.

Clock-Synchronous Serial I/O

(5) Function selection

For clock-synchronous serial I/O, the following functions can be selected:

(a) Function for choosing polarity

This function switches the polarity of the transfer clock. The following operations are available:

- Data is input at the falling edge of the transfer clock, and is output at the rising edge.
- Data is input at the rising edge of the transfer clock, and is output at the falling edge.

(b) Function for choosing which bit to transmit first

This function is to choose whether to transmit data from bit 0 or from bit 7. Choose either of the following:

- LSB first Data is transmitted from bit 0.
- MSB first Data is transmitted from bit 7.

(c) Function for choosing successive reception mode

Successive reception mode is a mode in which reading the receive buffer register makes the reception-enabled status ready. In this mode, there is no need to write dummy data to the transmit buffer register so as to make the reception-enabled status ready. But at the time of starting reception, read the receive buffer register into a dummy manner.

- Normal mode Writing dummy data to the transmit buffer register makes the reception enabled status ready.
- Successive reception mode Reading the reception buffer register makes the reception-enabled status ready.

(d) Function for outputting transfer clock to multiple pins

This function is to switch among pins to output the transfer clock. This function is effective only when selecting the internal clock. Switching among pins for outputting the transfer clock allows data transmission to two external ICs in a time-sharing manner.

(e) Function for choosing a transmission interrupt factor

The timing to generate a transmission interrupt can be selected from the following: the instant the transmission buffer is emptied or the instant the transmission register is emptied. When transmission buffer empty timing is selected, an interrupt occurs when transmitted data is moved from the transmission buffer to the transmission register. Therefore, data can be transmitted in succession. When transmission register empty timing is selected, an interrupt occurs when data transmission is complete.

Following are some examples in which various functions (a) through (e) are selected:

- Transmission Operation WITH: transmission at falling edge of transfer clock, LSB First, interrupt at instant transmission buffer is emptied; WITHOUT transfer clock output to multiple pins function ... P254
- Transmission Operation WITH: transmission at falling edge of transfer clock, LSB First, interrupt at instant transmission is completed; WITH transfer clock output to multiple pins function (UART0 selection available) P258
- Reception WITH: reception at falling edge of transfer clock, LSB First, successive reception mode disabled; WITHOUT transfer clock output to multiple pins function P262

Clock-Synchronous Serial I/O

(6) Input/output to the serial I/O and the direction register

To input an external signal to the serial I/O, set the direction register of the relevant port to input. To output signal from the serial I/O, set the direction register of the relevant port to output.

(7) Pins related to the serial I/O

- CLK0 pin Input/output pins for the transfer clock
- RxD0, RxD1 pins Input pins for data
- TxD0, TxD1 pins Output pins for data (Since TxD2 pin is N-channel open drain, this pin needs pull-up resistor.)
- CLKS pin Output pin for transfer clock. Can be used as transfer clock output pin in the transfer clock output to multiple pins function.

Note : UART1 cannot be used in clock-synchronous serial I/O mode.

(8) Registers related to the serial I/O

Figure 2.5.1 shows the memory map of serial I/O-related registers, and Figures 2.5.2 to 2.5.4 show serial I/O-related registers.

0051 ₁₆	UART0 transmit interrupt control register (S0TIC)
0052 ₁₆	UART0 receive interrupt control register (S0RIC)
0053 ₁₆	UART1 transmit interrupt control register (S1TIC)
0054 ₁₆	UART1 receive interrupt control register (S1RIC)
~	
03A0 ₁₆	UART0 transmit/receive mode register (U0MR)
03A1 ₁₆	UART0 bit rate generator (U0BRG)
03A2 ₁₆	UART0 transmit buffer register (U0TB)
03A3 ₁₆	
03A4 ₁₆	UART0 transmit/receive control register 0 (U0C0)
03A5 ₁₆	UART0 transmit/receive control register 1 (U0C1)
03A6 ₁₆	UART0 receive buffer register (U0RB)
03A7 ₁₆	
03A8 ₁₆	UART1 transmit/receive mode register (U1MR)
03A9 ₁₆	UART1 bit rate generator (U1BRG)
03AA ₁₆	UART1 transmit buffer register (U1TB)
03AB ₁₆	
03AC ₁₆	UART1 transmit/receive control register 0 (U1C0)
03AD ₁₆	UART1 transmit/receive control register 1 (U1C1)
03AE ₁₆	UART1 receive buffer register (U1RB)
03AF ₁₆	
03B0 ₁₆	UART transmit/receive control register 2 (UCON)
03B1 ₁₆	

Figure 2.5.1. Memory map of serial I/O-related registers

Clock-Synchronous Serial I/O

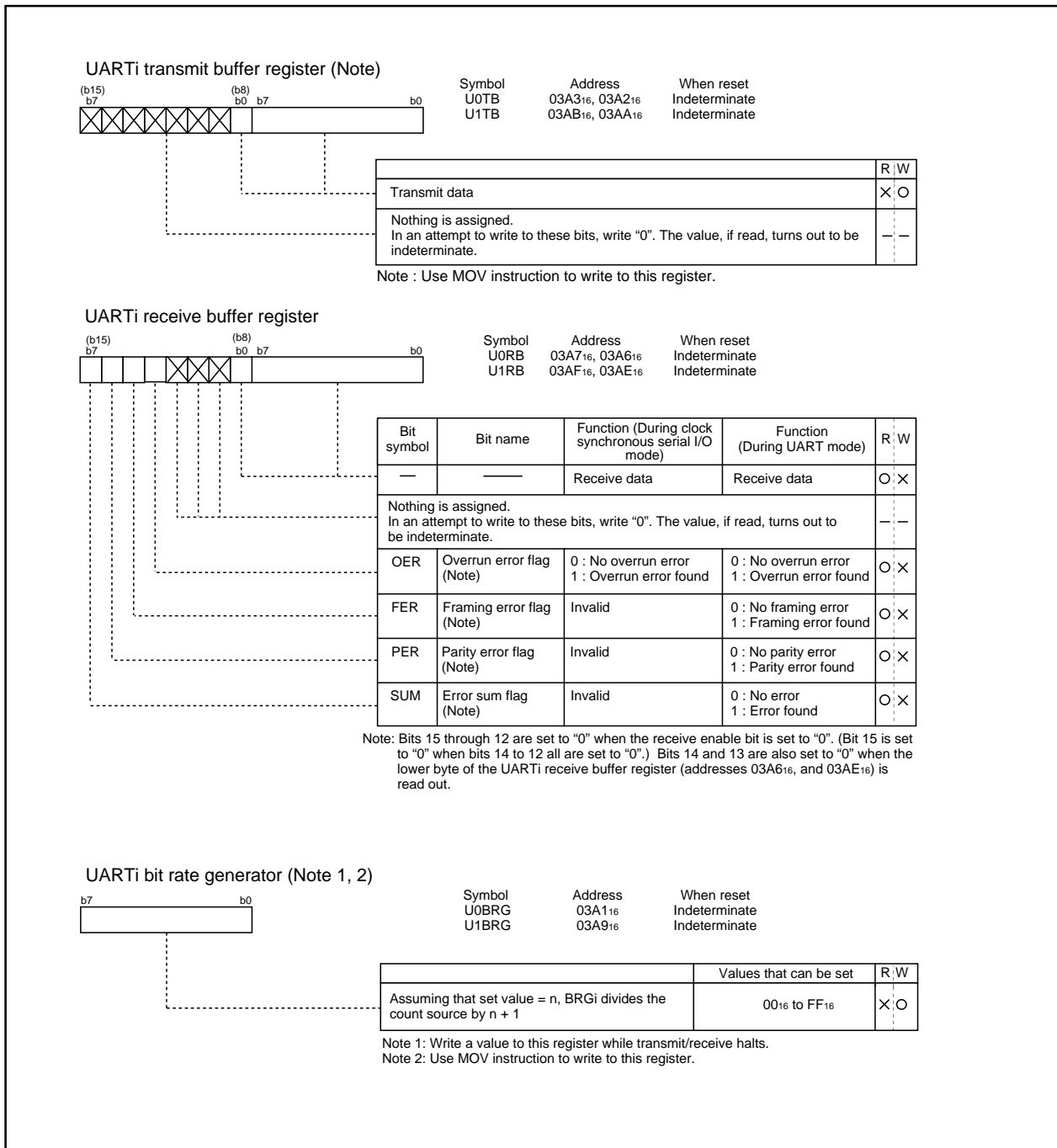


Figure 2.5.2. Serial I/O-related registers (1)

Clock-Synchronous Serial I/O

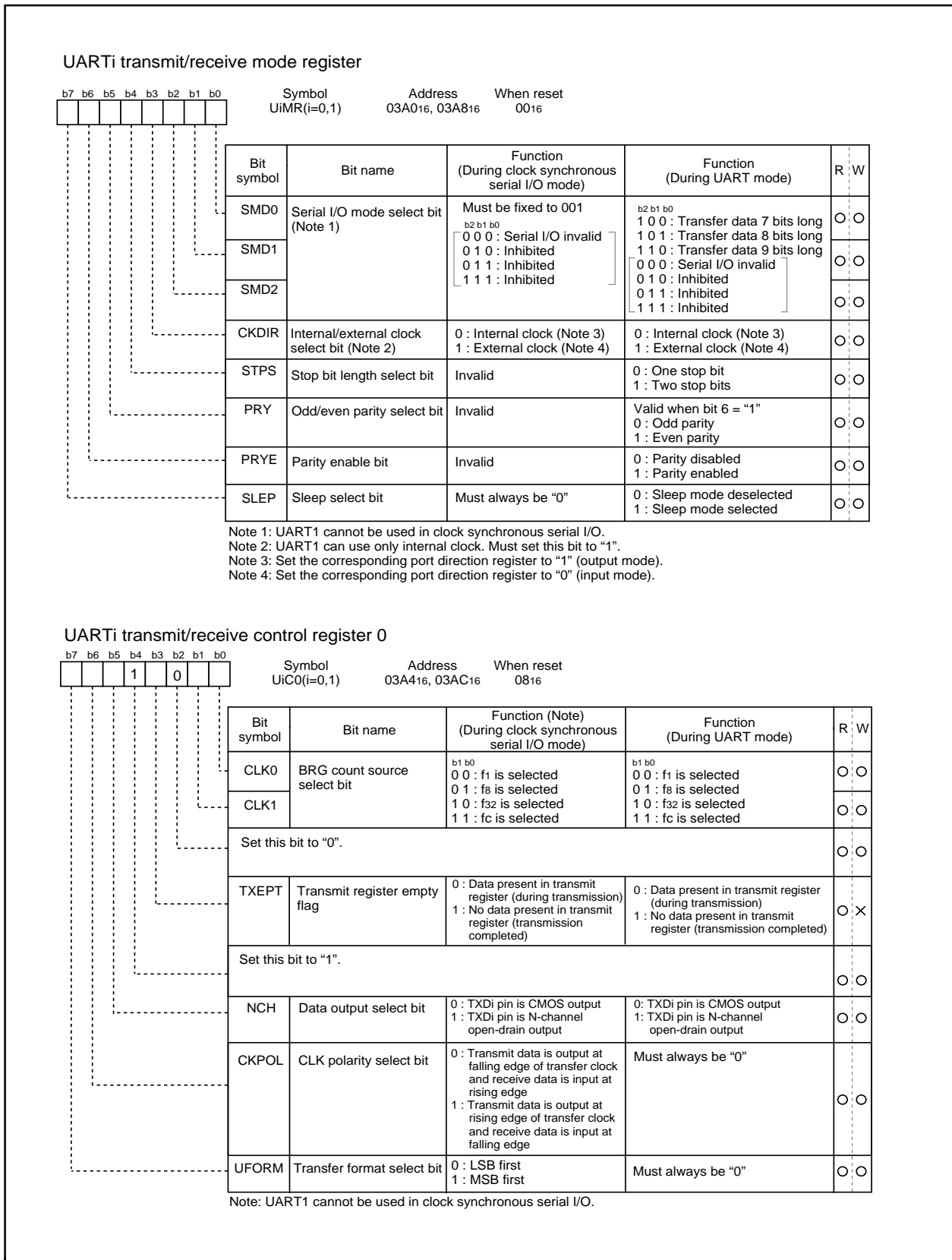


Figure 2.5.3. Serial I/O-related registers (2)

Clock-Synchronous Serial I/O

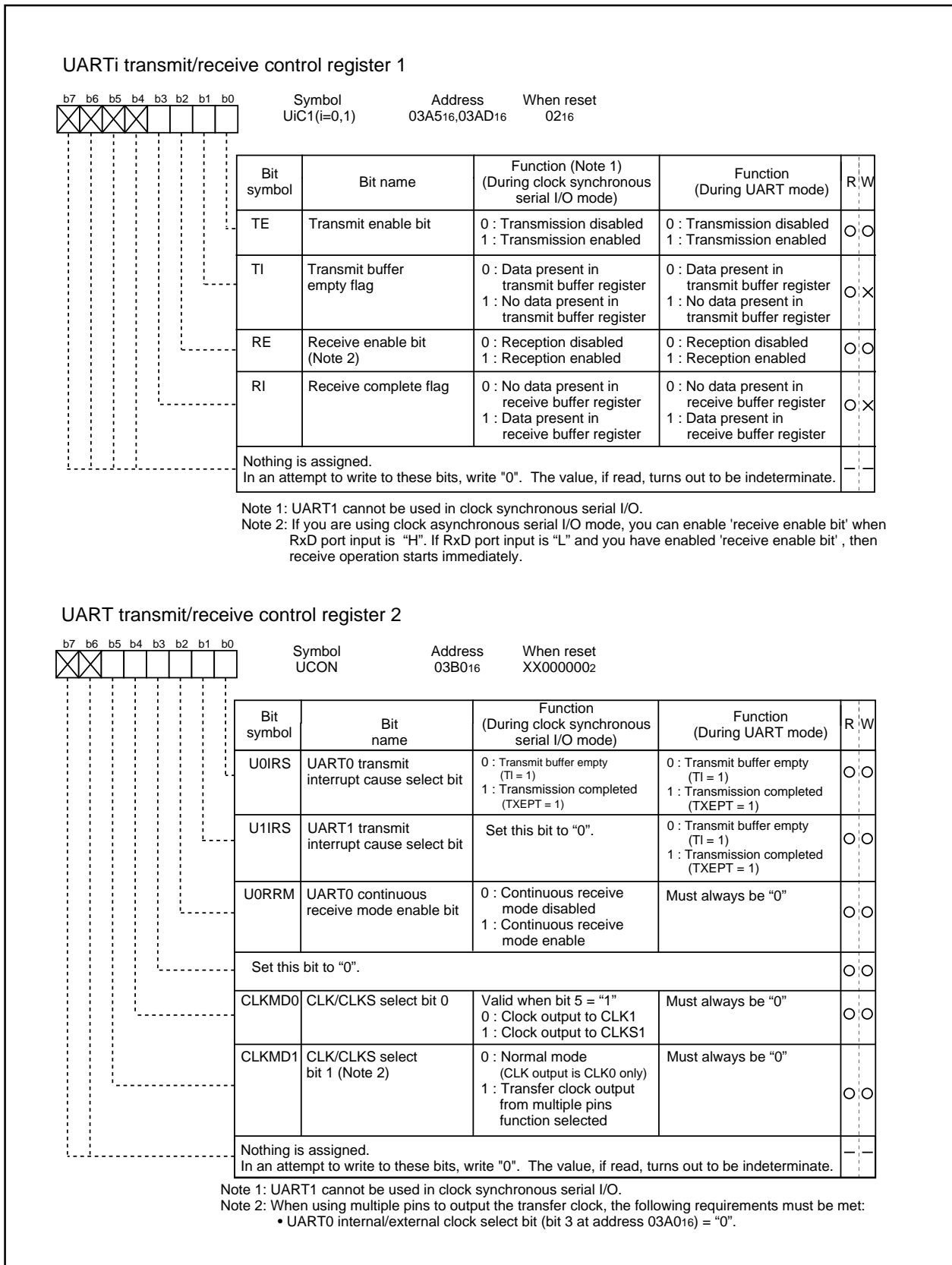


Figure 2.5.4. Serial I/O-related registers (3)

2.5.2 Operation of Serial I/O (transmission in clock-synchronous serial I/O mode)

In transmitting data in clock-synchronous serial I/O mode, choose functions from those listed in Table 2.5.1. Operations of the circled items are described below. Figure 2.5.5 shows the operation timing, and Figures 2.5.6 and 2.5.7 show the set-up procedures.

Table 2.5.1. Chosed functions

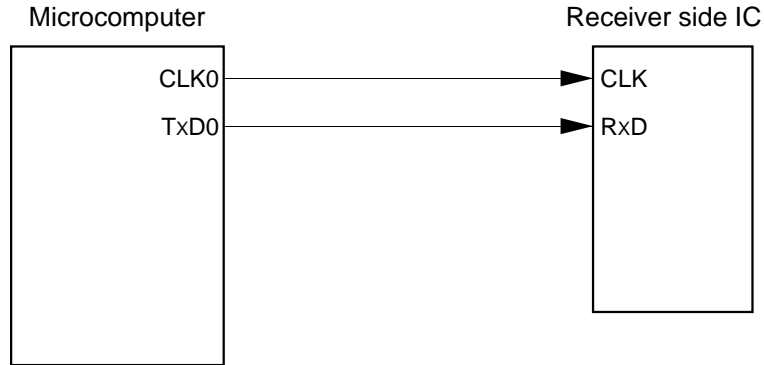
Item	Set-up	
Transfer clock source	<input type="radio"/>	Internal clock ($f_1 / f_8 / f_{32} / f_c$)
	<input type="radio"/>	External clock (CLK0 pin)
CLK polarity	<input type="radio"/>	Output transmission data at the falling edge of the transfer clock
	<input type="radio"/>	Output transmission data at the rising edge of the transfer clock
Transfer clock	<input type="radio"/>	LSB first
	<input type="radio"/>	MSB first
Transmission interrupt factor	<input type="radio"/>	Transmission buffer empty
	<input type="radio"/>	Transmission complete
Output transfer clock to multiple pins (Note)	<input type="radio"/>	Not selected
	<input type="radio"/>	Selected

Note: This can be selected only when UART0 is used in combination with the internal clock.

- Operation
- (1) Setting the transmit enable bit to "1" and writing transmission data to the UART0 transmit buffer register makes data transmissible status ready.
 - (2) In synchronization with the first falling edge of the transfer clock, transmission data held in the UART0 transmit buffer register is transmitted to the UART0 transmit register. At this time, the UART0 transmit interrupt request bit goes to "1". Also, the first bit of the transmission data is transmitted from the TxD0 pin. Then the data is transmitted bit by bit from the lower order in synchronization with the falling edges.
 - (3) When transmission of 1-byte data is completed, the transmit register empty flag goes to "1", which indicates that transmission is completed. The transfer clock stops at "H" level.
 - (4) If the next transmission data is set in the UART0 transmit buffer register while transmission is in progress (before the eighth bit has been transmitted), the data is transmitted in succession.

Clock-Synchronous Serial I/O

Example of wiring



Example of operation

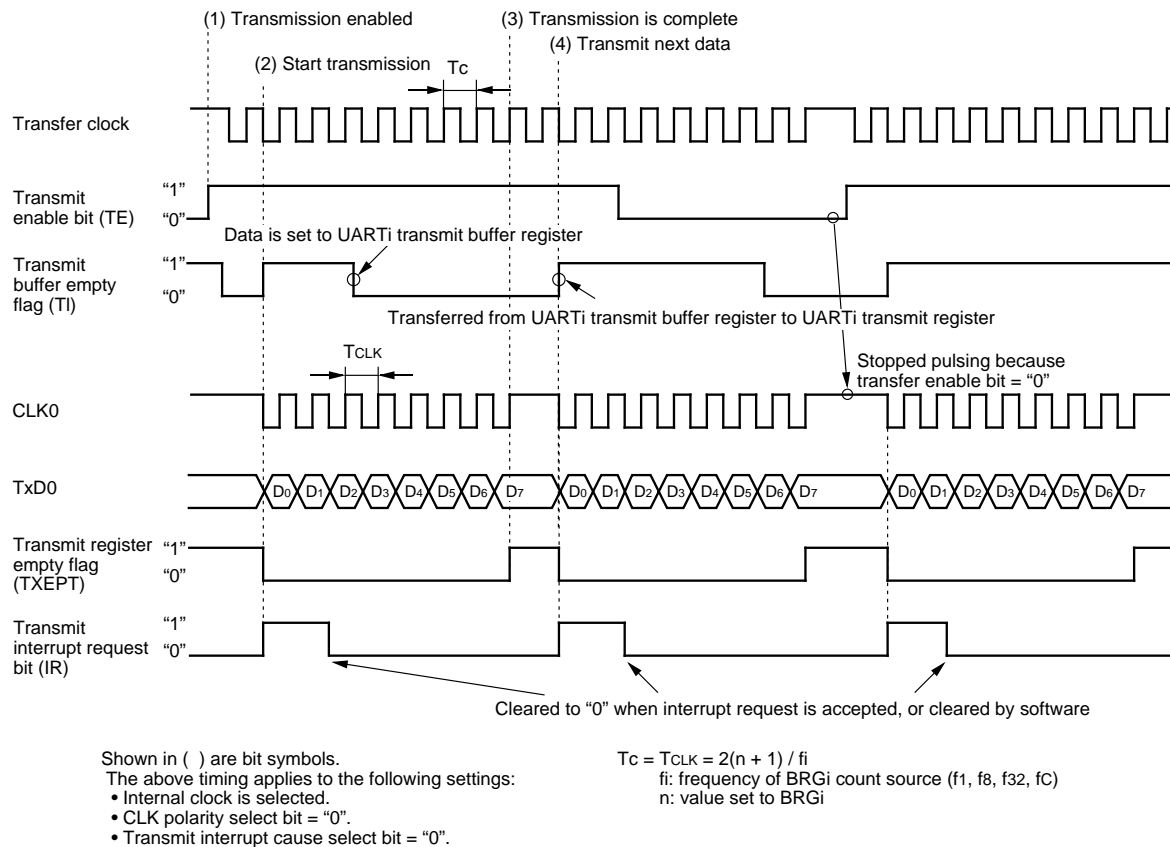


Figure 2.5.5. Operation timing of transmission in clock-synchronous serial I/O mode

Clock-Synchronous Serial I/O

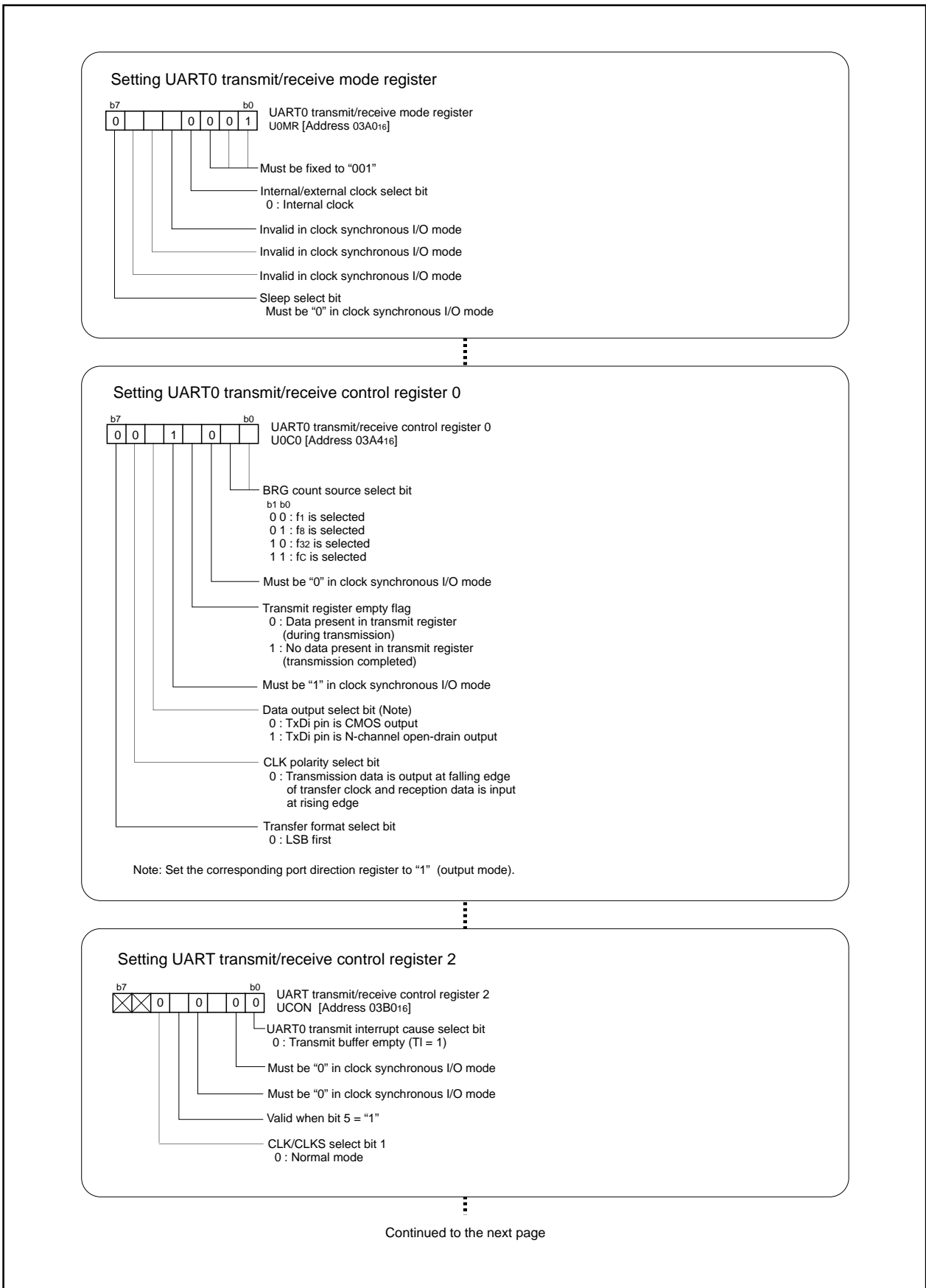


Figure 2.5.6. Set-up procedure of transmission in clock-synchronous serial I/O mode (1)

Clock-Synchronous Serial I/O

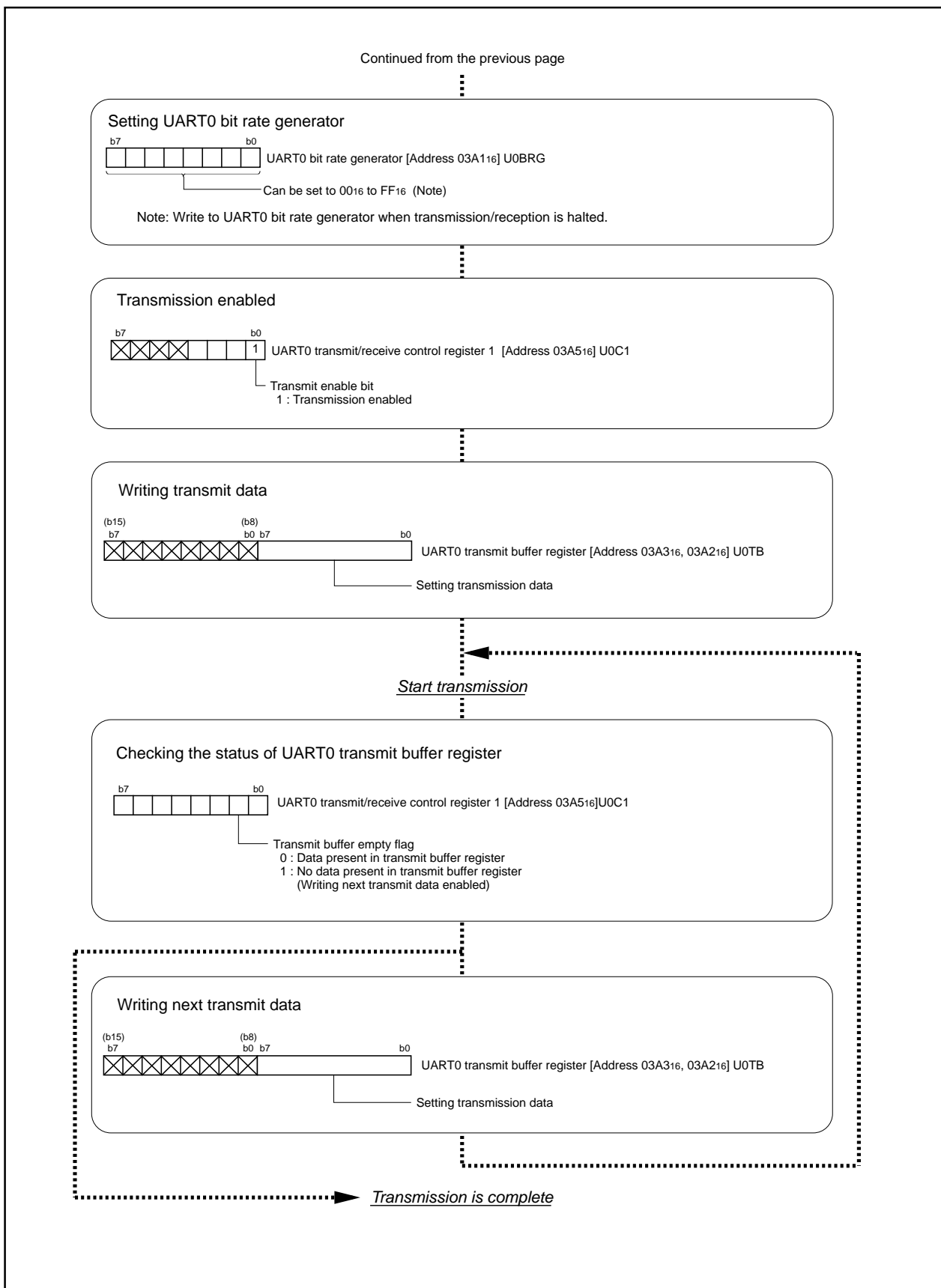


Figure 2.5.7. Set-up procedure of transmission in clock-synchronous serial I/O mode (2)

2.5.3 Operation of the Serial I/O (transmission in clock-synchronous serial I/O mode, transfer clock output from multiple pins function selected)

In transmitting data in clock-synchronous serial I/O mode, choose functions from those listed in Table 2.5.2. Operations of the circled items are described below. Figure 2.5.8 shows the operation timing, and Figures 2.5.9 and 2.5.10 show the set-up procedures.

Table 2.5.2. Chosed functions

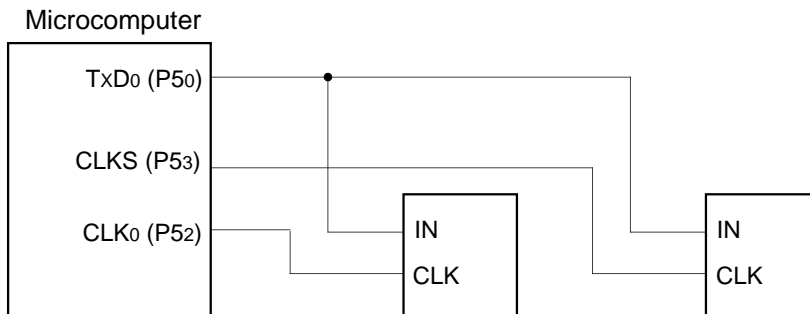
Item	Set-up	
Transfer clock source	<input type="radio"/>	Internal clock ($f_1 / f_8 / f_{32} / f_c$)
	<input type="radio"/>	External clock (CLK0 pin)
CLK polarity	<input type="radio"/>	Output transmission data at the falling edge of the transfer clock
	<input type="radio"/>	Output transmission data at the rising edge of the transfer clock
Transfer clock	<input type="radio"/>	LSB first
	<input type="radio"/>	MSB first
Transmission interrupt factor	<input type="radio"/>	Transmission buffer empty
	<input type="radio"/>	Transmission complete
Output transfer clock to multiple pins (Note)	<input type="radio"/>	Not selected
	<input type="radio"/>	Selected

Note: This can be selected only when UART0 is used in combination with the internal clock.

- Operation
- (1) Setting the transmit enable bit to "1" makes data transmissible status ready.
 - (2) When transmission data is written to the UART0 transmit buffer register, transmission data held in the UART0 transmit buffer register is transmitted to the UART0 transmit register in synchronization with the first falling edge of the transfer clock. At this time, the first bit of the transmission data is transmitted from the TxDo pin. Then the data is transmitted bit by bit from the lower order in synchronization with the falling edges of the transfer clock.
 - (3) When transmission of 1-byte data is completed, the transmit register empty flag goes to "1", which indicates that the transmission is completed. The transfer clock stops at "H" level. At this time, the UART0 transmit interrupt request bit goes to "1".
 - (4) Setting CLK/CLKS select bit 1 to "1" and setting CLK/CLKS select bit 0 to "1" causes the CLKS pin to go to the transfer clock output pin. Change the transfer clock output pin when transmission is halted.

Clock-Synchronous Serial I/O

Example of wiring



Note: This applies when performing only transmission with an internal clock selected in the clock synchronous serial I/O mode.

Example of operation

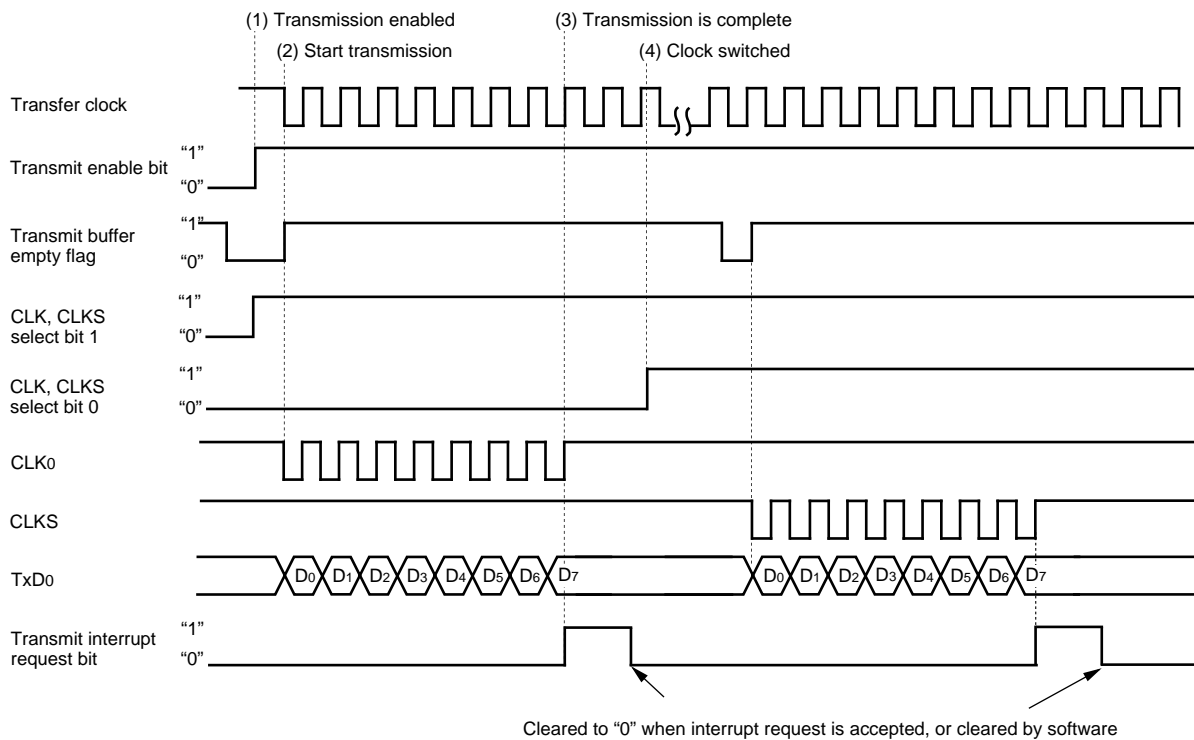


Figure 2.5.8. Operation timing of transmission in clock-synchronous serial I/O mode, transfer clock output from multiple pins function selected

Clock-Synchronous Serial I/O

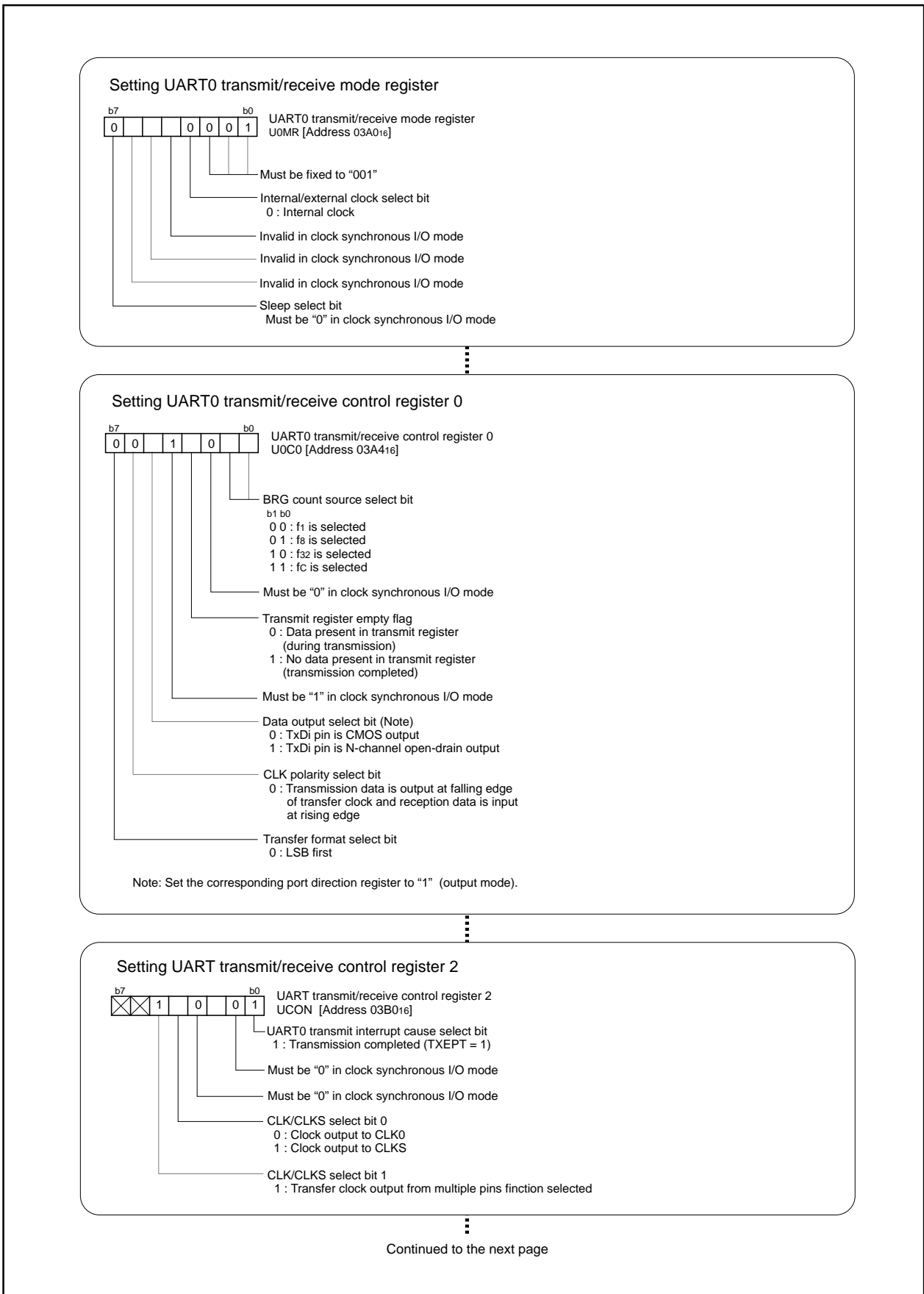


Figure 2.5.9. Set-up procedure of transmission in clock-synchronous serial I/O mode, transfer clock output from multiple pins function selected (1)

Clock-Synchronous Serial I/O

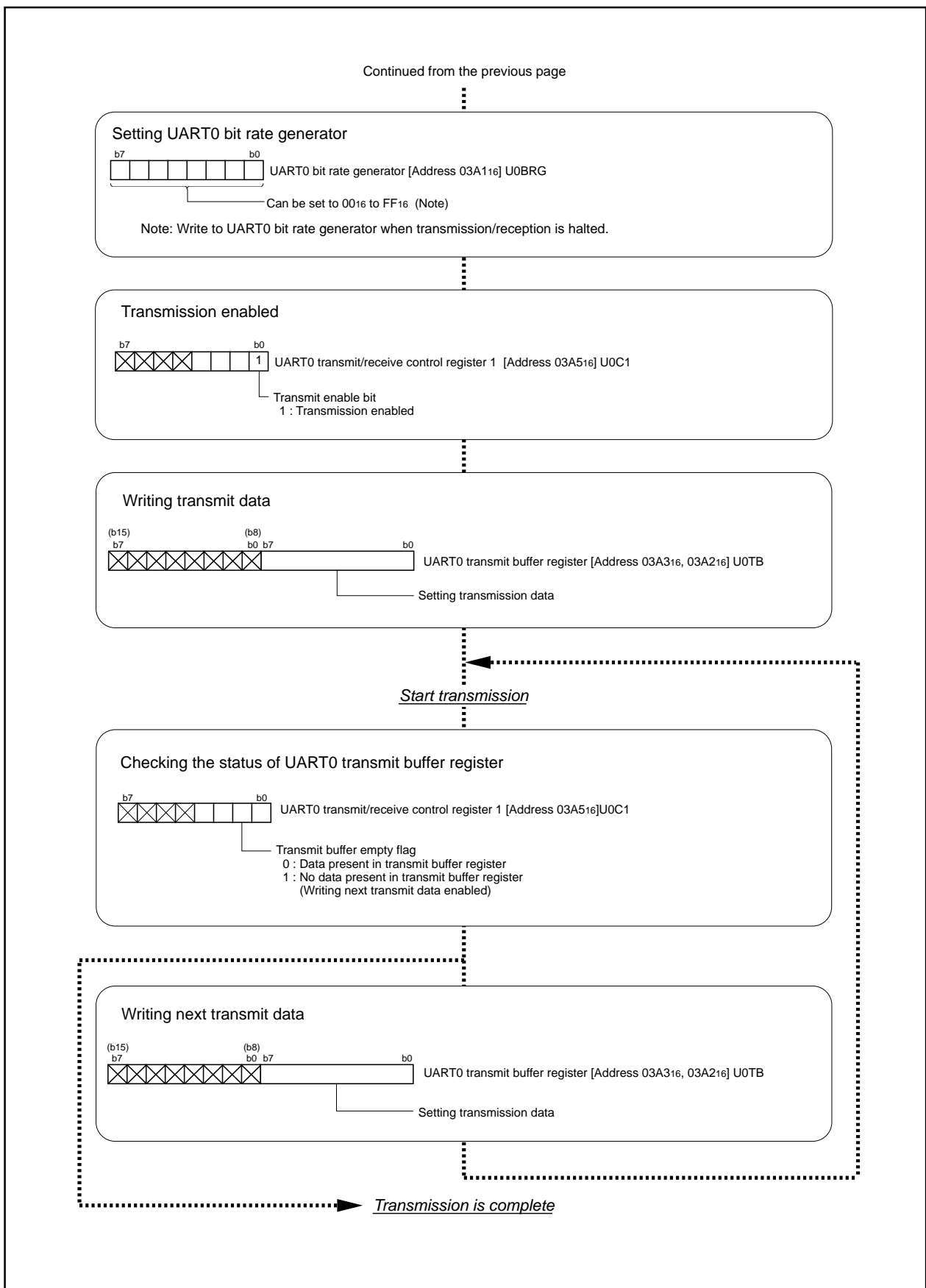


Figure 2.5.10. Set-up procedure of transmission in clock-synchronous serial I/O mode, transfer clock output from multiple pins function selected (2)

2.5.4 Operation of Serial I/O (reception in clock-synchronous serial I/O mode)

In receiving data in clock-synchronous serial I/O mode, choose functions from those listed in Table 2.5.3. Operations of the circled items are described below. Figure 2.5.11 shows the operation timing, and Figures 2.5.12 and 2.5.13 show the set-up procedures.

Table 2.5.3. Chosed functions

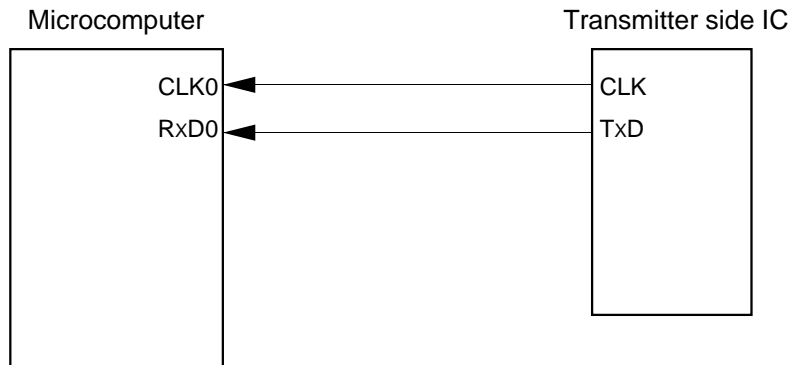
Item	Set-up	
Transfer clock source		Internal clock ($f_1 / f_8 / f_{32} / f_c$)
	<input type="radio"/>	External clock (CLK0 pin)
CLK polarity	<input type="radio"/>	Output transmission data at the falling edge of the transfer clock
		Output transmission data at the rising edge of the transfer clock
Transfer clock	<input type="radio"/>	LSB first
		MSB first
Continuous receive mode	<input type="radio"/>	Disabled
		Enabled
Output transfer clock to multiple pins (Note)	<input type="radio"/>	Not selected
		Selected

Note: This can be selected only when UART0 is used in combination with the internal clock.

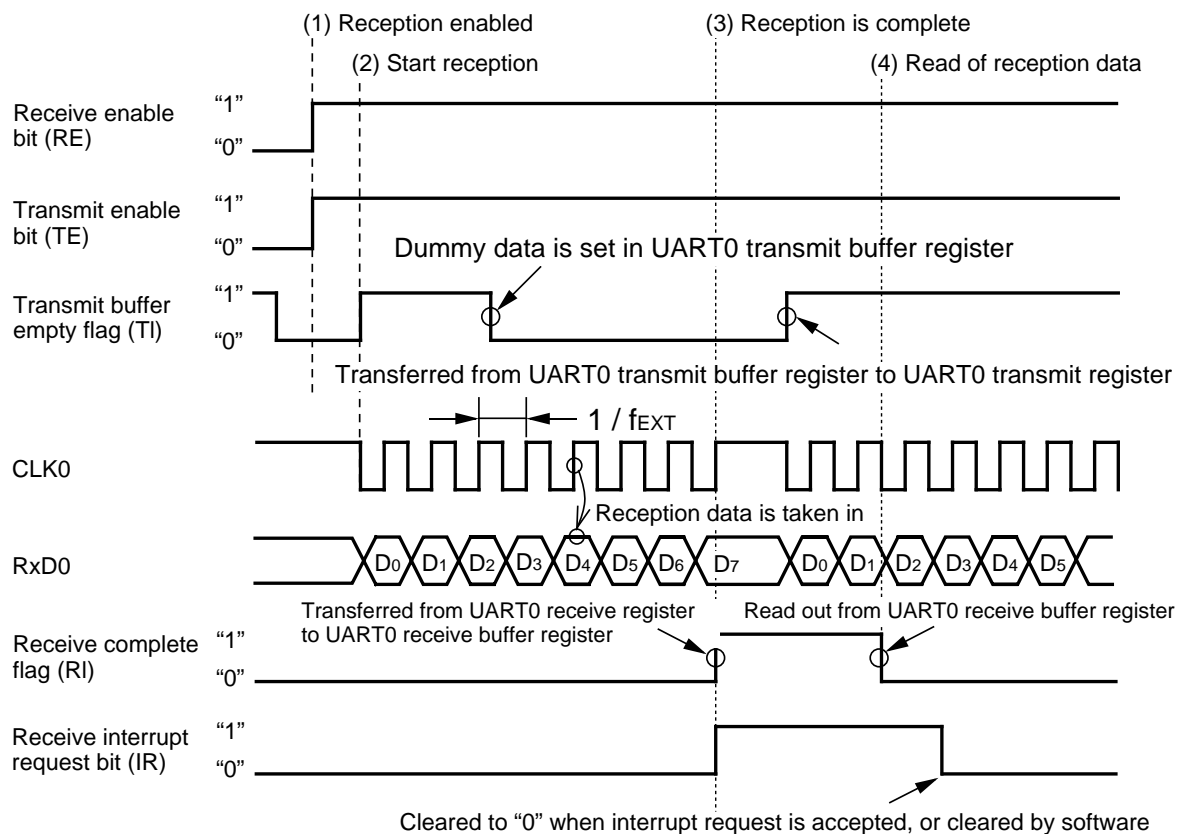
- Operation
- (1) Writing dummy data to the UART0 transmit buffer register, setting the receive enable bit to "1", and the transmit enable bit to "1", makes the data receivable status ready.
 - (2) In synchronization with the first rising edge of the transfer clock, the input signal to the RxD0 pin is stored in the highest bit of the UART0 receive register. Then, data is taken in by shifting right the content of the UART0 reception data in synchronization with the rising edges of the transfer clock.
 - (3) When 1-byte data lines up in the UART0 receive register, the content of the UART0 receive register is transmitted to the UART0 receive buffer register. The transfer clock stops at "H" level. At this time, the receive complete flag and the UART0 receive interrupt request bit goes to "1".
 - (4) The receive complete flag goes to "0" when the lower-order byte of the UART0 buffer register is read.

Clock-Synchronous Serial I/O

Example of wiring



Example of operation



Shown in () are bit symbols.

The above timing applies to the following settings:

- External clock is selected.
- CLK polarity select bit = "0".

f_{EXT} : frequency of external clock

Make sure that the following conditions are met when the CLK0 pin input = "H" before data reception

- Transmit enable bit → "1"
- Receive enable bit → "1"
- Dummy data write to UART0 transmit buffer register

Figure 2.5.11. Operation timing of reception in clock-synchronous serial I/O mode

Clock-Synchronous Serial I/O

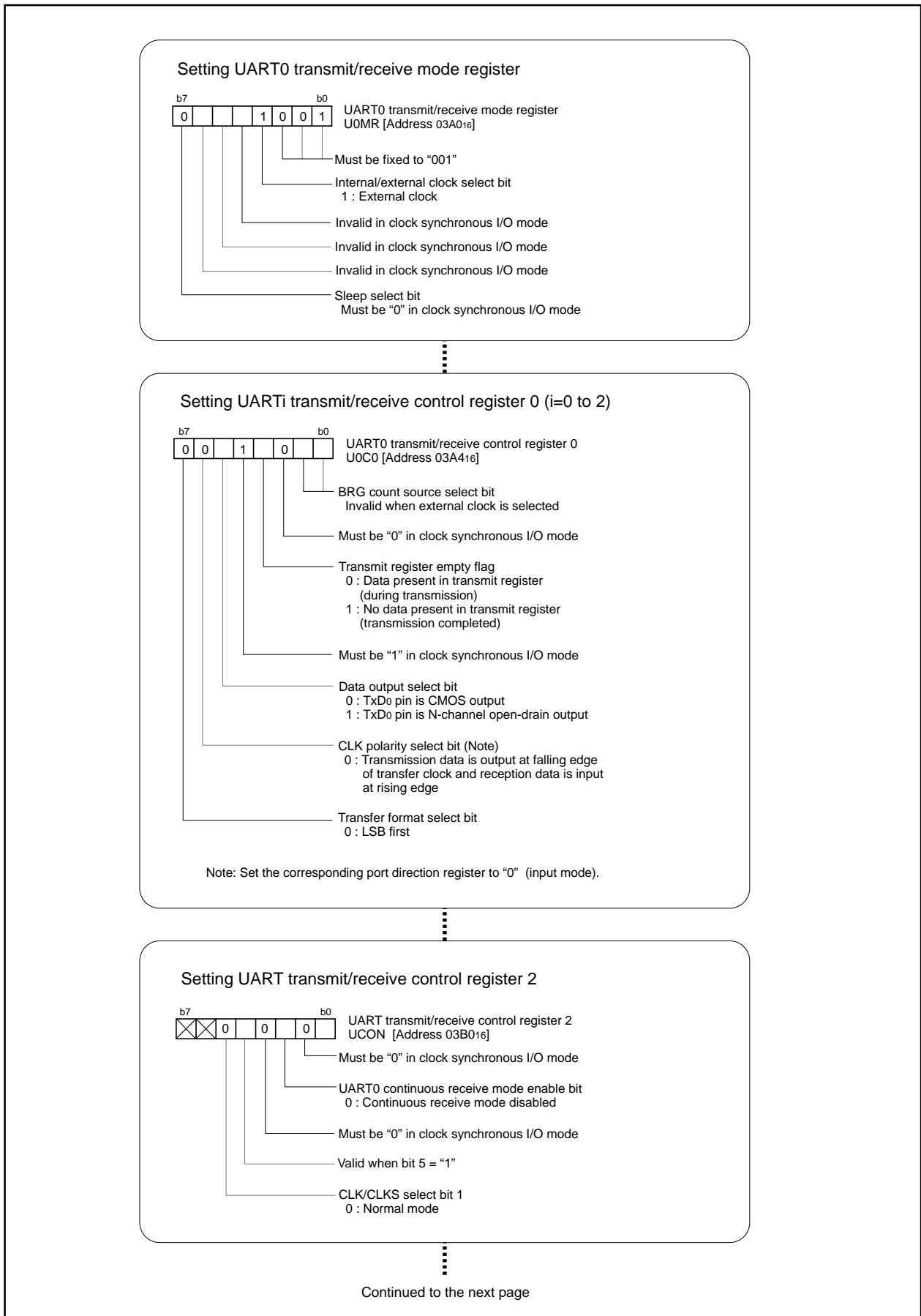


Figure 2.5.12. Set-up procedure of reception in clock-synchronous serial I/O mode (1)

Clock-Synchronous Serial I/O

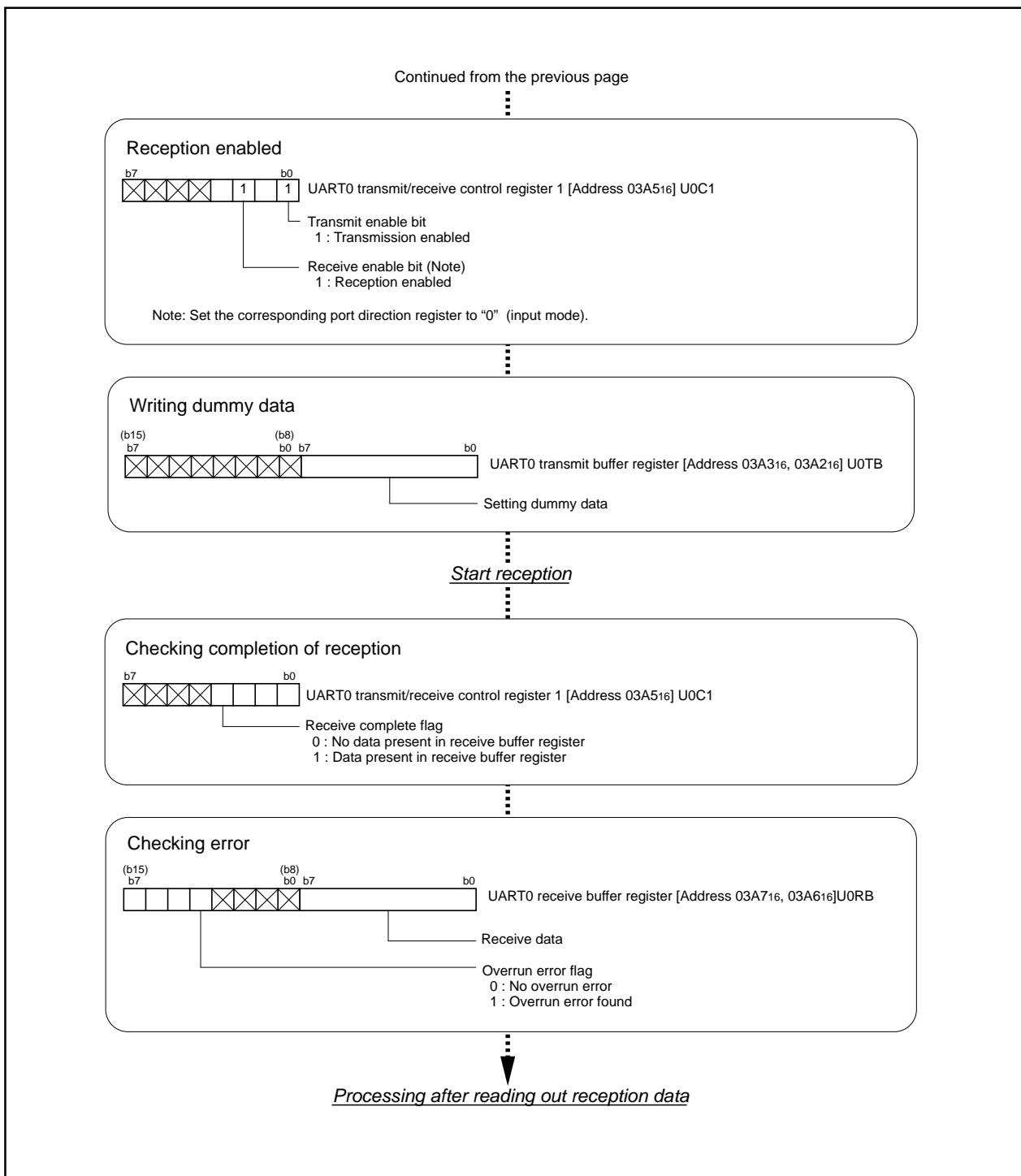


Figure 2.5.13. Set-up procedure of reception in clock-synchronous serial I/O mode (2)

2.5.5 Precautions for Serial I/O (in clock-synchronous serial I/O)

Transmission

- (1) With an external clock selected, perform the following set-up procedure with the CLK0 pin input level = "H" if the CLK polarity select bit = "0" or with the CLK0 pin input level = "L" if the CLK polarity select bit = "1":
 1. Set the transmit enable bit (to "1")
 2. Write transmission data to the UART0 transmit buffer register

Clock-Synchronous Serial I/O

- Reception
- (1) In operating the clock-synchronous serial I/O, operating a transmitter generates a shift clock. Fix settings for transmission even when using the device only for reception. Dummy data is output to the outside from the TxD0 pin (transmission pin) when receiving data.
 - (2) With the internal clock selected, setting the transmit enable bit to "1" (transmission-enabled status) and setting dummy data in the UART0 transmission buffer register generates a shift clock.
With the external clock selected, a shift clock is generated when the transmit enable bit is set to "1", dummy data is set in the UART0 transmit buffer register, and the external clock is input to the CLK0 pin.
 - (3) In receiving data in succession, an overrun error occurs when the next reception data is made ready in the UART0 receive register with the receive complete flag set to "1" (before the content of the UART0 receive buffer register is read), and overrun error flag is set to "1". In this instance, the next data is written to the UART0 receive buffer register, so handle with this problem by writing programs on transmission side and reception side so that the previous data is transmitted again.
If an overrun error occurs, the UART0 receive interrupt request bit does not go to "1".
 - (4) To receive data in succession, set dummy data in the lower-order byte of the UART0 transmit buffer register every time reception is made.
 - (5) With an external clock selected, perform the following set-up procedure with the CLK0 pin input level = "H" if the CLK polarity select bit = "0" or with the CLK0 pin input level = "L" if the CLK polarity select bit = "1":
 1. Set receive enable bit (to "1")
 2. Set transmit enable bit (to "1")
 3. Write dummy data to the UART0 transmit buffer register

UART

2.6 Clock-Asynchronous Serial I/O (UART)

2.6.1 Overview

UART handles communications by means of character-by-character synchronization. The transmission side and the reception side are independent of each other, so full-duplex communication is possible. The following is an overview of the clock-asynchronous serial I/O.

(1) Transmission/reception format

Figure 2.6.1 shows the transmission/reception format, and Table 2.6.1 shows the names and functions of transmission data.

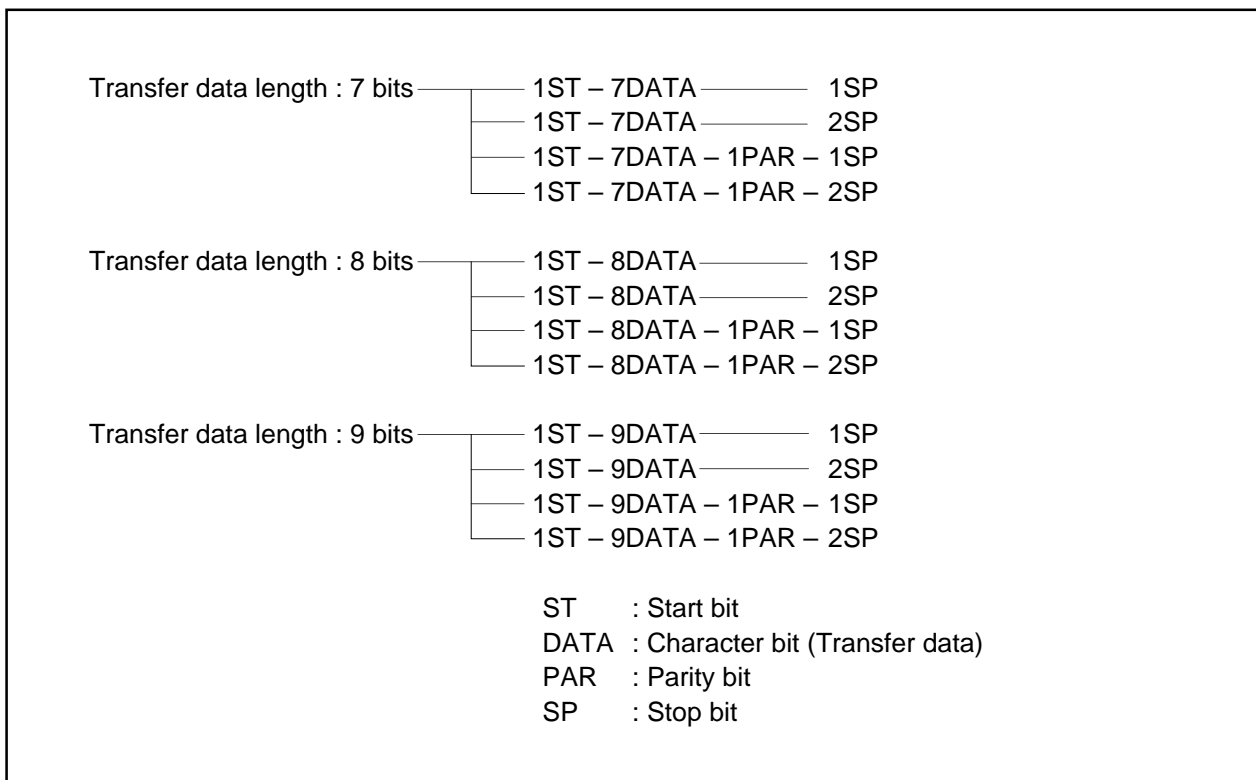


Figure 2.6.1. Transmission/reception format

Table 2.6.1. Transmission data names and functions

Name	Function
ST (start bit)	A 1-bit "L" signal to be added immediately before character bits. This bit signals the start of data transmission.
DATA (character bits)	Transmission data set in the UARTi transmit buffer register.
PAR (parity bit)	A signal to be added immediately after character bits so as to increase data reliability. The level of this signal so varies that the total number of 1's in character bits and this bit always becomes even or odd depending on which parity is chosen, even or odd.
SP (stop bit)	Either 1-bit or 2-bit "H" signal to be added immediately after character bits (after the parity bit if parity is checked). This / they signals the end of data transmission.

UART

(2) Transfer rate

The divide-by-16 frequency, resulting from division in the bit rate generator (BRG), becomes the transfer rate. The count source for the transfer rate register can be selected from f₁, f₈, f₃₂, and the input from the CLK pin. Clocks f₁, f₈, f₃₂ are derived by dividing the CPU's main clock by 1, 8, and 32 respectively.

Table 2.6.2. Example of baud rate setting

Baud rate (bps)	BRG's count source	System clock : 10MHz		System clock : 7.3728MHz	
		BRG's set value : n	Actual time (bps)	BRG's set value : n	Actual time (bps)
600	f ₈	129 (81 ₁₆)	600	95 (5F ₁₆)	600
1200	f ₈	64 (40 ₁₆)	1201	47 (2F ₁₆)	1200
2400	f ₈	32 (20 ₁₆)	2367	23 (17 ₁₆)	2400
4800	f ₁	129 (81 ₁₆)	4807	95 (5F ₁₆)	4800
9600	f ₁	64 (40 ₁₆)	9615	47 (2F ₁₆)	9600
14400	f ₁	42 (2A ₁₆)	14534	31 (1F ₁₆)	14400
19200	f ₁	32 (20 ₁₆)	18939	23 (17 ₁₆)	19200
28800	f ₁	21 (15 ₁₆)	28409	15 (F ₁₆)	28800
31250	f ₁	19 (13 ₁₆)	31250		

UART

(3) An error detection

In clock-asynchronous serial I/O mode, detect errors are shown in Table 2.6.3.

Table 2.6.3. Error detection

Type of error	Description	When the flag turns on	How to clear the flag
Overrun error	<ul style="list-style-type: none"> This error occurs when the next data lines up before the content of the UARTi receive buffer register is read. The next data is written to the UARTi receive buffer register. The UARTi receive interrupt request bit does not change. 	The error is detected when data is transferred from the UARTi receive register to the UARTi receive buffer register.	<ul style="list-style-type: none"> Set the receive enable bit to "0".
Framing error	<ul style="list-style-type: none"> This error occurs when the stop bit falls short of the set number of stop bits. 		<ul style="list-style-type: none"> Set the receive enable bit to "0". Read the lower-order byte of the UARTi receive buffer register.
Parity error	<ul style="list-style-type: none"> With parity enabled, this error occurs when the total number of 1's in character bits and the parity bit is different from the specified number. 		
Error-sum flag	<ul style="list-style-type: none"> This flag turns on when any error (overrun, framing, or parity) is detected. 		<ul style="list-style-type: none"> When all error (overrun, framing, and parity) are removed, the flag is cleared.

UART

(4) Functions selection

In operating UART, the following functions can be used:

(a) Sleep mode

Sleep mode is a mode in which data is transferred to a particular microcomputer among those connected by use of clock-asynchronous serial I/O devices.

The following are examples in which functions (a) to (e) are chosen:

- Transmission WITHOUT: other functions P276
- Reception WITHOUT: other functions P280

(5) Input/output to the serial I/O and the direction register

To input an external signal to the serial I/O, set the direction register of the relevant port to input. To output a signal from the serial I/O, set the direction register of the relevant port to output.

(6) Pins related to the serial I/O

- CLK₀ pins :Input pins for the transfer clock
- Rx_{D0}, Rx_{D1} pins :Input pins for data
- Tx_{D0}, Tx_{D1} pins :Output pins for data

UART

(8) Registers related to the serial I/O

Figure 2.6.2 shows the memory map of serial I/O-related registers, and Figures 2.6.3 to 2.6.7 show UARTi-related registers.

0051 ₁₆	UART0 transmit interrupt control register (S0TIC)
0052 ₁₆	UART0 receive interrupt control register (S0RIC)
0053 ₁₆	UART1 transmit interrupt control register(S1TIC)
0054 ₁₆	UART1 receive interrupt control register(S1RIC)
≈	
03A0 ₁₆	UART0 transmit/receive mode register (U0MR)
03A1 ₁₆	UART0 bit rate generator (U0BRG)
03A2 ₁₆	UART0 transmit buffer register (U0TB)
03A3 ₁₆	
03A4 ₁₆	UART0 transmit/receive control register 0 (U0C0)
03A5 ₁₆	UART0 transmit/receive control register 1 (U0C1)
03A6 ₁₆	UART0 receive buffer register (U0RB)
03A7 ₁₆	
03A8 ₁₆	UART1 transmit/receive mode register (U1MR)
03A9 ₁₆	UART1 bit rate generator (U1BRG)
03AA ₁₆	UART1 transmit buffer register (U1TB)
03AB ₁₆	
03AC ₁₆	UART1 transmit/receive control register 0 (U1C0)
03AD ₁₆	UART1 transmit/receive control register 1 (U1C1)
03AE ₁₆	UART1 receive buffer register (U1RB)
03AF ₁₆	
03B0 ₁₆	UART transmit/receive control register 2 (UCON)

Figure 2.6.2. Memory map of UARTi-related registers

UART

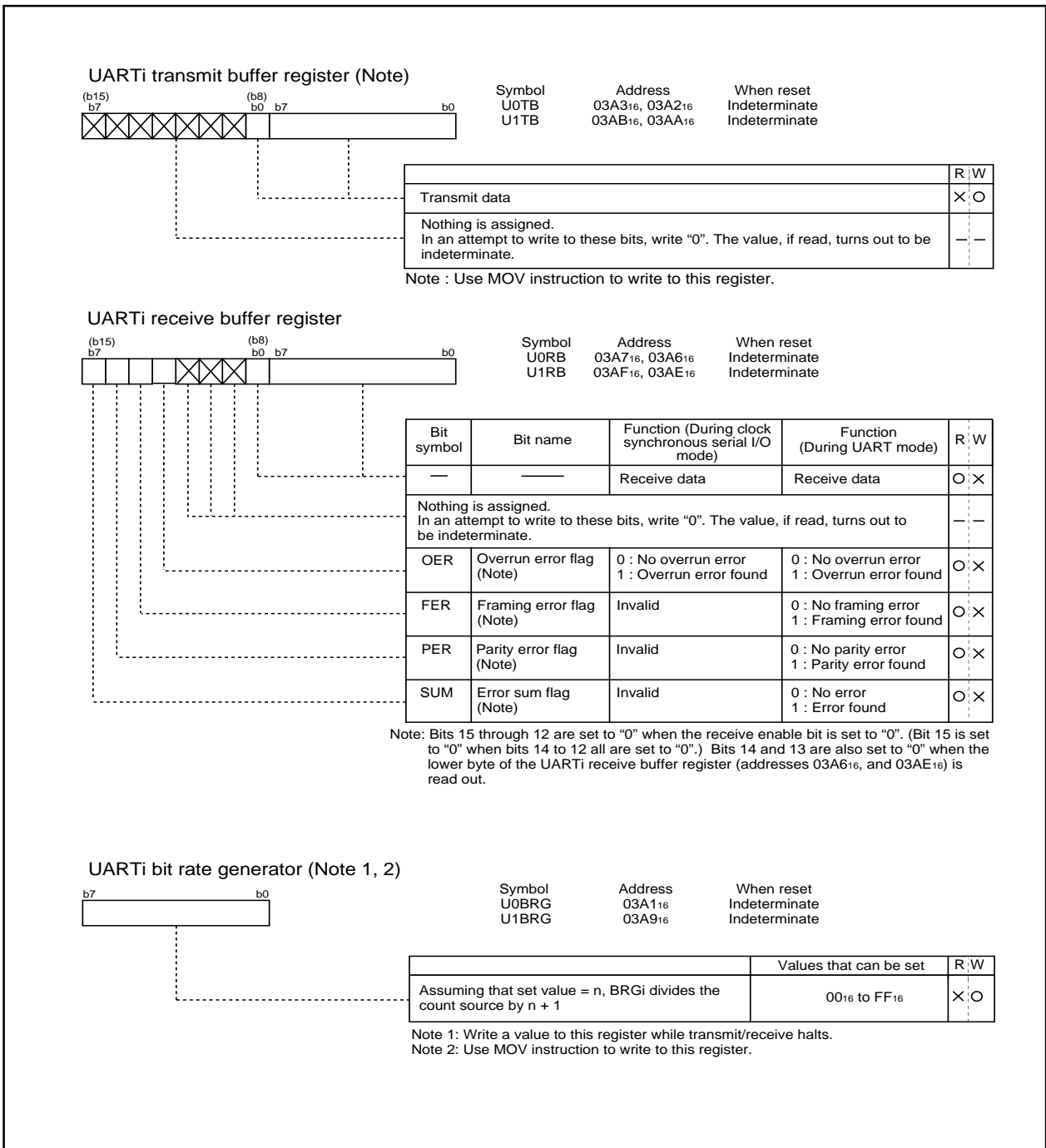


Figure 2.6.3. UARTi-related registers (1)

UART

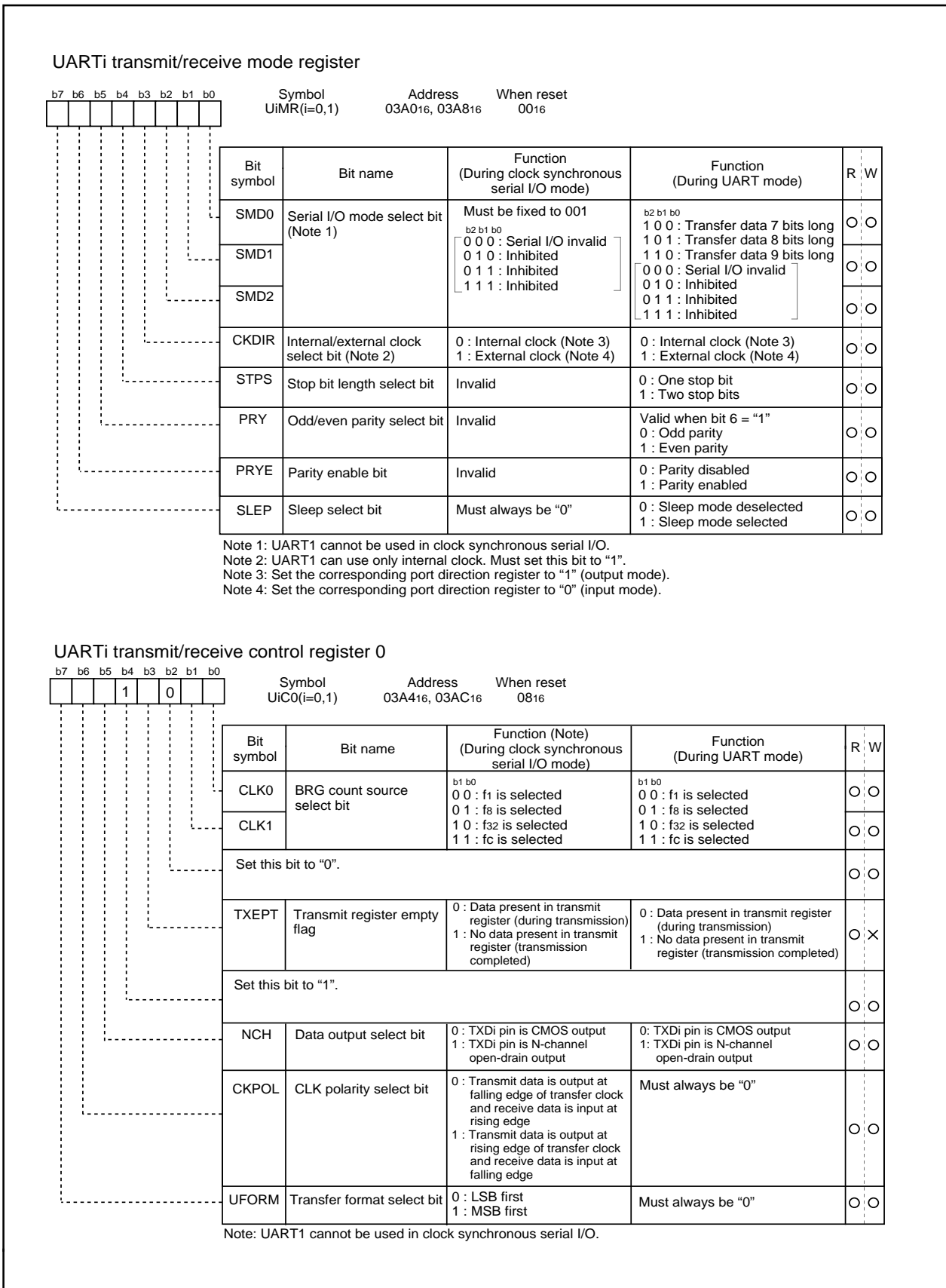


Figure 2.6.4. UARTi-related registers (2)

UART

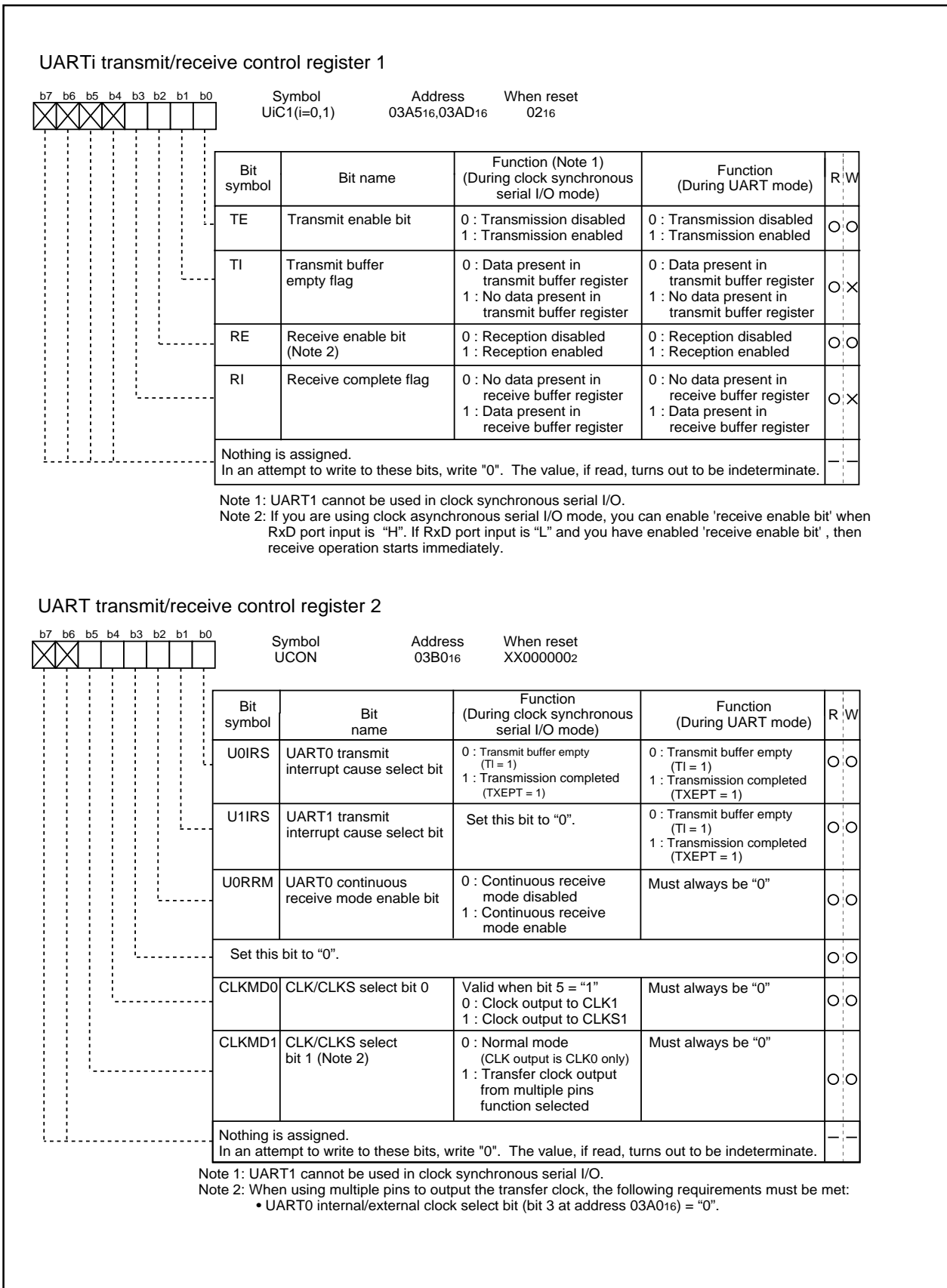


Figure 2.6.5. UARTi-related registers (3)

2.6.2 Operation of Serial I/O (transmission in UART mode)

In transmitting data in UART mode, choose functions from those listed in Table 2.6.4. Operations of the circled items are described below. Figure 2.6.6 shows the operation timing, and Figures 2.6.7 and 2.6.8 show the set-up procedures.

Table 2.6.4. Chosed functions

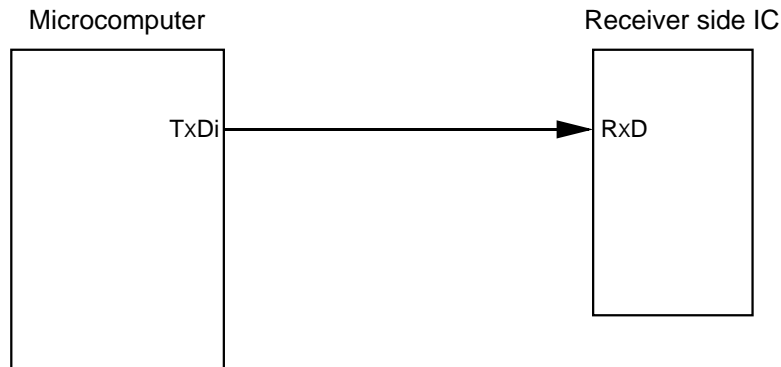
Item	Set-up	
Transfer clock source	<input type="radio"/>	Internal clock ($f_1 / f_8 / f_{32} / f_c$)
	<input type="radio"/>	External clock (CLK0 pin) (Note)
Transmission interrupt factor	<input type="radio"/>	Transmission buffer empty
	<input type="radio"/>	Transmission complete
Sleep mode	<input type="radio"/>	Sleep mode off
	<input type="radio"/>	Sleep mode selected

Note: UART1 cannot be selected external clock.

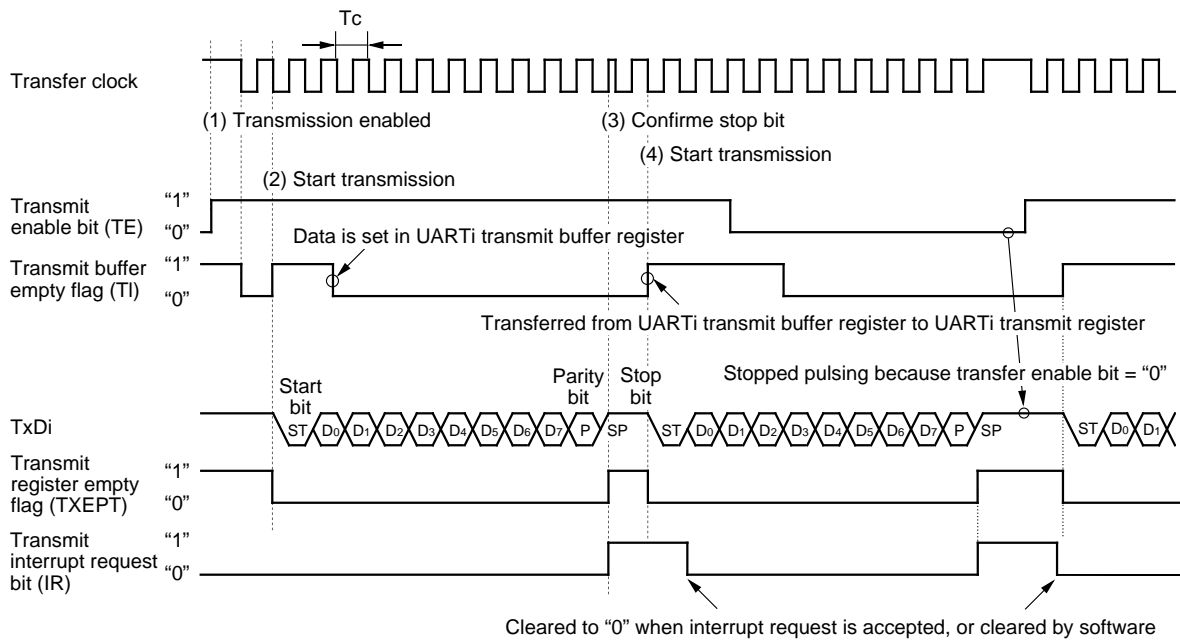
- Operation
- (1) Setting the transmit enable bit to “1” and writing transmission data to the UART_i transmit buffer register readies the data transmissible status.
 - (2) Transmission data held in the UART_i transmit buffer register is transmitted to the UART_i transmit register. At this time, the first bit (the start bit) of the transmission data is transmitted from the Tx_{Di} pin. Then, data is transmitted, bit by bit, in sequence: LSB, ..., MSB, parity bit, and stop bit(s).
 - (3) When the stop bit(s) is (are) transmitted, the transmit register empty flag goes to “1”, which indicates that transmission is completed. At this time, the UART_i transmit interrupt request bit goes to “1”. The transfer clock stops at “H” level.
 - (4) If the transmission condition of the next data is ready when transmission is completed, a start bit is generated following to stop bit(s), and the next data is transmitted.

UART

Example of wiring



Example of operation



Shown in () are bit symbols.

The above timing applies to the following settings :

- Parity is enabled.
- One stop bit.
- Transmit interrupt cause select bit = "1".

$$T_c = 16(n + 1) / f_i \text{ or } 16(n + 1) / f_{EXT}$$

f_i : frequency of BRGi count source (f_1, f_8, f_{32}, f_c)

f_{EXT} : frequency of BRGi count source (external clock)

n : value set to BRGi

Figure 2.6.6. Operation timing of transmission in UART mode

UART

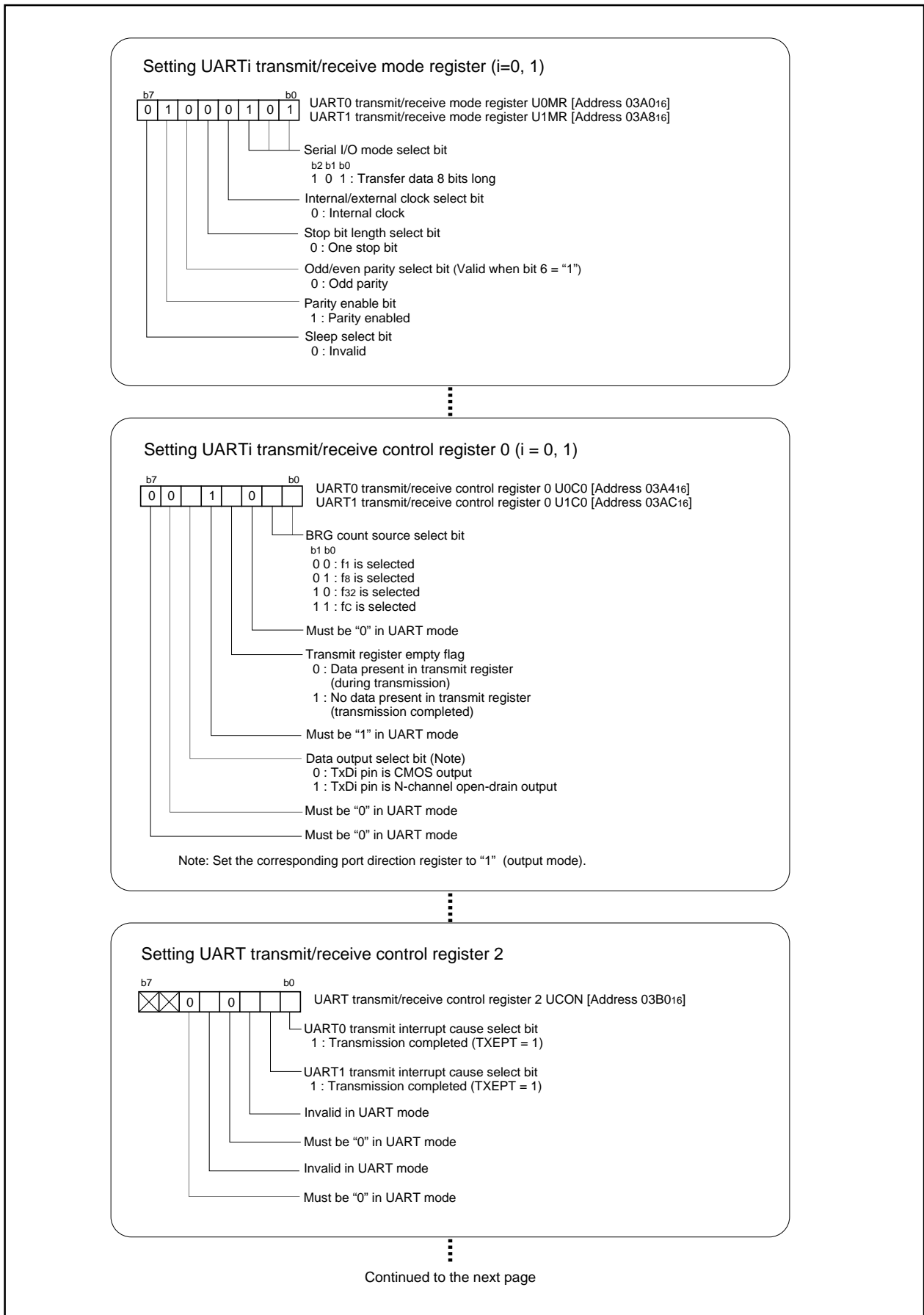


Figure 2.6.7. Set-up procedure of transmission in UART mode (1)

UART

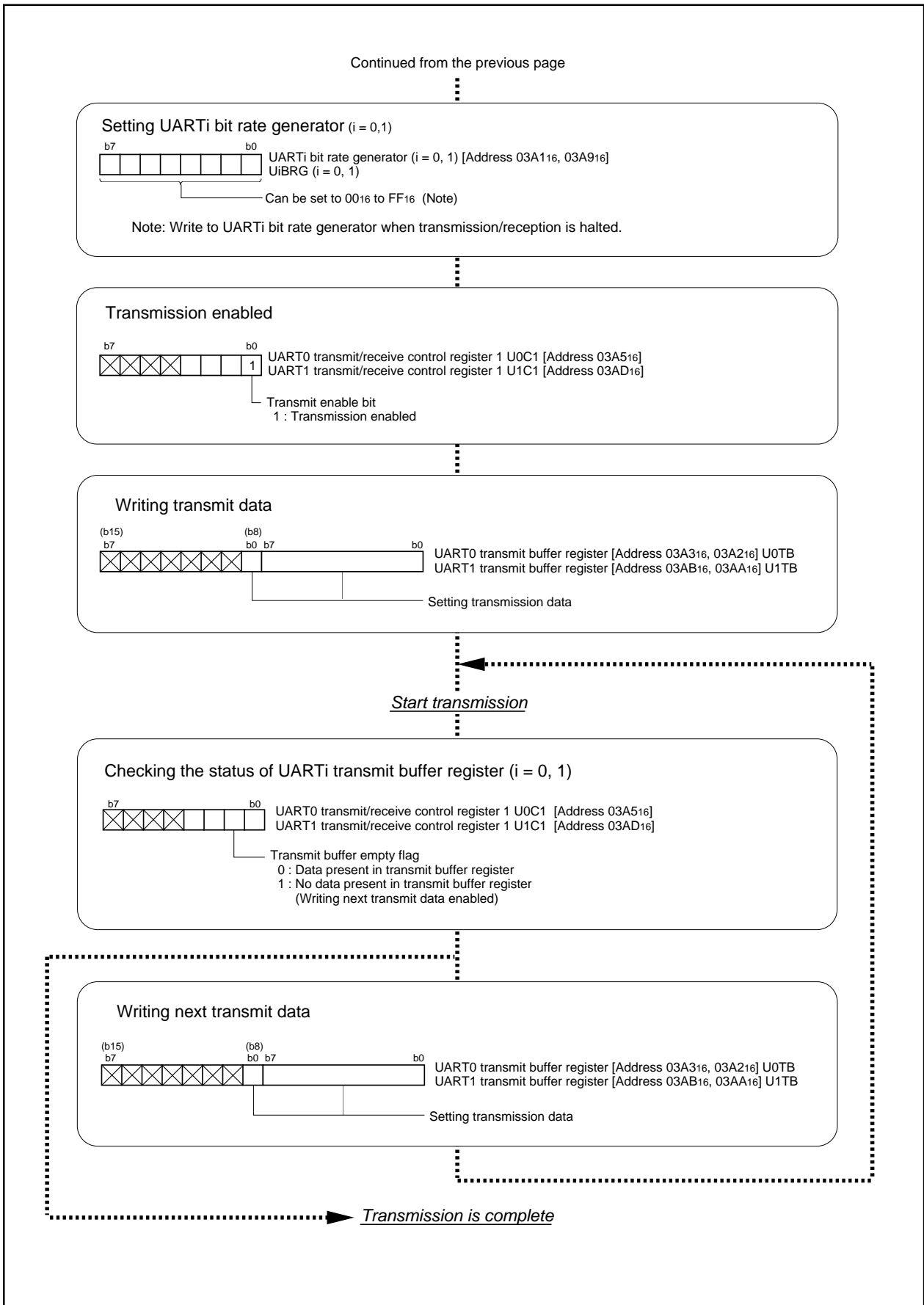


Figure 2.6.8. Set-up procedure of transmission in UART mode (2)

2.6.3 Operation of Serial I/O (reception in UART mode)

In receiving data in UART mode, choose functions from those listed in Table 2.6.5. Operations of the circled items are described below. Figure 2.6.9 shows the operation timing, and Figures 2.6.10 and 2.6.11 show the set-up procedures.

Table 2.6.5. Chosed functions

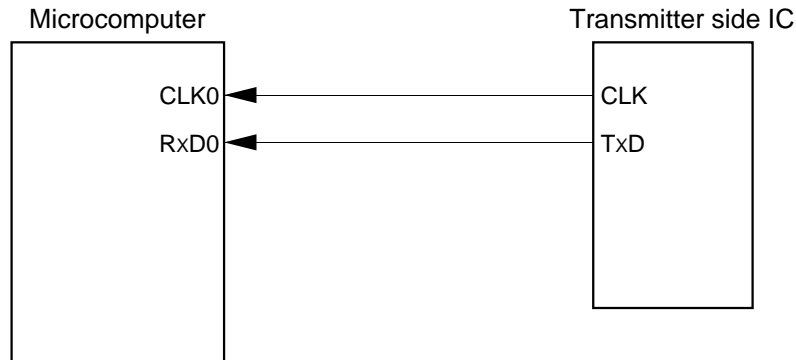
Item	Set-up	
Transfer clock source		Internal clock (f ₁ / f ₈ / f ₃₂ / f _c)
	○	External clock (CLK0 pin) (Note)
Sleep mode	○	Sleep mode off
		Sleep mode selected

Note: UART1 cannot be selected external clock.

- Operation
- (1) Setting the receive enable bit to "1" readies data-receivable status.
 - (2) When the first bit (the start bit) of reception data is received from the RxDi pin. Then, data is received, bit by bit, in sequence: LSB, ..., MSB, and stop bit(s).
 - (3) When the stop bit(s) is (are) received, the content of the UARTi receive register is transmitted to the UARTi receive buffer register.
 At this time, the receive complete flag goes to "1" to indicate that the reception is completed, the UARTi receive interrupt request bit goes to "1".
 - (4) The receive complete flag goes to "0" when the lower-order byte of the UARTi buffer register is read.

UART

Example of wiring



Example of operation

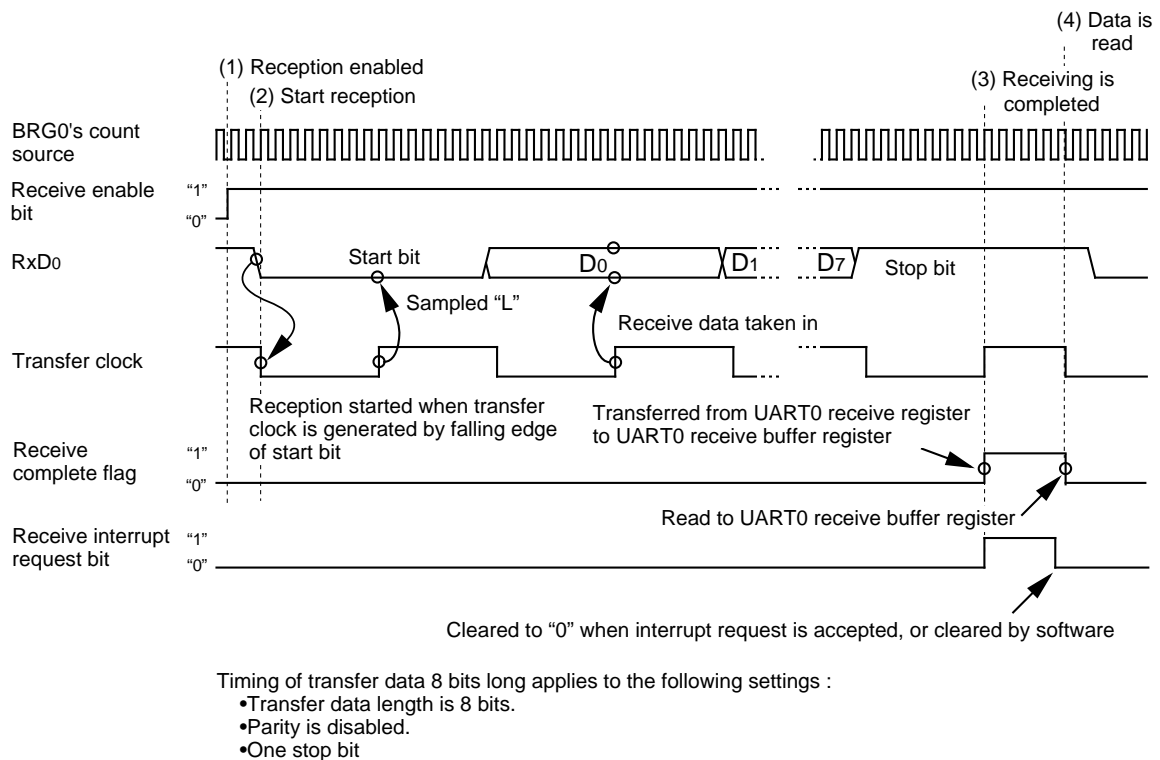


Figure 2.6.9. Operation timing of reception in UART mode

UART

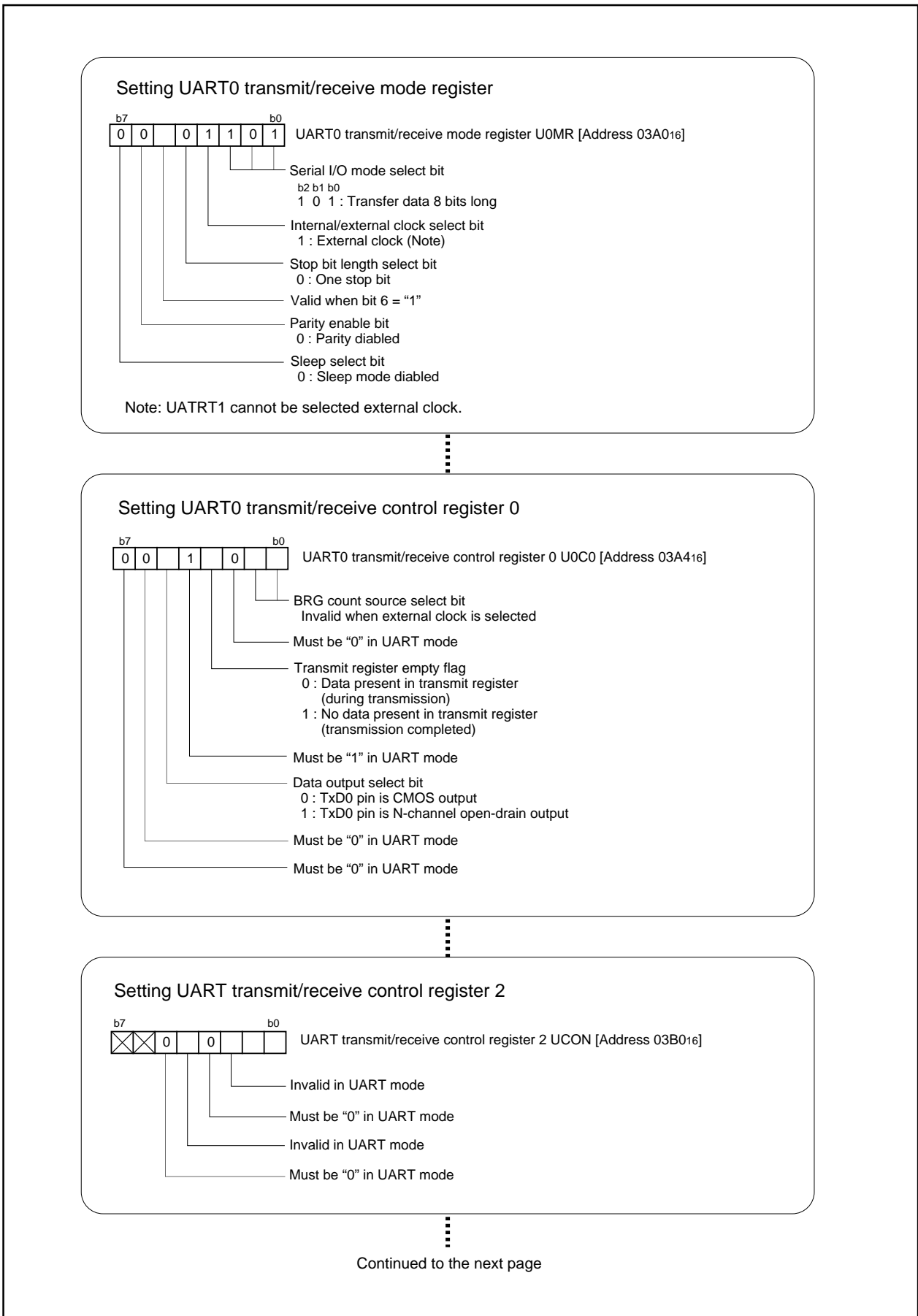


Figure 2.6.10. Set-up procedure of reception in UART mode (1)

UART

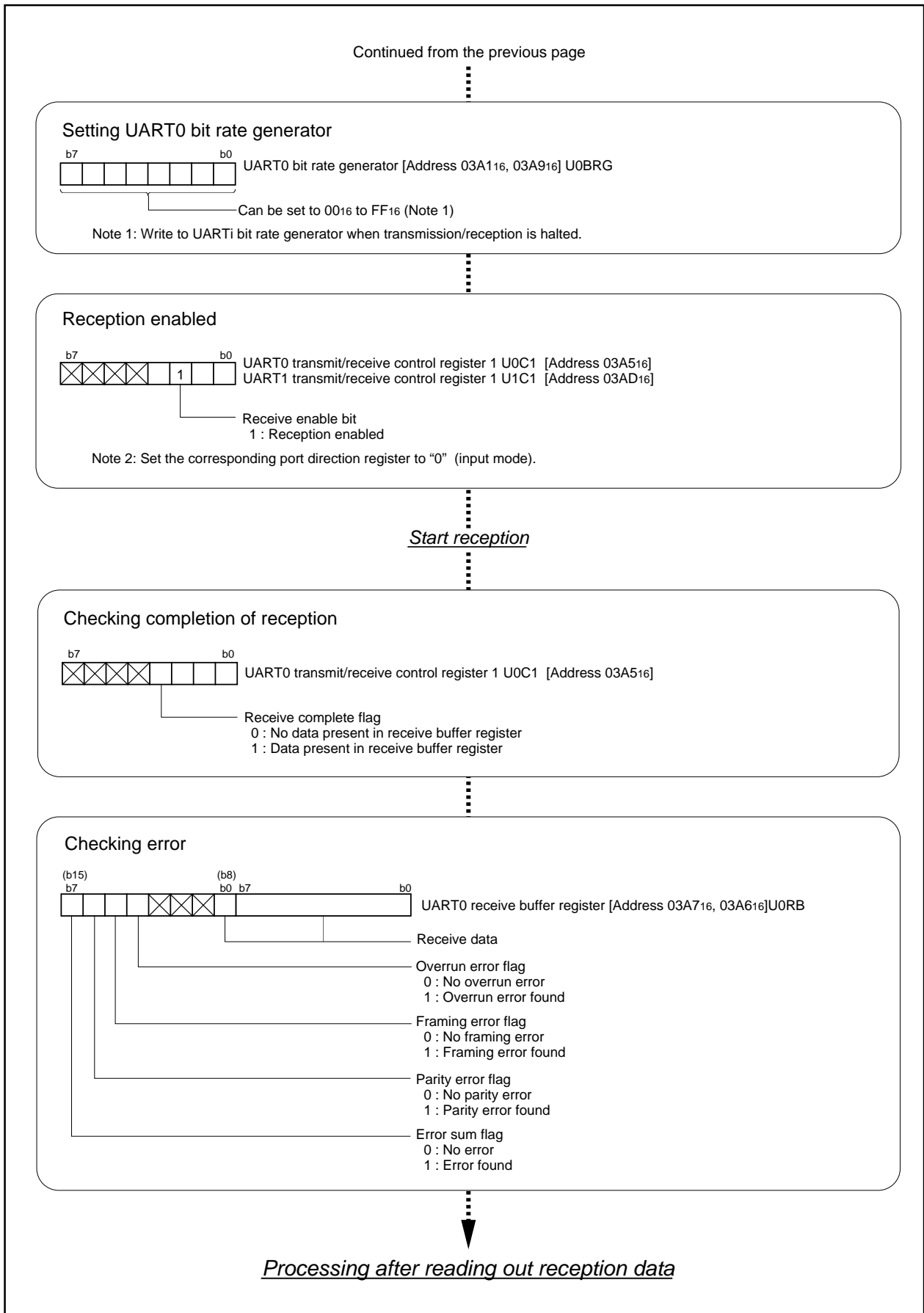


Figure 2.6.11. Set-up procedure of reception in UART mode (2)

2.7 A-D Converter

2.7.1 Overview

The A-D converter used in the M16C/60 group operates on a successive conversion basis. The following is an overview of the A-D converter.

(1) Mode

The A-D converter operates in one of five modes:

(a) One-shot mode

Carries out A-D conversion on input level of one specified pin only once.

(b) Repetition mode

Repeatedly carries out A-D conversion on input level of one specified pin.

(c) Single sweep mode

Carries out A-D conversion on input level of two or more specified pins only once.

(d) Repeated sweep mode 0

Repeatedly carries out A-D conversion on input level of two or more pins.

(e) Repeated sweep mode 1

Repeatedly carries out A-D conversion on input level of two or more pins. This mode is different from the repeated sweep mode 0 in that weights can be assigned to specifying pins control the number of conversion times.

(2) Operation clock

The operation clock in 5 V operation can be selected from the following: f_{AD} , divide-by-2 f_{AD} , and divide-by-4 f_{AD} . In 3 V operation, the selection is divide-by-2 f_{AD} or divide-by-4. The f_{AD} frequency is equal to that of the CPU's main clock.

(3) Conversion time

Number of conversion for A-D convertor varies depending on resolution as given. Table 2.7.1 shows relation between the A-D converter operation clock and conversion time.

Sample & Hold function selected:

33 cycles for 10-bit resolution, or 28 cycles for 8-bit resolution

No Sample & Hold function:

59 cycles for 10-bit resolution, or 49 cycles for 8-bit resolution

Table 2.7.1. Conversion time every operation clock

Frequency selection bit 1		0		1
Frequency selection bit 0		0	1	Invalid
A-D converter's operation clock		$\phi_{AD} = \frac{f_{AD}}{4}$	$\phi_{AD} = \frac{f_{AD}}{2}$	$\phi_{AD} = f_{AD}$
Min. conversion cycles (Note 1)	8-bit mode	28 X ϕ_{AD}		
	10-bit mode	33 X ϕ_{AD}		
Min. conversion time (Note 2)	8-bit mode	11.2 μ s	5.6 μ s	2.8 μ s
	10-bit mode	13.2 μ s	6.6 μ s	3.3 μ s

Note 1: The number of conversion cycles per one analog input pin.

Note 2: The conversion time per one analog input pin (when $f_{AD} = f(X_{IN}) = 10$ MHz)

A-D Converter

(4) Functions selection**(a) Sample & Hold function**

Sample & Hold function samples input voltage when A-D conversion starts and carries out A-D conversion on the voltage sampled. When A-D conversion starts, input voltage is sampled for 3 cycles of the operation clock. When the Sample & Hold function is selected, set the operation clock for A-D conversion to 1 MHz or higher.

(b) 8-bit A-D to 10-bit A-D switching function

Either 8-bit resolution or 10-bit resolution can be selected. When 8-bit resolution is selected, the 8 higher-order bits of the 10-bit A-D are subjected to A-D conversion. The equations for 10-bit resolution and 8-bit resolution are given below:

$$\text{10-bit resolution} \quad (V_{\text{ref}} \times n / 2^{10}) - (V_{\text{ref}} \times 0.5 / 2^{10}) \quad (n = 1 \text{ to } 1023), 0 (n = 0)$$

$$\text{8-bit resolution} \quad (V_{\text{ref}} \times n / 2^8) - (V_{\text{ref}} \times 0.5 / 2^{10}) \quad (n = 1 \text{ to } 256), 0 (n = 0)$$

(c) Analog input group function

The analog input pins can be switched between the port P6 group (AN0 to AN4) and the port P5 group (AN50 to AN54).

(d) Connecting or cutting Vref

Cutting Vref allows decrease of the current flowing into the A-D converter. To decrease the microcomputer's power consumption, cut Vref. To carry out A-D conversion, start A-D conversion 1 μ s or longer after connecting Vref.

The following are examples in which functions (a) through (d) are selected:

- One-shot mode P290
- Repeat mode P292
- Single sweep mode P294
- Repeated sweep mode 0 P296
- Repeated sweep mode 1 P298

(5) Input to A-D converter and direction register

To use the A-D converter, set the direction register of the relevant port to input.

(6) Pins related to A-D converter

- | | |
|-------------------------------|--|
| (a) AN0 pin through AN7 pin | Input pins of the A-D converter (Port P6 group) |
| (b) AN50 pin through AN57 pin | Input pins of the A-D converter (Port P5 group) |
| (c) AVcc pin | Power source pin of the analog section |
| (d) VREF pin | Input pin of reference voltage |
| (e) AVss pin | GND pin of the analog section |

A-D Converter

(7) A-D converter and related registers

Figure 2.7.1 shows the memory map of A-D converter-related registers, and Figures 2.7.2 through 2.7.4 show A-D converter-related registers.

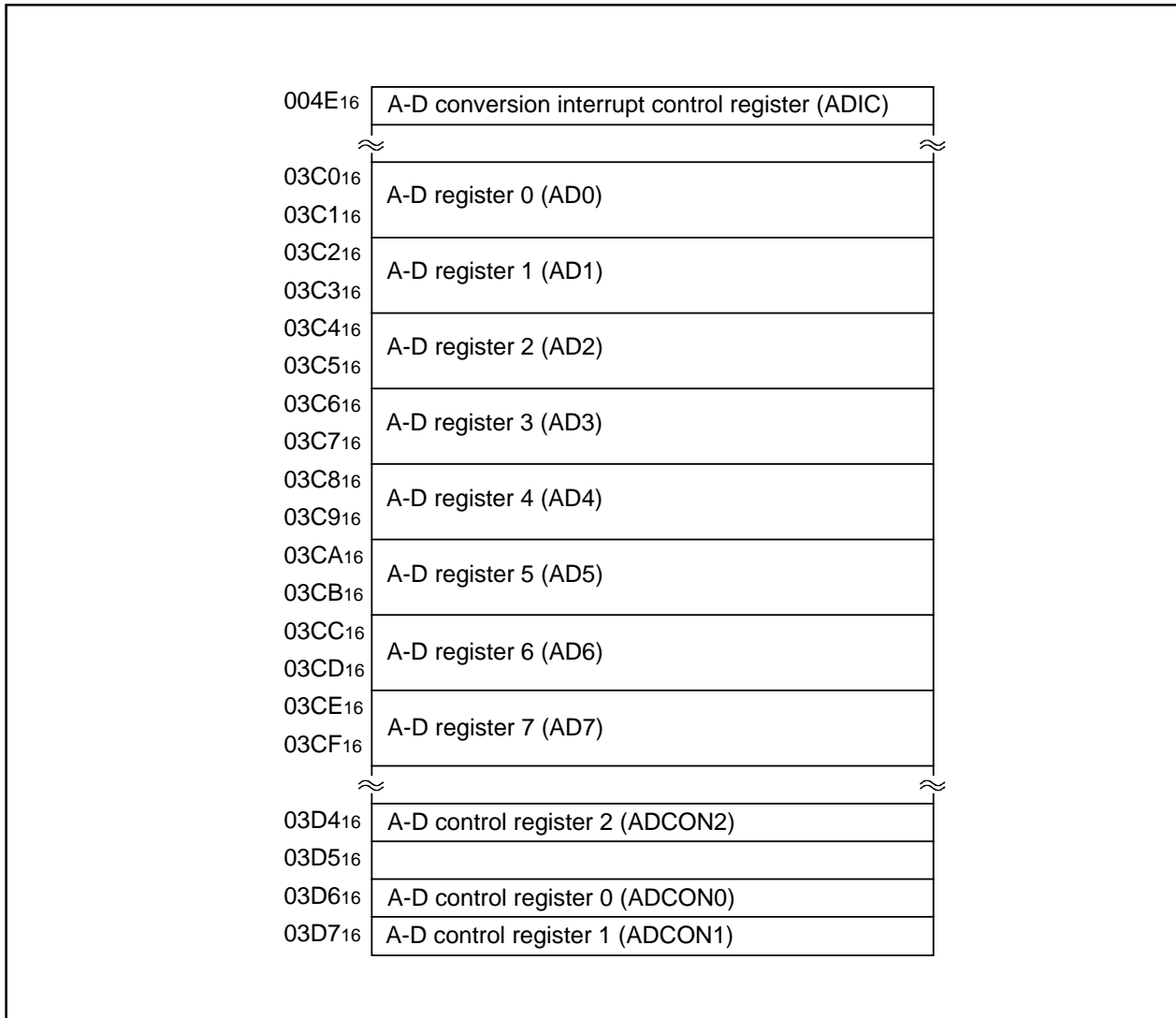


Figure 2.7.1. Memory map of A-D converter-related registers

A-D Converter

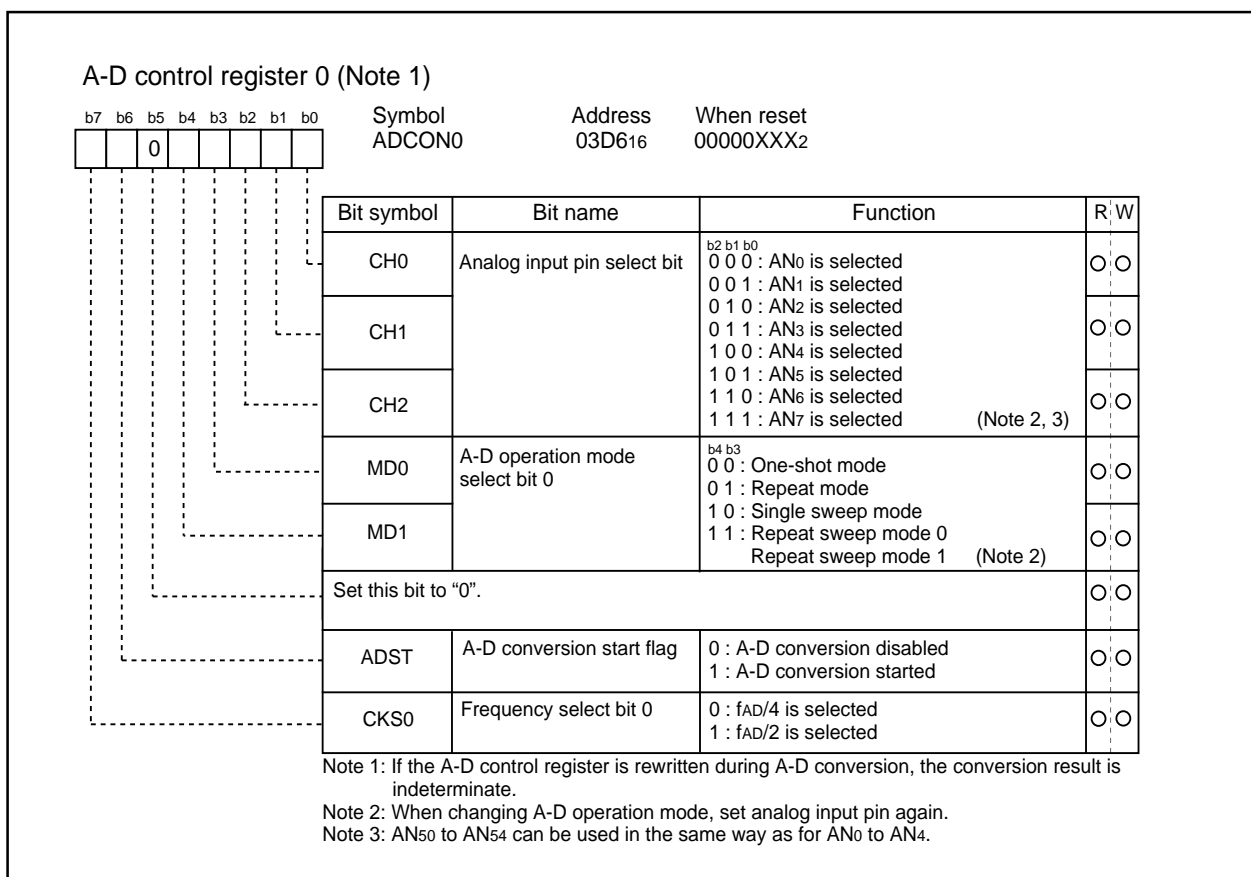


Figure 2.7.2. A-D converter-related registers (1)

A-D Converter

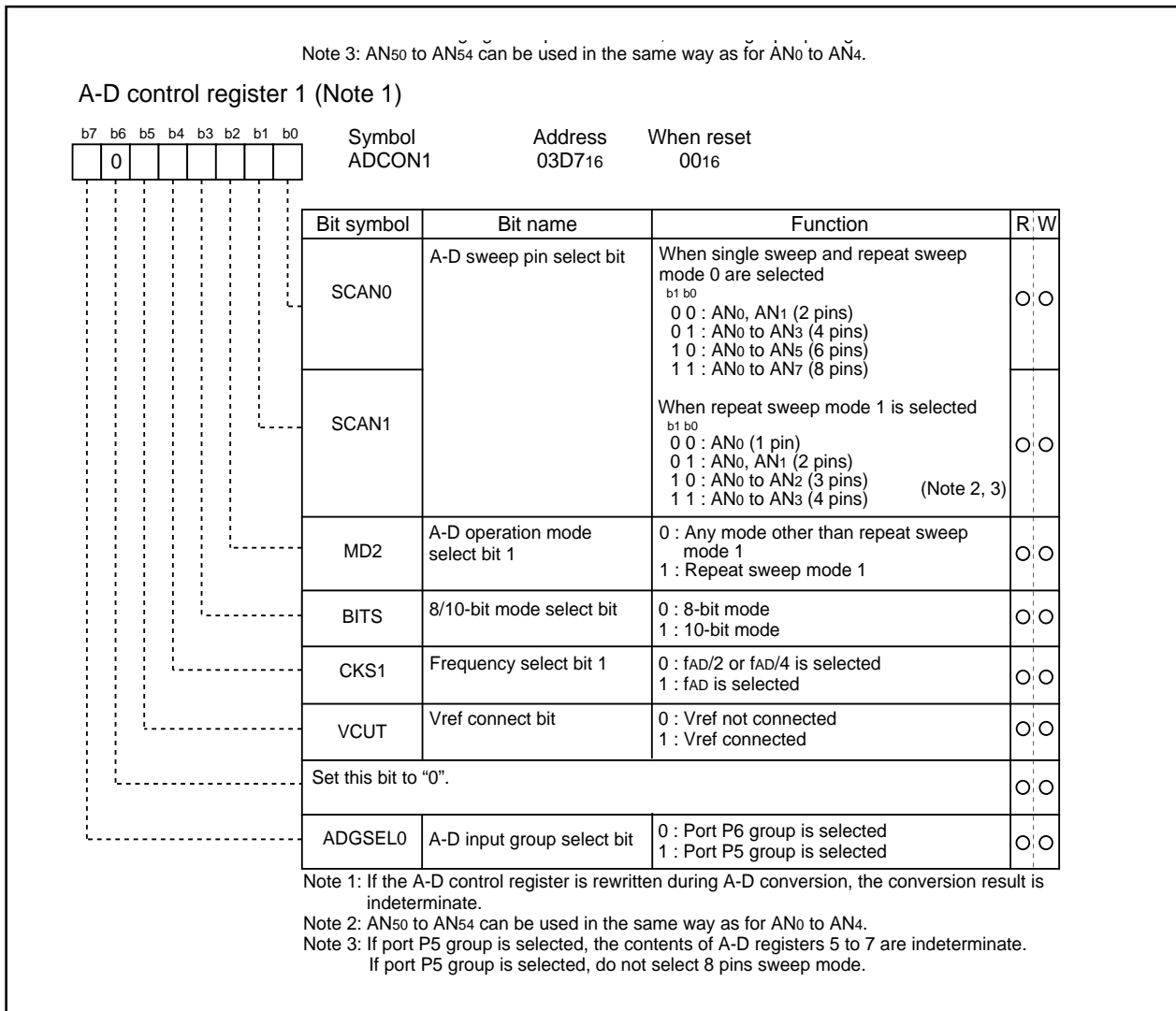


Figure 2.7.3. A-D converter-related registers (2)

A-D Converter

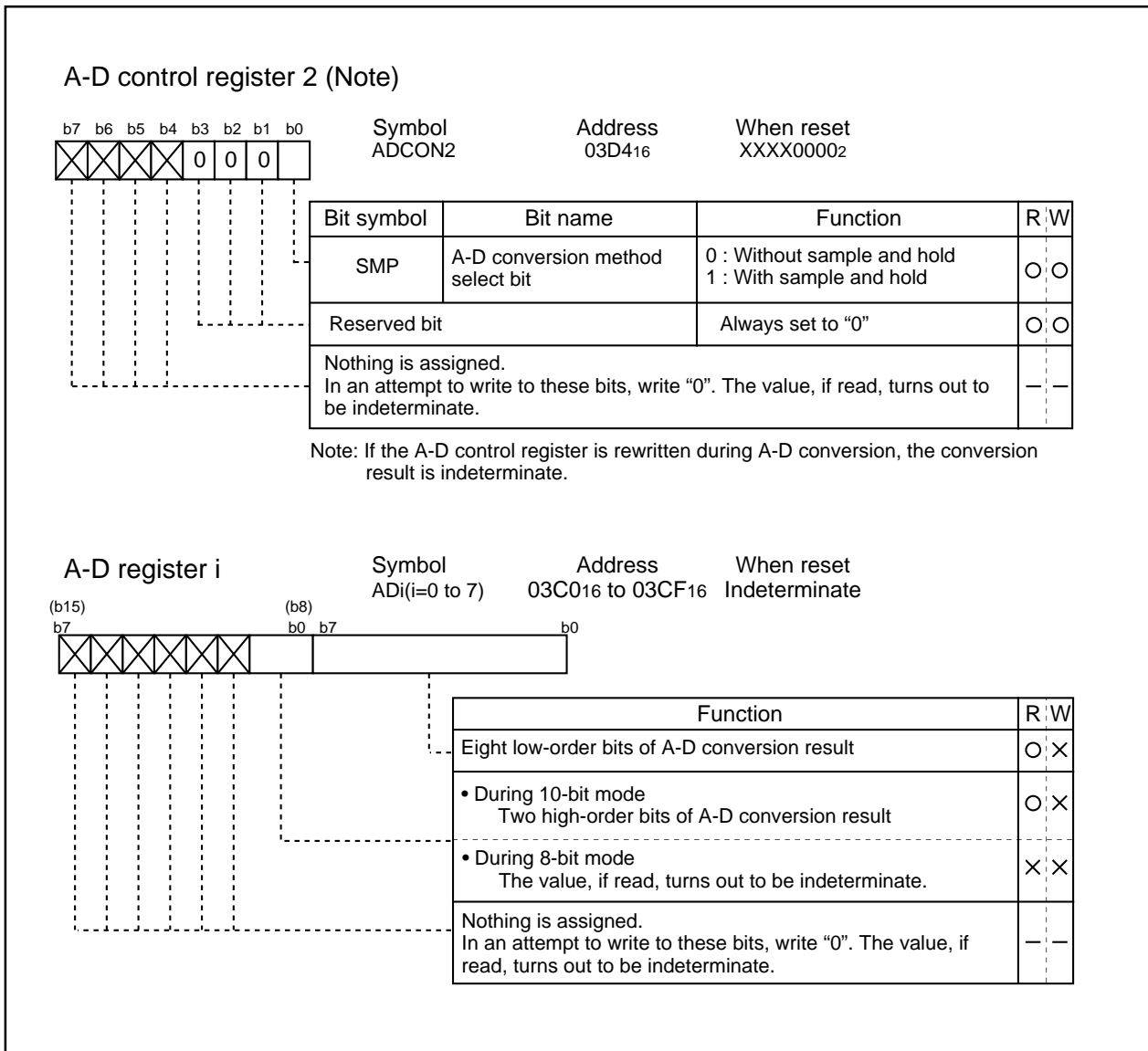


Figure 2.7.4. A-D converter-related registers (3)

A-D Converter

2.7.2 Operation of A-D converter (one-shot mode)

In one-shot mode, choose functions from those listed in Table 2.7.2. Operations of the circled items are described below. Figure 2.7.5 shows the operation timing, and Figure 2.7.6 shows the set-up procedure.

Table 2.7.2. Chosed functions

Item	Set-up
Operation clock ϕ_{AD}	○ Divided-by-4 f_{AD} / divided-by-2 f_{AD} / f_{AD}
Resolution	○ 8-bit / 10-bit
Analog input pin	○ One of AN ₀ pin to AN ₇ pin (Note)
Sample & Hold	○ Not activated
	○ Activated

Note : When the port P5 group is selected, analog input pins are changed from AN₀ to AN₄ to pins AN₅₀ to AN₅₄.

- Operation (1) Setting the A-D conversion start flag to "1" causes the A-D converter to begin operating.
 (2) After A-D conversion is completed, the content of the successive comparison register (conversion result) is transmitted to A-D register i. At this time, the A-D conversion interrupt request bit goes to "1". Also, the A-D conversion start flag goes to "0", and the A-D converter stops operating.

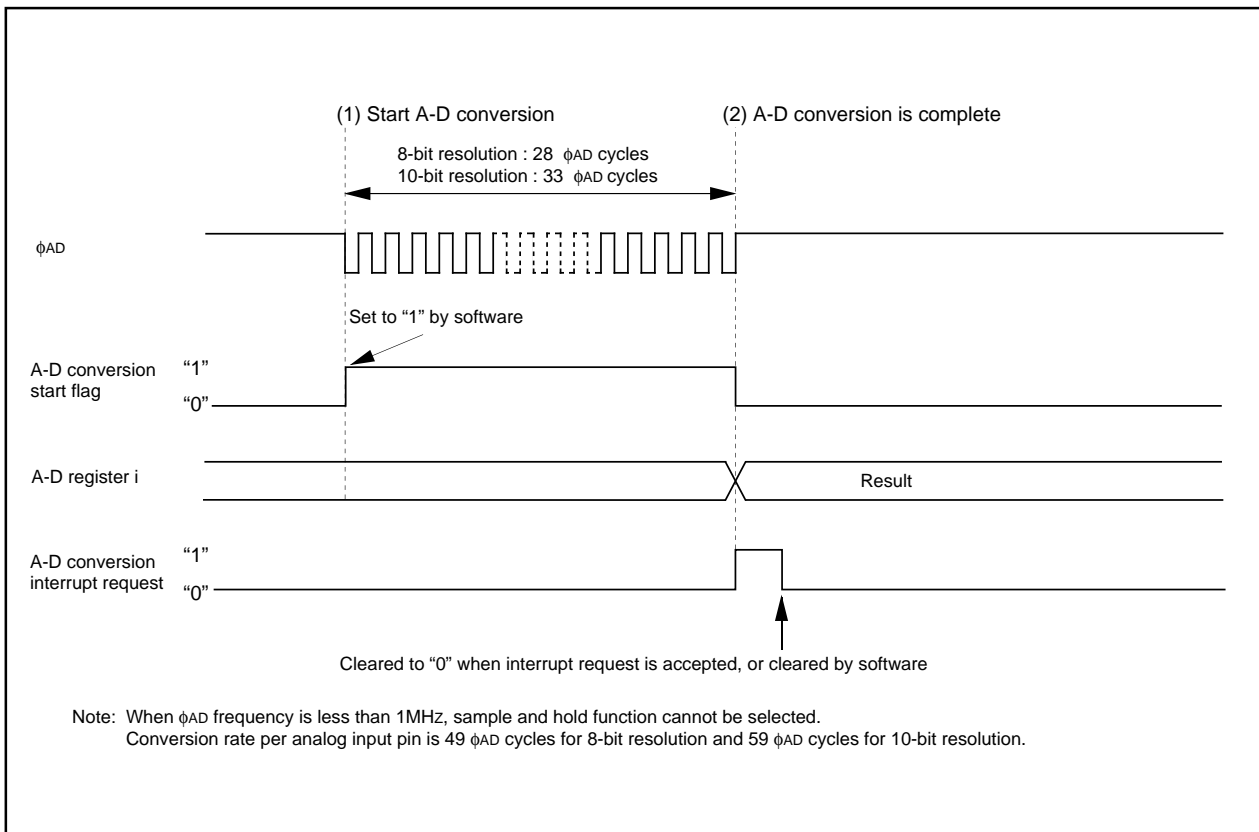


Figure 2.7.5. Operation timing of one-shot mode

A-D Converter

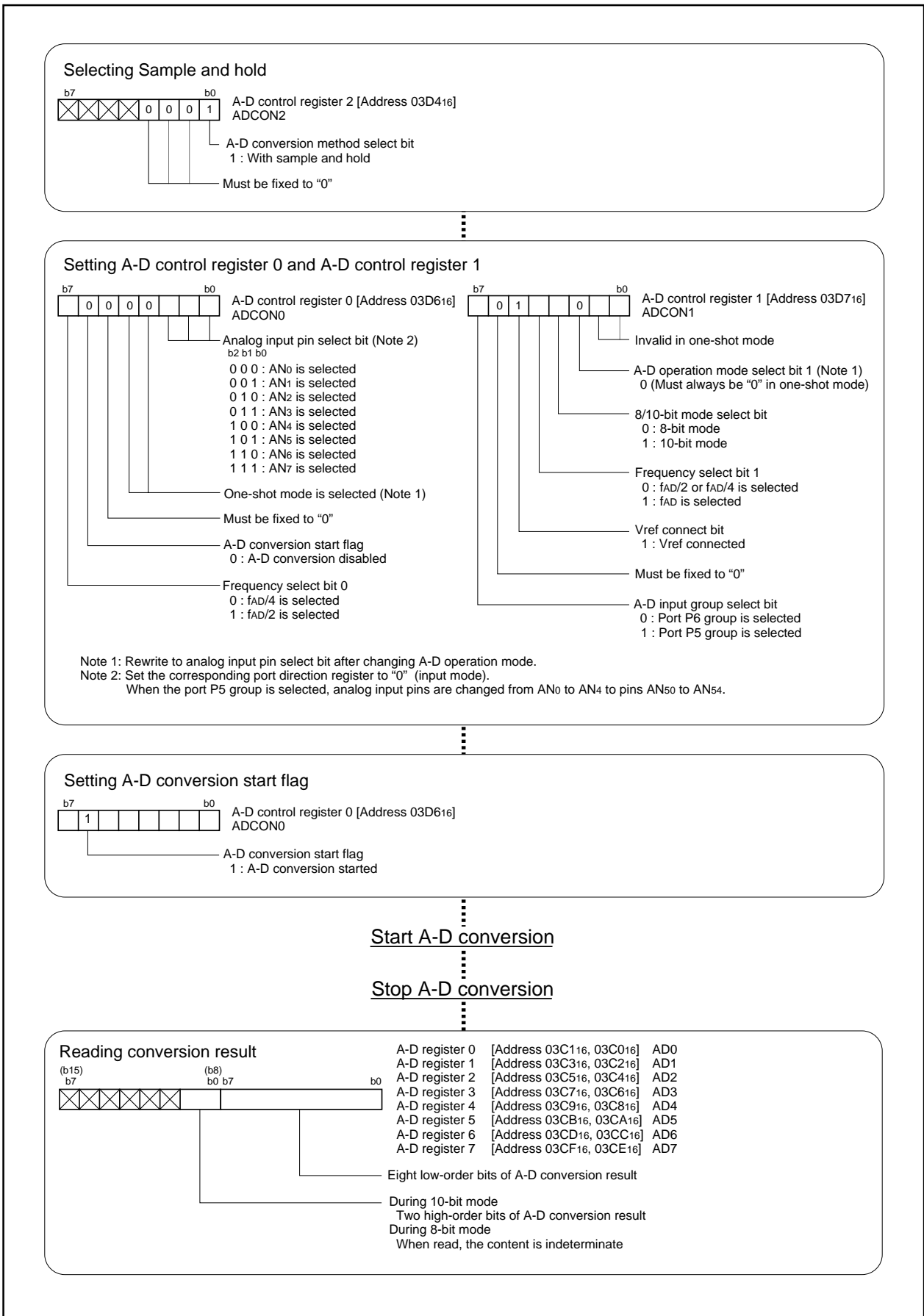


Figure 2.7.6. Set-up procedure of one-shot mode

A-D Converter

2.7.3 Operation of A-D Converter (in repeat mode)

In repeat mode, choose functions from those listed in Table 2.7.3. Operations of the circled items are described below. Figure 2.7.7 shows timing chart, and Figure 2.7.8 shows the set-up procedure.

Table 2.7.3. Chosed functions

Item	Set-up
Operation clock ϕ_{AD}	<input type="radio"/> Divided-by-4 f_{AD} / divided-by-2 f_{AD} / f_{AD}
Resolution	<input type="radio"/> 8-bit / 10-bit
Analog input pin	<input type="radio"/> One of AN ₀ pin to AN ₇ pin (Note)
Sample & Hold	<input type="checkbox"/> Not activated
	<input type="radio"/> Activated

Note : When the port P5 group is selected, analog input pins are changed from AN₀ to AN₄ to pins AN₅₀ to AN₅₄.

- Operation
- (1) Setting the A-D conversion start flag to "1" causes the A-D converter to start operating.
 - (2) After the first conversion is completed, the content of the successive comparison register (conversion result) is transmitted to A-D register i. The A-D conversion interrupt request bit does not go to "1".
 - (3) The A-D converter continues operating until the A-D conversion start flag is set to "0" by software. The conversion result is transmitted to A-D register i every time a conversion is completed.

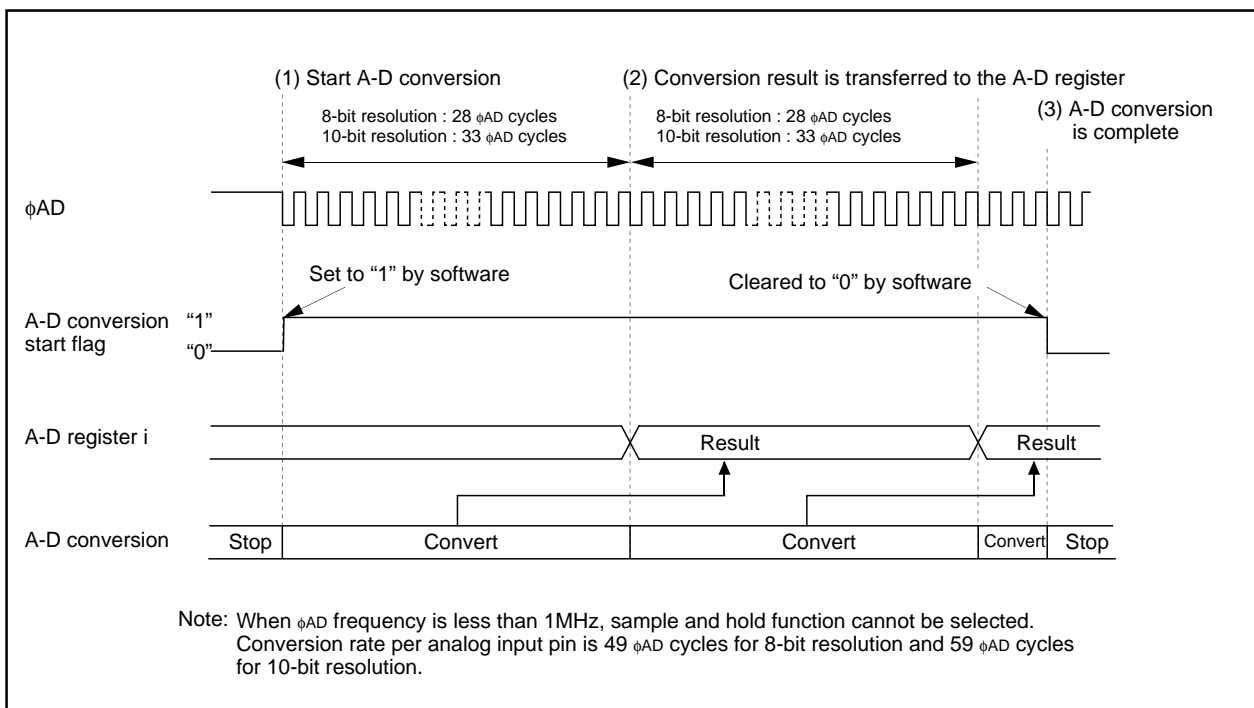


Figure 2.7.7. Operation timing of repeat mode

A-D Converter

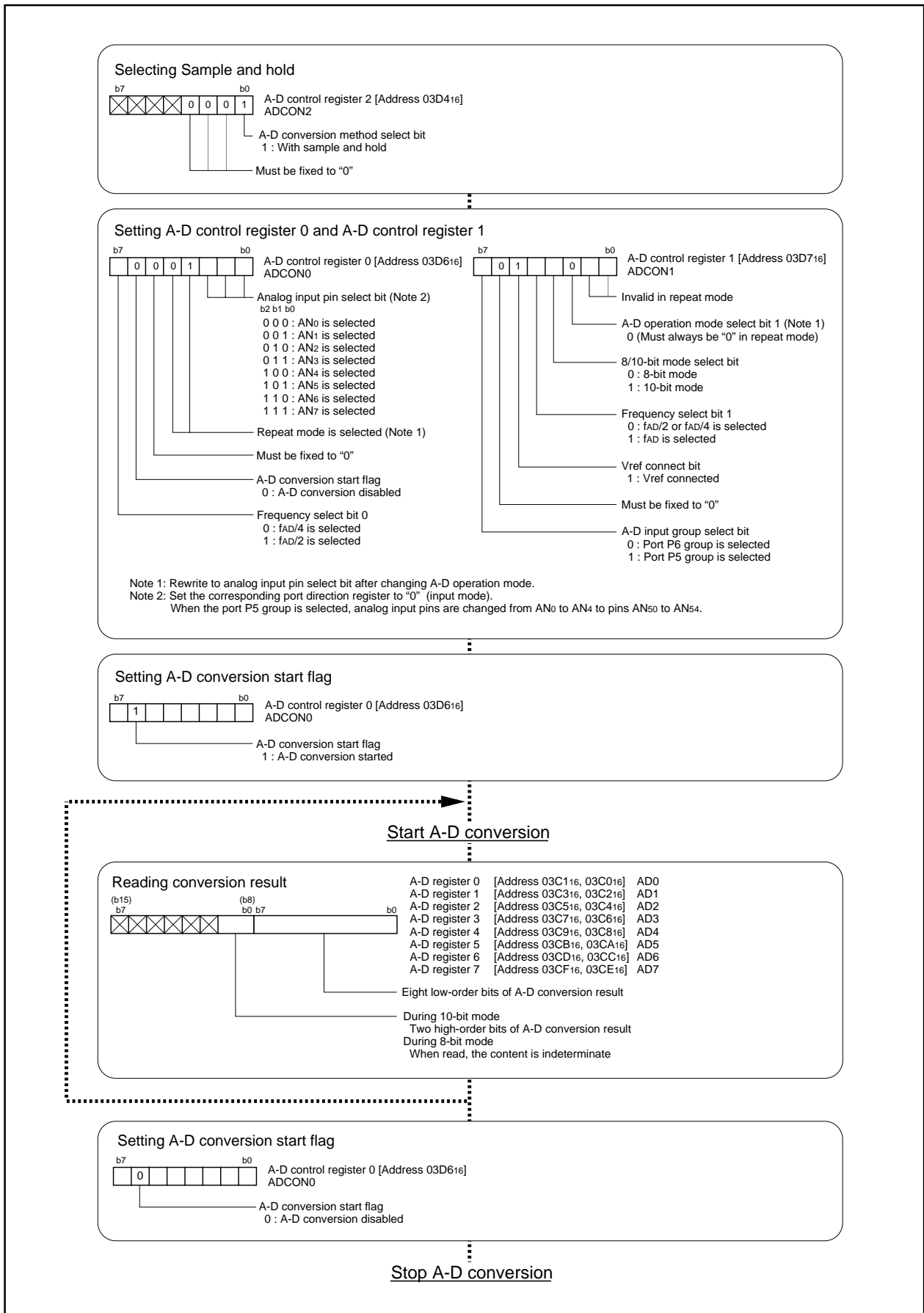


Figure 2.7.8. Set-up procedure of repeat mode

A-D Converter

2.7.4 Operation of A-D Converter (in single sweep mode)

In single sweep mode, choose functions from those listed in Table 2.7.4. Operations of the circled items are described below. Figure 2.7.9 shows timing chart, and Figure 2.7.10 shows the set-up procedure.

Table 2.7.4. Chosed functions

Item	Set-up
Operation clock ϕ_{AD}	○ Divided-by-4 f_{AD} / divided-by-2 f_{AD} / f_{AD}
Resolution	○ 8-bit / 10-bit
Analog input pin	○ AN ₀ and AN ₁ (2 pins) / AN ₀ to AN ₃ (4 pins) / AN ₀ to AN ₅ (6 pins) / AN ₀ to AN ₇ (8 pins) (Note)
Sample & Hold	Not activated
	○ Activated

Note : When the port P5 group is selected, analog input pins are changed from AN₀ to AN₄ to pins AN₅₀ to AN₅₄.

- Operation
- (1) Setting the A-D conversion start flag to "1" causes the A-D converter to start the conversion on voltage input to the AN₀/AN₅₀ pin.
 - (2) After the A-D conversion of voltage input to the AN₀/AN₅₀ pin is completed, the content of the successive comparison register (conversion result) is transmitted to A-D register 0. The A-D converter converts all analog input pins selected by the user. The conversion result is transmitted to A-D register i corresponding to each pin, every time conversion on one pin is completed.
 - (3) When the A-D conversion on all the analog input pins selected is completed, the A-D conversion interrupt request bit goes to "1". At this time, the A-D conversion start flag goes to "0". The A-D converter stops operating.

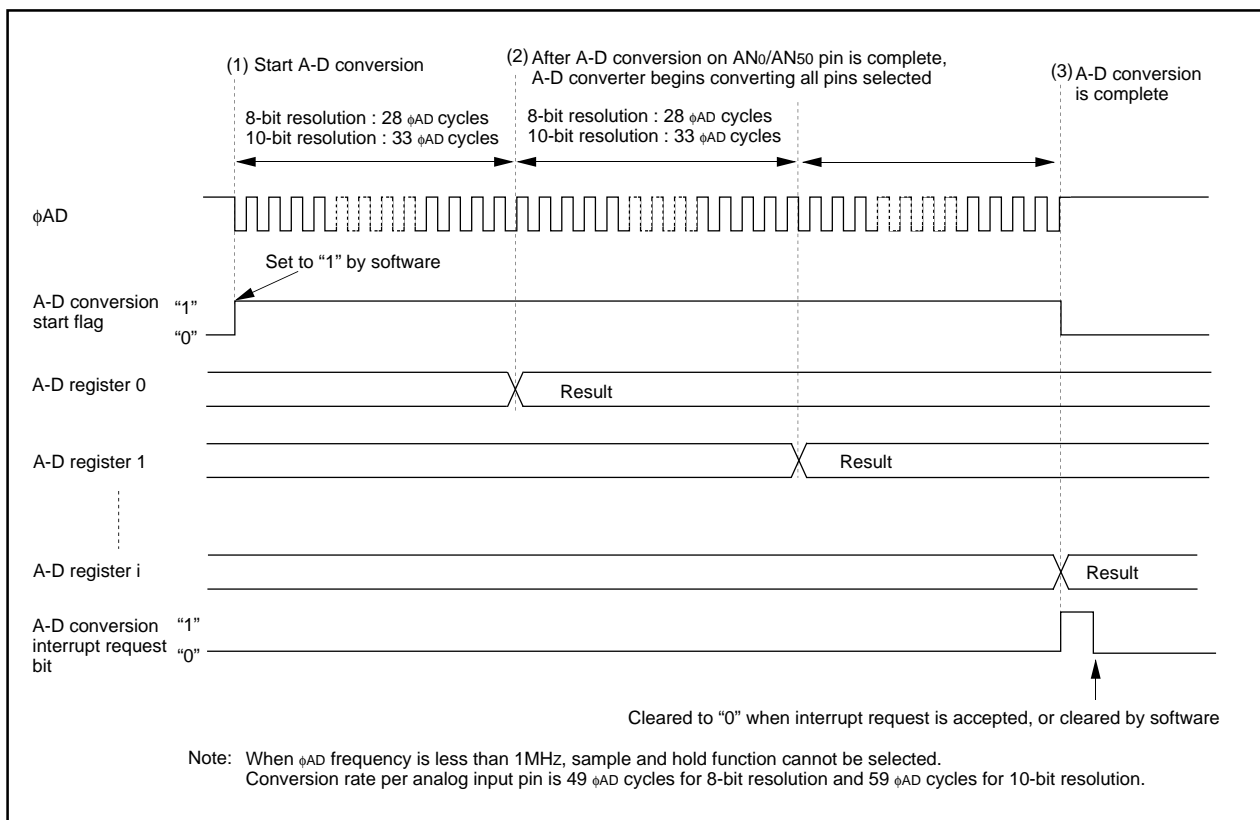
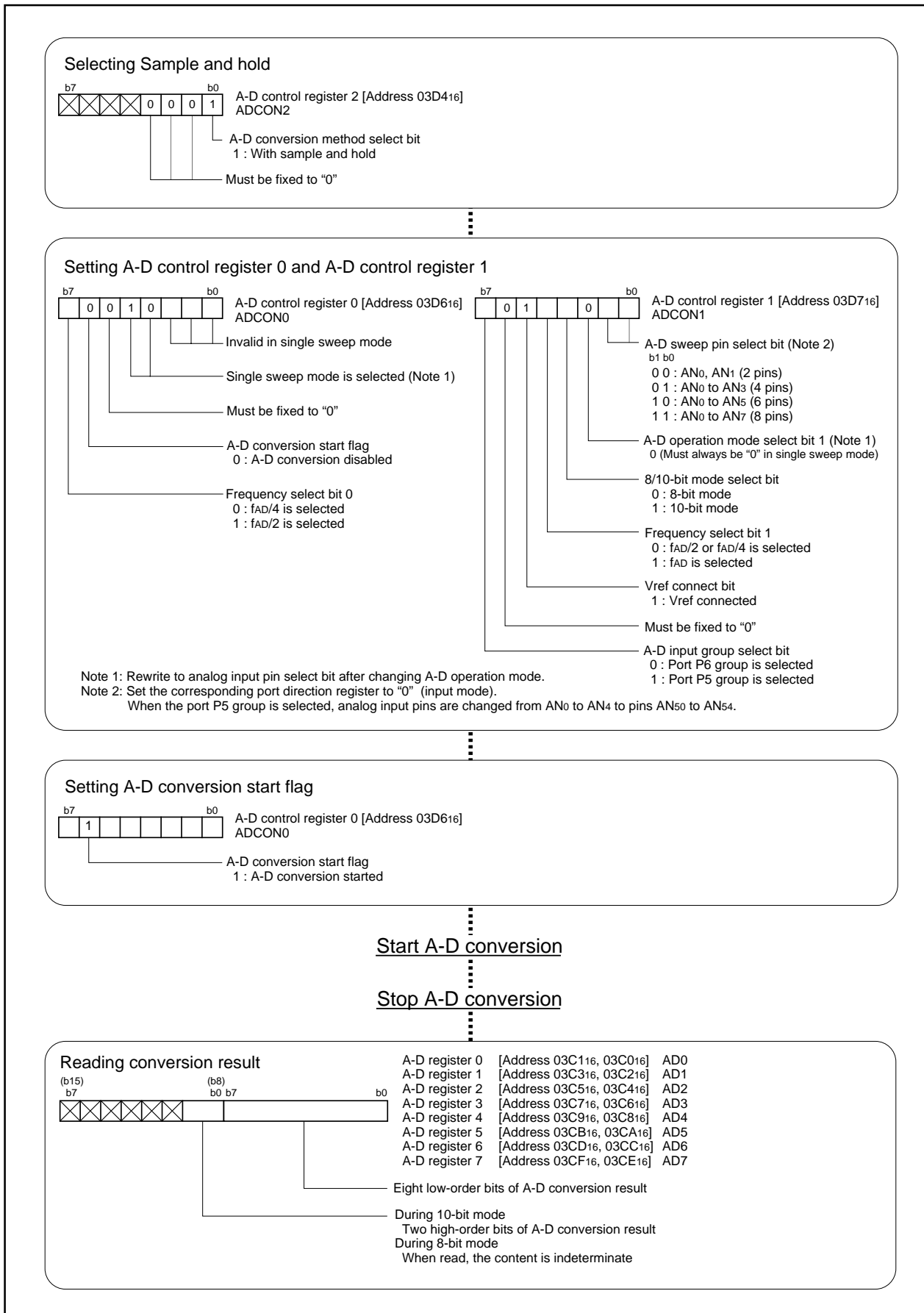


Figure 2.7.9. Operation timing of single sweep mode

A-D Converter



A-D Converter

2.7.5 Operation of A-D Converter (in repeat sweep mode 0)

In repeat sweep 0 mode, choose functions from those listed in Table 2.7.5. Operations of the circled items are described below. Figure 2.7.11 shows timing chart, and Figure 2.7.12 shows the set-up procedure.

Table 2.7.5. Chosed functions

Item	Set-up
Operation clock ϕ_{AD}	○ Divided-by-4 f_{AD} / divided-by-2 f_{AD} / f_{AD}
Resolution	○ 8-bit / 10-bit
Analog input pin	○ AN ₀ and AN ₁ (2 pins) / AN ₀ to AN ₃ (4 pins) / AN ₀ to AN ₅ (6 pins) / AN ₀ to AN ₇ (8 pins) (Note)
Sample & Hold	○ Not activated
	○ Activated

Note : When the port P5 group is selected, analog input pins are changed from AN₀ to AN₄ to pins AN₅₀ to AN₅₄.

- Operation
- (1) Setting the A-D conversion start flag to "1" causes the A-D converter to start the conversion on voltage input to the AN₀/AN₅₀ pin.
 - (2) After the A-D conversion of voltage input to the AN₀/AN₅₀ pin is completed, the content of the successive comparison register (conversion result) is transmitted to A-D register 0.
 - (3) The A-D converter converts all pins selected by the user. The conversion result is transmitted to A-D register i corresponding to each pin every time A-D conversion on the pin is completed. The A-D conversion interrupt request bit does not go to "1".
 - (4) The A-D converter continues operating until the A-D conversion start flag is set to "0" by software.

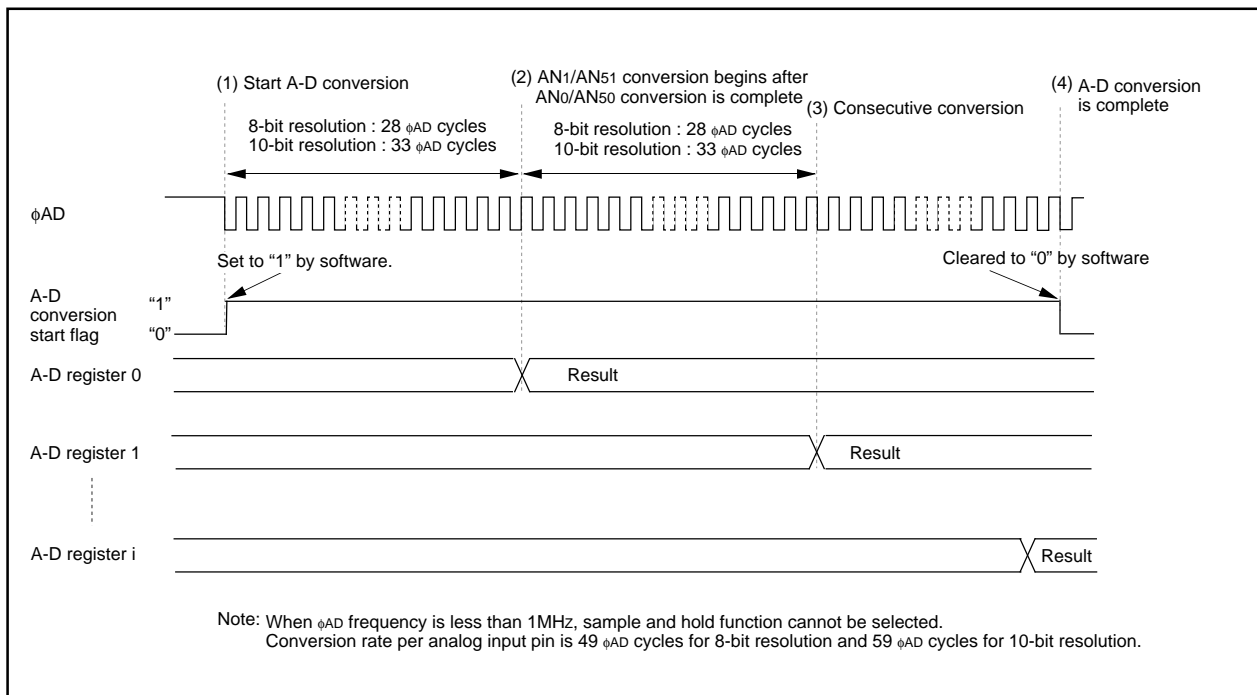


Figure 2.7.11. Operation timing of repeat sweep 0 mode

A-D Converter

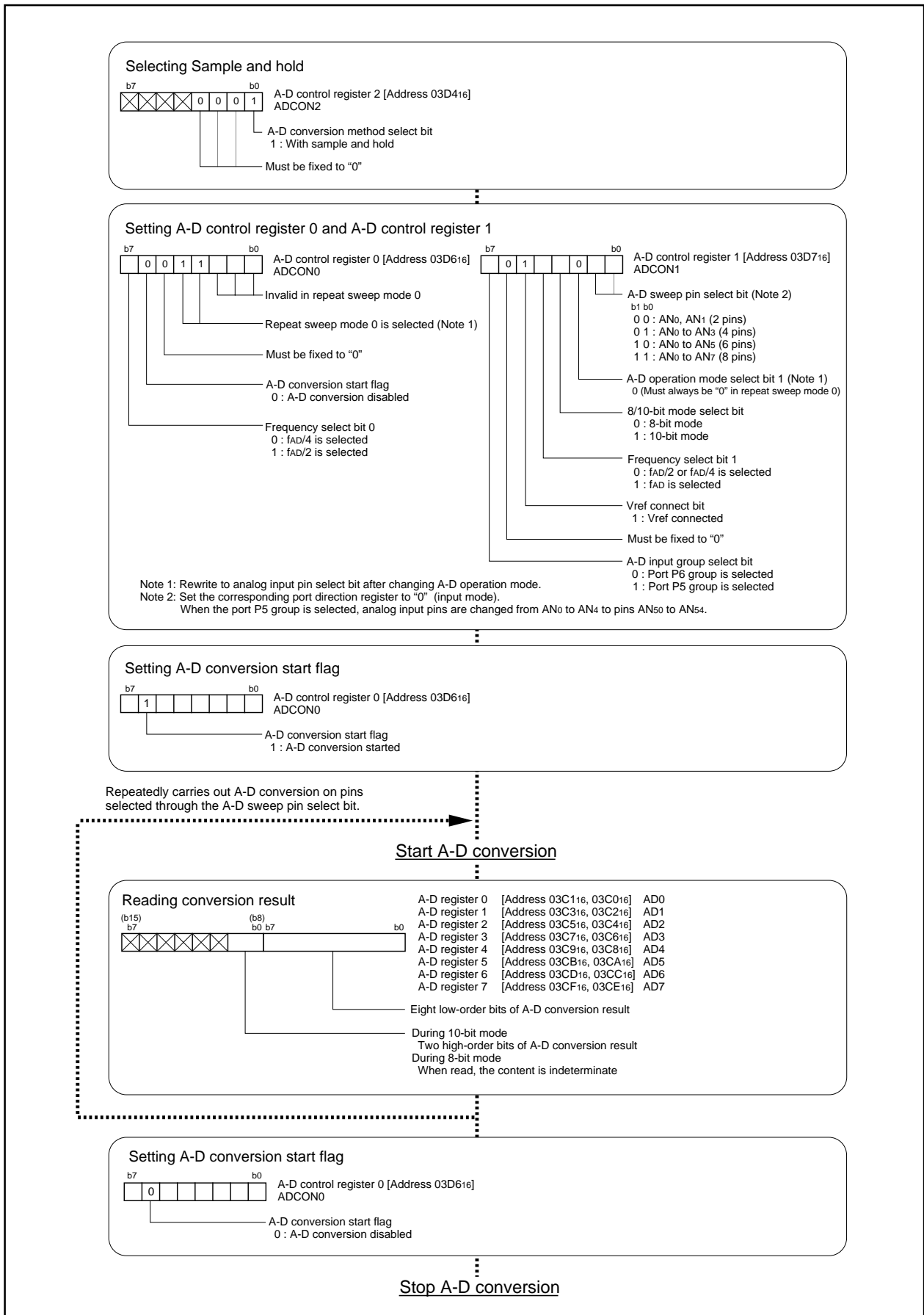


Figure 2.7.12. Set-up procedure of repeat sweep 0 mode

A-D Converter

2.7.6 Operation of A-D Converter (in repeat sweep mode 1)

In repeat sweep 1 mode, choose functions from those listed in Table 2.7.6. Operations of the circled items are described below. Figure 2.7.13 shows ANi pin's sweep sequence, Figure 2.7.14 shows timing chart, and Figure 2.7.15 shows the set-up procedure.

Table 2.7.6. Chosed functions

Item	Set-up
Operation clock ϕ_{AD}	○ Divided-by-4 f_{AD} / divided-by-2 f_{AD} / f_{AD}
Resolution	○ 8-bit / 10-bit
Analog input pin	○ AN0 (1 pins) / AN0 to AN1 (2 pins) / AN0 to AN2 (3 pins) / AN0 to AN3 (4 pins) (Note)
Sample & Hold	Not activated
	○ Activated

Note : When the port P5 group is selected, analog input pins are changed from AN0 to AN4 to pins AN50 to AN54.

- Operation
- (1) Setting the A-D conversion start flag to "1" causes the A-D converter to start the conversion on voltage input to the AN0/AN50 pin.
 - (2) After the A-D conversion on voltage input to the AN0/AN50 pin is completed, the content of the successive comparison register (conversion result) is transmitted to A-D register 0.
 - (3) Every time the A-D converter carries out A-D conversion on a selected analog input pin, the A-D converter carries out A-D conversion on only one unselected pin, and then the A-D converter carries out A-D conversion from the AN0 pin again. (See Figure 2.7.13.) The conversion result is transmitted to A-D register i every time conversion on a pin is completed. The A-D conversion interrupt request bit does not go to "1".
 - (4) The A-D converter continues operating until software goes the A-D conversion start flag to "0".

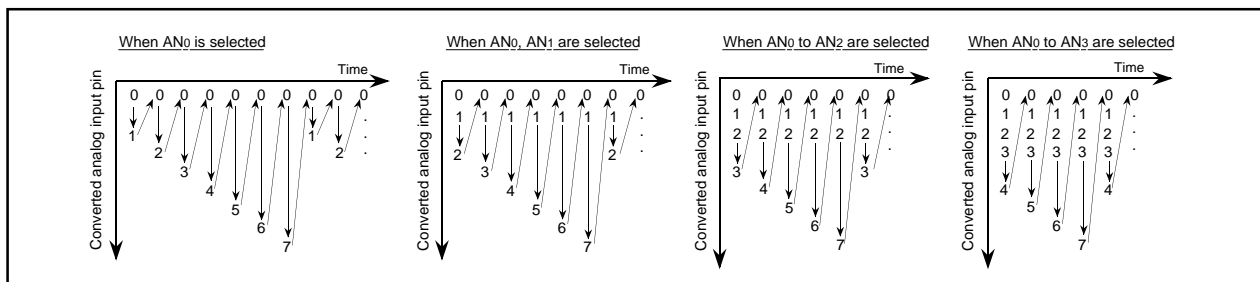


Figure 2.7.13. ANi pin's sweep sequence in repeat sweep mode

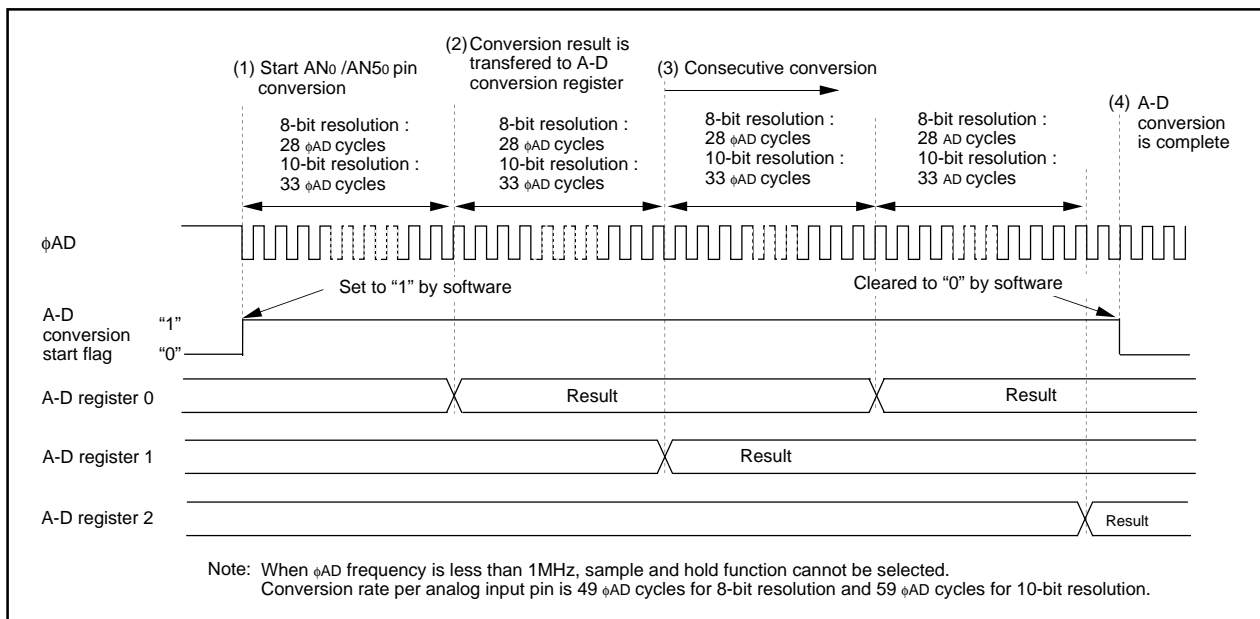


Figure 2.7.14. Operation timing of repeat sweep 1 mode

A-D Converter

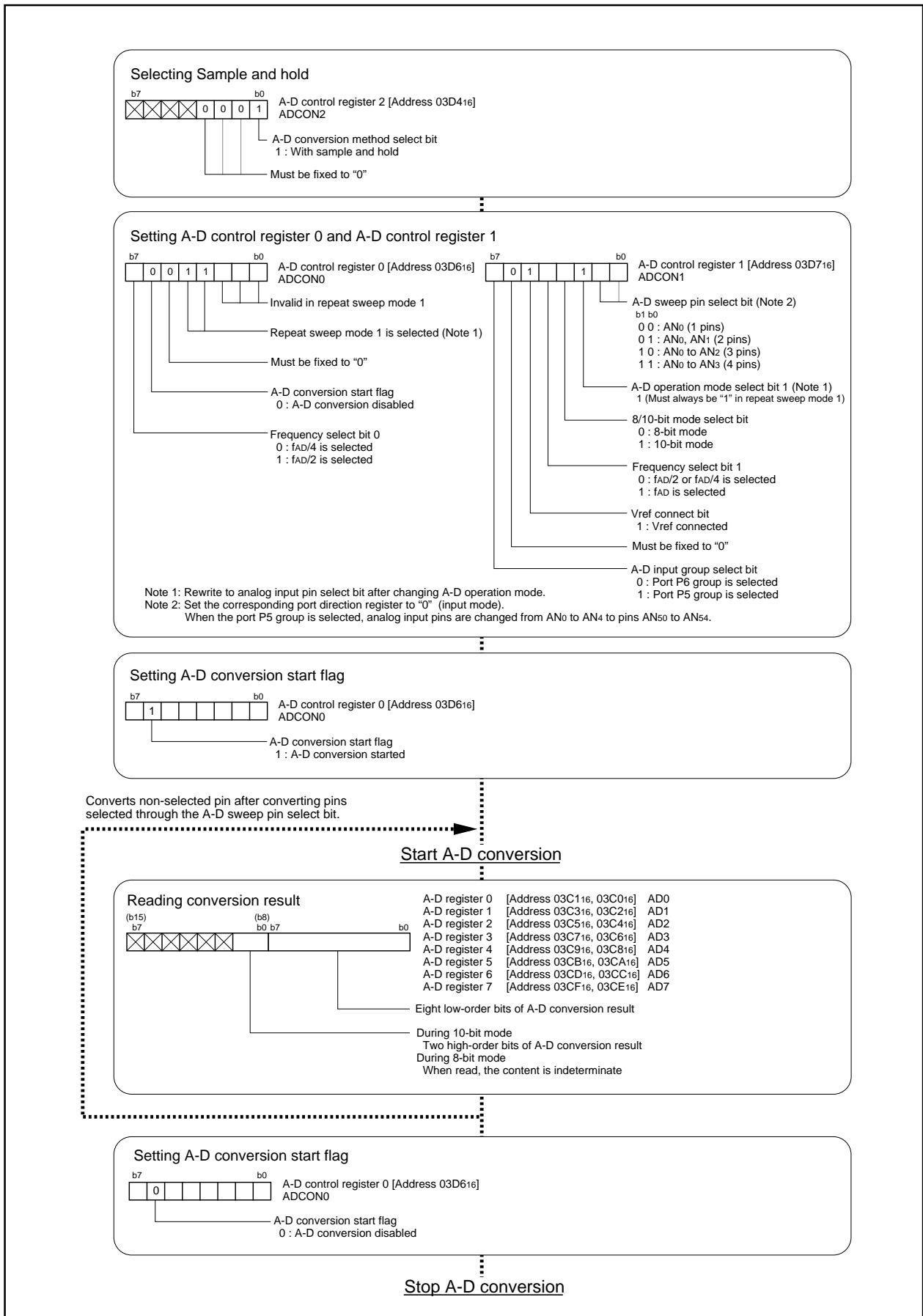


Figure 2.7.15. Set-up procedure of repeat sweep 1 mode

2.7.7 Precautions for A-D Converter

- (1) Write to each bit (except bit 6) of A-D control register 0, to each bit of A-D control register 1, and to bit 0 of A-D control register 2 when A-D conversion is stopped (before a trigger occurs).
 In particular, when the Vref connection bit is changed from 0 to 1, start A-D conversion after an elapse of 1 μ s or longer.
- (2) To reduce conversion error due to noise, connect a voltage to the AVcc pin and to the Vref pin from an independent source. It is recommended to connect a capacitor between the AVss pin and the AVcc pin, between the AVss pin and the Vref pin, and between the AVss pin and the analog input pin (ANi/AN5i). Figure 2.7.16 shows the an example of connecting the capacitors to these pins.

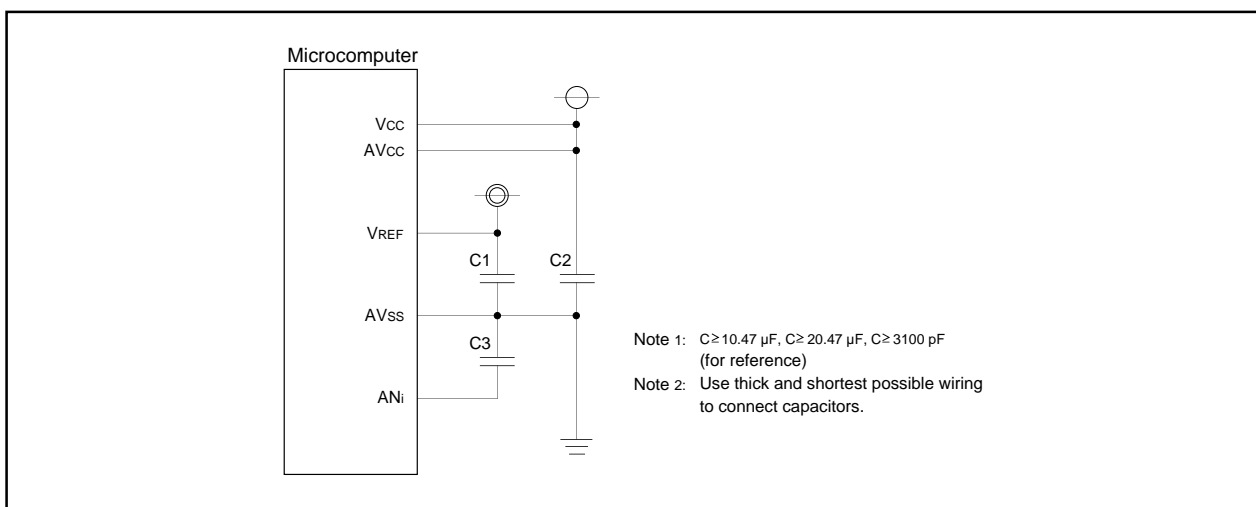


Figure 2.7.16. Use of capacitors to reduce noise

- (3) Set the direction register of the following ports to input: the port corresponding to a pin to be used as an analog input pin and external trigger input pin.
- (4) If using the A-D converter with $V_{cc} = 2.7V$ to $4.0V$:
 Use without fAD (no frequency division) for ϕ_{AD} .
 Select without the Sample & Hold feature.
 Select 8-bit mode.
- (5) Rewrite to analog input pin after changing A-D operation mode. The two cannot be set at the same time.
- (6) When using the one-shot or single sweep mode
 Confirm that A-D conversion is complete before reading the A-D register.
 (Note: When A-D conversion interrupt request bit is set, it shows that A-D conversion is completed.)
- (7) When using the repeat mode or repeat sweep mode 0 or 1
 Use the undivided main clock as the internal CPU clock.

2.7.8 Method of A-D Conversion (10-bit mode)

(1) The A-D converter compares the reference voltage (Vref) generated internally based on the contents of the successive comparison register with the analog input voltage (VIN) input from the analog input pin. Each bit of the comparison result is stored in the successive comparison register until analog-to-digital conversion (successive comparison method) is complete. If a trigger occurs, the A-D converter carries out the following:

1. Fixes bit 9 of the successive comparison register.

Compares Vref with VIN: [In this instance, the contents of the successive comparison register are "1000000002" (default).]

Bit 9 of the successive comparison register varies depending on the comparison result as follows.

If $V_{ref} < V_{IN}$, then "1" is assigned to bit 9.

If $V_{ref} > V_{IN}$, then "0" is assigned to bit 9.

2. Fixes bit 8 of the successive comparison register.

Sets bit 8 of the successive comparison register to "1", then compares Vref with VIN.

Bit 8 of the successive comparison register varies depending on the comparison result as follows:

If $V_{ref} < V_{IN}$, then "1" is assigned to bit 8.

If $V_{ref} > V_{IN}$, then "0" is assigned to bit 8.

3. Fixes bit 7 through bit 0 of the successive comparison register.

Carries out step 2 above on bit 7 through bit 0.

After bit 0 is fixed, the contents of the successive comparison register (conversion result) are transmitted to A-D register i.

Vref is generated based on the latest content of the successive comparison register. Table 2.7.7 shows the relationship of the successive comparison register contents and Vref. Table 2.7.8 shows how the successive comparison register and Vref vary while A-D conversion is in progress. Figure 2.7.17 shows theoretical A-D conversion characteristics.

Table 2.7.7. Relationship of the successive comparison register contents and Vref

Successive approximation register : n	Vref (V)
0	0
1 to 1023	$\frac{V_{REF}}{1024} \times n - \frac{V_{REF}}{2048}$

A-D Converter

Table 2.7.8. Variation of the successive comparison register and Vref while A-D conversion is in progress (10-bit mode)

	Successive approximation register	Vref change																						
A-D converter stopped	<table border="1" style="width: 100%; text-align: center;"> <tr> <td>b9</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>b0</td> </tr> <tr> <td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td> </tr> </table>	b9										b0	1	0	0	0	0	0	0	0	0	0	0	$\frac{V_{REF}}{2}$ [V]
b9										b0														
1	0	0	0	0	0	0	0	0	0	0														
1st comparison	<table border="1" style="width: 100%; text-align: center;"> <tr> <td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td> </tr> </table>	1	0	0	0	0	0	0	0	0	0	0	$\frac{V_{REF}}{2} - \frac{V_{REF}}{2048}$ [V]											
1	0	0	0	0	0	0	0	0	0	0														
2nd comparison	<table border="1" style="width: 100%; text-align: center;"> <tr> <td>n9</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td> </tr> </table> <p style="text-align: center;">↑ 1st comparison result</p>	n9	1	0	0	0	0	0	0	0	0	0	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} - \frac{V_{REF}}{2048}$ [V] $\left(\begin{matrix} n_9 = 1 & + & \frac{V_{REF}}{4} \\ n_9 = 0 & - & \frac{V_{REF}}{4} \end{matrix} \right)$											
n9	1	0	0	0	0	0	0	0	0	0														
3rd comparison	<table border="1" style="width: 100%; text-align: center;"> <tr> <td>n9</td><td>n8</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td> </tr> </table> <p style="text-align: center;">↑ 2nd comparison result</p>	n9	n8	1	0	0	0	0	0	0	0	0	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} \pm \frac{V_{REF}}{8} - \frac{V_{REF}}{2048}$ [V] $\left(\begin{matrix} n_8 = 1 & + & \frac{V_{REF}}{8} \\ n_8 = 0 & - & \frac{V_{REF}}{8} \end{matrix} \right)$											
n9	n8	1	0	0	0	0	0	0	0	0														
⋮	⋮	⋮																						
10th comparison	<table border="1" style="width: 100%; text-align: center;"> <tr> <td>n9</td><td>n8</td><td>n7</td><td>n6</td><td>n5</td><td>n4</td><td>n3</td><td>n2</td><td>n1</td><td>0</td> </tr> </table>	n9	n8	n7	n6	n5	n4	n3	n2	n1	0	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} \pm \frac{V_{REF}}{8} \pm \dots \pm \frac{V_{REF}}{1024} - \frac{V_{REF}}{2048}$ [V]												
n9	n8	n7	n6	n5	n4	n3	n2	n1	0															
Conversion complete	<table border="1" style="width: 100%; text-align: center;"> <tr> <td>n9</td><td>n8</td><td>n7</td><td>n6</td><td>n5</td><td>n4</td><td>n3</td><td>n2</td><td>n1</td><td>n0</td> </tr> </table> <p style="text-align: center;">This data transfers to the bit 0 to bit 9 of A-D register.</p>	n9	n8	n7	n6	n5	n4	n3	n2	n1	n0													
n9	n8	n7	n6	n5	n4	n3	n2	n1	n0															

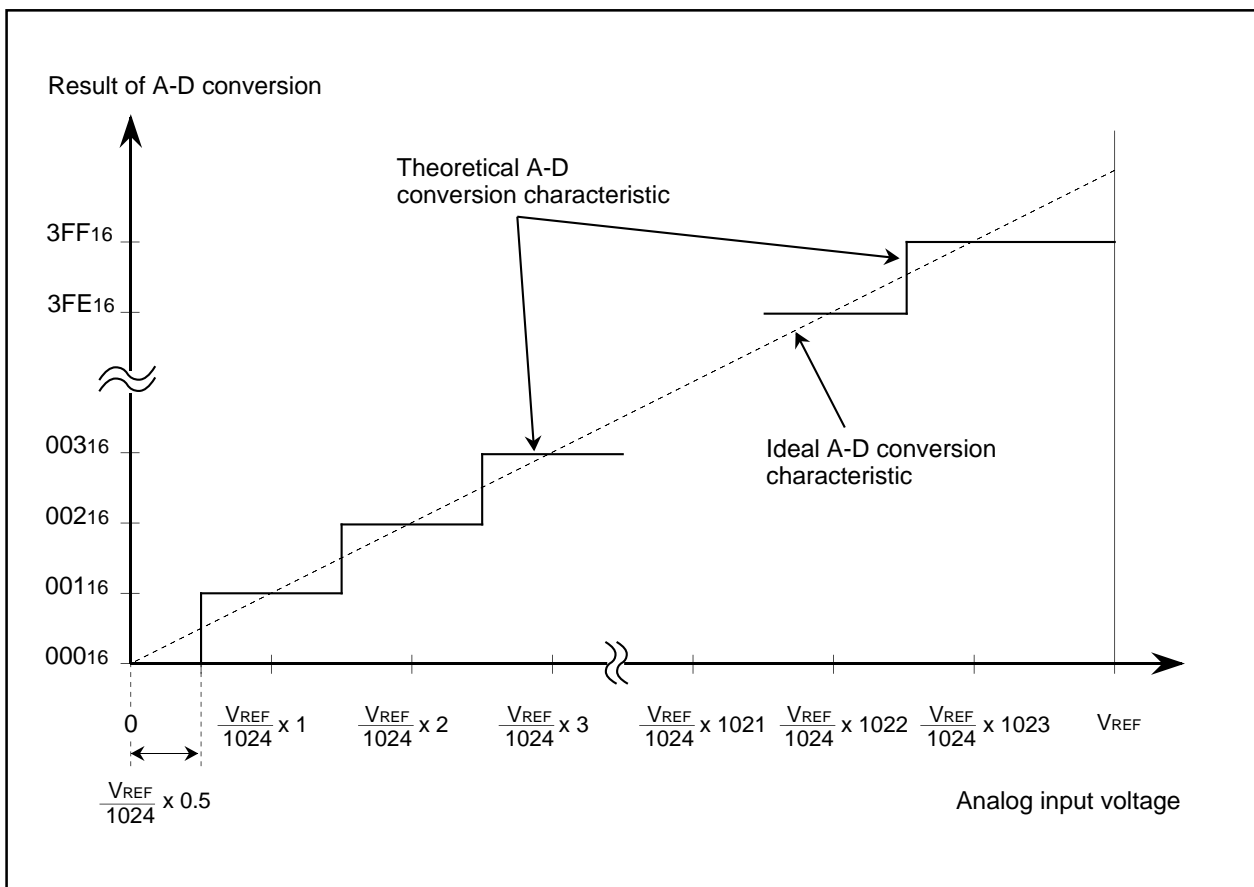


Figure 2.7.17. Theoretical A-D conversion characteristics (10-bit mode)

A-D Converter

2.7.9 Method of A-D Conversion (8-bit mode)

(1) In 8-bit mode, 8 higher-order bits of the 10-bit successive comparison register becomes A-D conversion result. Hence, if compared to a result obtained by using an 8-bit A-D converter, the voltage compared is different by $3 V_{REF}/2048$ (see what are underscored in Table 2.7.9), and differences in stepping points of output codes occur as shown in Figure 2.7.18.

Table 2.7.9. The comparison voltage in 8-bit mode compared to 8-bit A-D converter

		8-bit mode	8-bit A-D converter
Comparison voltage V_{ref}	n = 0	0	0
	n = 1 to 255	$\frac{V_{REF}}{2^8} \times n - \frac{V_{REF}}{2^{10}} \times 0.5$	$\frac{V_{REF}}{2^8} \times n - \frac{V_{REF}}{2^8} \times 0.5$

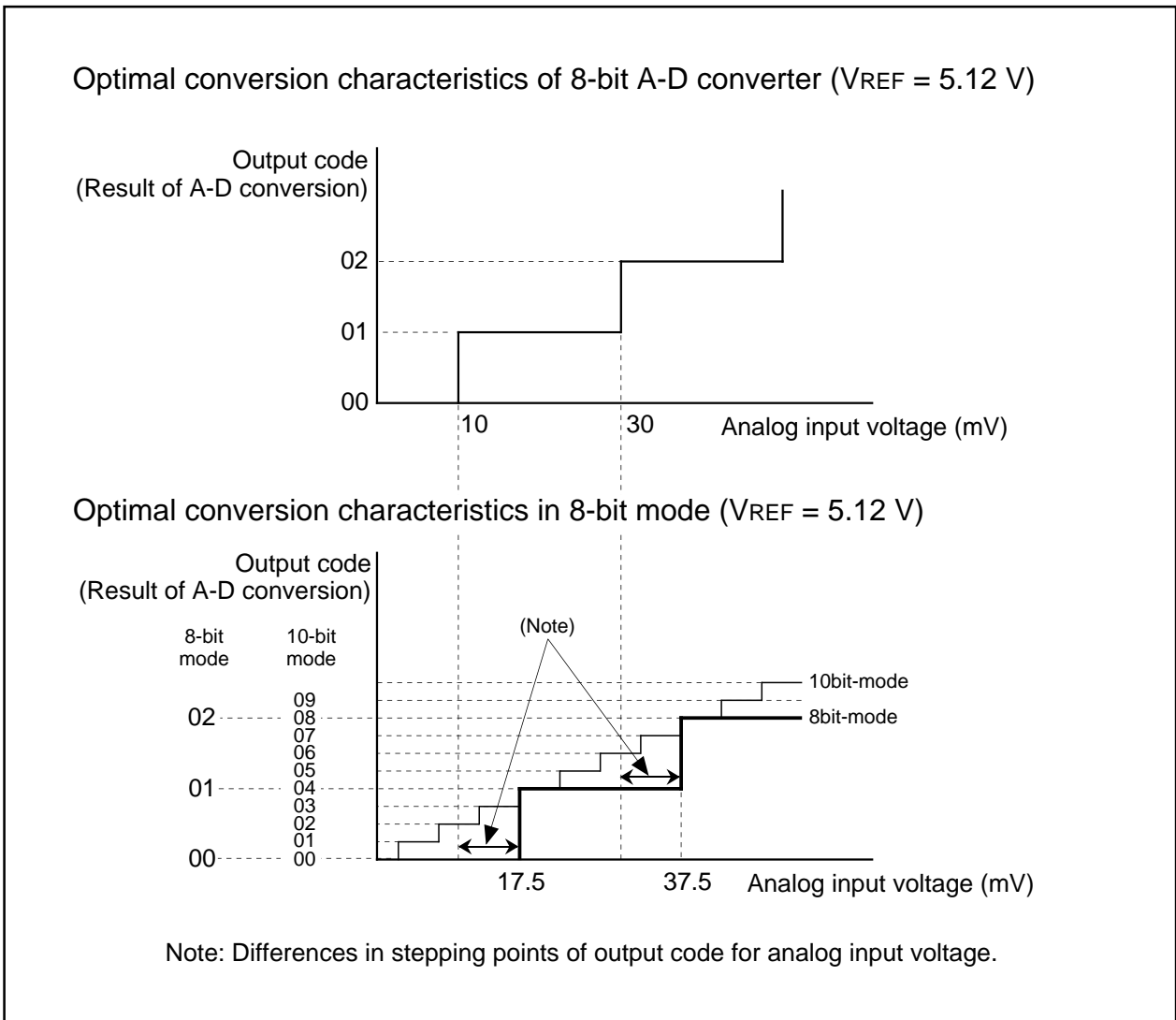


Figure 2.7.18. The level conversion characteristics of 8-bit mode and 8-bit A-D converter

A-D Converter

Table 2.7.10. Variation of the successive comparison register and Vref while A-D conversion is in progress (8-bit mode)

	Successive approximation register	Vref change
A-D converter stopped	$\begin{matrix} b9 & & & & & & & & & & b0 \\ \hline 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{matrix}$	$\frac{V_{REF}}{2}$ [V]
1st comparison	$\begin{matrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{matrix}$	$\frac{V_{REF}}{2} - \frac{V_{REF}}{2048}$ [V]
2nd comparison	$\begin{matrix} n9 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \uparrow & & & & & & & & & & \\ \text{1st comparison result} & & & & & & & & & & \end{matrix}$	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} - \frac{V_{REF}}{2048}$ [V] $\begin{matrix} (n9 = 1 & + & \frac{V_{REF}}{4}) \\ (n9 = 0 & - & \frac{V_{REF}}{4}) \end{matrix}$
3rd comparison	$\begin{matrix} n9 & n8 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \uparrow & \uparrow & & & & & & & & & \\ \text{2nd comparison result} & & & & & & & & & & \end{matrix}$	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} \pm \frac{V_{REF}}{8} - \frac{V_{REF}}{2048}$ [V] $\begin{matrix} (n8 = 1 & + & \frac{V_{REF}}{8}) \\ (n8 = 0 & - & \frac{V_{REF}}{8}) \end{matrix}$
⋮	⋮	⋮
8th comparison	$\begin{matrix} n9 & n8 & n7 & n6 & n5 & n4 & n3 & 1 & 0 & 0 & 0 \end{matrix}$	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} \pm \frac{V_{REF}}{8} \pm \dots \pm \frac{V_{REF}}{256} - \frac{V_{REF}}{2048}$ [V]
Conversion complete	$\begin{matrix} n9 & n8 & n7 & n6 & n5 & n4 & n3 & n2 & 0 & 0 & 0 \end{matrix}$ <p>This data transfers to bit 0 to bit 7 of A-D register.</p>	

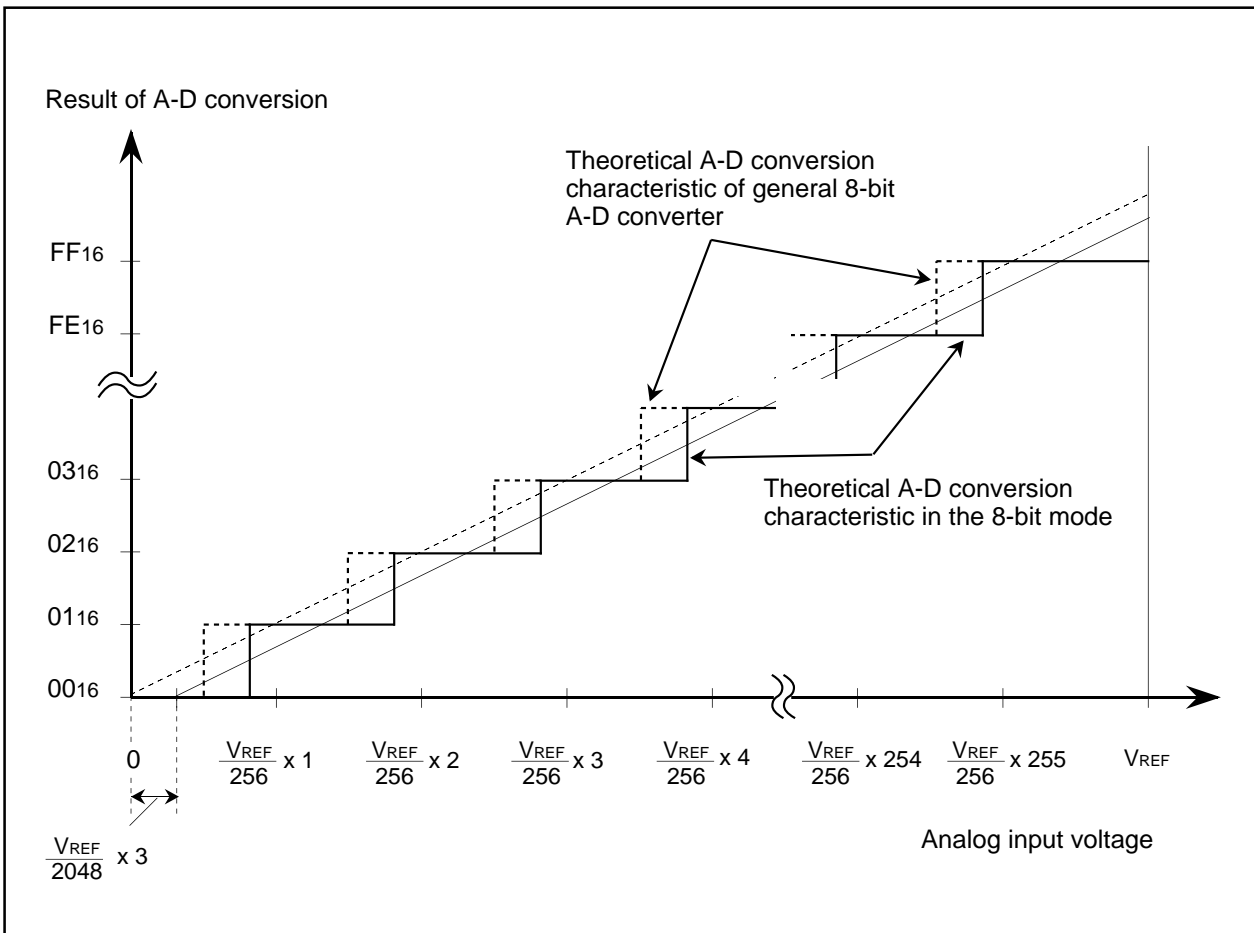


Figure 2.7.19. Theoretical A-D conversion characteristics (8-bit mode)

A-D Converter

2.7.10 Absolute Accuracy and Differential Non-Linearity Error

• Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A-D conversion characteristics, and actual A-D conversion result. When measuring absolute accuracy, the voltage at the middle point of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A-D conversion characteristics, is used as an analog input voltage. For example, if 10-bit resolution is used and if V_{REF} (reference voltage) = 5.12 V, then 1-LSB width becomes 5 mV, and 0 mV, 5 mV, 10 mV, 15 mV, 20 mV, ... are used as analog input voltages. If analog input voltage is 25 mV, "absolute accuracy = $\pm 3\text{LSB}$ " refers to the fact that actual A-D conversion falls on a range from "002₁₆" to "008₁₆" though an output code, "005₁₆", can be expected from the theoretical A-D conversion characteristics. Zero error and full-scale error are included in absolute accuracy.

Also, all the output codes for analog input voltage between V_{REF} and V_{CC} becomes "3FF₁₆".

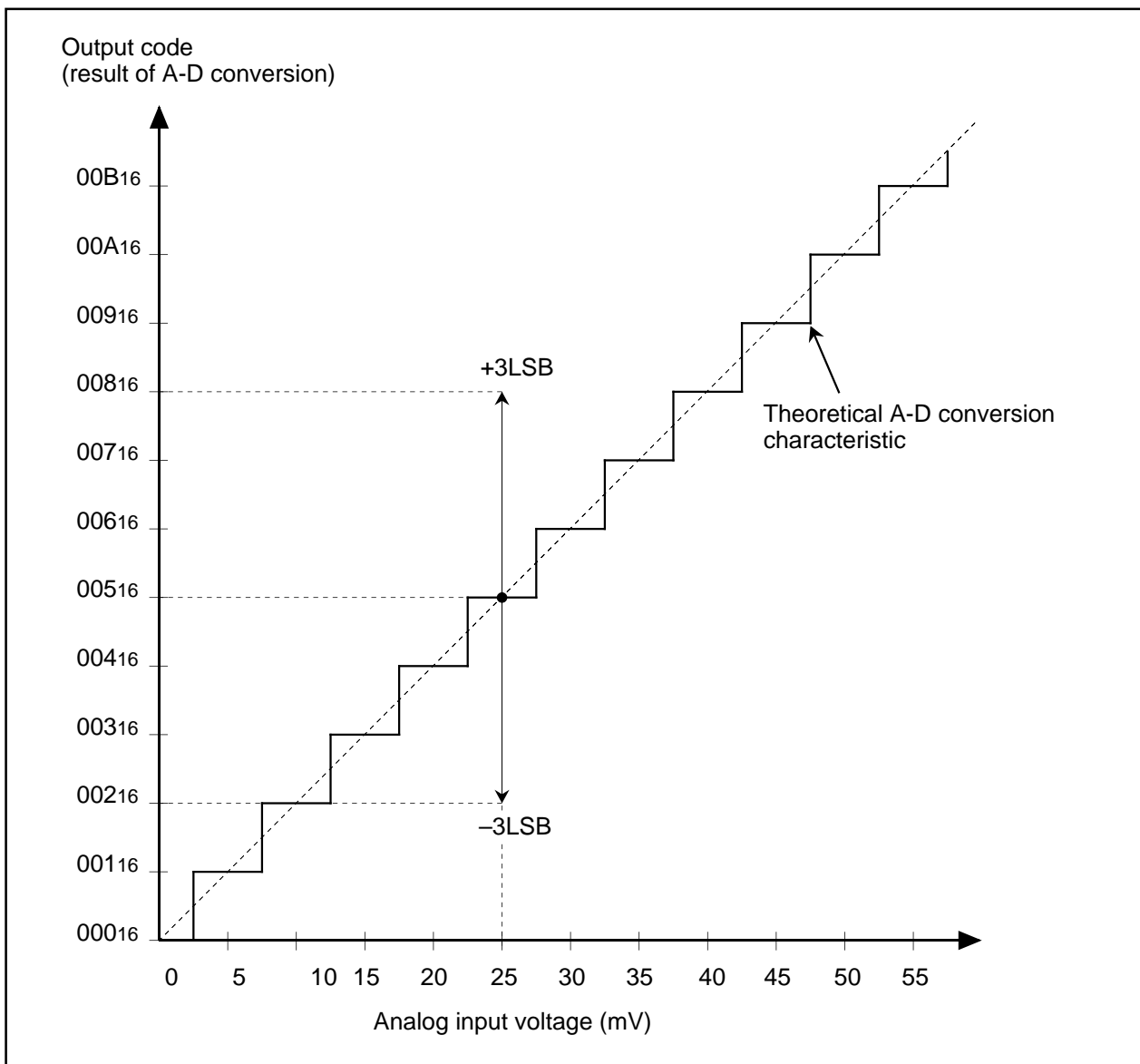


Figure 2.7.20. Absolute accuracy (10-bit resolution)

A-D Converter

• Differential non-linearity error

Differential non-linearity error refers to the difference between 1-LSB width based on the theoretical A-D conversion characteristics (an analog input width that can meet the expectation of outputting an equal code) and an actually measured 1-LSB width (analog input voltage width that outputs an equal code). If 10-bit resolution is used and if V_{REF} (reference voltage) = 5.12 V, "differential non-linearity error = ± 1 LSB" refers to the fact that 1-LSB width actually measured falls on a range from 0 mV to 10 mV though 1-LSB width based on the theoretical A-D conversion characteristics is 5 mV (see 5.2 A-D converter's standard characteristics).

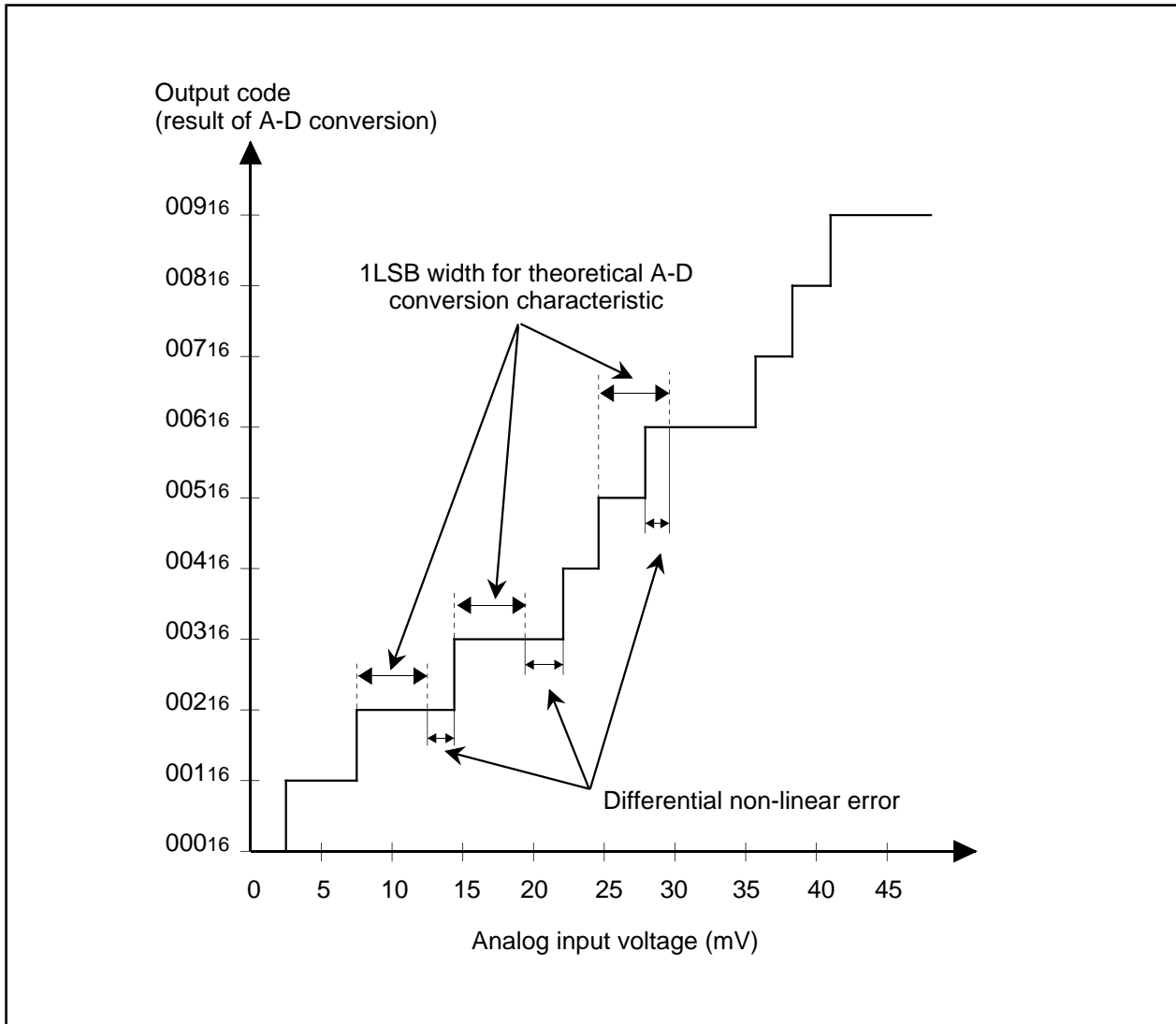


Figure 2.7.21. Differential non-linearity error (10-bit resolution)

A-D Converter

2.7.11 Internal Equivalent Circuit of Analog Input

Figure 2.7.22 shows the internal equivalent circuit of analog input.

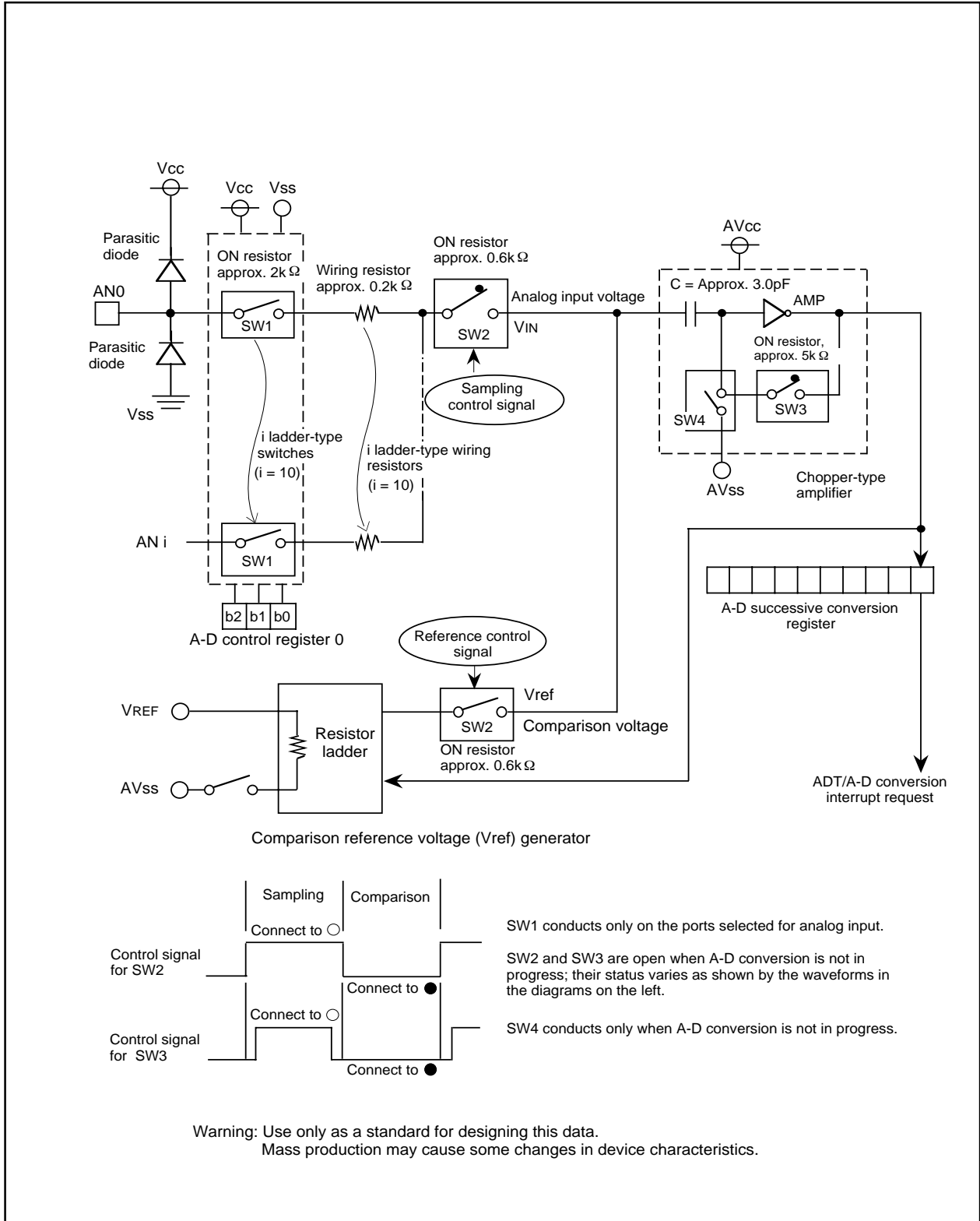


Figure 2.7.22. Internal equivalent circuit to analog input

2.7.12 Sensor's Output Impedance under A-D Conversion

To carry out A-D conversion properly, charging the internal capacitor C shown in Figure 2.7.23 has to be completed within a specified period of time. With T as the specified time, time T is the time that switches SW2 and SW3 are connected to O in Figure 2.7.22. Let output impedance of sensor equivalent circuit be R₀, microcomputer's internal resistance be R, precision (error) of the A-D converter be X, and the A-D converter's resolution be Y (Y is 1024 in the 10-bit mode, and 256 in the 8-bit mode).

$$V_c \text{ is generally } V_c = V_{IN} \left\{ 1 - e^{-\frac{t}{C(R_0 + R)}} \right\}$$

$$\text{And when } t = T, \quad V_c = V_{IN} - \frac{X}{Y} V_{IN} = V_{IN} \left(1 - \frac{X}{Y} \right)$$

$$e^{-\frac{T}{C(R_0 + R)}} = \frac{X}{Y}$$

$$-\frac{T}{C(R_0 + R)} = \ln \frac{X}{Y}$$

$$\text{Hence, } R_0 = -\frac{T}{C \cdot \ln \frac{X}{Y}} - R$$

With the model shown in Figure 2.7.29 as an example, when the difference between V_{IN} and V_c becomes 0.1LSB, we find impedance R₀ when voltage between pins V_c changes from 0 to V_{IN} - (0.1/1024) V_{IN} in time T. (0.1/1024) means that A-D precision drop due to insufficient capacitor charge is held to 0.1LSB at time of A-D conversion in the 10-bit mode. Actual error however is the value of absolute precision added to 0.1LSB. When f(X_{IN}) = 10 MHz, T = 0.3 μs in the A-D conversion mode with sample & hold. Output impedance R₀ for sufficiently charging capacitor C within time T is determined as follows.

T = 0.3 μs, R = 7.8 kΩ, C = 3 pF, X = 0.1, and Y = 1024. Hence,

$$R_0 = -\frac{0.3 \times 10^{-6}}{3.0 \times 10^{-12} \cdot \ln \frac{0.1}{1024}} - 7.8 \times 10^3 \approx 3.0 \times 10^3$$

Thus, the allowable output impedance of the sensor circuit capable of thoroughly driving the A-D converter turns out to be approximately 3.0 kΩ. Tables 2.7.11 and 2.7.12 show output impedance values based on the LSB values.

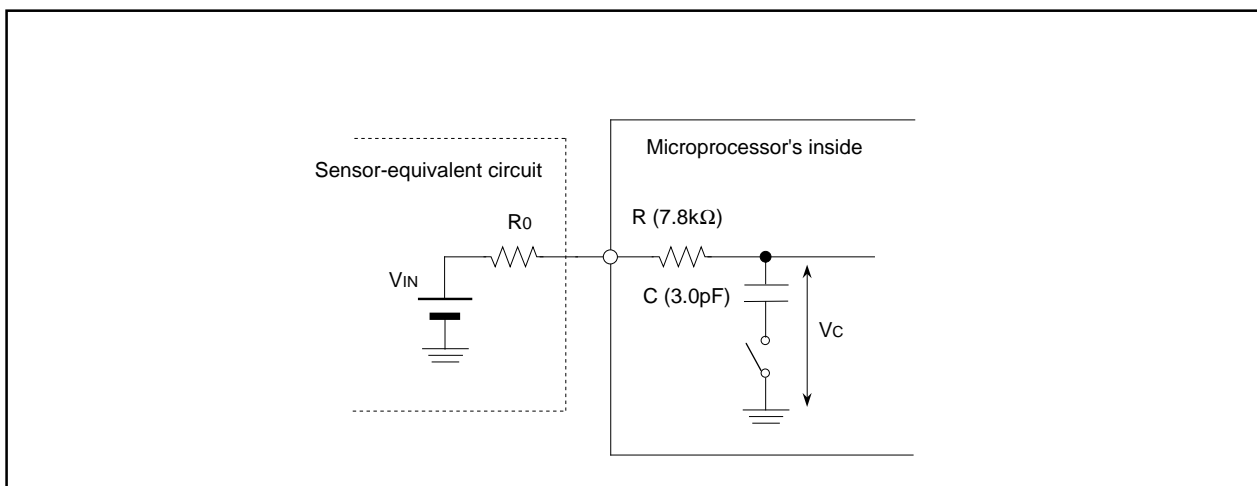


Figure 2.7.23 A circuit equivalent to the A-D conversion terminal

A-D Converter

Tables 2.7.11. Relation between output impedance and precision (error) of A-D converter (10-bit mode) Reference value

f(Xin) (MHz)	Cycle	Sampling time	R	C (pF)	Resolution (LSB)	R0
10	0.1	0.3 (3 x cycle, Sample & hold bit is enabled)	7.8	3.0	0.1	3.0
					0.3	4.5
					0.5	5.3
					0.7	5.9
					0.9	6.4
					1.1	6.8
					1.3	7.2
					1.5	7.5
					1.7	7.8
10	0.1	0.2 (2 x cycle, Sample & hold bit is disabled)	7.8	3.0	0.3	0.4
					0.5	0.9
					0.7	1.3
					0.9	1.7
					1.1	2.0
					1.3	2.2
					1.5	2.4
					1.7	2.6
					1.9	2.8

Tables 2.7.12. Relation between output impedance and precision (error) of A-D converter (8-bit mode) Reference value

f(Xin) (MHz)	Cycle	Sampling time	R	C (pF)	Resolution (LSB)	R0
10	0.1	0.3 (3 x cycle, Sample & hold bit is enabled)	7.8	3.0	0.1	4.9
					0.3	7.0
					0.5	8.2
					0.7	9.1
					0.9	9.9
					1.1	10.5
					1.3	11.1
					1.5	11.7
					1.7	12.1
10	0.1	0.2 (2 x cycle, Sample & hold bit is disabled)	7.8	3.0	0.1	0.7
					0.3	2.1
					0.5	2.9
					0.7	3.5
					0.9	4.0
					1.1	4.4
					1.3	4.8
					1.5	5.2
					1.7	5.5
1.9	5.8					

Watchdog Timer

2.8 Watchdog Timer

2.8.1 Overview

The watchdog timer can detect a runaway program using its 15-bit timer prescaler. The following is an overview of the watchdog timer.

(1) Watchdog timer start procedure

When reset, the watchdog timer is in stopped state. Writing to the watchdog timer start register initializes the watchdog timer to 7FFF₁₆ and causes it to start performing a down count. The watchdog timer, once started operating, cannot be stopped by any means other than stopping conditions.

(2) Watchdog timer stop conditions

The watchdog timer stops in any one of the following states:

- (a) Period in which the CPU is in stopped state
- (b) Period in which the CPU is in waiting state

(3) Watchdog timer initialization

The watchdog timer is initialized to 7FFF₁₆ in the cases given below, and begins a down count.

- (a) When the watchdog timer writes to the watchdog timer start register while a count is in progress
- (b) When the watchdog timer underflows

(4) Runaway detection

When the watchdog timer underflows, a watchdog timer interrupt occurs. In writing a program, write to the watchdog timer start register before the watchdog timer underflows. The watchdog timer interrupt occurs regardless of the status of the interrupt enable flag (I flag). In processing a watchdog timer interrupt, set the software reset bit to "1" to reset software.

(5) Watchdog timer cycle

The watchdog timer cycle varies depending on the BCLK and the frequency division ratio of the prescaler selected.

Table 2.8.1. The watchdog timer cycle

CM07	CM06	CM17	CM16	BCLK	WDC7	Period
0	0	0	0	10MHz	0	Approx. 52.4ms (Note)
					1	Approx. 419.2ms (Note)
0	0	0	1	5MHz	0	Approx. 104.9ms (Note)
					1	Approx. 838.8ms (Note)
0	0	1	0	2.5MHz	0	Approx. 209.7ms (Note)
					1	Approx. 1.68s (Note)
0	0	1	1	0.625MHz	0	Approx. 838.8ms (Note)
					1	Approx. 6.71s (Note)
0	1	Invalid	Invalid	1.25MHz	0	Approx. 419.2ms (Note)
					1	Approx. 3.35s (Note)
1	Invalid	Invalid	Invalid	32kHz	Invalid	Approx. 2s (Note)

Note: An error due to the prescaler occurs.

Watchdog Timer

(6) Registers related to the watchdog timer

Figure 2.8.1 shows the memory map of watchdog timer-related registers, and Figure 2.8.2 shows watchdog timer-related registers.

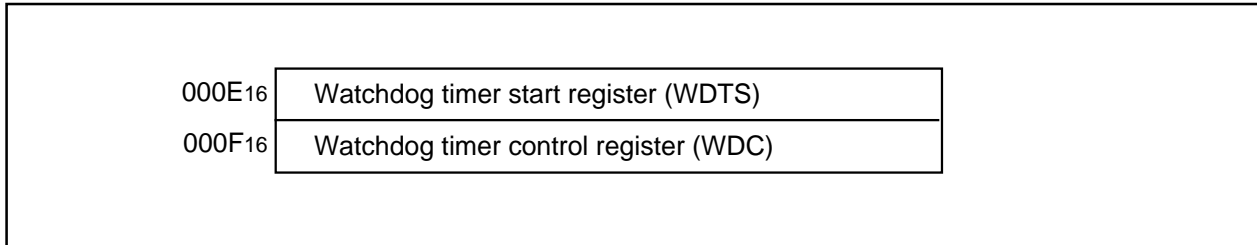


Figure 2.8.1. Memory map of watchdog timer-related registers

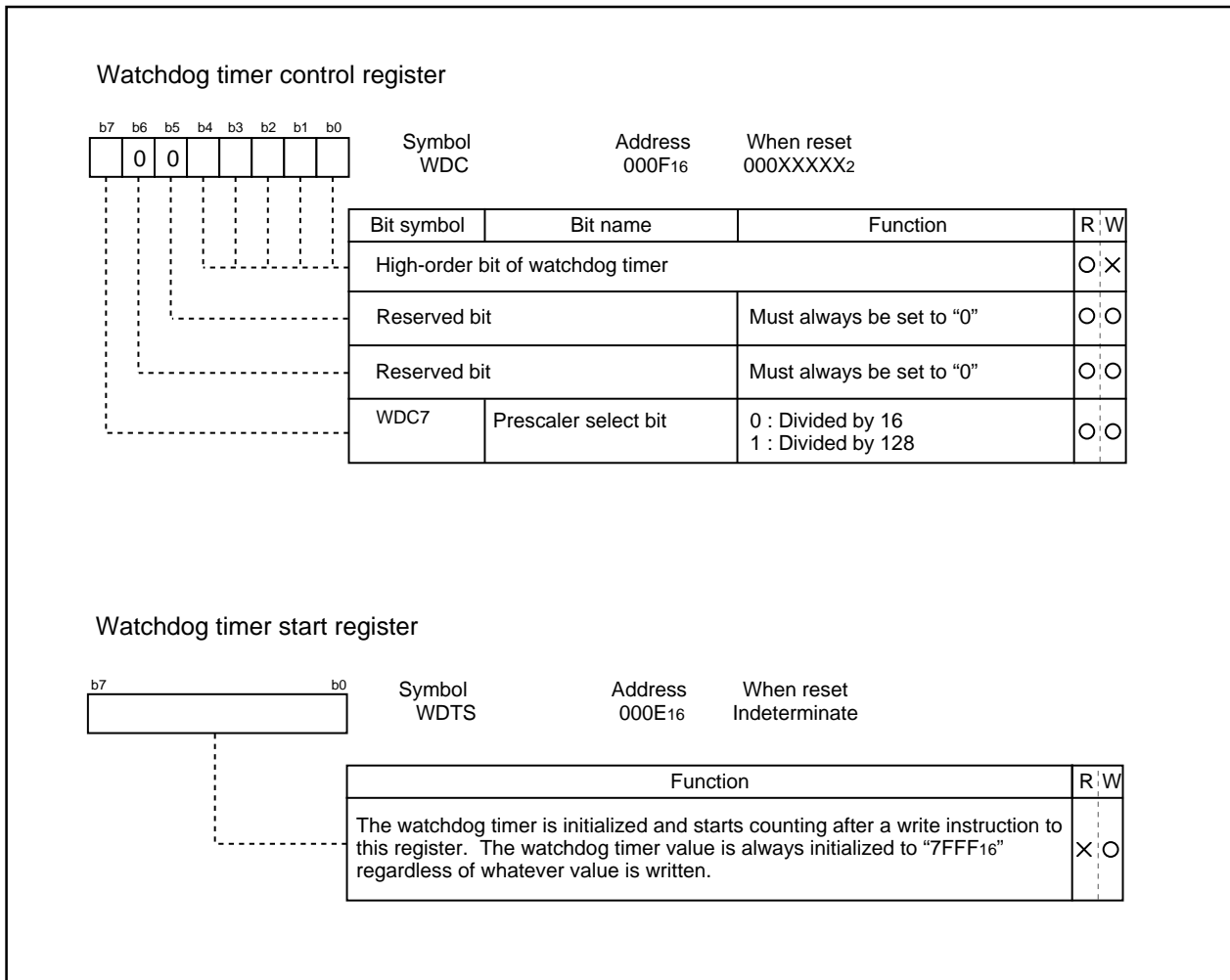


Figure 2.8.2. Watchdog timer-related registers

Watchdog Timer

2.8.2 Operation of Watchdog Timer

The following is an operation of the watchdog timer. Figure 2.8.3 shows the operation timing, and Figure 2.8.4 shows the set-up procedure.

- Operation
- (1) Writing to the watchdog timer start register initializes the watchdog timer to $7FFF_{16}$ and causes it to start a down count.
 - (2) With a count in progress, writing to the watchdog timer start register again initializes the watchdog timer to $7FFF_{16}$ and causes it to resume counting.
 - (3) Either executing the WAIT instruction or going to the stopped state causes the watchdog timer to hold the count in progress and to stop counting. The watchdog timer resumes counting after returning from the execution of the WAIT instruction or from the stopped state.
 - (4) If the watchdog timer underflows, it is initialized to $7FFF_{16}$ and continues counting. At this time, a watchdog timer interrupt occurs.

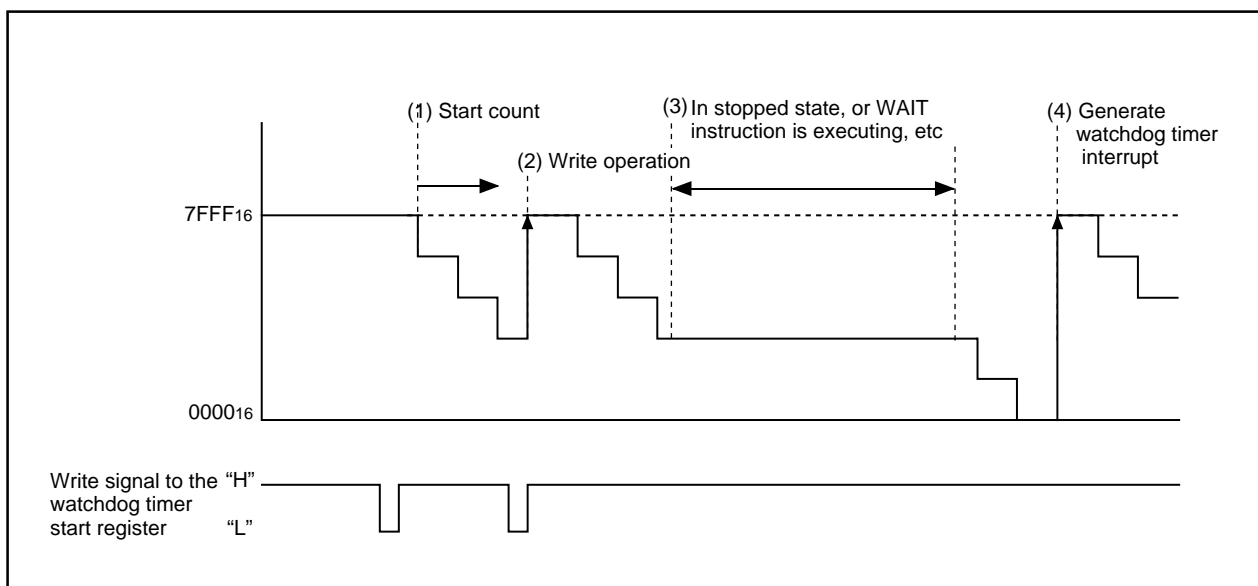


Figure 2.8.3. Operation timing of watchdog timer

Watchdog Timer

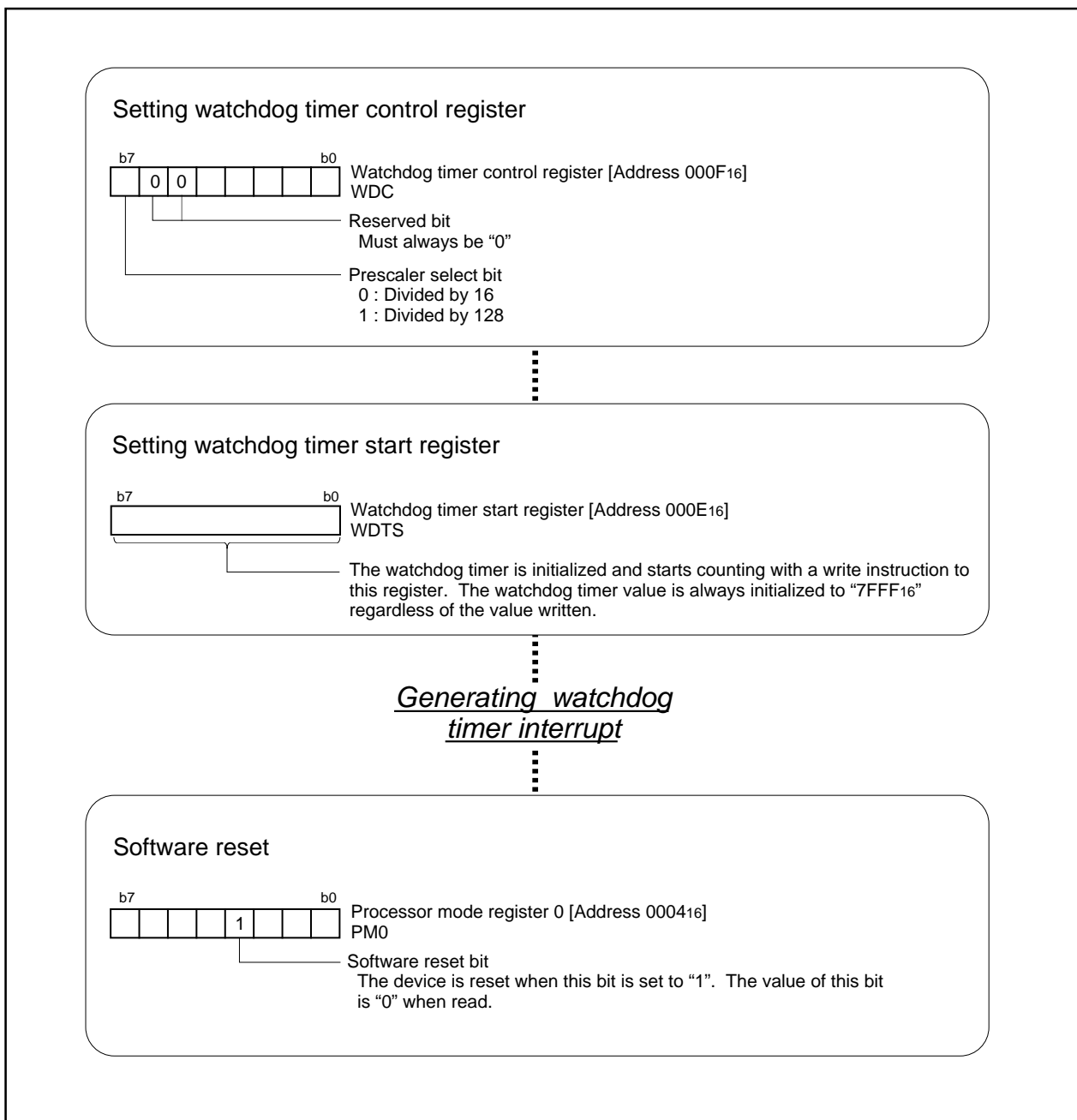


Figure 2.8.4. Set-up procedure of watchdog timer

Address Match Interrupt

2.9 Address Match Interrupt

2.9.1 Overview

The address match interrupt is used for correcting a ROM or for a simplified debugging-purpose monitor. The following is an overview of the address match interrupt.

(1) Enabling/disabling the address match interrupt

The address match interrupt enable bit can be used to enable and disable an address match interrupt. It is affected neither by the processor interrupt priority level (IPL) nor the interrupt enable flag (I flag).

(2) Timing of the address match interrupt

An interrupt occurs immediately before executing the instruction in the address indicated by the address match interrupt register. Set the first address of the instruction in the address match interrupt register. Setting a half address of an instruction or an address of tabulated data does not generate an address match interrupt.

The first instruction of an interrupt routine does not generate an address match interrupt either.

(3) Returning from an address match interrupt

The return address put in the stack when an address match interrupt occurs depends on the instruction not yet executed (the instruction the address match interrupt register indicates). The return address is not put in the stack. For this reason, to return from an address match interrupt, either rewrite the content of the stack and use the REIT instruction or use the POP instruction to restore the stack to the state as it was before the interrupt occurred and return by use of a jump instruction.

Figure 2.9.1 shows unexecuted instructions and corresponding the stacked addresses.

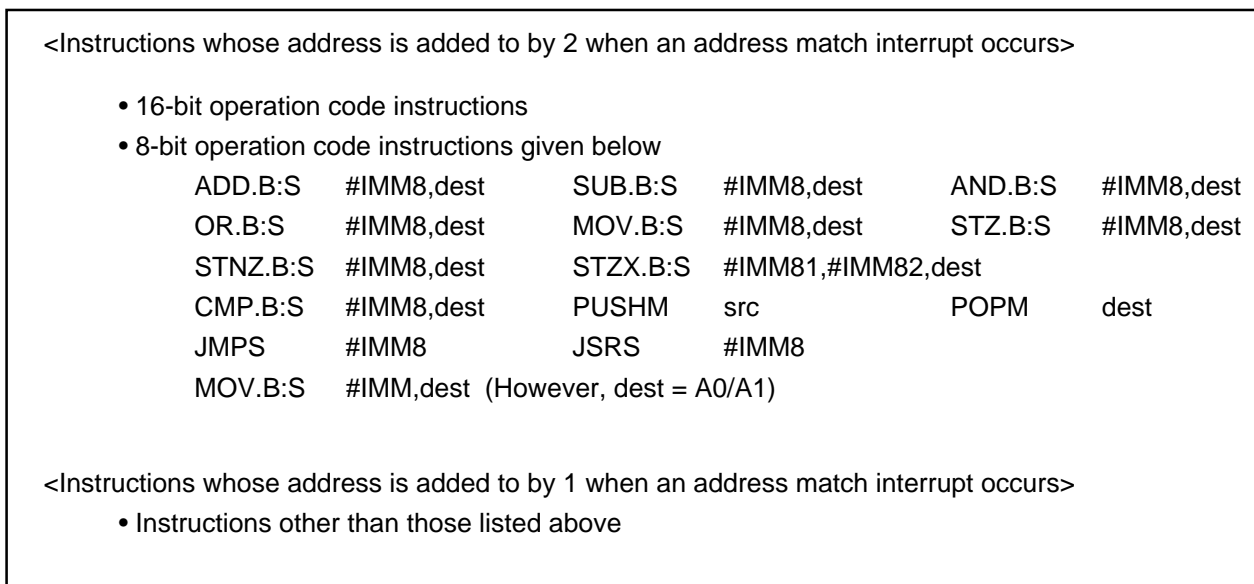


Figure 2.9.1. Unexecuted instructions and corresponding stacked addresses

(4) How to determine an address match interrupt

Address match interrupts can be set at two different locations. However, both location will have the same vector address. Therefore, it is necessary to determine which interrupt has occurred; address match interrupt 0 or address match interrupt 1. Using the content of the stack, etc., determine which interrupt has occurred according to the first part of the address match interrupt routine.

Address Match Interrupt

(5) Registers related to the address match interrupt

Figure 2.9.2 shows the memory map of address match interrupt-related registers, and Figure 2.9.3 shows address match interrupt-related registers.

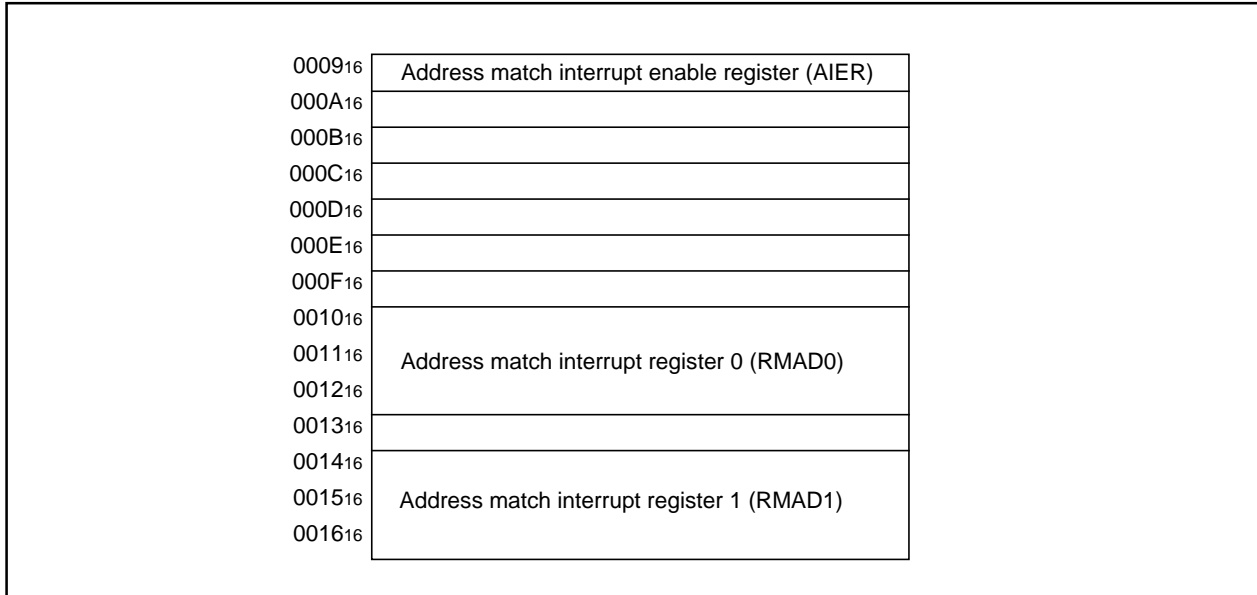


Figure 2.9.2. Memory map of address match interrupt-related registers

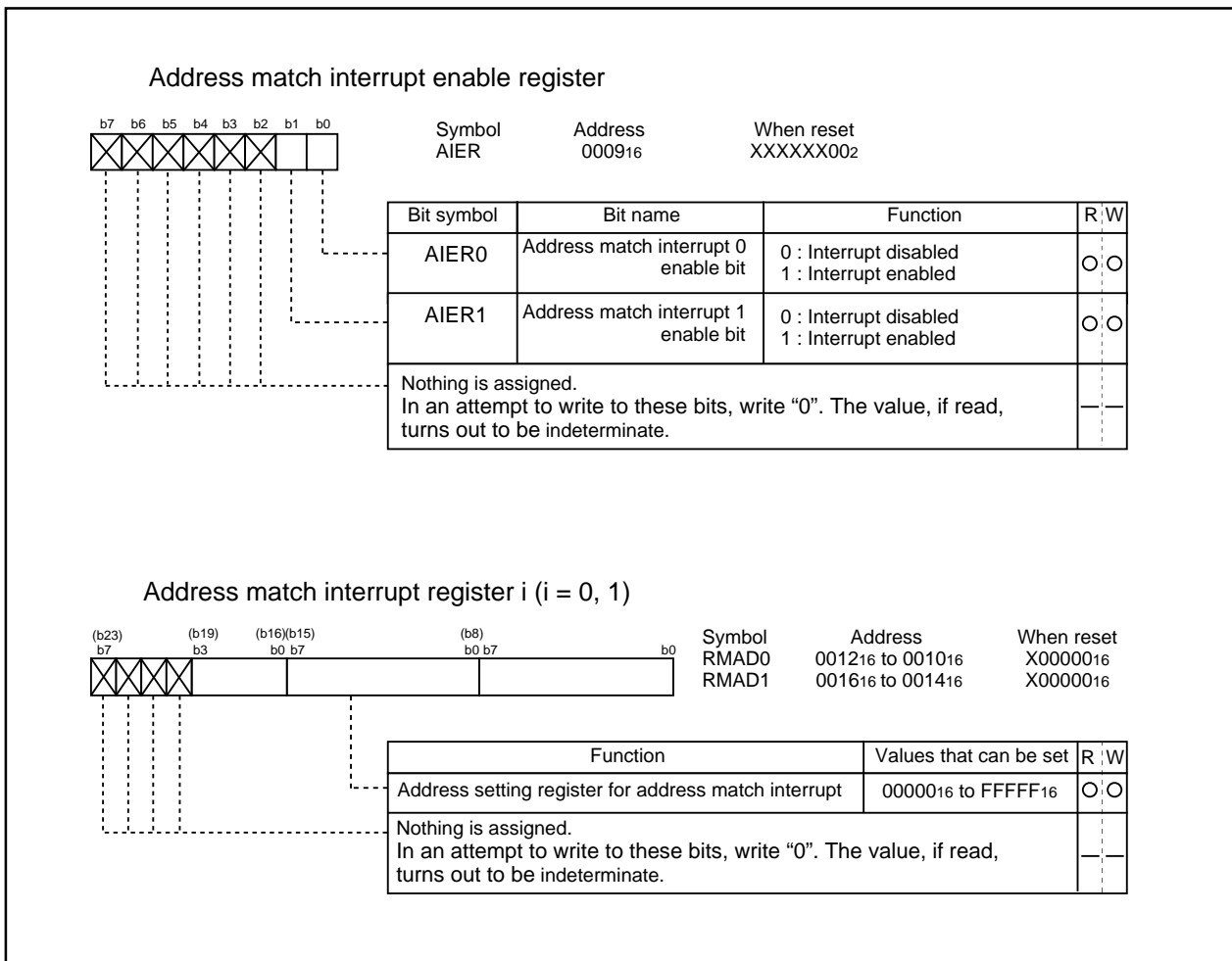


Figure 2.9.3. Address match interrupt-related registers

Address Match Interrupt

2.9.2 Operation of Address Match Interrupt

The following is an operation of address match interrupt. Figure 2.9.4 shows the set-up procedure of address match interrupt, and Figure 2.9.5 shows the overview of the address match interrupt handling routine.

- Operation
- (1) The address match interrupt handling routine sets an address to be used to cause the address match interrupt register to generate an interrupt.
 - (2) Setting the address match enable flag to "1" enables an interrupt to occur.
 - (3) An address match interrupt occurs immediately before the instruction in the address indicated by the address match interrupt register as a program is executed.

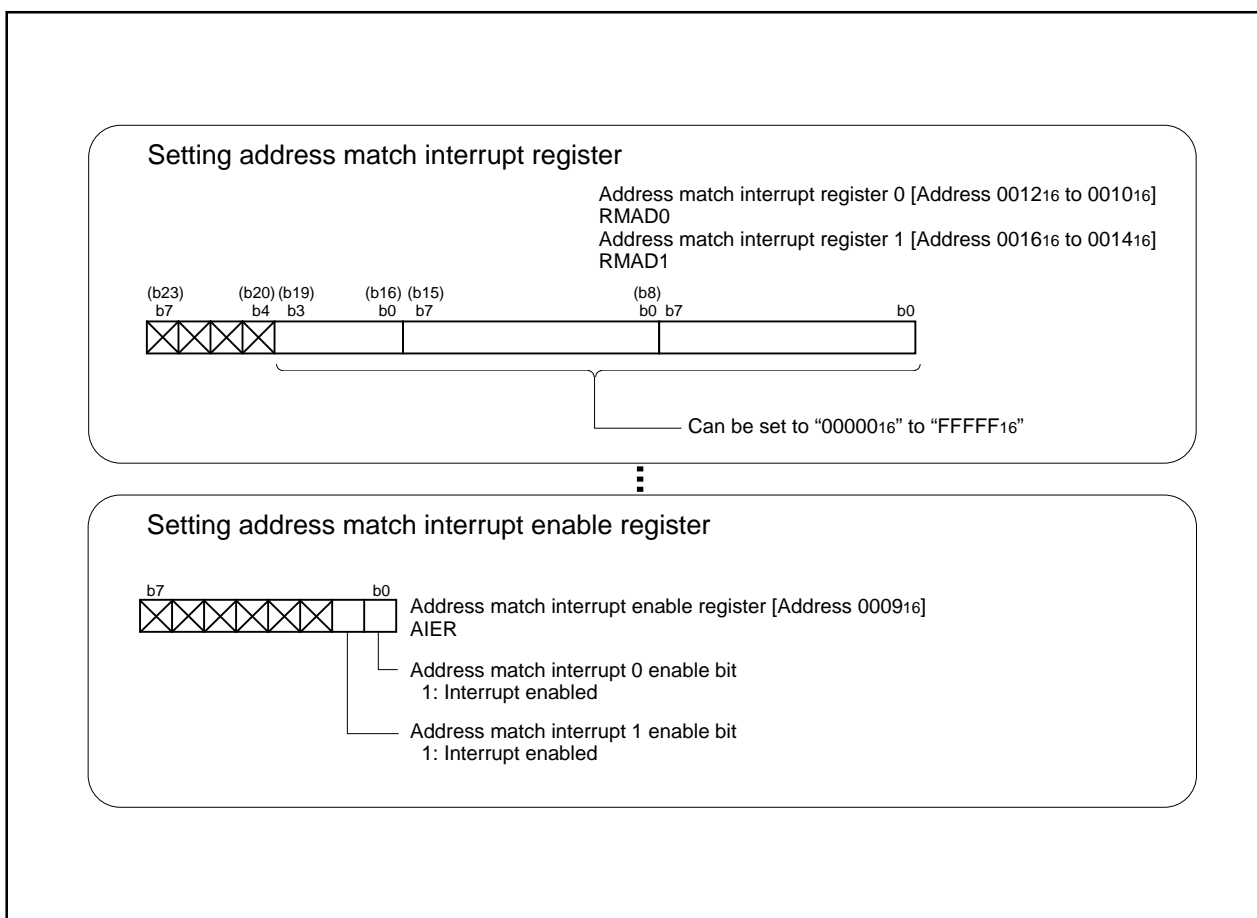


Figure 2.9.4. Set-up procedure of address match interrupt

Address Match Interrupt

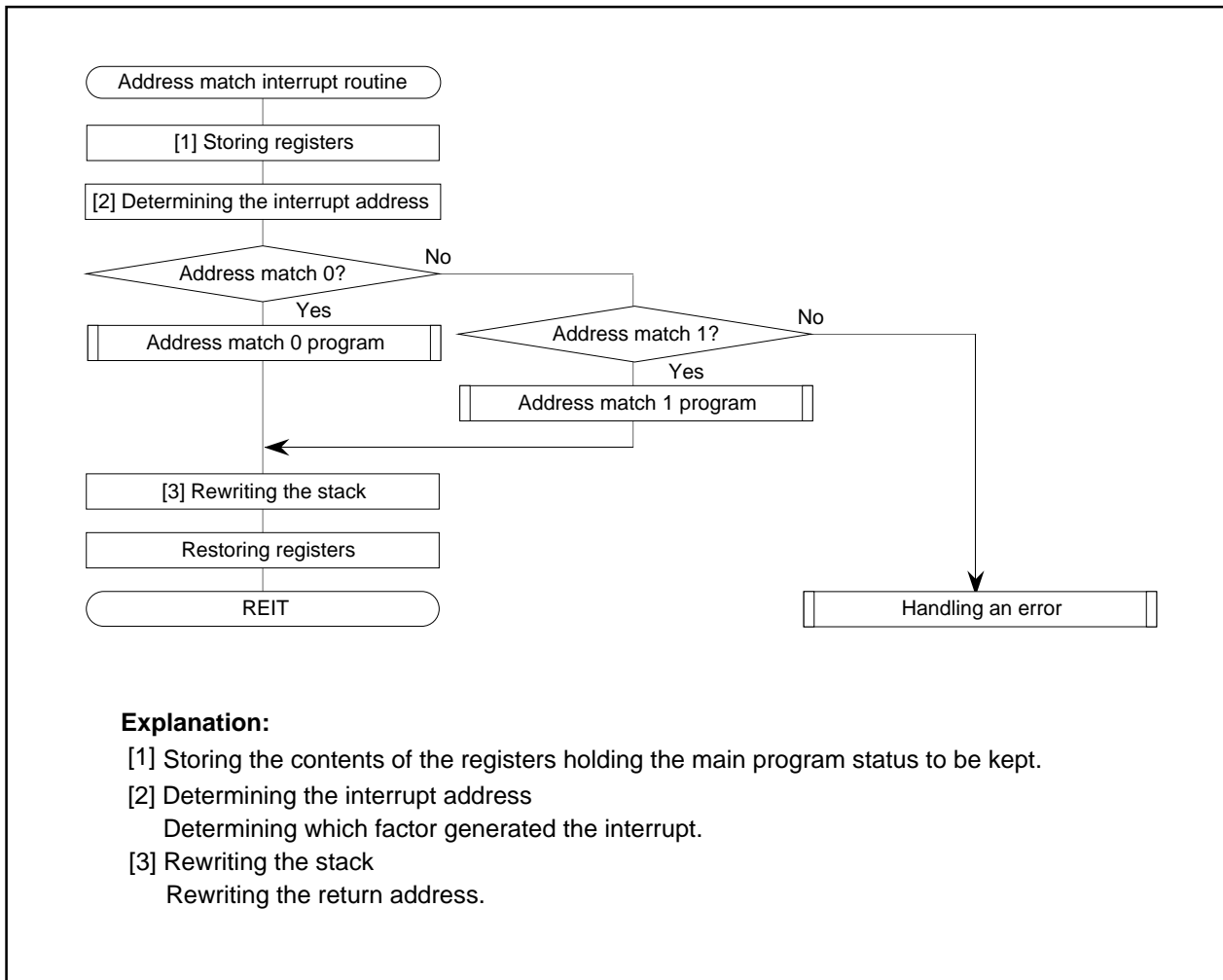


Figure 2.9.5. Overview of the address match interrupt handling routine

Key-Input Interrupt

2.10 Key-Input Interrupt

2.10.1 Overview

Key-input interrupt occurs when a falling edge is input to P00 through P07. The following is an overview of the key-input interrupt:

(1) Enabling/disabling the key-input interrupt

The key-input interrupt can be enabled and disabled using the key-input interrupt register. The key-input interrupt is affected by the interrupt priority level (IPL) and the interrupt enable flag (I flag).

(2) Occurrence timing of the key-input interrupt

With key-input interrupt acceptance enabled, pins P00 through P07, which are set to input, become key-input interrupt pins ($\bar{K}I_0$ through $\bar{K}I_7$). A key-input interrupt occurs when a falling edge is input to a key-input interrupt pin. At this moment, the level of other key-input interrupt pins must be "H". No interrupt occurs when the level of other key-input interrupt pins is "L".

(3) How to determine a key-input interrupt

A key-input interrupt occurs when a falling edge is input to one of eight pins, but each pin has the same vector address.

Therefore, read the input level of pins P00 through P07 in the key-input interrupt routine to determine the interrupted pin.

(4) Registers related to the key-input interrupt

Figure 2.10.1 shows the memory map of key-input interrupt-related registers, and Figure 2.10.2 shows key-input interrupt-related registers.

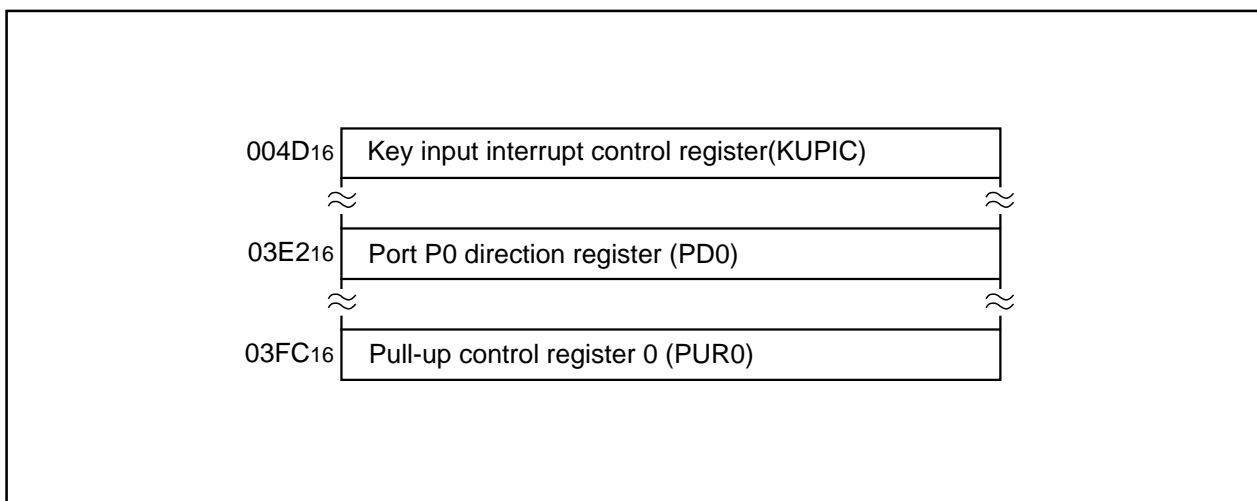
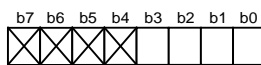


Figure 2.10.1. Memory map of key-input interrupt-related registers

Key-Input Interrupt

Interrupt control register (Note 2)



Symbol
KUPIC

Address
004D₁₆

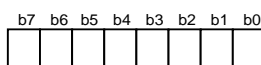
When reset
XXXXX000₂

Bit symbol	Bit name	Function	R	W
ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0 : Level 0 (interrupt disabled) 0 0 1 : Level 1 0 1 0 : Level 2 0 1 1 : Level 3 1 0 0 : Level 4 1 0 1 : Level 5 1 1 0 : Level 6 1 1 1 : Level 7	○	○
ILVL1			○	○
ILVL2			○	○
IR	Interrupt request bit	0 : Interrupt not requested 1 : Interrupt requested	○	○ (Note1)
Nothing is assigned. In an attempt to write to these bits, write "0". The value, if read, turns out to be indeterminate.			—	—

Note 1: This bit can only be accessed for reset (= 0), but cannot be accessed for set (= 1).

Note 2: To rewrite the interrupt control register, do so at a point that does not generate the interrupt request for that register. For details, see the precautions for interrupts.

Port P0 direction register



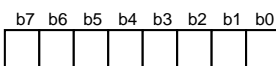
Symbol
PD0

Address
03E2₁₆

When reset
00₁₆

Bit symbol	Bit name	Function	R	W
PD0_0	Port P0 ₀ direction register	0 : Input mode (Functions as an input port) 1 : Output mode (Functions as an output port)	○	○
PD0_1	Port P0 ₁ direction register		○	○
PD0_2	Port P0 ₂ direction register		○	○
PD0_3	Port P0 ₃ direction register		○	○
PD0_4	Port P0 ₄ direction register		○	○
PD0_5	Port P0 ₅ direction register		○	○
PD0_6	Port P0 ₆ direction register		○	○
PD0_7	Port P0 ₇ direction register		○	○

Pull-up control register 0



Symbol
PUR0

Address
03FC₁₆

When reset
00₁₆

Bit symbol	Bit name	Function	R	W
PU00	P0 ₀ to P0 ₃ pull-up	The corresponding port is pulled high with a pull-up resistor 0 : Not pulled high 1 : Pulled high	○	○
PU01	P0 ₄ to P0 ₇ pull-up		○	○
PU02	P1 ₀ to P1 ₃ pull-up		○	○
PU03	P1 ₄ to P1 ₇ pull-up		○	○
—	—		○	○
—	—		○	○
—	—		○	○
PU06	P3 ₀ to P3 ₃ pull-up	○	○	
PU07	P3 ₄ to P3 ₅ pull-up	○	○	

Figure 2.10.2. key-input interrupt-related registers

Key-Input Interrupt

2.10.2 Operation of Key-Input Interrupt

The following is an operation of key-input interrupt. Figure 2.10.3 shows an example of a circuit that uses the key-input interrupt, Figure 2.10.4 shows an example of operation of key-input interrupt, and Figure 2.10.5 shows the setting procedure of key-input interrupt.

- Operation
- (1) Set the direction register of the ports to be changed to key-input interrupt pins to input, and set the pull-up function.
 - (2) Setting the key-input interrupt control register and setting the interrupt enable flag makes the interrupt-enabled state ready.
 - (3) If a falling edge is input to either $\overline{KI0}$ through $\overline{KI7}$, the key-input interrupt request bit goes to "1".

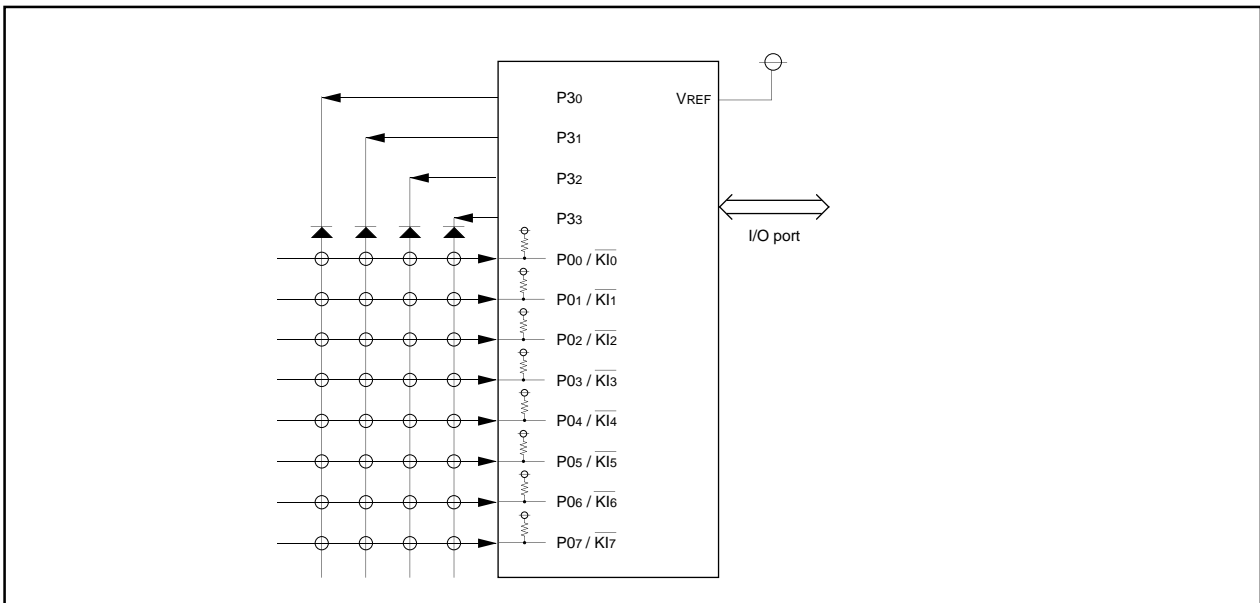


Figure 2.10.3. Example of circuit using the key-input interrupt

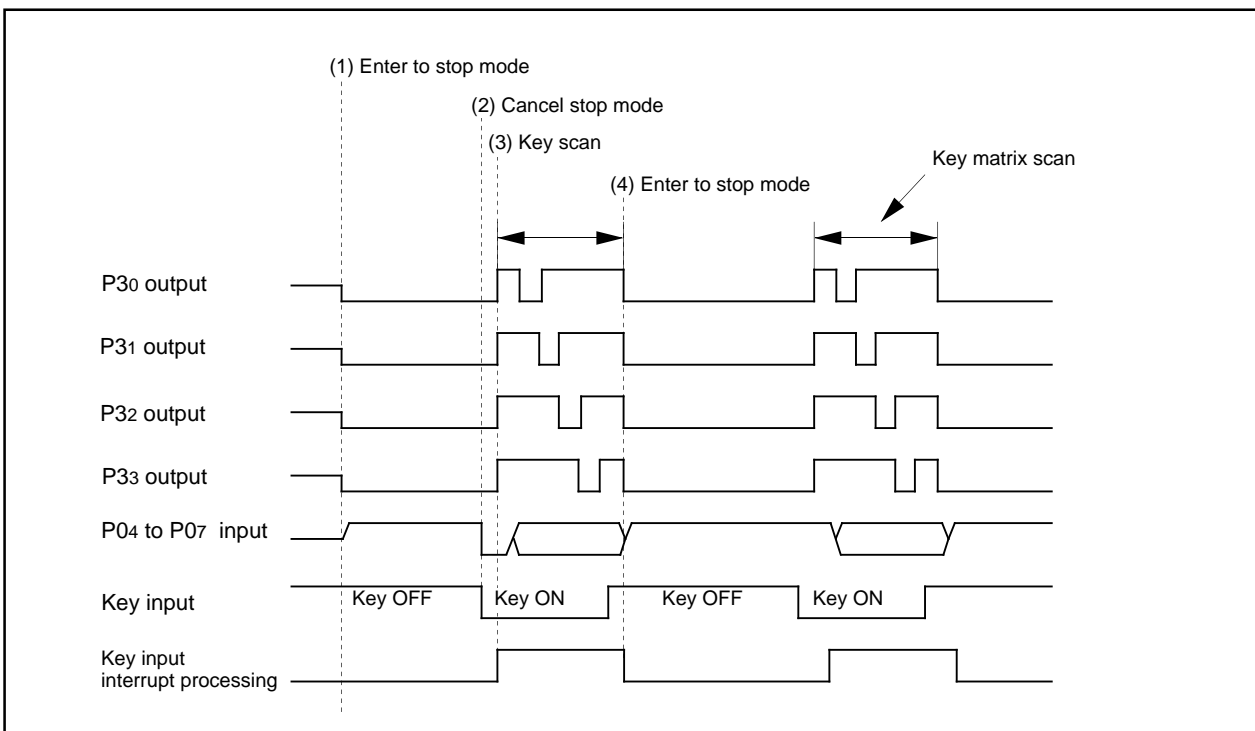


Figure 2.10.4. Example of operation of key-input interrupt

Key-Input Interrupt

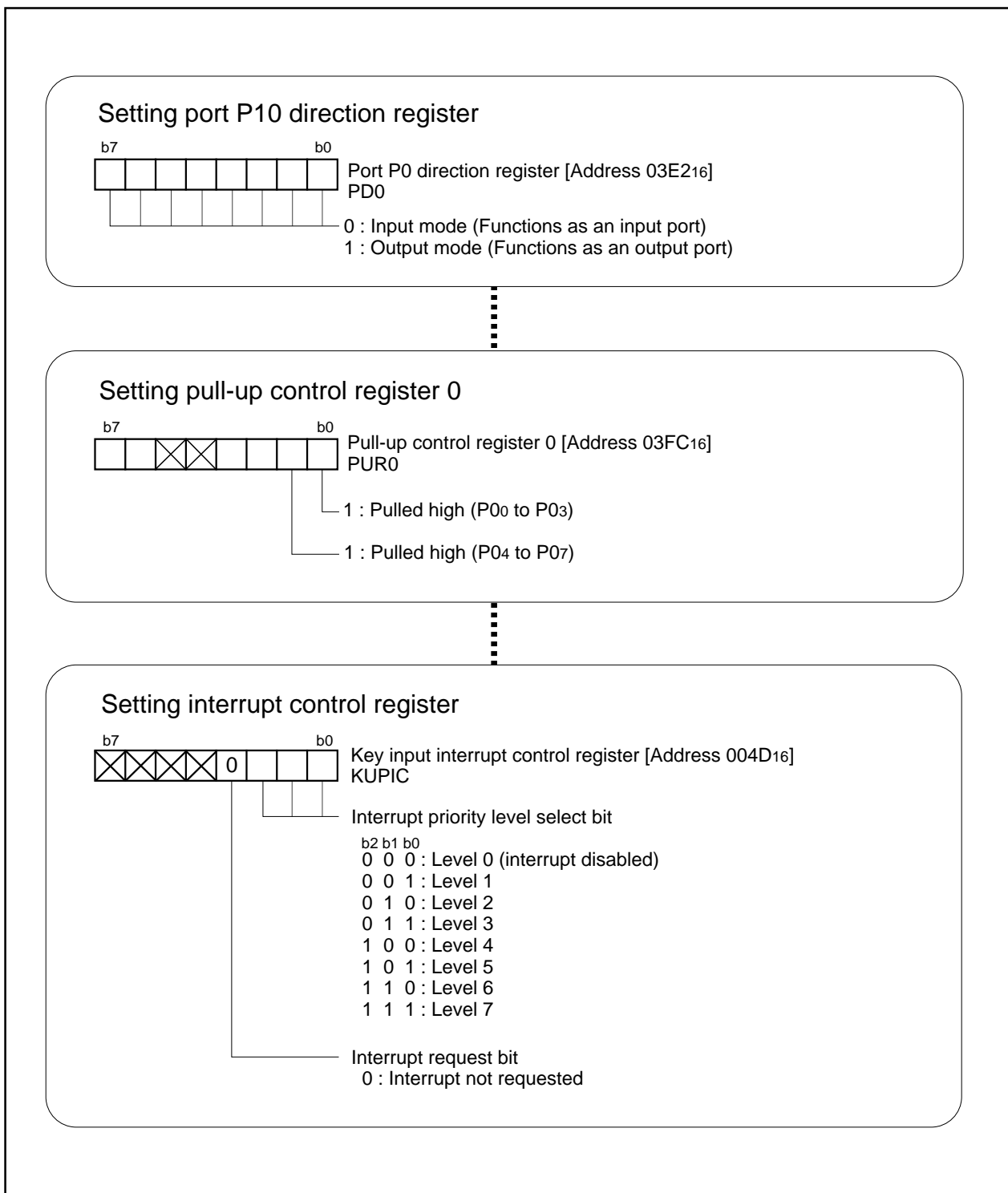


Figure 2.10.5. Set-up procedure of key-input interrupt

2.11 Power Control

2.11.1 Overview

'Power Control' refers to the reduction of CPU power consumption by stopping the CPU and oscillators, or decreasing the operation clock. The following is a description of the three available power control modes:

(1) Modes

Power control is available in three modes.

(a) Normal operation mode

- **High-speed mode**

Divide-by-1 frequency of the main clock becomes the BCLK. The CPU operates with the BCLK selected. Each peripheral function operates according to its assigned clock.

- **Medium-speed mode**

Divide-by-2, divide-by-4, divide-by-8, or divide-by-16 frequency of the main clock becomes the BCLK. The CPU operates according to the BCLK selected. Each peripheral function operates according to its assigned clock.

- **Low-speed mode**

fc becomes the BCLK. The CPU operates according to the fc clock. The fc clock is supplied by the secondary clock. Each peripheral function operates according to its assigned clock.

- **Low power consumption mode**

The main clock operating in low-speed mode is stopped. The CPU operates according to the fc clock. The fc clock is supplied by the secondary clock. The only peripheral functions that operate are those with the sub-clock selected as the count source.

(b) Wait mode

The CPU operation is stopped. The oscillators do not stop.

(c) Stop mode

All oscillators stop. The CPU and all built-in peripheral functions stop. This mode, among the three modes listed here, is the most effective in decreasing power consumption.

Figure 2.11.1 is the state transition diagram of the above modes.

Power Control

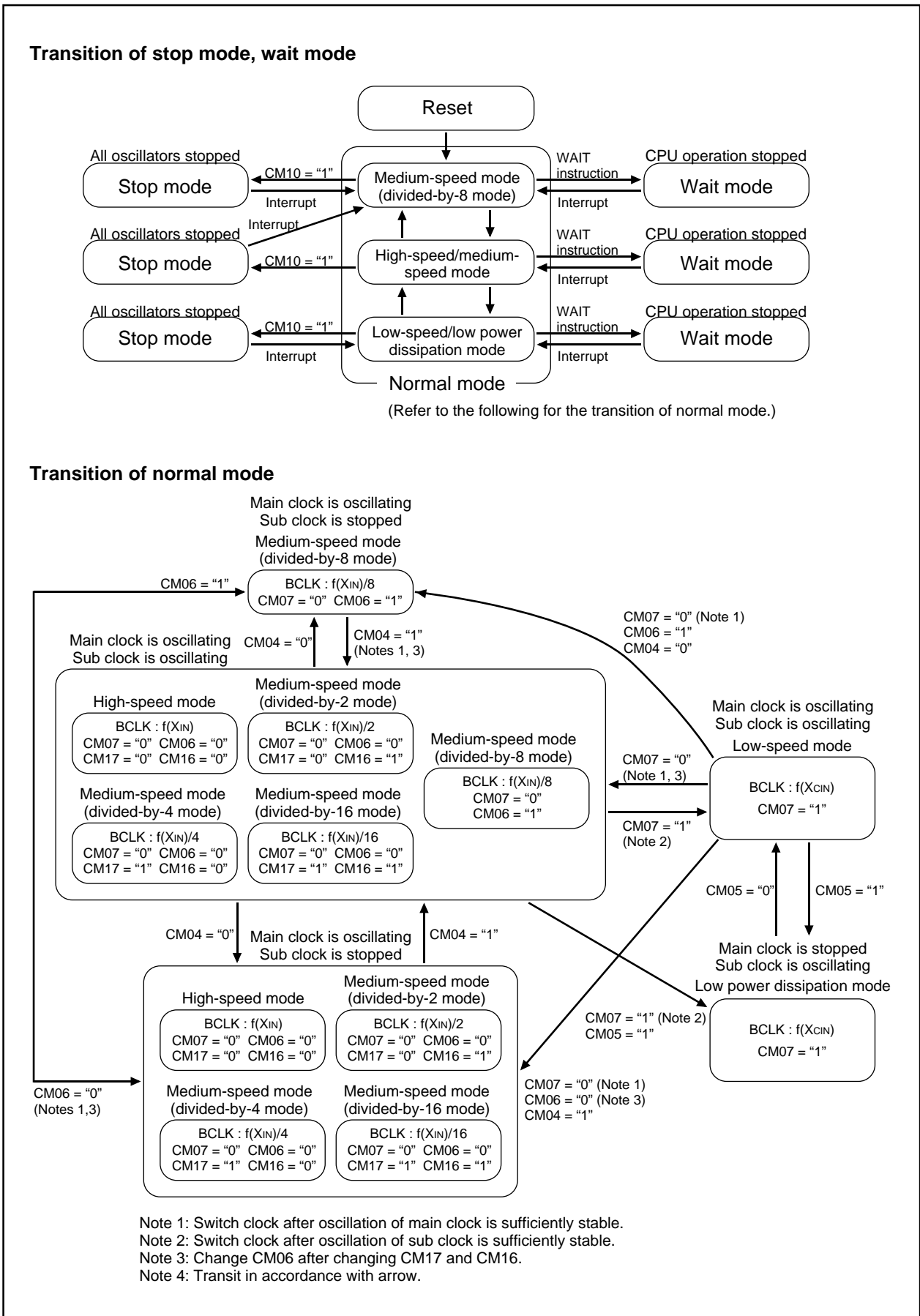


Figure 2.11.1. State transition diagram of power control mode

(2) Switching the driving capacity of the oscillation circuit

Both the main clock and the secondary clock have the ability to switch the driving capacity. Reducing the driving capacity after the oscillation stabilizes allows for further reduction in power consumption.

(3) Clearing stop mode and wait mode

The stop mode and wait mode can be cleared by generating an interrupt request, or by resetting hardware. Set the priority level of the interrupt to be used for clearing, higher than the processor interrupt priority level (IPL), and enable the interrupt enable flag (I flag). When an interrupt clears a mode, that interrupt is processed. Table 2.11.1 shows the interrupts that can be used for clearing a stop mode and wait mode.

(4) BCLK in returning from wait mode or stop mode

(a) Returning from wait mode

The processor immediately returns to the BCLK, which was in use before entering wait mode.

(b) Returning from stop mode

If operation was performed in the high speed mode or medium speed mode prior to engaging the stop mode, CM06 will change to "1" when operation shifts to the stop mode. CM17, CM16 and CM07 do not change. Accordingly, when operation is restored from the stop mode, operation starts in the 8 division mode.

Also, if operation was performed in the low speed mode prior to engaging the stop mode, CM06, CM17, CM16 and CM07 do not change. When operation is restored from the stop mode, operation starts in the low speed mode.

Table 2.11.1. Interrupts available for clearing stop mode and wait mode

Interrupt for clearing	Wait mode		Stop mode
	CM02 = 0	CM02 = 1(Note 4), CM07=0, CM05=0	
Key input interrupt	Possible	Possible	Possible
A-D interrupt	Note 3	Impossible	Impossible
UART0 transmit interrupt	Possible	Note 1	Note 1
UART0 receive interrupt	Possible	Note 1	Note 1
UART1 transmit interrupt	Possible	Impossible	Impossible
UART1 receive interrupt	Possible	Impossible	Impossible
Timer A0 interrupt	Possible	Note 2	Note 2
Timer B0 interrupt	Possible	Note 2	Note 2
Timer B1 interrupt	Possible	Note 2	Note 2
Timer X0 interrupt	Possible	Note 2	Note 2
Timer X1 interrupt	Possible	Note 2	Note 2
Timer X2 interrupt	Possible	Note 2	Note 2
INT0 interrupt	Possible	Possible	Possible
INT1 interrupt	Possible	Possible	Possible

Note 1: Can be used when an external clock in clock synchronous serial I/O mode is selected.

Note 2: Can be used when the external signal is being counted in event counter mode.

Note 3: Can be used in one-shot mode and one-shot sweep mode.

Note 4: When the MCU running in low-speed or low power dissipation mode, do not enter WAIT mode with CM02 set to 1.

Power Control

(5) Sequence of returning from stop mode

Sequence of returning from stop mode is oscillation start-up time and interrupt sequence.

When interrupt is generated in stop mode, CM10 becomes "0" and clearing stop mode.

Starting oscillation and supplying BCLK execute the interrupt sequence as follow:

In the interrupt sequence, the processor carries out the following in sequence given:

- (a) CPU gets the interrupt information (the interrupt number and interrupt request level) by reading address 00000₁₆. The interrupt request bit of the interrupt written in address 00000₁₆ will then be set to "0".
- (b) Saves the content of the flag register (FLG) as it was immediately before the start of interrupt sequence in the temporary register (Note) within the CPU.
- (c) Sets the interrupt enable flag (I flag), the debug flag (D flag), and the stack pointer assignment flag (U flag) to "0" (the U flag, however does not change if the INT instruction, in software interrupt numbers 32 through 63, is executed)
- (d) Saves the content of the temporary register (Note) within the CPU in the stack area.
- (e) Saves the content of the program counter (PC) in the stack area.
- (f) Sets the interrupt priority level of the accepted instruction in the IPL.

Note: This register cannot be utilized by the user.

After the interrupt sequence is completed, the processor resumes executing instructions from the first address of the interrupt routine.

Figure 2.11.2 shows the sequence of returning from stop mode.

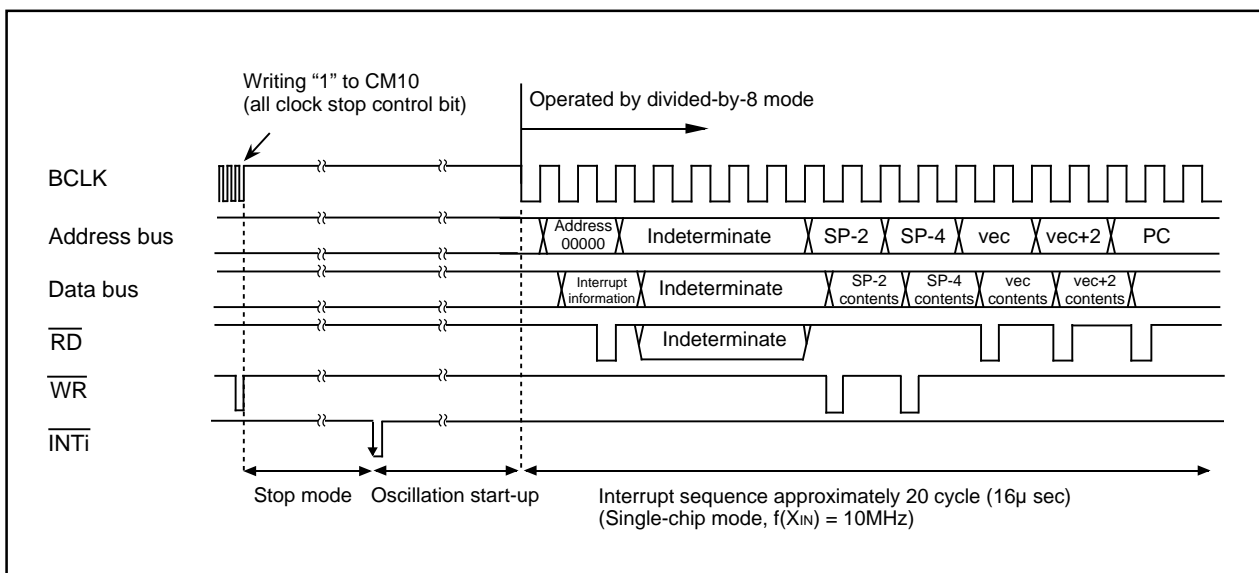


Figure 2.11.2. Sequence of returning from stop mode

(6) Registers related to power control

Figure 2.11.3 shows the memory map of power control-related registers, and Figure 2.11.4 shows power control-related registers.

Power Control

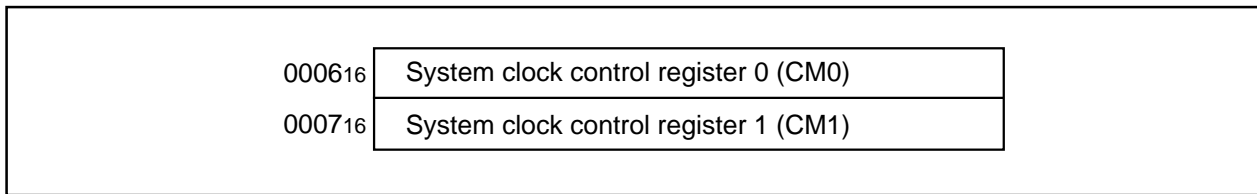


Figure 2.11.3. Memory map of power control-related registers

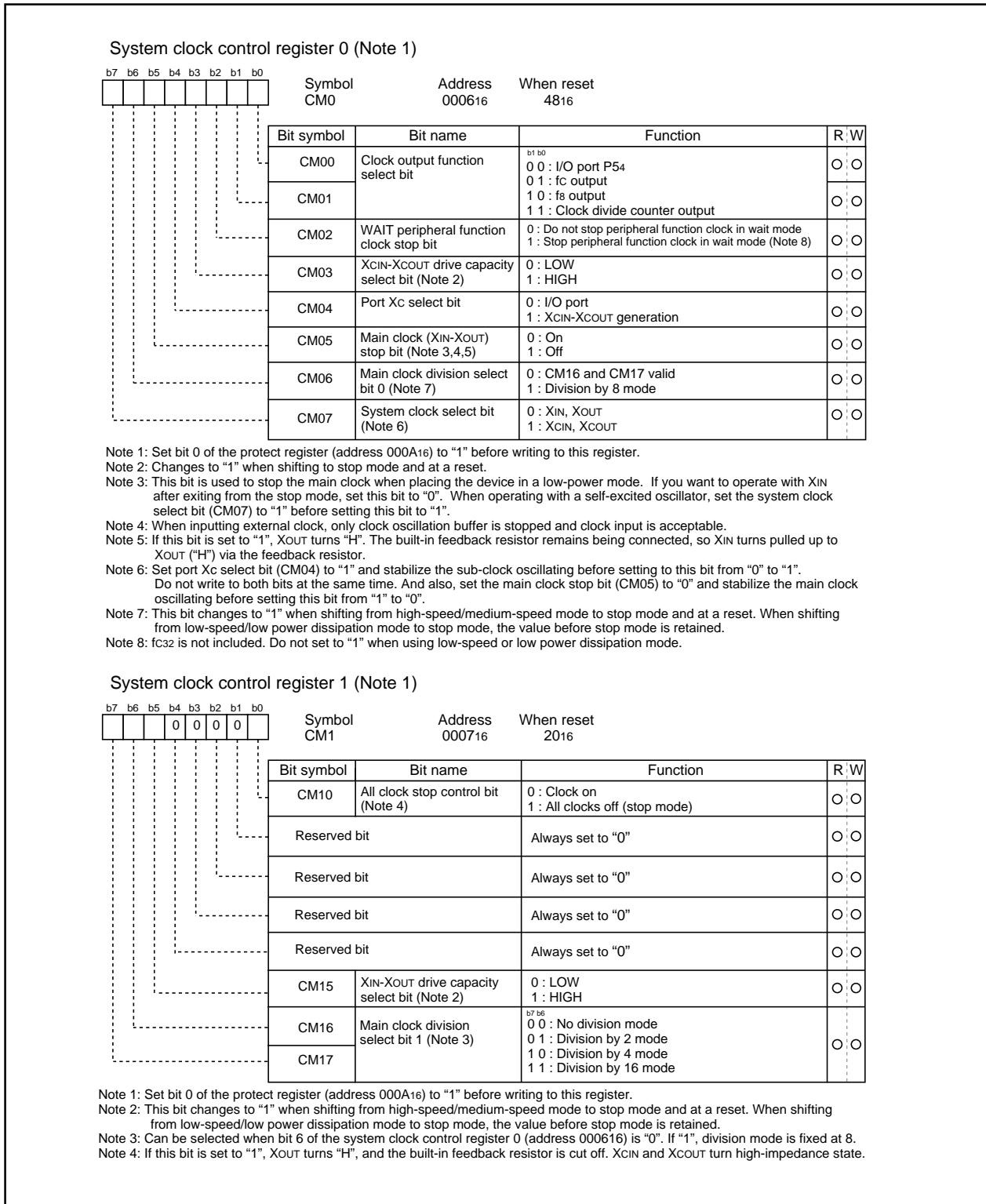


Figure 2.11.4. Power control-related registers

Power Control

2.11.2 Stop Mode Set-Up

Settings and operation for entering stop mode are described here.

- Operation (1) Enables the interrupt used for returning from stop mode.
- (2) Sets the interrupt enable flag (I flag) to "1".
- (3) Clearing the protection and setting every-clock stop bit to "1" stops oscillation and causes the processor to go into stop mode.

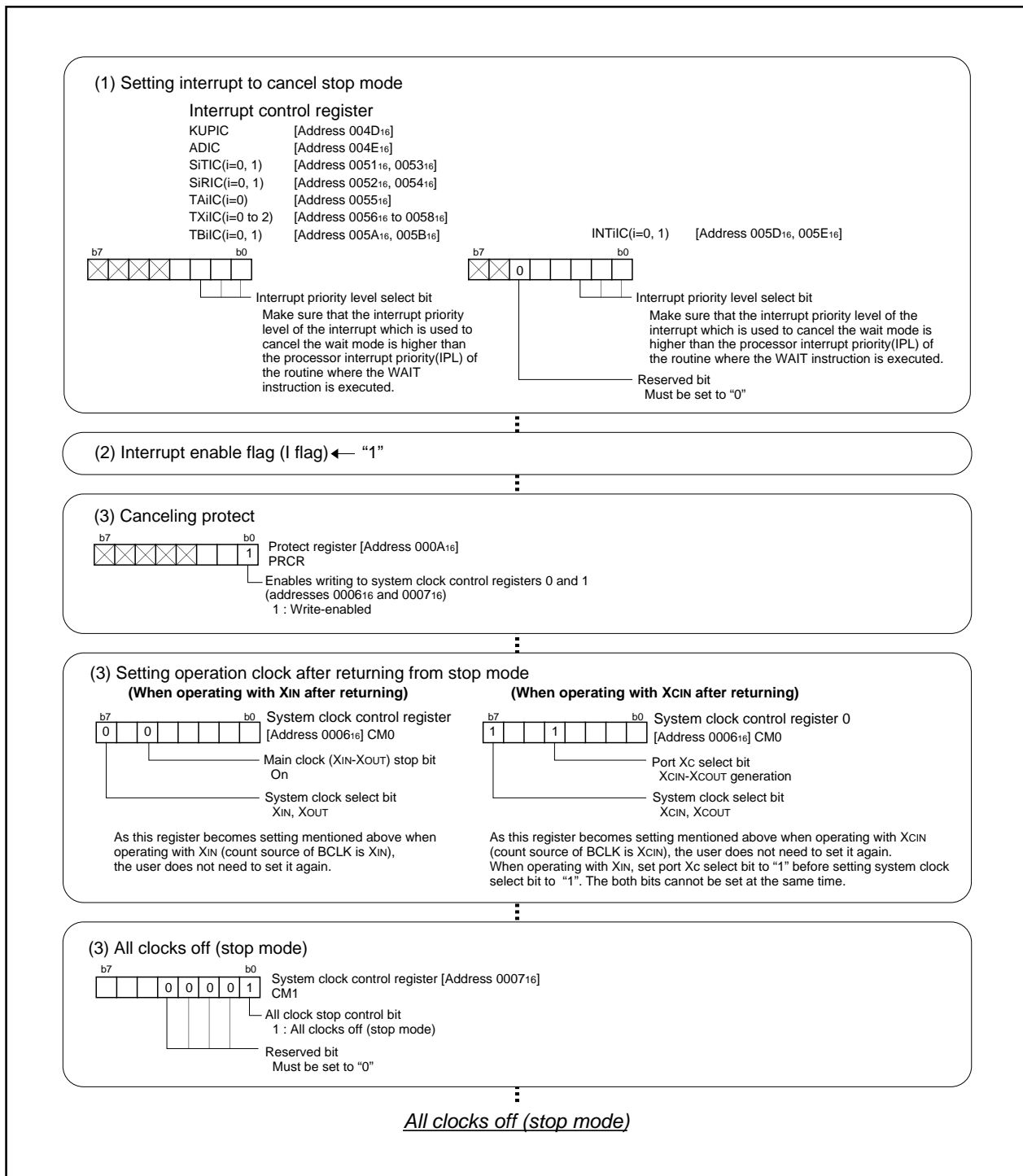


Figure 2.11.5. Example of stop mode set-up

Power Control

2.11.3 Wait Mode Set-Up

Settings and operation for entering wait mode are described here.

- Operation (1) Enables the interrupt used for returning from wait mode.
 (2) Sets the interrupt enable flag (I flag) to "1".
 (3) Clears the protection and changes the content of the system clock control register.
 (4) Executes the WAIT instruction.

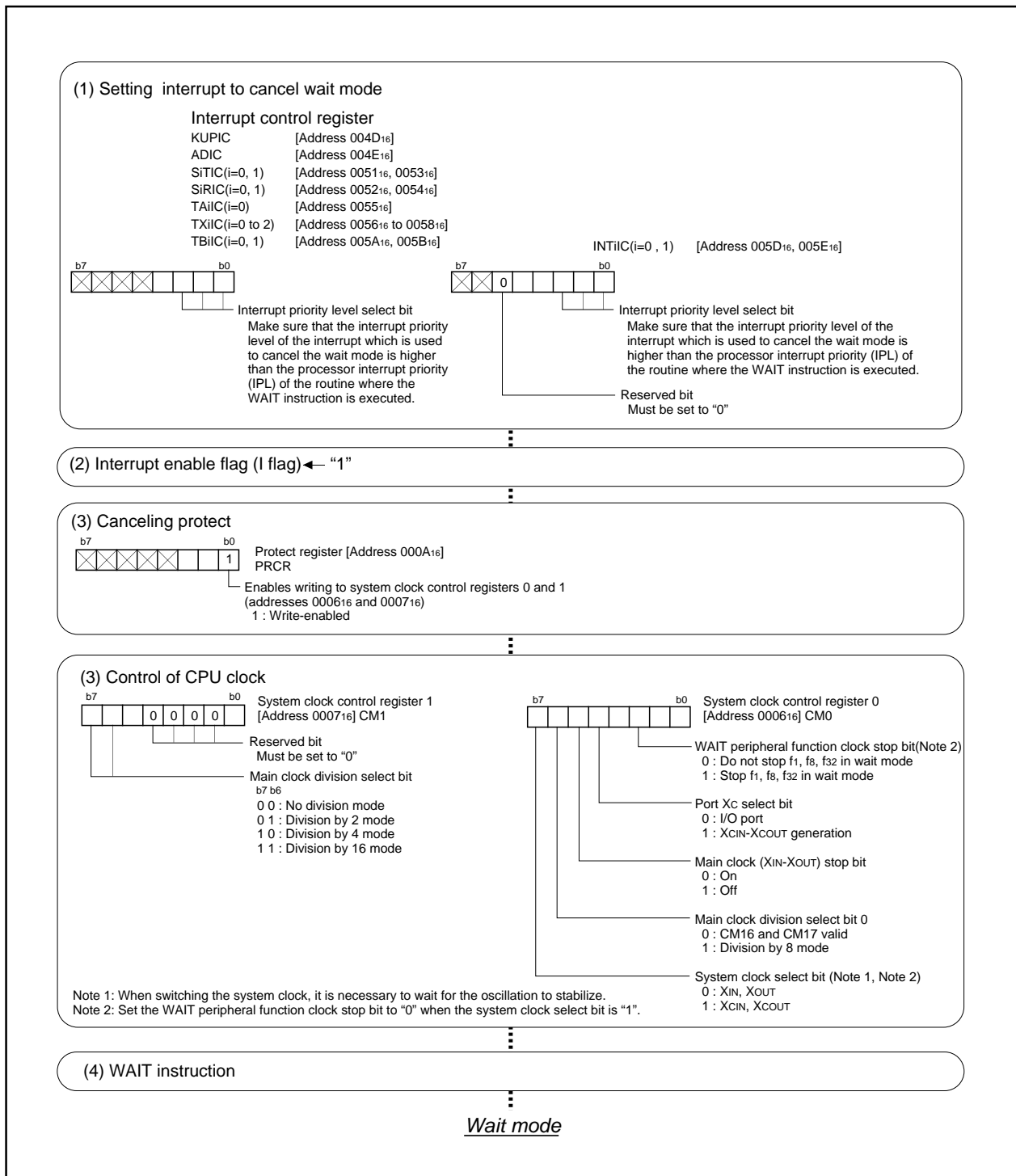


Figure 2.11.6. Example of wait mode set-up

2.11.4 Precautions in Power Control

- (1) When returning from stop mode by hardware reset, $\overline{\text{RESET}}$ pin must be set to "L" level until main clock oscillation is stabilized.
- (2) When switching to either wait mode or stop mode, instructions occupying four bytes either from the WAIT instruction or from the instruction that sets the every-clock stop bit to "1" within the instruction queue are prefetched and then the program stops. So put at least four NOPs in succession either to the WAIT instruction or to the instruction that sets the every-clock stop bit to "1".
- (3) Suggestions to reduce power consumption

- **Ports**

The processor retains the state of each programmable I/O port even when it goes to wait mode or to stop mode. A current flows in active I/O ports. A pass current flows in input ports that float. When entering wait mode or stop mode, set non-used ports to input and stabilize the potential.

- (a) **A-D converter**

A current always flows in the VREF pin. When entering wait mode or stop mode, set the Vref connection bit to "0" so that no current flows into the VREF pin.

- (b) **Stopping peripheral functions**

In wait mode, stop non-used wait peripheral functions using the peripheral function clock stop bit. However, peripheral function clock fc32 does not stop so that the peripherals using fc32 do not contribute to the power saving. When the MCU running in low-speed or low power dissipation mode, do not enter WAIT mode with this bit set to "1".

- (c) **Switching the oscillation-driving capacity**

Set the driving capacity to "LOW" when oscillation is stable.

- (d) **External clock**

When using an external clock input for the CPU clock, set the main clock stop bit to "1". Setting the main clock stop bit to "1" causes the XOUT pin not to operate and the power consumption goes down (when using an external clock input, the clock signal is input regardless of the content of the main clock stop bit).

2.12 Programmable I/O Ports

2.12.1 Overview

Forty-three programmable I/O ports. I/O pins also serve as I/O pins for built-in peripheral functions. Each port has a direction register that defines the I/O direction and also has a port register for I/O data. In addition, each port has a pull-up control register that defines pull-up in terms of 4 bits. Port P1 can be set to N-channel output transistor drive capacity.

The following is an overview of the programmable I/O ports:

(1) Writing to a port register

With the direction register set to output, the level of the written values from each relevant pin is output by writing to a port register. The output level conforms to CMOS output. Writing to the port register, with the direction register set to input, inputs a value to the port register, but nothing is output to the relevant pins. The output level remains floating.

(2) Reading a port register

With the direction register set to output, reading a port register takes out the content of the port register, not the content of the pin. With the direction register set to input, reading the port register takes out the content of the pin.

(3) Effect of the protection register

Data written to the direction register of P4 is affected by the protection register. The direction register of P4 cannot be easily rewritten.

(4) Setting pull-up

The pull-up control bit allows setting of the pull-up, in terms of 4 bits, either in use or not in use. For the four bits chosen, pull-up is effective only in the ports whose direction register is set to input. Pull-up is not effective in ports whose direction register is set to output.

Do not set pull-up of corresponding pin when XCIN/XCOUT is set or a port is used as A-D input.

(5) Drive capacity control

The drive capacity of the N channel output transistor on P1 can be set between "LOW" and "HIGH" in units of 1 bit. One bit corresponds to one pin.

(6) I/O functions of built-in peripheral devices

Table 2.12.1 shows relation between ports and I/O functions of built-in peripheral devices.

Table 2.12.1. Relation between ports and I/O functions of built-in peripheral devices

Port	Internal peripheral device I/O pins
P0	key-input interrupt function input pins
P40	I/O pin for serial I/O communication/Timer A input pin
P41	Timer A output pin
P42	Serial I/O input pin
P43, P44	Input pins for external interrupt/Timer X I/O pins
P45	Timer X I/O pin
P50 to P54	I/O pins for serial I/O communication/A-D converter input pins
P6	A-D converter input pins
P70, P71	Timer B input pins

(7) Examples of working on non-used pins

Table 2.12.2 contains examples of working on non-used pins. There are shown here for mere examples. In practical use, make suitable changes and perform sufficient evaluation in compliance with you application.

Table 2.12.2. Examples of working on unused pins in single-chip mode

Pin name	Connection
Ports P0, P1, P3 to P7	After setting for input mode, connect every pin to Vss or Vcc via a resistor; or after setting for output mode, leave these pins open. (Note 1)
XOUT (Note 2)	Open
AVCC	Connect to VCC
AVSS, VREF, BYTE	Connect to VSS

Note 1: If setting these pins in output mode and opening them, ports are in input mode until switched into output mode by use of software after reset. Thus the voltage levels of the pins become unstable, and there can be instances in which the power source current increases while the ports are in input mode.

In view of an instance in which the contents of the direction registers change due to a runaway generated by noise or other causes, setting the contents of the direction registers periodically by use of software increases program reliability.

Note 2: When an external clock is input to the XIN pin.

Programmable I/O Ports

(8) Registers related to the programmable I/O ports

Figure 2.12.1 shows the memory map of programmable I/O ports-related registers, and Figures 2.12.2 to 2.12.4 show programmable I/O ports-related registers.

03E0 ₁₆	Port P0 (P0)
03E1 ₁₆	Port P1 (P1)
03E2 ₁₆	Port P0 direction register (PD0)
03E3 ₁₆	Port P1 direction register (PD1)
03E4 ₁₆	
03E5 ₁₆	Port P3 (P3)
03E6 ₁₆	
03E7 ₁₆	Port P3 direction register (PD3)
03E8 ₁₆	Port P4 (P4)
03E9 ₁₆	Port P5 (P5)
03EA ₁₆	Port P4 direction register (PD4)
03EB ₁₆	Port P5 direction register (PD5)
03EC ₁₆	Port P6 (P6)
03ED ₁₆	Port P7 (P7)
03EE ₁₆	Port P6 direction register (PD6)
03EF ₁₆	Port P7 direction register (PD7)
	≈
03FC ₁₆	Pull-up control register 0 (PUR0)
03FD ₁₆	Pull-up control register 1 (PUR1)
03FE ₁₆	Port P1 drive control register (DRR)

Figure 2.12.1. Memory map of programmable I/O ports-related registers

Programmable I/O Ports

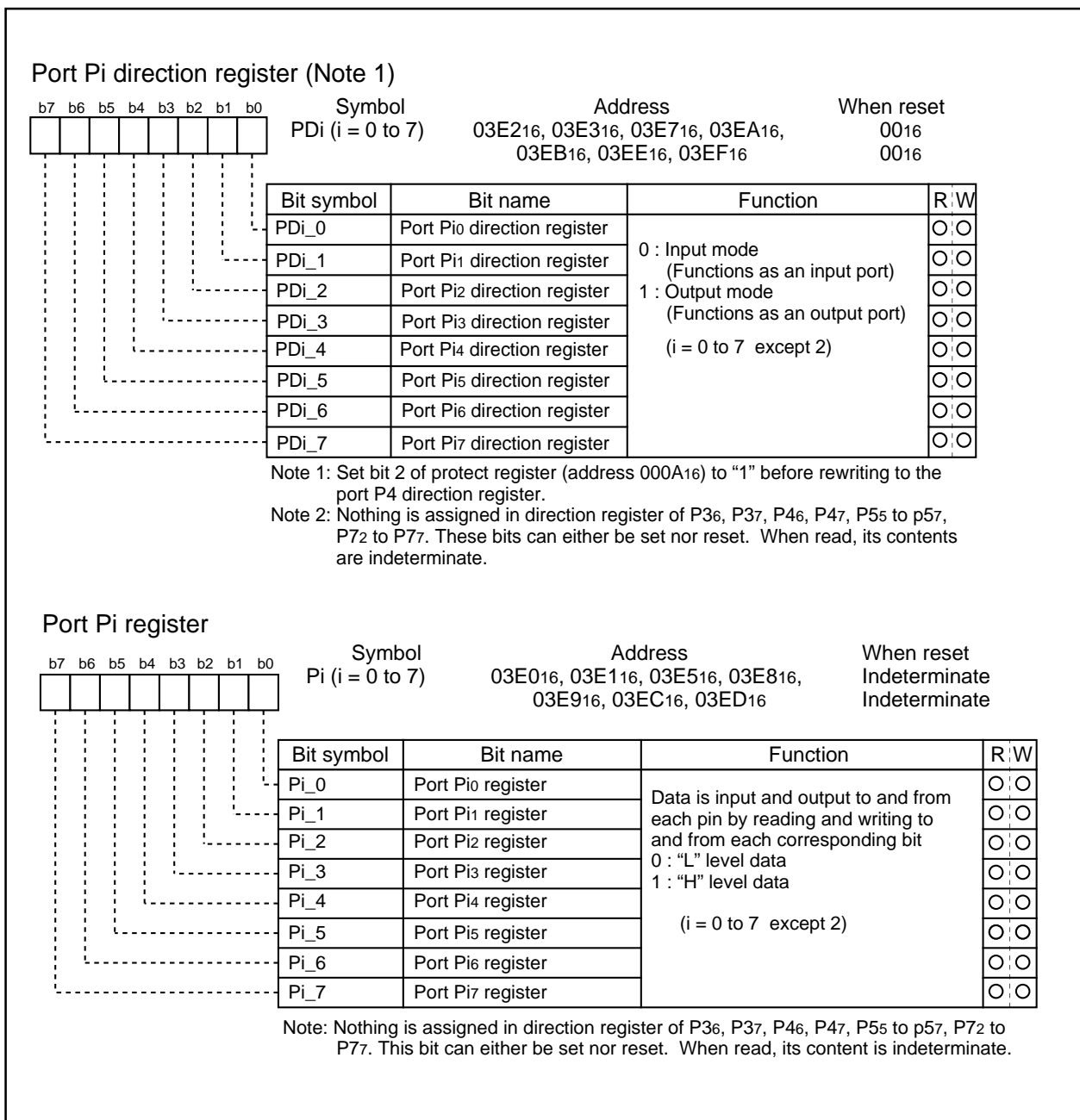


Figure 2.12.2. Programmable I/O ports-related registers (1)

Programmable I/O Ports

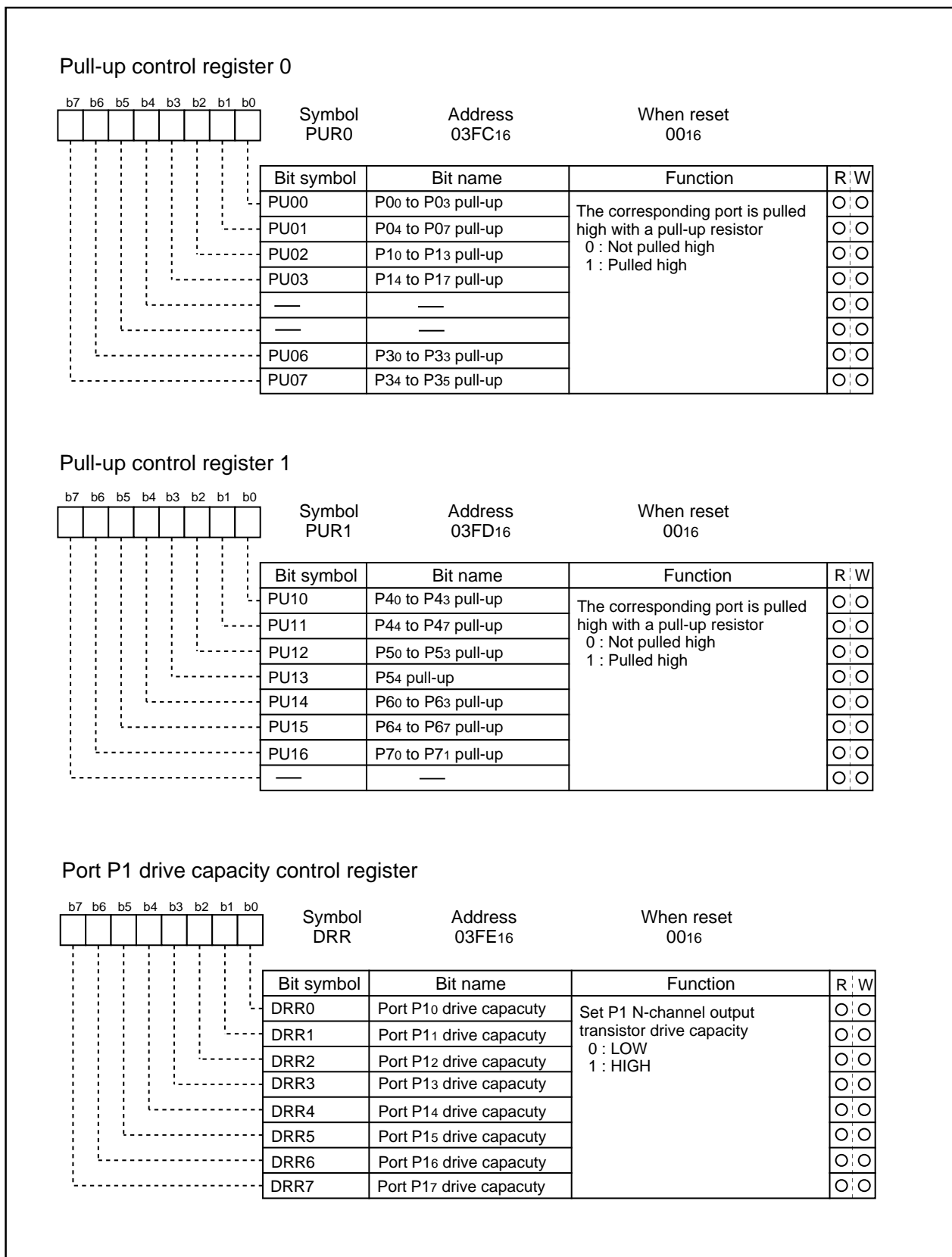


Figure 2.12.3. Programmable I/O ports-related registers (2)

Chapter 3

Examples of Peripheral functions Applications

Applications

This chapter presents applications in which peripheral functions built in the M16C/20 are used. They are shown here as examples. In practical use, make suitable changes and perform sufficient evaluation. For basic use, see Chapter 2 How to Use Peripheral Functions.

Here follows the list of applications that appear in this chapter.

- 3.1 Long-period timers P338
- 3.2 Variable-period variable-duty PWM output P342
- 3.3 Delayed one-shot output P346
- 3.4 Buzzer output P350
- 3.5 Solution for external interrupt pins shortage P352
- 3.6 Controlling power using stop mode P354
- 3.7 Controlling power using wait mode P358

Applications

[MEMO]

Timer X Applications

3.1 Long-Period Timers

Overview In this process, Timer X0 and Timer X1 are connected to make a 16-bit timer with a 16-bit prescaler. Figure 3.1.1 shows the operation timing, Figure 3.1.2 shows the connection diagram, and Figures 3.1.3 and 3.1.4 show the set-up procedure.

Use the following peripheral functions:

- Timer mode of timer X
- Event counter mode of timer X

Specifications

- (1) Set timer X0 to timer mode, and set timer X1 to event counter mode.
- (2) Perform a count on count source f1 using timer X0 to count for 1 ms, and perform a count on timer X0 using timer X1 to count for 1 second.
- (3) Connect a 10-MHz oscillator to XIN.

- Operation**
- (1) Setting the count start flag to "1" causes the counter to begin counting. The counter of timer X0 performs a down count on count source f1.
 - (2) If the counter of timer X0 underflows, the counter reloads the content of the reload register and continues counting. At this time, the timer X0 interrupt request bit goes to "1". The counter of timer X1 performs a down count on underflows in timer X0.
 - (3) If the counter of timer X1 underflows, the counter reloads the content of the reload register and continues counting. At this time, the timer X1 interrupt request bit goes to "1".

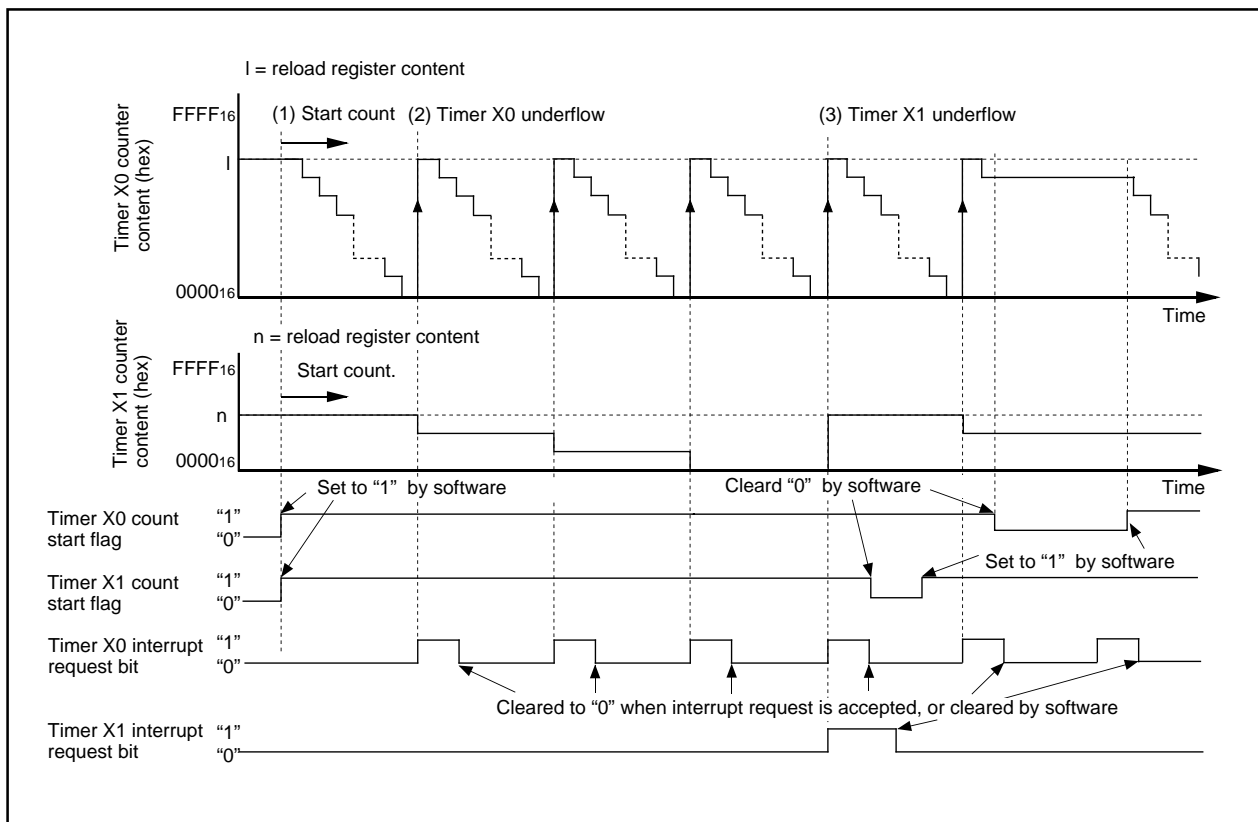


Figure 3.1.1. Operation timing of long-period timers

Timer X Applications

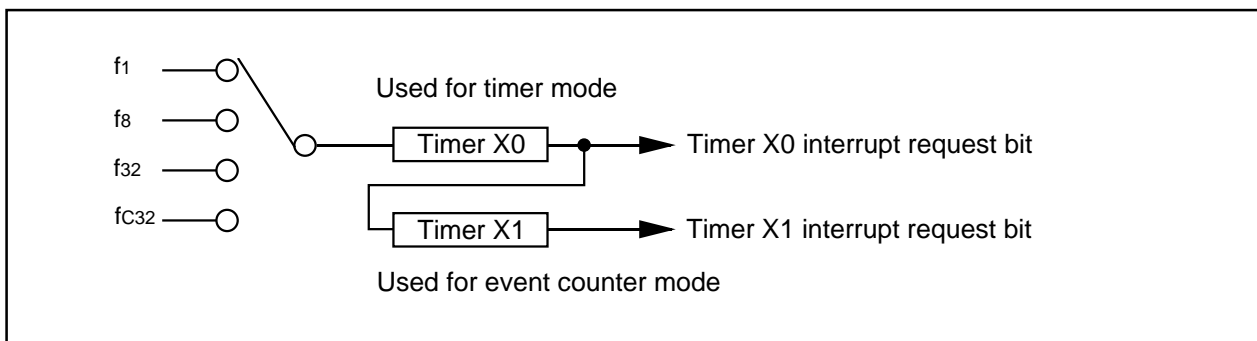
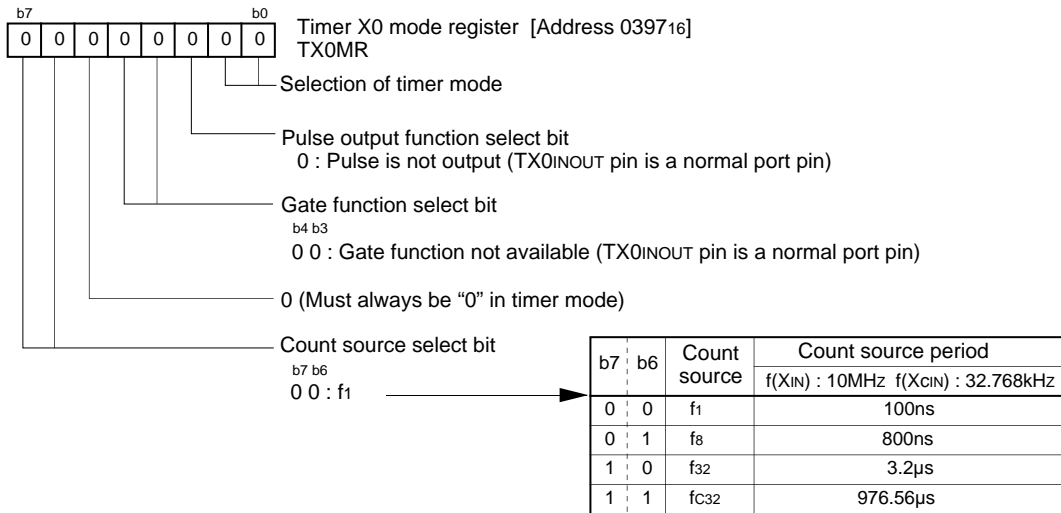


Figure 3.1.2. Connection diagram of long-period timers

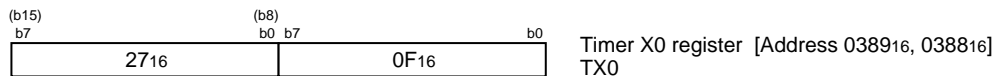
Timer X Applications

Setting timer X0

Selecting timer mode and functions

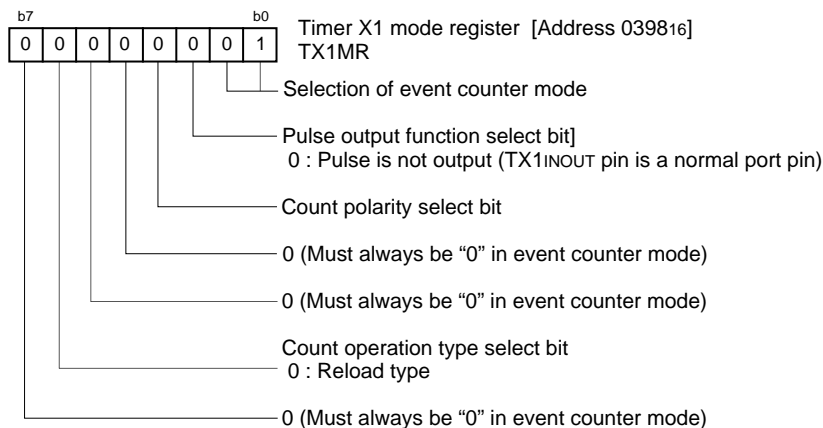


Setting divide ratio



Setting timer X1

Selecting event counter mode and each function



Continued to the next page

Figure 3.1.3. Set-up procedure of long-period timers (1)

Timer X Applications

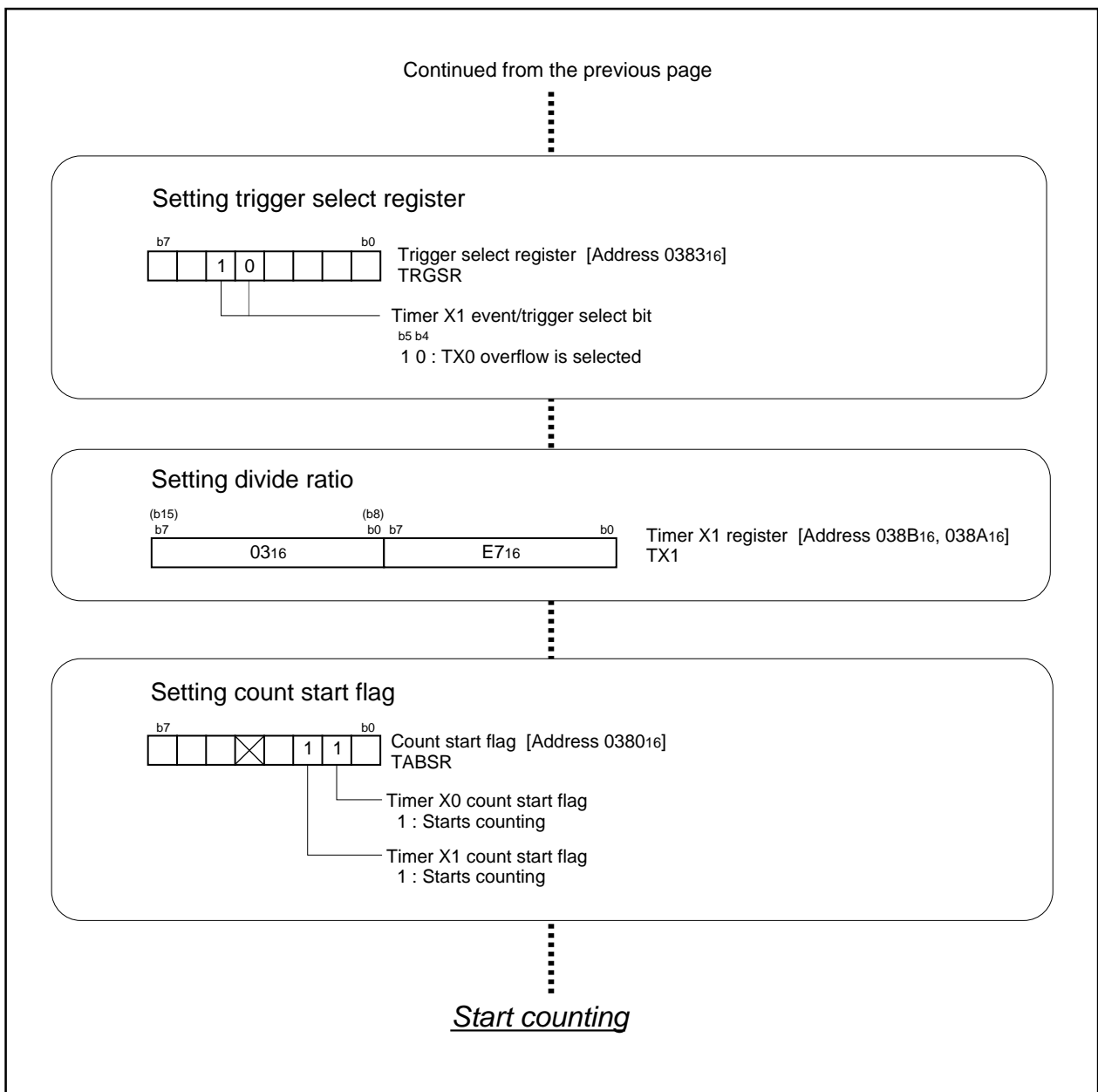


Figure 3.1.4. Set-up procedure of long-period timers (2)

3.2 Variable-Period Variable-Duty PWM Output

Overview In this process, Timer X0 and A1 are used to generate variable-period, variable-duty PWM output. Figure 3.2.1 shows the operation timing, Figure 3.2.2 shows the connection diagram, and Figures 3.2.3 and 3.2.4 show the set-up procedure.

Use the following peripheral functions:

- Timer mode of timer X
- One-shot timer mode of timer X

Specifications

- (1) Set timer X0 in timer mode, and set timer X1 in one-shot timer mode with pulse-output function.
- (2) Set 1 ms, the PWM period, to timer X0. Set 500 μ s, the width of PWM "H" pulse, to timer X1. Both timer X0 and timer X1 use f1 for the count source.
- (3) Connect a 10-MHz oscillator to XIN.

Operation

- (1) Setting the count start flag to "1" causes the counter of timer X0 to begin counting. The counter of timer X0 performs a down count on count source f1.
- (2) If the counter of timer X0 underflows, the counter reloads the content of the reload register and continues counting. At this time, the timer X0 interrupt request bit goes to "1".
- (3) An underflow in timer X0 triggers the counter of timer X1 and causes it to begin counting. When the counter of timer X1 begins counting, the output level of the TX1INOUT pin goes to "H".
- (4) As soon as the count of the counter of timer X1 becomes "0000₁₆", the output level of TX1INOUT pin goes to "L", and the counter reloads the content of the reload register and stops counting. At the same time, the timer X1 interrupt request bit goes to "1".

Timer X Applications

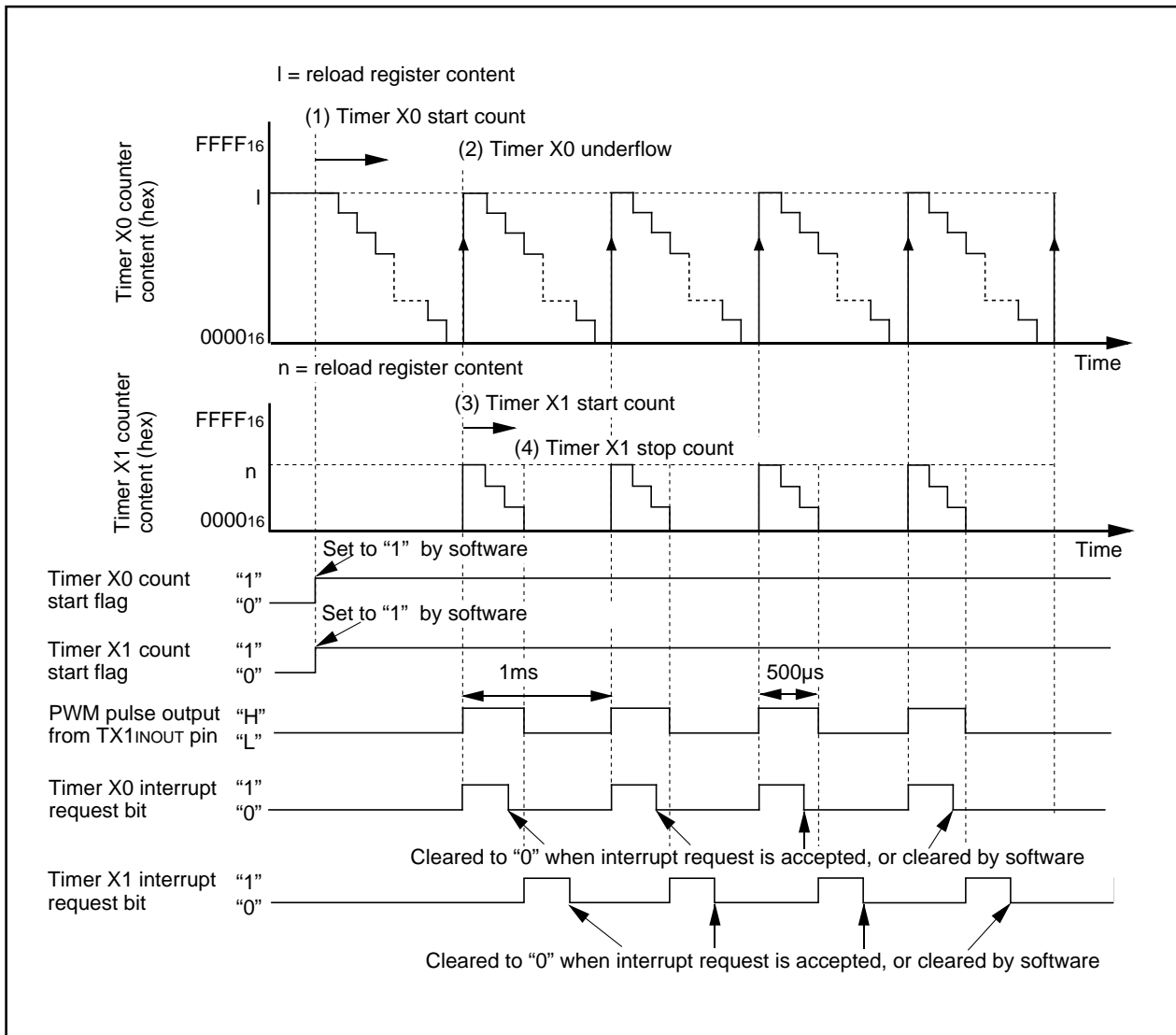


Figure 3.2.1. Operation timing of variable-period variable-duty PWM output

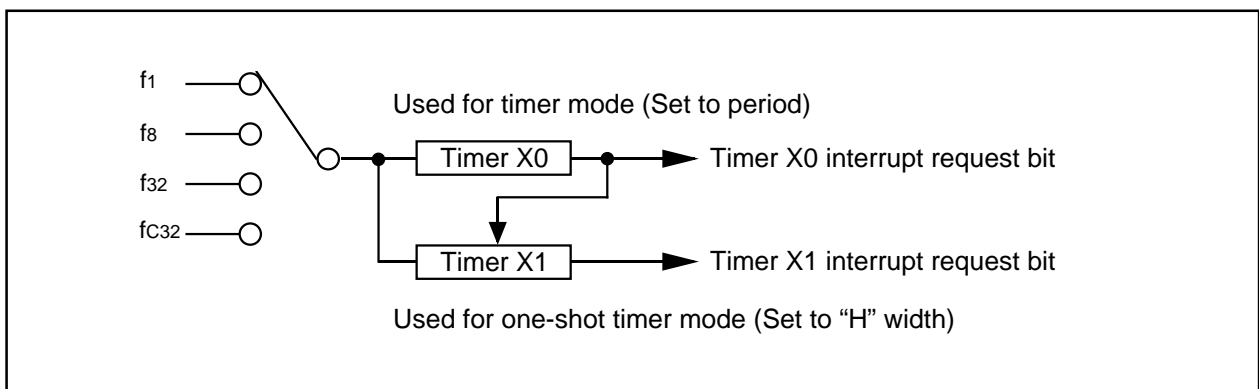
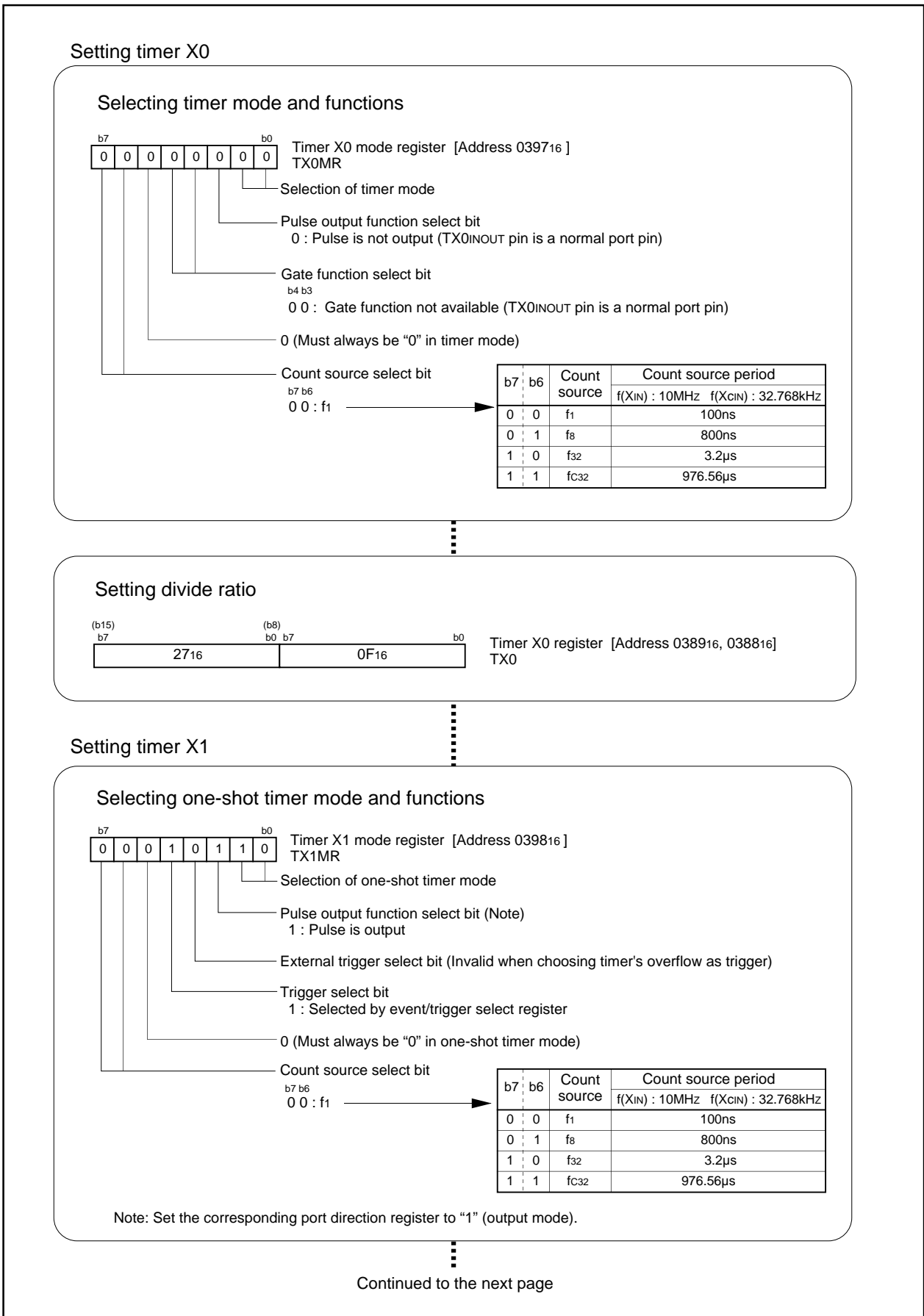


Figure 3.2.2. Connection diagram of variable-period variable-duty PWM output

Timer X Applications



Timer X Applications

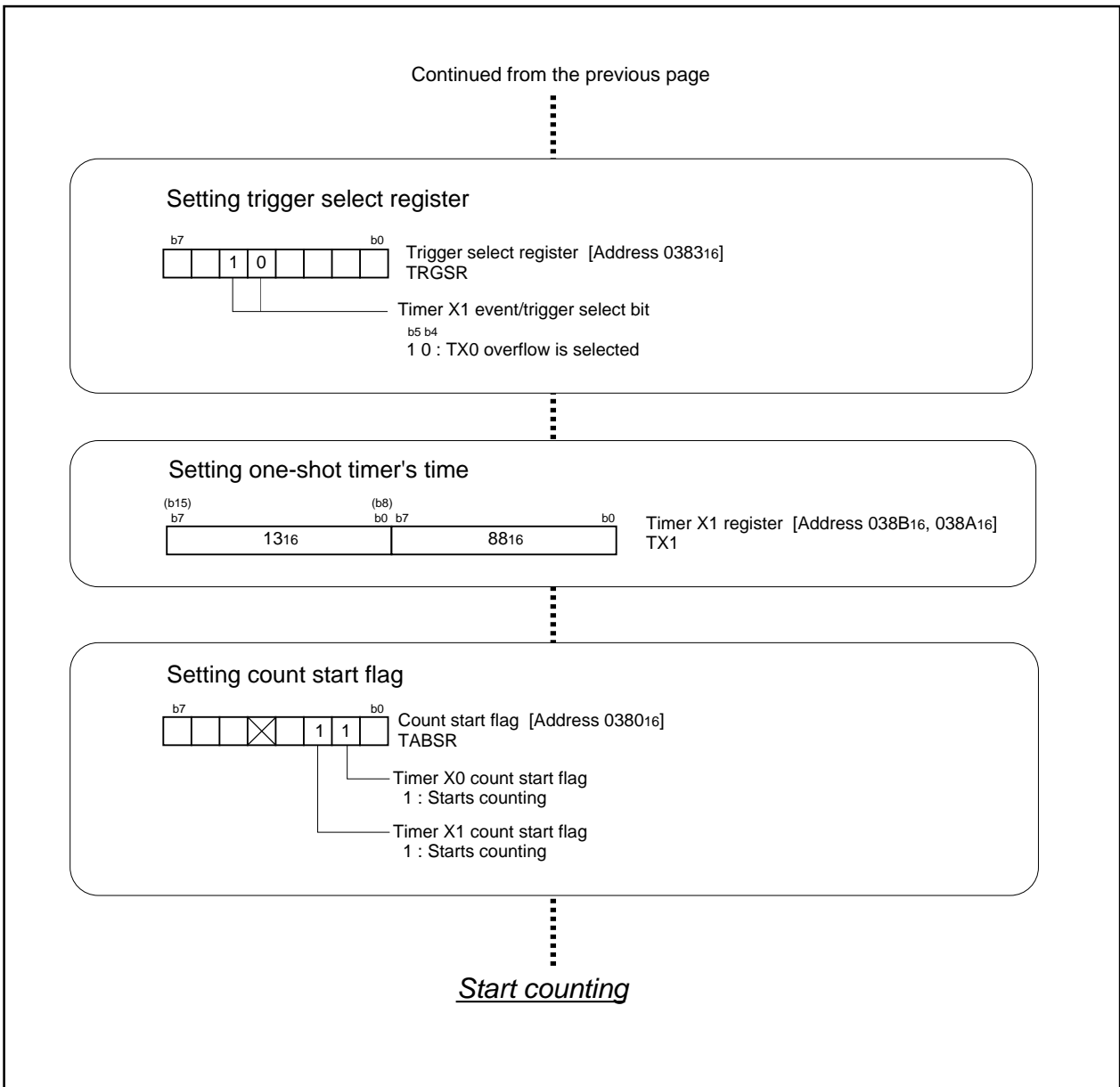


Figure 3.2.4. Set-up procedure of variable-period variable-duty PWM output (2)

3.3 Delayed One-Shot Output

Overview The following are steps of outputting a pulse only once after a specified elapse since an external trigger is input. Figure 3.3.1 shows the operation timing, Figure 3.3.2 shows the connection diagram, and Figures 3.3.3 and 3.3.4 show the set-up procedure.

Use the following peripheral function:

- One-shot timer mode of timer X

Specifications

- (1) Set timer X0 in one-shot timer mode, and set timer X1 in one-shot timer mode with pulse-output function.
- (2) Set 1 ms, an interval before a pulse is output, in timer X0; and set 50 μ s, a pulse width, in timer X1. Both timer X0 and timer X1 use f1 for the count source.
- (3) Connect a 10-MHz oscillator to XIN.

- Operation**
- (1) Setting the trigger select bit to "1" and setting the count start flag to "1" enables the counter of timer X0 to count.
 - (2) If an effective edge, selected by use of the external trigger select bit, is input to the TX0INOUT pin, the counter begins a down count. The counter of timer X0 performs a down count on count source f1.
 - (3) As soon as the counter of timer X0 becomes "0000₁₆", the counter reloads the content of the reload register and stops counting. At this time, the timer X0 interrupt request bit goes to "1".
 - (4) An underflow in timer X0 triggers the counter of timer X1 and causes it to begin counting. When timer X1 begins counting, the output level of the TX1INOUT pin goes to "H".
 - (5) As soon as the counter of timer X1 becomes "0000₁₆", the output level of the TX1INOUT pin goes to "L", the counter reloads the content of the reload register, and stops counting. At this time, timer X1 interrupt request bit goes to "1".

Timer X Applications

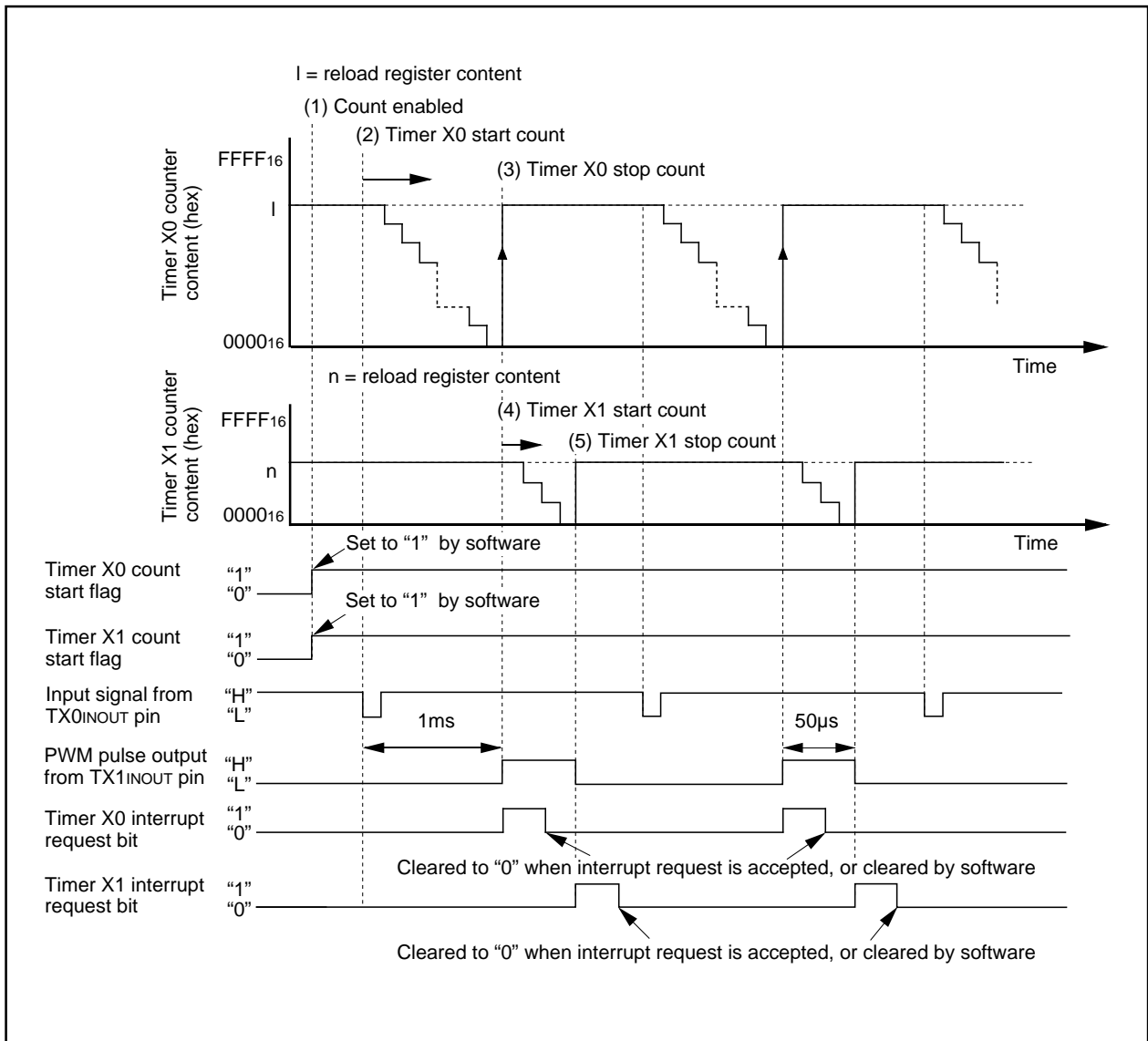


Figure 3.3.1. Operation timing of delayed one-shot output

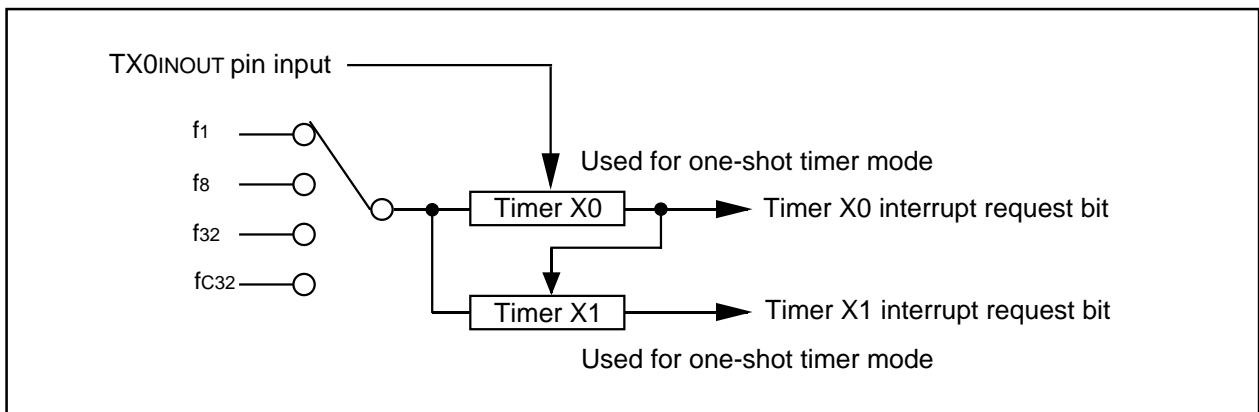
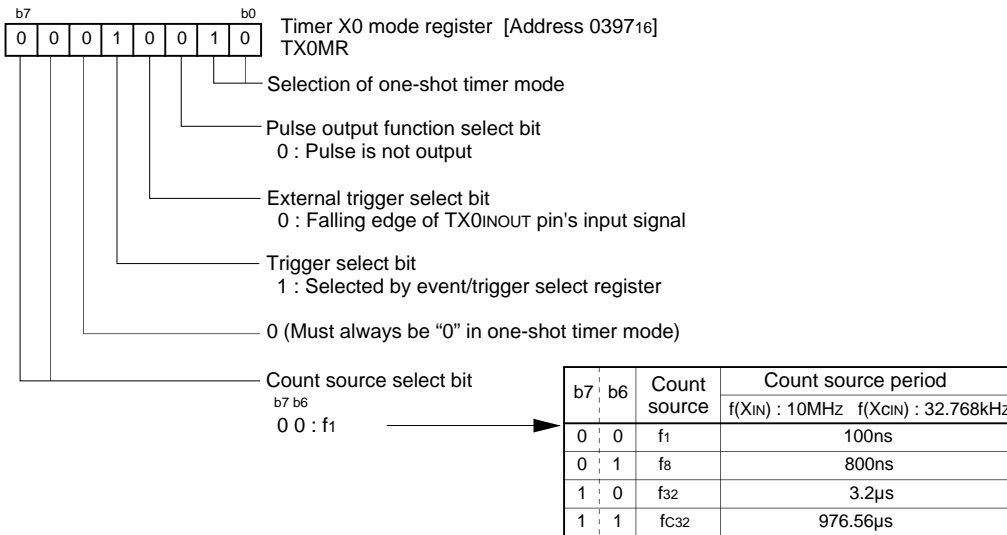


Figure 3.3.2. Connection diagram of delayed one-shot output

Timer X Applications

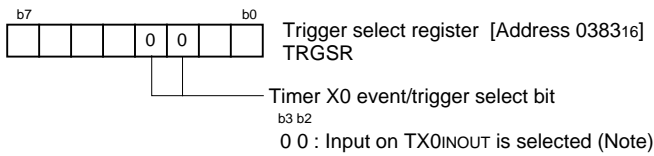
Setting timer X0

Selecting one-shot timer mode and functions



⋮

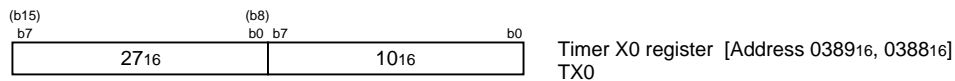
Setting trigger select register
(Select TX0INOUT pin to input TX0 trigger)



Note: Set the corresponding port direction register to "0" (input mode).

⋮

Setting delay time



⋮

Continued to the next page

Figure 3.3.3. Set-up procedure of delayed one-shot output (1)

Timer X Applications

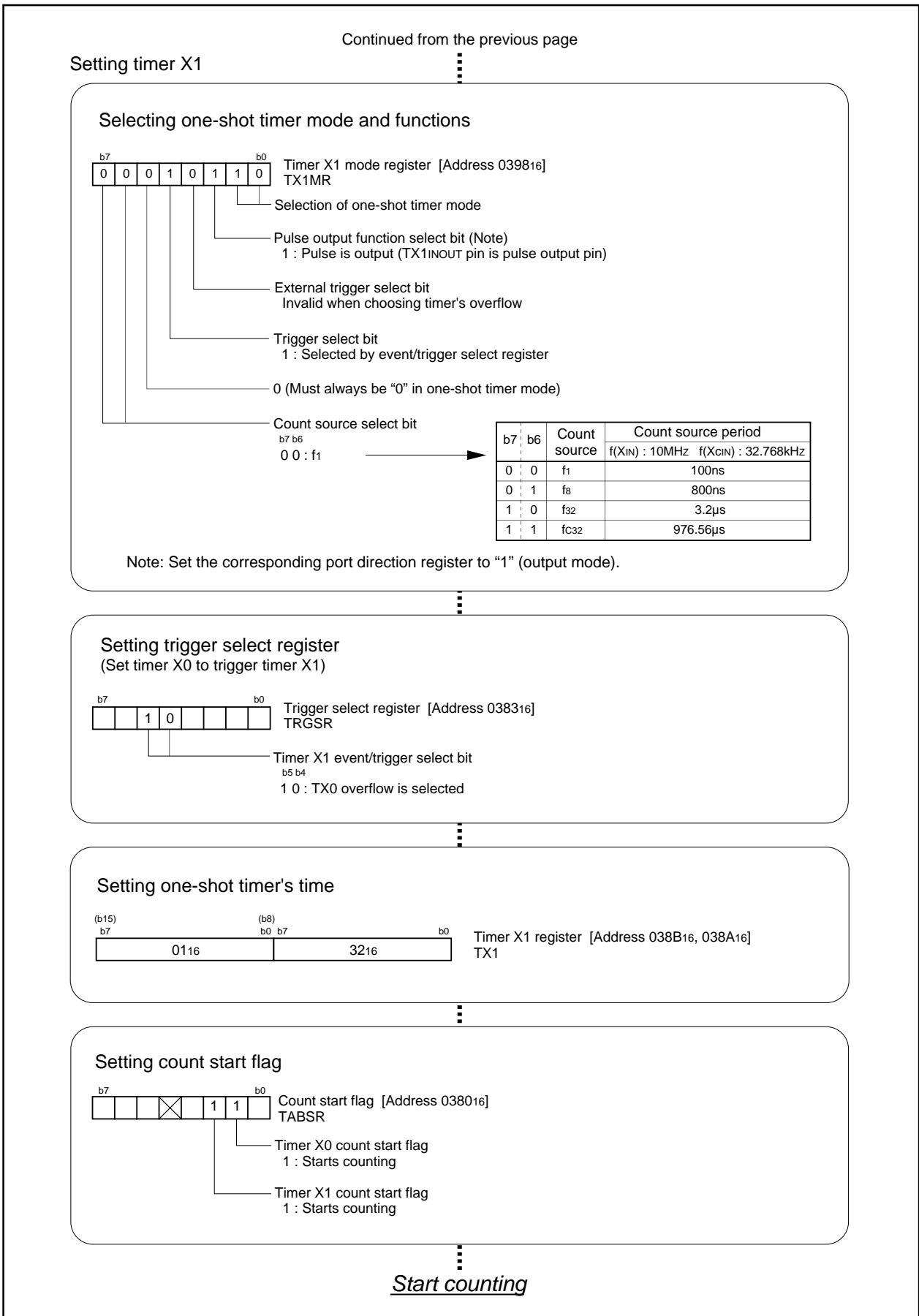


Figure 3.3.4. Set-up procedure of delayed one-shot output (2)

Timer X Applications

3.4 Buzzer Output

Overview The timer mode is used to make the buzzer ring. Figure 3.4.1 shows the operation timing, and Figure 3.4.2 shows the set-up procedure.

Use the following peripheral function:

- The pulse-outputting function in timer mode of timer X.

Specifications

- (1) Sound a 2-kHz buzz beep by use of timer X0.
- (2) Effect pull-up in the relevant port by use of a pull-up resistor. When the buzzer is off, set the port high-impedance, and stabilize the potential resulting from pulling up.
- (3) Connect a 10-MHz oscillator to XIN.

Operation (1) The microcomputer begins performing a count on timer X0. Timer X0 has disabled interrupts.
 (2) P43 is TX0INOUT pin. Setting the port P43 direction register to "1" (output mode) and outputs 2-kHz pulses.
 (3) The microcomputer stops outputting pulses by setting the port P43 direction register to "0" (input mode). P43 goes to an input pin, and the output from the pin becomes high-impedance.

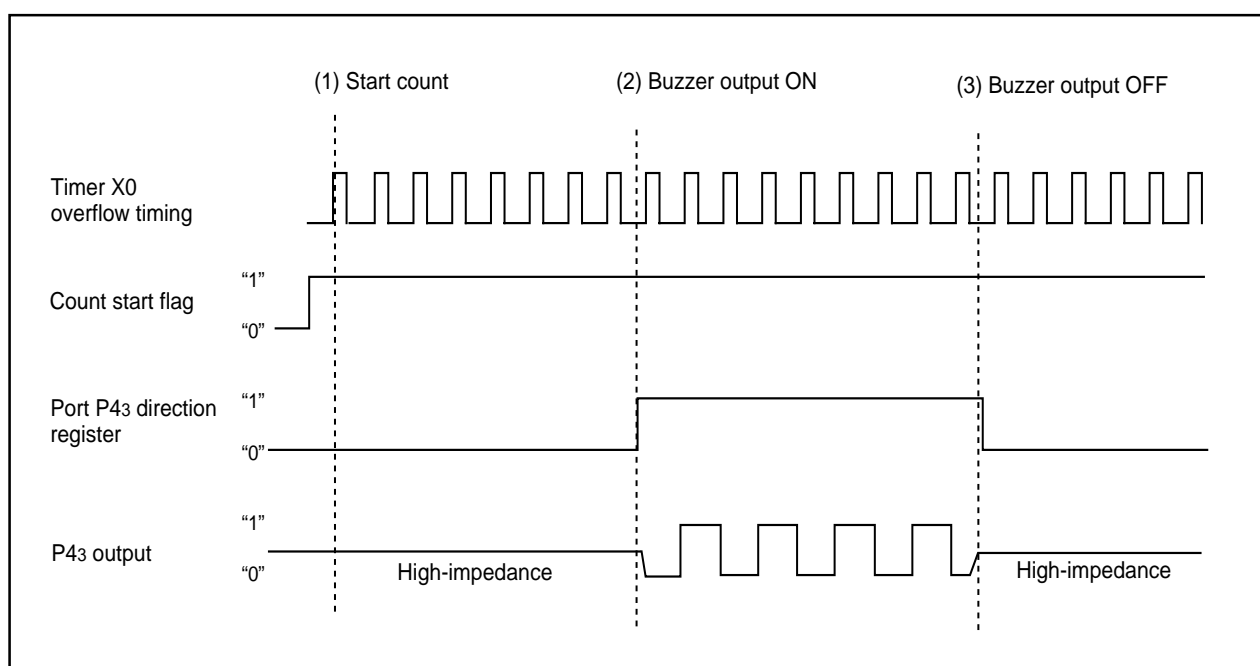


Figure 3.4.1. Operation timing of buzzer output

Timer X Applications

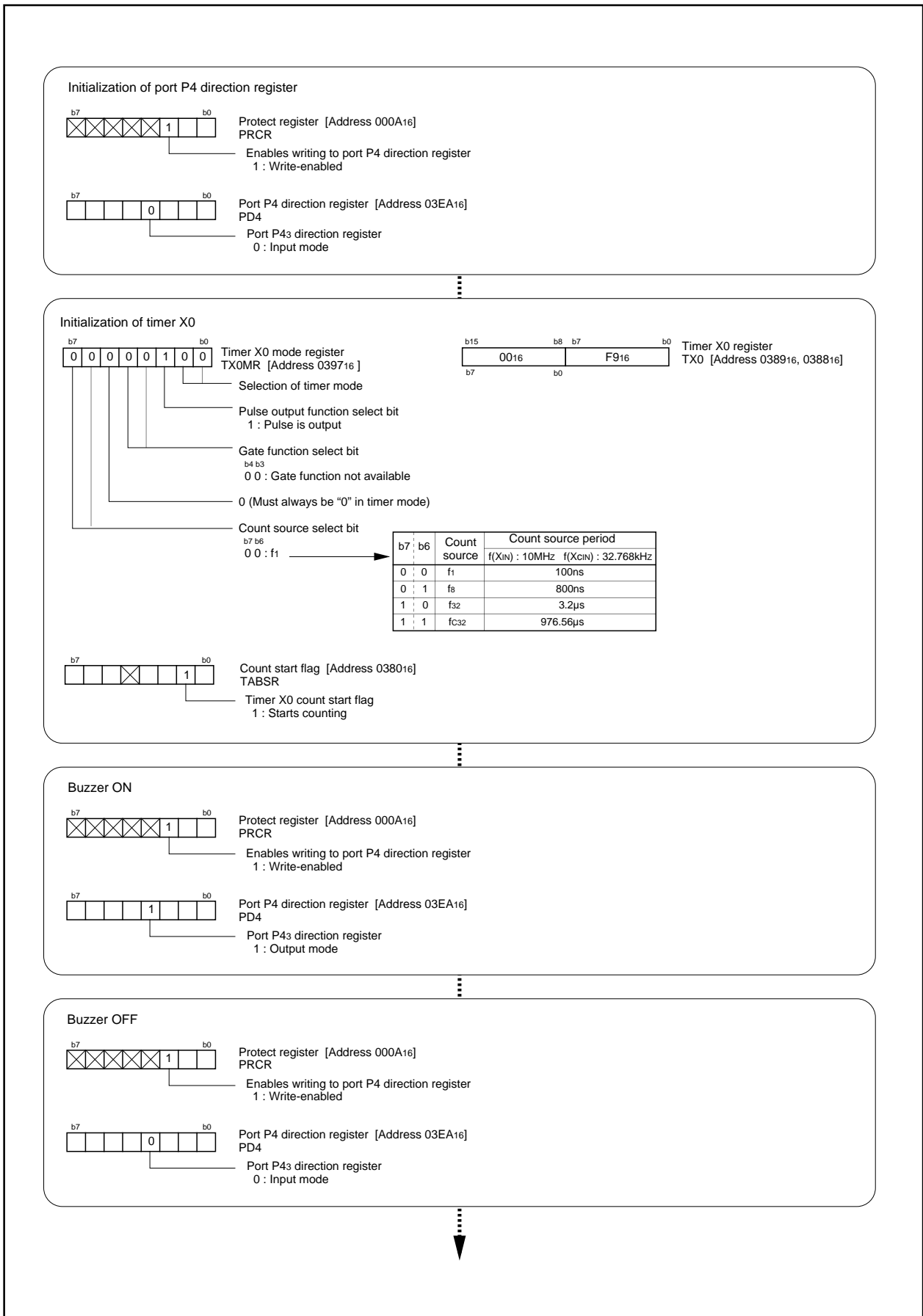


Figure 3.4.2. Set-up procedure of buzzer output

3.5 Solution for External Interrupt Pins Shortage

Overview The following are solution for external interrupt pins shortage. Figure 3.5.1 shows the set-up procedure.

Use the following peripheral function:

- Event counter mode of timer X

Specifications

(1) Inputting a falling edge to the TX0INOUT pin generates a timer X0 interrupt.

Operation (1) Set timer X0 to event counter mode, set timer to "0", and set interrupt priority levels in timer X0.
(2) Inputting a falling edge to the TX0INOUT pin generates a timer X0 interrupt.

Timer X Applications

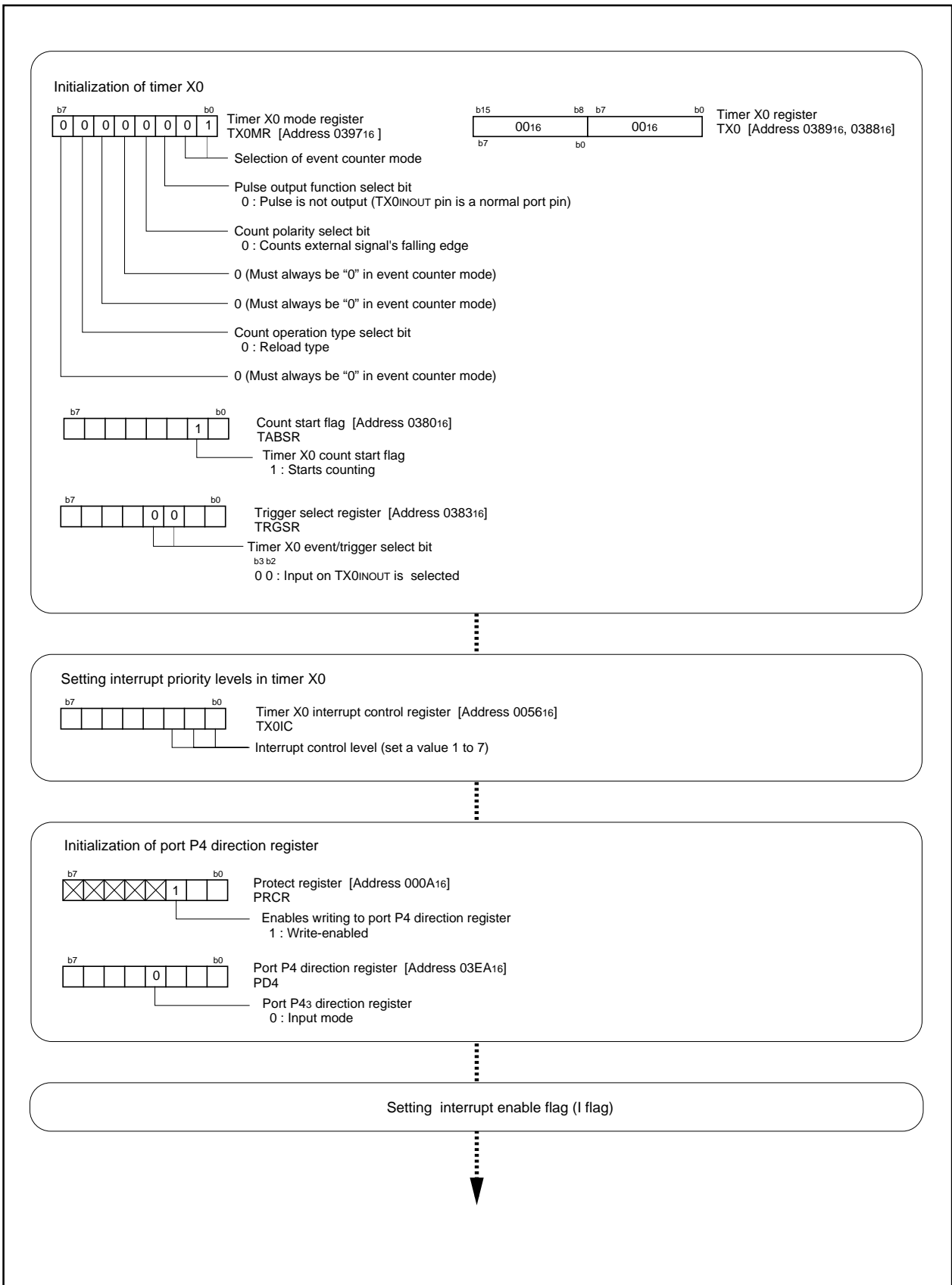


Figure 3.5.1. Set-up procedure of solution for a shortage of external interrupt pins

Controlling Power Applications

3.6 Controlling Power Using Stop Mode

Overview The following are steps for controlling power using stop mode. Figure 3.6.1 shows the operation timing, Figure 3.6.2 shows an example of circuit, and Figures 3.6.3 and 3.6.4 show the set-up procedure.

Use the following peripheral functions:

- Key-input interrupts
- Stop mode
- Pull-up function

Specifications

- (1) Use P30 through P33 for the scan output pins of a key matrix. Use the input pins ($\overline{KI0}$ through $\overline{KI7}$) of the key-input interrupt function for the key-input reading pins. The pull-up function is also used.
- (2) If a key-input interrupt request occurs, clear the stop mode and read a key.

- Operation**
- (1) Enable a key-input interrupt and set the pull-up function to pins $\overline{KI0}$ through $\overline{KI7}$. Change the output of P30 through P33 to "L" and enter stop mode.
 - (2) If a key is pressed, "L" is input to one of pins $\overline{KI0}$ through $\overline{KI7}$ to clear stop mode. A key-input interrupt occurs to execute the key-input interrupt handling routine.
 - (3) Sequentially set P30 through P33 to "L" to determine which key was pressed.
 - (4) When the process to determine the key pressed is completed, change the output from P30 through P33 to "L" again and enter stop mode.

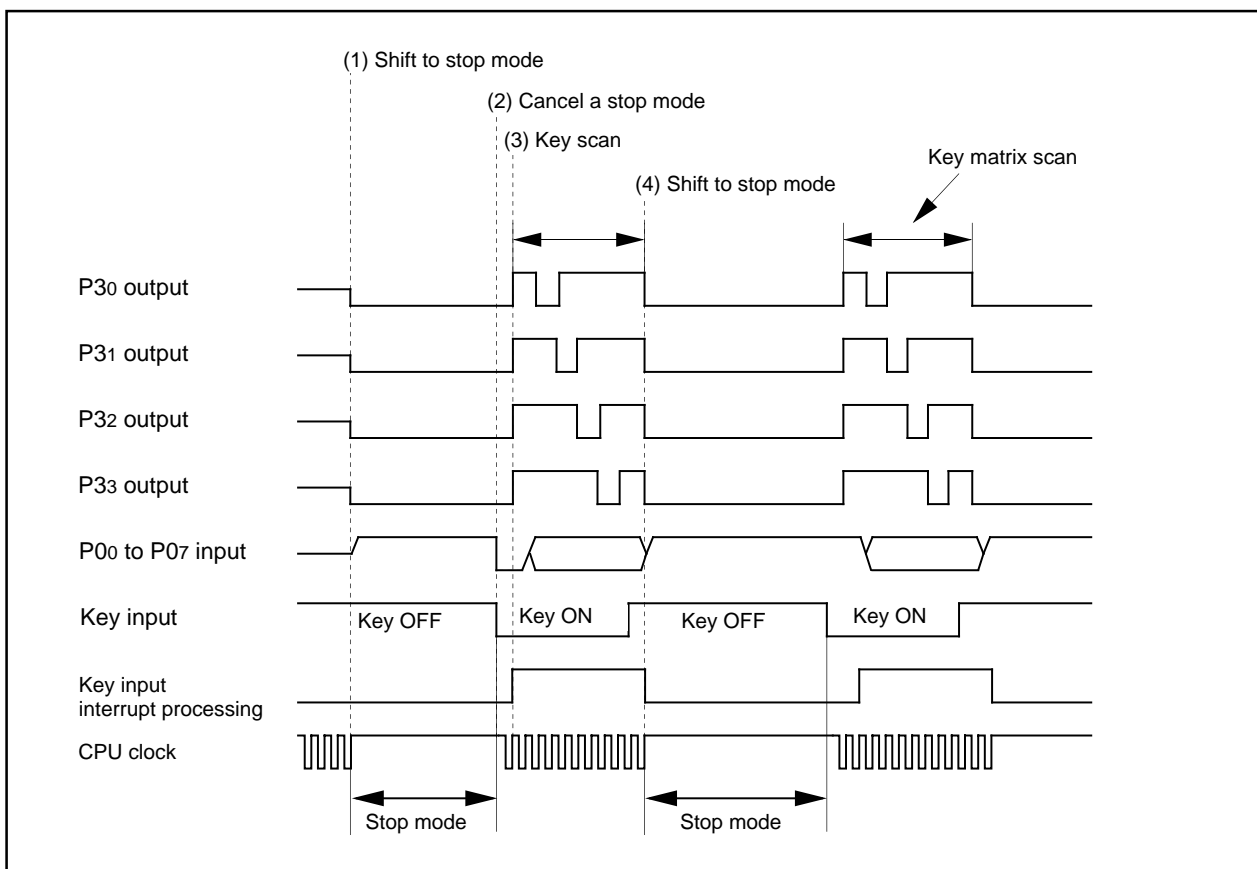


Figure 3.6.1. Operation timing of controlling power using stop mode

Controlling Power Applications

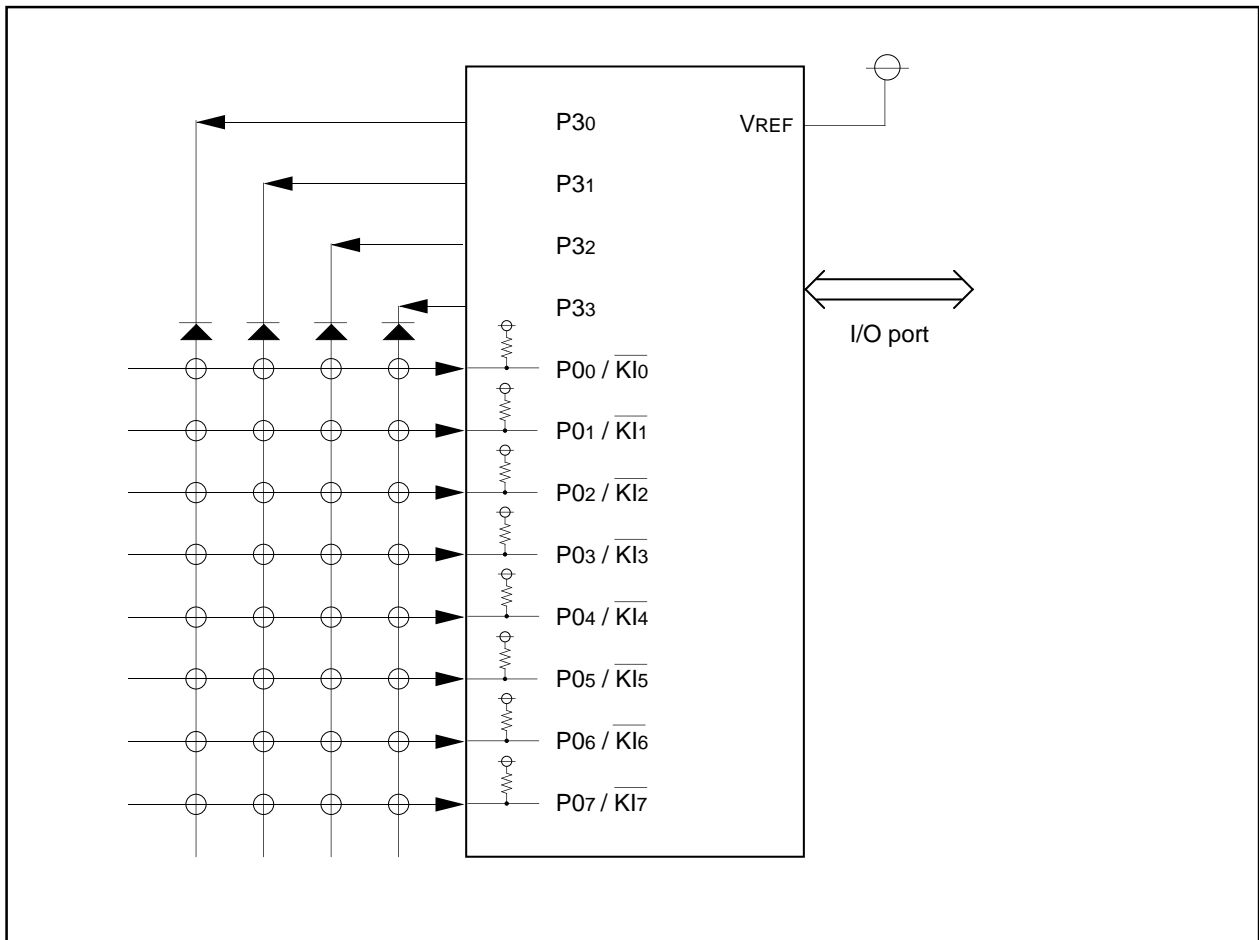


Figure 3.6.2. Example of circuit of controlling power using stop mode

Controlling Power Applications

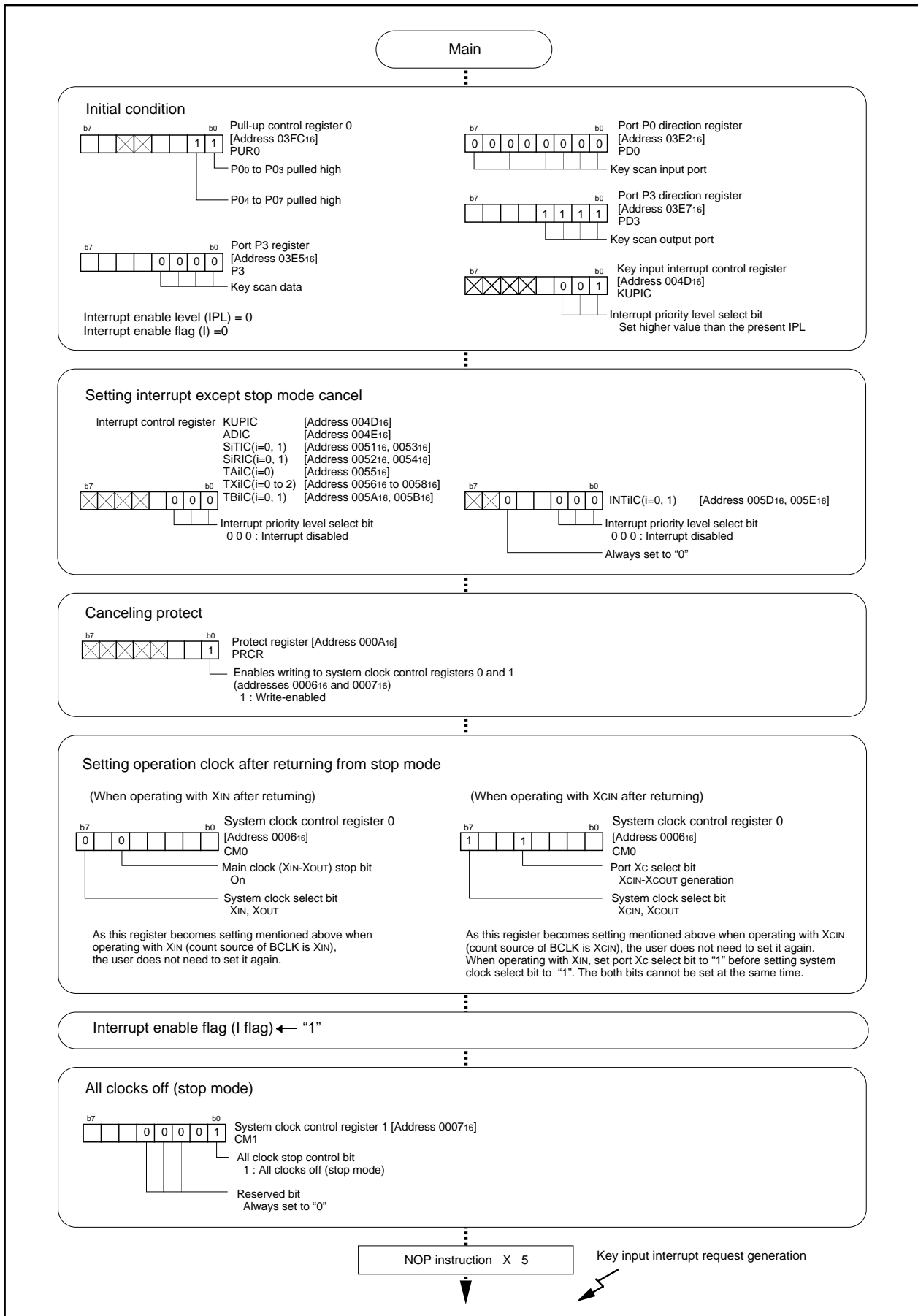


Figure 3.6.3. Set-up procedure of controlling power using stop mode (1)

Controlling Power Applications

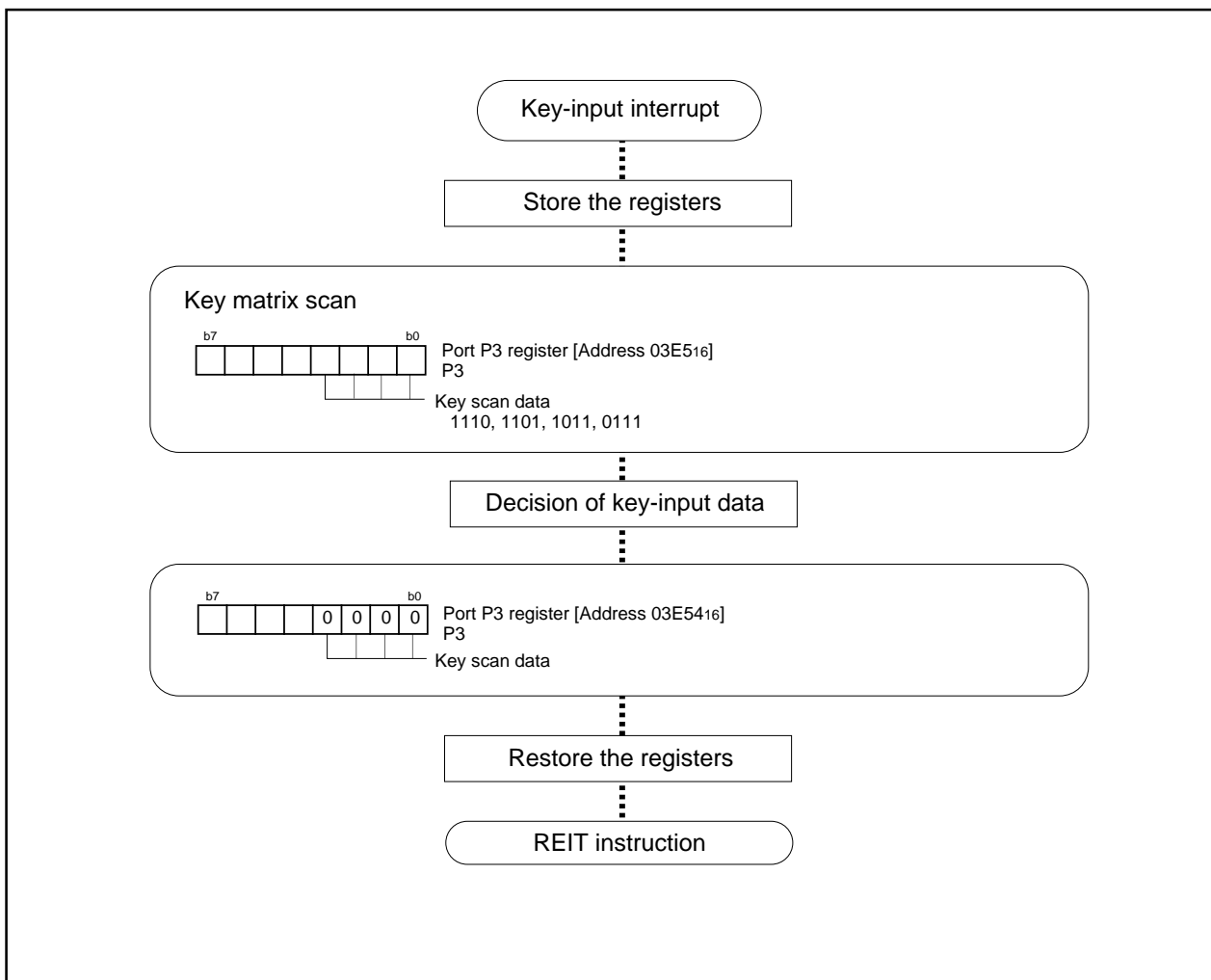


Figure 3.6.4. Set-up procedure of controlling power using stop mode (2)

Controlling Power Applications

3.7 Controlling Power Using Wait Mode

Overview The following are steps for controlling power using wait mode. Figure 3.7.1 shows the operation timing, and Figures 3.7.2 to 3.7.4 show the set-up procedure.

Use the following peripheral functions:

- Timer mode of timer B
- Wait mode

A flag named "F-WIT" is used in the set-up procedure. The purpose of this flag is to decide whether or not to clear wait mode. If F_WIT = "1" in the main program, the wait mode is entered; if F_WIT = "0", the wait mode is cleared.

Specifications

- (1) Connect a 32.768-kHz oscillator to XCIN to serve as the timer count source. As interrupts occur every one second, which is a count the timer reaches, the controller returns from wait mode and count the clock using a program.
- (2) Clear wait mode if a $\overline{\text{INT0}}$ interrupt request occurs.

Operation

- (1) Switch the system clock from XIN to XCIN to get low-speed mode.
- (2) Stop XIN and enter wait mode. In this instance, enable the timer B0 interrupt and the $\overline{\text{INT0}}$ interrupt.
- (3) When a timer B0 interrupt request occurs (at 1-second intervals), start supplying the BCLK from XCIN. At this time, count the clock within the routine that handles the timer B0 interrupts and enter wait mode again.
- (4) If a $\overline{\text{INT0}}$ interrupt occurs, start supplying the BCLK from XCIN. Start the XIN oscillation within the $\overline{\text{INT0}}$ interrupt, and switch the system clock to XIN.

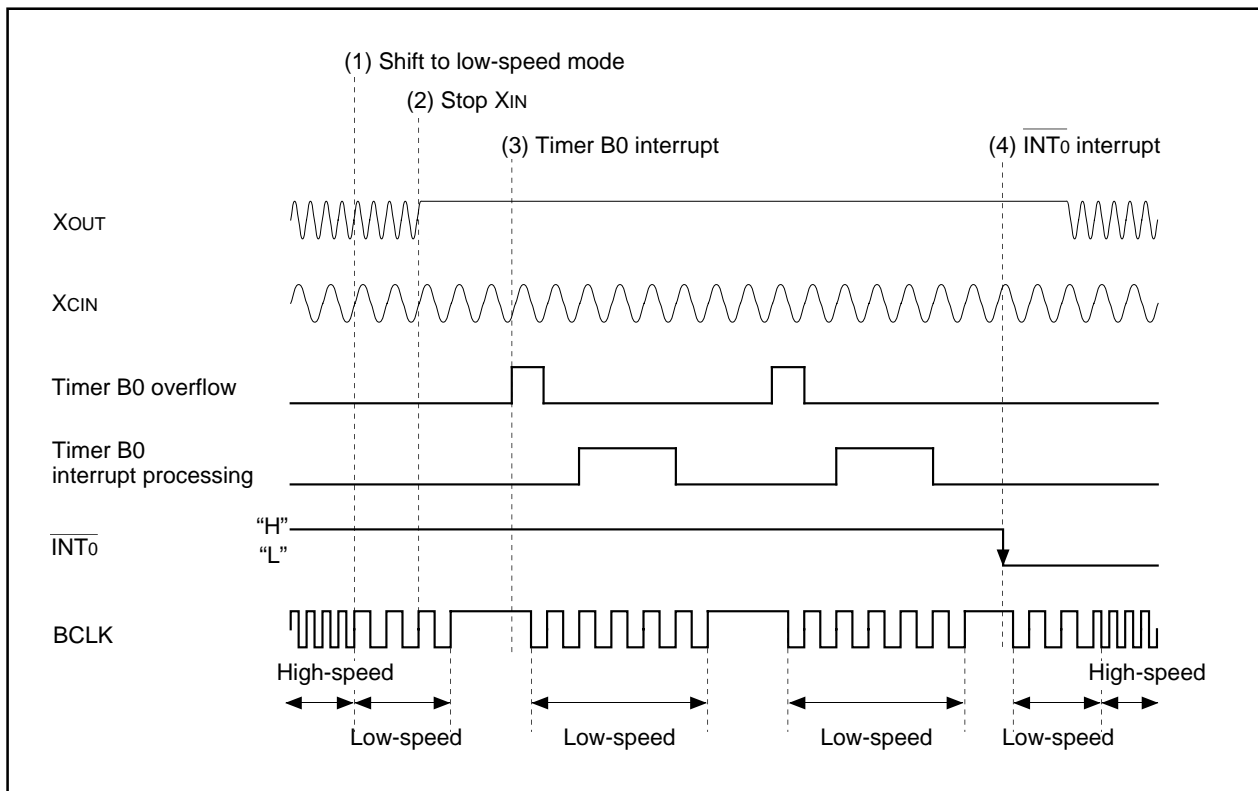


Figure 3.7.1. Operation timing of controlling power using wait mode

Controlling Power Applications

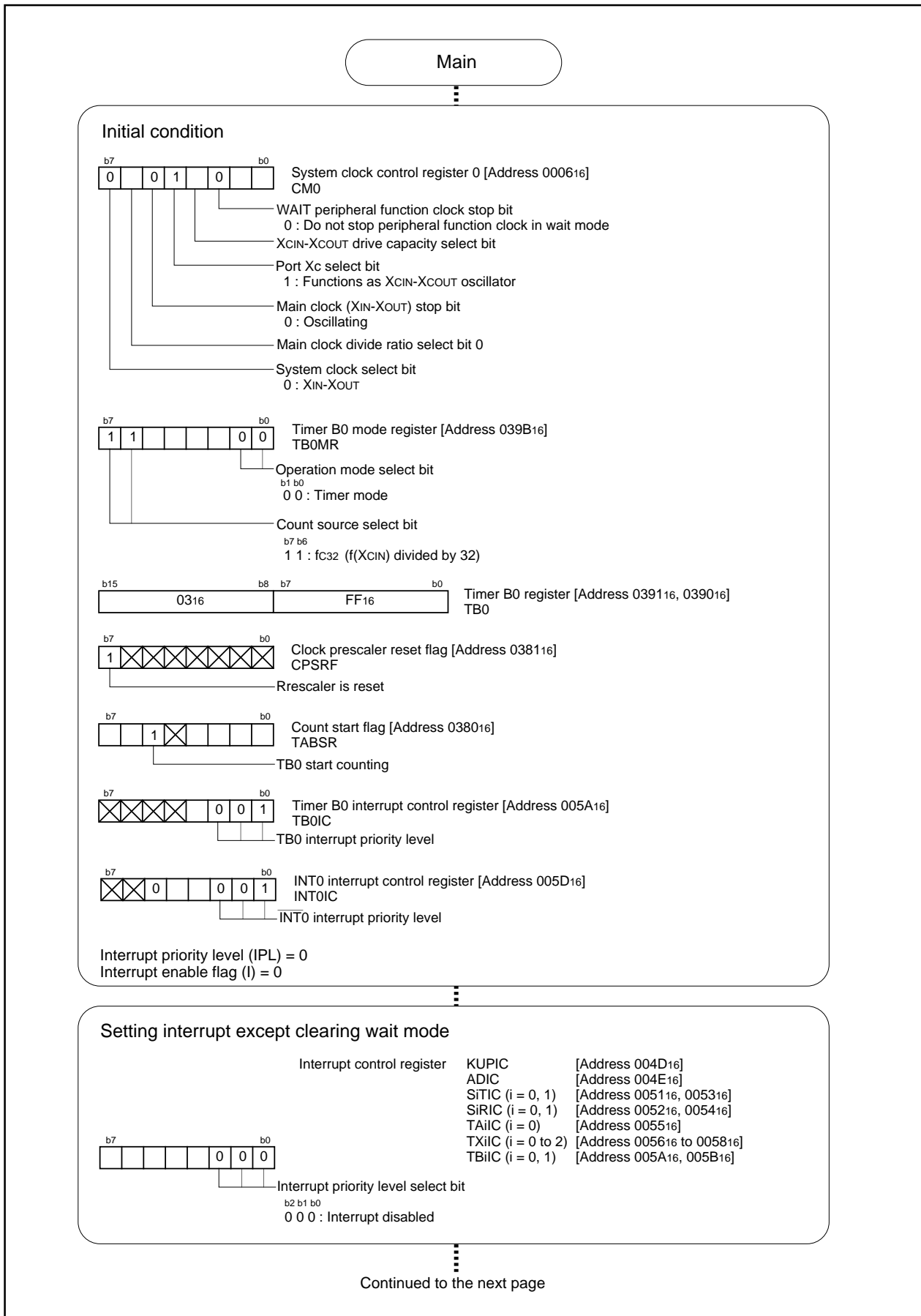


Figure 3.7.2. Set-up procedure of controlling power using wait mode (1)

Controlling Power Applications

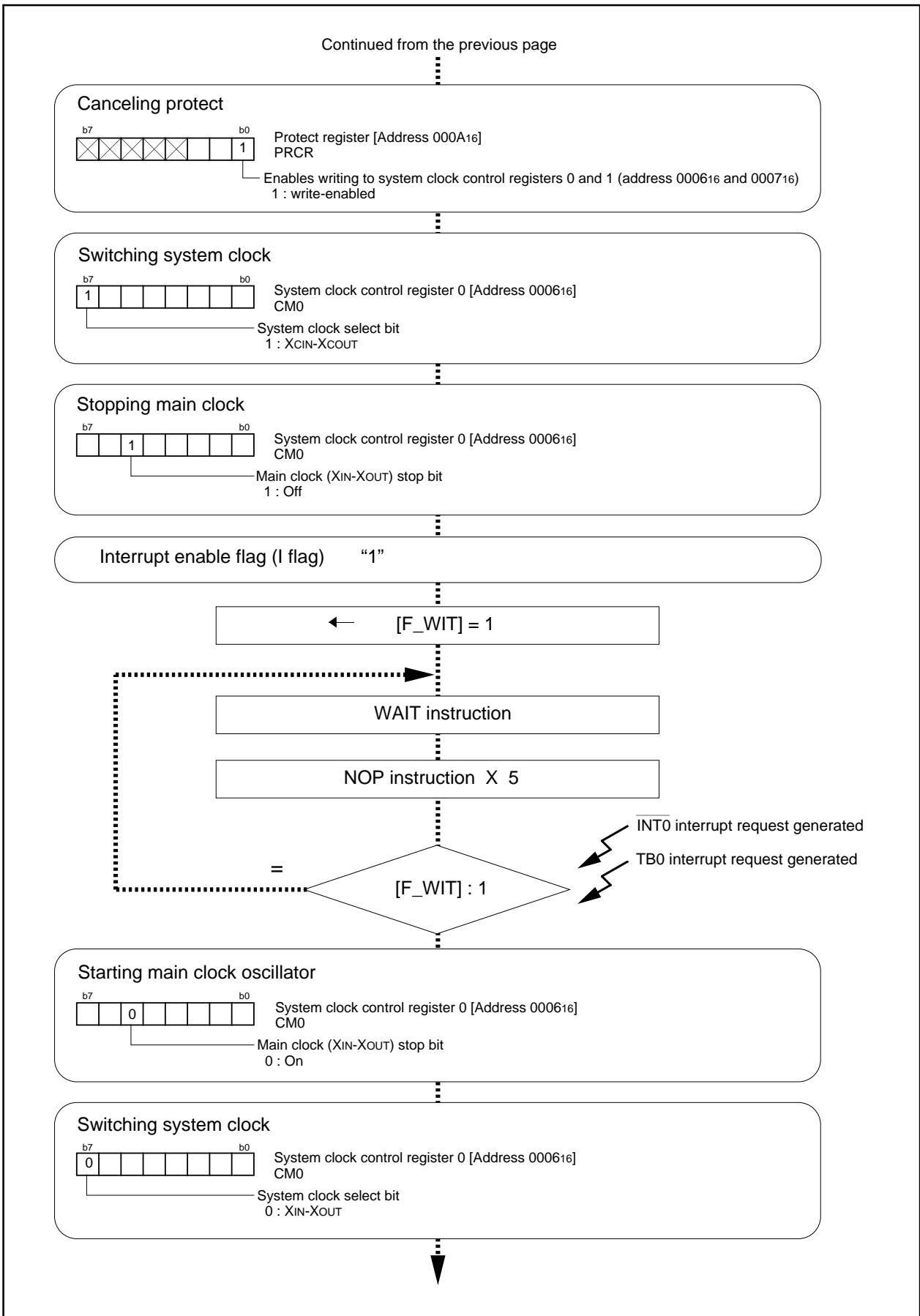


Figure 3.7.3. Set-up procedure of controlling power using wait mode (2)

Controlling Power Applications

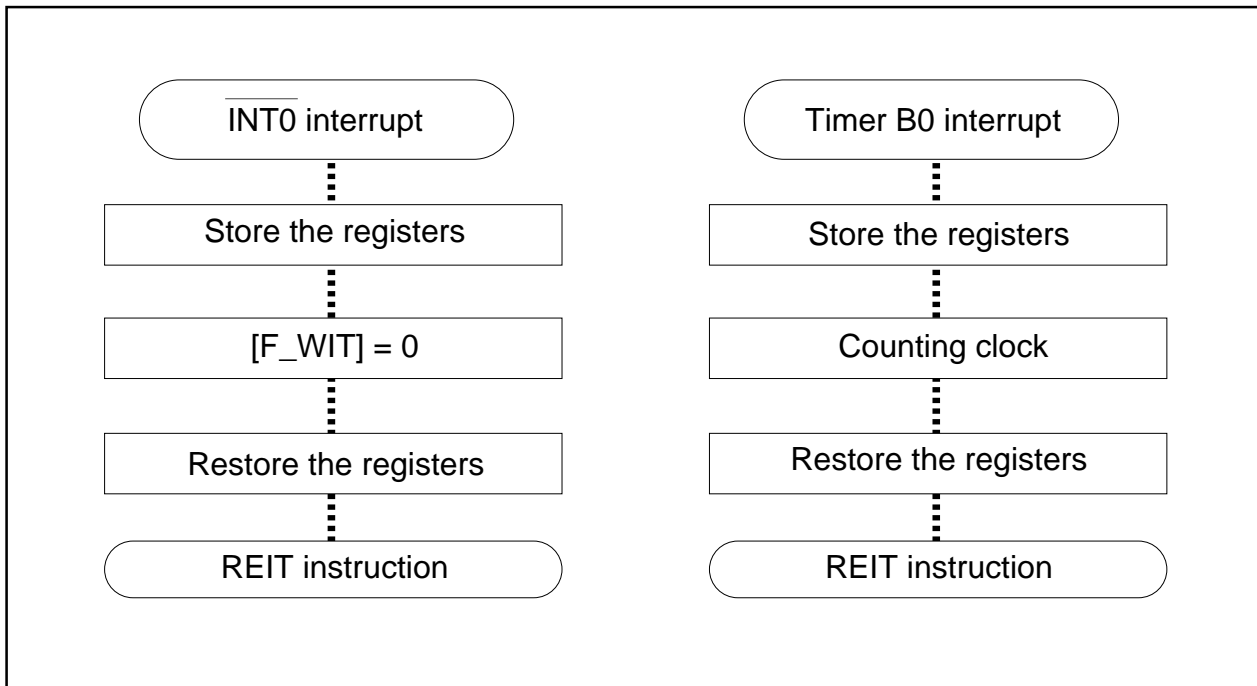


Figure 3.7.4. Set-up procedure of controlling power using wait mode (3)

Controlling Power Applications

[MEMO]

Chapter 4

Interrupt

Interrupt

4.1 Overview of Interrupt

4.1.1 Type of Interrupts

Figure 4.1.1 lists the types of interrupts.

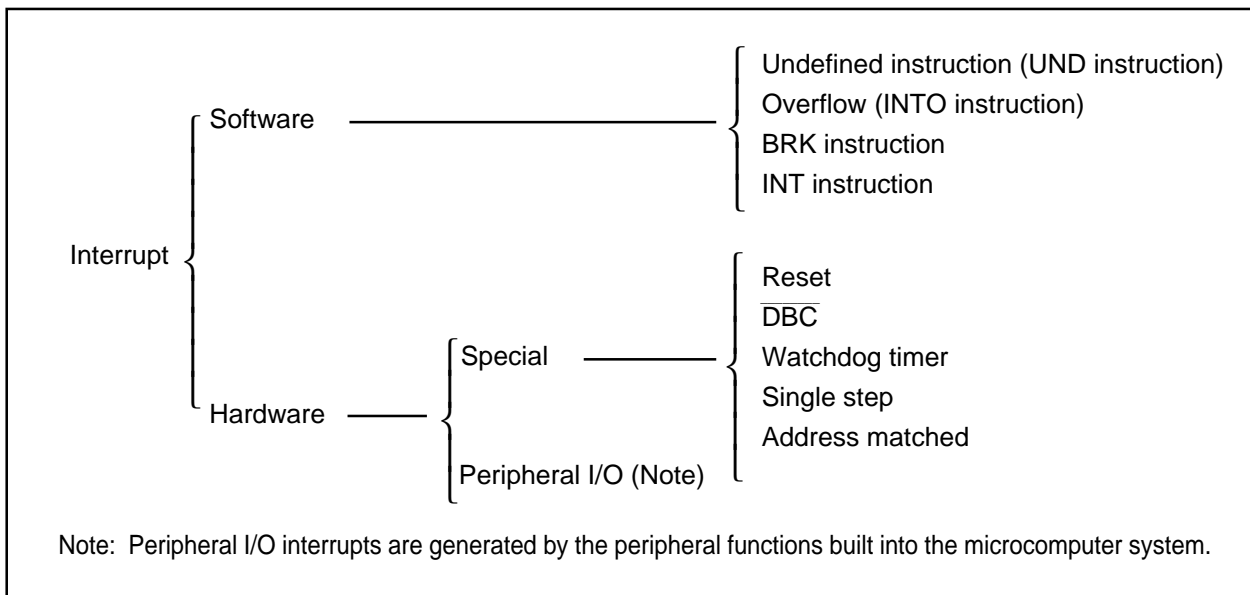


Figure 4.1.1. Classification of interrupts

- Maskable interrupt : An interrupt which can be enabled (disabled) by the interrupt enable flag (I flag) or whose interrupt priority **can be changed** by priority level.
- Non-maskable interrupt : An interrupt which cannot be enabled (disabled) by the interrupt enable flag (I flag) or whose interrupt priority **cannot be changed** by priority level.

4.1.2 Software Interrupts

A software interrupt occurs when executing certain instructions. Software interrupts are non-maskable interrupts.

- **Undefined instruction interrupt**

An undefined instruction interrupt occurs when executing the UND instruction.

- **Overflow interrupt**

An overflow interrupt occurs when executing the INTO instruction with the overflow flag (O flag) set to "1". The following are instructions whose O flag changes by arithmetic:

ABS, ADC, ADCF, ADD, CMP, DIV, DIVU, DIVX, NEG, RMPA, SBB, SHA, SUB

- **BRK interrupt**

A BRK interrupt occurs when executing the BRK instruction.

- **INT interrupt**

An INT interrupt occurs when assigning one of software interrupt numbers 0 through 63 and executing the INT instruction. Software interrupt numbers 0 through 31 are assigned to peripheral I/O interrupts, so executing the INT instruction allows executing the same interrupt routine that a peripheral I/O interrupt does.

The stack pointer (SP) used for the INT interrupt is dependent on which software interrupt number is involved.

So far as software interrupt numbers 0 through 31 are concerned, the microcomputer saves the stack pointer assignment flag (U flag) when it accepts an interrupt request. If change the U flag to "0" and select the interrupt stack pointer (ISP), and then execute an interrupt sequence. When returning from the interrupt routine, the U flag is returned to the state it was before the acceptance of interrupt request. So far as software numbers 32 through 63 are concerned, the stack pointer does not make a shift.

4.1.3 Hardware Interrupts

Hardware interrupts are classified into two types — special interrupts and peripheral I/O interrupts.

(1) Special interrupts

Special interrupts are non-maskable interrupts.

- **Reset**

Reset occurs if an “L” is input to the $\overline{\text{RESET}}$ pin.

- **DBC interrupt**

This interrupt is exclusively for the debugger, do not use it in other circumstances.

- **Watchdog timer interrupt**

Generated by the watchdog timer.

- **Single-step interrupt**

This interrupt is exclusively for the debugger, do not use it in other circumstances. With the debug flag (D flag) set to “1”, a single-step interrupt occurs after one instruction is executed.

- **Address match interrupt**

An address match interrupt occurs immediately before the instruction held in the address indicated by the address match interrupt register is executed with the address match interrupt enable bit set to “1”. If an address other than the first address of the instruction in the address match interrupt register is set, no address match interrupt occurs. For address match interrupt, see 2.9 Address match Interrupt.

(2) Peripheral I/O interrupts

A peripheral I/O interrupt is generated by one of built-in peripheral functions. Built-in peripheral functions are dependent on classes of products, so the interrupt factors too are dependent on classes of products. The interrupt vector table is the same as the one for software interrupt numbers 0 through 31 the INI instruction uses. Peripheral I/O interrupts are maskable interrupts.

- **Key-input interrupt**

A key-input interrupt occurs if an “L” is input to the $\overline{\text{KI}}$ pin.

- **A-D conversion interrupt**

This is an interrupt that the A-D converter generates.

- **UART0 and UART1 transmission interrupt**

These are interrupts that the serial I/O transmission generates.

- **UART0 and UART1 reception interrupt**

These are interrupts that the serial I/O reception generates.

- **Timer A0 interrupt**

This is an interrupt that timer A generates.

- **Timer B0 interrupt and timer B1 interrupt**

These are interrupts that timer B generates.

- **Timer X0 interrupt through timer X2 interrupt**

- **$\overline{\text{INT0}}$ interrupt and $\overline{\text{INT1}}$ interrupt**

An $\overline{\text{INT}}$ interrupt occurs if either a rising edge or a falling edge is input to the $\overline{\text{INT}}$ pin.

Interrupt

4.1.4 Interrupts and Interrupt Vector Tables

If an interrupt request is accepted, a program branches to the interrupt routine set in the interrupt vector table. Set the first address of the interrupt routine in each vector table. Two types of interrupt vector tables are available — fixed vector table in which addresses are fixed and variable vector table in which addresses can be varied by the setting.

- **Fixed vector tables**

The fixed vector table is a table in which addresses are fixed. The vector tables are located in an area extending from FFFDC₁₆ to FFFFF₁₆. One vector table comprises four bytes. Set the first address of interrupt routine in each vector table. Table 4.1.1 shows the interrupts assigned to the fixed vector tables and addresses of vector tables.

Table 4.1.1. Interrupts assigned to the fixed vector tables and addresses of vector tables

Interrupt source	Vector table addresses Address (L) to address (H)	Remarks
Undefined instruction	FFFD _{C16} to FFFD _{F16}	Interrupt on UND instruction
Overflow	FFFE ₀₁₆ to FFFE ₃₁₆	Interrupt on INTO instruction
BRK instruction	FFFE ₄₁₆ to FFFE ₇₁₆	If the vector contains FF ₁₆ , program execution starts from the address shown by the vector in the variable vector table
Address match	FFFE ₈₁₆ to FFFE _{B16}	There is an address-matching interrupt enable bit
Single step (Note)	FFFE _{C16} to FFFE _{F16}	Do not use
Watchdog timer	FFFF ₀₁₆ to FFFF ₃₁₆	
DBC (Note)	FFFF ₄₁₆ to FFFF ₇₁₆	Do not use
——	FFFF ₈₁₆ to FFFF _{B16}	——
Reset	FFFF _{C16} to FFFF _{F16}	

Note: Interrupts used for debugging purposes only.

Interrupt

• Variable vector tables

The addresses in the variable vector table can be modified, according to the user's settings. Indicate the first address using the interrupt table register (INTB). The 256-byte area subsequent to the address the INTB indicates becomes the area for the variable vector tables. One vector table comprises four bytes. Set the first address of the interrupt routine in each vector table. Table 4.1.2 shows the interrupts assigned to the variable vector tables and addresses of vector tables.

Table 4.1.2. Interrupts assigned to the variable vector tables and addresses of vector tables

Software interrupt number	Vector table address Address (L) to address (H)	Interrupt source	Remarks
Software interrupt number 0 —	+0 to +3 (Note)	BRK instruction —	Cannot be masked by I flag
Software interrupt number 11	+44 to +47 (Note)	—	
Software interrupt number 12	+48 to +51 (Note)	—	
Software interrupt number 13	+52 to +55 (Note)	Key input interrupt	
Software interrupt number 14 —	+56 to +59 (Note)	A-D —	
Software interrupt number 17	+68 to +71 (Note)	UART0 transmit	
Software interrupt number 18	+72 to +75 (Note)	UART0 receive	
Software interrupt number 19	+76 to +79 (Note)	UART1 transmit	
Software interrupt number 20	+80 to +83 (Note)	UART1 receive	
Software interrupt number 21	+84 to +87 (Note)	Timer A0	
Software interrupt number 22	+88 to +91 (Note)	Timer X0	
Software interrupt number 23	+92 to +95 (Note)	Timer X1	
Software interrupt number 24	+96 to +99 (Note)	Timer X2	
Software interrupt number 25	+100 to +103 (Note)	—	
Software interrupt number 26	+104 to +107 (Note)	Timer B0	
Software interrupt number 27	+108 to +111 (Note)	Timer B1	
Software interrupt number 28	+112 to +115 (Note)	—	
Software interrupt number 29	+116 to +119 (Note)	$\overline{\text{INT0}}$	
Software interrupt number 30	+120 to +123 (Note)	$\overline{\text{INT1}}$	
Software interrupt number 31	+124 to +127 (Note)	—	
Software interrupt number 32 to Software interrupt number 63	+128 to +131 (Note) to +252 to +255 (Note)	Software interrupt	Cannot be masked by I flag

Note : Address relative to address in interrupt table register (INTB).

Interrupt

4.2 Interrupt Control

Descriptions are given here regarding how to enable or disable maskable interrupts and how to set the priority to be accepted. What is described here does not apply to non-maskable interrupts.

Enable or disable a non-maskable interrupt using the interrupt enable flag (I flag), interrupt priority level selection bit, or processor interrupt priority level (IPL). Whether an interrupt request is present or absent is indicated by the interrupt request bit. The interrupt request bit and the interrupt priority level selection bit are located in the interrupt control register of each interrupt. Also, the interrupt enable flag (I flag) and the IPL are located in the flag register (FLG).

Table 4.2.1 shows the memory map of the interrupt control registers, and Table 4.2.2 shows the interrupt control registers.

004D ₁₆	Key input interrupt control register(KUPIC)
004E ₁₆	A-D conversion interrupt control register (ADIC)
004F ₁₆	
0050 ₁₆	
0051 ₁₆	UART0 transmit interrupt control register (S0TIC)
0052 ₁₆	UART0 receive interrupt control register (S0RIC)
0053 ₁₆	UART1 transmit interrupt control register(S1TIC)
0054 ₁₆	UART1 receive interrupt control register(S1RIC)
0055 ₁₆	Timer A0 interrupt control register (TA0IC)
0056 ₁₆	Timer X0 interrupt control register (TX0IC)
0057 ₁₆	Timer X1 interrupt control register (TX1IC)
0058 ₁₆	Timer X2 interrupt control register (TX2IC)
0059 ₁₆	
005A ₁₆	Timer B0 interrupt control register (TB0IC)
005B ₁₆	Timer B1 interrupt control register (TB1IC)
005C ₁₆	
005D ₁₆	INT0 interrupt control register (INT0IC)
005E ₁₆	INT1 interrupt control register (INT1IC)

Table 4.2.1. Memory map of the interrupt control registers

Interrupt

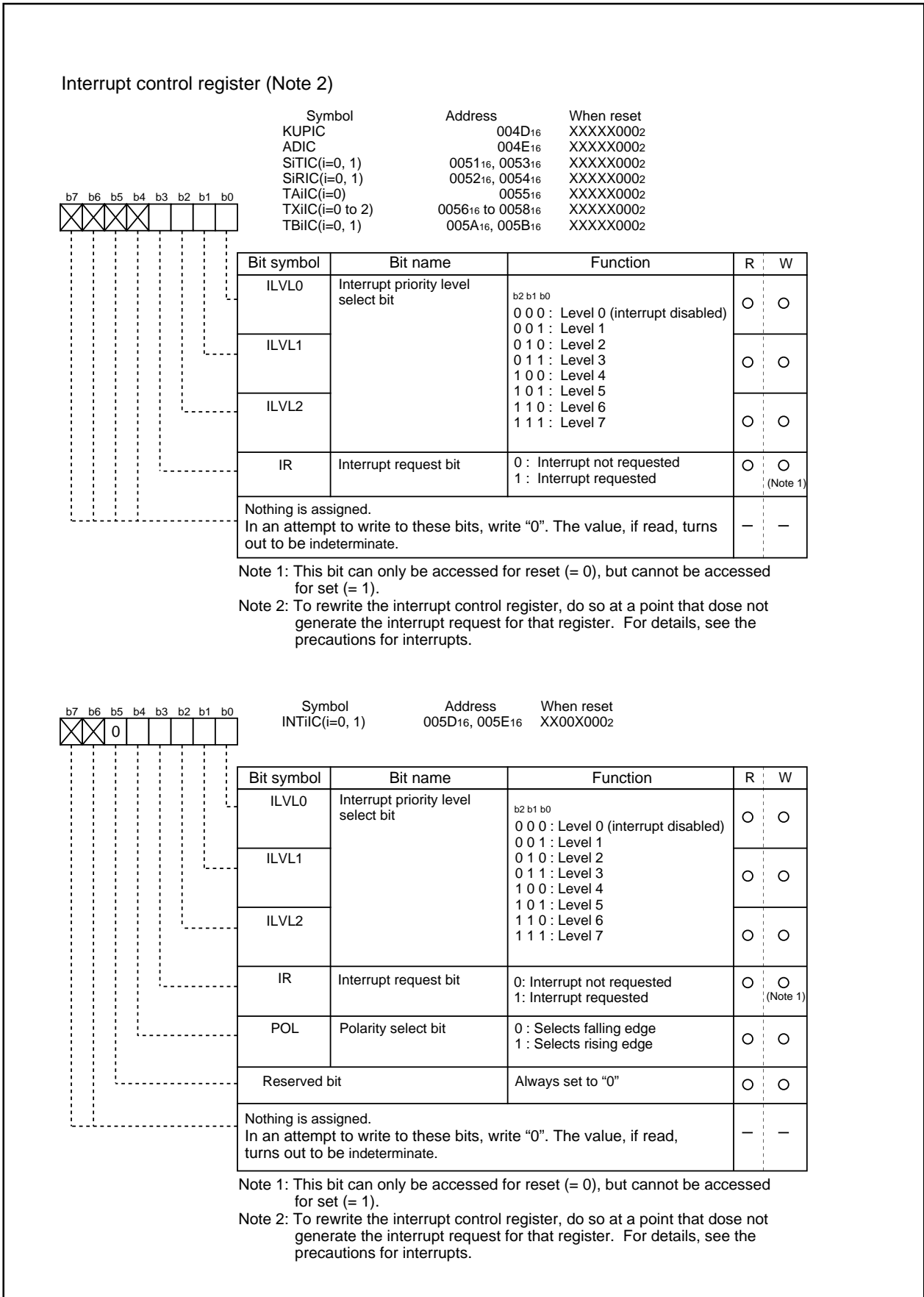


Figure 4.2.2. Interrupt control registers

Interrupt

4.2.1 Interrupt Enable Flag

The interrupt enable flag (I flag) controls the enabling and disabling of maskable interrupts. Setting this flag to "1" enables all maskable interrupts; setting it to "0" disables all maskable interrupts. This flag is set to "0" after reset.

The content is changed when the I flag is changed causes the acceptance of the interrupt request in the following timing:

- When changing the I flag using the REIT instruction, the acceptance of the interrupt takes effect as the REIT instruction is executed.
- When changing the I flag using one of the FCLR, FSET, POPC, and LDC instructions, the acceptance of the interrupt is effective as the next instruction is executed.

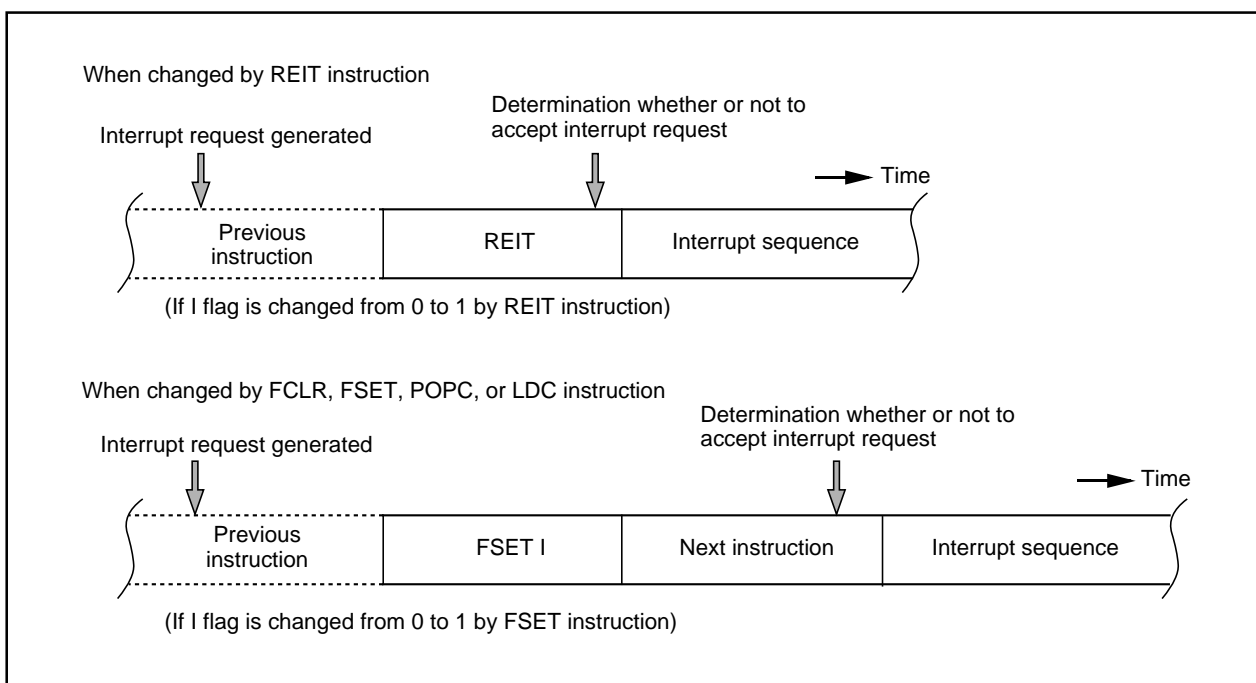


Figure 4.2.3. The timing of reflecting the change in the I flag to the interrupt

4.2.2 Interrupt Request Bit

The interrupt request bit is set to "1" by hardware when an interrupt is requested. After the interrupt is accepted and jumps to the corresponding interrupt vector, the request bit is set to "0" by hardware. The interrupt request bit can also be set to "0" by software. (Do not set this bit to "1").

Interrupt

4.2.3 Interrupt Priority Level Select Bit and Processor Interrupt Priority Level (IPL)

Set the interrupt priority level using the interrupt priority level select bit, which is one of the component bits of the interrupt control register. When an interrupt request occurs, the interrupt priority level is compared with the IPL. The interrupt is enabled only when the priority level of the interrupt is higher than the IPL. Therefore, setting the interrupt priority level to "0" disables the interrupt.

Table 4.2.1 shows the settings of interrupt priority levels and Table 4.2.2 shows the interrupt levels enabled, according to the consist of the IPL.

The following are conditions under which an interrupt is accepted:

- interrupt enable flag (I flag) = 1
- interrupt request bit = 1
- interrupt priority level > IPL

The interrupt enable flag (I flag), the interrupt request bit, the interrupt priority select bit, and the IPL are independent, and they are not affected by one another.

Table 4.2.1. Settings of interrupt priority levels


Interrupt priority level select bit	Interrupt priority level	Priority order
b2 b1 b0 0 0 0	Level 0 (interrupt disabled)	————
0 0 1	Level 1	Low  High
0 1 0	Level 2	
0 1 1	Level 3	
1 0 0	Level 4	
1 0 1	Level 5	
1 1 0	Level 6	
1 1 1	Level 7	

Table 4.2.2. Interrupt levels enabled according to the contents of the IPL

IPL	Enabled interrupt priority levels
IPL ₂ IPL ₁ IPL ₀ 0 0 0	Interrupt levels 1 and above are enabled
0 0 1	Interrupt levels 2 and above are enabled
0 1 0	Interrupt levels 3 and above are enabled
0 1 1	Interrupt levels 4 and above are enabled
1 0 0	Interrupt levels 5 and above are enabled
1 0 1	Interrupt levels 6 and above are enabled
1 1 0	Interrupt levels 7 and above are enabled
1 1 1	All maskable interrupts are disabled

When either the IPL or the interrupt priority level is changed, the new level is reflected to the interrupt in the following timing:

- When changing the IPL using the REIT instruction, the reflection takes effect as of the instruction that is executed in 2 clock cycles after the last clock cycle involved in the REIT instruction.
- When changing the IPL using either the POPC, LDC or LD IPL instruction, the reflection takes effect as of the instruction that is executed in 3 cycles after the last clock cycle involved in the instruction used.
- When changing the interrupt priority level using the MOV or similar instruction, the reflection takes effect as of the instruction that is executed in 2 clock cycles after the last clock cycle involved in the instruction used.

4.2.4 Rewrite the interrupt control register

To rewrite the interrupt control register, do so at a point that does not generate the interrupt request for that register. If there is possibility of the interrupt request occur, rewrite the interrupt control register after the interrupt is disabled. The program examples are described as follow:

Example 1:

```
INT_SWITCH1:
  FCLR  I           ; Disable interrupts.
  AND.B #00h, 0055h ; Clear TA0IC int. priority level and int. request bit.
  NOP                    ; Four NOP instructions are required when using HOLD function.
  NOP
  FSET  I           ; Enable interrupts.
```

Example 2:

```
INT_SWITCH2:
  FCLR  I           ; Disable interrupts.
  AND.B #00h, 0055h ; Clear TA0IC int. priority level and int. request bit.
  MOV.W MEM, R0     ; Dummy read.
  FSET  I           ; Enable interrupts.
```

Example 3:

```
INT_SWITCH3:
  PUSHC FLG         ; Push Flag register onto stack
  FCLR  I           ; Disable interrupts.
  AND.B #00h, 0055h ; Clear TA0IC int. priority level and int. request bit.
  POPC  FLG         ; Enable interrupts.
```

The reason why two NOP instructions (four when using the HOLD function) or dummy read are inserted before FSET I in Examples 1 and 2 is to prevent the interrupt enable flag I from being set before the interrupt control register is rewritten due to effects of the instruction queue.

When a instruction to rewrite the interrupt control register is executed but the interrupt is disabled, the interrupt request bit is not set sometimes even if the interrupt request for that register has been generated. This will depend on the instruction. If this creates problems, use the below instructions to change the register.

Instructions : AND, OR, BCLR, BSET

Interrupt

4.3 Interrupt Sequence

An interrupt sequence — what are performed over a period from the instant an interrupt is accepted to the instant the interrupt routine is executed — is described here.

If an interrupt occurs during execution of an instruction, the processor determines its priority when the execution of the instruction is completed, and transfers control to the interrupt sequence from the next cycle. If an interrupt occurs during execution of either the SMOVB, SMOVF, SSTR or RMPA instruction, the processor temporarily suspends the instruction being executed, and transfers control to the interrupt sequence.

In the interrupt sequence, the processor carries out the following in sequence given:

- (1) CPU gets the interrupt information (the interrupt number and interrupt request level) by reading address 00000_{16} .
- (2) Saves the content of the flag register (FLG) as it was immediately before the start of interrupt sequence in the temporary register (Note) within the CPU.
- (3) Sets the interrupt enable flag (I flag), the debug flag (D flag), and the stack pointer select flag (U flag) to "0" (the U flag, however does not change if the INT instruction, in software interrupt numbers 32 through 63, is executed)
- (4) Saves the content of the temporary register (Note 1) within the CPU in the stack area.
- (5) Saves the content of the program counter (PC) in the stack area.
- (6) Sets the interrupt priority level of the accepted instruction in the IPL.

After the interrupt sequence is completed, the processor resumes executing instructions from the first address of the interrupt routine.

Note: This register cannot be utilized by the user.

4.3.1 Interrupt Response Time

'Interrupt response time' is the period between the instant an interrupt occurs and the instant the first instruction within the interrupt routine has been executed. This time comprises the period from the occurrence of an interrupt to the completion of the instruction under execution at that moment (a) and the time required for executing the interrupt sequence (b). Figure 4.3.1 shows the interrupt response time.

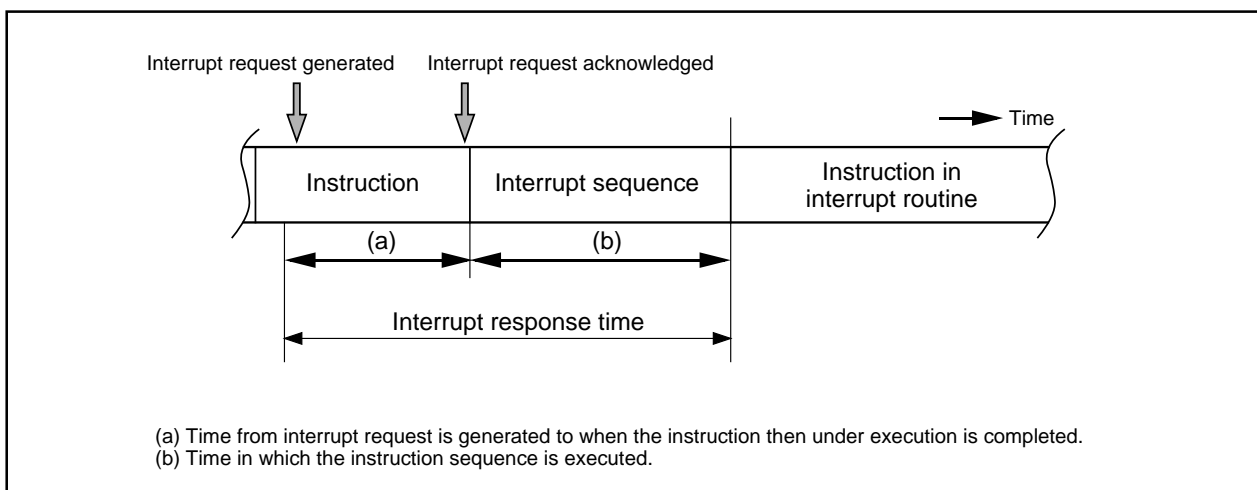


Figure 4.3.1. Interrupt response time

Interrupt

Time (a) is dependent on the instruction under execution. Thirty cycles is the maximum required for the DIVX instruction (without wait).

Time (b) is as shown in Table 4.3.1.

Table 4.3.1. Time required for executing the interrupt sequence

Interrupt vector address	Stack pointer (SP) value	16-Bit bus, without wait	8-Bit bus, without wait
Even	Even	18 cycles (Note 1)	20 cycles (Note 1)
Even	Odd	19 cycles (Note 1)	20 cycles (Note 1)
Odd (Note 2)	Even	19 cycles (Note 1)	20 cycles (Note 1)
Odd (Note 2)	Odd	20 cycles (Note 1)	20 cycles (Note 1)

Note 1: Add 2 cycles in the case of a $\overline{\text{DBC}}$ interrupt; add 1 cycle in the case either of an address coincidence interrupt or of a single-step interrupt.

Note 2: Locate an interrupt vector address in an even address, if possible.

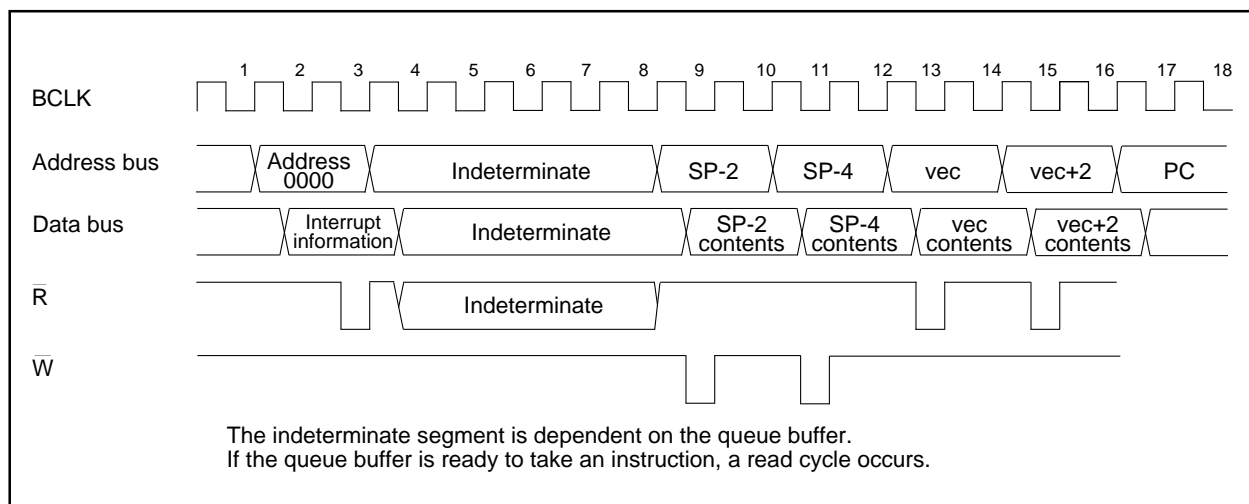


Figure 4.3.2. Time required for executing the interrupt sequence

4.3.2 Variation of IPL when Interrupt Request is Accepted

If an interrupt request is accepted, the interrupt priority level of the accepted interrupt is set in the IPL.

If an interrupt request, that does not have an interrupt priority level, is accepted, one of the values shown in Table 4.3.2 is set in the IPL.

Table 4.3.2. Relationship between interrupts without interrupt priority levels and IPL

Interrupt sources without priority levels	Value set in the IPL
Watchdog timer	7
Reset	0
Other	Not changed

Interrupt

4.3.3 Saving Registers

In the interrupt sequence, only the contents of the flag register (FLG) and that of the program counter (PC) are saved in the stack area.

First, the processor saves the four higher-order bits of the program counter, and 4 upper-order bits and 8 lower-order bits of the FLG register, 16 bits in total, in the stack area, then saves 16 lower-order bits of the program counter. Figure 4.3.3 shows the state of the stack as it was before the acceptance of the interrupt request, and the state the stack after the acceptance of the interrupt request.

Save other necessary registers at the beginning of the interrupt routine using software. Using the PUSHM instruction alone can save all the registers except the stack pointer (SP).

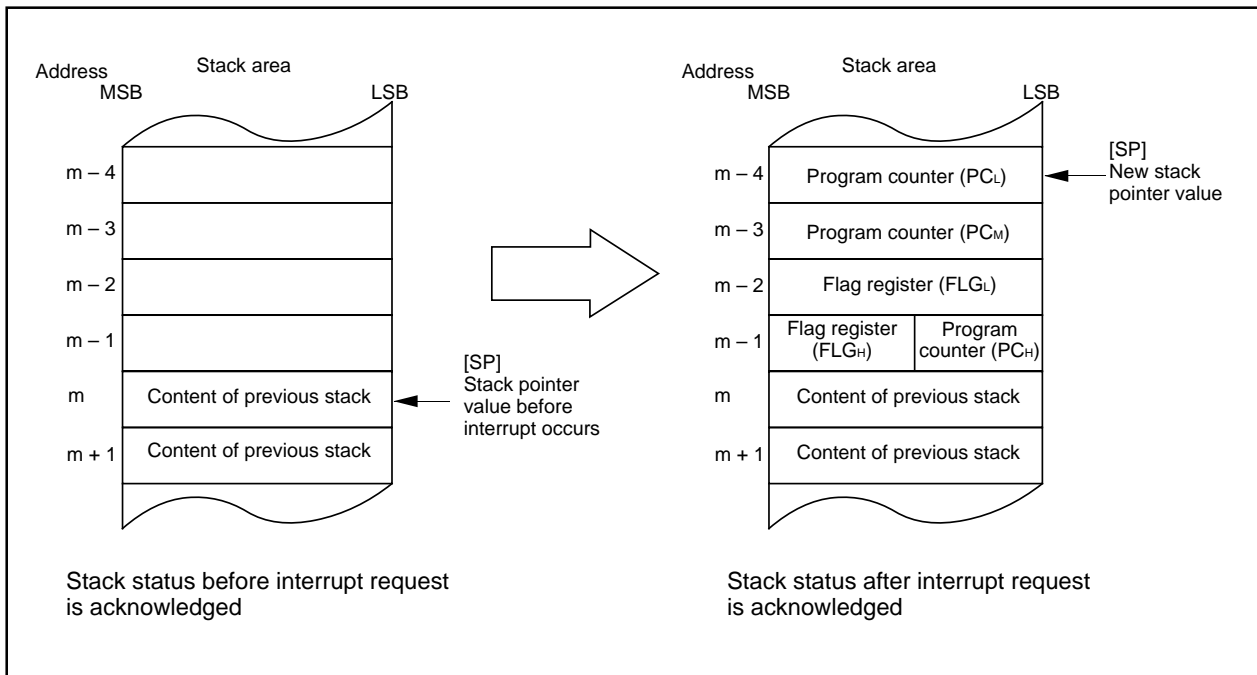


Figure 4.3.3. State of stack before and after acceptance of interrupt request

Interrupt

The operation of saving registers carried out in the interrupt sequence is dependent on whether the content of the stack pointer, at the time of acceptance of an interrupt request, is even or odd. If the content of the stack pointer (Note) is even, the content of the flag register (FLG) and the content of the program counter (PC) are saved, 16 bits at a time. If odd, their contents are saved in two steps, 8 bits at a time. Figure 4.3.4 shows the operation of the saving registers.

Note: Stack pointer indicated by U flag.

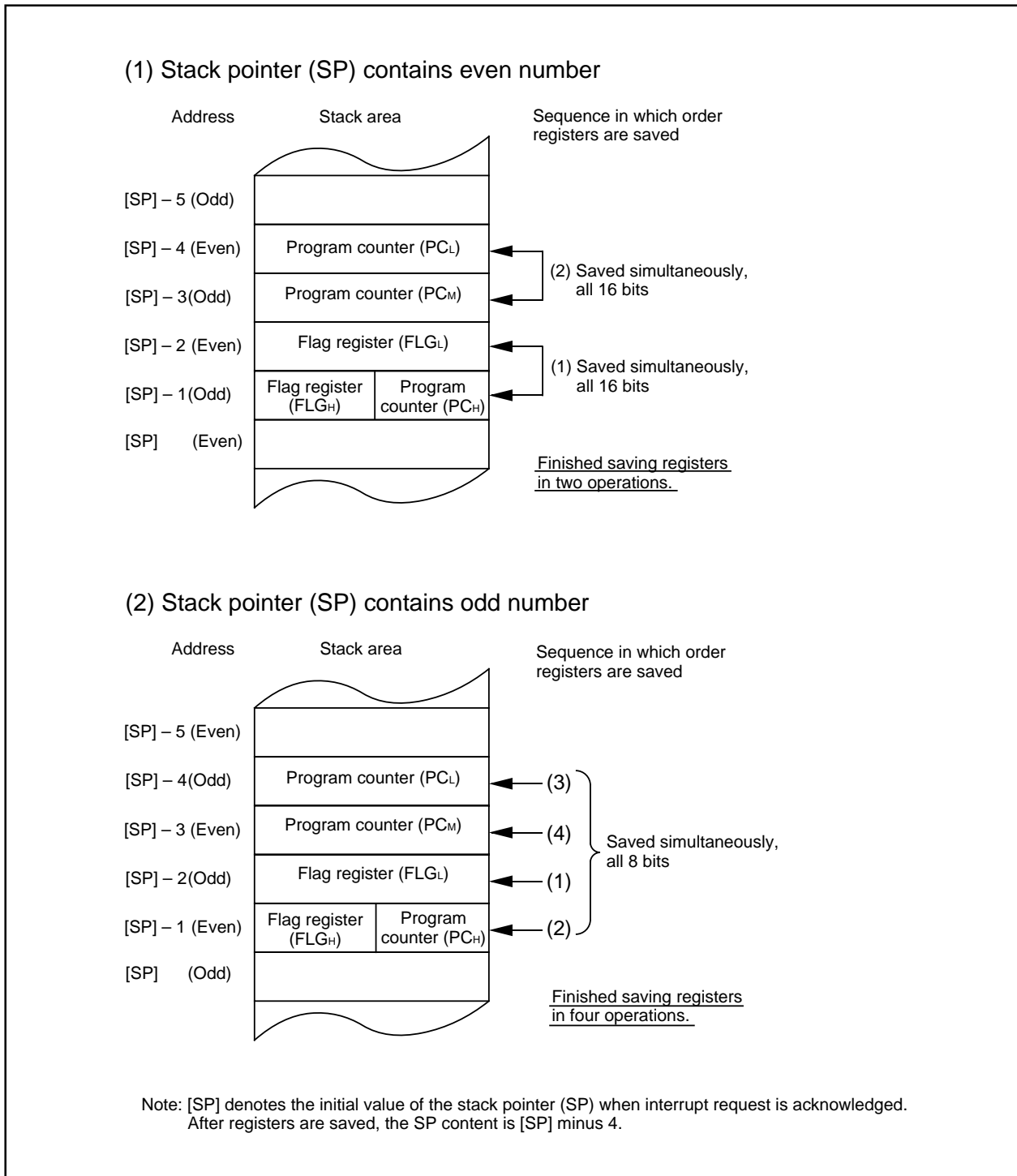


Figure 4.3.4. Operation of saving registers

4.4 Returning from an Interrupt Routine

Executing the REIT instruction at the end of an interrupt routine returns the contents of the flag register (FLG) as it was immediately before the start of interrupt sequence and the contents of the program counter (PC), both of which have been saved in the stack area. Then control returns to the program that was being executed before the acceptance of the interrupt request, so that the suspended process resumes.

Return the other registers saved by software within the interrupt routine using the POPM or similar instruction before executing the REIT instruction.

4.5 Interrupt Priority

If there are two or more interrupt requests occurring at a point in time within a single sampling (checking whether interrupt requests are made), the interrupt assigned a higher priority is accepted.

Assign an arbitrary priority to maskable interrupts (peripheral I/O interrupts) using the interrupt priority level select bit. If the same interrupt priority level is assigned, however, the interrupt assigned a higher hardware priority is accepted (see Figure 4.5.1).

Priorities of the special interrupts, such as Reset (dealt with as an interrupt assigned the highest priority), watchdog timer interrupt, etc. are regulated by hardware.

Figure 4.5.2 shows the priorities of hardware interrupts.

Software interrupts are not affected by the interrupt priority. If an instruction is executed, control branches invariably to the interrupt routine.

Interrupt

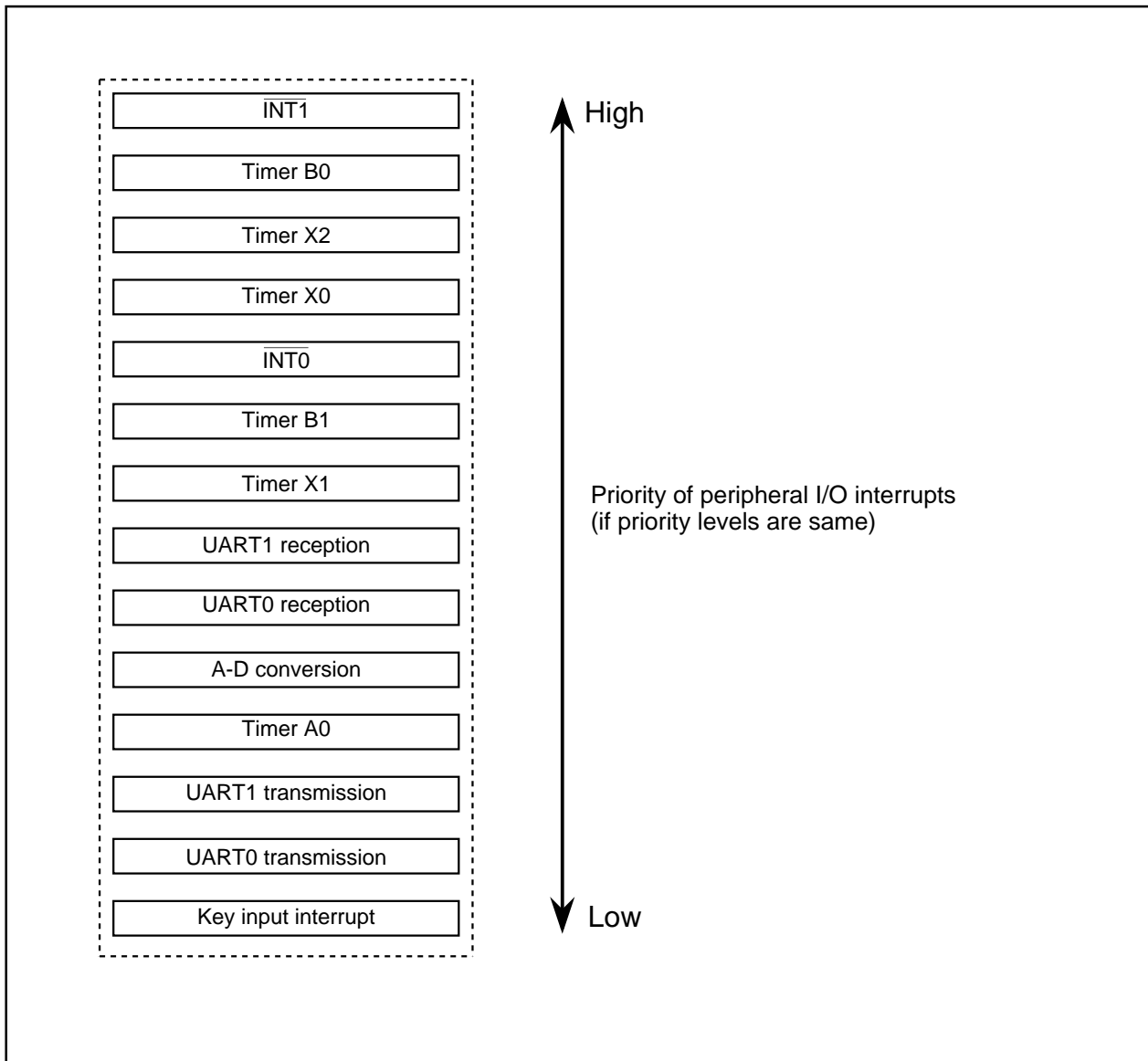


Figure 4.5.1. Maskable interrupts priorities (peripheral I/O interrupts)

Reset > \overline{DBC} > Watchdog timer > Peripheral I/O > Single step > Address match

Figure 4.5.2. Hardware interrupts priorities

Interrupt

4.6 Multiple Interrupts

The state when control branched to an interrupt routine is described below:

- The interrupt enable flag (I flag) is set to "0" (the interrupt is disabled).
- The interrupt request bit of the accepted interrupt is set to "0".
- The processor interrupt priority level (IPL) is assigned to the same interrupt priority level as assigned to the accepted interrupt.

Setting the interrupt enable flag (I flag) to "1" within an interrupt routine allows an interrupt request assigned a priority higher than the IPL to be accepted. Figure 4.6.1 shows the scheme of multiple interrupts.

An interrupt request that is not accepted because of low priority will be held. If the condition following is met when the REIT instruction returns the IPL and the interrupt priority is determined, then the interrupt request being held is accepted.

Interrupt priority level of the interrupt request being held > Returned the IPL

Interrupt

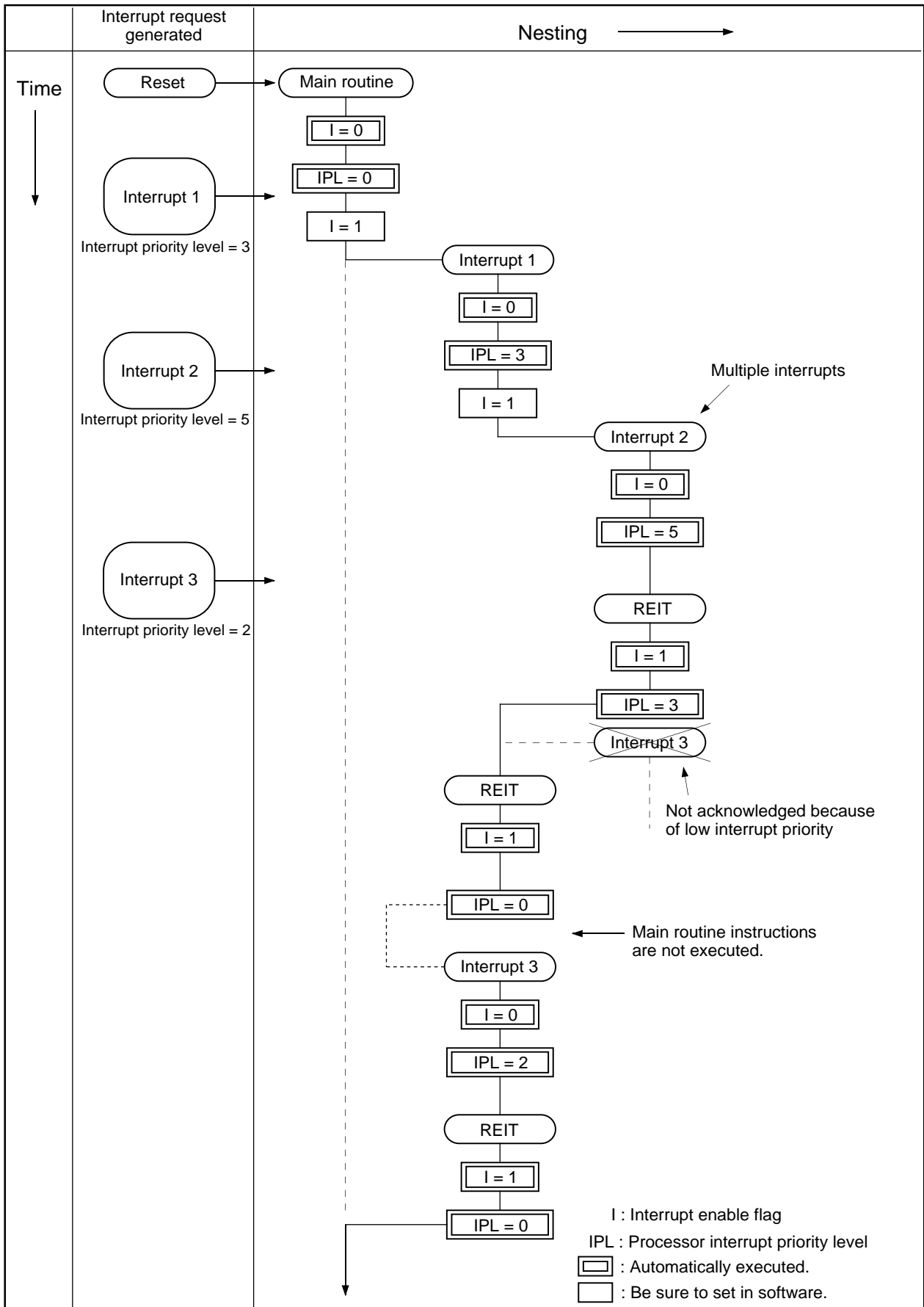


Figure 4.6.1. Multiple interrupts

Interrupt

4.7 Precautions for Interrupts

(1) Reading address 00000₁₆

- When maskable interrupt is occurred, CPU read the interrupt information (the interrupt number and interrupt request level) in the interrupt sequence.

The interrupt request bit of the certain interrupt written in address 00000₁₆ will then be set to "0".

Reading address 00000₁₆ by software sets enabled highest priority interrupt source request bit to "0".

Though the interrupt is generated, the interrupt routine may not be executed.

Do not read address 00000₁₆ by software.

(2) Setting the stack pointer

- The value of the stack pointer immediately after reset is initialized to 0000₁₆. Accepting an interrupt before setting a value in the stack pointer may become a factor of runaway. Be sure to set a value in the stack pointer before accepting an interrupt. Concerning the first instruction immediately after reset, generating any interrupts is prohibited.

(3) External interrupt

- Either an "L" level or an "H" level of at least 250 ns width is necessary for the signal input to pins $\overline{INT_0}$ and $\overline{INT_1}$ regardless of the CPU operation clock.
- When the polarity of the $\overline{INT_0}$ and $\overline{INT_1}$ pins is changed, the interrupt request bit is sometimes set to "1". After changing the polarity, set the interrupt request bit to "0". Figure 4.7.1 shows the procedure for changing the \overline{INT} interrupt generate factor.

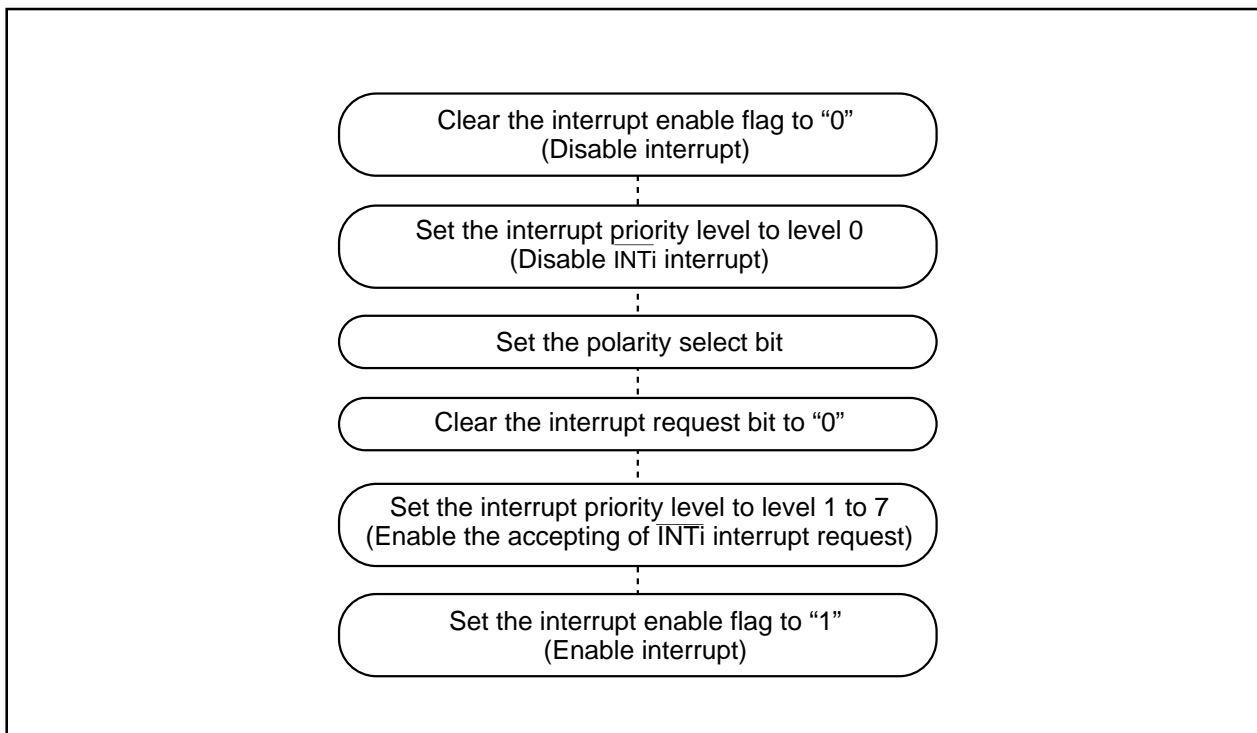


Figure 4.7.1. Switching condition of \overline{INT} interrupt request

Interrupt

(4) Rewrite the interrupt control register

- To rewrite the interrupt control register, do so at a point that does not generate the interrupt request for that register. If there is possibility of the interrupt request occur, rewrite the interrupt control register after the interrupt is disabled. The program examples are described as follow:

Example 1:

```

INT_SWITCH1:
  FCLR  I           ; Disable interrupts.
  AND.B #00h, 0055h ; Clear TA0IC int. priority level and int. request bit.
  NOP                ; Four NOP instructions are required when using HOLD function.
  NOP
  FSET  I           ; Enable interrupts.

```

Example 2:

```

INT_SWITCH2:
  FCLR  I           ; Disable interrupts.
  AND.B #00h, 0055h ; Clear TA0IC int. priority level and int. request bit.
  MOV.W MEM, R0     ; Dummy read.
  FSET  I           ; Enable interrupts.

```

Example 3:

```

INT_SWITCH3:
  PUSHC FLG        ; Push Flag register onto stack
  FCLR  I           ; Disable interrupts.
  AND.B #00h, 0055h ; Clear TA0IC int. priority level and int. request bit.
  POPC  FLG        ; Enable interrupts.

```

The reason why two NOP instructions (four when using the HOLD function) or dummy read are inserted before FSET I in Examples 1 and 2 is to prevent the interrupt enable flag I from being set before the interrupt control register is rewritten due to effects of the instruction queue.

- When a instruction to rewrite the interrupt control register is executed but the interrupt is disabled, the interrupt request bit is not set sometimes even if the interrupt request for that register has been generated. This will depend on the instruction. If this creates problems, use the below instructions to change the register.

Instructions : AND, OR, BCLR, BSET

Interrupt

[MEMO]

Chapter 5

Standard Characteristics

Standard Characteristics

5.1 Standard DC Characteristics

The standard characteristics given in this section are examples of M30201M4-XXXFP. The contents of these examples cannot be guaranteed. For standardized values, see "Electric characteristics".

5.1.1 Standard Ports Characteristics

Figures 5.1.1 through 5.1.6 show the standard ports characteristics.

Standard Characteristics

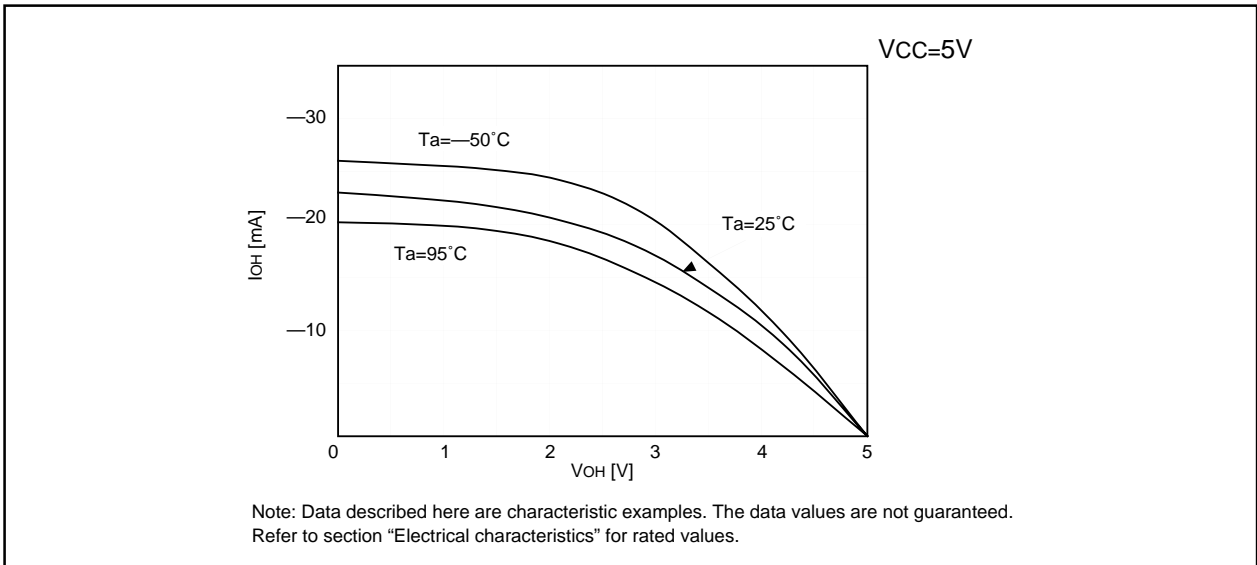


Figure 5.1.1. IOH - VOH standard characteristics of ports P0 to P7 (VCC = 5V)

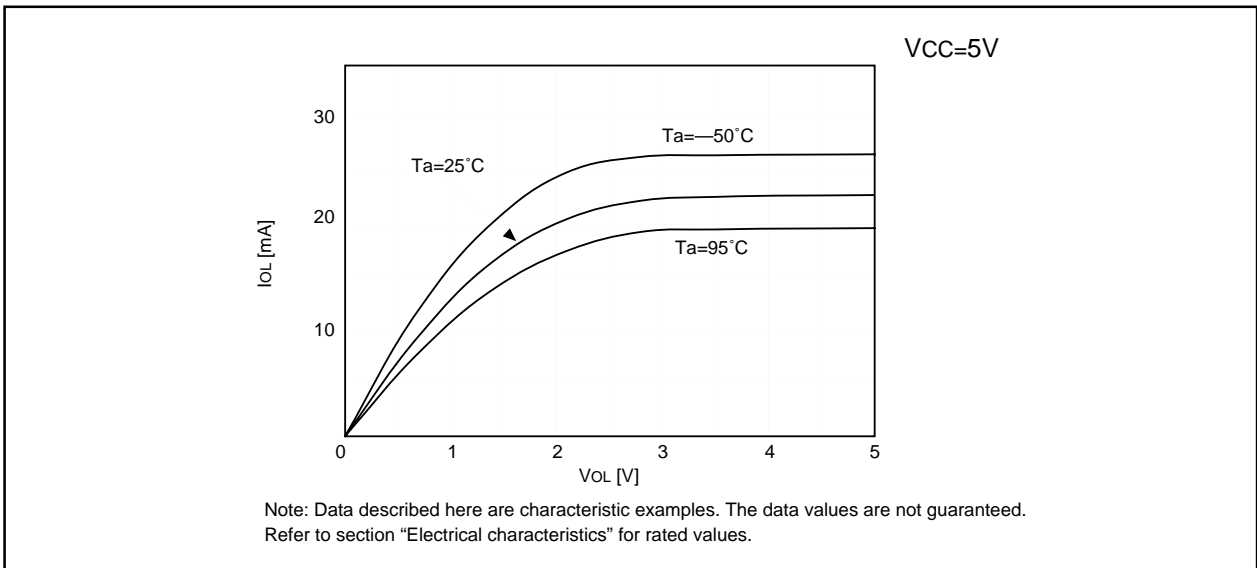


Figure 5.1.2. IOL - VOL standard characteristics of ports P0 to P7 (VCC = 5V)

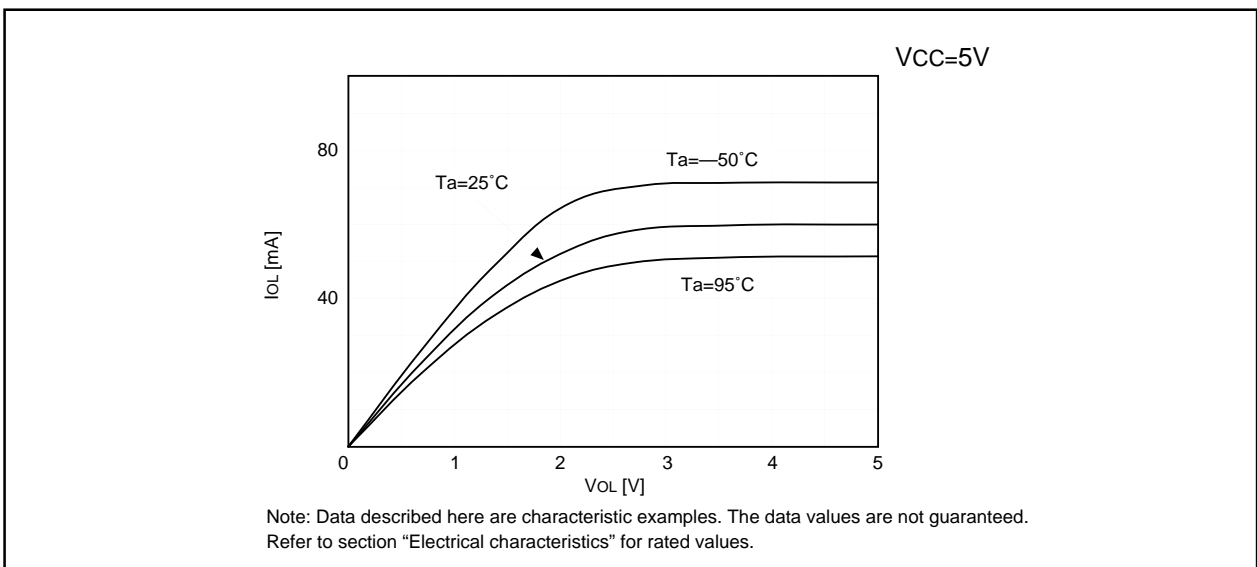


Figure 5.1.3. IOL - VOL standard characteristics of port P1 (VCC = 5V, HIGH POWER)

Standard Characteristics

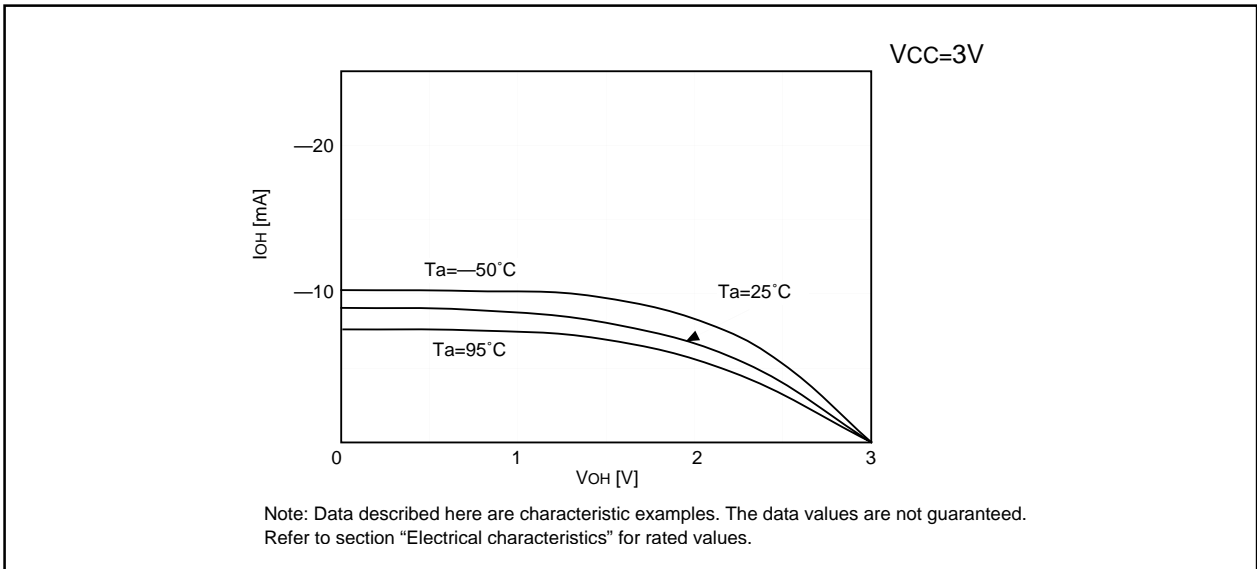


Figure 5.1.4. IOH - VOH standard characteristics of ports P0 to P7 (VCC = 3V)

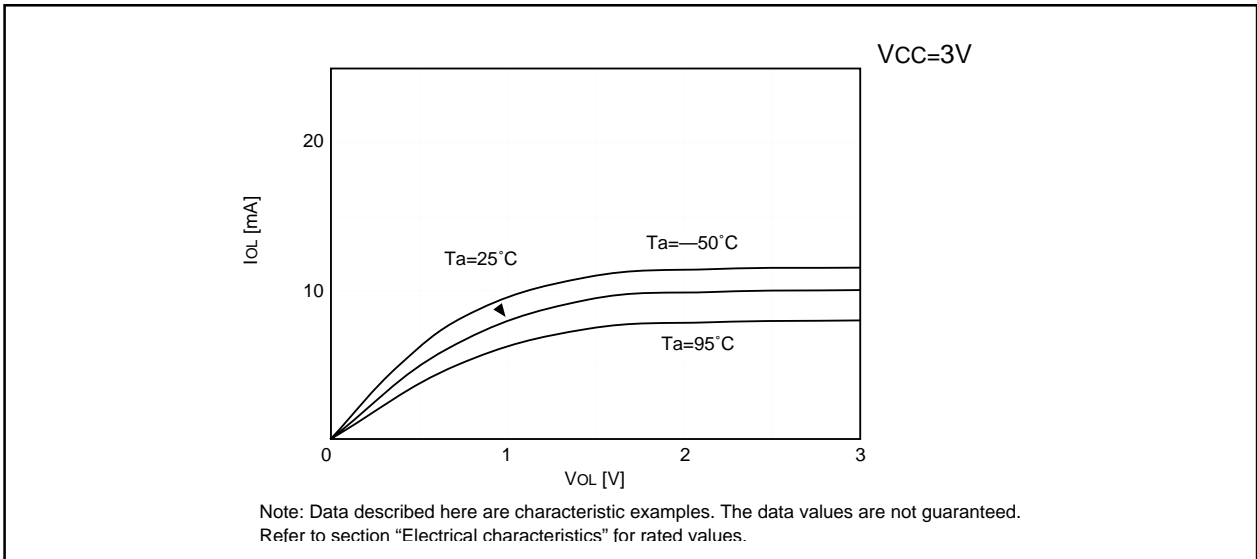


Figure 5.1.5. IOL - VOL standard characteristics of ports P0 to P7 (VCC = 3V)

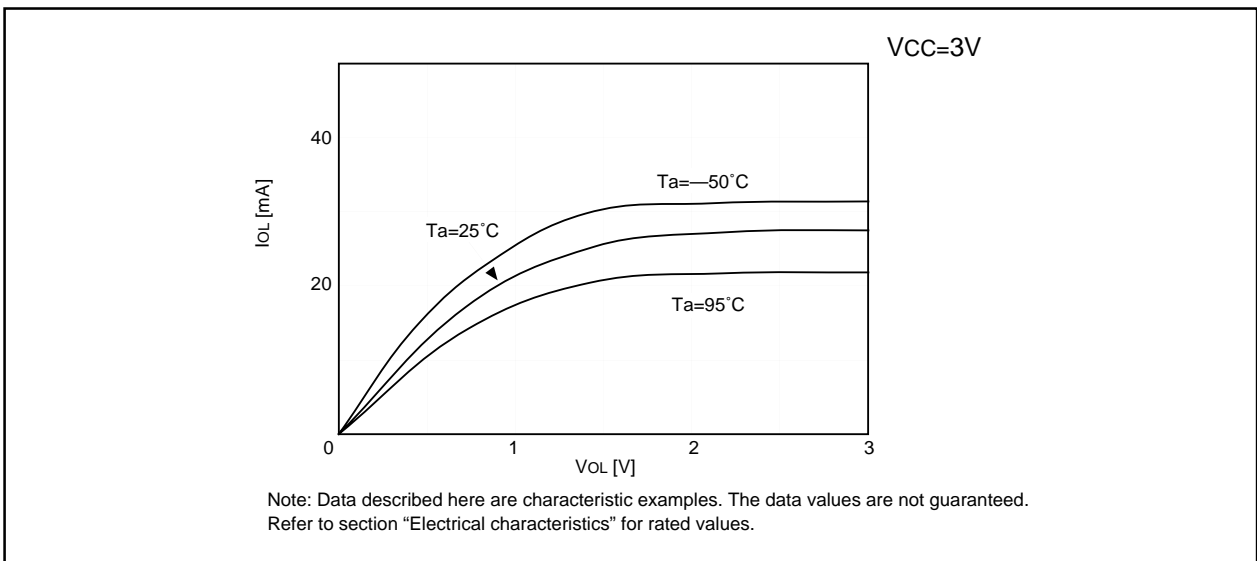
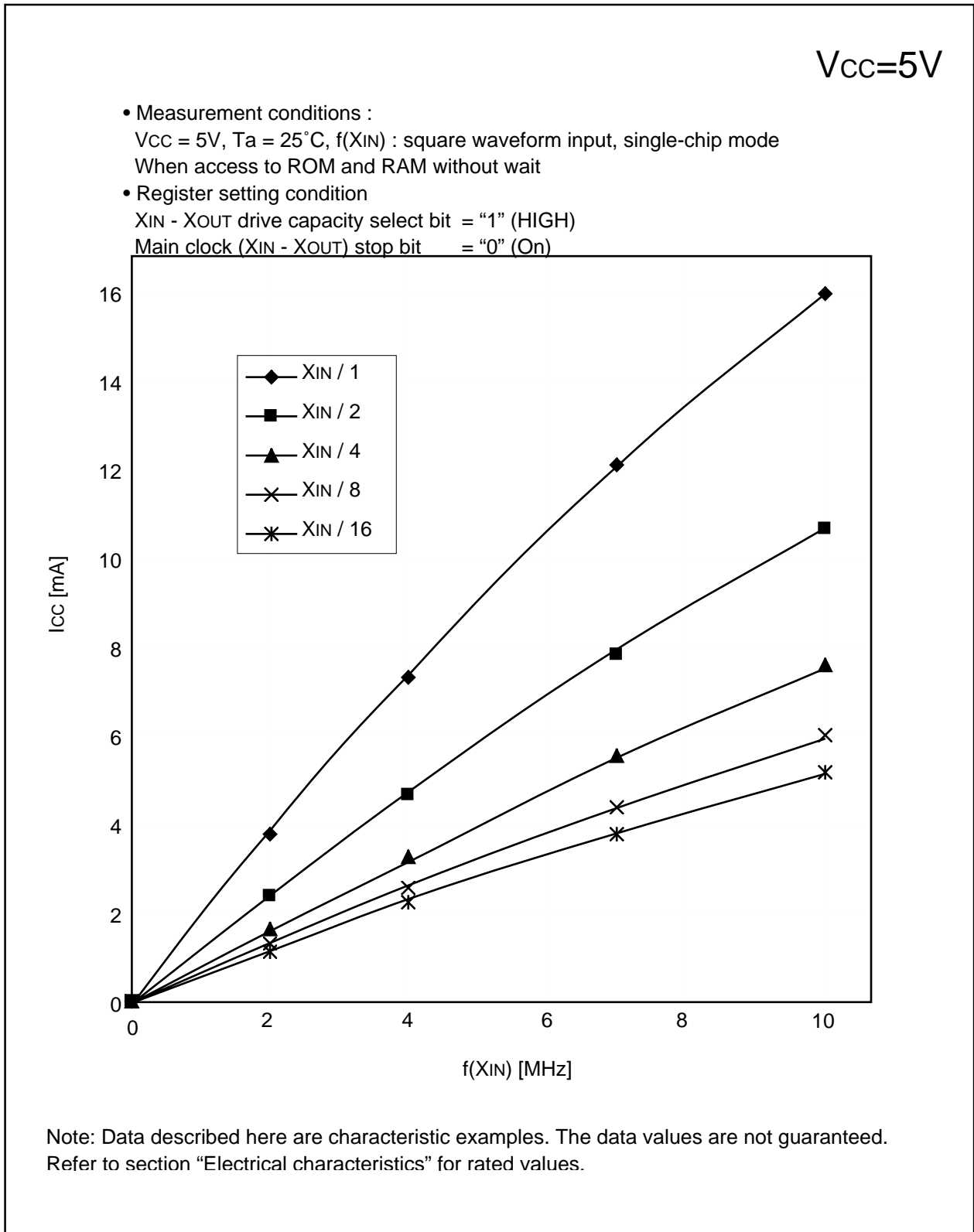


Figure 5.1.6. IOL - VOL standard characteristics of port P1 (VCC = 3V, HIGH POWER)

Standard Characteristics

5.1.2 Standard Characteristics of $I_{CC-f}(X_{IN})$

Figures 5.1.7 and 5.1.8 show the standard characteristics of $I_{CC-f}(X_{IN})$. The standard characteristics given in this section are examples of M30201M4-XXXFP. The contents of these examples cannot be guaranteed. For standardized values, see "Electric characteristics".

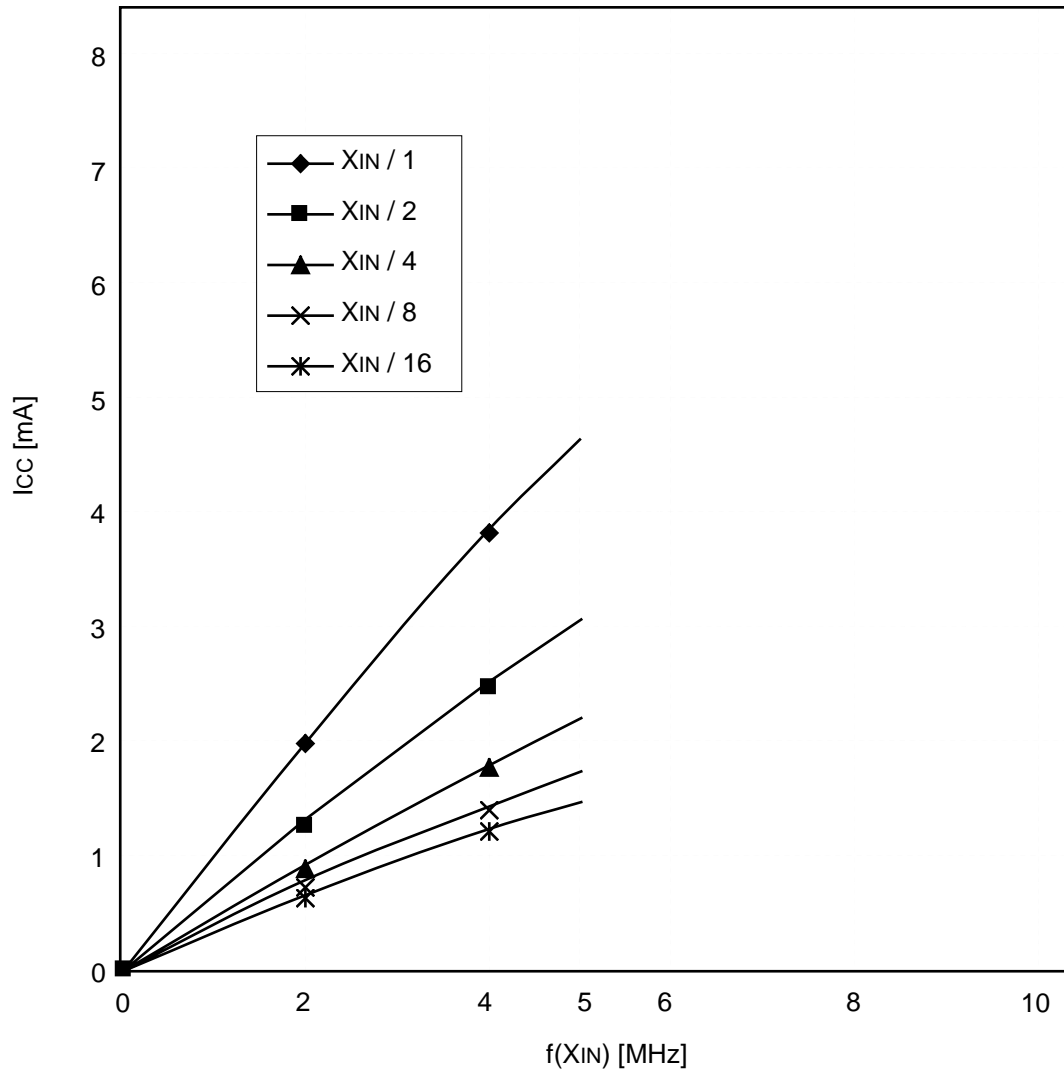


Figures 5.1.7. Standard characteristics of $I_{CC-f}(X_{IN})$ ($V_{CC} = 5V$)

Standard Characteristics

$V_{CC}=3V$

- Measurement conditions :
 $V_{CC} = 3V$, $T_a = 25^{\circ}C$, $f(X_{IN})$: square waveform input, single-chip mode
 When access to ROM and RAM without wait
- Register setting condition
 $X_{IN} - X_{OUT}$ drive capacity select bit = "1" (HIGH)
 Main clock ($X_{IN} - X_{OUT}$) stop bit = "0" (On)



Note: Data described here are characteristic examples. The data values are not guaranteed. Refer to section "Electrical characteristics" for rated values.

Figures 5.1.8. Standard characteristics of I_{CC} - $f(X_{IN})$ ($V_{CC} = 3V$)

Standard Characteristics

5.2 Standard Characteristics of Pull-Up Resistor

Figure 5.2.1 shows an example of the standard characteristics of the pull-up resistor. The standard characteristics given in this section are examples of M30201M4-XXXFP. The contents of these examples cannot be guaranteed. For standardized values, see "Electric characteristics".

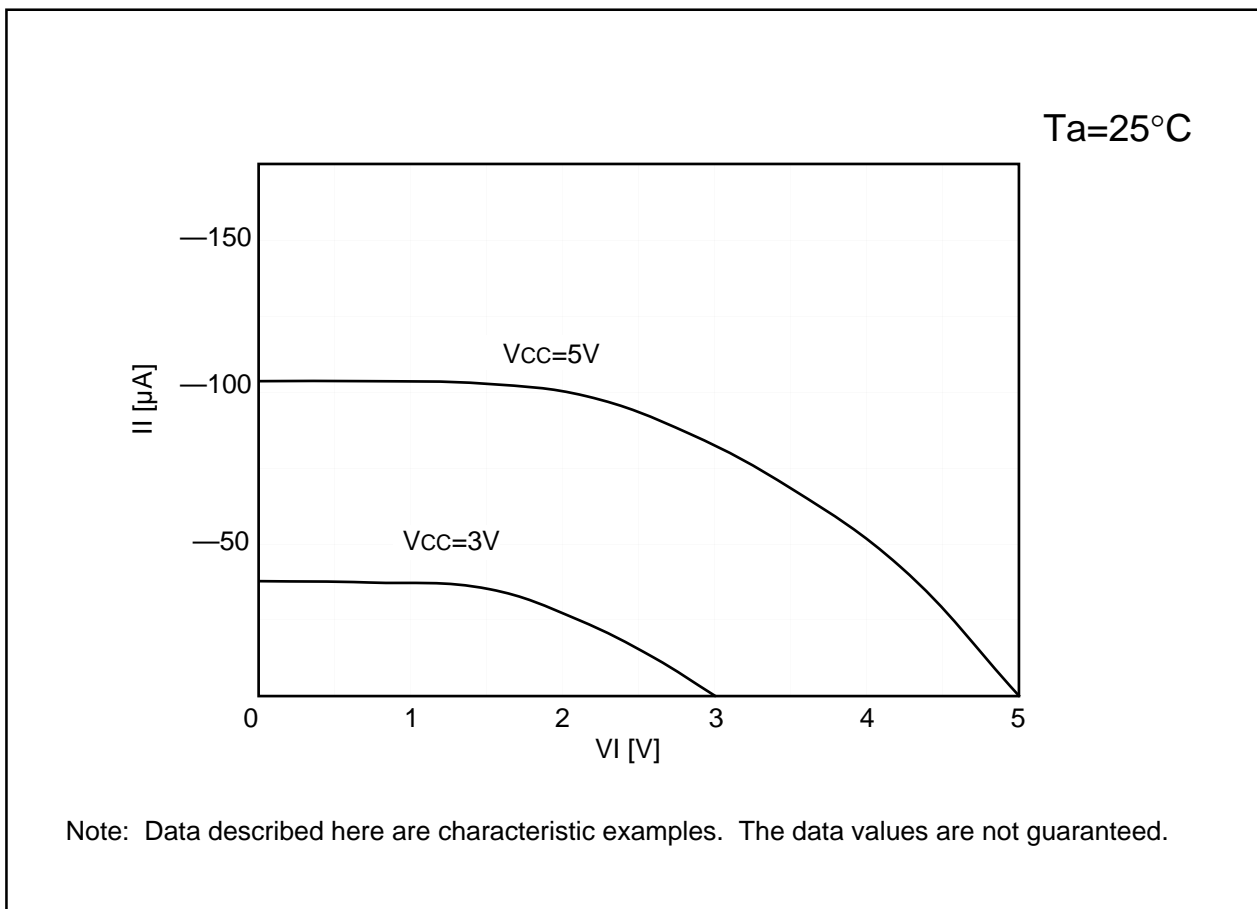


Figure 5.2.1. Example of the standard characteristics of the pull-up resistor

Standard Characteristics (Flash memory version)

5.3 Standard DC Characteristics (Flash memory version)

The standard characteristics given in this section are examples of M30201F6FP. The contents of these examples cannot be guaranteed. For standardized values, see "Electric characteristics".

5.3.1 Standard Ports Characteristics

Figures 5.3.1 through 5.3.3 show the standard ports characteristics.

Standard Characteristics (Flash memory version)

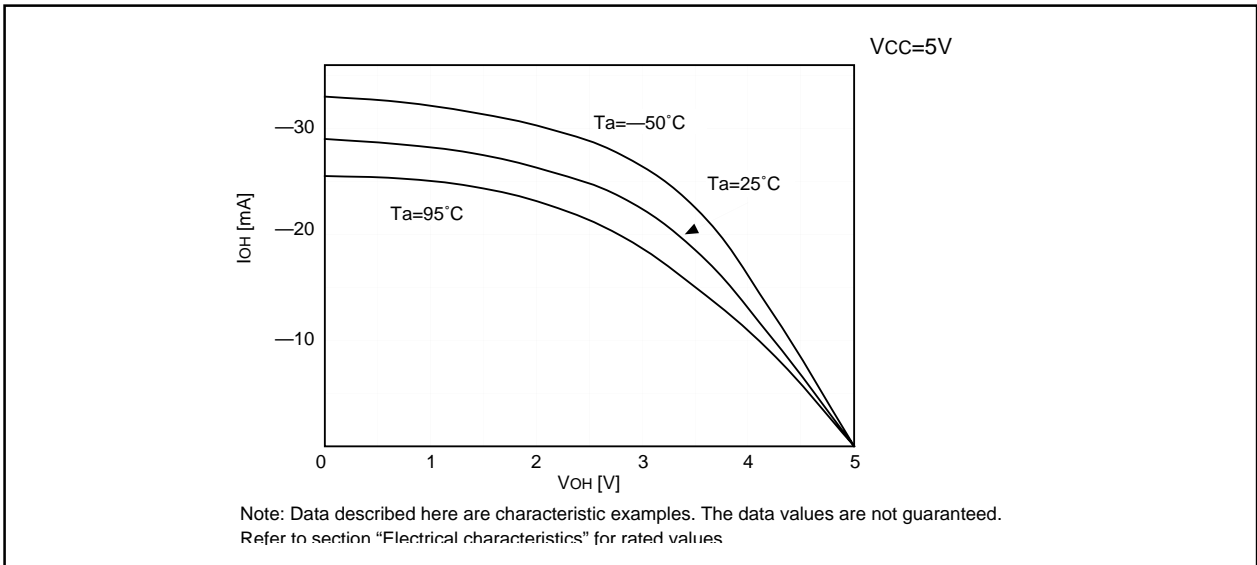


Figure 5.3.1. IOH - VOH standard characteristics of ports P0 to P7 (VCC = 5V)

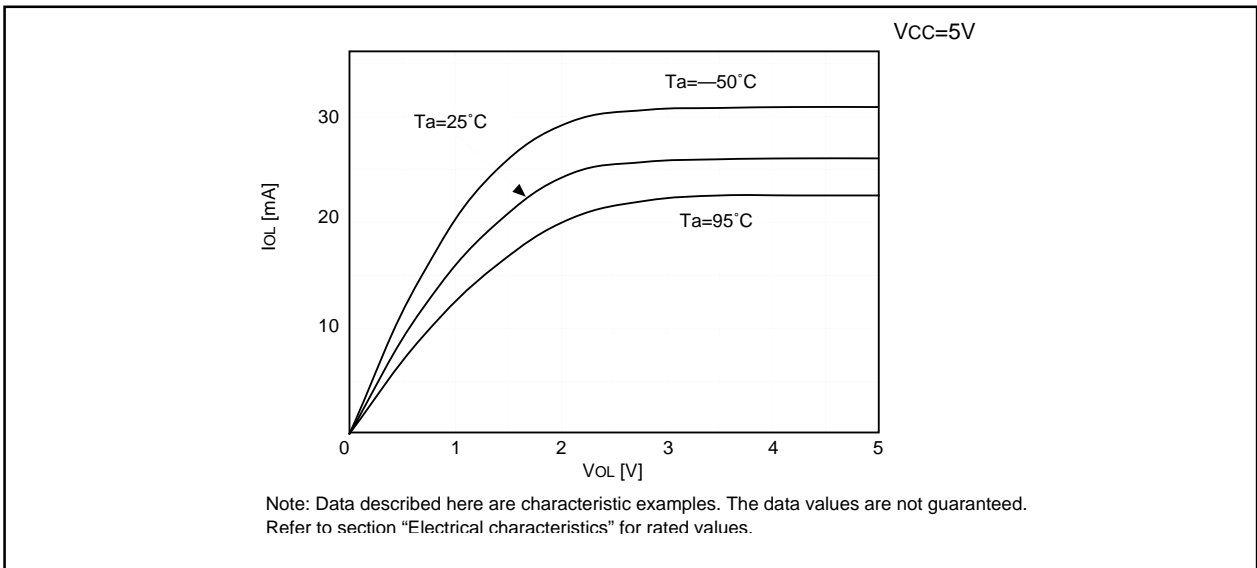


Figure 5.3.2. IOL - VOL standard characteristics of ports P0 to P7 (VCC = 5V)

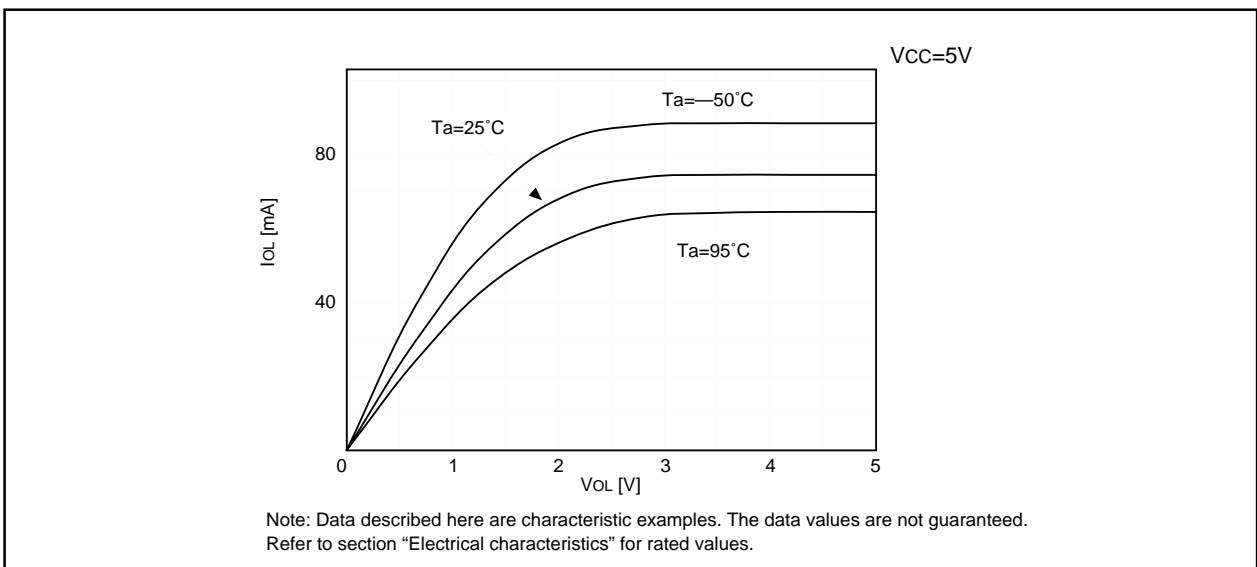
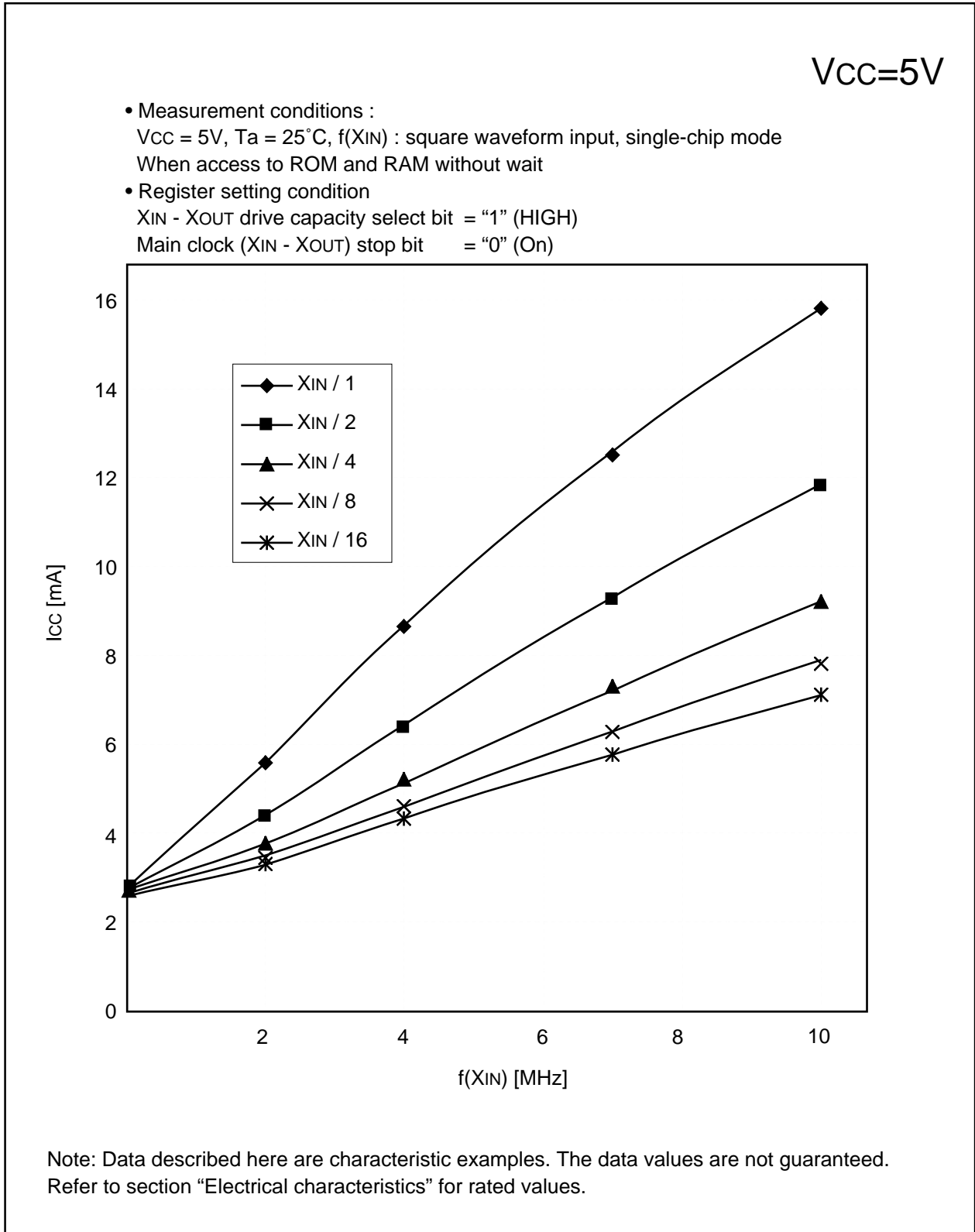


Figure 5.3.3. IOL - VOL standard characteristics of port P1 (VCC = 5V, HIGH POWER)

Standard Characteristics (Flash memory version)

5.3.2 Standard Characteristics of $I_{CC-f}(X_{IN})$

Figure 5.3.4 shows the Characteristics of $I_{CC-f}(X_{IN})$. The standard characteristics given in this section are examples of M30201F6FP. The contents of these examples cannot be guaranteed. For standardized values, see "Electric characteristics".



Figures 5.3.4. Standard characteristics of $I_{CC-f}(X_{IN})$ ($V_{CC} = 5V$)

Standard Characteristics (Flash memory version)

5.4 Standard Characteristics of Pull-Up Resistor

Figure 5.4.1 shows an example of the standard characteristics of the pull-up resistor. The standard characteristics given in this section are examples of M30201F6FP. The contents of these examples cannot be guaranteed. For standardized values, see "Electric characteristics".

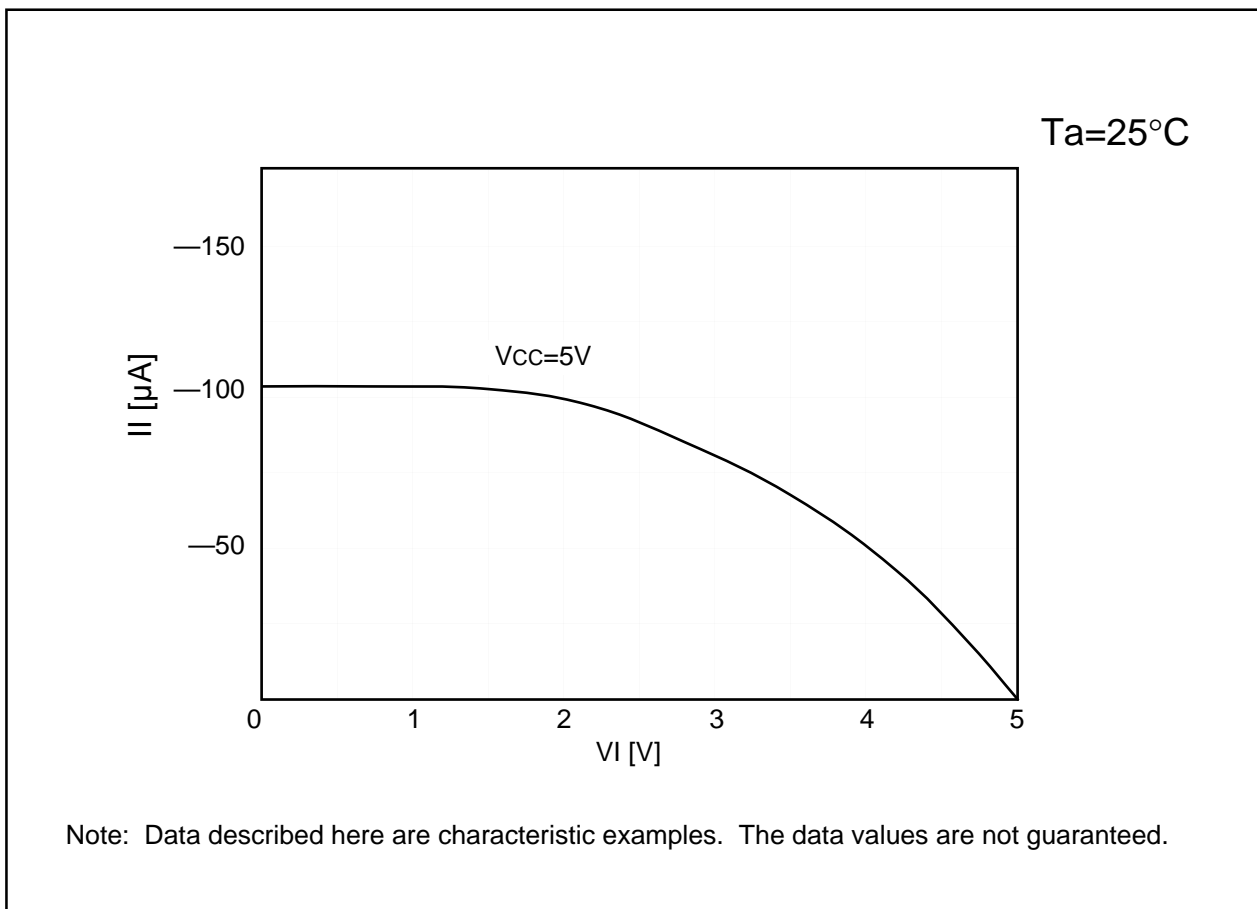


Figure 5.4.1. Example of the standard characteristics of the pull-up resistor

Appendix 1 Check Sheet

Appendix 1 Check Sheet

The following check sheet was created based on items which had been the source of problems in the past. We recommend you refer to the check sheet when troubleshooting.

Checks regarding register initial settings

- Has the initial setting been made in the interrupt stack pointer (ISP) at the top of the program?
- Has the initial setting been made in the user stack pointer (USP)? (Only if using the USP)
- Does the USP overlap the ISP area? (Only if using the USP)
- Is interrupt enabled after setting the ISP and USP?
- Is the top address of the variable interrupt vector table set in the interrupt table register (INTB)?
- Is interrupt enabled after setting the INTB?
- Has the initial setting been made in the frame base register (FB)? (Only if using the FB)
- Has the initial setting been made in the stack base register (SB)? (Only if using the SB)

Checks regarding the internal memory

- Does the RAM capacity used in the program exceed the RAM capacity of the microcomputer?
- Does the ROM capacity used in the program exceed the ROM capacity of the microcomputer?

Checks regarding the protect register

- Is writing enabled in the protect register (address 000A₁₆) before writing in the system clock control register (addresses 0006₁₆ and 0007₁₆)?
- Is writing enabled in the protect register before writing in the processor mode register (addresses 0004₁₆ and 0005₁₆)?
- Is writing enabled in the protect register before writing in the port P4 direction register (address 03EA₁₆)?
- Is writing effectuated in the port P4 direction register by the next instruction after writing is enabled in the protect register?
- Does not an interrupt generate between the instruction writing is enabled in the protect register and the instruction writing in the port P4 direction register?

Appendix 1 Check Sheet

Checks regarding the timer

- Is the timer started after a value is set in the timer register?

Checks regarding low power consumption

- In the low power consumption mode, does not current flow from Vref when the Vref connection bit (bit 5 in address 03D716) is set?
- Is not voltage level of port floating in the low power consumption mode?

Checks regarding Interrupt

- When rewrite the interrupt register, do so at a point that does not generate the interrupt request?

Checks regarding low voltage

- When using at low voltage, have you checked recommended operating conditions and changed the wait bit (address 000516, bit 7) to "1"?

Checks regarding A-D converter

- Have you selected other than fAD (no dividing) for ϕ_{AD} when using the A-D converter at $V_{CC} = 2.7 - 4.0V$?
- Have you selected no sample & hold function when using the A-D converter at $V_{CC} = 2.7 - 4.0V$?
- Have you selected 8-bit mode when using the A-D converter at $V_{CC} = 2.7 - 4.0V$?

Appendix 2 Hexadecimal instruction CODE table

	D7 to D4	0000	0001	0010	0011	0100	0101	0110	0111
D3 to D0		0	1	2	3	4	5	6	7
0000	0	BRK	AND.B:S R0H,R0L	ADD.B:S R0H,R0L	MOV.B:S R0H,A0	BCLR:S 0,11[SB]	BNOT:S 0,11[SB]	JMP.S label	MULU.B src,dest
0001	1	MOV.B:S R0L,dsp:8[SB]	AND.B:S dsp:8[SB],R0L	ADD.B:S dsp:8[SB],R0L	MOV.B:S dsp:8[SB],A0	BCLR:S 1,11[SB]	BNOT:S 1,11[SB]	JMP.S label	MULU.W src,dest
0010	2	MOV.B:S R0L,dsp:8[FB]	AND.B:S dsp:8[FB],R0L	ADD.B:S dsp:8[FB],R0L	MOV.B:S dsp:8[FB],A0	BCLR:S 2,11[SB]	BNOT:S 2,11[SB]	JMP.S label	MOV.B:G src,dest
0011	3	MOV.B:S R0L,abs16	AND.B:S abs16,R0L	ADD.B:S abs16,R0L	MOV.B:S abs16,A0	BCLR:S 3,11[SB]	BNOT:S 3,11[SB]	JMP.S label	MOV.W:G src,dest
0100	4	NOP	AND.B:S R0L,R0H	ADD.B:S R0L,R0H	MOV.B:S R0Çk,A1	BCLR:S 4,11[SB]	BNOT:S 4,11[SB]	JMP.S label	CODE_74
0101	5	MOV.B:S R0H,dsp:8[SB]	AND.B:S dsp:8[SB],R0H	ADD.B:S dsp:8[SB],R0H	MOV.B:S dsp:8[SB],A1	BCLR:S 5,11[SB]	BNOT:S 5,11[SB]	JMP.S label	CODE_75
0110	6	MOV.B:S R0H,dsp:8[FB]	AND.B:S dsp:8[FB],R0H	ADD.B:S dsp:8[FB],R0H	MOV.B:S dsp:8[FB],A1	BCLR:S 6,11[SB]	BNOT:S 6,11[SB]	JMP.S label	CODE_76
0111	7	MOV.B:S R0H,abs16	AND.B:S abs16,R0H	ADD.B:S abs16,R0H	MOV.B:S abs16,A1	BCLR:S 7,11[SB]	BNOT:S 7,11[SB]	JMP.S label	CODE_77
1000	8	MOV.B:S R0H,R0L	OR.B:S R0H,R0L	SUB.B:S R0H,R0L	CMP.B:S R0H,R0L	BSET:S 0,11[SB]	BTST:S 0,11[SB]	JGEU/C label	MUL.B src,dest
1001	9	MOV.B:S dsp:8[SB],R0L	OR.B:S dsp:8[SB],R0L	SUB.B:S dsp:8[SB],R0L	CMP.B:S dsp:8[SB],R0L	BSET:S 1,11[SB]	BTST:S 1,11[SB]	JGTU label	MUL.W src,dest
1010	A	MOV.B:S dsp:8[FB],R0L	OR.B:S dsp:8[FB],R0L	SUB.B:S dsp:8[FB],R0L	CMP.B:S dsp:8[FB],R0L	BSET:S 2,11[SB]	BTST:S 2,11[SB]	JEQ/Z label	CODE_7A
1011	B	MOV.B:S abs16,R0L	OR.B:S abs16,R0L	SUB.B:S abs16,R0L	CMP.B:S abs16,R0L	BSET:S 3,11[SB]	BTST:S 3,11[SB]	JN label	CODE_7B
1100	C	MOV.B:S R0L,R0H	OR.B:S R0L,R0H	SUB.B:S R0L,R0H	CMP.B:S R0L,R0H	BSET:S 4,11[SB]	BTST:S 4,11[SB]	JLTU/NC label	CODE_7C
1101	D	MOV.B:S dsp:8[SB],R0H	OR.B:S dsp:8[SB],R0H	SUB.B:S dsp:8[SB],R0H	CMP.B:S dsp:8[SB],R0H	BSET:S 5,11[SB]	BTST:S 5,11[SB]	JLEU label	CODE_7D
1110	E	MOV.B:S dsp:8[FB],R0H	OR.B:S dsp:8[FB],R0H	SUB.B:S dsp:8[FB],R0H	CMP.B:S dsp:8[FB],R0H	BSET:S 6,11[SB]	BTST:S 6,11[SB]	JNE/JNZ label	CODE_7E
1111	F	MOV.B:S abs16,R0H	OR.B:S abs16,R0H	SUB.B:S abs16,R0H	CMP.B:S abs16,R0H	BSET:S 7,11[SB]	BTST:S 7,11[SB]	JPZ label	

The next instruction is arranged in each CODE.

CODE_74:STE,MOV,PUSH,NEG,ROT,NOT,LDE,POP,SHL,SHA

CODE_75:STE,MOV,PUSH,NEG,ROT,NOT,LDE,POP,SHL,SHA

CODE_76:TST,XOR,AND,OR,ADD,SUB,ADC,SBB,CMP,DIVX,ROL,RORC,DIVU,DIV,ADCF,ABS

CODE_77:TST,XOR,AND,OR,ADD,SUB,ADC,SBB,CMP,DIVX,ROL,RORC,DIVU,DIV,ADCF,ABS

CODE_7A:XCHG,LDC

CODE_7B:XCHG,STC

CODE_7C:MOV Dir,MULU,MUL,EXTS,STC,DIVU,DIV,PUSH,DIVX,DADD,DSUB,DADC,DSBB,SMOVF,SMOVV,SSTR,ADD,LDCTX,RMPA,ENTER

CODE_7D:JMPI,JSRI,MULU,MUL,PUSHA,LDIPL,ADD,J Cnd,BMCnd,DIVU,DIV,PUSH,DIVX,DADD,DSUB,DADC,DSBB,SMOVF,SMOVV,SSTR,STCTX,RMPA,EXITD,WAIT

CODE_7E:BTSTC,BM Cnd,BNTST,BAND,BNAND,BOR,BNOR,BCLR,BSET,BNOT,BTST,BXOR,BNXOR

CODE_7F:SHL,FSET,FCLR,MOVA,LDC,SHA,PUSHC,POPC,INT

Appendix 2 Hexadecimal instruction CODE table

	D7 to D4	1000	1001	1010	1011	1100	1101	1110	1111
D3 to D0		8	9	A	B	C	D	E	F
0000	0	TST.B src,dest	AND.B:G src,dest	ADD.B:G src,dest	ADC.B src,dest	CMP.B:G src,dest	CMP.B:Q #IMM,dest	ROT.B #IMM,dest	SHA.B #IMM,dest
0001	1	TST.W src,dest	AND.W:G src,dest	ADD.W:G src,dest	ADC.w src,dest	CMP.W:G src,dest	CMP.W:Q #IMM,dest	ROT.W #IMM,dest	SHA.W #IMM,dest
0010	2	PUSH.B:S R0L	POP.B:S R0L	MOV.W:S #IMM,A0	INC.W A0	PUSH.W:S A0	POP.W:S A0	MOV.B:S #IMM,A0	DEC.W A0
0011	3	ADD.B:S #IMM8,R0H	AND.B:S #IMM8,R0H	INC.B R0H	MOV.B:Z #0,R0H	MOV.B:S #IMM8,R0H	STNZ #IMM8,R0H	CMP.B:S #IMM8,R0H	RTS
0100	4	ADD.B:S #IMM8,R0L	AND.B:S #IMM8,R0L	INC.B R0L	MOV.B:Z #0,R0L	MOV.B:S #IMM8,R0L	STNZ #IMM8,R0L	CMP.B:S #IMM8,R0L	JMP.W label
0101	5	ADD.B:S #IMM8,dsp:8[SB]	AND.B:S #IMM8,dsp:8[SB]	INC.B dsp:8[SB]	MOV.B:Z #0,dsp:8[SB]	MOV.B:S #IMM8,dsp:8[SB]	STNZ #IMM8,dsp:8[SB]	CMP.B:S #IMM8,dsp:8[SB]	JSR.W label
0110	6	ADD.B:S #IMM8,dsp:8[FB]	AND.B:S #IMM8,dsp:8[FB]	INC.B dsp:8[FB]	MOV.B:Z #0,dsp:8[FB]	MOV.B:S #IMM8,dsp:8[FB]	STNZ #IMM8,dsp:8[FB]	CMP.B:S #IMM8,dsp:8[FB]	INTO
0111	7	ADD.B:S #IMM8,abs16	AND.B:S #IMM8,abs16	INC.B abs16	MOV.B:Z #0,abs16	MOV.B:S #IMM8,abs16	STNZ #IMM8,abs16	CMP.B:S #IMM8,abs16	
1000	8	XOR.B src,dest	OR.B:G src,dest	SUB.B:G src,dest	SBB.B src,dest	ADD.B:Q #IMM,dest	MOV.B:Q #IMM,dest	SHL.B #IMM,dest	ADJNZ.B #IMM,dest,label
1001	9	XOR.W src,dest	OR.W:G src,dest	SUB.W:G src,dest	SBB.W src,dest	ADD.W:Q #IMM,dest	MOV.W:Q #IMM,dest	SHL.W #IMM,dest	ADJNZ.W #IMM,dest,label
1010	A	PUSH.B:S R0H	POP.B:S R0H	MOV.W:S #IMM,A1	INC.W A1	PUSH.W:S A1	POP.W:S A1	MOV.B:S #IMM,A1	DEC.W A1
1011	B	SUB.B:S #IMM8,R0H	OR.B:S #IMM8,R0H	DEC.B R0H	NOT.B:S R0H	STZ #IMM8,R0H	STZX #IMM8,#IMM8,R0H	CODE_EB	REIT
1100	C	SUB.B:S #IMM8,R0L	OR.B:S #IMM8,R0L	DEC.B R0L	NOT.B:S R0L	STZ #IMM8,R0L	STZX #IMM8,#IMM8,R0L	PUSHM src	JMP.A label
1101	D	SUB.B:S #IMM8,dsp:8[SB]	OR.B:S #IMM8,dsp:8[SB]	DEC.B dsp:8[SB]	NOT.B:S dsp:8[SB]	STZ #IMM8,dsp:8[SB]	STZX #IMM8,#IMM8,dsp:8[SB]	POPM dest	JSR.A label
1110	E	SUB.B:S #IMM8,dsp:8[FB]	OR.B:S #IMM8,dsp:8[FB]	DEC.B dsp:8[FB]	NOT.B:S dsp:8[FB]	STZ #IMM8,dsp:8[FB]	STZX #IMM8,#IMM8,dsp:8[FB]	JMPS #IMM8	JMP.B label
1111	F	SUB.B:S #IMM8,abs16	OR.B:S #IMM8,abs16	DEC.B abs16	NOT.B:S abs16	STZ #IMM8,abs16	STZX #IMM8,#IMM8,abs16	JSRS #IMM8	UND

Revision History

Version	Contents for change	Revision date
REV.C	<p>Pages 2, 6 internal interrupt 9 ->13</p> <p>Pages 2, 6 2.7 to 5.5V (f(XIN)=<u>7MHz with software one-wait</u>):mask ROM version ->2.7 to 5.5V (f(XIN)=<u>3.5MHz</u>):mask ROM version</p> <p>Page 6 Power consumption <u>18mA</u> (f(XIN)=<u>7MHz</u> with software one-wait, VCC=3V) -><u>11mA</u> (f(XIN)=<u>3.5MHz</u> , VCC=3V)</p> <p>Page 7 M30201M2-XXXSP/FP, M30201M2T-XXXSP/FP ->Delete M30201M4T-XXXSP, M30201F6T-XXXSP ->Delete M30201M6-XXXFP, M30201M6T-XXXFP ->Addition</p> <p>Pages 10, 11 Figures 1.7 and 1.8 are partly revised.</p> <p>Page 15 Figure 1.11 is partly revised.</p> <p>Page 17 Figure 1.14 is partly revised (Bit 7 of the processor mode register 1). Wait bit ->Reserved bit</p> <p>Page 18 Software wait</p> <p>Page 21 Figure 1.18 is partly revised (Note 8 is partly revised).</p> <p>Page 22 Figure 1.19 is partly revised (n=0716 : approx. <u>16.5kHz</u> -> <u>19.5kHz</u>).</p> <p>Page 34 Figure 1.24 is partly revised (Note 2 is added).</p> <p>Page 50 Figure 1.39 is partly revised.</p> <p>Page 78 Figure 1.72 is partly revised (UARTi transmit/receive mode register).</p> <p>Page 79 Figure 1.73 is partly revised.</p> <p>Page 81 Figure 1.74 is partly revised.</p> <p>Page 86 Figure 1.79 is partly revised.</p> <p>Pages 91 to 97 Figures 1.83 to 1.89 are partly revised.</p> <p>Pages 111 to 114, 119 to 123 Tables 1.36 to 1.39 and 1.56 to 1.71 are partly revised.</p> <p>Page 125 Table 1.74 is partly revised (Boot ROM area <u>4 K</u> bytes -> <u>3.5 K</u> bytes) .</p> <p>Page 143 to 169 Standard serial I/O mode 2 is added.</p>	01.4.12
Revision history	M30201 Group User's Manual	

Version	Contents for change	Revision date
REV.C	Page 204 2.2.15 Precaution for Timer A (one-shot timer mode) (3) is partly revised. Page 219 2.3.7 Precautions for Timer B (pulse period/pulse width measurement mode) (3) is partly revised. Page 309 Table 2.7.11 and Table 2.7.12 are partly revised. Page 320 Figure 2.10.3 is partly revised. Page 324 Table 2.11.1 is partly revised. Page 328 Figure 2.11.6 is partly revised. Page 329 2.11.4 Precautions in Power Control (b) is partly revised. Page 355 Figure 3.6.2 is partly revised. Page 359 Figure 3.7.2 is partly revised.	01.6.8
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