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RENESAS SEMICONDUCTOR RELIABILITY REPORT

DEVICE: M30853FJVGP

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M30853FJVGP (E/W 100cyc Typ.)

RELIABILITY TEST REPORT

This report presents the reliability test results for the M30853FJVGP.
The M30853FJVGP is single-chip 16/32-bit microcomputer using CMOS technology with high performance Si gate process, and this is molded 100-pin plastic flat package.

<FEATURES>
16/32-bit CPU(108 basic machine instructions)
Serial input output ports
Multifunction 16-bit timer
RAM, Flash memory
10-bit A-D converter
8-bit D-A converter
CRC calculation circuit
DMAC
Watchdog timer
Intelligent I/O

1. Reliability test results

We performed the reliability test for the M30853FJVGP.
The failure criteria measuring conditions during reliability test is as follows :

(1)Visual : Solderability - Soldering area of less than 95% of the soaked area
(2)Electrical characteristics
DC(VOH,VOL,IIH,IIL,Icc etc)
Functions (CPU,ROM,RAM,Timer,Interrupt,Frequency etc)

(1) High-Temperature Operating life(HTOL)

Since the operating life test was performed to simulate the continuous system operation in the field use, the test circuit during the operating life test was arranged to simulate the system operation, dynamically excited the internal circuits.
This test circuit is shown in figure 1.
There were no failures, as shown in Table 1.

*Estimated failure ratio
activation energy : $\triangle$ E(the oxide breakdown)=0.3eV
field condition : Ta=55°C and Vcc=5.0V
coefficient of voltage acceleration is 133
coefficient of temperature acceleration is 6.5

0.92/(76×2000×6.5×133)=7FIT(confidence level : 60%)

(2) Humidity test

The 85°C85%RH humidity test and pressure-cooker test were performed. The bias condition during the humidity bias test is shown in Figure 2.
No failures are observed in these humidity test with bias and P.C.T.

(3) ESD

The ESD tests are performed using condenser charge method.
The test circuit for condenser charge method(HBM : human body model) is shown in Figure3
The test results are shown in Figure 5.

(4) Latch-Up(Pulse Current Injection)

The Latch-Up tests are performed using pulse current injection.
The test circuit for pulse current injection is shown in Figure 4, and the test result is shown in Figure 6.

(5) Others, Mechanical stress, environmental test results

There were no failures, as shown in Table 1.

(6) Data retension

This IC has a Flash memory. Main failure modes of this memory are Data retension.
This failure mode is that some programed data is changed "0" to "1" in field use. There are two mode of data retension. One is the random failure mode which is due to the oxide defects, ionic contamination.
It is rare case in mass-production from estimated failure rate at the operating life test.
The other is the intrinsic wear-out failure mode due to the over storage time at normal memory cells.
There are no failure at the data retention test of 96h.
So, the mean time to failure(MTTF) of Data retension is estimated 2.1×10^7 hours at 85°C, using acceleration facton,.

Activation energy (△ E) for intrinsic mode : 1.2eV
Coefficient of temperature acceleration : 2.1×10^5
MTTF = $96h \times 2.1 \times 10^5 = 2.1 \times 10^7$ h

2. Conclusion

It is considered that the M30853FJVGP have sufficient reliability for automotive use.

Table 1. Reliability Test Results M30853FJVGP

Group	Test Items	Test Conditions	LTPD	Sample Size	Failures	N.B.
1	Solderability	215+5/-5°C 10s lead immersed Rosin flux used	10	22	0	(note1)
		245+5/-5°C 5s lead immersed Rosin flux used (Pb Free plating type)	10	22	0	(note1)
2	Resistance to Soldering Heat	IR reflow Ta=255°C 16s, 260°Cmax 3times (note3)	10	22	0	
	Thermal shock	-55°C / 125°C 15cycles (10min/cycle)				
	Temperature Cycle	-65°C / 150°C 1000cycles (1h/cycle)				
3	Lead integrity (Lead Fatigue)	0.5N 10s tension	15	15	0	(note1)
4	Shock	15000m/s ^{2} 0.5ms 3times X1,X2,Y1,Y2,Z1,Z2 directions	10	22	0	(note1)
	Vibration	200m/s ^{2} X,Y,Zdirections 4times 100 - 2000Hz 4min/cycle				
	Acceleration	200000m/s ^{2} X1,X2,Y1,Y2,Z1,Z2directions 1min				
5	High temperature storage	Ta=150°C 2000h	10	22	0	(note4)
6	High-Temperature Operating Life(HTOL)	Ta=125°C 2000h Vcc1=Vcc2=6.5V	3	76	0	Refer to Fig.1 (note4)
7	Low-Temperature Operating Life	Ta=-55°C 2000h Vcc1=Vcc2=6.5V	10	22	0	Refer to Fig.1 (note4)
8	Temperature Humidity Bias(THB)	85°C/85%RH 2000h Vcc1=Vcc2=5.5V	10	22	0	Refer to Fig.2 (note2)
9	Pressure cooker	121°C 100%RH 240h	10	22	0	(note2)
10	ESD	C=100pF, R=1.5k ohm, 1time	-	5	Refer to Fig.5	Refer to Fig.3
11	Latch-Up (Pulse Current Injection)	Pulse Current Injection 1time width 10ms Vcc1=Vcc2=5.5V	-	5	Refer to Fig.6	Refer to Fig.4
12	ERASE/WRITE	Ta=25°C, 100times	10	22	0	
13	Data retension	Ta=250°C, 96h	10	22	0	(note5)

note1) These test is performed by different device with same package type
note2) Preconditioning : Baking(125°C24h)+Absorption(30°C70%RH, 7d)+IR reflow(255°C 16s, 260°Cmax 3times)
note3) Preconditioning : Baking(125°C24h)+Absorption(30°C70%RH, 7d)
note4) Preconditioning : E/W 100 cycles
note5) These test is performed by different device with same wafer process type

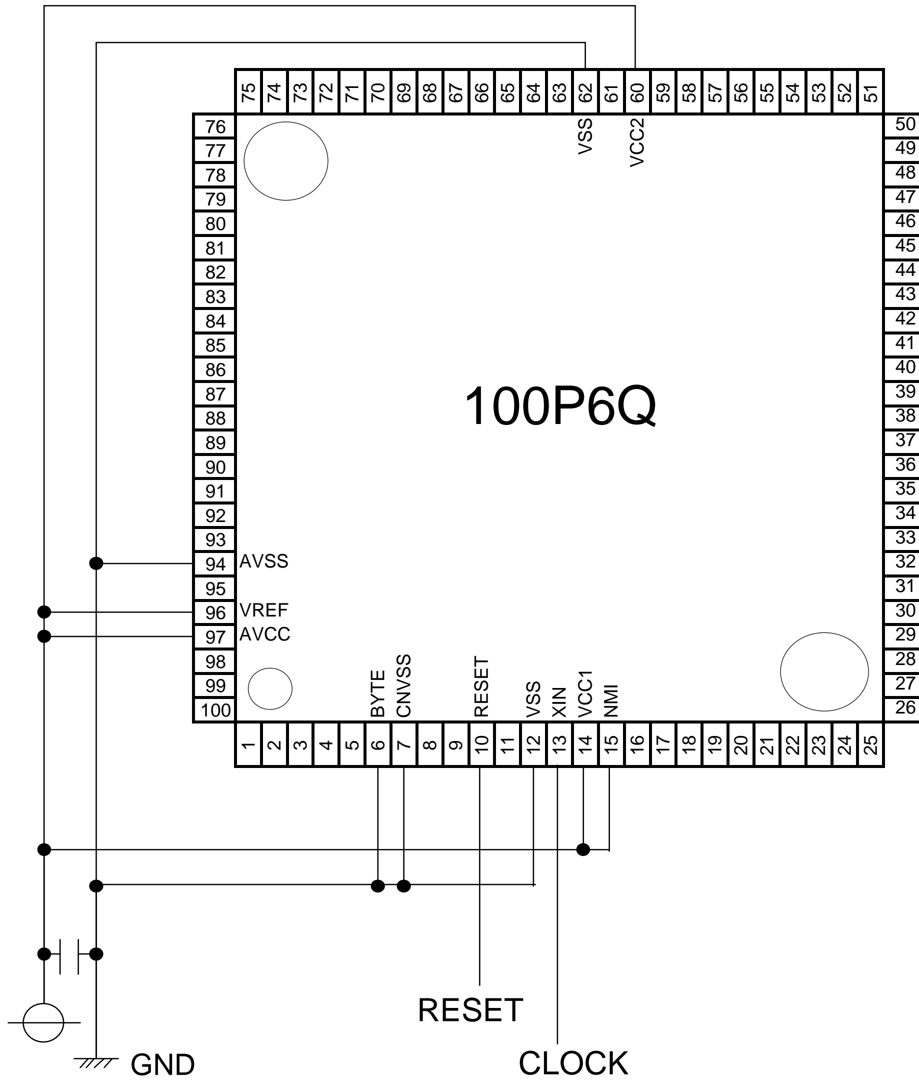

Figure 1. Operating Life Test Circuit

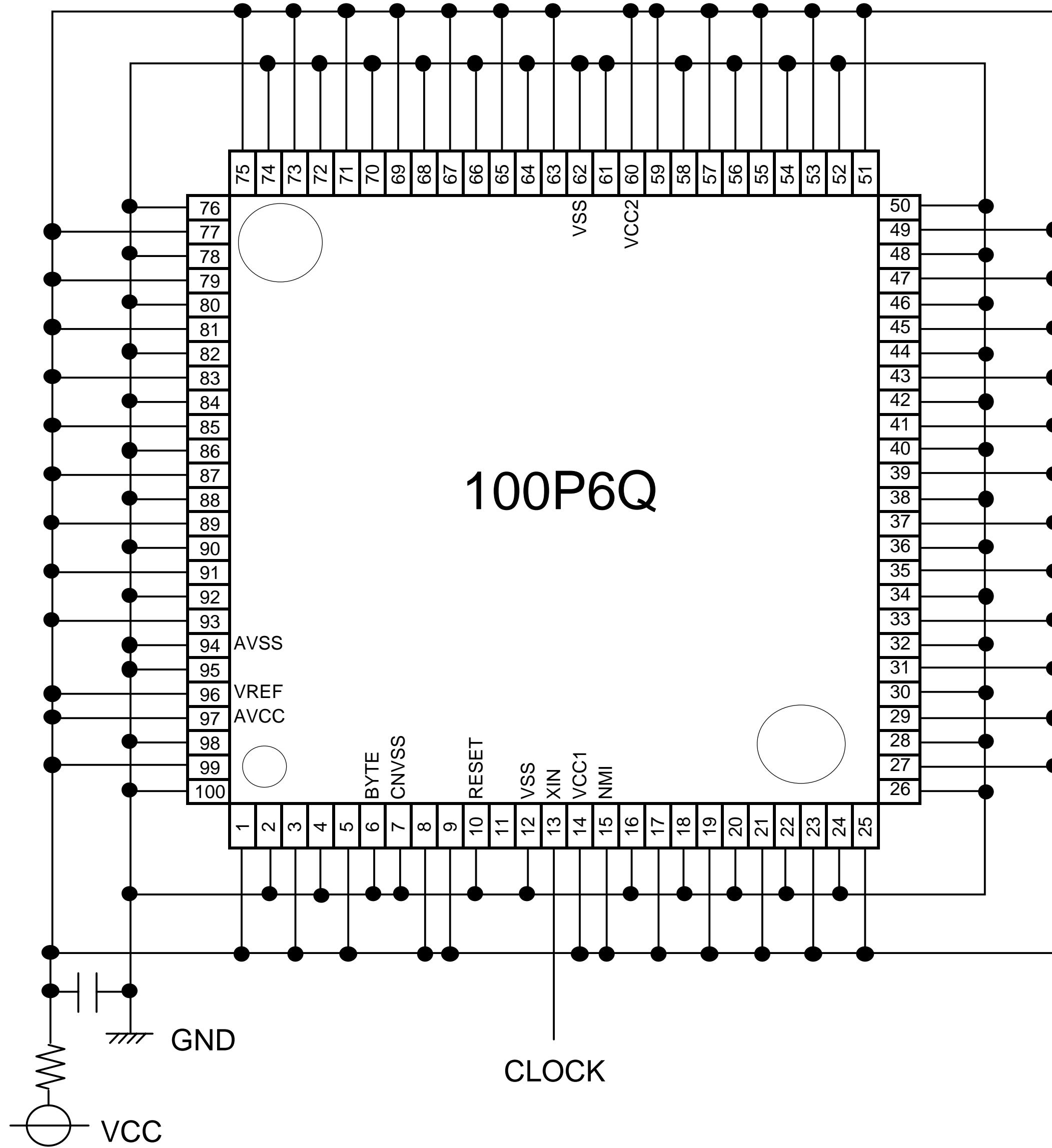

Figure 2. Temperature Humidity Bias Test Circuit

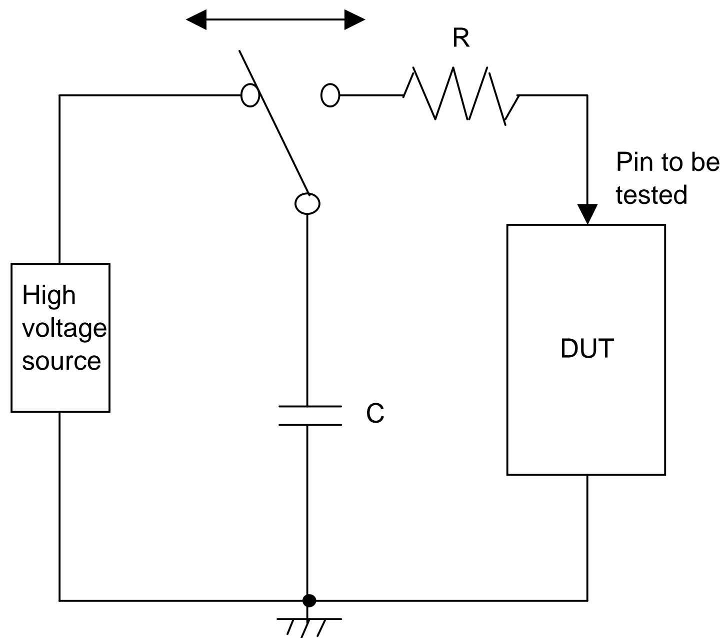

Figure 3. ESD test circuit

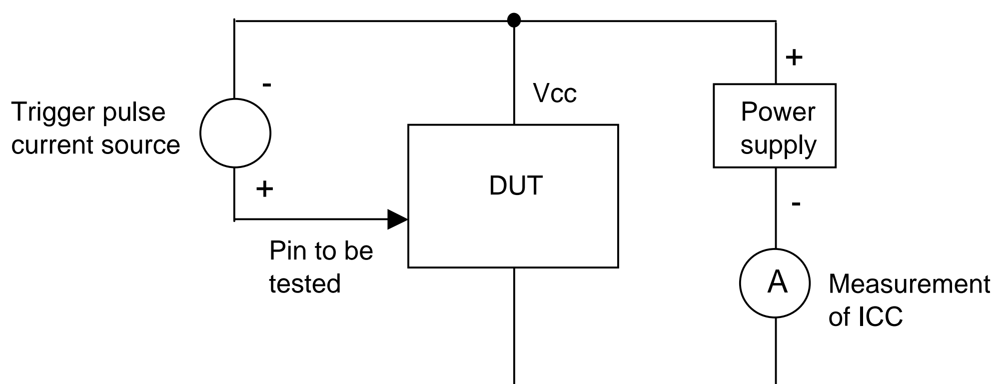

Figure 4-1. Latch-Up test circuit(Positive current)

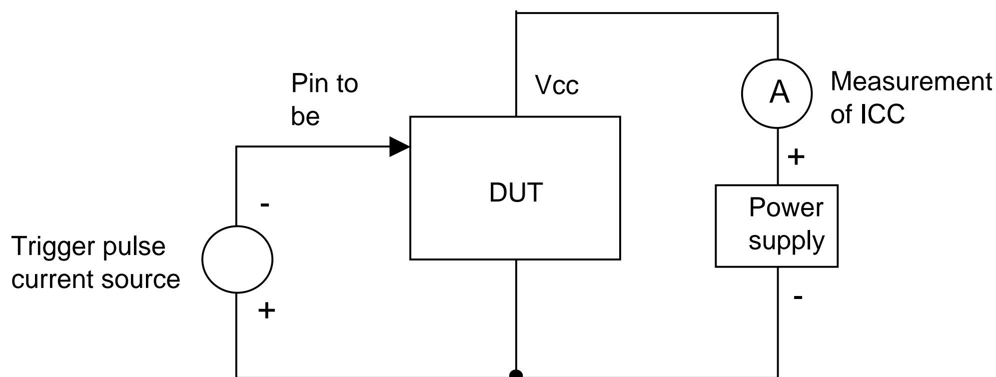

Figure 4-2. Latch-Up test circuit(Negative current)

Figure5-1. The result of Electrostatic discharge sensitivity
100pF,1.5k ohm, Vss=AVss=COM

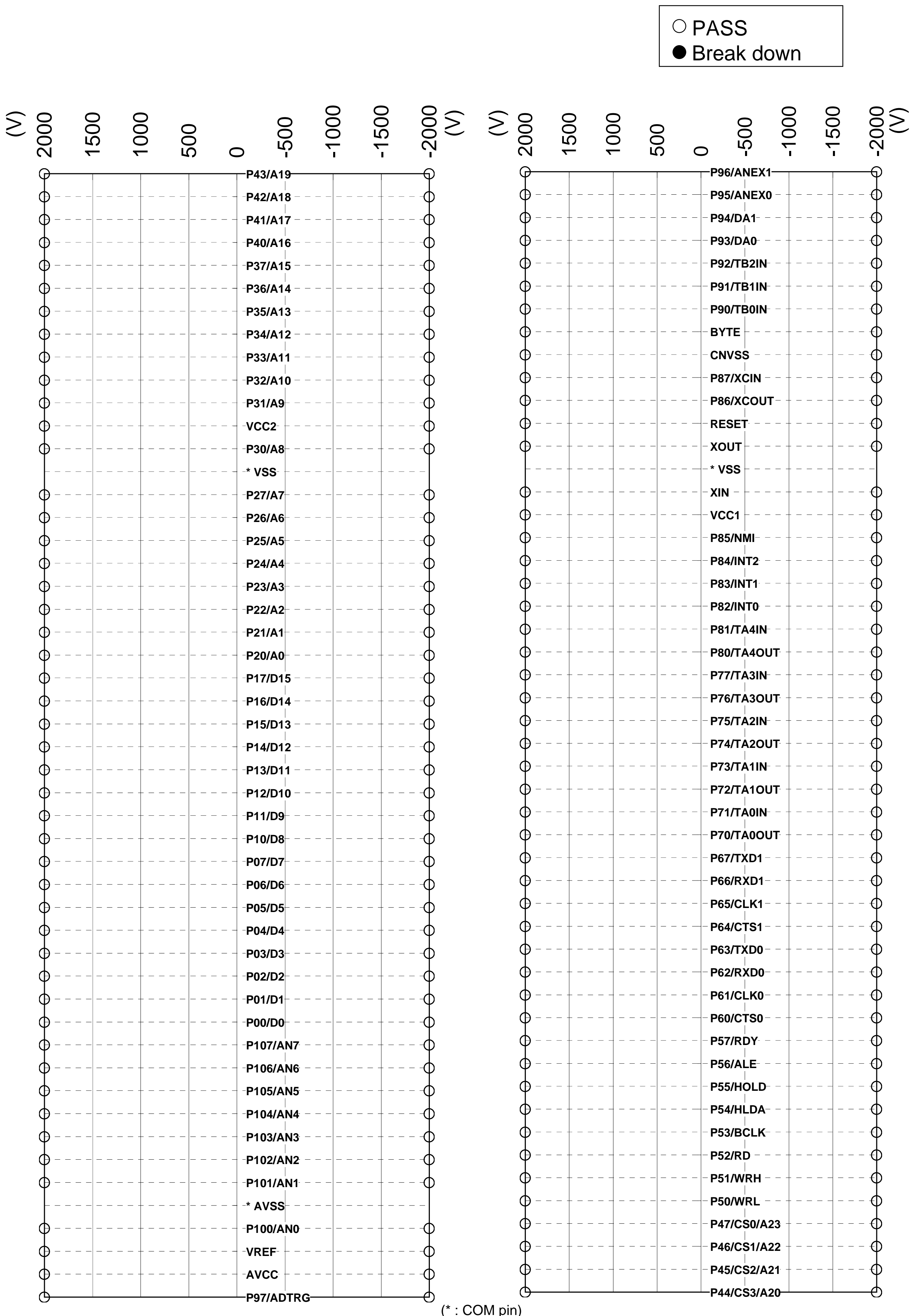

Figure5-2. The result of Electrostatic discharge sensitivity
100pF,1.5k ohm, Vcc1=Vcc2=AVcc=COM

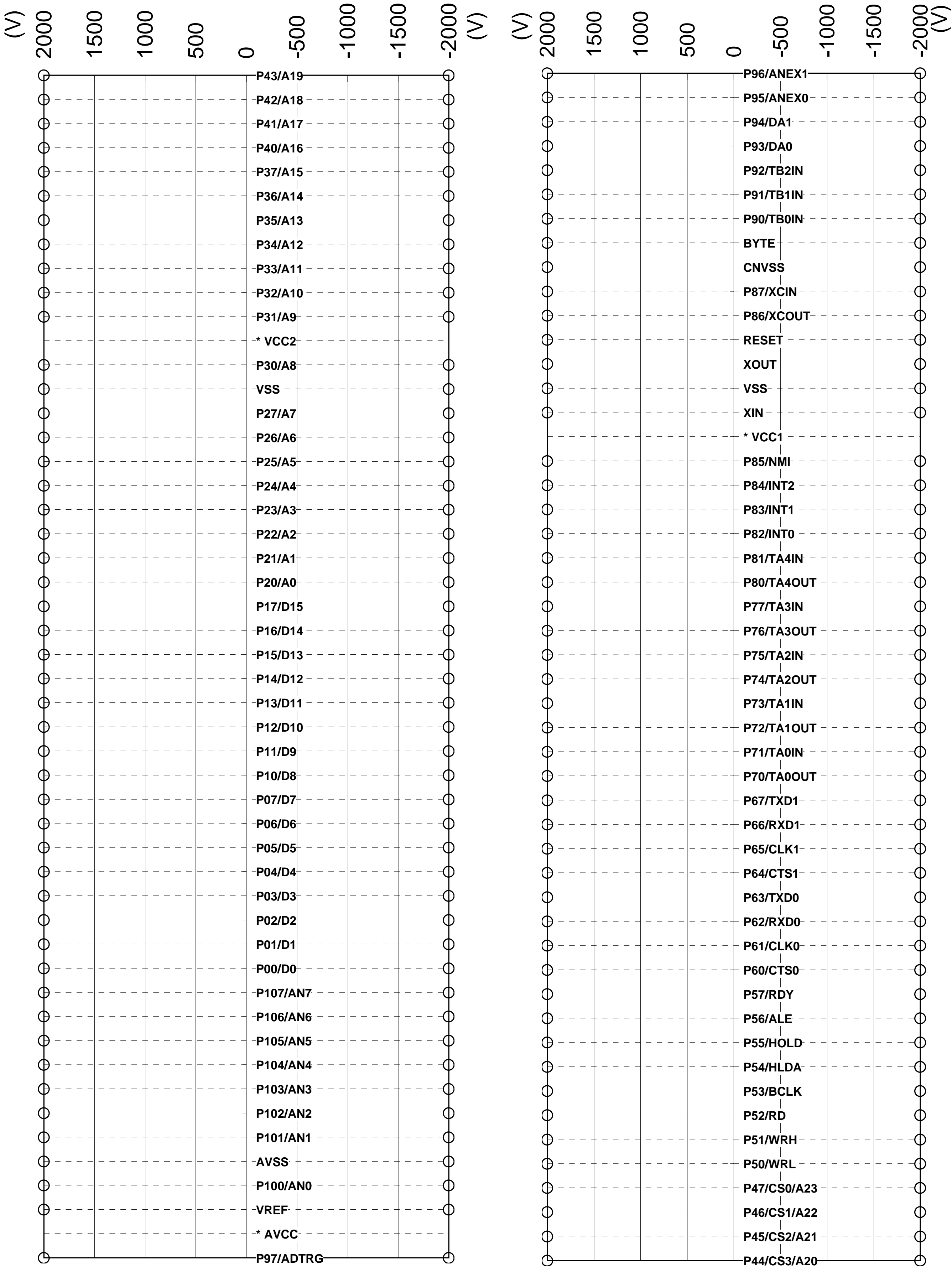

Figure6. The result of Latch-Up immunity

Vcc1=Vcc2=AVcc=5.5V, Vss=AVss=0V