FUJITSU

UV ERASABLE 262144-BIT READ ONLY MEMORY

MBM 27256-17
MBM 27256-20
MBM 27256-25

February 1986
Edition 3.0

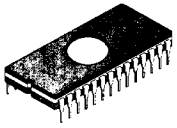
MOS 262144 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

The Fujitsu MBM 27256 is a high speed 262,144-bit static NMOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for applications where rapid turn-around and/or bit pattern experimentation are important.

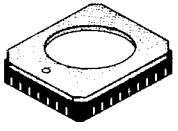
A 28-pin Dual In-Line package and a 32-pad Leadless Chip Carrier with a transparent lid is used to package the MBM 27256. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM 27256 is fabricated using NMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 32,768 words by 8 bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.

- 32,768 words x 8 bits organization, fully decoded
- Single location programming
- Programmable utilizing the Quick Pro™ algorithm
- Program voltage: 12.5V
- Low power requirement
  - Active: 525mW
  - Standby: 210mW
- No clocks required (fully static operation)
- Output Enable ($\overline{OE}$) pin for simple memory expansion
- Fast access time:
  170ns max. (MBM 27256-17)
  200ns max. (MBM 27256-20)
  250ns max. (MBM 27256-25)
- TTL compatible inputs/outputs
- Three-state output with OR-tie capability
- Single +5V supply, ±5% tolerance
- Standard 28-pin Ceramic (Cerdip)
  DIP: Suffix-Z
  Standard 32-pad Ceramic
  LCC: Suffix-CV

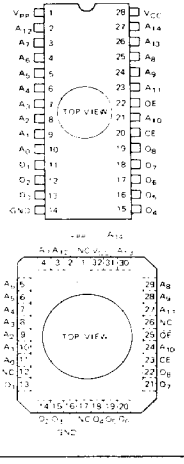


CERAMIC PACKAGE
DIP-28C-C01



CERAMIC PACKAGE
LCC-32C-A01

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage with Respect to GND	V_{CC}	-0.6 to +7	V
V_{PP} Voltage with Respect to GND	V_{PP}	-0.6 to +14	V
Voltage on A_9 with Respect to GND	V_{A9}	-0.6 to +13.5	V
All Inputs/Outputs Voltage with Respect to GND	V_{IN}, V_{OUT}	-0.6 to +7	V
Temperature under Bias	T_{BIAS}	-25 to +85	°C
Storage Temperature	T_{STG}	-65 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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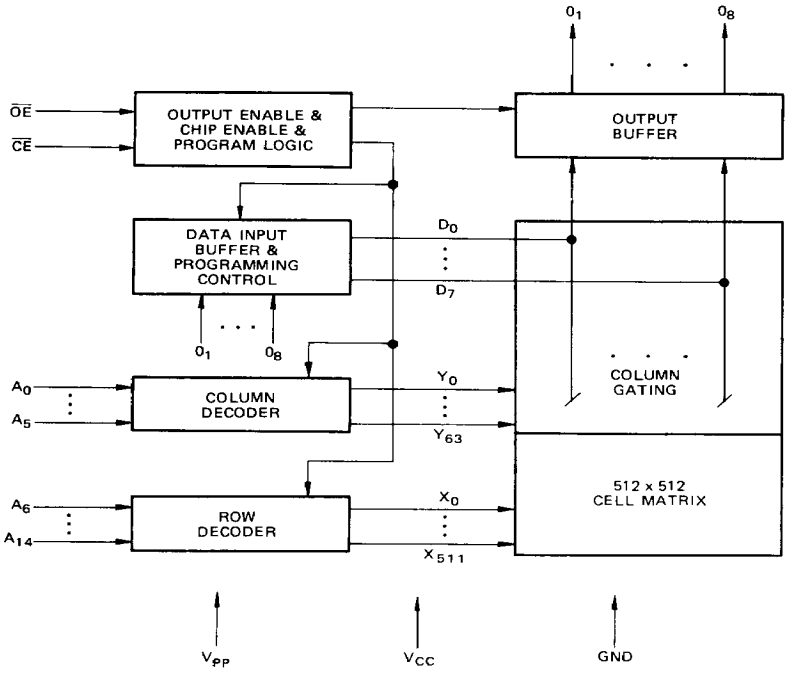
Fig. 1 – MBM 27256 BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}		4	6	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}		8	12	pF

FUNCTIONS AND PIN CONNECTIONS

Function (Pin No.) / Mode	Address Input (2 ~ 10, 21, 23, 25 ~ 27)	A_9 (24)	Data I/O (11 ~ 13, 15 ~ 19)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{CC} (28)	V_{PP} (1)	GND (14)
Read	A_{IN}	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	+5V	+5V	GND
Output Disable	A_{IN}	A_{IN}	High-Z	V_{IL}	V_{IH}	+5V	+5V	GND
Standby	Don't Care	Don't Care	High-Z	V_{IH}	Don't Care	+5V	+5V	GND
Program	A_{IN}	A_{IN}	D_{IN}	V_{IL}	V_{IH}	+6V	+12.5V	GND
Program Verify	A_{IN}	A_{IN}	D_{OUT}	Don't Care	V_{IL}	+6V	+12.5V	GND
Program Inhibit	Dont't Care	Don't Care	High-Z	V_{IH}	V_{IH}	+6V	+12.5V	GND
Electronic Signature	A_{IN}	+12V	Code	V_{IL}	V_{IL}	+5V	+5V	GND

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RECOMMENDED OPERATING CONDITIONS
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} Supply Voltate*	V_{CC}	4.75	5.0	5.25	V
V_{PP} Supply Voltage	V_{PP}	V_{CC} -0.6		V_{CC} +0.6	V
Input High Voltage	V_{IH}	2.0		V_{CC} + 1	V
Input Low Voltage	V_{IL}	-0.1		0.8	V
Operating Temperature	T_A	0		70	°C

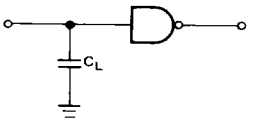
Note: *V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.

DC CHARACTERISTICS
(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current (V_{IN} = 5.25V)	$\|I_{LI}\|$			10	μA
Output Leakage Current (V_{OUT} = 5.25V)	$\|I_{LO}\|$			10	μA
V_{CC} Standby Current ($\overline{CE}$ = V_{IH})	I_{CC1}			40	mA
V_{CC} Supply Current ($\overline{CE}$ = V_{IL})	I_{CC2}			100	mA
V_{PP} Supply Current (V_{PP} = V_{CC} ± 0.6V)	I_{PP1}			5	mA
Output Low Voltage (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage (I_{OH} = -400μA)	V_{OH}	2.4			V

Fig. 2 — AC TEST CONDITIONS (INCLUDING PROGRAMMING)

Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Times:	≤ 20ns
Timing Measurement Reference Levels:	0.8V and 2.0V for inputs 0.8V and 2.0V for outputs
Output Load:	1 TTL gate and C_L = 100pF



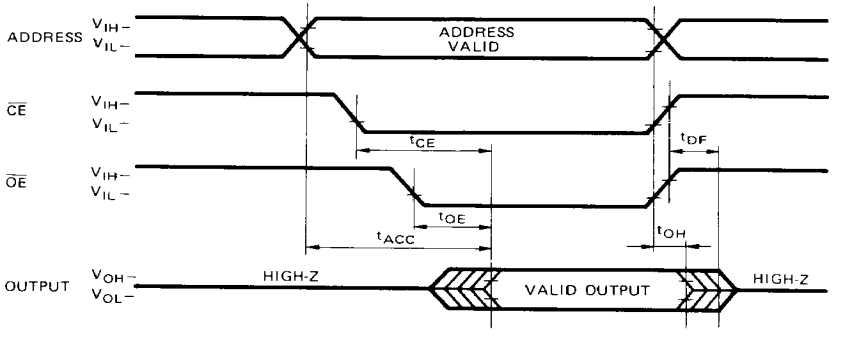
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	MBM 27256-17			MBM 27256-20			MBM 27256-25			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Address Access Time*1 ($\overline{CE}$ = $\overline{OE}$ = V_{IL})	t_{ACC}			170			200			250	ns
$\overline{CE}$ to Output Delay ($\overline{OE}$ = V_{IL})	t_{CE}			170			200			250	ns
$\overline{OE}$ to Output Delay*1 ($\overline{CE}$ = V_{IL})	t_{OE}			75			75			100	ns
Address to Output Hold	t_{OH}	0			0			0			ns
Output Enable High to Output Float*2	t_{DF}	0		60	0		60	0		105	ns

Notes: *1 $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
*2 t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
Output Float is defined as the point where data is no longer driven.

OPERATION TIMING DIAGRAM



CHARACTERISTICS CURVES

Fig. 3 – SUPPLY CURRENT (STANDBY) vs. SUPPLY VOLTAGE

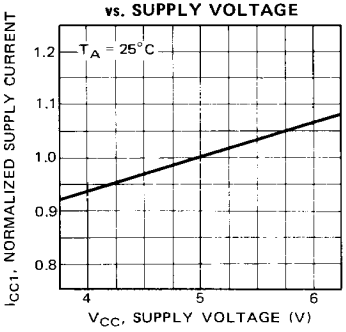


Fig. 4 – SUPPLY CURRENT (STANDBY) vs. AMBIENT TEMPERATURE

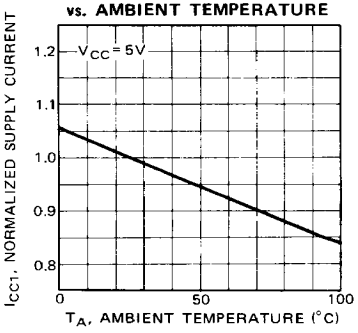


Fig. 5 – SUPPLY CURRENT (ACTIVE) vs. SUPPLY VOLTAGE

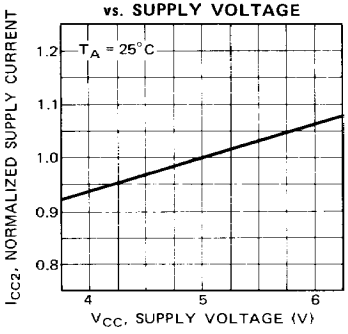


Fig. 6 – SUPPLY CURRENT (ACTIVE) vs. AMBIENT TEMPERATURE

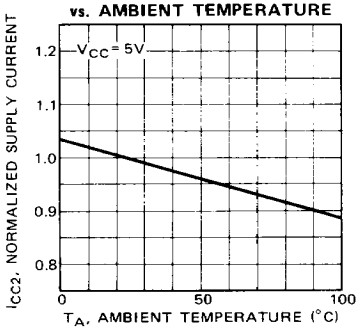


Fig. 7 – ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE

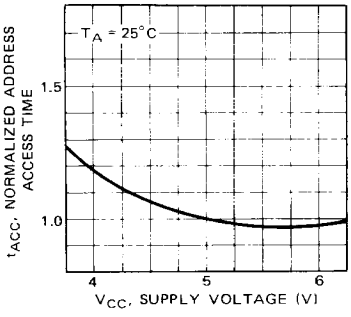


Fig. 8 – ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE

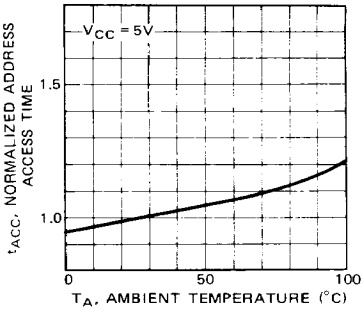


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Fig. 9 – $\overline{CE}$ TO OUTPUT DELAY vs. AMBIENT TEMPERATURE

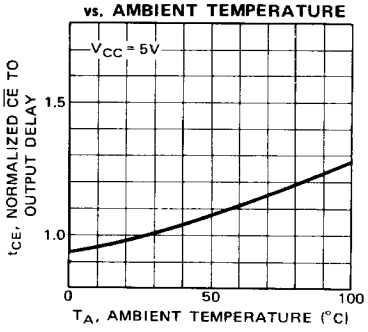


Fig. 10 – $\overline{CE}$ TO OUTPUT DELAY vs. SUPPLY VOLTAGE

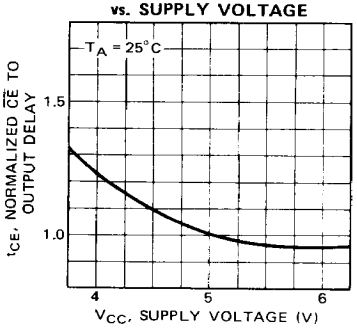


Fig. 11 – $\overline{OE}$ TO OUTPUT DELAY
$\overline{OE}$ HIGH TO OUTPUT FLOAT vs. AMBIENT TEMPERATURE

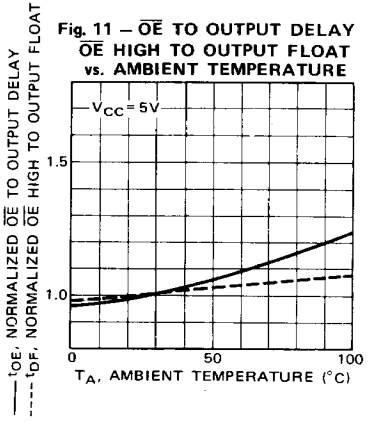


Fig. 12 – OUTPUT SOURCE CURRENT vs. OUTPUT HIGH VOLTAGE

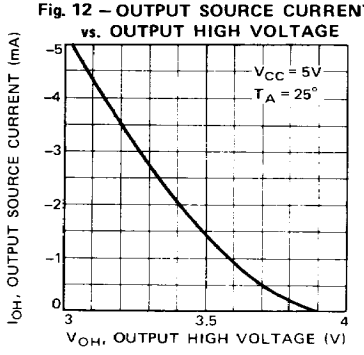


Fig. 13 – OUTPUT SINK CURRENT vs. OUTPUT LOW VOLTAGE

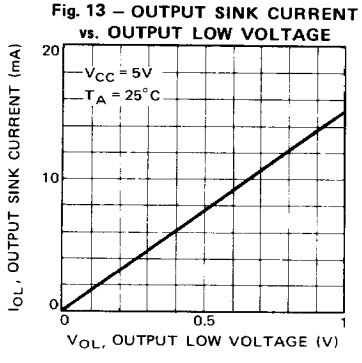
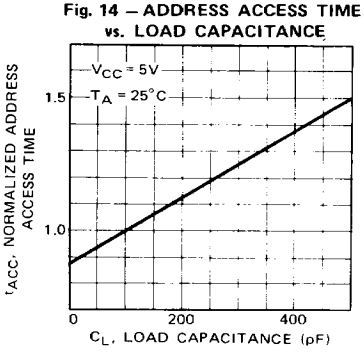


Fig. 14 – ADDRESS ACCESS TIME vs. LOAD CAPACITANCE



PROGRAMMING/ERASING INFORMATION

PROGRAMMING

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM 27256 has all 262,144 bits in the "1", or high state. "0's" are loaded into the MBM 27256 through the procedure of programming.

The MBM 27256 is programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The programming mode is entered when +12.5V and +6V are applied to V_{PP} and V_{CC} respectively, and $\overline{CE}$ and $\overline{OE}$ are V_{IH}. A 0.1μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device. The address to be programmed is applied to the proper address pins. The 8 bit data pattern to be written is placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 1ms programming pulse is applied to $\overline{CE}$ and after that one additional pulse which is 3 times as wide as previous pulse is applied to $\overline{CE}$ to accomplish the programming.

Procedure of Quick Pro™ (Refer to the attached flowchart.)

1) Set the start address (=G) at the address pins.
2) Set V_{CC} = 6V, V_{PP} = 12.5V and $\overline{CE}$ = V_{IH}.
3) Clear the programming pulse counter (X ← 0).
4) Input data to respective pins.
5) Apply ONE programming pulse (t_{PW} = 1ms Typ.) to $\overline{CE}$.
6) Increment the counter (X ← X+1).
7) Compare the number (=X) of applied programming pulse with 25 and then verify the programmed data. If programmed data is verified, go to the next step regardless of X value. If X = 25 and programmed data is not verified, the device fails. If X = 25 and programmed data is not verified, go back to the step 5).
8) Apply one additional wide programming pulse to $\overline{CE}$ (3X ms).
9) Compare the address with an end address (=N). If the programmed address is the end address, proceed to the next step. If not, increment the address (G ← G+1) and then go to the step 3) for the next address.
10) Set V_{CC} = V_{PP} = 5V.
11) Verify the all programmed data. If the verification succeeds, the programming completes. If any programmed data is not the same as original data, the device fails.

A continuous TTL low level should not apply to $\overline{CE}$ input pin during the program mode (V_{PP} = 12.5V, V_{CC} = 6V and $\overline{OE}$ = V_{IH}) because it is required that one programming pulse width does not exceed 78.75 ms at each address.

ERASURE

In order to clear all locations of their programmed contents it is necessary to expose the MBM 27256 to an ultraviolet light source. A dosage of 15 W-seconds/cm^2 is required to completely erase an MBM 27256. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000μW/cm^2 for 15 to 21 minutes.

The MBM 27256 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM 27256 and similar devices, will erase with light sources having wavelengths shorter than 4000Å. Although erasure time will be much longer than with UV source at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MBM 27256, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

ELECTRONIC SIGNATURE

The MBM 27256 has electronic signature mode which is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm.

The electronic signature is activated when +12V is applied to address line A_9 (pin 24) of the MBM 27256. Two identifier bytes are readed out from the outputs by toggling address line A_0 (pin 10) from V_{IL} to V_{IH}. The address lines from A_1 to A_{13} must be hold at V_{IL} to keep the electronic signature mode. See the table below.

A_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	Definition
V_{IL}	0	0	1	0	0	0	0	0	Manufacture
V_{IH}	0	1	0	0	0	0	0	0	Device

Note: A_9 = 12V ± 0.5V
A_1 thru A_8 = A_{10} thru A_{13} = $\overline{CE}$ = $\overline{OE}$ = V_{IL}
A_{14} = Either V_{IL} or V_{IH}

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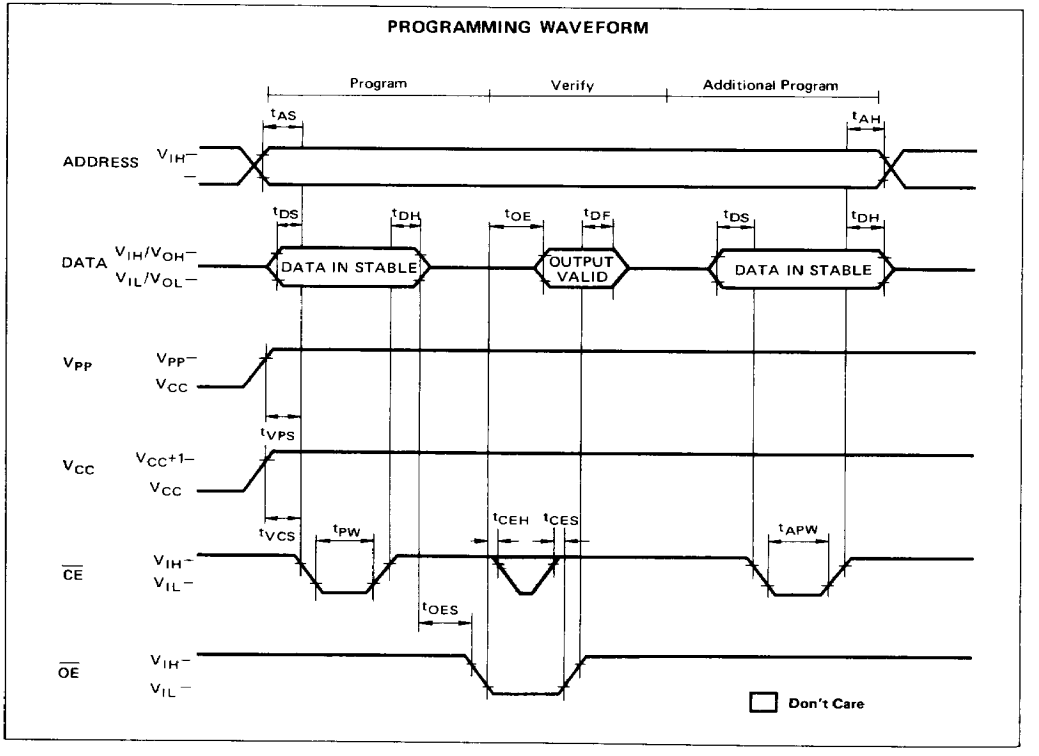
PROGRAMMING/ERASING INFORMATION (Cont'd)



DC CHARACTERISTICS
(T_A = 25±5°C, V_{CC} *1=6V±0.25V, V_{PP} *2=12.5V±0.3V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = 6.25V/0.45V)	$\|I_{LI}\|$			10	μA
V_{PP} Supply Current ($\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH})	I_{PP2}			50	mA
V_{PP} Supply Current ($\overline{OE}$ = V_{IL})	I_{PP3}			5	mA
V_{CC} Supply Current	I_{CC3}			100	mA
Input Low Level	V_{IL}	-0.1		0.8	V
Input High Level	V_{IH}	2.0		V_{CC}+1	V
Output Low Voltage During Verify (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage During Verify (I_{OH} = -400μA)	V_{OH}	2.4			V

Note: *1 V_{CC} must be applied either coincidently or before V_{PP} and removed either concidently or after V_{PP}.
*2 V_{PP} must not be greater than 14 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 12.5 volts. Also, during $\overline{CE}$ = V_{IL} $\overline{OE}$ = V_{IH}, V_{PP} must not be switched from V_{CC} to V_{PP} volts or vice versa.

AC CHARACTERISTICS
(T_A = 25±5°C, V_{CC} = 6V±0.25V, V_{PP} = 12.5V±0.3V)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	2			μs
Output Enable Setup Time	t_{OES}	2			μs
Chip Enable Setup Time	t_{CES}	2			μs
Data Setup Time	t_{DS}	2			μs
V_{PP} Setup Time	t_{VPS}	2			μs
V_{CC} Setup Time	t_{VCS}	2			μs
Address Hold Time	t_{AH}	2			μs
Data Hold Time	t_{DH}	2			μs
Chip Enable Hold Time	t_{CEH}	2			μs
Output Enable to Output Valid	t_{OE}			120	ns
Output Disable to Output Float Delay	t_{DF}			105	ns
Programming Pulse Width	t_{PW}	0.95	1	1.05	ms
Programming Pulse Number		1		25	times
Additional Programming Pulse width	t_{APW}	2.85		78.75	ms

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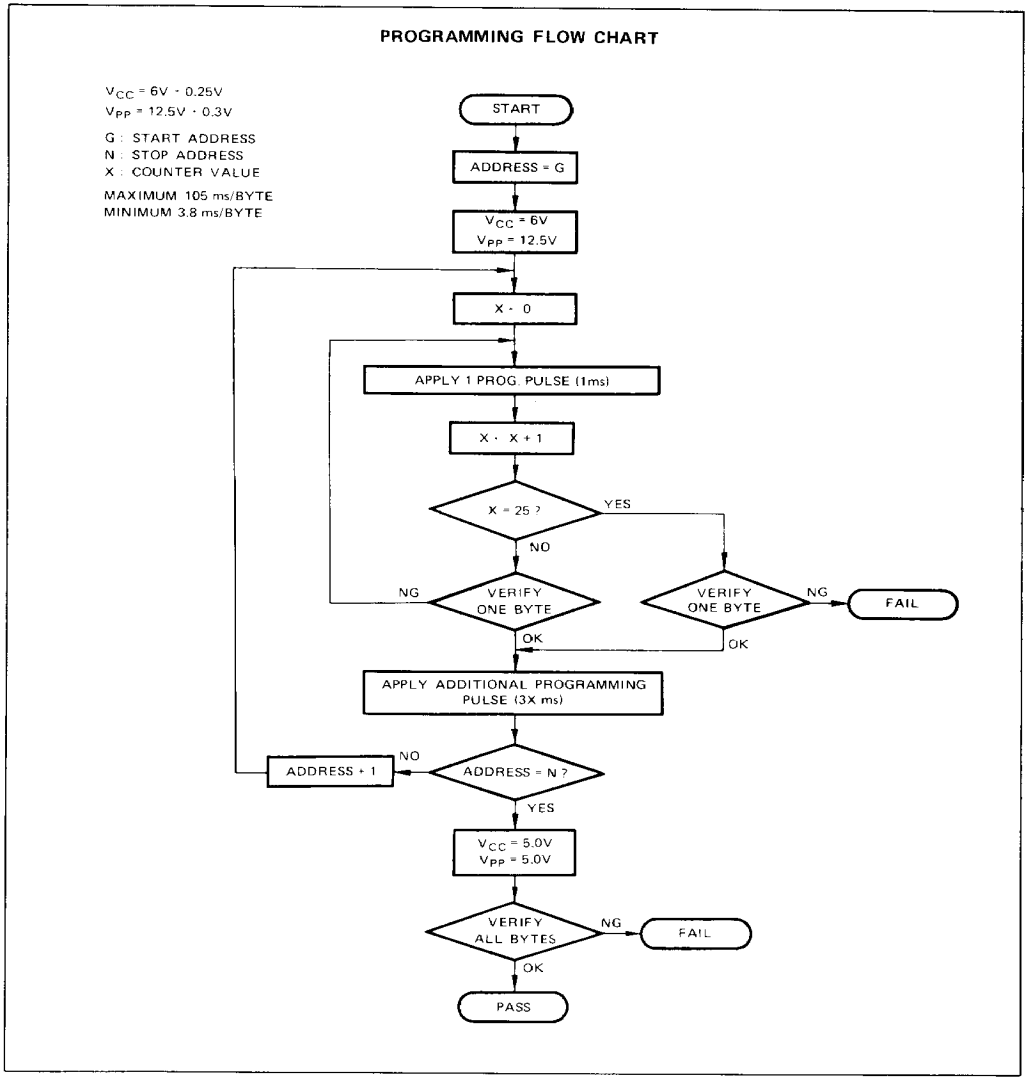
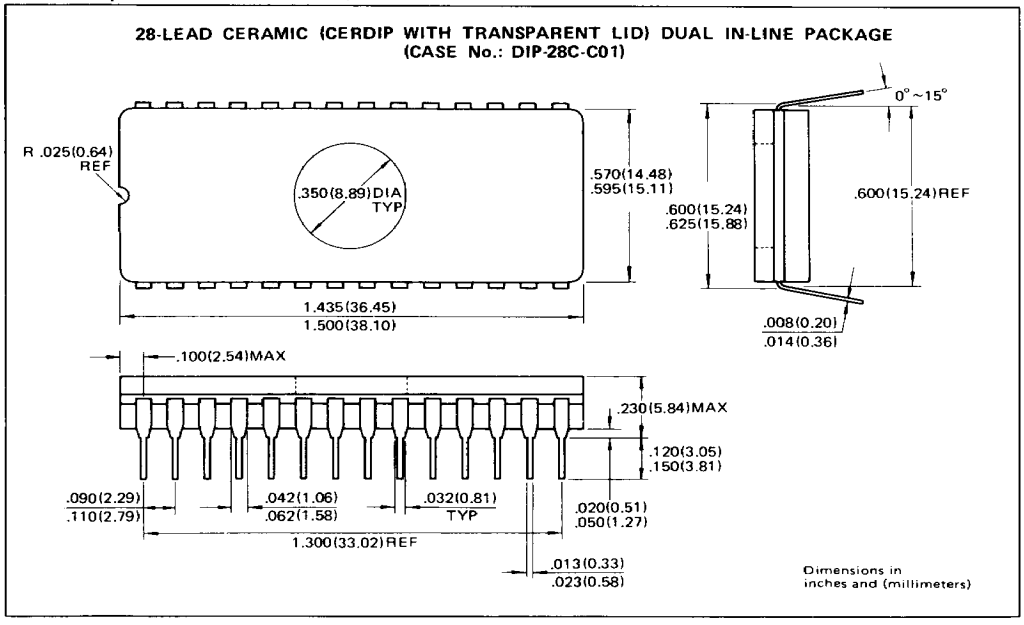
PROGRAMMING/ERASING INFORMATION (Cont'd)



PACKAGE DIMENSIONS

Standerd 28-pin Ceramic DIP (Suffix : -Z)



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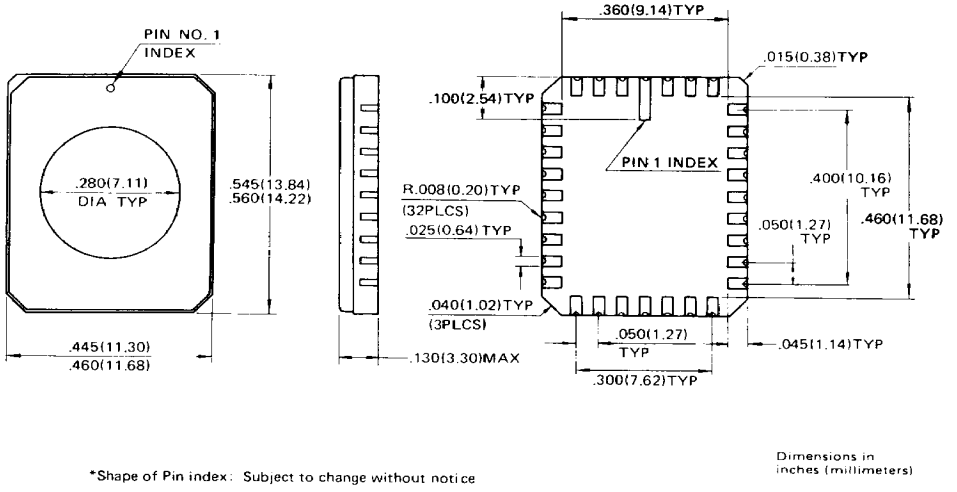
PACKAGE DIMENSIONS

Standerd 32-pad Ceramic LCC (Suffix : -CV)

32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No. : LCC-32C-A01)



*Shape of Pin index: Subject to change without notice

Dimensions in
inches (millimeters)

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