DS05–20810–3E

FLASH MEMORY

CMOS

4M (512K × 8) BIT

MBM29F040A - 70/-90/-12

■ DISTINCTIVE CHARACTERISTICS

- **Single 5.0 V read, write and erase**
  Minimizes system level power requirements
- **Compatible with JEDEC-standard commands**
  Uses same software commands as E^2PROMs
- **Compatible with JEDEC-standard byte-wide pinouts**
  32-pin PLCC (Package suffix: PD)
  32-pin TSOP (Package suffix: PFTN – Normal Bend Type, PFTR – Reversed Bend Type)
  Note: If there are special requirements not specified above (such as DIP package), please contact Fujitsu sales office.

- **Minimum 100,000 write/erase cycles**
- **High performance**
  70 ns maximum access time
- **Sector erase architecture**
  8 equal size sectors of 64K bytes each
  Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Embedded Erase™ Algorithms**
  Automatically pre-programs and erases the chip or any sector
- **Embedded Program™ Algorithms**
  Automatically writes and verifies data at specified address
- **Data Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Low power consumption**
  20 mA typical active read current
  30 mA typical write/erase current
  25 µA typical standby current
- **Low Vcc write inhibit ≤ 3.2 V**
- **Sector protection**
  Hardware method disables any combination of sectors from write or erase operations
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read data in another sector within the same device

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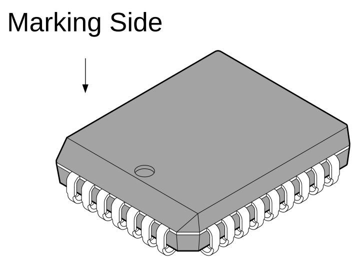
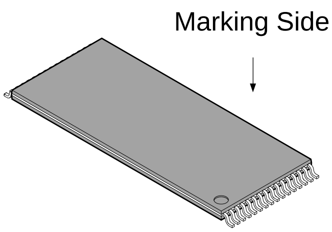
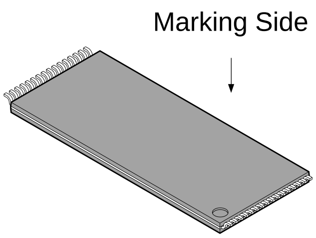
■ PACKAGE



32-pin Plastic LCC
(LCC-32P-M02)



32-pin Plastic TSOP
(FPT-32P-M24 — Assembly: Malaysia)



32-pin Plastic TSOP
(FPT-32P-M25 — Assembly: Malaysia)

■ GENERAL DESCRIPTION

The MBM29F040A is a 4M-bit, 5.0 V-only Flash memory organized as 512K bytes of 8 bits each. The MBM29F040A is offered in a 32-pin PLCC and 32-pin TSOP package. This device is designed to be programmed in-system with the standard system 5.0 V VCC supply. A 12.0 V VPP is not required for write or erase operations. The device can also be reprogrammed in standard EPROM programmers.

The standard MBM29F040A offers access times between 70 ns and 120 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$), and output enable ($\overline{OE}$) controls.

The MBM29F040A is pin and command set compatible with JEDEC standard 4M-bit E^2PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0 V Flash or EPROM devices.

The MBM29F040A is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in less than one second. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The entire chip or any individual sector is typically erased and verified in 1.5 seconds. (If already completely preprogrammed.)

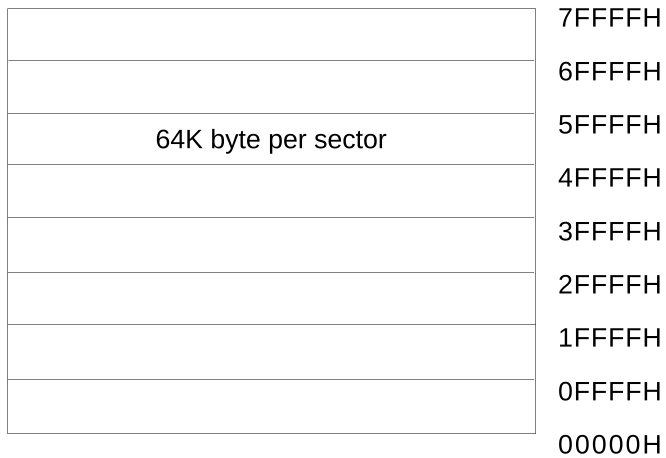
This device also features a sector erase architecture. The sector mode allows for 64K byte sectors of memory to be erased and reprogrammed without affecting other sectors. The MBM29F040A is erased when shipped from the factory.

The device features single 5.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{Data}$ Polling of DQ_7 or by the Toggle Bit feature on DQ_6. Once the end of a program or erase cycle has been completed, the device internally resets to the read mode.

Fujitsu's Flash technology combines years of EPROM and E^2PROM experience to produce the highest levels of quality, reliability and cost effectiveness. The MBM29F040A memory electrically erases the entire chip or all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

FLEXIBLE SECTOR-ERASE ARCHITECTURE

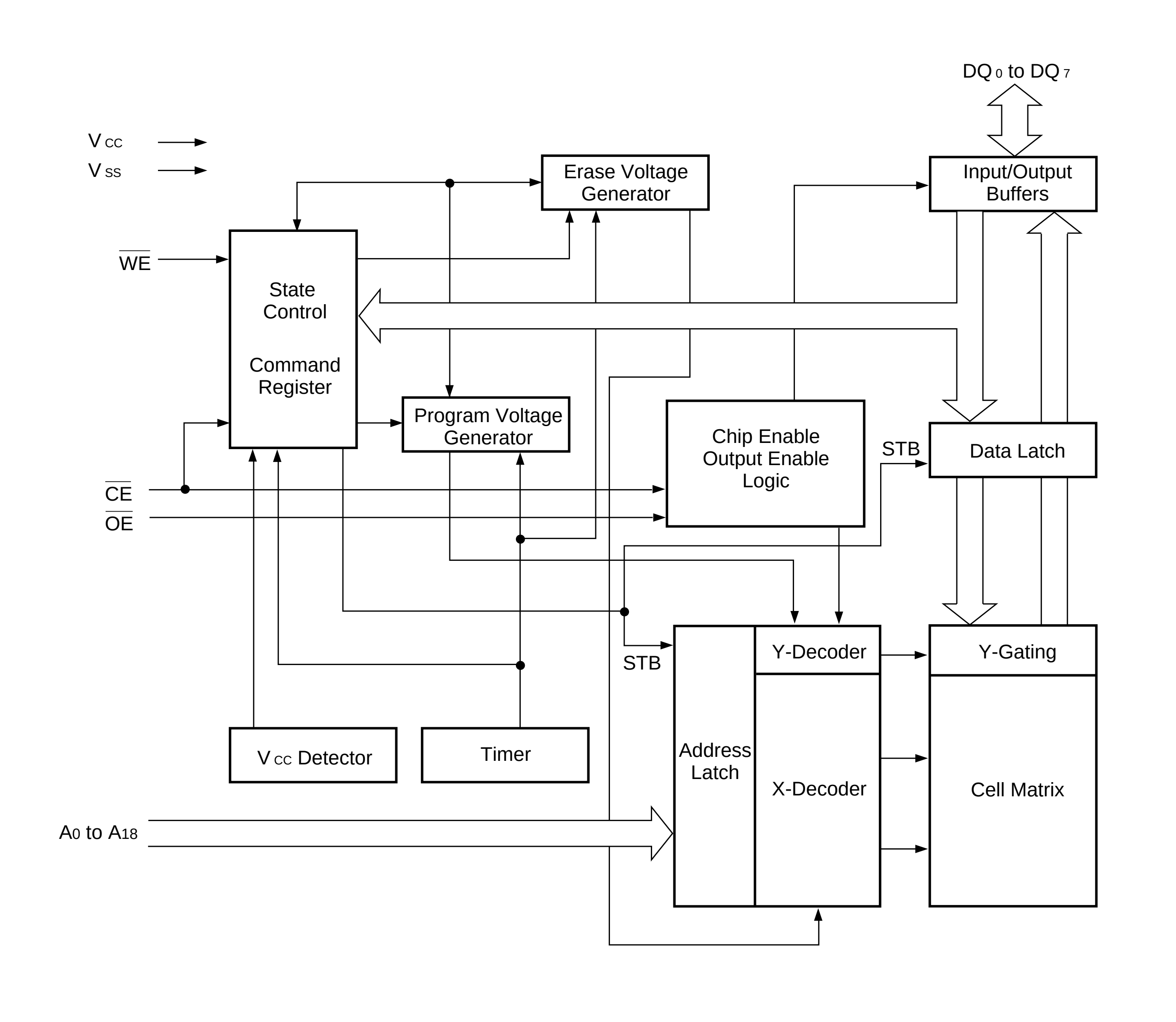
- 64K byte per sector
- Individual-sector, multiple-sector, or bulk-erase capability
- Individual or multiple-sector protection is user definable



■ PRODUCT SELECTOR GUIDE

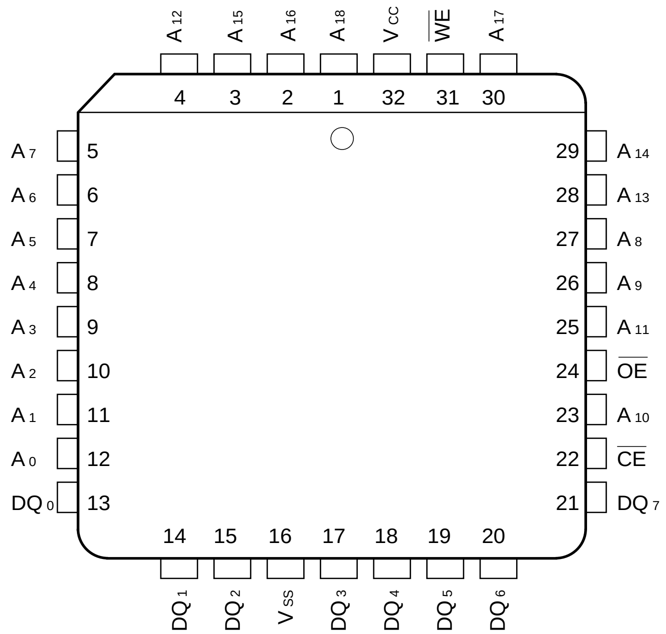
Part No.		MBM29F040A		
Ordering Part No.	V_{CC} = 5.0 V ± 5 %	MBM29F040A – 70	—	—
	V_{CC} = 5.0 V ± 10 %	—	MBM29F040A – 90	MBM29F040A – 12
Max. Access Time (ns)		70	90	120
$\overline{CE}$ Access (ns)		70	90	120
$\overline{OE}$ Access (ns)		30	35	50

■ BLOCK DIAGRAM



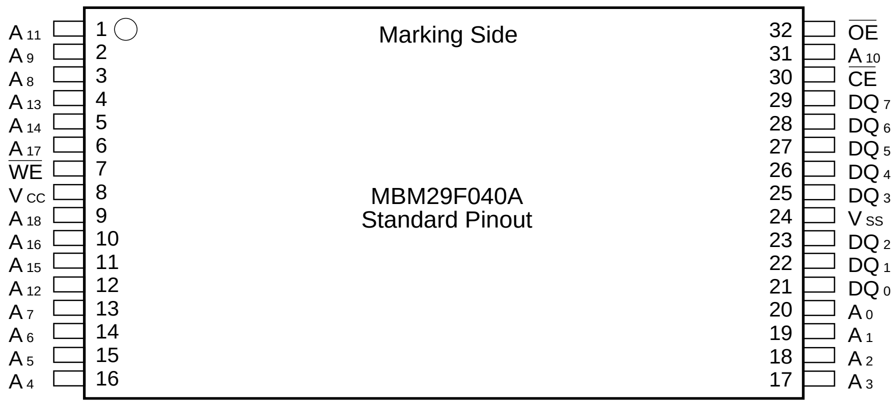
■ CONNECTION DIAGRAMS

PLCC

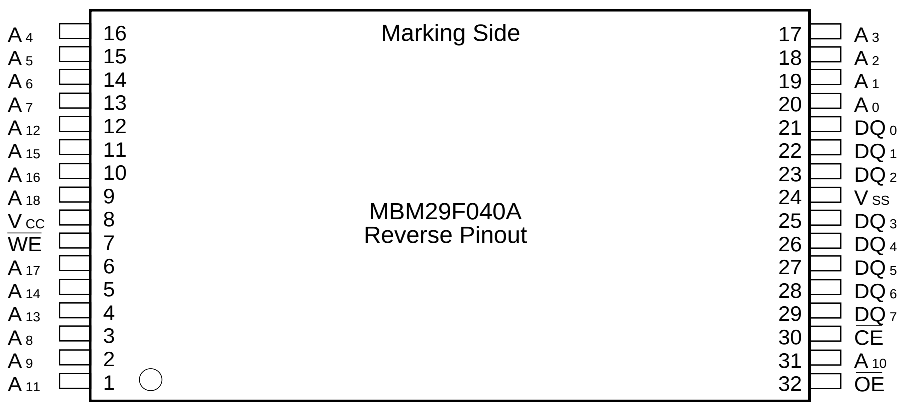


LCC-32P-M02

TSOP



FPT-32P-M24



FPT-32P-M25

■ LOGIC SYMBOL

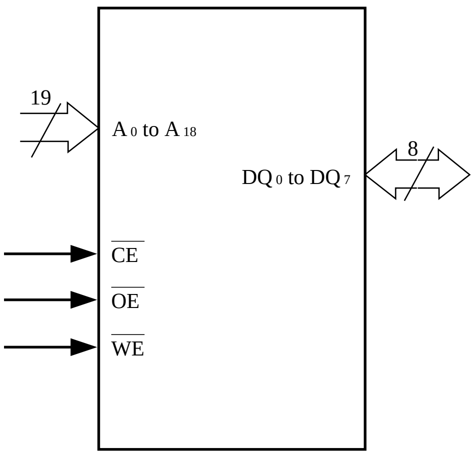


Table 1 MBM29F040A Pin Configuration

Pin	Function
A_0 to A_{18}	Address Inputs
DQ_0 to DQ_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{SS}	Device Ground
V_{CC}	Device Power Supply (5.0 V ± 10 % or ± 5 %)

Table 2 MBM29F040A User Bus Operations

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A_0	A_1	A_6	A_9	I/O
Auto-Select Manufacturer Code (1)	L	L	H	L	L	L	V_{ID}	Code
Auto-Select Device Code (1)	L	L	H	H	L	L	V_{ID}	Code
Read (3)	L	L	H	A_0	A_1	A_6	A_9	D_{OUT}
Standby	H	X	X	X	X	X	X	HIGH-Z
Output Disable	L	H	H	X	X	X	X	HIGH-Z
Write	L	H	L	A_0	A_1	A_6	A_9	D_{IN}
Enable Sector Protection (2)	L	V_{ID}	L	X	X	X	V_{ID}	X
Verify Sector Protection (2)	L	L	H	L	H	L	V_{ID}	Code

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.

Notes: 1. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 5.
2. Refer to the section on Sector Protection.
3. $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.

■ ORDERING INFORMATION

Standard Products

Fujitsu standard products are available in several packages. The order number is formed by a combination of:

MBM29F040A –90 PD

PACKAGE TYPE
PD = 32-Pin Rectangular Plastic Leaded Chip Carrier (PLCC)
PFTN = 32-Pin Thin Small Outline Package (TSOP) Standard Pinout
PFTR = 32-Pin Thin Small Outline Package (TSOP) Reverse Pinout

SPEED OPTION
See Product Selector Guide

DEVICE NUMBER/DESCRIPTION
MBM29F040A
4Mega-bit (512K × 8-Bit) CMOS Flash Memory
5.0 V-only Read, Write, and Erase
64K Byte Sectors

Read Mode

The MBM29F040A has two control functions which must be satisfied in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for a device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable for at least t_{ACC}-t_{OE} time).

Standby Mode

The MBM29F040A has two standby modes, a CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.3$ V.), when the current consumed is less than 100 μA; and a TTL standby mode ($\overline{CE}$ is held at V_{IH}.) when the current required is reduced to approximately 1 mA. In the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure or programming, the device will draw active current until the operation is completed.

Output Disable

With the $\overline{OE}$ input at a logic high level (V_{IH}), output from the device is disabled. This will cause the output pins to be in a high impedance state.

Autoselect

The autoselect mode allows the reading out of a binary code from the device and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 12.5 V) on address pin A_9. Two identifier bytes may then be sequenced from the device outputs by toggling address A_0 from V_{IL} to V_{IH}. All addresses are DON'T CARES except A_0, A_1, and A_6.

The manufacturer and device codes may also be read via the command register, for instances when the MBM29F040A is erased or programmed in a system without access to high voltage on the A_9 pin. The command sequence is illustrated in Table 5. (Refer to Autoselect Command section.)

Table 3 MBM29F040A Sector Protection Verify Autoselect Codes

Type	A_{18}	A_{17}	A_{16}	A_6	A_1	A_0	Code (HEX)	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacture's Code	X	X	X	V_{IL}	V_{IL}	V_{IL}	04H	0	0	0	0	0	1	0	0
Device Code	X	X	X	V_{IL}	V_{IL}	V_{IH}	A4H	1	0	1	0	0	1	0	0
Sector Protection	Sector Addresses			V_{IL}	V_{IH}	V_{IL}	01H*	0	0	0	0	0	0	0	1

*: Outputs 01H at protected sector addresses and 00H at unprotected sector addresses.

Table 4 Sector Address Tables

Sector Address	A_{18}	A_{17}	A_{16}	Address Range
SA0	0	0	0	00000H to 0FFFFH
SA1	0	0	1	10000H to 1FFFFH
SA2	0	1	0	20000H to 2FFFFH
SA3	0	1	1	30000H to 3FFFFH
SA4	1	0	0	40000H to 4FFFFH
SA5	1	0	1	50000H to 5FFFFH
SA6	1	1	0	60000H to 6FFFFH
SA7	1	1	1	70000H to 7FFFFH

Byte 0 ($A_0 = V_{IL}$) represents the manufacture's code (Fujitsu = 04H) and byte 1 ($A_0 = V_{IH}$) the device identifier code (MBM29F040A = A4H). These two bytes are given in the Table 3. All identifiers for manufactures and device will exhibit odd parity with the MSB (DQ_7) defined as the parity bit. In order to read the proper device codes when executing the autoselect, A_1 must be V_{IL}. (See Table 3.)

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later; while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Sector Protection

The MBM29F040A features hardware sector protection. This feature will disable both program and erase operations in any number of sectors (0 through 8). The sector protection feature is enabled using programming equipment at the user's site. The device is shipped with all sectors unprotected.

To activate this mode, the programming equipment must force V_{ID} on address pin A_9 and control pin $\overline{OE}$, (suggest V_{ID} = 11.5 V) and $\overline{CE}$ = V_{IL}. The sector addresses (A_{18}, A_{17} and A_{16}) should be set to the sector to be protected. Table 4 defines the sector address for each of the eight (8) individual sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector addresses must be held constant during the $\overline{WE}$ pulse. Refer to figures 10 and 15 sector protection waveforms and algorithm.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on address pin A_9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. Scanning the sector addresses (A_{16}, A_{17}, and A_{18}) while (A_6, A_1, A_0) = (0, 1, 0) will produce a logical "1" code at device output DQ_0 for a protected sector. Otherwise the device will produce 00H for unprotected sector. In this mode, the lower order addresses, except for A_0, A_1, and A_6 are

DON'T CARES. Address locations with $A_1 = V_{IL}$ are reserved for Autoselect manufacturer and device codes.

It is also possible to determine if a sector is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02H, where the higher order addresses (A_{16}, A_{17}, and A_{18}) are the sector address will produce a logical "1" at DQ_0 for a protected sector. See Table 3 for Autoselect codes.

Table 5 MBM29F040A Command Definitions

Command Sequence Read/Reset	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset*	1	XXXXH	F0H	—	—	—	—	—	—	—	—	—	—
Read/Reset*	3	5555H	AAH	2AAAH	55H	5555H	F0H	RA	RD	—	—	—	—
Autoselect	3	5555H	AAH	2AAAH	55H	5555H	90H	—	—	—	—	—	—
Byte Program	4	5555H	AAH	2AAAH	55H	5555H	A0H	PA	PD	—	—	—	—
Chip Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H
Sector Erase Suspend	Erase can be suspended during sector erase with Addr (H or L). Data (B0H)												
Sector Erase Resume	Erase can be resumed after suspend with Addr (H or L). Data (30H)												

Notes: 1. Address bits A_0 to A_{15} = X = H or L for all address commands except for Program Address (PA) and Sector Address (SA).
2. Bus operations are defined in Table 2.
3. RA = Address of the memory location to be read.
PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
SA = Address of the sector to be erased. The combination of A_{18}, A_{17}, and A_{16} will uniquely select any sector.
4. RD = Data read from location RA during read operation.
PD = Data to be programmed at location PA. Data is latched on the falling edge of $\overline{WE}$.
*: Either of the two reset commands will reset the device.

Command Definitions

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to read mode. Table 5 defines the valid register command sequences. Note that the Erase Suspend (B_0) and Erase Resume (30) commands are valid only while the Sector Erase operation is in progress.

Read/Reset Command

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage (V_{ID} = 11.5 V to 12.5 V). However, multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains an autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the autoselect command sequence into the command register. Following the command write, a read cycle from address XX00H retrieves the manufacture code of 04H. A read cycle from address XX01H returns the device code A4H. (See Table 3.) All manufacturer and device codes will exhibit odd parity with the MSB (DQ_7) defined as the parity bit.
Sector state (protection or unprotection) will be informed address XX02H.
Scanning the sector addresses (A_{16}, A_{17}, A_{18}) while (A_6, A_1, A_0) = (0, 1, 0) will produce a logical "1" at device output DQ_0 for a protected sector.
To terminate the operation, it is necessary to write the read/reset command sequence into the register.

Byte Programming

The device is programmed on a byte-by-byte basis. Programming is a four bus cycle operation. There are two "unlock" write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) begins programming. Upon executing the Embedded Program Algorithm command sequence the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The automatic programming operation is completed when the data on DQ_7 is equivalent to data written to this bit (See Write Operation Status section.) at which time the device returns to the read mode and addresses are no longer latched. Therefore, the device requires that a valid address to the device be supplied by the system at this particular instance of time. Hence, $\overline{\text{Data}}$ Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during this period will be ignored.

Programming is allowed in any sequence and across sector boundaries. Beware that a data "0" cannot be programmed back to a "1". Attempting to do so will probably hang up the device (Exceed timing limits.), or perhaps result in an apparent success according to the data polling algorithm but a read from reset/read mode will show that the data is still "0". Only erase operations can convert "0"s to "1"s.

Figure 11 illustrates the Embedded Programming Algorithm using typical command strings and bus operations.

Chip Erase

Chip erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the chip erase command.

Chip erase does not require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the device automatically will program and verify the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when the data on DQ_7 is "1" (See Write Operation Status section.) at which time the device returns to read the mode.

Figure 12 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

Sector Erase

Sector erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the sector erase command. The sector address (Any address location within the desired sector.) is latched on the falling edge of $\overline{WE}$, while the command (Data=30H) is latched on the rising edge of $\overline{WE}$. A time-out of 50 µs from the rising edge of the last sector erase command will initiate the sector erase command(s).

Multiple sectors may be erased concurrently by writing the six bus cycle operations as described above. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than 50 µs, otherwise that command will not be accepted. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of 50 µs from the rising edge of the last $\overline{WE}$ will initiate the execution of the Sector Erase command(s). If another falling edge of the $\overline{WE}$ occurs within the 50 µs time-out window the timer is reset. (Monitor DQ_3 to determine if the sector erase timer window is still open, see section DQ_3, Sector Erase Timer.) Any command other than Sector Erase or Erase Suspend during this time-out period will reset the device to read mode, ignoring the previous command string. Resetting the device after it has begun execution will result in the data of the operated sectors being undefined (messed up). In that case, restart the erase on those sectors and allow them to complete. (Refer to the Write Operation Status section for Sector Erase Timer operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 7).

Sector erase does not require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations.

The automatic sector erase begins after the 50 µs time out from the rising edge of the $\overline{WE}$ pulse for the last sector erase command pulse and terminates when the data on DQ_7 is "1" (See Write Operation Status section.) at which time the device returns to the read mode. During the execution of the Sector Erase command, only the Erase Suspend and Erase Resume commands are allowed. All other commands will reset the device to read mode. $\overline{Data}$ polling must be performed at an address within any of the sectors being erased.

Figure 12 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

Erase Suspend

The Erase Suspend command allows the user to interrupt the chip and then do data reads (not program) from a non-busy sector while it is in the middle of a Sector Erase operation (which may take up to several seconds). This command is applicable ONLY during the Sector Erase operation and will be ignored if written during the chip Erase or Programming operation. The Erase Suspend command (B_0) will be allowed only during the Sector Erase Operation that will include the sector erase time-out period after the Sector Erase commands (30). Writing this command during the time-out will result in immediate termination of the time-out period. Any subsequent writes of the Sector Erase command will be taken as the Erase Resume command. Note that any other commands during the time out will reset the device to read mode. The addresses are DON' T CARES in writing the Erase Suspend or Erase Resume commands.

When the Erase Suspend command is written during a Sector Erase operation, the chip will take between 0.1 µs to 10 µs to suspend the erase operation and go into erase suspended read mode (pseudo-read mode), during which the user can read from a sector that is NOT being erased. A read from a sector being erased may result in invalid data. The user must monitor the toggle bit to determine if the chip has entered the pseudo-read mode, at which time the toggle bit stops toggling. An address of a sector NOT being erased must be used to read the toggle bit, otherwise the user may encounter intermittent problems. Note that the user must keep track of what state the chip is in since there is no external indication of whether the chip is in pseudo-read mode or actual read mode. After the user writes the Erase Suspend command and waits until the toggle bit stops toggling, data reads from the device may then be performed. Any further writes of the Erase Suspend command at this time will be ignored.

Every time an Erase Suspend command followed by an Erase Resume command is written, the internal (pulse) counters are reset. These counters are used to count the number of high voltage pulses the memory cell requires to program or erase. If the count exceeds a certain limit, then the DQ_5 bit will be set (Exceeded Time Limit flag). This resetting of the counters is necessary since the Erase Suspend command can potentially interrupt or disrupt the high voltage pulses.

To resume the operation of Sector Erase, the Resume command (30) should be written. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed.

Write Operation Status

Table 6 Hardware Sequence Flags

Status		DQ_7	DQ_6	DQ_5	DQ_3	DQ_2 to DQ_0
In progress	Auto-programming	$\overline{DQ_7}$	Toggle	0	0	$\overline{(D)}$
	Program/Erase in Auto Erase	0	Toggle	0	1	
Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	1	0	0	
	Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	
Exceeded Time Limits	Auto-Programming	$\overline{DQ_7}$	Toggle	1	0	
	Program/Erase in Auto-Erase	0	Toggle	1	1	

Note: DQ_0, DQ_1 and DQ_2 are reserve pins for future use. DQ_4 is for Fujitsu internal use only.

DQ_7

$\overline{\text{Data}}$ Polling

The MBM29F040A device features $\overline{\text{Data}}$ Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm an attempt to read the device will produce the compliment of the data last written to DQ_7. Upon completion of the Embedded Program

Algorithm, an attempt to read the device will produce the true data last written to DQ_7. During the Embedded Erase Algorithm, an attempt to read the device will produce a “0” at the DQ_7 output. Upon completion of the Embedded Erase Algorithm an attempt to read the device will produce a “1” at the DQ_7 output. The flowchart for $\overline{\text{Data}}$ Polling (DQ_7) is shown in Figure 13.

For chip erase, and sector erase the $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six write pulse sequence. For sector erase, the $\overline{\text{Data}}$ Polling is valid after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse. $\overline{\text{Data}}$ Polling must be performed at sector address within any of the sectors being erased and not a protected sector. Otherwise, the status may not be valid. Once the Embedded Algorithm operation is close to being completed, the MBM29F040A data pins (DQ_7) may change asynchronously while the output enable ($\overline{\text{OE}}$) is asserted low. This means that the device is driving status information on DQ_7 at one instant of time and then that byte's valid data at the next instant of time. Depending on when the system samples the DQ_7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operation and DQ_7 has a valid data, the data outputs on DQ_0 to DQ_6 may be still invalid. The valid data on DQ_0 to DQ_7 will be read on the successive read attempts.

The $\overline{\text{Data}}$ Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, or sector erase time-out (see Table 6).

See Figure 8 for the $\overline{\text{Data}}$ Polling timing specifications and diagrams.

DQ_6

Toggle Bit

The MBM29F040A also features the “Toggle Bit” as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{\text{OE}}$ toggling) data from the device will result in DQ_6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ_6 will stop toggling and valid data will be read on the next successive attempts. During programming, the Toggle Bit is valid after the rising edge of the fourth $\overline{\text{WE}}$ pulse in the four write pulse sequence. For chip erase and sector erase, the Toggle Bit is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six write pulse sequence. For Sector erase, the Toggle Bit is valid after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse. The Toggle Bit is active during the sector time out.

In programming, if the sector being written to is protected, the toggle bit will toggle for about 2 µs and then stop toggling without the data having changed. In erase, the device will erase all the selected sectors except for the ones that are protected. If all selected sectors are protected, the chip will toggle the toggle bit for about 100 µs and then drop back into read mode, having changed none of the data.

Either $\overline{\text{CE}}$ or $\overline{\text{OE}}$ toggling will cause the DQ_6 to toggle. In addition, an Erase Suspend/Resume command will cause DQ_6 to toggle. (See Figure 9 for the Toggle Bit timing specifications and diagrams.)

DQ_5

Exceeded Timing Limits

DQ_5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ_5 will produce a “1”. This is a failure condition which indicates that the program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling is the only operating function of the device under this condition. The $\overline{\text{CE}}$ circuit will partially power down the device under these conditions (to approximately 2 mA). The $\overline{\text{OE}}$ and $\overline{\text{WE}}$ pins will control the output disable functions as described in Table 2.

If this failure condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused, however, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this failure condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this failure condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector may not be reused, (other sectors are still functional and can be reused).

The DQ_5 failure condition may also appear if a user tries to program a non blank location without erasing. In this case the device locks out and never completes the Embedded Algorithm operation. Hence, the system never reads a valid data on DQ_7 bit and DQ_6 never stops toggling. Once the device has exceeded timing limits, the DQ_5 bit will indicate a "1." Please note that this is not a device failure condition since the device was incorrectly used.

DQ_3

Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. DQ_3 will remain low until the time-out is complete. $\overline{\text{Data}}$ Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{\text{Data}}$ Polling or the Toggle Bit indicates the device has been written with a valid erase command. DQ_3 may be used to determine if the sector erase timer window is still open. If DQ_3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by $\overline{\text{Data}}$ Polling or Toggle Bit. If DQ_3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ_3 prior to and following each subsequent sector erase command. If DQ_3 were high on the second status check, the command may not have been accepted.

Refer to Table 6: Hardware Sequence Flags.

Data Protection

The MBM29F040A is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting form V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.2 V (typically 3.7 V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on $\overline{\text{OE}}$, $\overline{\text{CE}}$, or $\overline{\text{WE}}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{\text{OE}}$ = V_{IL}, $\overline{\text{CE}}$ = V_{IH}, or $\overline{\text{WE}}$ = V_{IH}. To initiate a write cycle $\overline{\text{CE}}$ and

$\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

■ ABSOLUTE MAXIMUM RATINGS

Storage Temperature ....–45 °C to +125 °C
Ambient Temperature with Power Applied ....–25 °C to +85 °C
Voltage with Respect to Ground All pins except A_9, $\overline{OE}$ (Note 1) ....–2.0 V to +7.0 V
V_{CC} (Note 1) ....–2.0 V to +7.0 V
A_9, $\overline{OE}$ (Note 2) ....–2.0 V to +13.5 V

Notes: 1. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may negative overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} +0.5 V. During voltage transitions, outputs may positive overshoot to V_{CC} +2.0 V for periods of up to 20 ns.

2. Minimum DC input voltage on A_9 and $\overline{OE}$ pins are –0.5 V. During voltage transitions, A_9 and $\overline{OE}$ pins may negative overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A_9 and $\overline{OE}$ pins are +13.5 V which may overshoot to 14.0 V for periods of up to 20 ns.

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

■ OPERATING RANGES

Commercial Devices
Ambient Temperature (T_A) ....0 °C to +70 °C
V_{CC} Supply Voltages
V_{CC} for MBM29F040A-70 ....+4.75 V to +5.25 V
V_{CC} for MBM29F040A-90/-12 ....+4.50 V to +5.50 V
Operating ranges define those limits between which the functionality of the device is guaranteed.

■ MAXIMUM OVERSHOOT

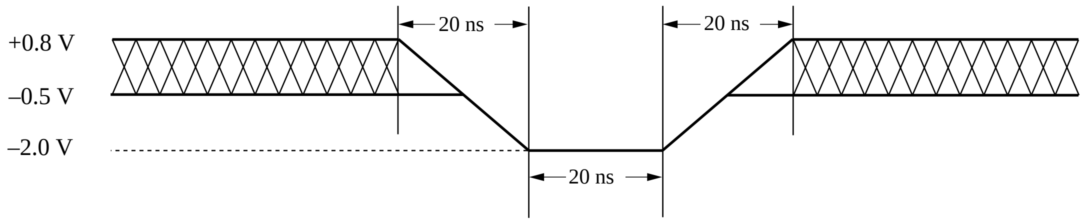


Figure 1 Maximum Negative Overshoot Waveform

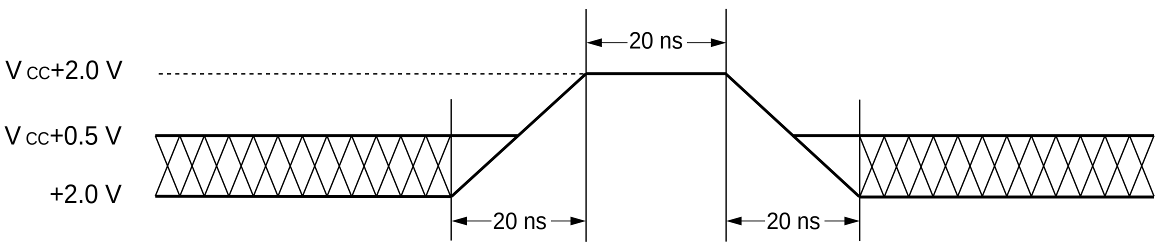
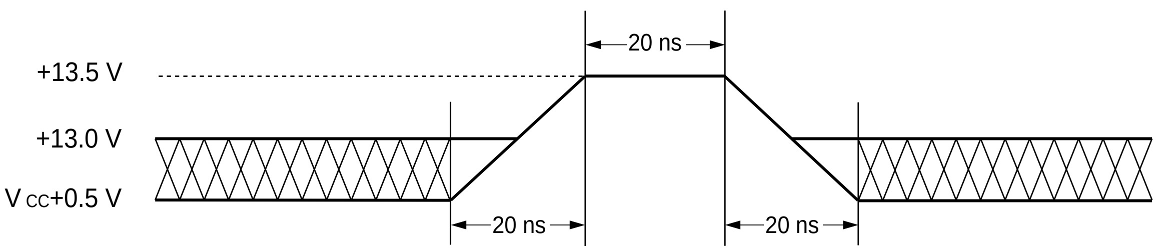


Figure 2 Maximum Positive Overshoot Waveform



*:This waveform is applied for A_9, $\overline{OE}$, and $\overline{RESET}$.

Figure 3 Maximum Positive Overshoot Waveform

■ DC CHARACTERISTICS

• **TTL/NMOS Compatible**

Parameter Symbol	Parameter Description	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max.	—	±1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max.	—	±1.0	µA
I_{LIT}	A_9, $\overline{OE}$ Inputs Leakage Current	$V_{CC} = V_{CC}$ Max., A_9, $\overline{OE}$ = 12.0 V	—	50	µA
I_{CC1}	V_{CC} Active Current (Note 1)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	—	40	mA
I_{CC2}	V_{CC} Active Current (Note 2)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	—	60	mA
I_{CC3}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max., $\overline{CE} = V_{IH}$	—	1.0	mA
V_{IL}	Input Low Level		–0.5	0.8	V
V_{IH}	Input High Level		2.0	V_{CC}+0.5	V
V_{ID}	Voltage for Autoselect and Sector Protection (A_9, $\overline{OE}$)	V_{CC} = 5.0 V	11.5	12.5	V
V_{OL}	Output Low Voltage Level	I_{OL} = 12 mA, $V_{CC} = V_{CC}$ Min.	—	0.45	V
V_{OH}	Output High Voltage Level	I_{OH} = –2.5 mA, $V_{CC} = V_{CC}$ Min.	2.4	—	V
V_{LKO}	Low V_{CC} Lock-Out Voltage		3.2	4.2	V

Notes: 1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz).
The frequency component typically is 2 mA/MHz, with $\overline{OE}$ at VIH.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.

• **CMOS Compatible**

Parameter Symbol	Parameter Description	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max.	—	±1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max.	—	±1.0	µA
I_{LIT}	A_9, $\overline{OE}$ Inputs Leakage Current	$V_{CC} = V_{CC}$ Max., A_9, $\overline{OE}$ = 12.0 V	—	50	µA
I_{CC1}	V_{CC} Active Current (Note 1)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	—	40	mA
I_{CC2}	V_{CC} Active Current (Note 2)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	—	60	mA
I_{CC3}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max., $\overline{CE} = V_{CC}±0.3$ V	—	100	µA
V_{IL}	Input Low Level		–0.5	0.8	V
V_{IH}	Input High Level		0.7×V_{CC}	V_{CC}+0.3	V
V_{ID}	Voltage for Autoselect and Sector Protection (A_9, $\overline{OE}$)	V_{CC} = 5.0 V	11.5	12.5	V
V_{OL}	Output Low Voltage Level	I_{OL} = 12.0 mA, $V_{CC} = V_{CC}$ Min.	—	0.45	V
V_{OH1}	Output High Voltage Level	I_{OH} = –2.5 mA, $V_{CC} = V_{CC}$ Min.	0.85×V_{CC}	—	V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC}$ Min.	V_{CC}–0.4	—	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2	4.2	V

Notes: 1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz).
The frequency component typically is 2 mA/MHz, with $\overline{OE}$ at V_{IH}.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.

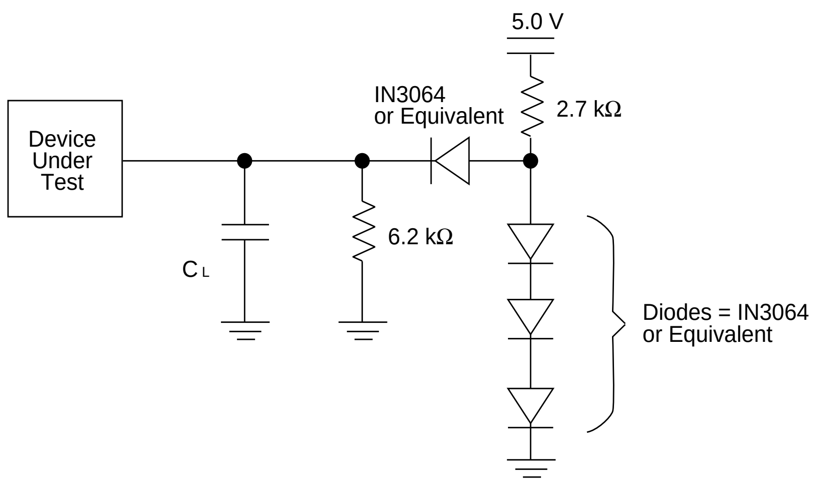
■ AC CHARACTERISTICS

• **Read Only Operations Characteristics**

Parameter Symbol JEDEC	Parameter Symbol Standard	Description	Test Setup		–70 (Note 1)	–90 (Note 2)	–12 (Note 2)	Unit
t_{AVAV}	t_{RC}	Read Cycle Time		Min.	70	90	120	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = V_{IL} $\overline{OE}$ = V_{IL}	Max.	70	90	120	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Max.	70	90	120	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay		Max.	30	35	50	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High-Z		Max.	20	20	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High-Z		Max.	20	20	30	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First		Min.	0	0	0	ns

Notes: 1. Test Conditions:
Output Load: 1 TTL gate and 30 pF
Input rise and fall times: 5 ns
Input pulse levels: 0.0 V to 3.0 V
Timing measurement reference level
Input: 1.5 V
Output: 1.5 V

2. Test Conditions:
Output Load: 1 TTL gate and 100 pF
Input rise and fall times: 20 ns
Input pulse levels: 0.45 V to 2.4 V
Timing measurement reference level
Input: 0.8 V and 2.0 V
Output: 0.8 V and 2.0 V



Note: For –70: C_L = 30 pF including jig capacitance
For all others: C_L = 100 pF including jig capacitance

Figure 4 Test Conditions

• **Write/Erase/Program Operations**
Alternate $\overline{WE}$ Controlled Writes

Parameter Symbol JEDEC	Parameter Symbol Standard	Description			–70	–90	–12	Unit
t_{AVAV}	t_{WC}	Write Cycle Time		Min.	70	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min.	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time		Min.	45	45	50	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min.	30	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min.	0	0	0	ns
—	t_{OES}	Output Enable Setup Time		Min.	0	0	0	ns
—	t_{OEH}	Output Enable Hold Time	Read	Min.	0	0	0	ns
			Toggle and $\overline{Data}$ Polling	Min.	10	10	10	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write		Min.	0	0	0	ns
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup Time		Min.	0	0	0	ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time		Min.	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min.	35	45	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min.	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation		Typ.	16	16	16	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 1)		Typ.	1.5	1.5	1.5	sec
				Max.	30	30	30	sec
—	t_{VCS}	V_{CC} Setup Time		Min.	50	50	50	µs
—	t_{VLHT}	Voltage Transition Time (Note 2)		Min.	4	4	4	µs
—	t_{WPP}	Write Pulse Width (Note 2)		Min.	100	100	100	µs
—	t_{OESP}	$\overline{OE}$ Setup Time to $\overline{WE}$ Active (Note 2)		Min.	4	4	4	µs
—	t_{CSP}	$\overline{CE}$ Setup Time to $\overline{WE}$ Active (Note 2)		Min.	4	4	4	µs

Notes: 1. This does not include the preprogramming time.
2. This timing is for Sector Protection operation.

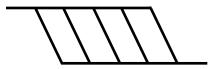
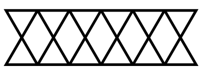
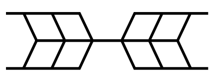
- **Write/Erase/Program Operations**
  Alternate $\overline{CE}$ Controlled Writes

Parameter Symbol		Description		–70	–90	–12	Unit
JEDEC	Standard						
t_{AVAV}	t_{WC}	Write Cycle Time	Min.	70	90	120	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min.	0	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time	Min.	45	45	50	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min.	30	45	50	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min.	0	0	0	ns
—	t_{OES}	Output Enable Setup Time	Min.	0	0	0	ns
—	t_{OEH}	Output Enable Hold Time: Read	Min.	0	0	0	ns
		Output Enable Hold Time: Toggle and $\overline{Data}$ Polling	Min.	10	10	10	ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write	Min.	0	0	0	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time	Min.	0	0	0	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time	Min.	0	0	0	ns
t_{ELEH}	t_{CP}	$\overline{CE}$ Pulse Width	Min.	35	45	50	ns
t_{EHEL}	t_{CPH}	$\overline{CE}$ Pulse Width High	Min.	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation	Typ.	16	16	16	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note)	Typ.	1.5	1.5	1.5	sec
			Max.	30	30	30	sec
—	t_{VCS}	V_{CC} Setup Time	Min.	50	50	50	µs

Note: This does not include the preprogramming time.

■ SWITCHING WAVEFORMS

• Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	H or L: Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High-Impedance “Off” State

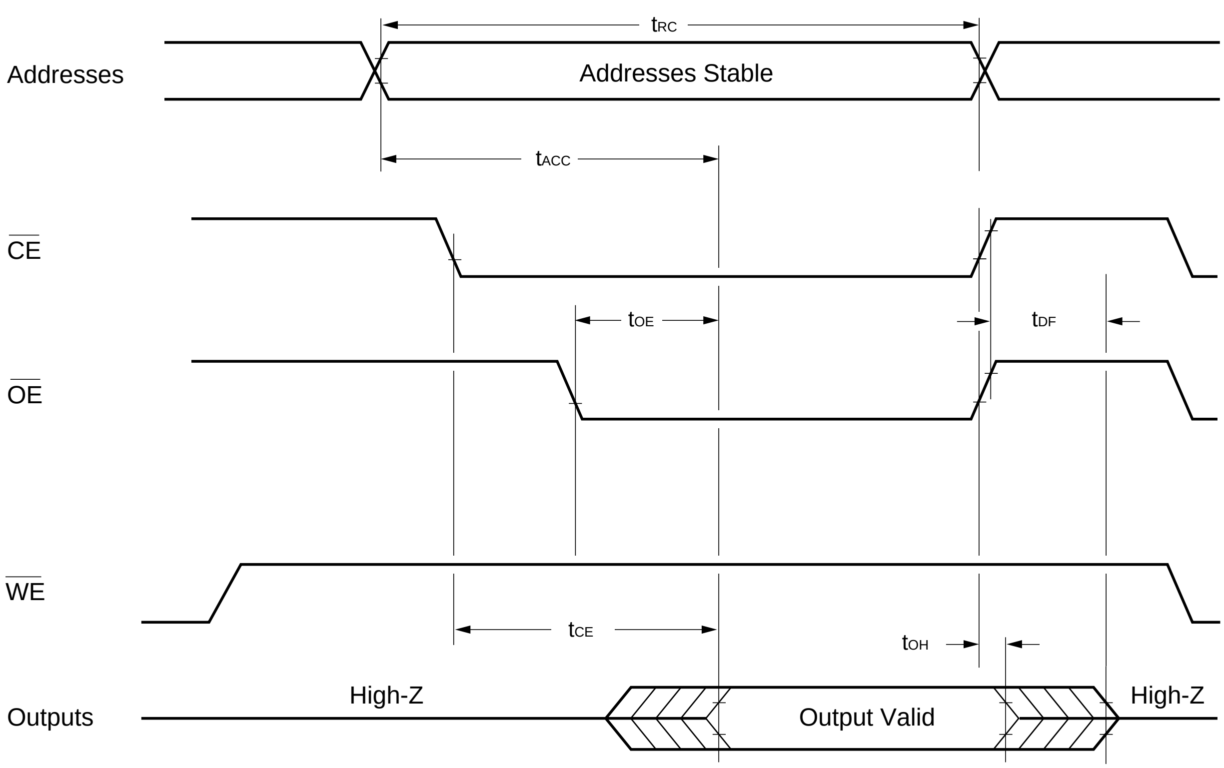
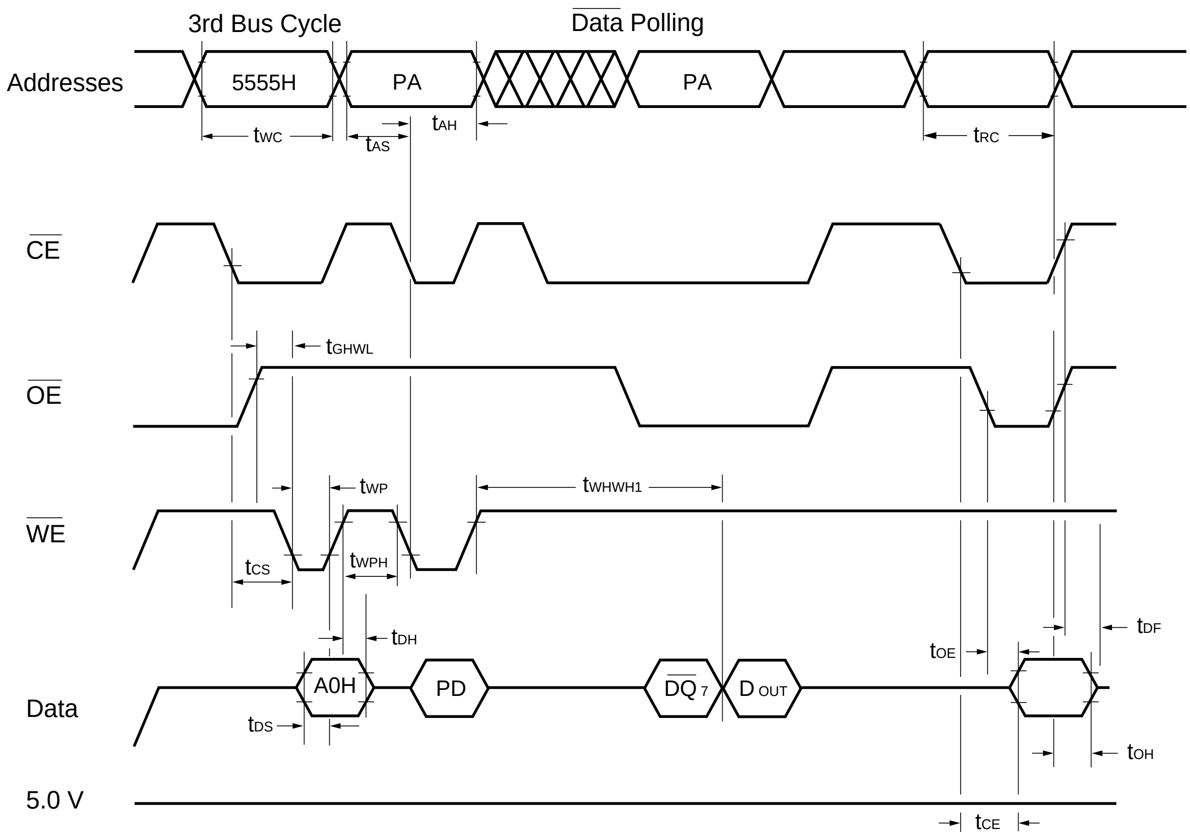
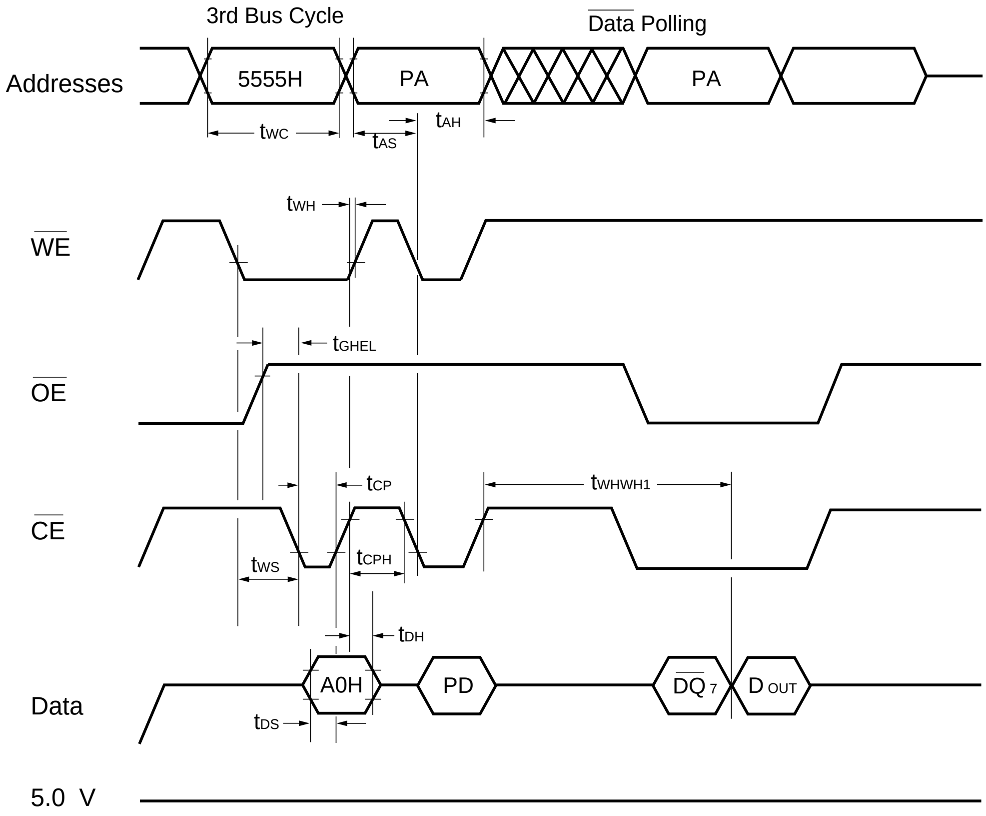


Figure 5 AC Waveforms for Read Operations



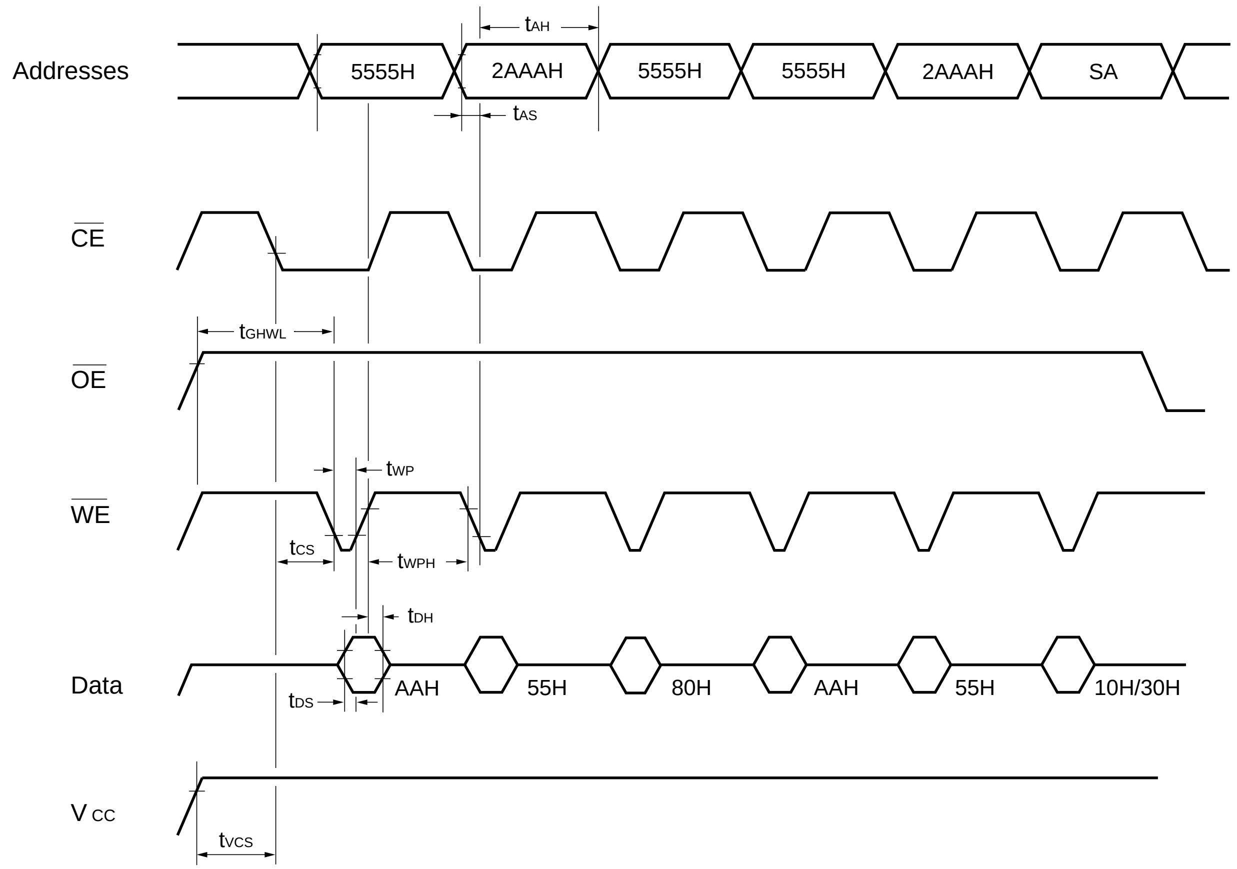
Notes: 1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. $\overline{DQ_7}$ is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

Figure 6 Alternate $\overline{\text{WE}}$ Controlled Program Operation Timings



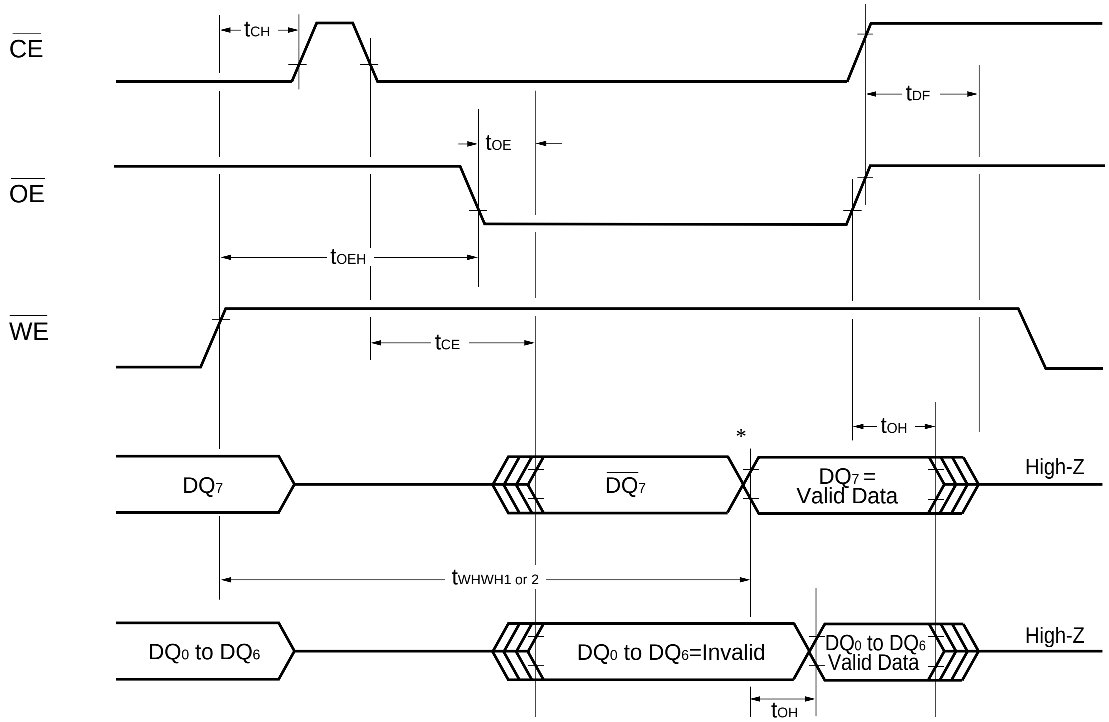
Notes: 1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. $\overline{DQ_7}$ is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

Figure 7 Alternate $\overline{CE}$ Controlled Program Operation Timings



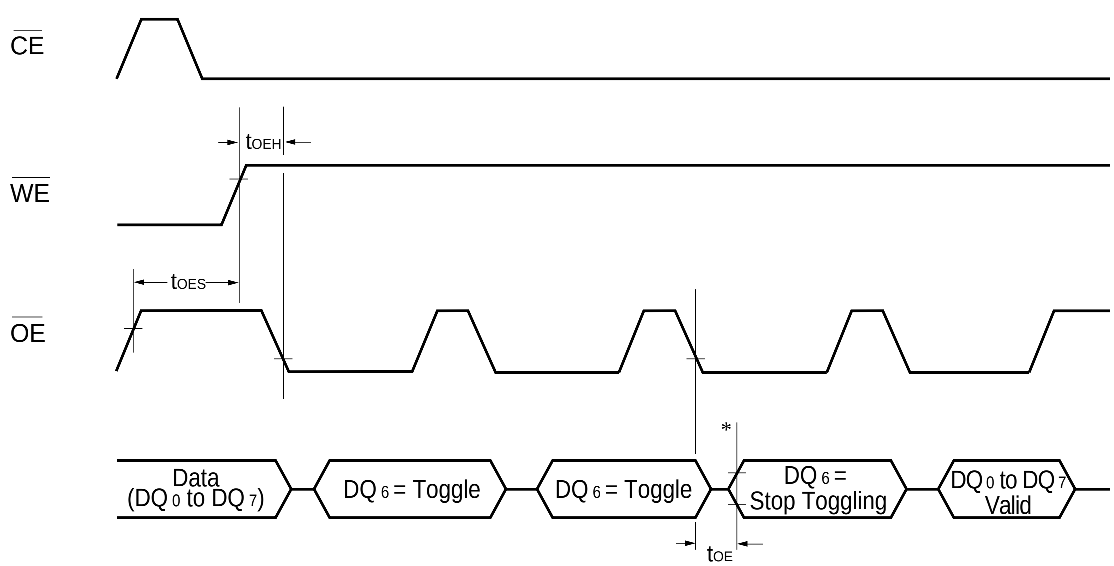
Note: SA is the sector address for Sector Erase. Addresses = 5555H for Chip Erase

Figure 8 AC Waveforms Chip/Sector Erase Operations



*: DQ_7 = Valid Data (The device has completed the Embedded operation).

Figure 9 AC Waveforms for Data Polling during Embedded Algorithm Operations



*: DQ_6 stops toggling (The device has completed the Embedded operation).

Figure 10 AC Waveforms for Toggle Bit during Embedded Algorithm Operations

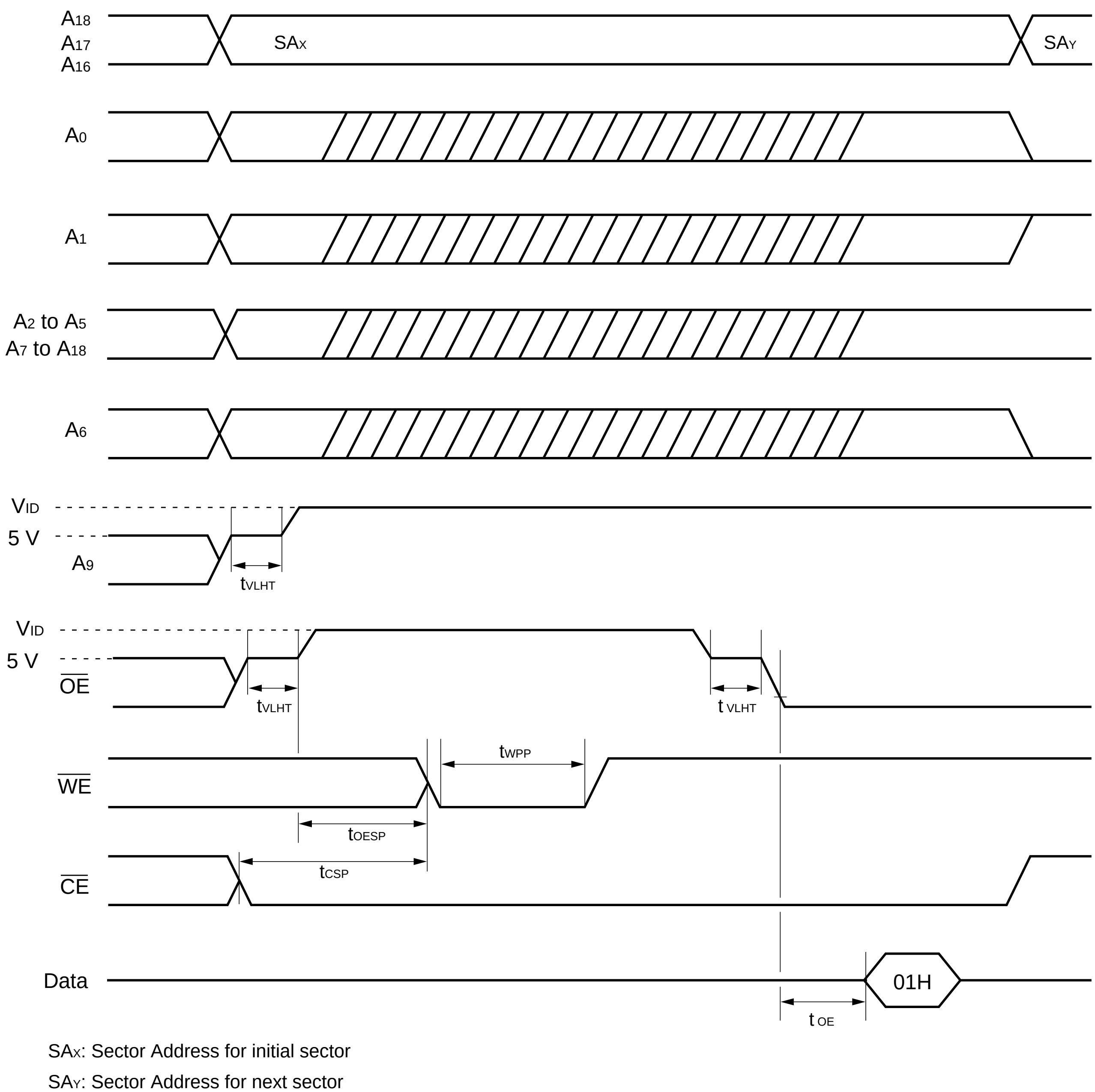


Figure 11 AC Waveforms for Sector Protection

EMBEDDED ALGORITHMS

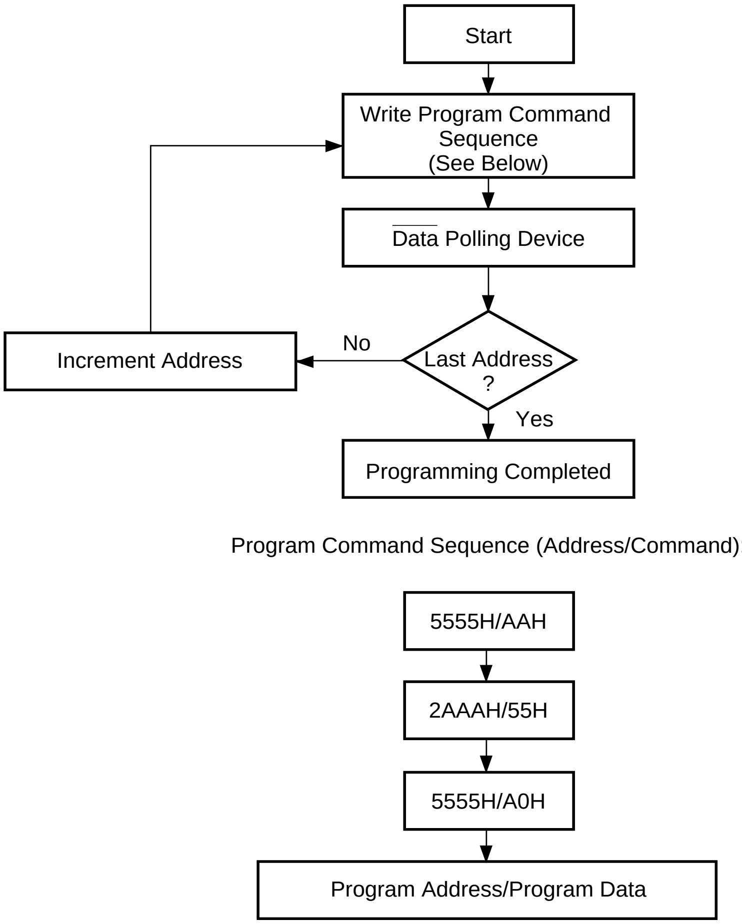


Figure 12 Embedded Programming Algorithm

Table 7 Embedded Programming Algorithm

Bus Operation	Command Sequence	Comment
Standby*		
Write	Program	Valid Address/Data Sequence
Read		$\overline{\text{Data}}$ Polling to Verify Programming
Standby*		Compare Data Output to Data Expected

*: Device is either powered-down, erase inhibit or program inhibit.

EMBEDDED ALGORITHMS

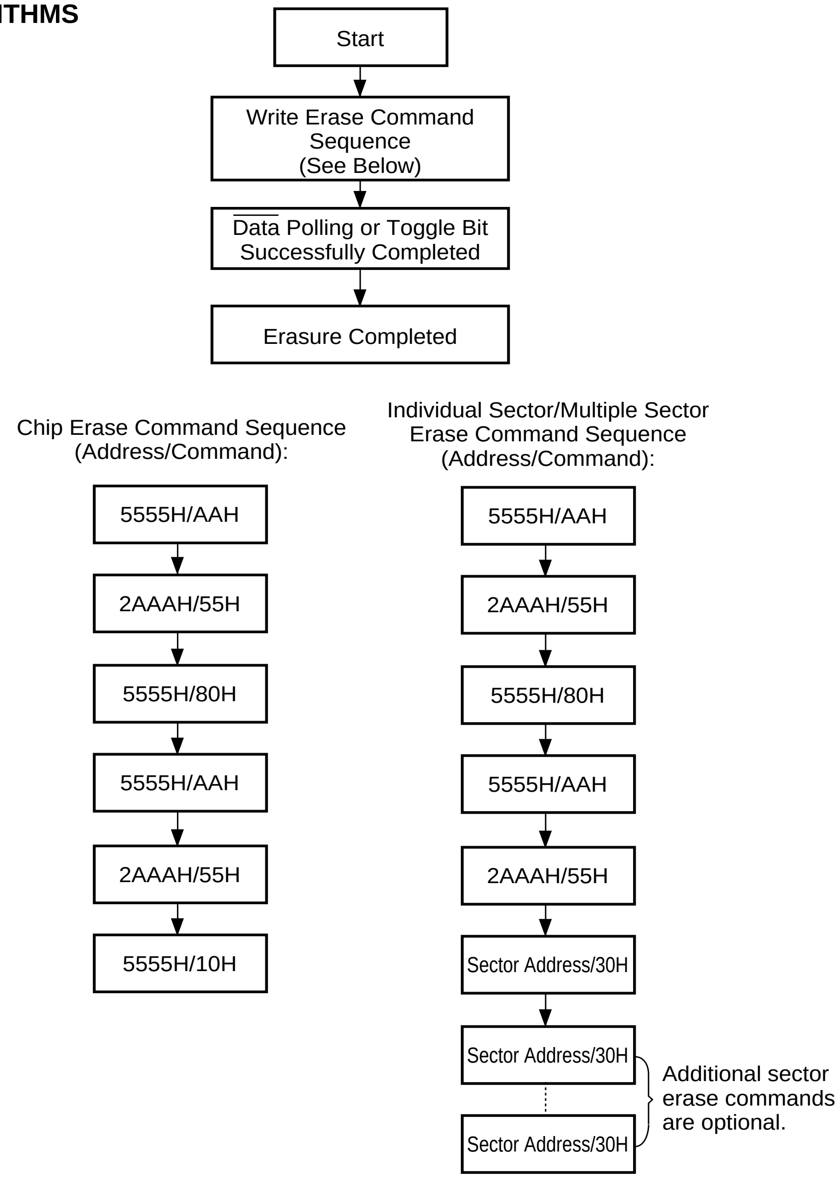
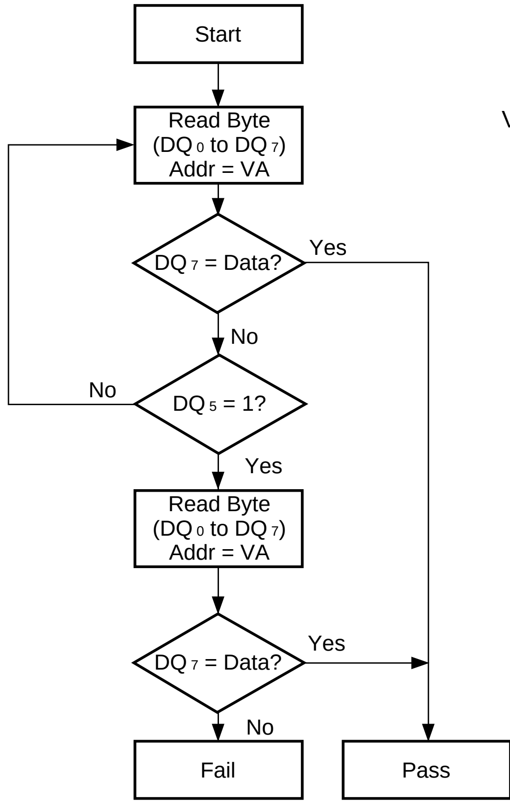


Figure 13 Embedded Erase Algorithm

Table 8 Embedded Erase Algorithm

Bus Operation	Command Sequence	Comment
Standby*		
Write	Erase	
Read		Data Polling to Verify Erasure
Standby*		Compare Output to FFH

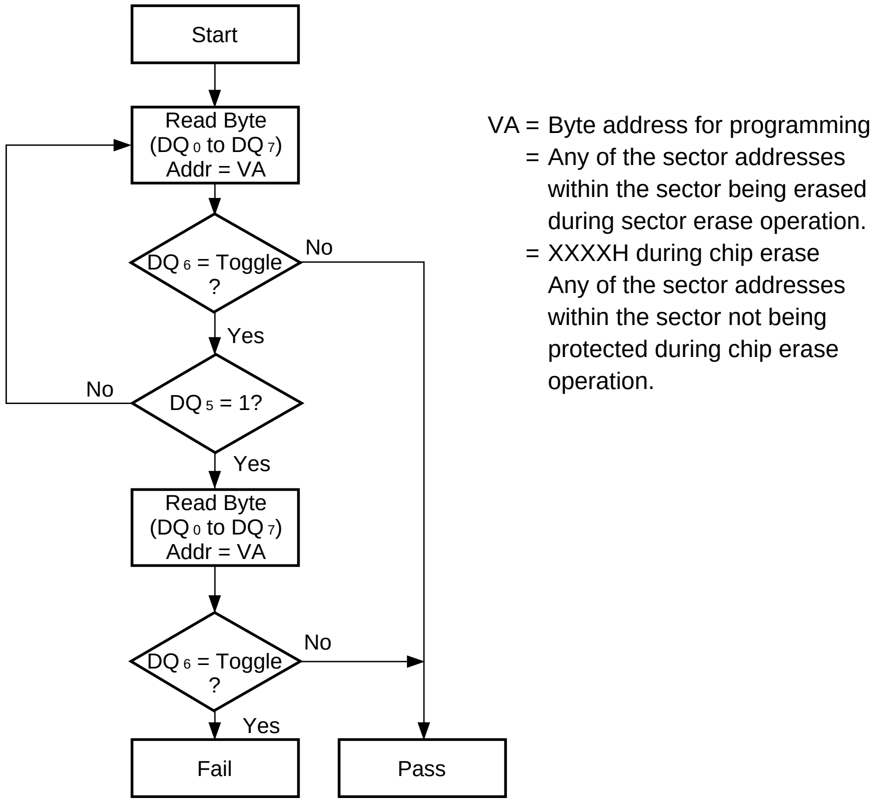
*: Device is either powered-down, erase inhibit or program inhibit.



VA = Byte address for programming
= Any of the sector addresses within the sector being erased during sector erase operation.
= Any of the sector addresses within the sector not being protected during chip erase operation.

Note: DQ_7 is rechecked even if DQ_5 = “1” because DQ_7 may change simultaneously with DQ_5.

Figure 14 Data Polling Algorithm



Note: DQ_6 is rechecked even if DQ_5 = "1" because DQ_6 may stop toggling at the same time as DQ_5 changing to "1" .

Figure 15 Toggle Bit Algorithm

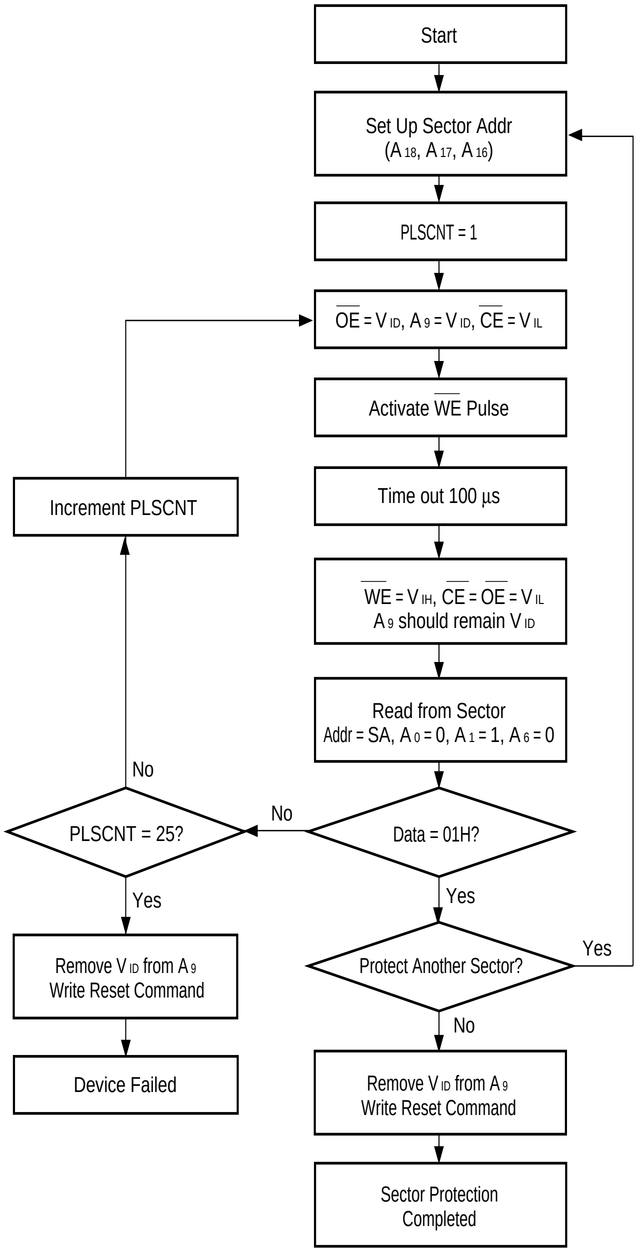


Figure 16 Sector Protection Algorithm

■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limit			Unit	Comment
	Min.	Typ.	Max.		
Sector Erase Time	—	1.5	30	sec	Excludes 00H programming prior to erasure
Byte Programming Time	—	16	1000	µs	Excludes system-level overhead
Chip Programming Time	—	8.5	50	sec	Excludes system-level overhead
Erase/Program Cycle	100,000	1,000,000	—	Cycles	

■ TSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	6	7.5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8.5	12	pF
C_{IN2}	Control Pin Capacitance	$V_{IN} = 0$	7.5	9	pF

Note: Test conditions $T_A = 25$ °C, f = 1.0 MHz

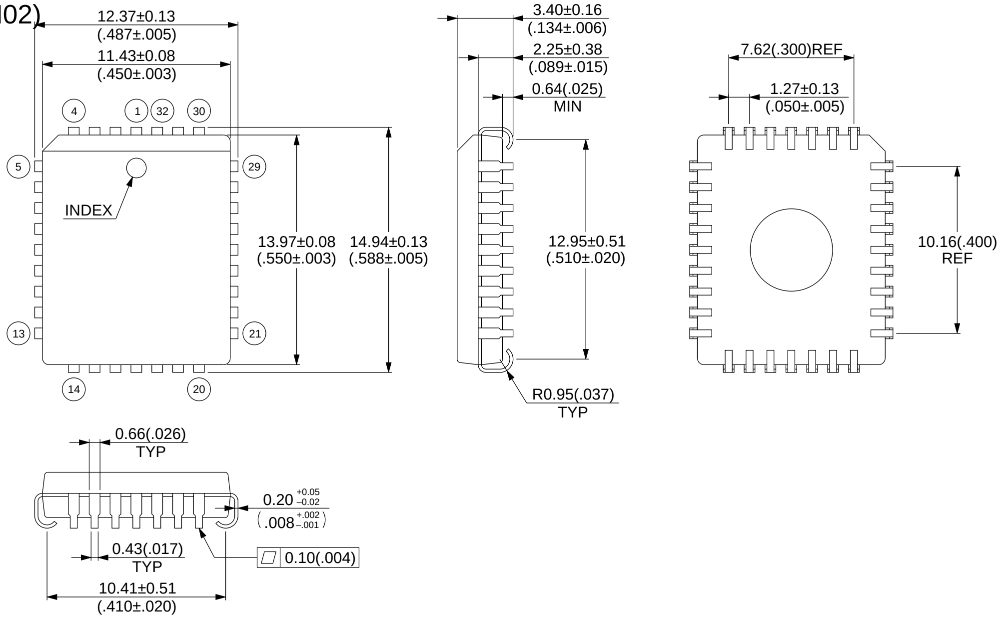
■ PLCC PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	12	pF
C_{IN2}	Control Pin Capacitance	$V_{IN} = 0$	8	12	pF

Note: Test conditions $T_A = 25$ °C, f = 1.0 MHz

■ PACKAGE DIMENSIONS

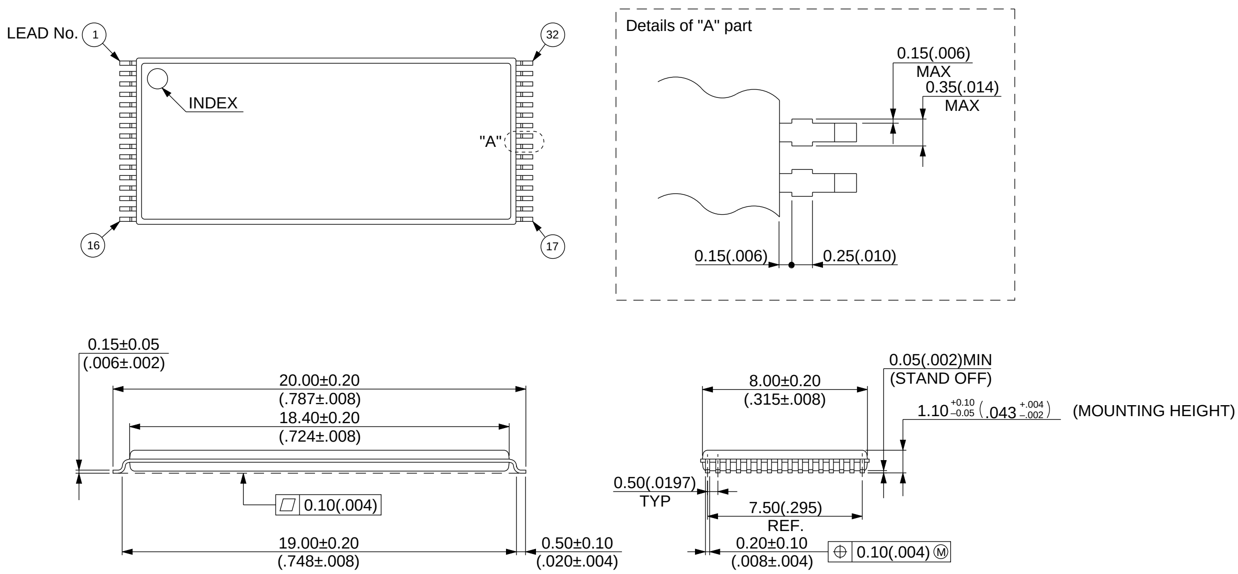
(Suffix: PD)
Plastic • LCC, 32 Pin
(LCC-32P-M02)



Dimensions in mm (inches)

(Suffix: PFTN – Assembly: Malaysia)
Plastic • TSOP, 32 Pin
(FPT-32P-M24)

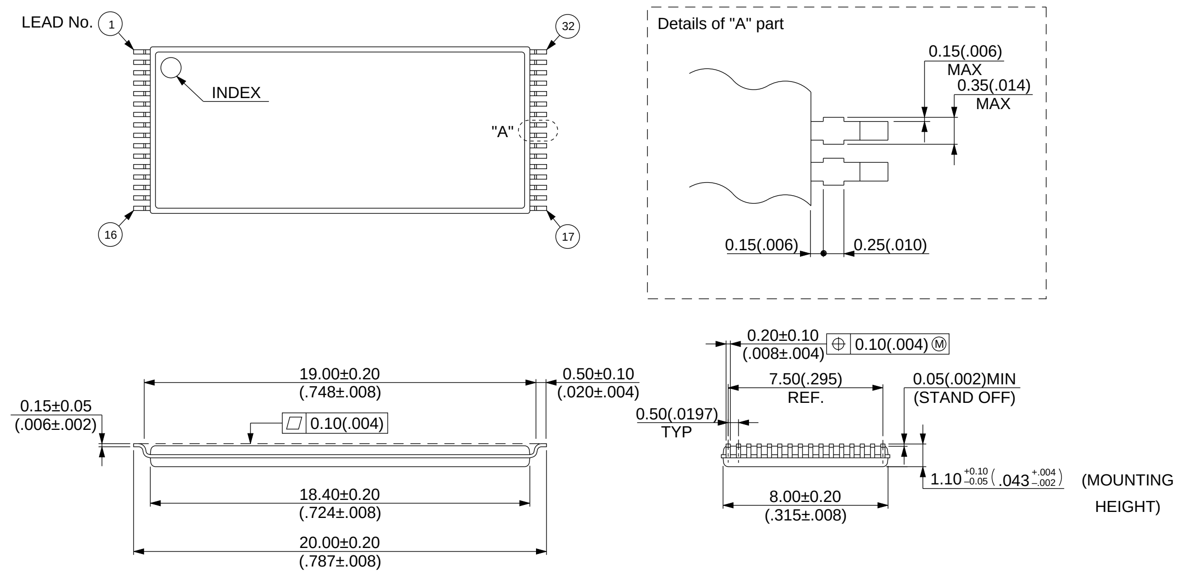
*Resin protrusion • Each side 0.15 (.006) MAX.



Dimensions in mm (inches)

*Resin protrusion • Each side 0.15 (.006) MAX.

(Suffix: PFTR – Assembly: Malaysia)
Plastic • TSOP, 32 Pin
(FPT-32P-M25)



Dimensions in mm (inches)

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