

# Differential Data and Clock D Flip-Flop

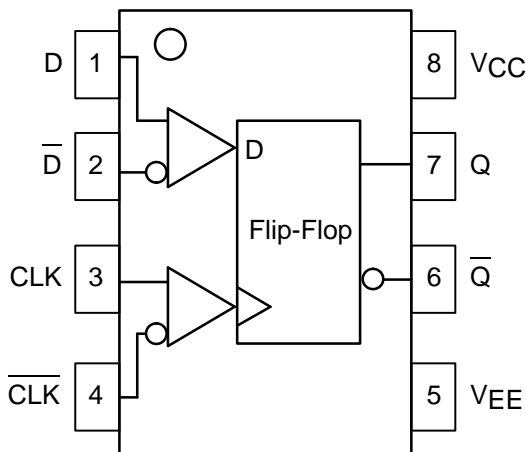
The MC10EL/100EL52 is a differential data, differential clock D flip-flop with reset. The device is functionally equivalent to the E452 device with higher performance capabilities. With propagation delays and output transition times significantly faster than the E452 the EL52 is ideally suited for those applications which require the ultimate in AC performance.

Data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The differential clock inputs of the EL52 allow the device to also be used as a negative edge triggered device.

The EL52 employs input clamping circuitry so that under open input conditions (pulled down to V<sub>EE</sub>) the outputs of the device will remain stable.

- 365ps Propagation Delay
- 2.0GHz Toggle Frequency
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection

## LOGIC DIAGRAM AND PINOUT ASSIGNMENT



# MC10EL52 MC100EL52



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-05

## PIN DESCRIPTION

PIN	FUNCTION
D	Data Input
CLK	Clock Input
Q	Data Output

## TRUTH TABLE

D	CLK	Q
L	Z	L
H	Z	H

Z = LOW to HIGH Transition



# MC10EL52 MC100EL52

## DC CHARACTERISTICS ( $V_{EE} = V_{EE}(\text{min})$ to $V_{EE}(\text{max})$ ; $V_{CC} = \text{GND}$ )

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current 10EL 100EL		21 21	25 25		21 21	25 25		21 21	25 25		21 24	25 29	mA
$V_{EE}$	Power Supply Voltage 10EL 100EL	-4.94 -4.20	-5.2 -4.5	-5.5 -5.5	-4.94 -4.20	-5.2 -4.5	-5.5 -5.5	-4.75 -4.20	-5.2 -4.5	-5.5 -5.5	-4.75 -4.20	-5.2 -4.5	-5.5 -5.5	V
$I_{IH}$	Input HIGH Current			150			150			150			150	$\mu\text{A}$

## AC CHARACTERISTICS ( $V_{EE} = V_{EE}(\text{min})$ to $V_{EE}(\text{max})$ ; $V_{CC} = \text{GND}$ )

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\text{MAX}}$	Maximum Toggle Frequency	1.8	2.5		2.2	2.8		2.2	2.8		2.2	2.8		GHz
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay to Output CLK	225	335	515	275	365	465	275	365	465	320	410	510	ps
$t_{\text{S}}$	Setup Time	125	0		125	0		125	0		125	0		ps
$t_{\text{H}}$	Hold Time	150	50		150	50		150	50		150	50		ps
$t_{\text{PW}}$	Minimum Pulse Width	400			400			400			400			ps
$V_{\text{PP}}$	Minimum Input Swing <sup>1</sup>	150			150			150			150			mV
$V_{\text{CMR}}$	Common Mode Range <sup>2</sup> D (10EL) D (100EL) CLK (10EL) CLK (100EL)	-0.4 -0.4 -0.6 -0.8		-1.6 -1.2 See <sup>3</sup> See <sup>3</sup>	-0.4 -0.4 -0.6 -0.8		-1.6 -1.2 See <sup>3</sup> See <sup>3</sup>	-0.4 -0.4 -0.6 -0.8		-1.6 -1.2 See <sup>3</sup> See <sup>3</sup>	-0.4 -0.4 -0.6 -0.8		-1.6 -1.2 See <sup>3</sup> See <sup>3</sup>	V
$t_{\text{r}}$ $t_{\text{f}}$	Output Rise/Fall Times Q (20% – 80%)	100	225	350	100	225	350	100	225	350	100	225	350	ps

1. Minimum input swing for which AC parameters are guaranteed.
2. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{\text{ppmin}}$  and 1V.
3. The lower end of the CMR range is dependent on  $V_{\text{EE}}$  and is equal to  $V_{\text{EE}} + 2.5\text{V}$ .

OUTLINE DIMENSIONS

D SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751-05  
ISSUE P



NOTES:

1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. DIMENSIONS ARE IN MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
6. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	4.80	5.00
B	3.80	4.00
C	1.35	1.75
D	0.35	0.49
F	0.40	1.25
G	1.27 BSC	
J	0.18	0.25
K	0.10	0.25
M	0°	7°
P	5.80	6.20
R	0.25	0.50

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