

MOTOROLA

Specifications and Applications Information

SWITCHMODE REGULATOR CONTROL CIRCUIT

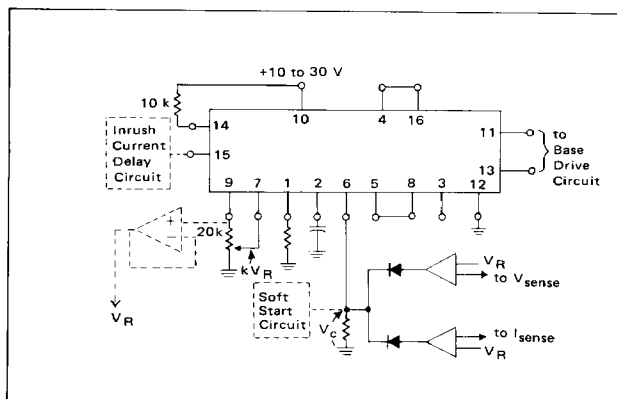
The MC3520/3420 is an inverter control unit which provides all the control circuitry for PWM push-pull, bridge and series type switchmode power supplies.

These devices are designed to supply the pulse width modulated drive to the bases of two external power transistors. Other applications where these devices can be used are in transformerless voltage doublers, transformer coupled dc-to-dc converters and other power control functions.

The MC3520 is specified over the military operating range of -55°C to $+125^{\circ}\text{C}$. The MC3420 is specified from 0°C to $+70^{\circ}\text{C}$.

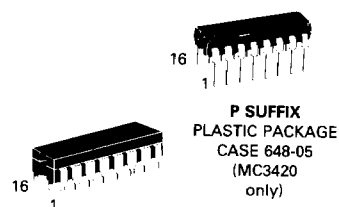
- Includes Symmetrical Oscillator
- On Chip Pulse Width Modulator, Voltage Reference, Dead Time Comparator, and Phase Splitter
- Output Frequency Adjustable (2.0 kHz to 100 kHz)
- Inhibit and Symmetry Correction Inputs Available
- Controlled Start-Up
- Frequency and Dead Time are Independently Adjustable (0% to 100%)
- Can be Slaved to Other MC3420s
- Open Collector Outputs
- Output Capability 50 mA (Max.)
- On Chip Protection Against Double Pulsing of Same Output During Load Transient Condition

FIGURE 1—TYPICAL APPLICATION

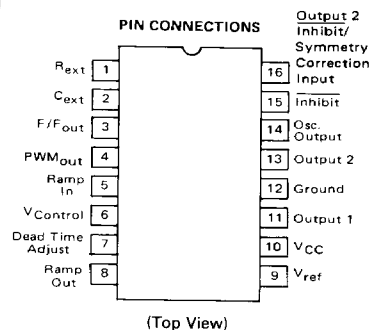


SWITCHMODE REGULATOR CONTROL CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUITS



L SUFFIX
CERAMIC PACKAGE
CASE 620-02



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE
MC3420P	0 to +70°C	Plastic DIP
MC3420L	0 to +70°C	Ceramic DIP
MC3520L	-55 to +125°C	Ceramic DIP

MAXIMUM RATINGS

Rating	Symbol	MC3520	MC3420	Unit
Power Supply Voltage	V_{CC}	30		V
Output Voltage (pins 11 and 13)	V_{out}	40		V
Oscillator Output Voltage (pin 14)	V_{14}	30		V
Voltage at pin 4	V_4	2.0		V
Voltage at pins 3 and 8	V_3, V_8	5.0		V
Voltage at pin 5	V_5	7.0		V
Power Dissipation	P_D	See Thermal Information		
Operating Junction Temperature	T_J	—	125	$^{\circ}\text{C}$
Plastic Package		150	150	
Ceramic Package				
Operating Ambient Temperature Range	T_A	-55 to +125	0 to +70	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 10$ to 30 V, $T_A = 25^{\circ}\text{C}$ unless otherwise noted.)

Characteristic	Figure	Symbol	MC3520			MC3420			Unit
			Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION									
Reference Voltage ($I_{ref} = 400 \mu A$)	5	V_{ref}	7.6	7.8	8.0	7.4	7.8	8.2	V
Temperature Coefficient of Reference Voltage ($V_{CC} = 15$ V, $I_{ref} = 400 \mu A$)	5	TCV_{ref}	—	0.008	0.03	—	0.008	0.03	%/°C
Input Regulation of Reference Voltage ($I_{ref} = 400 \mu A$) ($I_{ref} = 1.0$ mA)	5	Reg_{line}	— —	3.0 5.0	7.5 —	— —	4.0 5.0	7.5 —	mV/V
DC SUPPLY SECTION									
Supply Voltage	5	V_{in}	10	—	30	10	—	30	V
Supply Current ($R_{ext} = 10$ k Ω , excluding load and current and reference current)	5	I_D	—	—	16	—	—	22	mA
OSCILLATOR SECTION									
Line Frequency Stability ($f = 20$ kHz) ($f = 20$ kHz, $V_{CC} = 15$ V, T_{low} to T_{high})	5	Δf Δf	— —	— 0.03	3.0 —	— —	— 0.04	5.0 —	% %/°C
Maximum Output Frequency ($V_{CC} = 15$ V)	6	f_{max}	100	200	—	100	200	—	kHz
Minimum Output Frequency ($V_{CC} = 15$ V)	6	f_{min}	—	2.0	5.0	—	2.0	5.0	kHz
Oscillator Output Saturation Voltage (I_{14} sink = 5.0 mA)	11	$V_{osc(sat)}$	—	0.2	0.5	—	0.2	0.5	V
OUTPUT SECTION									
Output Saturation Voltage ($I_L = 40$ mA, T_{high} to T_{low}) ($I_L = 25$ mA, T_{high} to T_{low})	7	$V_{CE(sat)}$	— —	0.33 0.22	0.5 —	— —	0.33 0.22	0.5 —	V
Output Leakage Current ($V_{CE} = 40$ V, Pins 11 and 13)	8	I_{CE}	—	—	50	—	—	50	μA
COMPARATOR SECTION									
Pulse Width Adjustment Range	9	ΔPW	0	—	100	0	—	100	%
Dead Time Adjustment Range	9	ΔDT	0	—	100	0	—	100	%
Temperature Coefficient of Dead Time	—	$TCDT$	—	0.1	—	—	0.1	—	%/°C
Comparator Bias Currents	12, 13 14	I_{IB} I_{IB}	— —	5.0 10	15 30	— —	5.0 10	15 30	μA μA

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Figure	Symbol	MC3520			MC3420			Unit
			Min	Typ	Max	Min	Typ	Max	
AUXILIARY INPUTS/OUTPUTS									
Ramp Voltage	5								V
Peak High		$V_{\text{ramp(Hi)}}$	5.5	6.0	6.5	5.5	6.0	6.5	V
Peak Low		$V_{\text{ramp(Low)}}$	2.0	2.4	2.8	2.0	2.4	2.8	V
Ramp Voltage Change ($V_{\text{ramp Hi}} - V_{\text{ramp Low}}$)	5	ΔV_{ramp}	3.0	3.5	4.0	3.0	3.5	4.0	V
Ramp Out Sink Current	5	I_{sink}	—	400	—	—	400	—	μA
Ramp Out Source Current	5	I_{source}	—	3.0	—	—	3.0	—	mA
Inhibit Input Current — High ($V_{\text{IH}} = 2.0 \text{ V}$)	10	I_{IH}	—	—	40	—	—	40	μA
Inhibit Input Current — Low ($V_{\text{IL}} = 0.8 \text{ V}$)	10	I_{IL}	—	-25	-180	—	-25	-180	μA
Symmetry Correction Input/Output 2 Inhibit Current — High ($V_{\text{SY}} = 2.0 \text{ V}$, Pin 16)	10	$I_{\text{SY/H}}$	—	—	40	—	—	40	μA
Symmetry Correction Input/Output 2 Inhibit Current — Low ($V_{\text{SY}} = 0.8 \text{ V}$, Pin 16)	10	$I_{\text{SY/L}}$	—	-10	-180	—	-10	-180	μA
F/F _{out} Source Current	—	I_{source}	—	2.0	—	—	2.0	—	mA
OUTPUT AC CHARACTERISTICS (T _A = T _{typ} , V _{CC} = ±15 V, f = 20 kHz)									

OUTPUT AC CHARACTERISTICS ($T_A = T_{\text{high}}$, $V_{\text{CC}} = +15 \text{ V}$, $f = 20 \text{ kHz}$)

Rise Time	15	t_r	—	40	—	—	40	—	ns
Fall Time	15	t_f	—	150	—	—	150	—	ns
Overlap Time	15	t_{ov}	—	275	—	—	275	—	ns
Asymmetry (Duty Cycle = 50%)	15	$\frac{t_{\text{on1}} - t_{\text{on2}}}{t_{\text{on1}}}$	—	± 1.0	—	—	± 1.0	—	%

NOTE:

 $T_{\text{high}} = +125^\circ\text{C}$ for MC3520 $+70^\circ\text{C}$ for MC3420 $T_{\text{low}} = -55^\circ\text{C}$ for MC3520 0°C for MC3420

FIGURE 2—EQUIVALENT CIRCUIT

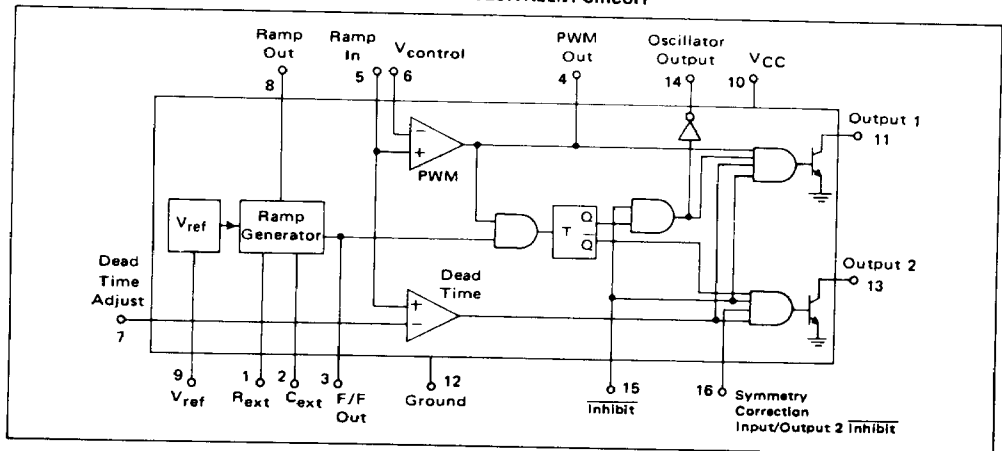
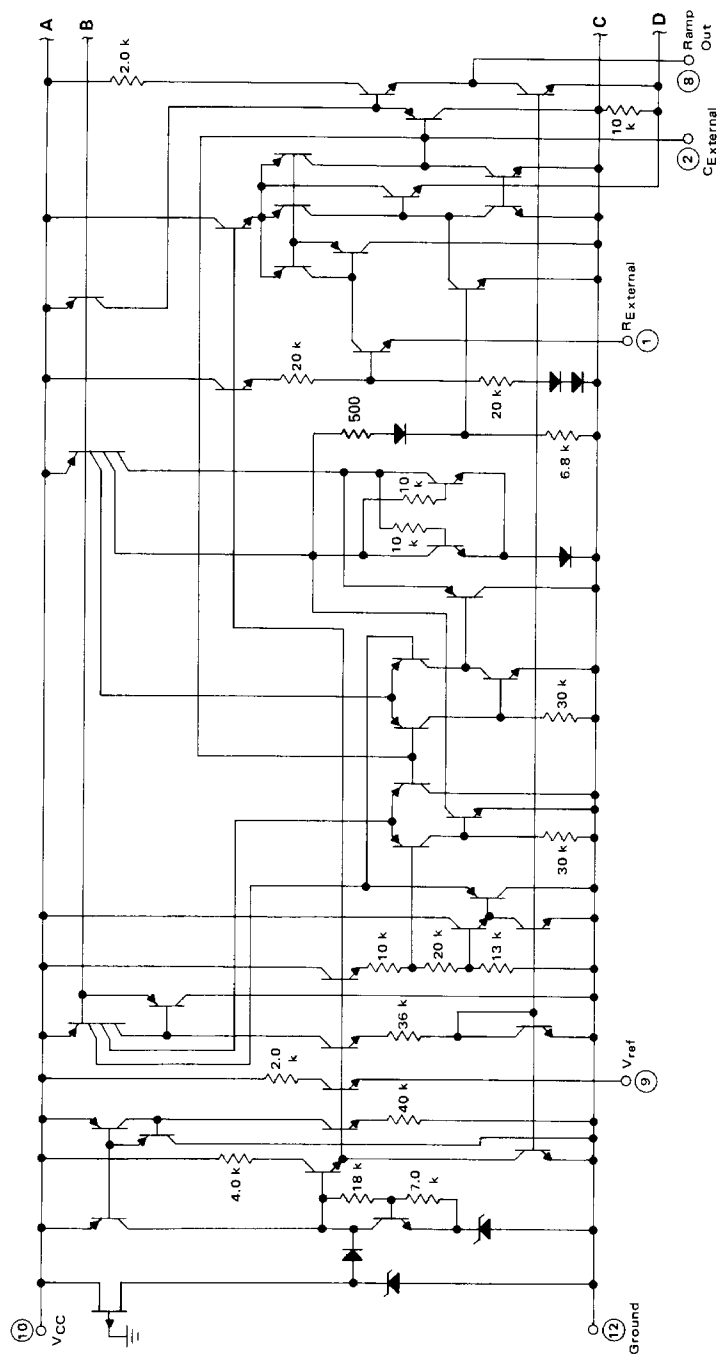


FIGURE 3 — CIRCUIT SCHEMATIC
(continued next page)



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GENERAL INFORMATION

The internal block diagram of the MC3420 is shown in Figure 2, and consists of the following sections:

Voltage Reference

A stable reference voltage is generated by the MC3420 primarily for internal use. However, it is also available externally at Pin 9 (V_{ref}) for use in setting the dead time (Pin 7) and for use as a reference for the external control loop error amplifiers.

Ramp Generator

The ramp generator section produces a symmetrical triangular waveform ramping between 2.4 V and 6.0 V, with frequency determined by an external resistor (R_{ext}) and capacitor (C_{ext}) tied from Pins 1 and 2, respectively, to ground.

PWM Comparator

The output of the ramp generator at pin 8 is normally connected to Pin 5, RAMP IN. The PWM (pulse width modulation) comparator compares the voltage at Pin 6 ($V_{control}$) to the ramp generator output. The level of $V_{control}$ determines the outputs' pulse width or duty cycle. The duty cycle of each output can vary, exclusive of dead time, from 50% (when $V_{control}$ is at approximately 2.4 V) to 0% ($V_{control}$ approximately 6.0 V).

Dead Time Comparator

An additional comparator has been included in MC3420 to allow independent adjustment of system dead time or maximum duty cycle. By dividing down V_{ref} at Pin 9 with a resistive divider or potentiometer, and applying this voltage to Pin 7, a stable dead time is obtained for prevention of inverter switching transistor cross conduction at high duty cycles due to storage time delays.

Phase Splitter

A phase splitter is included to obtain two 180° out of phase outputs for use in multiple transistor inverter systems. It consists of a toggle flip-flop whose clock signal is derived by "ANDing" the output of the PWM comparator and a signal from the ramp generator section. This "AND" gate ensures that the outputs truly alternate under control loop transient conditions. Better understanding of this feature and MC3420 operation may be gained by studying the circuit waveforms, shown in Figure 4.

FIGURE 4 – INTERNAL WAVEFORMS

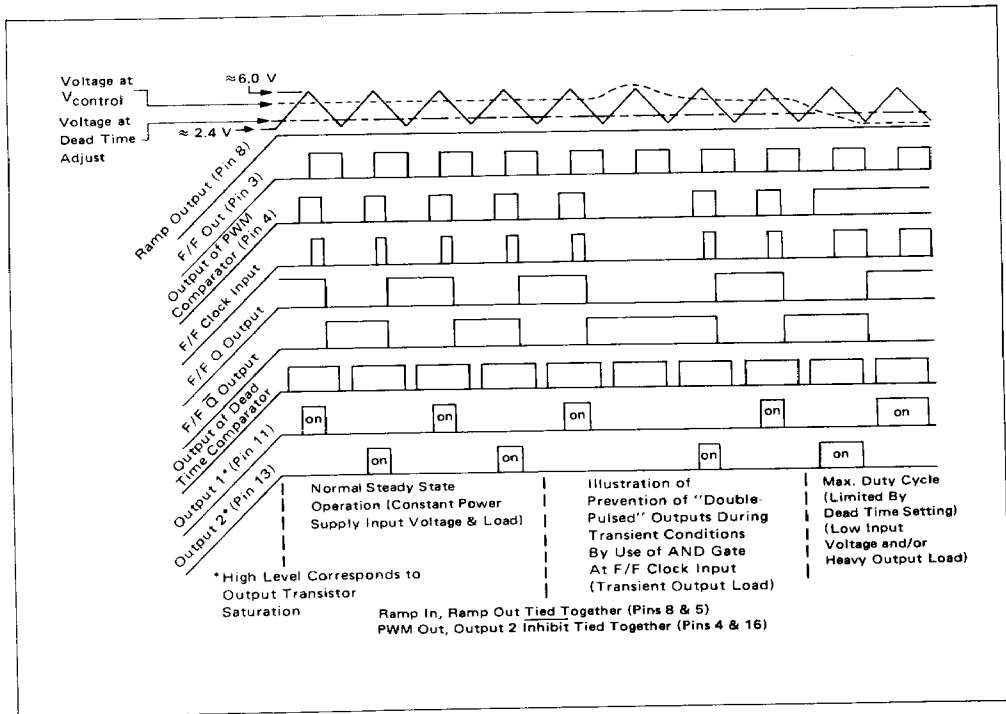


FIGURE 5 – STANDARD AC, DC TEST CIRCUIT

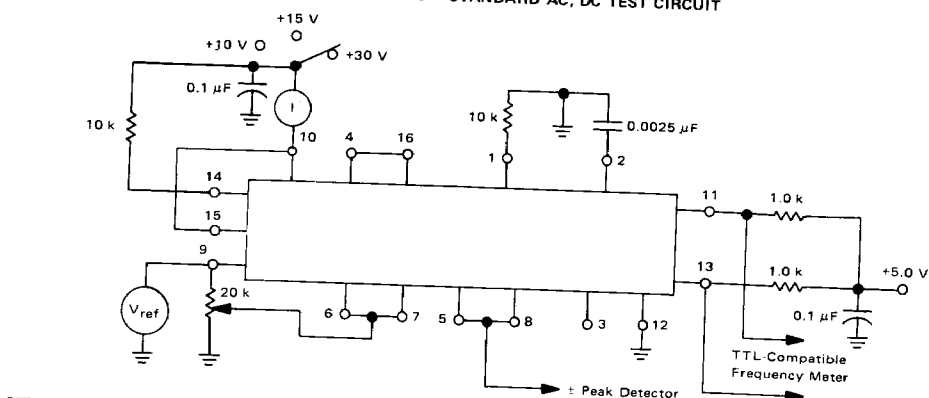


FIGURE 6 – FREQUENCY LIMIT TEST CIRCUIT

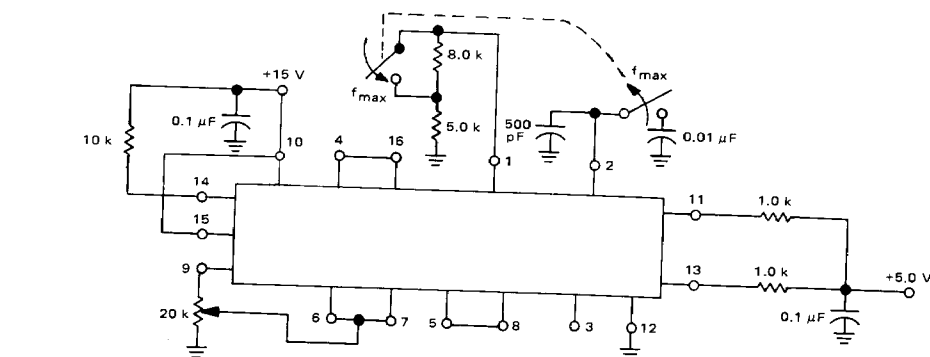
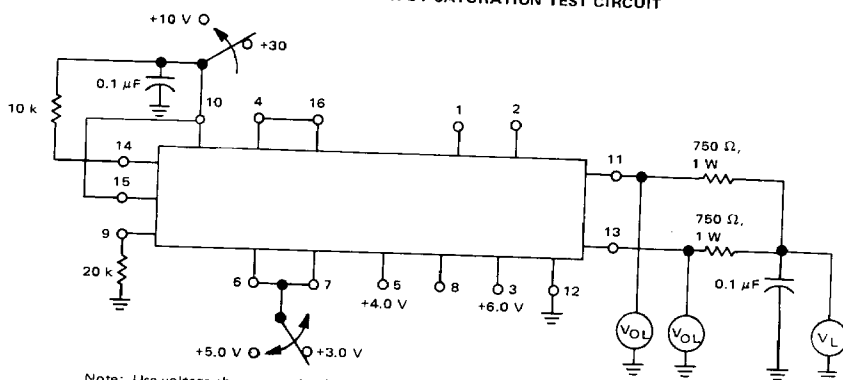


FIGURE 7 – OUTPUT SATURATION TEST CIRCUIT



Note: Use voltage change on pins 6, 7 to change output states.
A voltage must always be present on pins 6 and 7.

FIGURE 8 – OUTPUT LEAKAGE TEST CIRCUIT

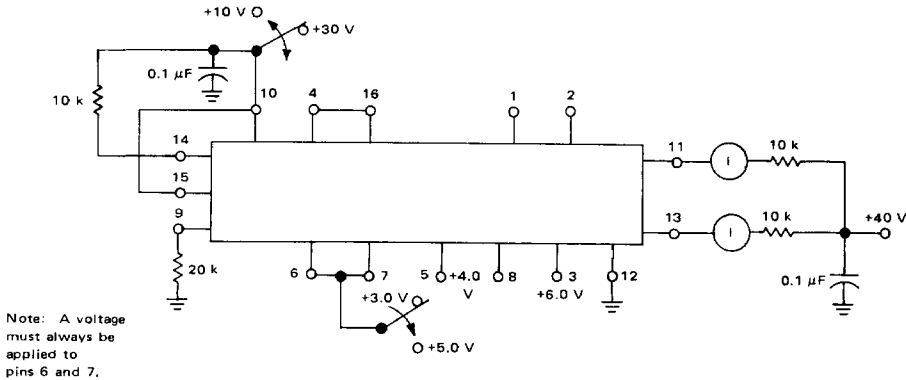
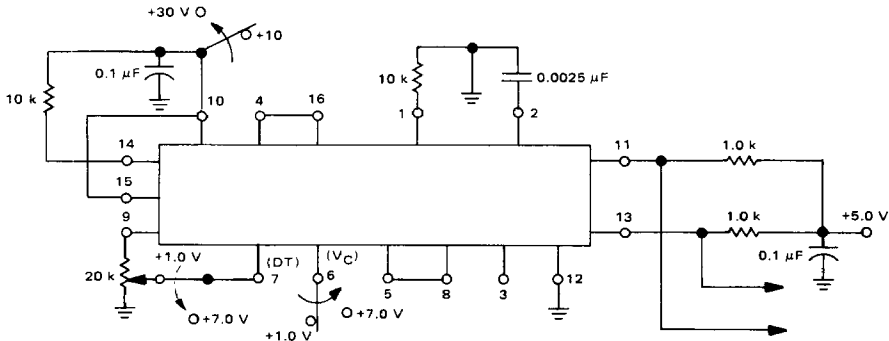


FIGURE 9 – OUTPUT DUTY CYCLE TEST CIRCUIT



TYPICAL DUTY CYCLE versus DEAD TIME VOLTAGE		TYPICAL DUTY CYCLE versus PWM VOLTAGE ($V_{control}$)	
PIN 7. DEAD TIME VOLTAGE (V) ($V_{control} = 2.0$ V)	% DUTY CYCLE (FOR EACH OUTPUT)	PIN 6. $V_{control}$ (V) (DEAD TIME VOLTAGE = 1.0 V)	% DUTY CYCLE (FOR EACH OUTPUT)
2.0	50	2.0	50
2.5	46	2.5	46
3.0	40	3.0	40
3.5	33	3.5	33
4.0	26	4.0	26
4.5	18	4.5	18
5.0	11	5.0	11
5.5	4.0	5.5	4.0
6.0	0	6.0	0

	V ₆	V ₇	
	Volts		
100% Adjust			(Pin 11 + Pin 13 = Logic "1")
Dead Time	1.0	1.0	
Pulse Width	1.0	1.0	
0% Adjust			(Pin 11)(Pin 13) = Logic "1"
Dead Time	7.0	1.0	
Pulse Width	1.0	7.0	

NOTE: Logic "1" is TTL-Compatible V_{OH} .

The diagram shows a 16-pin integrated circuit (IC) with the following connections:

- Pin 1:** Connected to a $10\text{ k}\Omega$ resistor, which is connected to a $+30\text{ V}$ source.
- Pin 2:** Connected to a $0.0025\text{ }\mu\text{F}$ capacitor, which is connected to ground.
- Pin 3:** Connected to ground.
- Pin 4:** Connected to Pin 16.
- Pin 5:** Connected to Pin 8.
- Pin 6:** Connected to a $+5.0\text{ V}$ source.
- Pin 7:** Connected to a $+3.0\text{ V}$ source.
- Pin 8:** Connected to Pin 5.
- Pin 9:** Connected to a $20\text{ k}\Omega$ resistor, which is connected to ground.
- Pin 10:** Connected to a $0.1\text{ }\mu\text{F}$ capacitor, which is connected to a $+30\text{ V}$ source.
- Pin 11:** Connected to a $1.0\text{ k}\Omega$ resistor, which is connected to a $+5.0\text{ V}$ source.
- Pin 12:** Connected to ground.
- Pin 13:** Connected to a $1.0\text{ k}\Omega$ resistor, which is connected to a $+5.0\text{ V}$ source.
- Pin 14:** Connected to a $5.6\text{ k}\Omega$ resistor, which is connected to a $+30\text{ V}$ source.
- Pin 15:** Connected to a voltmeter (V).
- Pin 16:** Connected to Pin 4.

The diagram shows a 16-pin integrated circuit (IC) with the following connections:

- Pin 1:** Connected to a $+3.0\text{ V}$ source through a $10\text{ k}\Omega$ resistor.
- Pin 2:** Connected to a $+10\text{ V}$ source through a $0.1\text{ }\mu\text{F}$ capacitor.
- Pin 3:** Connected to a $+4.0\text{ V}$ source through a $20\text{ k}\Omega$ resistor.
- Pin 4:** Connected to a $+5.0\text{ V}$ source through a $1.0\text{ k}\Omega$ resistor.
- Pin 5:** Connected to a $+5.0\text{ V}$ source through a $1.0\text{ k}\Omega$ resistor.
- Pin 6:** Connected to a $+5.0\text{ V}$ source through a $0.1\text{ }\mu\text{F}$ capacitor.
- Pin 7:** Connected to a $+5.0\text{ V}$ source through a $0.1\text{ }\mu\text{F}$ capacitor.
- Pin 8:** Connected to a $+5.0\text{ V}$ source through a $0.1\text{ }\mu\text{F}$ capacitor.
- Pin 9:** Connected to a $+5.0\text{ V}$ source through a $0.1\text{ }\mu\text{F}$ capacitor.
- Pin 10:** Connected to a $+5.0\text{ V}$ source through a $0.1\text{ }\mu\text{F}$ capacitor.
- Pin 11:** Connected to a $+5.0\text{ V}$ source through a $1.0\text{ k}\Omega$ resistor.
- Pin 12:** Connected to a $+5.0\text{ V}$ source through a $0.1\text{ }\mu\text{F}$ capacitor.
- Pin 13:** Connected to a $+5.0\text{ V}$ source through a $1.0\text{ k}\Omega$ resistor.
- Pin 14:** Connected to a $+5.0\text{ V}$ source through a $1.0\text{ k}\Omega$ resistor.
- Pin 15:** Connected to a $+5.0\text{ V}$ source through a $1.0\text{ k}\Omega$ resistor.
- Pin 16:** Connected to a $+5.0\text{ V}$ source through a $1.0\text{ k}\Omega$ resistor.

FIGURE 13 – DEAD TIME BIAS CURRENT TEST CIRCUIT

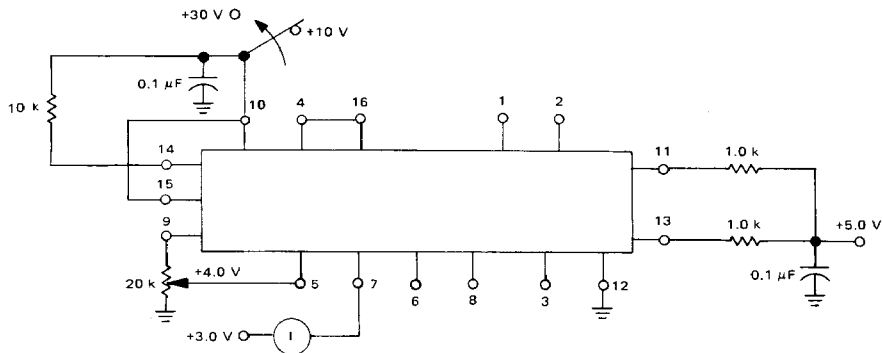


FIGURE 14 – RAMP IN BIAS CURRENT TEST CIRCUIT

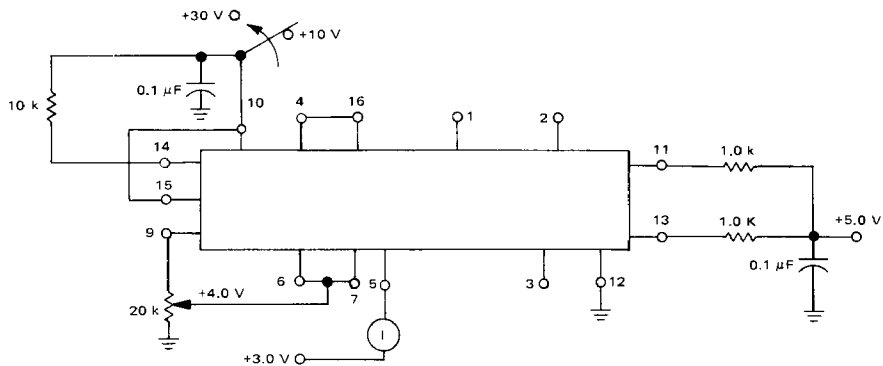
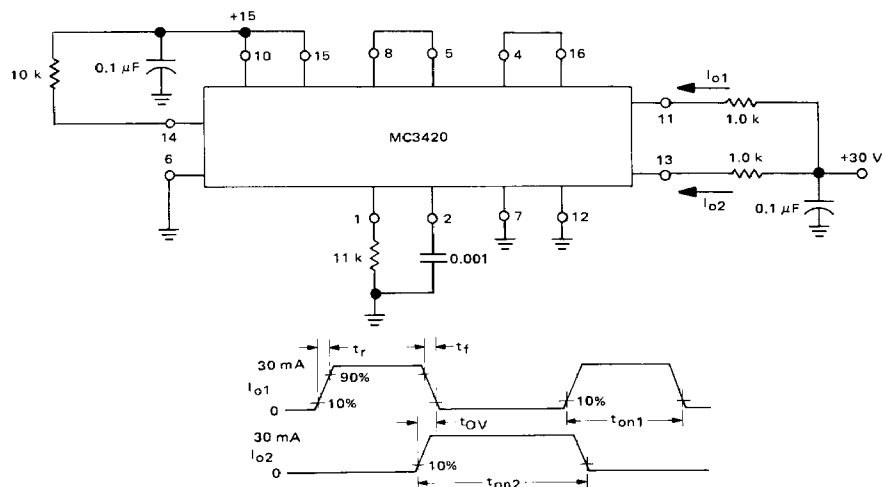


FIGURE 15 – AC TEST CIRCUIT AND WAVEFORMS



TYPICAL CHARACTERISTICS

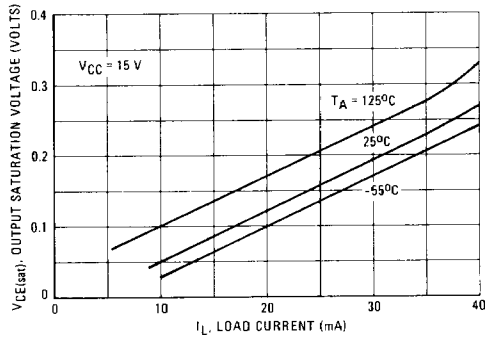
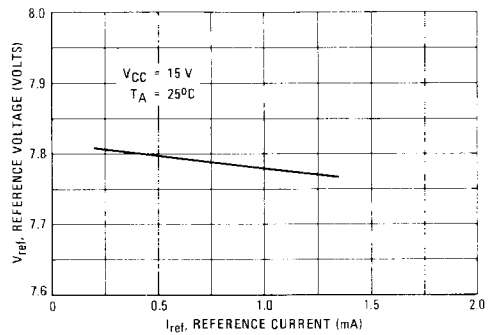
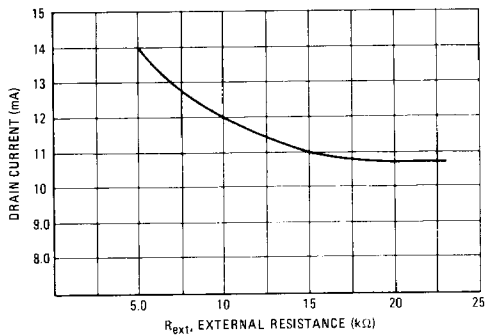
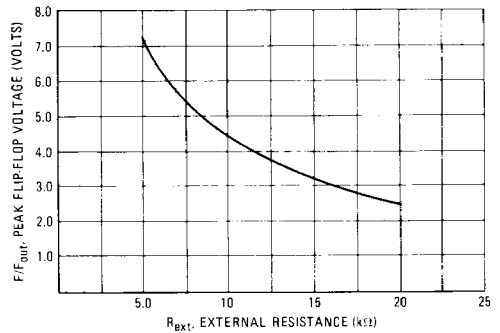
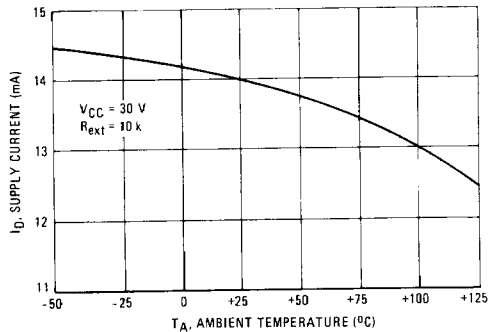
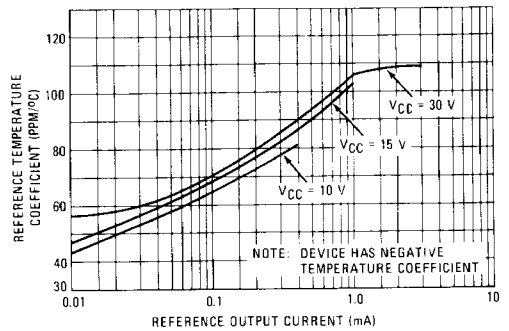
FIGURE 16 – OUTPUT SATURATION VOLTAGE
versus LOAD CURRENTFIGURE 17 – REFERENCE VOLTAGE versus
REFERENCE CURRENTFIGURE 18 – DRAIN CURRENT versus
EXTERNAL RESISTANCEFIGURE 19 – PEAK FLIP-FLOP_{out} VOLTAGE
versus EXTERNAL RESISTANCE

FIGURE 20 – DRAIN CURRENT versus TEMPERATURE

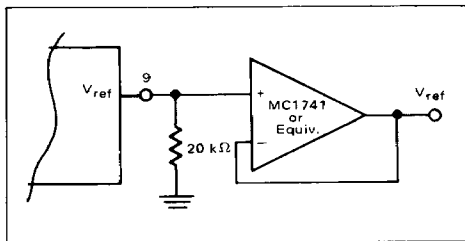
FIGURE 21 – REFERENCE VOLTAGE TEMPERATURE
COEFFICIENT versus OUTPUT CURRENT

OPERATION AND APPLICATIONS INFORMATION

The Voltage Reference

The temperature coefficient of V_{ref} has been optimized for a $400\ \mu A$ ($\approx 20\ k\Omega$) load. If increased current capability is required, an op amp buffer may be used, as shown in Figure 22.

FIGURE 22



Output Frequency

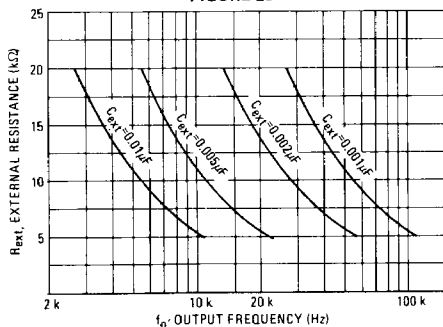
The values of R_{ext} and C_{ext} for a given output frequency, f_o , can be found from:

$$f_o \approx \frac{0.55}{R_{ext} C_{ext}}; 5.0\ k\Omega \leq R_{ext} \leq 20\ k\Omega \text{ (Eq. 1)}$$

or from the graph shown in Figure 23.

Note that f_o refers to the frequency of Output 1 (Pin 11) or Output 2 (Pin 13). The frequency of the ramp generator output waveform at Pin 8 will be twice f_o .

FIGURE 23

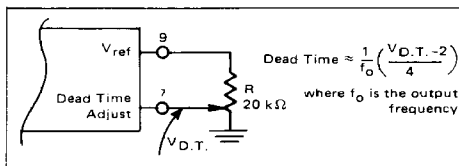


Dead Time

Figure 24 illustrates how to set or adjust the MC3420 outputs' dead time or maximum duty cycle. For minimum dead time drift with temperature or supply voltage, $V_{D.T.}$ should be derived from V_{ref} as shown.

Pin 7 should always be tied to some voltage between Gnd and V_{ref} .

FIGURE 24

Connections to the $V_{control}$ Pin

In many systems, it is necessary to make multiple connections to the $V_{control}$ Pin in order to implement features in addition to voltage regulation such as current limiting, soft start, etc. These can be made by the use of a simple "diode-OR" connection, as shown in Figure 25. This allows whichever control element is seeking the lowest PWM duty cycle to dominate. Note that a resistor, R_1 , whose value is $\leq 50\ k\Omega$ is placed from the $V_{control}$ Pin to ground. This is necessary to provide a dc path for the PWM comparator input bias current under all conditions.

The system duty cycle is given by:

$$D.C. (\%) \approx \frac{V_{control} - 2}{4} \times 100 \text{ (Eq. 2)}$$

FIGURE 25

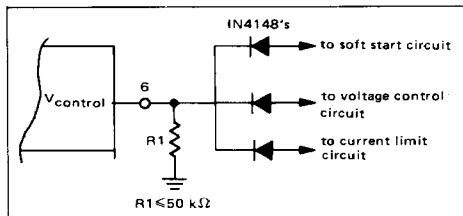


FIGURE 26



15 V, 2 A DC-to-DC Converter

Figure 29 illustrates the use of the MC3520 in a PWM switching power supply utilizing a single series switching element (see Appendix for description of PWM switching supply configurations). The series switching transistor, Q1, chops the dc input voltage, V_{in} , at a frequency of ≈ 25 kHz, and the resulting waveform is filtered by L1 and C1 to provide the dc output voltage. The frequency is set by R4 and C3, and since the outputs of the MC3520 are wire-ORed together, f_o is twice that given by Equation 1 and Figure 23. V_o is regulated by comparing its value to the MC3520's reference voltage and amplifying the error voltage with U1. The output of U1 is fed into the MC3520 to provide PWM to Q1, thereby controlling its duty cycle and thus the value of V_o .

C2 provides a soft-start feature during power up to prevent output voltage overshoots and excessive start up currents through Q1.

Short circuit protection is provided by R_{SC} , Q3 and Q4. When an overcurrent condition occurs, Q3 is turned on by the voltage across R_{SC} ; Q3 drives Q4 on, which raises the voltage at pin 6 ($V_{control}$) of the MC3520, reducing Q1's duty cycle and maintaining a constant output current of ≈ 2.5 A.

5 V, 50 A Line-Operated Supply

A 5 V, 50 A line-operated 20 kHz switching power supply using the MC3520 is shown in Figures 30a and b. An explanation of the operation of each section of the supply follows.

Input Section

The 120 Vac line is full wave voltage doubled by CR1, CR2, C1 and C2 to provide 310 Vdc to the power section of the supply. Inrush surge current limiting is provided by R1, which is shorted out of the circuit by Q1 after C1 and C2 are initially charged.

Power Section

The supply utilizes two switching transistors, Q2 and Q3, in a half-bridge configuration (see Appendix) to drive the high frequency power transformer, T2.

The bases of Q2 and Q3 are driven by T3 and T4, respectively, to provide isolation from the control and base drive sections of the supply. CR3, CR5, CR6, and CR8 constitute anti-saturation (Baker) clamps which provide increased and more uniform switching speeds for

Q2 and Q3. CR4 and CR7 allow reverse base currents during turn off.

Output Section

The output of T2 is rectified by Schottky diodes, CR9 and CR10. VR1 is a transient suppressor to protect CR9 and CR10 from transients that might cause reverse breakdown. L1 and C4 constitute the output filter. C4 should have very low ESR (equivalent series resistance) at 20 kHz to provide the most effective filtering. L2 and C5 make up a high-frequency filter to reduce commutation spikes which pass L1 due to its interwinding capacitance. R_{SC} provides output overcurrent sensing to the control section.

Control Section

The MC3520 provides the PWM control for the supply. R2 is adjusted to obtain a 20 kHz operating frequency. R3 adjusts the dead time ($\approx 5 \mu s$ each half-cycle). U1A and U1B are the output current and output voltage error amplifiers, respectively. R5 sets the output voltage while R4 determines the output current limit. C7 and C8 are the current and voltage loop compensation capacitors.

C6 provides the soft-start feature while Q4 ensures a soft-start after each system inhibit (pin 15 low).

Base Drive Section

Turn on drive to the power section switching transistors occurs when each of the outputs of the MC3520 saturate. Q5 or Q6 are therefore turned on, and 15 V applied to the primaries of T3 or T4, supplying forward base drive to Q2 or Q3.

Turn off drive occurs when Q5 or Q6 turn off, and the magnetizing energy stored in T3 or T4's core is transformed into a negative "flyback" voltage at their secondaries, providing reverse base drive to Q2 or Q3. CR11 and CR12 act as clamps, to prevent this flyback voltage from exceeding -5 V at T3 or T4's secondary (30 V on Q5 or Q6's collector).

Q1 Driver Section

Q7 and T1 provide the gate drive to Q1. Q7 starts operating after an initial delay of 100 ms created by the soft-start circuit, thereby allowing C1 and C2 to charge up before firing Q1.

FIGURE 29 — 15 V, 2A DC-TO-DC CONVERTER

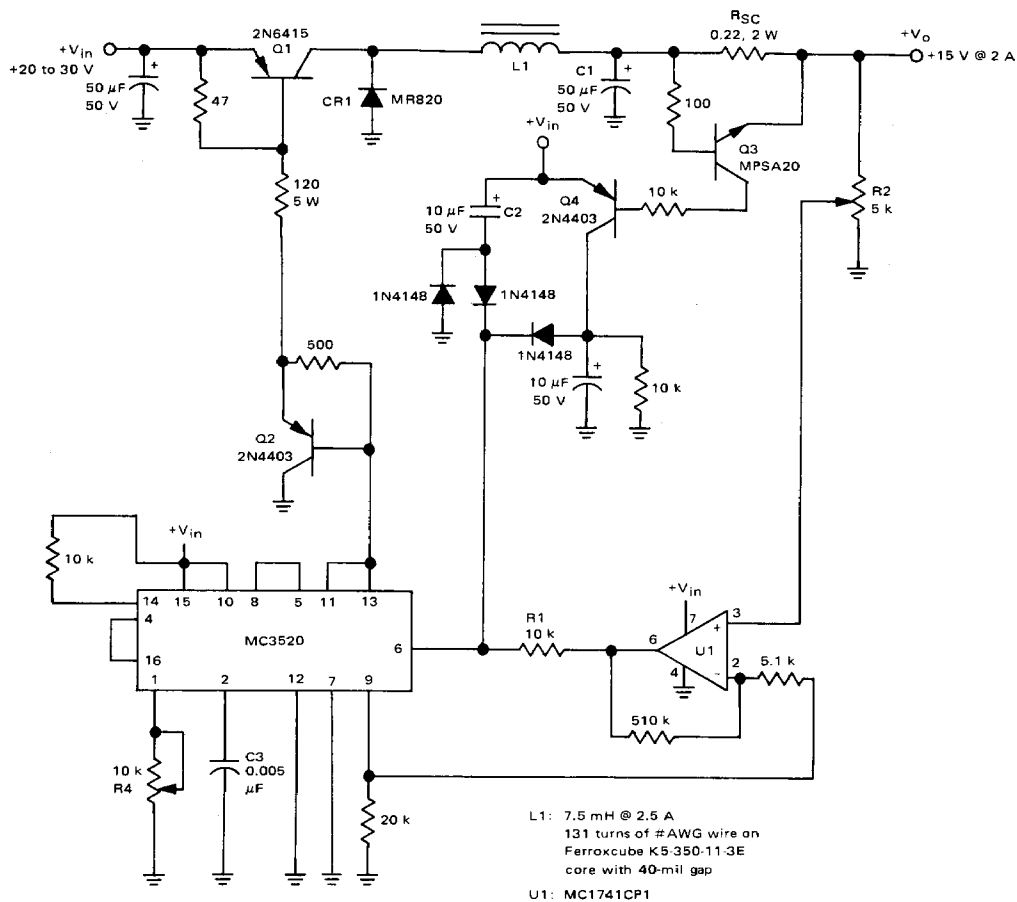
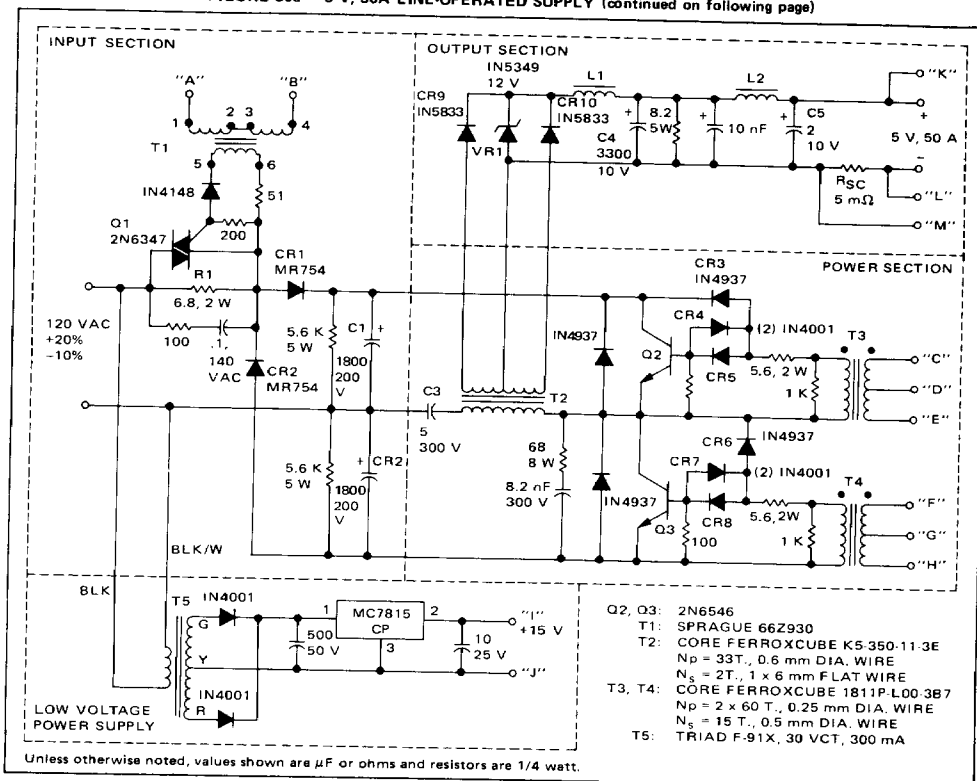


FIGURE 30a - 5 V, 50 A LINE-OPERATED SUPPLY (continued on following page)



Performance	
Line Regulation:	0.4%
Load Regulation:	0.25%
Output Ripple and Noise:	60 mV p-p 25 mV rms
Line current surge at turn-on:	35 A max
Efficiency:	80%

CONTROL SECTION

U1: MC3458P1

U1A: Output Current Adjust

U1B: Output Voltage Adjust

BASE DRIVE SECTION

(2) IN4001

Q1 DRIVER SECTION

Q1 DRIVER SECTION

Unless otherwise noted, values shown are μF or ohms and resistors are 1/4 watt.

Figure 2A shows the two-transistor push-pull configuration. Unlike the series configuration, it can be used to either step-up or step-down the input voltage, V_{CC} , and also provides input-output isolation. It does, however, have the disadvantage that additional circuitry must be used to provide symmetry correction for the prevention of transformer saturation.

Half-Bridge Configuration

The half-bridge configuration, shown in Figure 3A, does not suffer from the symmetry problems of the push-pull configuration since the transformer primary is capacitively coupled. This prevents transformer core saturation since no net dc current is allowed to flow in its primary.

Note that for the same input power, bus voltage, and duty cycle, the half-bridge requires switching transistors

which have twice the current and half the voltage requirements as those of the push-pull configuration.

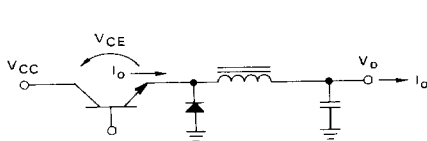
Full-Bridge Configuration

By replacing the bridge capacitors, C, of the half-bridge configuration of Figure 4A results. With this configuration, double the power of the half-bridge configuration can be obtained at the expense of two additional switching transistors and their associated circuitry.

ABBREVIATIONS USED IN FIGURES 1A THROUGH 4A

I_C :	Switching transistor collector current
V_{CE} :	Switching transistor collector-to-emitter voltage
P_{in} :	Average input power
D.C.:	Inverter duty cycle
V_{CC} :	DC bus voltage
$V_{CEO(sus)}$:	V_{CE} that transistor must withstand during turn-on
V_{CEX} :	V_{CE} that transistor must block during non-conduction period.

FIGURE 1A — SERIES CONFIGURATION



TRANSISTOR REQUIREMENTS*

$$I_C \geq I_o$$

$$V_{CEO(sus)} \geq V_{CC}$$

$$V_{CEX} \geq V_{CC}$$

*See explanation of abbreviations in text.

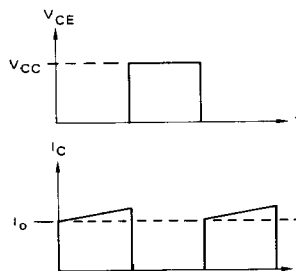
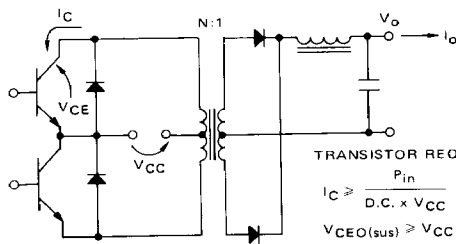


FIGURE 2A — PUSH-PULL CONFIGURATION



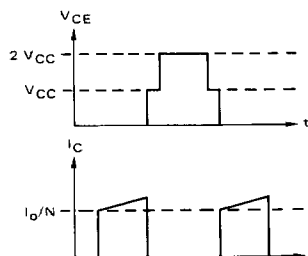
TRANSISTOR REQUIREMENTS*

$$I_C \geq \frac{P_{in}}{D.C. \times V_{CC}}$$

$$V_{CEO(sus)} \geq V_{CC}$$

$$V_{CEX} \geq 2 V_{CC}$$

*See explanation of abbreviations in text.



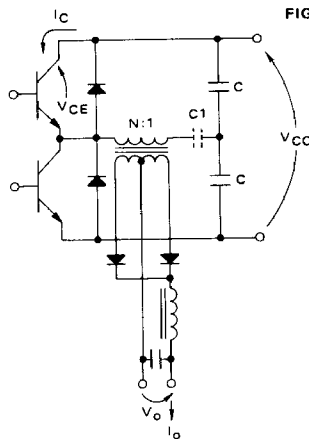
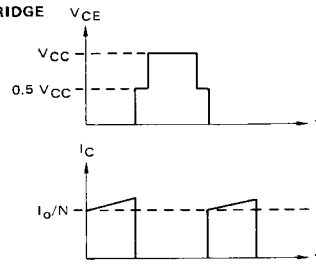


FIGURE 3A — HALF-BRIDGE CONFIGURATION



TRANSISTOR REQUIREMENTS*

$$I_C \geq \frac{2 \times P_{in}}{D.C. \times V_{CC}}$$

$$V_{CE0(sus)} \geq V_{CC}/2$$

$$V_{CEX} \geq V_{CC}$$

*See explanation of abbreviations in text.

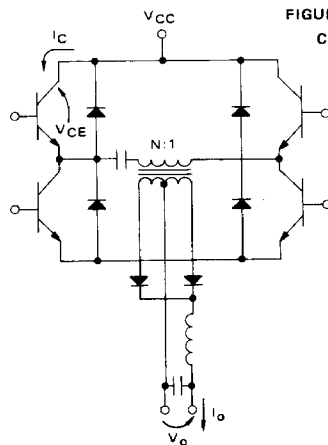
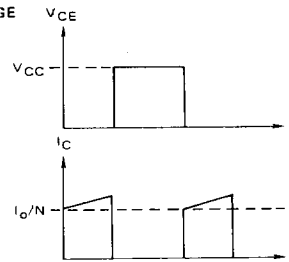


FIGURE 4A — FULL-BRIDGE CONFIGURATION



TRANSISTOR REQUIREMENTS*

$$I_C \geq \frac{P_{in}}{D.C. \times V_{CC}}$$

$$V_{CE0(sus)} \geq V_{CC}$$

$$V_{CEX} \geq V_{CC}$$

*See explanation of abbreviations in text.

REFERENCES

More detailed information on switching power supplies may be obtained by consulting the following articles:

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