



MK2049-02/03 Communications Clock PLLs

Description

The MK2049-02 and MK2049-03 are Phase-Locked Loop (PLL) based clock synthesizers that accept multiple input frequencies. With an 8 kHz clock input as a reference, the MK2049-02/03 generate T1, E1, T3, E3, ISDN, xDSL, and other communications frequencies. This allows for the generation of clocks frequency-locked and phase-locked to an 8 kHz backplane clock, simplifying clock synchronization in communications systems. The MK2049-02/03 can also accept a T1, E1, T3, or E3 input clock and provide the same output for loop timing. All outputs are frequency-locked together and to the input.

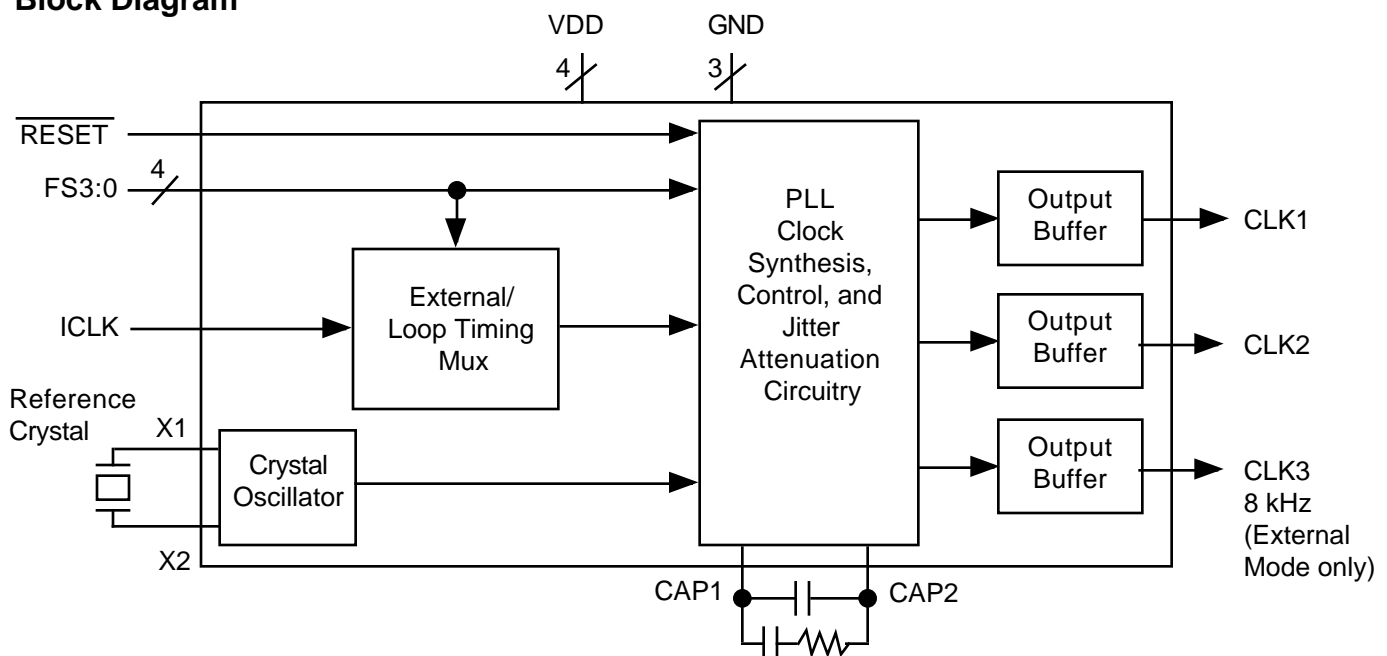
These parts also have a jitter-attenuated buffer capability. In this mode, the MK2049-02/03 are ideal for filtering jitter from 27 MHz video clocks or other clocks with high jitter.

ICS can customize these devices for many other different frequencies. Contact your ICS representative for more details.

Features

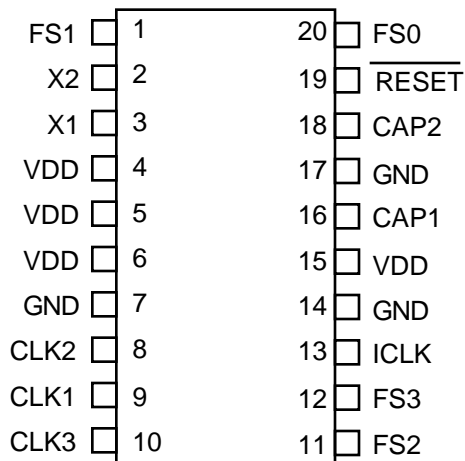
- Packaged in 20 pin SOIC
- Fixed input-output phase relationship on most clock selections
- Meets the TR62411, ETS300 011, and GR-1244 specification for MTIE, Pull-in/Hold-in Range, Phase Transients, and Jitter Generation for Stratum 3, 4, and 4E
- Accept multiple inputs: 8 kHz backplane clock, Loop Timing frequencies, or 10-28 MHz
- Lock to 8 kHz ± 100 ppm (External mode)
- Buffer Mode allows jitter attenuation of 10–28 MHz input and x1/x0.5 or x2/x4 outputs
- Exact internal ratios enable zero ppm error
- Output clock rates include T1, E1, T3, E3, ISDN, xDSL, and OC3 submultiples
- 5 V $\pm 5\%$ operation. Refer to MK2049-34 for 3.3 V

Block Diagram





Pin Assignment



20 pin (300 mil) SOIC

Pin Descriptions

Number	Name	Type	Description
1	FS1	I	Frequency Select 1. Determines CLK input/outputs per tables on pages 4 & 5.
2	X2	XO	Crystal connection. Connect to a MHz crystal as shown in the tables on pages 4 & 5.
3	X1	XI	Crystal connection. Connect to a MHz crystal as shown in the tables on pages 4 & 5.
4	VDD	P	Connect to +5V.
5	VDD	P	Connect to +5V.
6	VDD	P	Connect to +5V.
7	GND	P	Connect to ground.
8	CLK2	O	Clock 2 output determined by status of FS3:0 per tables on pages 4 & 5.
9	CLK1	O	Clock 1 output determined by status of FS3:0 per tables on pages 4 & 5. Always 1/2 of CLK2.
10	CLK3	O	Clock 3 as shown in tables on pages 4 & 5; typically recovered 8 kHz clock output.
11	FS2	I	Frequency Select 2. Determines CLK input/outputs per tables on pages 4 & 5.
12	FS3	I	Frequency Select 3. Determines CLK input/outputs per tables on pages 4 & 5.
13	ICLK	I	Input clock connection. Connect to 8 kHz backplane or MHz clock.
14	GND	P	Connect to ground.
15	VDD	P	Connect to +5V.
16	CAP1	LF	Connect the loop filter ceramic capacitors and resistor between this pin and CAP2.
17	GND	P	Connect to ground.
18	CAP2	LF	Connect the loop filter ceramic capacitors and resistor between this pin and CAP1.
19	<u>RESET</u>	I	Reset pin. Resets internal PLL when low. Outputs will stop low. Internal pull-up resistor.
20	FS0	I	Frequency Select 0. Determines CLK input/outputs per tables on pages 4 & 5.

Type: XI, XO = crystal connections, I = Input, O = output, P = power supply connection, LF = loop filter connections



Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (Note 1)					
Supply Voltage, VDD	Referenced to GND			7	V
Inputs and Clock Outputs		-0.5		VDD+0.5	V
Ambient Operating Temperature	MK2049-0xS	0		70	°C
	MK2049-0xSI	-40		85	°C
Soldering Temperature	Max of 10 seconds			250	°C
Storage Temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 5V unless noted)					
Operating Voltage, VDD		4.75	5	5.25	V
Input High Voltage, VIH		2			V
Input Low Voltage, VIL				0.8	V
Input High Voltage, VIH	Pin 19 only	VDD-0.5			V
Input Low Voltage, VIL	Pin 19 only			0.5	V
Output High Voltage	IOH=-4 mA	VDD-0.4			V
Output High Voltage	IOH=-8 mA	2.4			V
Output Low Voltage	IOL=8 mA			0.4	V
Operating Supply Current, IDD	No Load, VDD=5.0V		20		mA
Short Circuit Current	Each output		±100		mA
Input Capacitance, FS3:0			7		pF
AC CHARACTERISTICS (VDD = 5V unless noted)					
Input Frequency, External Mode, Note 3	ICLK		8.000		kHz
Input Clock Pulse Width		10			ns
Propagation Delay	ICLK to CLK2		0	2	ns
Output-Output Skew, Zero Delay Selections	CLK1 to CLK2, Note 2			500	ps
Output Clock Rise Time	0.8 to 2.0 V			1.5	ns
Output Clock Fall Time	2.0 to 0.8 V			1.5	ns
Output Clock Duty Cycle, High Time	At VDD/2	40		60	%
Actual mean frequency error versus target	Any clock selection		0	0	ppm

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.
2. CLK1 in the MK2049-02 may have the rising or falling edge aligned with the rising edge of CLK2. See the INPUT AND OUTPUT SYNCHRONIZATION section for more details.
3. For loop timing modes and buffer modes, see tables on page 2 for required input clock frequencies.



MK2049-02 Output Decoding Table – External Mode (MHz)

ICLK	FS3	FS2	FS1	FS0	CLK1 (Note 3)	CLK2	Crystal	CLK3
8 kHz	0	0	0	0	1.544	3.088	12.352	8 kHz
8 kHz	0	0	0	1	2.048	4.096	12.288	8 kHz
8 kHz	0	0	1	0	22.368	44.736	11.184	8 kHz
8 kHz	0	0	1	1	17.184	34.368	11.456	8 kHz
8 kHz	0	1	0	0	19.44	38.88	12.96	8 kHz
8 kHz	0	1	0	1	16.384	32.768	8.192	8 kHz
8 kHz	0	1	1	0	24.576	49.152	12.288	8 kHz
8 kHz	0	1	1	1	25.92	51.84	12.96	8 kHz
8 kHz	1	1	0	0	10.24	20.48	10.24	8 kHz
8 kHz	1	1	0	1	4.096	8.192	12.288	8 kHz

MK2049-02 Output Decoding Table – Loop Timing Mode (MHz)

ICLK	FS3	FS2	FS1	FS0	CLK1 (Note 3)	CLK2	Crystal	CLK3
1.544	1	0	0	0	1.544	3.088	12.352	N/A
2.048	1	0	0	1	2.048	4.096	12.288	N/A
44.736	1	0	1	0	22.368	44.736	11.184	N/A
34.368	1	0	1	1	17.184	34.368	11.456	N/A

MK2049-02 Output Decoding Table – Buffer Mode (MHz)

ICLK	FS3	FS2	FS1	FS0	CLK1 (Note 3)	CLK2	Crystal	CLK3
19 - 28	1	1	1	0	ICLK/2	ICLK	ICLK/2	N/A
10 - 14	1	1	1	1	2*ICLK	4*ICLK	ICLK	N/A

- 0 = connect directly to ground, 1 = connect directly to VDD.
- Crystal is connected to pins 2 and 3; clock input is applied to pin 13.


= No Zero (Fixed) I/O Delay for these selections shown in the shaded boxes.

Note 3: CLK1 rising or falling edge may align with the input clock. See Figure 1 on page 6 for more details.



MK2049-03 Output Decoding Table – External Mode (MHz)

ICLK	FS3	FS2	FS1	FS0	CLK1	CLK2	CLK3	Crystal
8 kHz	0	0	0	0	1.544	3.088	8 kHz	12.352
8 kHz	0	0	0	1	2.048	4.096	8 kHz	12.288
8 kHz	0	0	1	0	18.688	37.376	8 kHz	9.344
8 kHz	0	0	1	1	7.68	15.36	8 kHz	10.24
8 kHz	0	1	0	0	19.44	38.88	8 kHz	9.72
8 kHz	0	1	0	1	16.384	32.768	8 kHz	8.192
8 kHz	0	1	1	0	24.576	49.152	8 kHz	12.288
8 kHz	0	1	1	1	8.64	17.28	8 kHz	11.52
8 kHz	1	0	1	0	12.416	24.832	8 kHz	12.416
8 kHz	1	0	1	1	18.528	37.056	1.544 MHz	12.352
8 kHz	1	1	0	0	10.24	20.48	8 kHz	10.24
8 kHz	1	1	0	1	4.096	8.192	8 kHz	8.192

 = No Zero (Fixed) I/O Delay for these selections shown in the shaded boxes.

MK2049-03 Output Decoding Table – Loop Timing Mode (MHz) for T1/E1

ICLK	FS3	FS2	FS1	FS0	CLK1	CLK2	Crystal	CLK3
1.544	1	0	0	0	1.544	3.088	12.352	N/A
2.048	1	0	0	1	2.048	4.096	12.288	N/A

MK2049-03 Output Decoding Table – Buffer Mode (MHz)

ICLK	FS3	FS2	FS1	FS0	CLK1	CLK2	Crystal	CLK3
19 - 28	1	1	1	0	ICLK/2	ICLK	ICLK/2	N/A
10 - 14	1	1	1	1	2*ICLK	4*ICLK	ICLK	Low

- 0 = connect directly to ground, 1 = connect directly to VDD.
- Crystal is connected to pins 2 and 3; clock input is applied to pin 13.

OPERATING MODES

The MK2049-02/03 have three operating modes: External, Loop Timing, and Buffer. Although each mode uses an input clock to generate various output clocks, there are important differences in their input and crystal requirements.

External Mode

The MK2049-02/03 accept an external 8 kHz clock and will produce a number of common communication clock frequencies. The 8 kHz input clock does not need to have a 50% duty cycle; a “high” or “on” pulse as narrow as 10 ns is acceptable. In the MK2049-02, the rising edge of CLK2 is aligned with the rising edge of the 8 kHz ICLK; refer to Figure 1 for more details. In the MK2049-03, the rising edges of CLK1 and CLK2 are both aligned with the rising edge of the 8 kHz ICLK (unless noted in the shaded area of the table); refer to Figure 2 for more details.

Loop Timing Mode

This mode can be used to remove the jitter from standard high-frequency communication clocks. For T1 and E1 inputs, the CLK1 output will be the same as the input frequency, with CLK2 at twice the input frequency. For T3



OPERATING MODES (continued)

and E3 inputs, CLK1 will be 1/2 the input frequency and CLK2 will be the same as the input frequency.

Buffer Mode

Unlike the other two modes that accept only a single specified input frequency, Buffer Mode will accept a wider range of input clocks. The input jitter is attenuated, and the outputs on CLK1 and CLK2 also provide the option of getting x1, x2, x4, or 1/2 of the input frequency. For example, this mode can be used to remove the jitter from a 27 MHz clock, generating low-jitter 27 MHz and 13.5 MHz outputs.

INPUT AND OUTPUT SYNCHRONIZATION

As shown in the tables on pages 4 and 5, the MK2049-02/03 offer a Zero Delay feature in most selections. In these selections, there is an internal feedback path between ICLK and the CLK2 output clock. This provides a fixed phase relationship between the input and output, a requirement in many communications systems.

MK2049-02

As illustrated in the diagram below, when using the MK2049-02 in one of the Zero Delay selections, the rising edge of ICLK will be aligned with the rising edge of CLK2. However, the CLK1 edge in these cases will be either rising or falling. (8 kHz is used in this illustration, but the same is true for the Zero Delay selections in the Loop Timing and Buffer modes.)

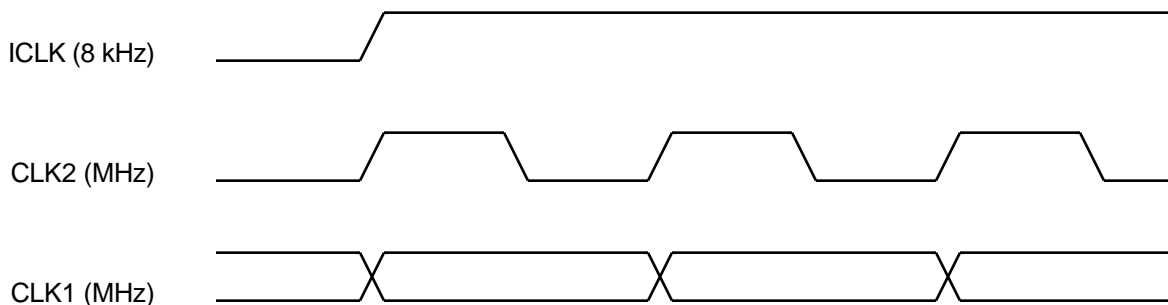


Figure 1. MK2049-02 Input and Output Clock Waveforms in Zero Delay Selections



INPUT AND OUTPUT SYNCHRONIZATION (continued)

MK2049-03

As illustrated in the diagram below, when using the MK2049-03 in one of the Zero Delay selections, the rising edge of ICLK will be aligned with the rising edges of CLK1 and CLK2.

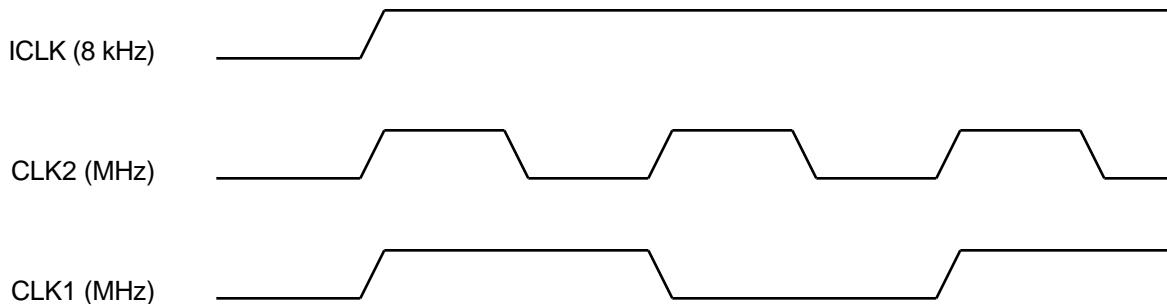


Figure 2. MK2049-03 Input and Output Clock Waveforms in Zero Delay Selections

In the MK2049-02 and MK2049-03 selections that are not Zero Delay, the phase relationship between the input and output clocks is not predictable. Although it will not change once the MK2049-02/03 is running, this relationship is likely to change when power is interrupted.

Measuring Zero Delay on the MK2049

The MK2049-02/03 both produce low-jitter output clocks. In addition, both parts have a very low bandwidth--on the order of a few Hertz. Since most 8 kHz input clocks will have high jitter, this can make measuring the input-to-output skew (zero delay feature) very difficult. The MK2049 are designed to reject the input jitter; when the input and output clocks are both displayed on an oscilloscope, they may appear not to be locked because the scope trigger point is constantly changing with the input jitter. In fact, the input and output clocks probably are locked, and the MK2049 will have zero delay to the average position of the 8 kHz input clock. In order to see this clearly, a low jitter 8 kHz input clock is necessary. Most lab frequency sources are NOT SUITABLE for this since they have high jitter at low frequencies.

Frequency Locking to the Input

In all modes, the output clocks are frequency-locked to the input. The output will remain at the specified output frequency as long as the combined variation of the input frequency and the crystal does not exceed 100 ppm. For example, if the crystal can vary ± 40 ppm (initial accuracy + temperature + aging), then the input frequency can vary by up to 60 ppm and still have the output clock remain frequency-locked.



LAYOUT AND EXTERNAL COMPONENTS

The MK2049-02/03 require a minimum number of external components for proper operation. Decoupling capacitors of $0.01\mu\text{F}$ must be connected between VDD and GND pins close to the chip (especially pins 4 and 7, 15 and 17), and $33\ \Omega$ terminating resistors should be used on clock outputs with traces longer than 1 inch (assuming 50 traces).

PC Board Layout

A proper board layout is critical to the successful use of the MK2049. In particular, the CAP1 and CAP2 pins are very sensitive to noise and leakage (CAP2 at pin 18 is the most sensitive). Traces must be as short as possible and the two capacitors and resistor must be mounted next to the device as shown below. The capacitor shown between pins 15 and 17, and the one between pins 5 and 7 are the power supply decoupling capacitors. The high frequency output clocks on pins 8 and 9 should have a series termination of $33\ \Omega$ connected close to the pin. Additional improvements will come from keeping all components on the same side of the board, minimizing vias through other signal layers, and routing other signals away from the MK2049. You may also refer to MAN05 for additional suggestions on layout of the crystal section.

The crystal traces should include pads for small capacitors from X1 and X2 to ground; these are used to adjust the stray capacitance of the board to match the crystal load capacitance. The typical telecom reference frequency is accurate to much less than 1 ppm, so the MK2049 may lock and run properly even if the board capacitance is not adjusted with these fixed capacitors. However, ICS MicroClock recommends that the adjustment capacitors be included to minimize the effects of variation in individual crystals, temperature, and aging. The value of these capacitors (typically 0-4 pF) is determined once for a given board layout, using the procedure described in the section titled "Determining the Crystal Frequency Adjustment Capacitors".

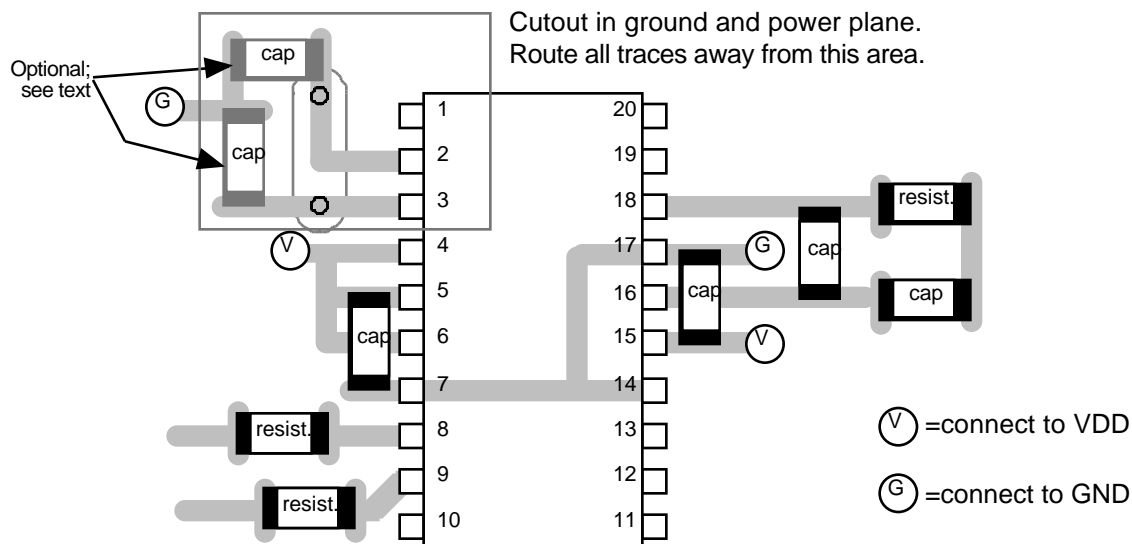


Figure 3. Typical MK2049-02/03 Layout



LAYOUT AND EXTERNAL COMPONENTS (continued)

External Components Selection

The external loop filter should be connected between CAP1 and CAP2 as shown in Figure 4 below, and as close to the chip as possible. High quality ceramic capacitors are recommended. DO NOT use any type of polarized or electrolytic capacitor. Ceramic capacitors should have C0G or NP0 dielectric. Another alternative is the Panasonic PPS polymer dielectric series; their part number for the 0.1 μF cap is ECHU1C104JB5. Avoid high-K dielectrics like Z5U and X7R; these and other ceramics which have piezoelectric properties allow mechanical vibration in the system to increase the output jitter because the mechanical energy is converted directly to voltage noise on the VCO input.

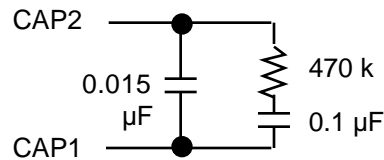


Figure 4. Loop Filter Component Values

Typical component values are shown. Contact the ICS applications department at (408)297-1201 for the recommended values for your application.

Crystal Operation

The MK2049 operates by phase locking the input signal to a VCXO which consists of the special recommended crystal and the integrated VCXO oscillator circuit on the MK2049. To achieve the best performance and reliability, the layout guidelines shown on the previous page must be closely followed.

The frequency of oscillation of a quartz crystal is determined by its cut and by the load capacitors connected to it. The MK2049 has variable load capacitors on-chip which “pull”, or change the frequency of the crystal. External stray capacitance must be kept to a minimum to ensure maximum pullability of the crystal. To achieve this, the layout should use short traces between the MK2049 and the crystal.

For the VCXO to operate correctly, a crystal properly specified and matched to the MK2049-02/03 must be used. For more information, including a list of recommended crystals, refer to application note MAN05.



LAYOUT AND EXTERNAL COMPONENTS (continued)

Determining the Crystal Frequency Adjustment Capacitors

To determine the crystal adjustment capacitor values, you will need a PC board of your final layout, a frequency counter capable of less than 1 ppm resolution and accuracy, two power supplies, and some samples of the crystals which you plan to use in production, along with measured initial accuracy for each crystal at the specified load capacitance, C_L .

To determine the value of the crystal capacitors:

1. Connect VDD of the MK2049 to 5.0 V. Connect pin 18 of the MK2049 to the second power supply. Adjust the voltage on pin 18 to 0.0 V. Measure and record the frequency of the CLK1 or CLK2 output.
2. Adjust the voltage on pin 18 to 3.0 V. Measure and record the frequency of the same output.

To calculate the centering error:

$$\text{Centering error} = 10^6 \left[\frac{(f_{3.0V} - f_{\text{target}}) + (f_{0.0V} - f_{\text{target}})}{f_{\text{target}}} \right] - \text{error}_{\text{xtal}}$$

Where $f_{\text{target}} = 44.736000$ MHz, for example, and $\text{error}_{\text{xtal}} =$ actual initial accuracy (in ppm) of the crystal being measured.

If the centering error is less than ± 15 ppm, no adjustment is needed. If the centering error is more than 15 ppm negative, the PC board has too much stray capacitance and will need to be redone with a new layout to reduce stray capacitance. (The crystal may be re-specified to a lower load capacitance instead. Contact ICS for details.) If the centering error is more than 15 ppm positive, add identical fixed centering capacitors from each crystal pin to ground. The value for each of these caps (in pF) is given by:

$$\text{External Capacitor} = 2 * (\text{centering error}) / (\text{trim sensitivity})$$

Trim sensitivity is a parameter which can be supplied by your crystal vendor. If you do not know the value, assume it is 30 ppm/pF. After any changes, repeat the measurement to verify that the remaining error is acceptably low (less than ± 15 ppm).

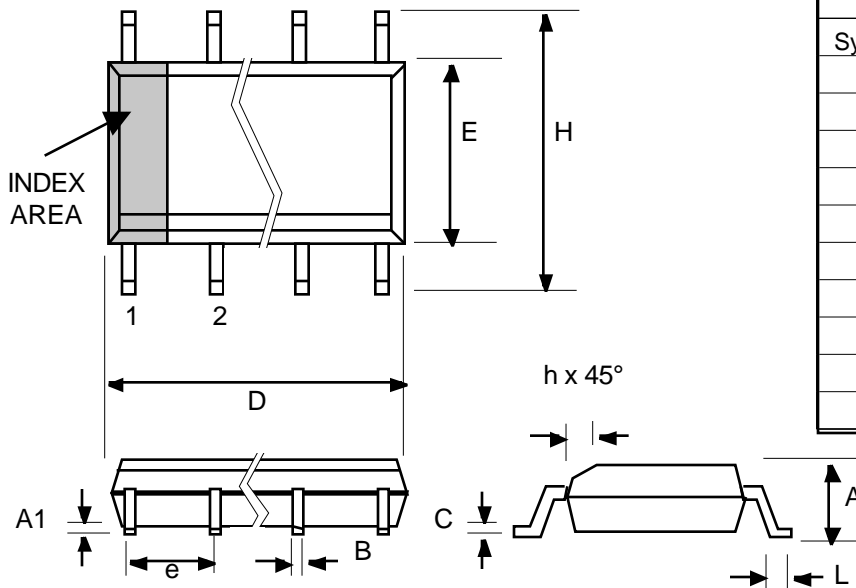
The ICS applications department can perform this procedure on your board. Call us at 408-295-9800, and we will arrange for you to send us a PC board (stuffed or unstuffed) and one of your crystals. We will calculate the value of capacitors needed.



MK2049-02/03 Communications Clock PLLs

Package Outline and Package Dimensions
(For current dimensional specifications, see JEDEC Publication No. 95.)

20 pin SOIC



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	--	0.104	--	2.65
A1	0.0040	--	0.10	--
B	0.013	0.020	0.33	0.51
C	0.007	0.013	0.18	0.33
D	0.496	0.512	12.60	13.00
E	0.291	0.299	7.40	7.60
e	.050 BSC		1.27 BSC	
H	0.394	0.419	10.01	10.64
h	0.01	0.029	0.25	0.74
L	0.016	0.050	0.41	1.27

Ordering Information

Part/Order Number	Marking	Package	Temperature
MK2049-02S	MK2049-02S	20 pin SOIC	0 to 70 °C
MK2049-02STR	MK2049-02S	Add Tape & Reel	0 to 70 °C
MK2049-02SI	MK2049-02SI	20 pin SOIC	-40 to 85 °C
MK2049-02SITR	MK2049-02SI	Add Tape & Reel	-40 to 85 °C
MK2049-03S	MK2049-03S	20 pin SOIC	0 to 70 °C
MK2049-03STR	MK2049-03S	Add Tape & Reel	0 to 70 °C
MK2049-03SI	MK2049-03SI	20 pin SOIC	-40 to 85 °C
MK2049-03SITR	MK2049-03SI	Add Tape & Reel	-40 to 85 °C

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