MP7528

CMOS
Dual Buffered Multiplying 8-Bit
Digital-to-Analog Converter

FEATURES

- **On-Chip Latches for Both DACs**
- **+5 V to +15 V Operation**
- **DACs Matched to 1%**
- **Four Quadrant Multiplication**
- **15 V CMOS Compatible**
- **See MP7529A or MP7529B for Improved Performance**

APPLICATIONS

- **Microprocessor Controlled Gain Circuits**
- **Microprocessor Controlled Attenuator Circuits**
- **Microprocessor Controlled Function Generation**
- **Precision AGC Circuits**
- **Bus Structured Instruments**

GENERAL DESCRIPTION

The MP7528 is a dual 8-bit digital/analog converter designed using EXAR's proven decoded DAC architecture. It features excellent DAC-to-DAC matching and guaranteed monotonicity.

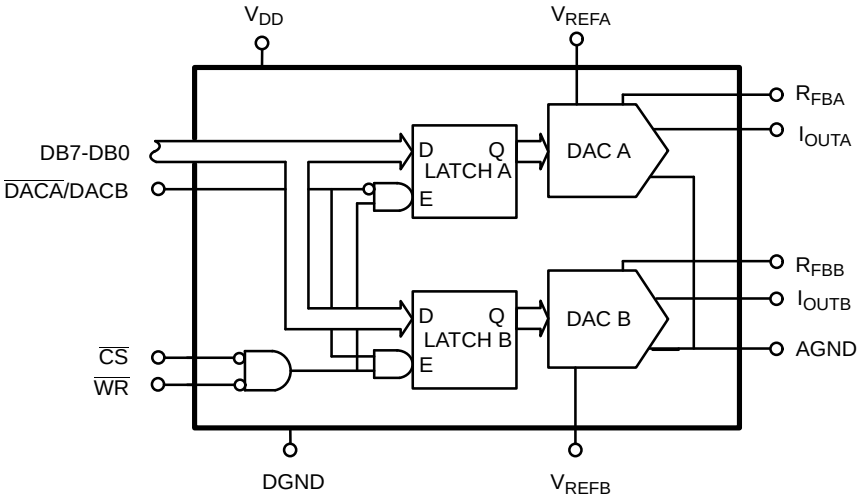
Separate on-chip latches are provided for each DAC to allow easy microprocessor interface.

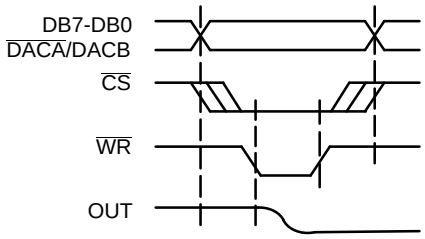
Data is transferred into either of the two DAC data latches via a common 8-bit TTL/CMOS compatible input port. Control input $\overline{DACA}$/DACB determines which DAC is to be loaded. The MP7528's load cycle is similar to the write cycle of a random access memory and the device is bus compatible with most 8-bit microprocessors.

The device operates from a +5V to +15V power supply with only 2 mA of current (maximum).

Both DACs offer excellent four quadrant multiplication characteristics with a separate reference input and feedback resistor for each DAC.

SIMPLIFIED BLOCK AND TIMING DIAGRAM





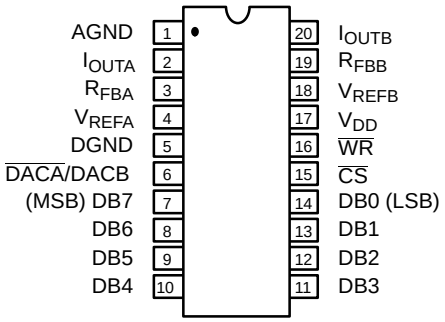
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (LSB)
Plastic Dip	–40 to +85°C	MP7528JN	±1	±1	±6
Plastic Dip	–40 to +85°C	MP7528KN	±1/2	±1	±4
Plastic Dip	–40 to +85°C	MP7528LN	±1/4	±1	±3
SOIC	–40 to +85°C	MP7528JS	±1	±1	±6
SOIC	–40 to +85°C	MP7528KS	±1/2	±1	±4
SOIC	–40 to +85°C	MP7528LS	±1/4	±1	±3
PLCC	–40 to +85°C	MP7528JP	±1	±1	±6
PLCC	–40 to +85°C	MP7528KP	±1/2	±1	±4
PLCC	–40 to +85°C	MP7528LP	±1/4	±1	±3
Ceramic Dip	–40 to +85°C	MP7528AD	±1	±1	±6
Ceramic Dip	–40 to +85°C	MP7528BD	±1/2	±1	±4
Ceramic Dip	–40 to +85°C	MP7528CD	±1/4	±1	±3
Ceramic Dip	–55 to +125°C	MP7528SD*	±1	±1	±6
Ceramic Dip	–55 to +125°C	MP7528TD*	±1/2	±1	±4

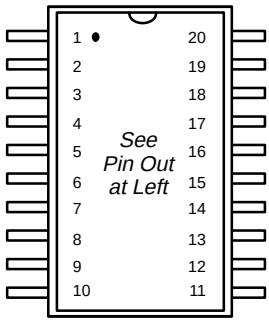
*Contact factory for non-compliant military processing

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions

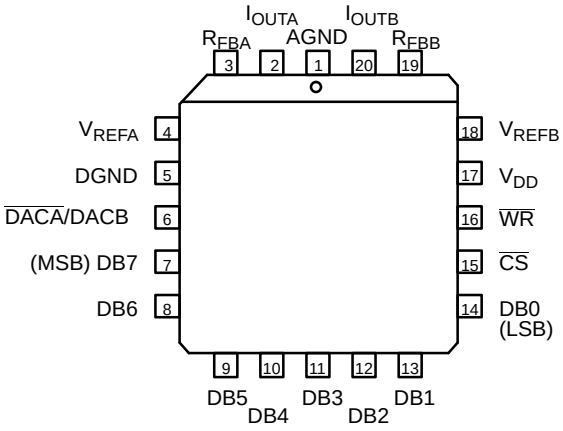


20 Pin CDIP, PDIP (0.300”)
D20, N20



20 Pin SOIC (Jedec, 0.300”)
S20

PIN CONFIGURATIONS (CONT'D)



20 Pin PLCC
P20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	AGND	Analog Ground
2	I_{OUTA}	Current Out DAC A
3	R_{FBA}	Feedback Resistor for DAC A
4	V_{REFA}	Reference Input for DAC A
5	DGND	Digital Ground
6	$\overline{DAC\ A}$/ DAC B	DAC Select
7	DB7 (MSB)	Data Input Bit 7
8	DB6	Data Input Bit 6
9	DB5	Data Input Bit 5
10	DB4	Data Input Bit 4
11	DB3	Data Input Bit 3
12	DB2	Data Input Bit 2
13	DB1	Data Input Bit 1
14	DB0 (LSB)	Data Input Bit 0
15	$\overline{CS}$	Chip Select
16	$\overline{WR}$	Write
17	V_{DD}	Power Supply
18	V_{REFB}	Reference Input for DAC B
19	R_{FBB}	Feedback Resistor for DAC B
20	I_{OUTB}	Current Out DAC B

ELECTRICAL CHARACTERISTICS
(V_{DD} = + 5 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								
Resolution (All Grades)	N	8			8			Bits
Integral Non-Linearity (Relative Accuracy)	INL						LSB	End Point Linearity Spec.
J, A, S				±1		±1		
K, B, T				±1/2		±1/2		
L, C				±1/4		±1/4		
Monotonicity								Guaranteed over temp
Differential Non-Linearity	DNL			±1		±1	LSB	All grades monotonic over full temperature range.
J, A, S								
K, B, T								
L, C								
Gain Error	GE						LSB	Using Internal R_{FB}
J, A, S				±4		±6		Digital Inputs = V_{INH}
K, B, T				±2		±4		
L, C				±1		±3		
Gain Temperature Coefficient[2]	TC_{GE}					±70	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±200		±400	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5% Digital Inputs = V_{INH}
Output Leakage Current (Pin 2)	I_{OUT1}			±50nA		±400nA	nA	Digital Inputs = V_{INL}
Output Leakage Current (Pin 20)	I_{OUT2}			±50nA		±400nA	nA	Digital Inputs = V_{INH}
Input Resistance	V_{REFA}	8		15	8	15	kΩ	TC = –300 ppm/°C max.
	V_{REFB}	8		15	8	15	kΩ	11 kΩ typical
Input Resistance Matching				±1		±1	%	
DYNAMIC PERFORMANCE[2]								R_L=100Ω, C_L=13pF
Harmonic Distortion	THD		–85				dB	V_{IN} = $6V_{RMS}$ @ 1 KHz
Digital Crosstalk	Q		30				nVs	Measured for code transition Z_S to F_{SS}
Channel-to-Channel Isolation	CCI		–77				dB	
AC Feedthrough at I_{OUT1}	F_T		–70			–65	dB	V_{REF} = 10kHz, 20 Vp-p, sinewave
Glitch Energy	Egl		160				nVs	Z_S to F_S Input Change
Propagation Delay	t_{PD}		220			270	ns	From digital input to 90% of final analog output current

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DIGITAL INPUTS[3]								
Logical "1" Voltage	V_{IH}	2.4			2.4		V	
Logical "0" Voltage	V_{IL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}			±1		±10	µA	
Input Capacitance[2]								
Data	C_{IN}			10		10	pF	
Control	C_{IN}			15		15	pF	
ANALOG OUTPUTS[2]								
Output Capacitance								
	C_{OUTA}			120		120	pF	DAC Inputs all 1's
	C_{OUTA}			50		50	pF	DAC Inputs all 0's
	C_{OUTB}			120		120	pF	DAC Inputs all 1's
	C_{OUTB}			50		50	pF	DAC Inputs all 0's
POWER SUPPLY[5]								
Functional Voltage Range[2]	V_{DD}	4.5		15.75	4.5	15.75	V	
Supply Current	I_{DD}			2		2	mA	All digital inputs = 0 V or all = 5 V
				2		2	mA	All digital inputs = V_{IL} or all = V_{IH}
SWITCHING CHARACTERISTICS[4]								
Chip Select to Write Set-Up Time	t_{CS}	200			230		ns	
Chip Select to Write Hold Time	t_{CH}	20			30		ns	
DAC Select to Write Set-Up Time	t_{AS}	200			230		ns	
DAC Select to Write Hold Time	t_{AH}	20			30			
Data Valid to Write Set-Up Time	t_{DS}	110			130		ns	
Data Valid to Write Hold Time	t_{DH}	0			0		ns	
Write Pulse Width	t_{WR}	180			200		ns	

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See timing diagram.
5 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ELECTRICAL CHARACTERISTICS

(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								
Resolution (All Grades)	N	8			8			Bits
Integral Non-Linearity (Relative Accuracy)	INL						LSB	End Point Linearity Spec.
J, A, S				±1		±1		
K, B, T				±1/2		±1/2		
L, C				±1/4		±1/4		
Monotonicity								Guaranteed over temp
Differential Non-Linearity	DNL						LSB	All grades monotonic over full temperature range.
J, A, S				±1		±1		
K, B, T				±1		±1		
L, C				±1		±1		
Gain Error	GE						LSB	Using Internal R_{FB}
J, A, S				±4		±5		Digital Inputs = V_{INH}
K, B, T				±2		±3		
L, C				±1		±1		
Gain Temperature Coefficient[2]	TC_{GE}					±35	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±100		±200	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5% Digital Inputs = V_{INH}
Output Leakage Current (Pin 2)	I_{OUT1}			±50nA		±200nA	nA	Digital Inputs = V_{INL}
Output Leakage Current (Pin 20)	I_{OUT2}			±50nA		±200nA	nA	Digital Inputs = V_{INH}
Input Resistance	V_{REFA}	8		15	8	15	kΩ	TC = –300 ppm/°C max.
	V_{REFB}	8		15	8	15	kΩ	11 kΩ typical
Input Resistance Matching				±1		±1	%	
DYNAMIC PERFORMANCE[2]								R_L=100Ω, C_L=13pF
Harmonic Distortion	THD		–85				dB	V_{IN} = 6V_{RMS} @ 1 KHz
Digital Crosstalk	Q		60				nVs	Measured for code transition ZS to F_S
Channel-to-Channel Isolation	CCI		–77				dB	
AC Feedthrough at I_{OUT1}	F_T		–70		–65		dB	V_{REF} = 10kHz, 20 Vp-p, sinewave
Glitch Energy	Egl		440				nVs	ZS to F_S Input Change
Propagation Delay	t_{PD}			80		100	ns	From 50% of digital input to 90% of final analog output current
DIGITAL INPUTS[3]								
Logical “1” Voltage	V_{IH}	13.5			13.5		V	
Logical “0” Voltage	V_{IL}			1.5		1.5	V	
Input Leakage Current	I_{ILKG}			±1		±10	µA	
Input Capacitance[2]								
Data	C_{IN}			10		10	pF	
Control	C_{IN}			15		15	pF	

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
ANALOG OUTPUTS[2]								
Output Capacitance								
	C_{OUTA}			120		120	pF	DAC Inputs all 1's
	C_{OUTA}			50		50	pF	DAC Inputs all 0's
	C_{OUTB}			120		120	pF	DAC Inputs all 1's
	C_{OUTB}			50		50	pF	DAC Inputs all 0's
POWER SUPPLY[5]								
Functional Voltage Range[2]	V_{DD}	4.5		15.75	4.5	15.75	V	
Supply Current	I_{DD}			2		2	mA	All digital inputs = 0 V or all = 5 V
				2		2	mA	All digital inputs = V_{IL} or all = V_{IH}
SWITCHING CHARACTERISTICS								
Chip Select to Write Set-Up Time	t_{CS}	60			80		ns	
Chip Select to Write Hold Time	t_{CH}	10			15		ns	
DAC Select to Write Set-Up Time	t_{AS}	60			80		ns	
DAC Select to Write Hold Time	t_{AH}	10			15		ns	
Data Valid to Write Set-Up Time	t_{DS}	30			40		ns	
Data Valid to Write Hold Time	t_{DH}	0			0		ns	
Write Pulse Width	t_{WR}	60			80		ns	

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See timing diagram.
5 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... +17 V
AGND to DGND ..... ±1 V
(Functionality Guaranteed ±0.5 V)
Digital Input Voltage to DGND ..... –0.5 V, +17 V
V_{PIN2}, V_{PIN20} to GND ..... –0.5 V, +17 V
V_{REFA}, V_{REFB} to GND ..... ±25
V_{RFBA}, V_{RFBB} to GND ..... ±25 V
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 secs.) ..... +300°C
Package Power Dissipation Rating to 75°C
CDIP, PDIP, SOIC, PLCC 900mW
Derates above 75°C ..... 12mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies.
3 GND refers to AGND and DGND.

INTERFACE LOGIC INFORMATION

DAC Selection: Both DAC latches share a common 8-bit input port. The control input $\overline{DACA}$/DACB selects which DAC can accept data from the input port.

Mode Selection: Inputs $\overline{CS}$ and $\overline{WR}$ control the operating mode of the selected DAC. See Mode Selection Table below:

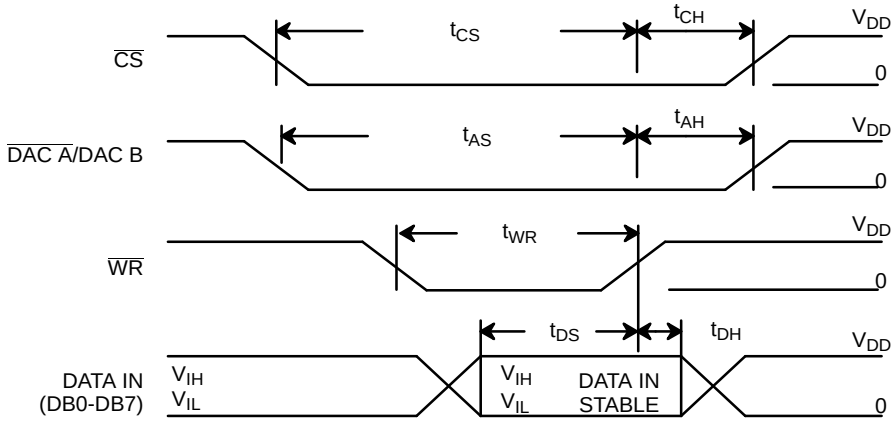
Write Mode: When $\overline{CS}$ and $\overline{WR}$ are both low the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to activity on DB0-DB7.

Hold Mode: The selected DAC latch retains the data which was present on DB0-DB7 just prior to $\overline{CS}$ and $\overline{WR}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

$\overline{DAC\ A}$/DAC B	$\overline{CS}$	$\overline{WR}$	DAC A	DAC B
L	L	L	Write	Hold
H	L	L	Hold	Write
X	H	X	Hold	Hold
X	X	H	Hold	Hold

L = LOW state, H = HIGH state, X = Don't care state

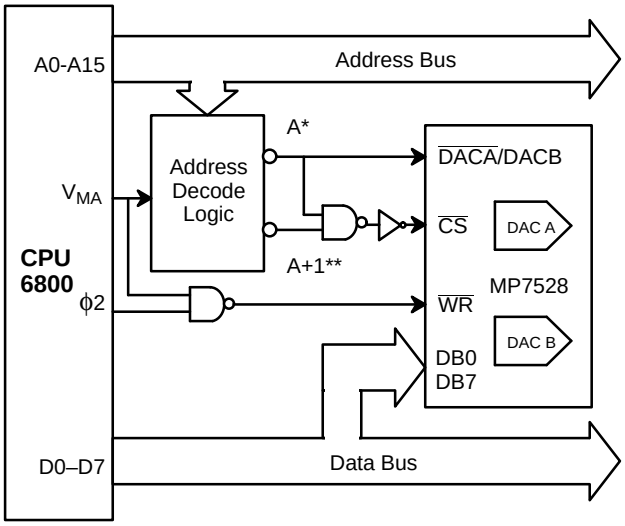
Table 1. Mode Selection Table



NOTES:
1. All input signal rise and fall times measured from 10% to 90% of V_{DD}.
   V_{DD} = +5 V, $t_r = t_f$ = 20 ns
   V_{DD} = +15 V, $t_r = t_f$ = 40 ns
2. Timing measurement reference level is $V_{IH} + V_{IL} / 2$

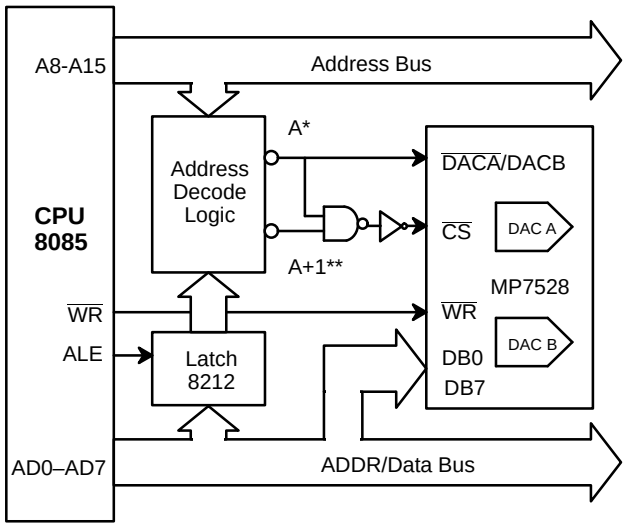
Figure 1. Write Cycle Timing Diagram

MICROPROCESSOR INTERFACE



Analog circuitry has been omitted for clarity
*A = Decoded 7528 DAC A Address
**A + 1 = Decoded 7528 DAC B Address

Figure 2. MP7528 Dual DAC to 6800 CPU Interface

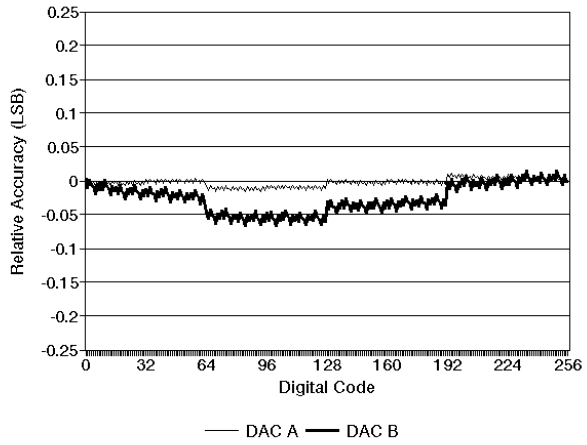


Analog circuitry has been omitted for clarity
*A = Decoded 7528 DAC A Address
**A + 1 = Decoded 7528 DAC B Address

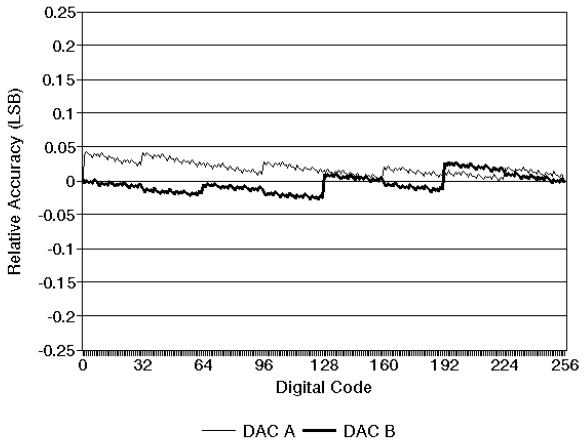
NOTE:
8085 instruction SHLD (store H & L direct) can update both DACS with data from H and L registers

Figure 3. MP7528 Dual DAC to 8085 CPU Interface

PERFORMANCE CHARACTERISTICS



Graph 1. Relative Accuracy vs. Digital Code 5 V



Graph 2. Relative Accuracy vs. Digital Code 15 V

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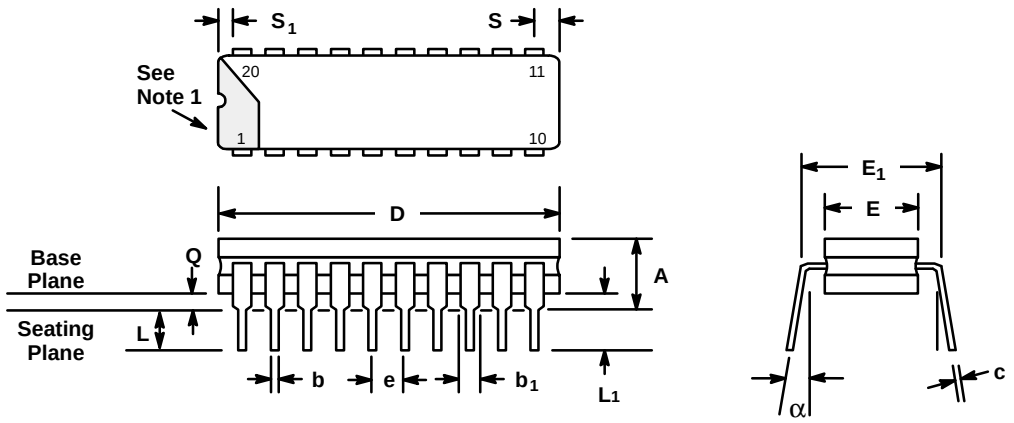
20 LEAD CERAMIC DUAL-IN-LINE
(300 MIL CDIP)
D20

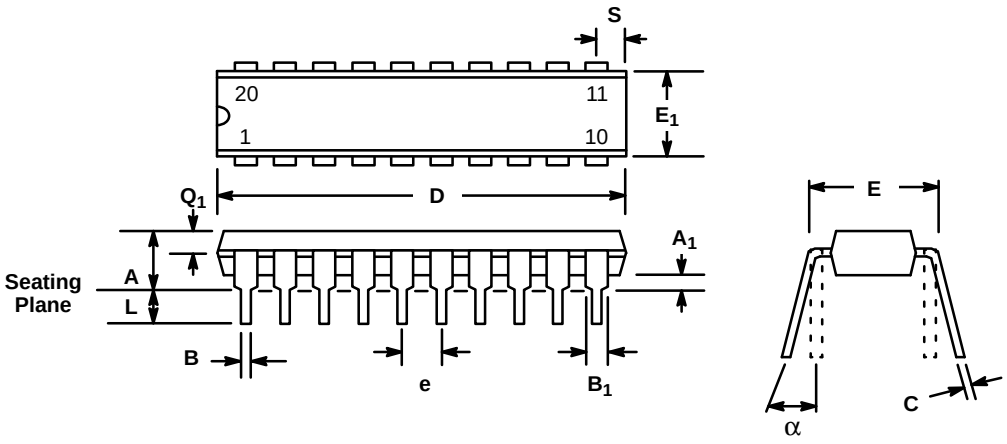


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.356	0.584	—
b_1	0.038	0.065	0.965	1.65	2
c	0.008	0.015	0.203	0.381	—
D	—	1.060	—	26.92	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.070	0.381	1.78	3
S	—	0.080	—	2.03	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. This is measured to outside of lead, not center.

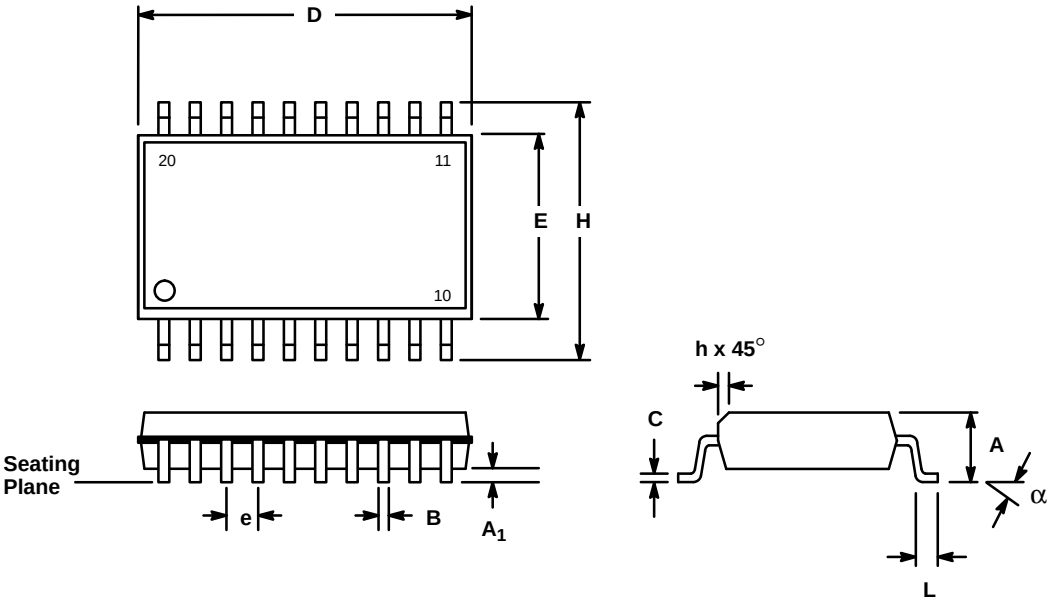
20 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
N20



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	0.945	1.060	24.0	26.92
E	0.295	0.325	7.49	8.26
E_1	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.040	0.080	1.02	2.03

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

20 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)
S20



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.097	0.104	2.464	2.642
A_1	0.0050	0.0115	0.127	0.292
B	0.014	0.019	0.356	0.483
C	0.0091	0.0125	0.231	0.318
D	0.500	0.510	12.70	12.95
E	0.292	0.299	7.42	7.59
e	0.050 BSC		1.27 BSC	
H	0.400	0.410	10.16	10.41
h	0.010	0.016	0.254	0.406
L	0.016	0.035	0.406	0.889
α	0°	8°	0°	8°

Notes

Notes

NOTICE

EXAR Corporation reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. EXAR Corporation assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contains here in are only for illustration purposes and may vary depending upon a user's specific application. While the information in this publication has been carefully checked; no responsibility, however, is assumed for inaccuracies.

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