

MSP430x13x, MSP430x14x, MSP430x14x1 MIXED SIGNAL MICROCONTROLLER

SLAS272F – JULY 2000 – REVISED JUNE 2004

- Low Supply-Voltage Range, 1.8 V . . . 3.6 V
- Ultralow-Power Consumption:
 - Active Mode: 280 μ A at 1 MHz, 2.2V
 - Standby Mode: 1.6 μ A
 - Off Mode (RAM Retention): 0.1 μ A
- Five Power-Saving Modes
- Wake-Up From Standby Mode in less than 6 μ s
- 16-Bit RISC Architecture, 125-ns Instruction Cycle Time
- 12-Bit A/D Converter With Internal Reference, Sample-and-Hold and Autoscan Feature
- 16-Bit Timer_B With Seven Capture/Compare-With-Shadow Registers
- 16-Bit Timer_A With Three Capture/Compare Registers
- On-Chip Comparator
- Serial Onboard Programming, No External Programming Voltage Needed
- Programmable Code Protection by Security Fuse
- Serial Communication Interface (USART), Functions as Asynchronous UART or Synchronous SPI Interface
 - Two USARTs (USART0, USART1) — MSP430x14x(1) Devices
 - One USART (USART0) — MSP430x13x Devices
- Family Members Include:
 - MSP430F133:
8KB+256B Flash Memory, 256B RAM
 - MSP430F135:
16KB+256B Flash Memory, 512B RAM
 - MSP430F147, MSP430F1471†:
32KB+256B Flash Memory, 1KB RAM
 - MSP430F148, MSP430F1481†:
48KB+256B Flash Memory, 2KB RAM
 - MSP430F149, MSP430F1491†:
60KB+256B Flash Memory, 2KB RAM
- Available in 64-Pin Quad Flat Pack (QFP) and 64-pin QFN
- For Complete Module Descriptions, See the *MSP430x1xx Family User's Guide*, Literature Number SLAU049

† The MSP430F14x1 devices are identical to the MSP430F14x devices with the exception that the ADC12 module is not implemented.

description

The Texas Instruments MSP430 family of ultralow-power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that attribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6 μ s.

The MSP430x13x and the MSP430x14x(1) series are microcontroller configurations with two built-in 16-bit timers, a fast 12-bit A/D converter (not implemented on the MSP430F14x1 devices), one or two universal serial synchronous/asynchronous communication interfaces (USART), and 48 I/O pins.

Typical applications include sensor systems that capture analog signals, convert them to digital values, and process and transmit the data to a host system. The timers make the configurations ideal for industrial control applications such as ripple counters, digital motor control, EE-meters, hand-held meters, etc. The hardware multiplier enhances the performance and offers a broad code and hardware-compatible family solution.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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MSP430x13x, MSP430x14x, MSP430x14x1 MIXED SIGNAL MICROCONTROLLER

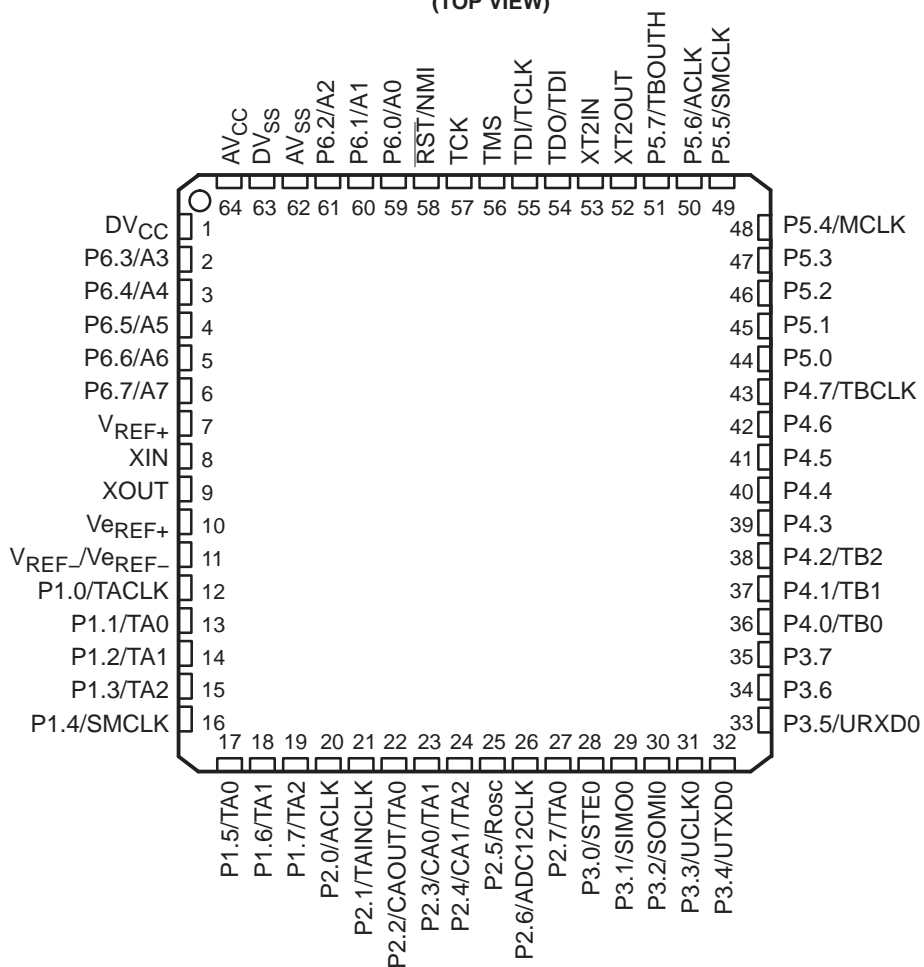
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AVAILABLE OPTIONS

T _A	PACKAGED DEVICES		
	PLASTIC 64-PIN QFP (PM)	PLASTIC 64-PIN QFP (PAG)	PLASTIC 64-PIN QFN (RTD)
-40°C to 85°C	MSP430F133IPM MSP430F135IPM MSP430F147IPM MSP430F1471IPM MSP430F148IPM MSP430F1481IPM MSP430F149IPM MSP430F1491IPM	MSP430F133IPAG MSP430F135IPAG MSP430F147IPAG MSP430F148IPAG MSP430F149IPAG	MSP430F133IRTD MSP430F135IRTD MSP430F147IRTD MSP430F1471IRTD MSP430F148IRTD MSP430F1481IRTD MSP430F149IRTD MSP430F1491IRTD

pin designation, MSP430F133, MSP430F135

PM, PAG, RTD PACKAGE (TOP VIEW)

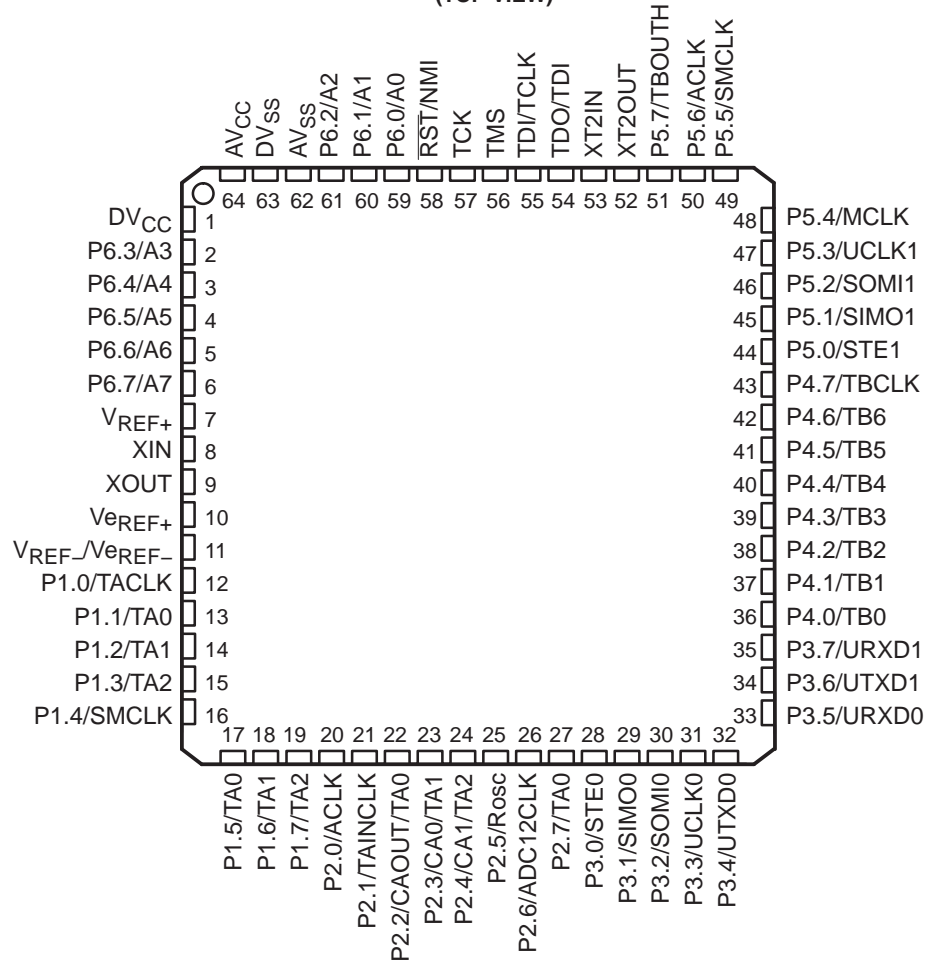


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pin designation, MSP430F147, MSP430F148, MSP430F149

PM, PAG, RTD PACKAGE
(TOP VIEW)

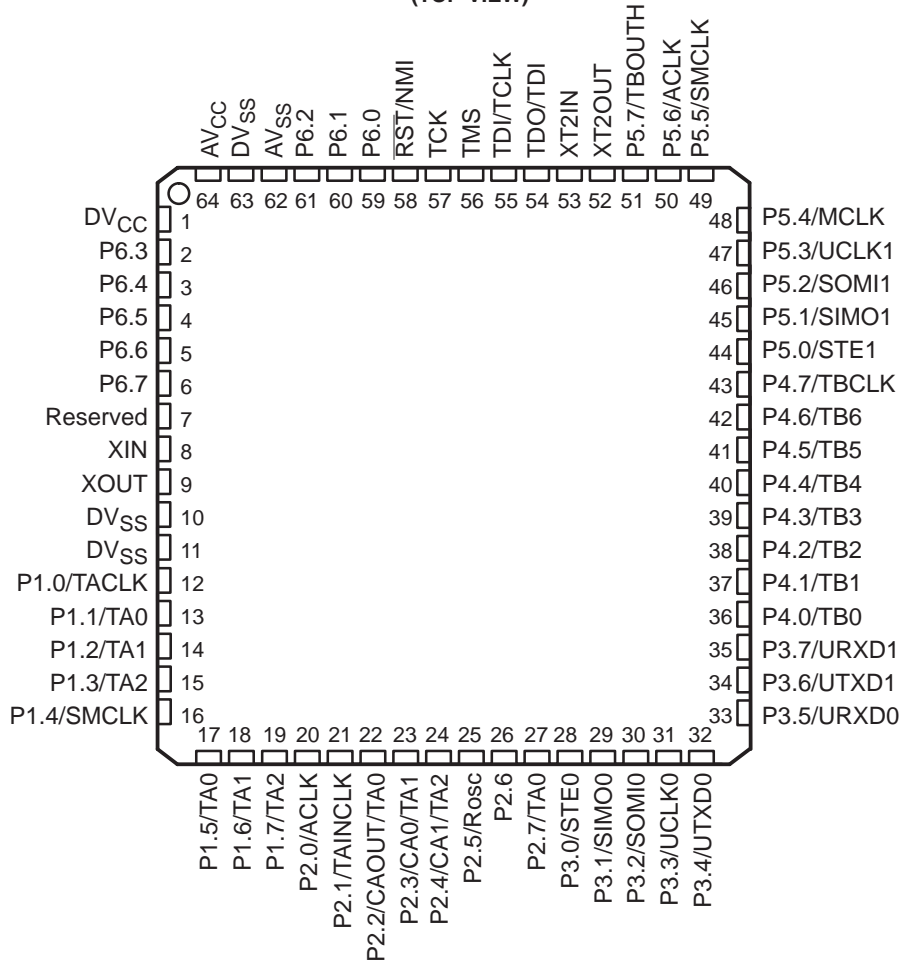


MSP430x13x, MSP430x14x, MSP430x14x1 MIXED SIGNAL MICROCONTROLLER

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pin designation, MSP430F1471, MSP430F1481, MSP430F1491

PM, RTD PACKAGE
(TOP VIEW)

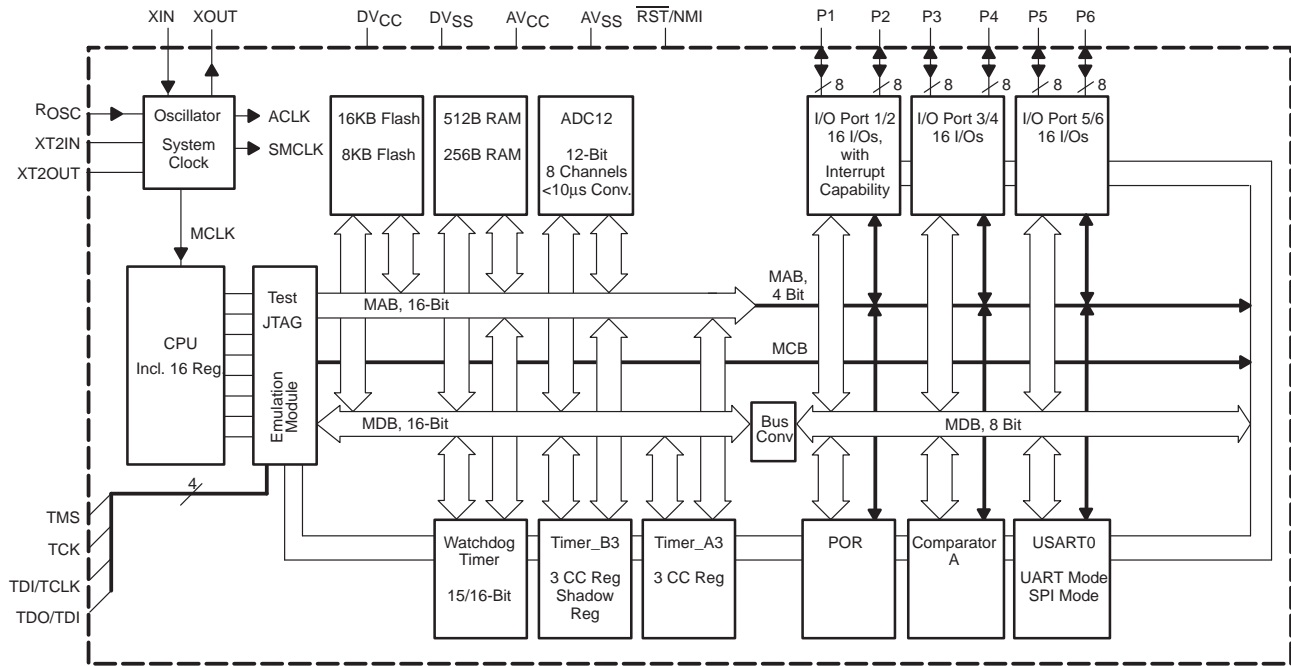


MSP430x13x, MSP430x14x, MSP430x14x1 MIXED SIGNAL MICROCONTROLLER

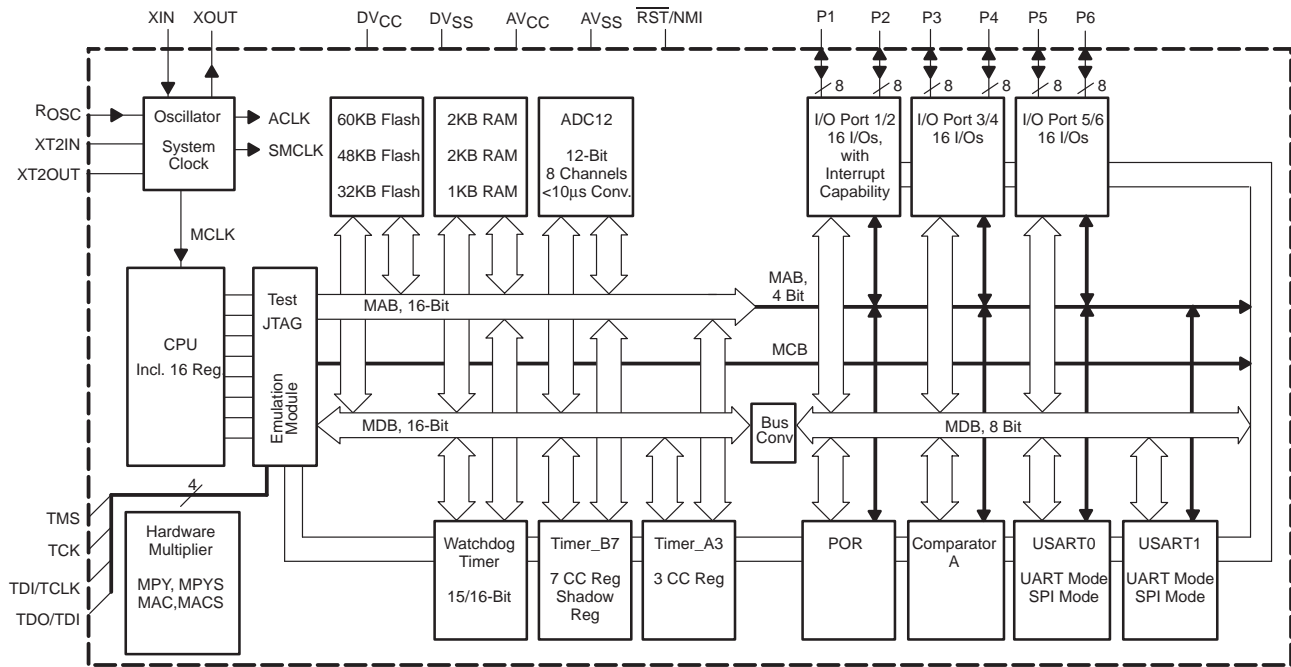
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functional block diagrams

MSP430x13x



MSP430x14x

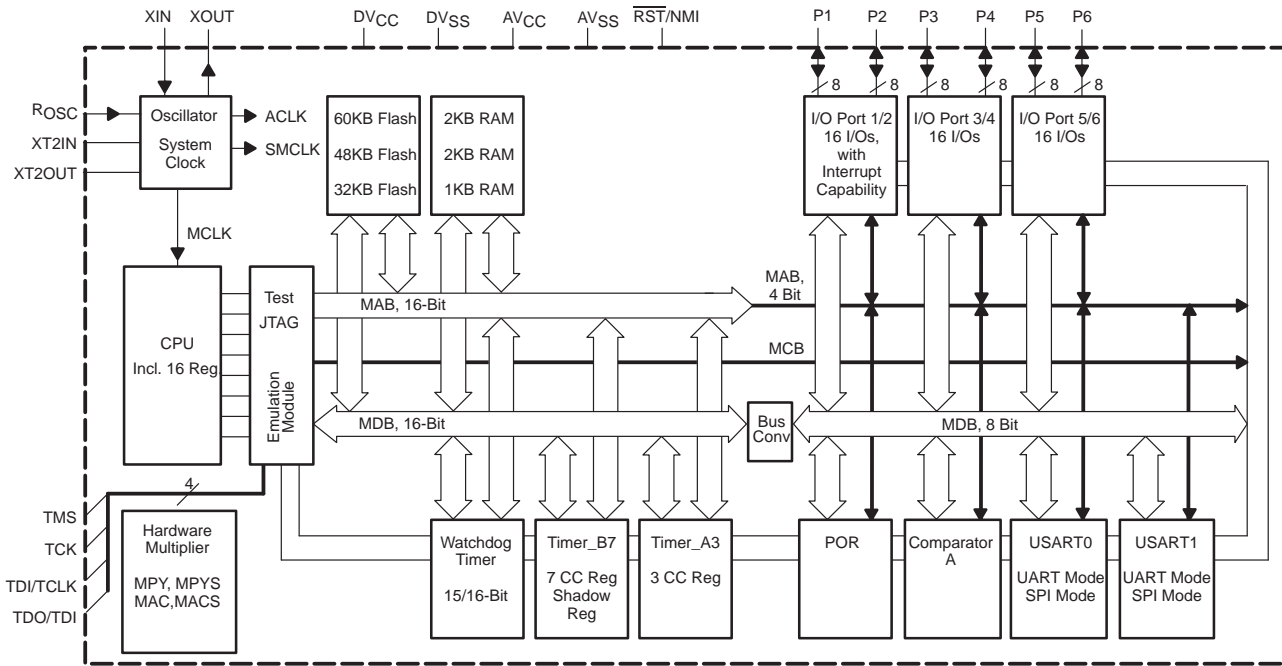


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functional block diagrams (continued)

MSP430x14x1



MSP430x13x, MSP430x14x, MSP430x14x1 MIXED SIGNAL MICROCONTROLLER

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Terminal Functions

MSP430x13x, MSP430x14x

TERMINAL NAME	NO.	I/O	DESCRIPTION
AV _{CC}	64		Analog supply voltage, positive terminal. Supplies the analog portion of the analog-to-digital converter.
AV _{SS}	62		Analog supply voltage, negative terminal. Supplies the analog portion of the analog-to-digital converter.
DV _{CC}	1		Digital supply voltage, positive terminal. Supplies all digital parts.
DV _{SS}	63		Digital supply voltage, negative terminal. Supplies all digital parts.
P1.0/TACLK	12	I/O	General-purpose digital I/O pin/Timer_A, clock signal TACLK input
P1.1/TA0	13	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI0A input, compare: Out0 output/BSL transmit
P1.2/TA1	14	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI1A input, compare: Out1 output
P1.3/TA2	15	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI2A input, compare: Out2 output
P1.4/SMCLK	16	I/O	General-purpose digital I/O pin/SMCLK signal output
P1.5/TA0	17	I/O	General-purpose digital I/O pin/Timer_A, compare: Out0 output
P1.6/TA1	18	I/O	General-purpose digital I/O pin/Timer_A, compare: Out1 output
P1.7/TA2	19	I/O	General-purpose digital I/O pin/Timer_A, compare: Out2 output/
P2.0/ACLK	20	I/O	General-purpose digital I/O pin/ACLK output
P2.1/TAINCLK	21	I/O	General-purpose digital I/O pin/Timer_A, clock signal at INCLK
P2.2/CAOUT/TA0	22	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI0B input/Comparator_A output/BSL receive
P2.3/CA0/TA1	23	I/O	General-purpose digital I/O pin/Timer_A, compare: Out1 output/Comparator_A input
P2.4/CA1/TA2	24	I/O	General-purpose digital I/O pin/Timer_A, compare: Out2 output/Comparator_A input
P2.5/R _{OSC}	25	I/O	General-purpose digital I/O pin/input for external resistor defining the DCO nominal frequency
P2.6/ADC12CLK	26	I/O	General-purpose digital I/O pin/conversion clock – 12-bit ADC
P2.7/TA0	27	I/O	General-purpose digital I/O pin/Timer_A, compare: Out0 output
P3.0/STE0	28	I/O	General-purpose digital I/O pin/slave transmit enable – USART0/SPI mode
P3.1/SIMO0	29	I/O	General-purpose digital I/O pin/slave in/master out of USART0/SPI mode
P3.2/SOMI0	30	I/O	General-purpose digital I/O pin/slave out/master in of USART0/SPI mode
P3.3/UCLK0	31	I/O	General-purpose digital I/O/USART0 clock: external input – UART or SPI mode, output – SPI mode
P3.4/UTXD0	32	I/O	General-purpose digital I/O pin/transmit data out – USART0/UART mode
P3.5/URXD0	33	I/O	General-purpose digital I/O pin/receive data in – USART0/UART mode
P3.6/UTXD1†	34	I/O	General-purpose digital I/O pin/transmit data out – USART1/UART mode
P3.7/URXD1†	35	I/O	General-purpose digital I/O pin/receive data in – USART1/UART mode
P4.0/TB0	36	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI0A or CCI0B input, compare: Out0 output
P4.1/TB1	37	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI1A or CCI1B input, compare: Out1 output
P4.2/TB2	38	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI2A or CCI2B input, compare: Out2 output
P4.3/TB3†	39	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI3A or CCI3B input, compare: Out3 output
P4.4/TB4†	40	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI4A or CCI4B input, compare: Out4 output
P4.5/TB5†	41	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI5A or CCI5B input, compare: Out5 output
P4.6/TB6†	42	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI6A or CCI6B input, compare: Out6 output
P4.7/TBCLK	43	I/O	General-purpose digital I/O pin/Timer_B, clock signal TBCLK input
P5.0/STE1†	44	I/O	General-purpose digital I/O pin/slave transmit enable – USART1/SPI mode
P5.1/SIMO1†	45	I/O	General-purpose digital I/O pin/slave in/master out of USART1/SPI mode
P5.2/SOMI1†	46	I/O	General-purpose digital I/O pin/slave out/master in of USART1/SPI mode
P5.3/UCLK1†	47	I/O	General-purpose digital I/O pin/USART1 clock: external input – UART or SPI mode, output – SPI mode
P5.4/MCLK	48	I/O	General-purpose digital I/O pin/main system clock MCLK output
P5.5/SMCLK	49	I/O	General-purpose digital I/O pin/submain system clock SMCLK output

† 14x devices only



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Terminal Functions (Continued)

MSP430x13x, MSP430x14x (continued)

TERMINAL NAME	NO.	I/O	DESCRIPTION
P5.6/ACLK	50	I/O	General-purpose digital I/O pin/auxiliary clock ACLK output
P5.7/TBOUTH	51	I/O	General-purpose digital I/O pin/switch all PWM digital output ports to high impedance – Timer_B7: TB0 to TB6
P6.0/A0	59	I/O	General-purpose digital I/O pin/analog input a0 – 12-bit ADC
P6.1/A1	60	I/O	General-purpose digital I/O pin/analog input a1 – 12-bit ADC
P6.2/A2	61	I/O	General-purpose digital I/O pin/analog input a2 – 12-bit ADC
P6.3/A3	2	I/O	General-purpose digital I/O pin/analog input a3 – 12-bit ADC
P6.4/A4	3	I/O	General-purpose digital I/O pin/analog input a4 – 12-bit ADC
P6.5/A5	4	I/O	General-purpose digital I/O pin/analog input a5 – 12-bit ADC
P6.6/A6	5	I/O	General-purpose digital I/O pin/analog input a6 – 12-bit ADC
P6.7/A7	6	I/O	General-purpose digital I/O pin/analog input a7 – 12-bit ADC
RST/NMI	58	I	Reset input, nonmaskable interrupt input port, or bootstrap loader start (in Flash devices).
TCK	57	I	Test clock. TCK is the clock input port for device programming test and bootstrap loader start (in Flash devices).
TDI/TCLK	55	I	Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.
TDO/TDI	54	I/O	Test data output port. TDO/TDI data output or programming data input terminal
TMS	56	I	Test mode select. TMS is used as an input port for device programming and test.
V _{REF+}	10	I	Input for an external reference voltage to the ADC
V _{REF+}	7	O	Output of positive terminal of the reference voltage in the ADC
V _{REF-} /V _{REF-}	11	I	Negative terminal for the ADC's reference voltage for both sources, the internal reference voltage, or an external applied reference voltage
XIN	8	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	O	Output terminal of crystal oscillator XT1
XT2IN	53	I	Input port for crystal oscillator XT2. Only standard crystals can be connected.
XT2OUT	52	O	Output terminal of crystal oscillator XT2
QFN Pad	NA	NA	QFN package pad connection to DV _{SS} recommended.

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Terminal Functions

MSP430x14x1

TERMINAL NAME	NO.	I/O	DESCRIPTION
AV _{CC}	64		Analog supply voltage, positive terminal.
AV _{SS}	62		Analog supply voltage, negative terminal.
DV _{CC}	1		Digital supply voltage, positive terminal. Supplies all digital parts.
DV _{SS}	63		Digital supply voltage, negative terminal. Supplies all digital parts.
P1.0/TACLK	12	I/O	General-purpose digital I/O pin/Timer_A, clock signal TACLK input
P1.1/TA0	13	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI0A input, compare: Out0 output/BSL transmit
P1.2/TA1	14	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI1A input, compare: Out1 output
P1.3/TA2	15	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI2A input, compare: Out2 output
P1.4/SMCLK	16	I/O	General-purpose digital I/O pin/SMCLK signal output
P1.5/TA0	17	I/O	General-purpose digital I/O pin/Timer_A, compare: Out0 output
P1.6/TA1	18	I/O	General-purpose digital I/O pin/Timer_A, compare: Out1 output
P1.7/TA2	19	I/O	General-purpose digital I/O pin/Timer_A, compare: Out2 output
P2.0/ACLK	20	I/O	General-purpose digital I/O pin/ACLK output
P2.1/TAINCLK	21	I/O	General-purpose digital I/O pin/Timer_A, clock signal at INCLK
P2.2/CAOUT/TA0	22	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI0B input/Comparator_A output/BSL receive
P2.3/CA0/TA1	23	I/O	General-purpose digital I/O pin/Timer_A, compare: Out1 output/Comparator_A input
P2.4/CA1/TA2	24	I/O	General-purpose digital I/O pin/Timer_A, compare: Out2 output/Comparator_A input
P2.5/R _{OSC}	25	I/O	General-purpose digital I/O pin/input for external resistor defining the DCO nominal frequency
P2.6	26	I/O	General-purpose digital I/O pin
P2.7/TA0	27	I/O	General-purpose digital I/O pin/Timer_A, compare: Out0 output
P3.0/STE0	28	I/O	General-purpose digital I/O pin/slave transmit enable – USART0/SPI mode
P3.1/SIMO0	29	I/O	General-purpose digital I/O pin/slave in/master out of USART0/SPI mode
P3.2/SOMI0	30	I/O	General-purpose digital I/O pin/slave out/master in of USART0/SPI mode
P3.3/UCLK0	31	I/O	General-purpose digital I/O/USART0 clock: external input – UART or SPI mode, output – SPI mode
P3.4/UTXD0	32	I/O	General-purpose digital I/O pin/transmit data out – USART0/UART mode
P3.5/URXD0	33	I/O	General-purpose digital I/O pin/receive data in – USART0/UART mode
P3.6/UTXD1	34	I/O	General-purpose digital I/O pin/transmit data out – USART1/UART mode
P3.7/URXD1	35	I/O	General-purpose digital I/O pin/receive data in – USART1/UART mode
P4.0/TB0	36	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI0A or CCI0B input, compare: Out0 output
P4.1/TB1	37	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI1A or CCI1B input, compare: Out1 output
P4.2/TB2	38	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI2A or CCI2B input, compare: Out2 output
P4.3/TB3	39	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI3A or CCI3B input, compare: Out3 output
P4.4/TB4	40	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI4A or CCI4B input, compare: Out4 output
P4.5/TB5	41	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI5A or CCI5B input, compare: Out5 output
P4.6/TB6	42	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI6A or CCI6B input, compare: Out6 output
P4.7/TBCLK	43	I/O	General-purpose digital I/O pin/Timer_B, clock signal TBCLK input
P5.0/STE1	44	I/O	General-purpose digital I/O pin/slave transmit enable – USART1/SPI mode
P5.1/SIMO1	45	I/O	General-purpose digital I/O pin/slave in/master out of USART1/SPI mode
P5.2/SOMI1	46	I/O	General-purpose digital I/O pin/slave out/master in of USART1/SPI mode
P5.3/UCLK1	47	I/O	General-purpose digital I/O pin/USART1 clock: external input – UART or SPI mode, output – SPI mode
P5.4/MCLK	48	I/O	General-purpose digital I/O pin/main system clock MCLK output
P5.5/SMCLK	49	I/O	General-purpose digital I/O pin/submain system clock SMCLK output



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Terminal Functions (Continued)

MSP430x14x1 (continued)

TERMINAL NAME	NO.	I/O	DESCRIPTION
P5.6/ACLK	50	I/O	General-purpose digital I/O pin/auxiliary clock ACLK output
P5.7/TBOUTH	51	I/O	General-purpose digital I/O pin/switch all PWM digital output ports to high impedance – Timer_B7: TB0 to TB6
P6.0	59	I/O	General-purpose digital I/O pin
P6.1	60	I/O	General-purpose digital I/O pin
P6.2	61	I/O	General-purpose digital I/O pin
P6.3	2	I/O	General-purpose digital I/O pin
P6.4	3	I/O	General-purpose digital I/O pin
P6.5	4	I/O	General-purpose digital I/O pin
P6.6	5	I/O	General-purpose digital I/O pin
P6.7	6	I/O	General-purpose digital I/O pin
RST/NMI	58	I	Reset input, nonmaskable interrupt input port, or bootstrap loader start (in Flash devices).
TCK	57	I	Test clock. TCK is the clock input port for device programming test and bootstrap loader start (in Flash devices).
TDI/TCLK	55	I	Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.
TDO/TDI	54	I/O	Test data output port. TDO/TDI data output or programming data input terminal
TMS	56	I	Test mode select. TMS is used as an input port for device programming and test.
DV _{SS}	10	I	Connect to DV _{SS}
Reserved	7		Reserved, do not connect externally
DV _{SS}	11	I	Connect to DV _{SS}
XIN	8	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	O	Output terminal of crystal oscillator XT1
XT2IN	53	I	Input port for crystal oscillator XT2. Only standard crystals can be connected.
XT2OUT	52	O	Output terminal of crystal oscillator XT2
QFN Pad	NA	NA	QFN package pad connection to DV _{SS} recommended.



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short-form description

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

Program Counter	PC/R0
Stack Pointer	SP/R1
Status Register	SR/CG1/R2
Constant Generator	CG2/R3
General-Purpose Register	R4
General-Purpose Register	R5
General-Purpose Register	R6
General-Purpose Register	R7
General-Purpose Register	R8
General-Purpose Register	R9
General-Purpose Register	R10
General-Purpose Register	R11
General-Purpose Register	R12
General-Purpose Register	R13
General-Purpose Register	R14
General-Purpose Register	R15

instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; the address modes are listed in Table 2.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g. ADD R4,R5	R4 + R5 ----> R5
Single operands, destination only	e.g. CALL R8	PC -->(TOS), R8--> PC
Relative jump, un/conditional	e.g. JNE	Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	●	●	MOV Rs,Rd	MOV R10,R11	R10 --> R11
Indexed	●	●	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)--> M(6+R6)
Symbolic (PC relative)	●	●	MOV EDE,TONI		M(EDE) --> M(TONI)
Absolute	●	●	MOV &MEM,&TCDAT		M(MEM) --> M(TCDAT)
Indirect	●		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) --> M(Tab+R6)
Indirect autoincrement	●		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) --> R11 R10 + 2--> R10
Immediate	●		MOV #X,TONI	MOV #45,TONI	#45 --> M(TONI)

NOTE: S = source D = destination

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operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode AM;
 - All clocks are active
- Low-power mode 0 (LPM0);
 - CPU is disabled
ACLK and SMCLK remain active. MCLK is disabled
- Low-power mode 1 (LPM1);
 - CPU is disabled
ACLK and SMCLK remain active. MCLK is disabled
DCO's dc-generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2);
 - CPU is disabled
MCLK and SMCLK are disabled
DCO's dc-generator remains enabled
ACLK remains active
- Low-power mode 3 (LPM3);
 - CPU is disabled
MCLK and SMCLK are disabled
DCO's dc-generator is disabled
ACLK remains active
- Low-power mode 4 (LPM4);
 - CPU is disabled
ACLK is disabled
MCLK and SMCLK are disabled
DCO's dc-generator is disabled
Crystal oscillator is stopped



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interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range 0FFFFh – 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External Reset Watchdog Flash memory	WDTIFG KEYV (see Note 1)	Reset	0FFFEh	15, highest
NMI Oscillator Fault Flash memory access violation	NMIIFG (see Notes 1 & 4) OFIFG (see Notes 1 & 4) ACCVIFG (see Notes 1 & 4)	(Non)maskable (Non)maskable (Non)maskable	0FFFCh	14
Timer_B7 (see Note 5)	TBCCR0 CCIFG (see Note 2)	Maskable	0FFFAh	13
Timer_B7 (see Note 5)	TBCCR1 to 6 CCIFGs, TBIFG (see Notes 1 & 2)	Maskable	0FFF8h	12
Comparator_A	CAIFG	Maskable	0FFF6h	11
Watchdog timer	WDTIFG	Maskable	0FFF4h	10
USART0 receive	URXIFG0	Maskable	0FFF2h	9
USART0 transmit	UTXIFG0	Maskable	0FFF0h	8
ADC12 (see Note 6)	ADC12IFG (see Notes 1 & 2)	Maskable	0FEEh	7
Timer_A3	TACCR0 CCIFG (see Note 2)	Maskable	0FFECh	6
Timer_A3	TACCR1 CCIFG, TACCR2 CCIFG, TAIFG (see Notes 1 & 2)	Maskable	0FEEAh	5
I/O port P1 (eight flags)	P1IFG.0 to P1IFG.7 (see Notes 1 & 2)	Maskable	0FFE8h	4
USART1 receive	URXIFG1	Maskable	0FFE6h	3
USART1 transmit	UTXIFG1		0FFE4h	2
I/O port P2 (eight flags)	P2IFG.0 to P2IFG.7 (see Notes 1 & 2)	Maskable	0FFE2h	1
			0FFE0h	0, lowest

- NOTES:
- Multiple source flags
 - Interrupt flags are located in the module.
 - Nonmaskable: neither the individual nor the general interrupt-enable bit will disable an interrupt event.
 - (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable can not disable it.
 - Timer_B7 in MSP430x14x(1) family has 7 CCRs; Timer_B3 in MSP430x13x family has 3 CCRs. In Timer_B3 there are only interrupt flags TBCCR0, 1, and 2 CCIFGs and the interrupt-enable bits TBCCTL0, 1, and 2 CCIEs.
 - ADC12 is not implemented on the 14x1 devices.

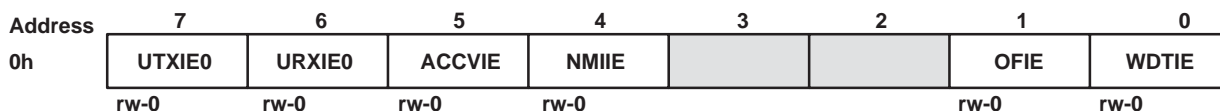
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special function registers

Most interrupt and module-enable bits are collected in the lowest address space. Special-function register bits not allocated to a functional purpose are not physically present in the device. This arrangement provides simple software access.

interrupt enable 1 and 2



WDTIE: Watchdog-timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode.

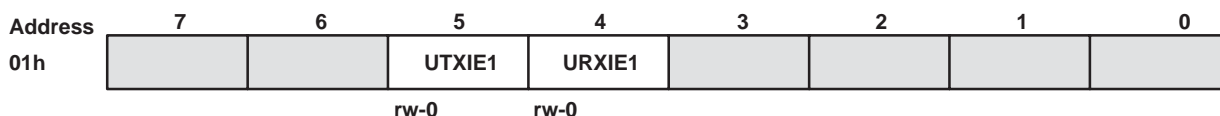
OFIE: Oscillator-fault-interrupt enable

NMIIE: Nonmaskable-interrupt enable

ACCVIE: Flash access violation interrupt enable

URXIE0: USART0: UART and SPI receive-interrupt enable

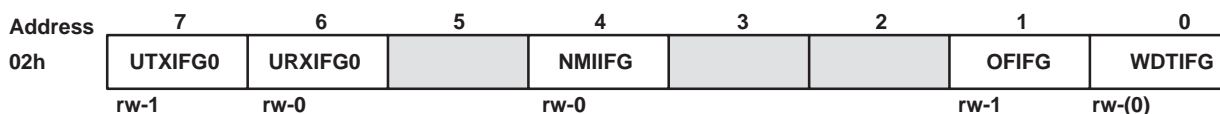
UTXIE0: USART0: UART and SPI transmit-interrupt enable



URXIE1: USART1: UART and SPI receive-interrupt enable

UTXIE1: USART1: UART and SPI transmit-interrupt enable

interrupt flag register 1 and 2



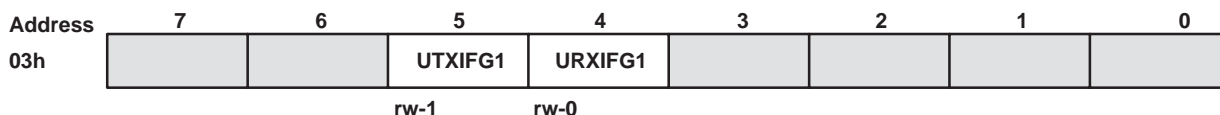
WDTIFG: Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on V_{CC} power up or a reset condition at the \overline{RST}/NMI pin in reset mode.

OFIFG: Flag set on oscillator fault

NMIIFG: Set via \overline{RST}/NMI pin

URXIFG0: USART0: UART and SPI receive flag

UTXIFG0: USART0: UART and SPI transmit flag

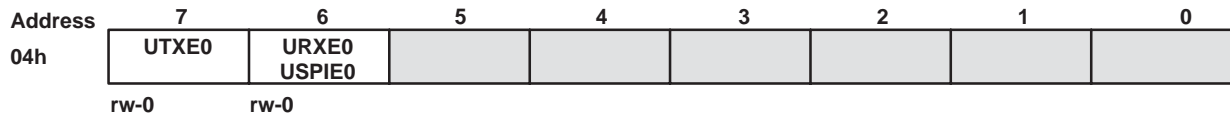


URXIFG1: USART1: UART and SPI receive flag

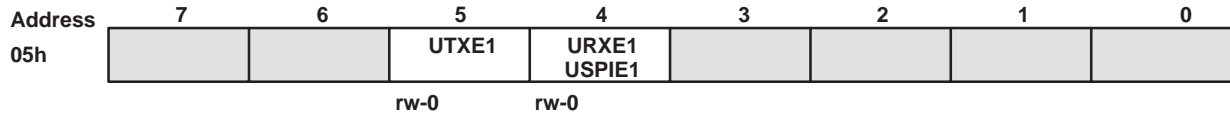
UTXIFG1: USART1: UART and SPI transmit flag



module enable registers 1 and 2



URXE0: USART0: UART receive enable
 UTXE0: USART0: UART transmit enable
 USPIE0: USART0: SPI (synchronous peripheral interface) transmit and receive enable



URXE1: USART1: UART receive enable
 UTXE1: USART1: UART transmit enable
 USPIE1: USART1: SPI (synchronous peripheral interface) transmit and receive enable

Legend: rw: Bit Can Be Read and Written
 rw-0: Bit Can Be Read and Written. It Is Reset by PUC.
 SFR Bit Not Present in Device

memory organization

		MSP430F133	MSP430F135	MSP430F147 MSP430F1471	MSP430F148 MSP430F1481	MSP430F149 MSP430F1491
Memory	Size	8KB	16KB	32KB	48KB	60KB
	Main: interrupt vector	0FFFFh – 0FFE0h	0FFFFh – 0FFE0h	0FFFFh – 0FFE0h	0FFFFh – 0FFE0h	0FFFFh – 0FFE0h
Main: code memory	Flash	0FFFFh – 0E000h	0FFFFh – 0C000h	0FFFFh – 08000h	0FFFFh – 04000h	0FFFFh – 01100h
	Information memory					
Boot memory	Size	256 Byte	256 Byte	256 Byte	256 Byte	256 Byte
	Flash	010FFh – 01000h	010FFh – 01000h	010FFh – 01000h	010FFh – 01000h	010FFh – 01000h
RAM	Size	1KB	1KB	1KB	1KB	1KB
	ROM	0FFFh – 0C00h	0FFFh – 0C00h	0FFFh – 0C00h	0FFFh – 0C00h	0FFFh – 0C00h
Peripherals	Size	256 Byte	512 Byte	1KB	2KB	2KB
	16-bit	02FFh – 0200h	03FFh – 0200h	05FFh – 0200h	09FFh – 0200h	09FFh – 0200h
	8-bit					
SFR	16-bit	01FFh – 0100h	01FFh – 0100h	01FFh – 0100h	01FFh – 0100h	01FFh – 0100h
	8-bit	0FFh – 010h	0FFh – 010h	0FFh – 010h	0FFh – 010h	0FFh – 010h
	8-bit	0Fh – 00h	0Fh – 00h	0Fh – 00h	0Fh – 00h	0Fh – 00h

bootstrap loader (BSL)

The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the Application report *Features of the MSP430 Bootstrap Loader*, Literature Number SLAA089.

BSL Function	PM, PAG & RTD Package Pins
Data Transmit	13 - P1.1
Data Receive	22 - P2.2

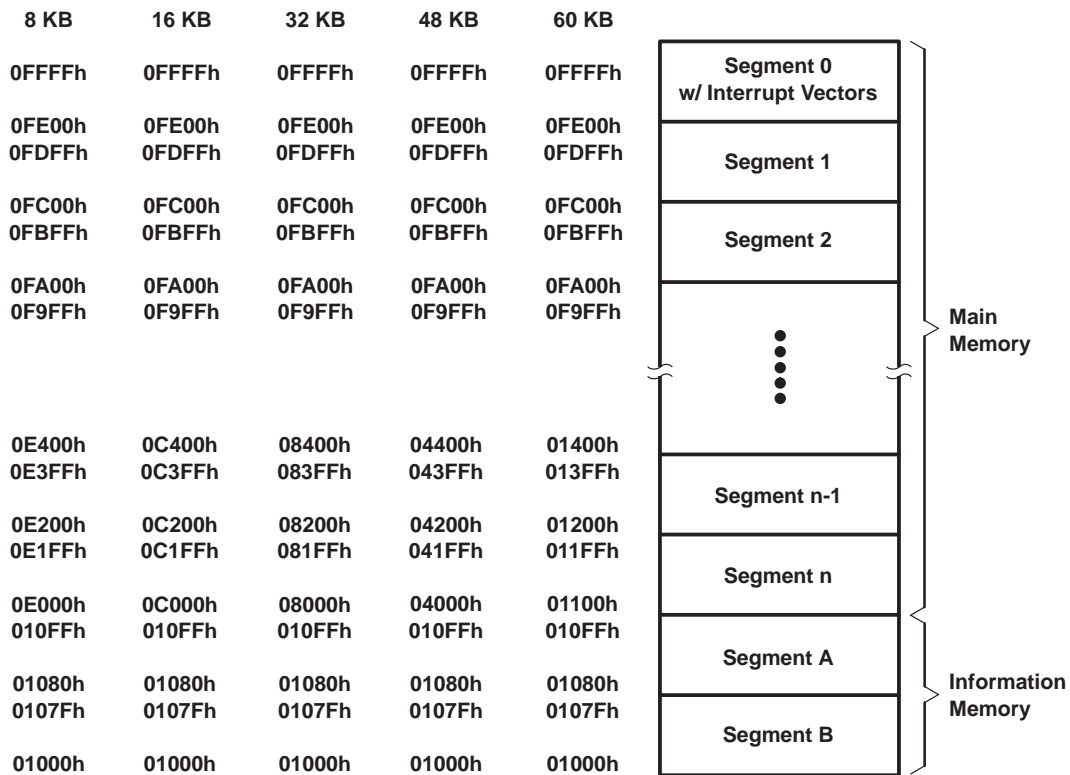
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flash memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0–n. Segments A and B are also called *information memory*.
- New devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory prior to the first use.



peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, see the *MSP430x1xx Family User's Guide*, literature number SLAU049.

digital I/O

There are six 8-bit I/O ports implemented—ports P1 through P6:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.

oscillator and system clock

The clock system in the MSP430x13x and MSP43x14x(1) family of devices is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal digitally-controlled oscillator (DCO) and a high frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low-power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6 μ s. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high frequency crystal.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

watchdog timer

The primary function of the watchdog timer (WDT) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

hardware multiplier (MSP430x14x and MSP430x14x1 Only)

The multiplication operation is supported by a dedicated peripheral module. The module performs 16×16 , 16×8 , 8×16 , and 8×8 bit operations. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

USART0

The MSP430x13x and the MSP430x14x(1) have one hardware universal synchronous/asynchronous receive transmit (USART0) peripheral module that is used for serial data communication. The USART supports synchronous SPI (3 or 4 pin) and asynchronous UART communication protocols, using double-buffered transmit and receive channels.

USART1 (MSP430x14x and MSP430x14x1 Only)

The MSP430x14x(1) has a second hardware universal synchronous/asynchronous receive transmit (USART1) peripheral module that is used for serial data communication. The USART supports synchronous SPI (3 or 4 pin) and asynchronous UART communication protocols, using double-buffered transmit and receive channels. Operation of USART1 is identical to USART0.

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comparator_A

The primary function of the comparator_A module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

ADC12 (Not implemented in the MSP430x14x1)

The ADC12 module supports fast, 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator and a 16 word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer_A3 Signal Connections					
Input Pin Number	Device Input Signal	Module Input Name	Module Block	Module Output Signal	Output Pin Number
12 - P1.0	TACLK	TACLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
21 - P2.1	TAINCLK	INCLK			
13 - P1.1	TA0	CCI0A	CCR0	TA0	13 - P1.1
22 - P2.2	TA0	CCI0B			17 - P1.5
	DVSS	GND			27 - P2.7
	DVCC	VCC			
14 - P1.2	TA1	CCI1A	CCR1	TA1	14 - P1.2
	CAOUT (internal)	CCI1B			18 - P1.6
	DVSS	GND			23 - P2.3
	DVCC	VCC			ADC12 (internal)
15 - P1.3	TA2	CCI2A	CCR2	TA2	15 - P1.3
	ACLK (internal)	CCI2B			19 - P1.7
	DVSS	GND			24 - P2.4
	DVCC	VCC			

timer_B3 (MSP430x13x Only)

Timer_B3 is a 16-bit timer/counter with three capture/compare registers. Timer_B3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.



timer_B7 (MSP430x14x and MSP430x14x1 Only)

Timer_B7 is a 16-bit timer/counter with seven capture/compare registers. Timer_B7 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B7 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer_B3/B7 Signal Connections†					
Input Pin Number	Device Input Signal	Module Input Name	Module Block	Module Output Signal	Output Pin Number
43 - P4.7	TBCLK	TBCLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
43 - P4.7	TBCLK	INCLK			
36 - P4.0	TB0	CCI0A	CCR0	TB0	36 - P4.0
36 - P4.0	TB0	CCI0B			ADC12 (internal)
	DVSS	GND			
	DVCC	VCC			
37 - P4.1	TB1	CCI1A	CCR1	TB1	37 - P4.1
37 - P4.1	TB1	CCI1B			ADC12 (internal)
	DVSS	GND			
	DVCC	VCC			
38 - P4.2	TB2	CCI2A	CCR2	TB2	38 - P4.2
38 - P4.2	TB2	CCI2B			
	DVSS	GND			
	DVCC	VCC			
39 - P4.3	TB3	CCI3A	CCR3	TB3	39 - P4.3
39 - P4.3	TB3	CCI3B			
	DVSS	GND			
	DVCC	VCC			
40 - P4.4	TB4	CCI4A	CCR4	TB4	40 - P4.4
40 - P4.4	TB4	CCI4B			
	DVSS	GND			
	DVCC	VCC			
41 - P4.5	TB5	CCI5A	CCR5	TB5	41 - P4.5
41 - P4.5	TB5	CCI5B			
	DVSS	GND			
	DVCC	VCC			
42 - P4.6	TB6	CCI6A	CCR6	TB6	42 - P4.6
	ACLK (internal)	CCI6B			
	DVSS	GND			
	DVCC	VCC			

† Timer_B3 implements three capture/compare blocks (CCR0, CCR1 and CCR2 only).

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peripheral file map

PERIPHERALS WITH WORD ACCESS			
Watchdog	Watchdog Timer control	WDTCTL	0120h
Timer_B7/ Timer_B3 (see Note 1)	Timer_B interrupt vector	TBIV	011Eh
	Timer_B control	TBCTL	0180h
	Capture/compare control 0	TBCCTL0	0182h
	Capture/compare control 1	TBCCTL1	0184h
	Capture/compare control 2	TBCCTL2	0186h
	Capture/compare control 3	TBCCTL3	0188h
	Capture/compare control 4	TBCCTL4	018Ah
	Capture/compare control 5	TBCCTL5	018Ch
	Capture/compare control 6	TBCCTL6	018Eh
	Timer_B register	TBR	0190h
	Capture/compare register 0	TBCCR0	0192h
	Capture/compare register 1	TBCCR1	0194h
	Capture/compare register 2	TBCCR2	0196h
	Capture/compare register 3	TBCCR3	0198h
Capture/compare register 4	TBCCR4	019Ah	
Capture/compare register 5	TBCCR5	019Ch	
Capture/compare register 6	TBCCR6	019Eh	
Timer_A3	Timer_A interrupt vector	TAIV	012Eh
	Timer_A control	TACTL	0160h
	Capture/compare control 0	TACCTL0	0162h
	Capture/compare control 1	TACCTL1	0164h
	Capture/compare control 2	TACCTL2	0166h
	Reserved		0168h
	Reserved		016Ah
	Reserved		016Ch
	Reserved		016Eh
	Timer_A register	TAR	0170h
	Capture/compare register 0	TACCR0	0172h
	Capture/compare register 1	TACCR1	0174h
	Capture/compare register 2	TACCR2	0176h
	Reserved		0178h
Reserved		017Ah	
Reserved		017Ch	
Reserved		017Eh	
Hardware Multiplier (MSP430x14x and MSP430x14x1 only)	Sum extend	SUMEXT	013Eh
	Result high word	RESHI	013Ch
	Result low word	RESLO	013Ah
	Second operand	OP2	0138h
	Multiply signed +accumulate/operand1	MACS	0136h
	Multiply+accumulate/operand1	MAC	0134h
	Multiply signed/operand1	MPYS	0132h
Multiply unsigned/operand1	MPY	0130h	

NOTE 1: Timer_B7 in MSP430x14x(1) family has 7 CCRs, Timer_B3 in MSP430x13x family has 3 CCRs.



peripheral file map (continued)

PERIPHERALS WITH WORD ACCESS (CONTINUED)			
Flash	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
ADC12 (Not implemented in the MSP430x14x1)	Conversion memory 15	ADC12MEM15	015Eh
	Conversion memory 14	ADC12MEM14	015Ch
	Conversion memory 13	ADC12MEM13	015Ah
	Conversion memory 12	ADC12MEM12	0158h
	Conversion memory 11	ADC12MEM11	0156h
	Conversion memory 10	ADC12MEM10	0154h
	Conversion memory 9	ADC12MEM9	0152h
	Conversion memory 8	ADC12MEM8	0150h
	Conversion memory 7	ADC12MEM7	014Eh
	Conversion memory 6	ADC12MEM6	014Ch
	Conversion memory 5	ADC12MEM5	014Ah
	Conversion memory 4	ADC12MEM4	0148h
	Conversion memory 3	ADC12MEM3	0146h
	Conversion memory 2	ADC12MEM2	0144h
	Conversion memory 1	ADC12MEM1	0142h
	Conversion memory 0	ADC12MEM0	0140h
	Interrupt-vector-word register	ADC12IV	01A8h
	Inerrupt-enable register	ADC12IE	01A6h
	Inerrupt-flag register	ADC12IFG	01A4h
	Control register 1	ADC12CTL1	01A2h
	Control register 0	ADC12CTL0	01A0h
	ADC memory-control register15	ADC12MCTL15	08Fh
	ADC memory-control register14	ADC12MCTL14	08Eh
	ADC memory-control register13	ADC12MCTL13	08Dh
	ADC memory-control register12	ADC12MCTL12	08Ch
	ADC memory-control register11	ADC12MCTL11	08Bh
	ADC memory-control register10	ADC12MCTL10	08Ah
	ADC memory-control register9	ADC12MCTL9	089h
	ADC memory-control register8	ADC12MCTL8	088h
	ADC memory-control register7	ADC12MCTL7	087h
	ADC memory-control register6	ADC12MCTL6	086h
	ADC memory-control register5	ADC12MCTL5	085h
	ADC memory-control register4	ADC12MCTL4	084h
ADC memory-control register3	ADC12MCTL3	083h	
ADC memory-control register2	ADC12MCTL2	082h	
ADC memory-control register1	ADC12MCTL1	081h	
ADC memory-control register0	ADC12MCTL0	080h	

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peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS			
USART1 (MSP430x14x and MSP430x14x1 only)	Transmit buffer	U1TXBUF	07Fh
	Receive buffer	U1RXBUF	07Eh
	Baud rate	U1BR1	07Dh
	Baud rate	U1BR0	07Ch
	Modulation control	U1MCTL	07Bh
	Receive control	U1RCTL	07Ah
	Transmit control	U1TCTL	079h
	USART control	U1CTL	078h
USART0	Transmit buffer	U0TXBUF	077h
	Receive buffer	U0RXBUF	076h
	Baud rate	U0BR1	075h
	Baud rate	U0BR0	074h
	Modulation control	U0MCTL	073h
	Receive control	U0RCTL	072h
	Transmit control	U0TCTL	071h
	USART control	U0CTL	070h
Comparator_A	Comparator_A port disable	CAPD	05Bh
	Comparator_A control2	CACTL2	05Ah
	Comparator_A control1	CACTL1	059h
Basic Clock	Basic clock system control2	BCSCTL2	058h
	Basic clock system control1	BCSCTL1	057h
	DCO clock frequency control	DCOCTL	056h
Port P6	Port P6 selection	P6SEL	037h
	Port P6 direction	P6DIR	036h
	Port P6 output	P6OUT	035h
	Port P6 input	P6IN	034h
Port P5	Port P5 selection	P5SEL	033h
	Port P5 direction	P5DIR	032h
	Port P5 output	P5OUT	031h
	Port P5 input	P5IN	030h
Port P4	Port P4 selection	P4SEL	01Fh
	Port P4 direction	P4DIR	01Eh
	Port P4 output	P4OUT	01Dh
	Port P4 input	P4IN	01Ch
Port P3	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt-edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h



peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS (CONTINUED)			
Port P1	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt-edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special Functions	SFR module enable 2	ME2	005h
	SFR module enable 1	ME1	004h
	SFR interrupt flag2	IFG2	003h
	SFR interrupt flag1	IFG1	002h
	SFR interrupt enable2	IE2	001h
	SFR interrupt enable1	IE1	000h

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Voltage applied at V_{CC} to V_{SS}	-0.3 V to + 4.1 V
Voltage applied to any pin (see Note)	-0.3 V to $V_{CC}+0.3$ V
Diode current at any device terminal	± 2 mA
Storage temperature (unprogrammed device)	-55°C to 150°C
Storage temperature (programmed device)	-40°C to 85°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltages referenced to V_{SS} . The JTAG fuse-blow voltage, V_{FB} , is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.

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recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNITS	
Supply voltage during program execution, V_{CC} ($AV_{CC} = DV_{CC} = V_{CC}$)		1.8		3.6	V	
Supply voltage during flash memory programming, V_{CC} ($AV_{CC} = DV_{CC} = V_{CC}$)		2.7		3.6	V	
Supply voltage, V_{SS} ($AV_{SS} = DV_{SS} = V_{SS}$)		0.0		0.0	V	
Operating free-air temperature range, T_A		-40		85	°C	
LFXT1 crystal frequency, $f_{(LFXT1)}$ (see Notes 1 and 2)	LF selected, XTS=0	Watch crystal		32768	Hz	
	XT1 selected, XTS=1	Ceramic resonator		450	8000	kHz
	XT1 selected, XTS=1	Crystal		1000	8000	kHz
XT2 crystal frequency, $f_{(XT2)}$	Ceramic resonator		450	8000	kHz	
	Crystal		1000	8000		
Processor frequency (signal MCLK), $f_{(System)}$	$V_{CC} = 1.8\text{ V}$		DC	4.15	MHz	
	$V_{CC} = 3.6\text{ V}$		DC	8		

- NOTES: 1. In LF mode, the LFXT1 oscillator requires a watch crystal. A 5.1MΩ resistor from XOUT to V_{SS} is recommended when $V_{CC} < 2.5\text{ V}$. In XT1 mode, the LFXT1 and XT2 oscillators accept a ceramic resonator or crystal up to 4.15MHz at $V_{CC} \geq 2.2\text{ V}$. In XT1 mode, the LFXT1 and XT2 oscillators accept a ceramic resonator or crystal up to 8MHz at $V_{CC} \geq 2.8\text{ V}$.
2. In LF mode, the LFXT1 oscillator requires a watch crystal. In XT1 mode, LFXT1 accepts a ceramic resonator or a crystal.

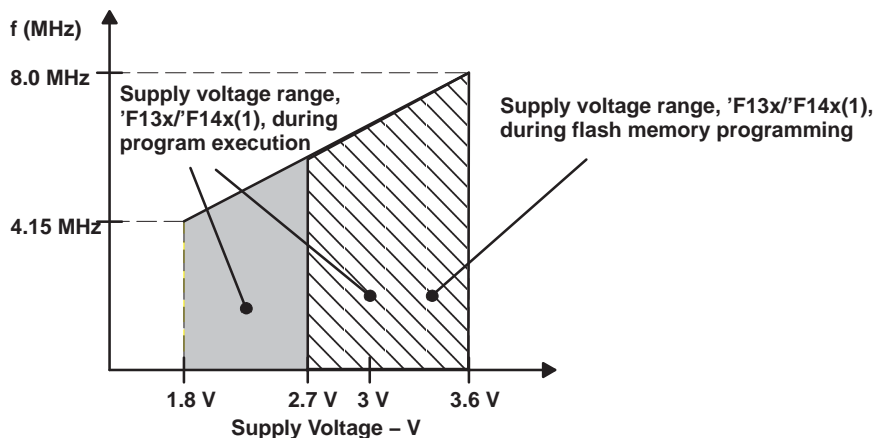


Figure 1. Frequency vs Supply Voltage, MSP430F13x or MSP430F14x(1)

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

supply current into AV_{CC} + DV_{CC} excluding external current

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{(AM)}$	Active mode, (see Note 1) $f(MCLK) = f(SMCLK) = 1$ MHz, $f(ACLK) = 32,768$ Hz XTS=0, SELM=(0,1)	$T_A = -40^{\circ}\text{C}$ to 85°C	$V_{CC} = 2.2$ V	280	350	μA	
			$V_{CC} = 3$ V	420	560		
$I_{(AM)}$	Active mode, (see Note 1) $f(MCLK) = f(SMCLK) = 4$ 096 Hz, $f(ACLK) = 4,096$ Hz XTS=0, SELM=(0,1) XTS=0, SELM=3	$T_A = -40^{\circ}\text{C}$ to 85°C	$V_{CC} = 2.2$ V	2.5	7	μA	
			$V_{CC} = 3$ V	9	20		
$I_{(LPM0)}$	Low-power mode, (LPM0) (see Note 1)	$T_A = -40^{\circ}\text{C}$ to 85°C	$V_{CC} = 2.2$ V	32	45	μA	
			$V_{CC} = 3$ V	55	70		
$I_{(LPM2)}$	Low-power mode, (LPM2), $f(MCLK) = f(SMCLK) = 0$ MHz, $f(ACLK) = 32,768$ Hz, SCG0 = 0	$T_A = -40^{\circ}\text{C}$ to 85°C	$V_{CC} = 2.2$ V	11	14	μA	
			$V_{CC} = 3$ V	17	22		
$I_{(LPM3)}$	Low-power mode, (LPM3) $f(MCLK) = f(SMCLK) = 0$ MHz, $f(ACLK) = 32,768$ Hz, SCG0 = 1 (see Note 2)	$T_A = -40^{\circ}\text{C}$	$V_{CC} = 2.2$ V	0.8	1.5	μA	
				$T_A = 25^{\circ}\text{C}$	0.9		1.5
				$T_A = 85^{\circ}\text{C}$	1.6		2.8
		$T_A = -40^{\circ}\text{C}$	$V_{CC} = 3$ V	1.8	2.2	μA	
				$T_A = 25^{\circ}\text{C}$	1.6		1.9
				$T_A = 85^{\circ}\text{C}$	2.3		3.9
$I_{(LPM4)}$	Low-power mode, (LPM4) $f(MCLK) = 0$ MHz, $f(SMCLK) = 0$ MHz, $f(ACLK) = 0$ Hz, SCG0 = 1	$T_A = -40^{\circ}\text{C}$	$V_{CC} = 2.2$ V	0.1	0.5	μA	
				$T_A = 25^{\circ}\text{C}$	0.1		0.5
				$T_A = 85^{\circ}\text{C}$	0.8		2.5
		$T_A = -40^{\circ}\text{C}$	$V_{CC} = 3$ V	0.1	0.5	μA	
				$T_A = 25^{\circ}\text{C}$	0.1		0.5
				$T_A = 85^{\circ}\text{C}$	0.8		2.5

- NOTES: 1. Timer_B is clocked by $f(DCOCLK) = 1$ MHz. All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.
2. Timer_B is clocked by $f(ACLK) = 32,768$ Hz. All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current. The current consumption in LPM2 and LPM3 are measured with ACLK selected.

Current consumption of active mode versus system frequency, F-version

$$I_{(AM)} = I_{(AM)} [1 \text{ MHz}] \times f(\text{System}) [\text{MHz}]$$

Current consumption of active mode versus supply voltage, F-version

$$I_{(AM)} = I_{(AM)} [3 \text{ V}] + 175 \mu\text{A/V} \times (V_{CC} - 3 \text{ V})$$

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

SCHMITT-trigger inputs – Ports P1, P2, P3, P4, P5, and P6

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 2.2 V	1.1		1.5	V
		V _{CC} = 3 V	1.5		1.9	
V _{IT-}	Negative-going input threshold voltage	V _{CC} = 2.2 V	0.4		0.9	V
		V _{CC} = 3 V	0.90		1.3	
V _{hys}	Input voltage hysteresis (V _{IT+} – V _{IT-})	V _{CC} = 2.2 V	0.3		1.1	V
		V _{CC} = 3 V	0.5		1	

standard inputs – \overline{RST}/NMI ; JTAG: TCK, TMS, TDI/TCLK, TDO/TDI

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IL}	Low-level input voltage	V _{CC} = 2.2 V / 3 V	V _{SS}		V _{SS} +0.6	V
V _{IH}	High-level input voltage		0.8×V _{CC}		V _{CC}	V

inputs Px.x, TA_x, TB_x

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
t _(int)	External interrupt timing	Port P1, P2: P1.x to P2.x, external trigger signal for the interrupt flag, (see Note 1)	2.2 V/3 V	1.5			cycle
			2.2 V	62			ns
			3 V	50			
t _(cap)	Timer_A, Timer_B capture timing	TA0, TA1, TA2 TB0, TB1, TB2, TB3, TB4, TB5, TB6 (see Note 2)	2.2 V	62			ns
			3 V	50			
f _(TAext)	Timer_A, Timer_B clock frequency externally applied to pin	TACLK, TBCLK, INCLK: t _(H) = t _(L)	2.2 V			8	MHz
f _(TBext)			3 V			10	
f _(TAint)	Timer_A, Timer_B clock frequency	SMCLK or ACLK signal selected	2.2 V			8	MHz
f _(TBint)			3 V			10	

- NOTES: 1. The external signal sets the interrupt flag every time the minimum t_(int) cycle and time parameters are met. It may be set even with trigger signals shorter than t_(int). Both the cycle and timing specifications must be met to ensure the flag is set. t_(int) is measured in MCLK cycles.
2. Seven capture/compare registers in 'x14x(1) and three capture/compare registers in 'x13x.

leakage current (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I _{lkg} (P1.x)	Leakage current (see Note 1)	Port P1	V _(P1.x) (see Note 2)			±50	nA
I _{lkg} (P2.x)		Port P2	V _(P2.3) V _(P2.4) (see Note 2)	V _{CC} = 2.2 V/3 V		±50	
I _{lkg} (P6.x)		Port P6	V _(P6.x) (see Note 2)			±50	

- NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as input and there must be no optional pullup or pulldown resistor.



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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

outputs – Ports P1, P2, P3, P4, P5, and P6

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OH} High-level output voltage	I _{OH(max)} = -1 mA, V _{CC} = 2.2 V, See Note 1	V _{CC} -0.25		V _{CC}	V
	I _{OH(max)} = -6 mA, V _{CC} = 2.2 V, See Note 2	V _{CC} -0.6		V _{CC}	
	I _{OH(max)} = -1 mA, V _{CC} = 3 V, See Note 1	V _{CC} -0.25		V _{CC}	
	I _{OH(max)} = -6 mA, V _{CC} = 3 V, See Note 2	V _{CC} -0.6		V _{CC}	
V _{OL} Low-level output voltage	I _{OL(max)} = 1.5 mA, V _{CC} = 2.2 V, See Note 1	V _{SS}		V _{SS} +0.25	V
	I _{OL(max)} = 6 mA, V _{CC} = 2.2 V, See Note 2	V _{SS}		V _{SS} +0.6	
	I _{OL(max)} = 1.5 mA, V _{CC} = 3 V, See Note 1	V _{SS}		V _{SS} +0.25	
	I _{OL(max)} = 6 mA, V _{CC} = 3 V, See Note 2	V _{SS}		V _{SS} +0.6	

- NOTES: 1. The maximum total current, I_{OH(max)} and I_{OL(max)}, for all outputs combined, should not exceed ±6 mA to satisfy the maximum specified voltage drop.
 2. The maximum total current, I_{OH(max)} and I_{OL(max)}, for all outputs combined, should not exceed ±24 mA to satisfy the maximum specified voltage drop.

output frequency

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
f _{TAX} TA0..2, TB0–TB6, Internal clock source, SMCLK signal applied (see Note 1)	C _L = 20 pF	DC		f _{System}	MHz	
f _{ACLK} , f _{MCLK} , f _{SMCLK} P5.6/ACLK, P5.4/MCLK, P5.5/SMCLK	C _L = 20 pF			f _{System}		
t _{Xdc} Duty cycle of output frequency,	P2.0/ACLK C _L = 20 pF, V _{CC} = 2.2 V / 3 V	f _{ACLK} = f _{LFXT1} = f _{XT1}		40%	60%	
		f _{ACLK} = f _{LFXT1} = f _{LF}		30%	70%	
		f _{ACLK} = f _{LFXT1/n}			50%	
	P1.4/SMCLK, C _L = 20 pF, V _{CC} = 2.2 V / 3 V	f _{SMCLK} = f _{LFXT1} = f _{XT1}			40%	60%
		f _{SMCLK} = f _{LFXT1} = f _{LF}			35%	65%
		f _{SMCLK} = f _{LFXT1/n}		50%– 15 ns	50%	50%– 15 ns
	f _{SMCLK} = f _{DCOCLK}		50%– 15 ns	50%	50%– 15 ns	

NOTE 1: The limits of the system clock MCLK has to be met; the system (MCLK) frequency should not exceed the limits. MCLK and SMCLK frequencies can be different.

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

outputs – Ports P1, P2, P3, P4, P5, and P6 (continued)

TYPICAL LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

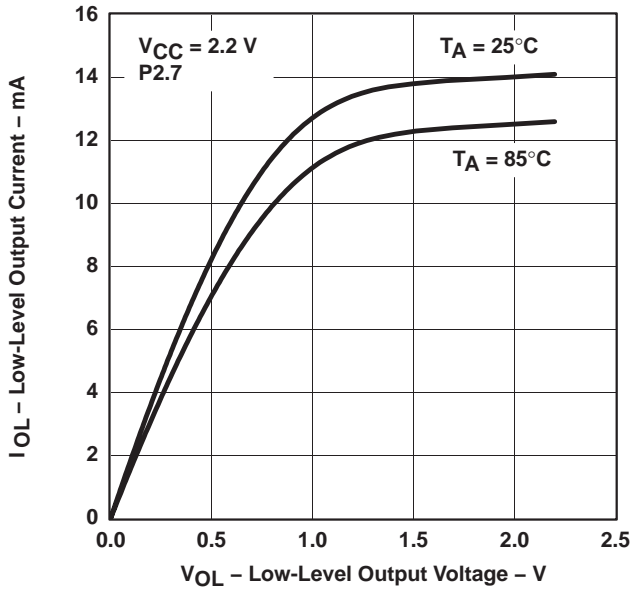


Figure 2

TYPICAL LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

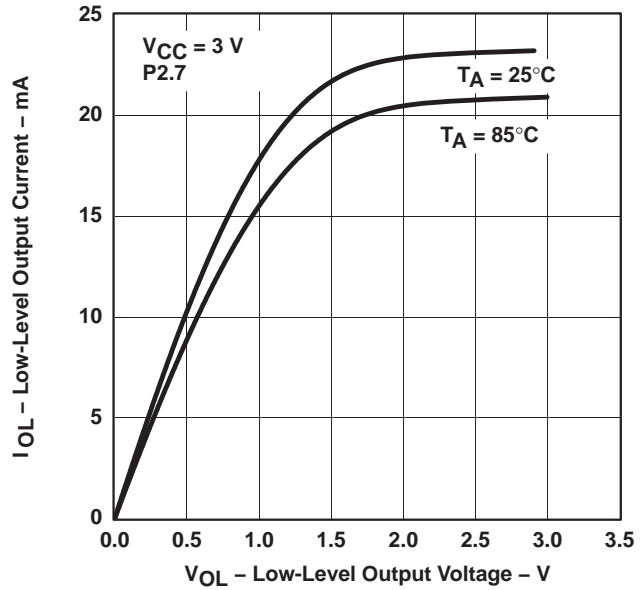


Figure 3

TYPICAL HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

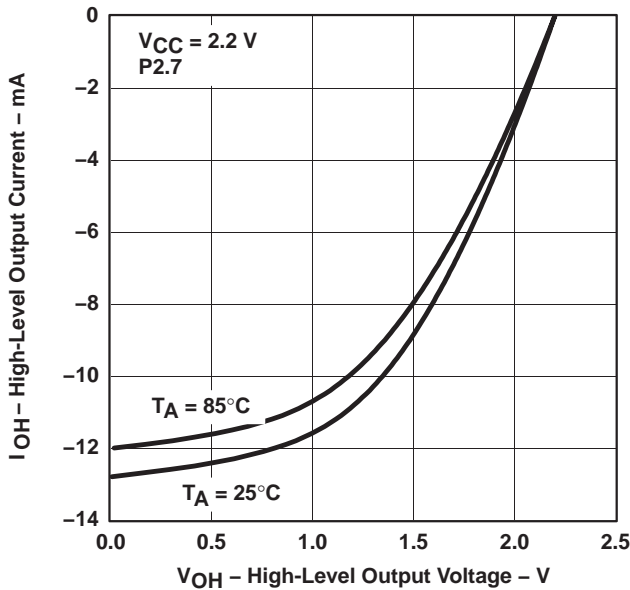


Figure 4

TYPICAL HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

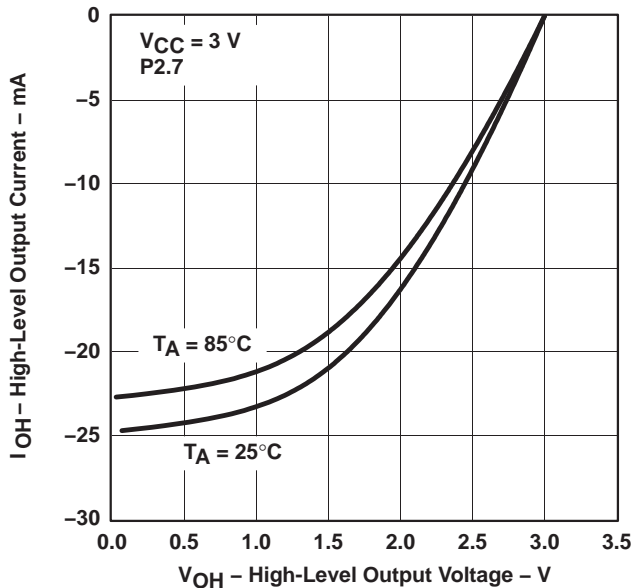


Figure 5

MSP430x13x, MSP430x14x, MSP430x14x1 MIXED SIGNAL MICROCONTROLLER

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

wake-up LPM3

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _(LPM3) Delay time	f = 1 MHz	V _{CC} = 2.2 V/3 V			6	μs
	f = 2 MHz				6	
	f = 3 MHz				6	

RAM

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{RAMh}	CPU HALTED (see Note 1)	1.6			V

NOTE 1: This parameter defines the minimum supply voltage when the data in program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

Comparator_A (see Note 1)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
I _(DD)	CAON=1, CARSEL=0, CAREF=0	V _{CC} = 2.2 V		25	40	μA
		V _{CC} = 3 V		45	60	
I _(Refladder/Refdiode)	CAON=1, CARSEL=0, CAREF=1/2/3, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2	V _{CC} = 2.2 V		30	50	μA
		V _{CC} = 3 V		45	71	
V _(IC) Common-mode input voltage	CAON =1	V _{CC} = 2.2 V/3 V	0		V _{CC} -1	V
V _(Ref025) $\frac{\text{Voltage @ } 0.25 V_{CC} \text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=1, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2	V _{CC} = 2.2 V/3 V	0.23	0.24	0.25	
V _(Ref050) $\frac{\text{Voltage @ } 0.5 V_{CC} \text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=2, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2	V _{CC} = 2.2 V/3 V	0.47	0.48	0.5	
V _(RefVT) (see Figure 6)	PCA0=1, CARSEL=1, CAREF=3, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2 T _A = 85°C	V _{CC} = 2.2 V	390	480	540	mV
		V _{CC} = 3 V	400	490	550	
V _(offset) Offset voltage	See Note 2	V _{CC} = 2.2 V/3 V	-30		30	mV
V _{hys} Input hysteresis	CAON=1	V _{CC} = 2.2 V/3 V	0	0.7	1.4	mV
t _(response LH)	T _A = 25°C, Overdrive 10 mV, Without filter: CAF=0	V _{CC} = 2.2 V	130	210	300	ns
		V _{CC} = 3 V	80	150	240	
	T _A = 25°C, Overdrive 10 mV, With filter: CAF=1	V _{CC} = 2.2 V	1.4	1.9	3.4	μs
		V _{CC} = 3 V	0.9	1.5	2.6	
t _(response HL)	T _A = 25°C, Overdrive 10 mV, Without filter: CAF=0	V _{CC} = 2.2 V	130	210	300	ns
		V _{CC} = 3 V	80	150	240	
	T _A = 25°C, Overdrive 10 mV, With filter: CAF=1	V _{CC} = 2.2 V	1.4	1.9	3.4	μs
		V _{CC} = 3 V	0.9	1.5	2.6	

NOTES: 1. The leakage current for the Comparator_A terminals is identical to I_{lkg(Px.x)} specification.
2. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A inputs on successive measurements. The two successive measurements are then summed together.



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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

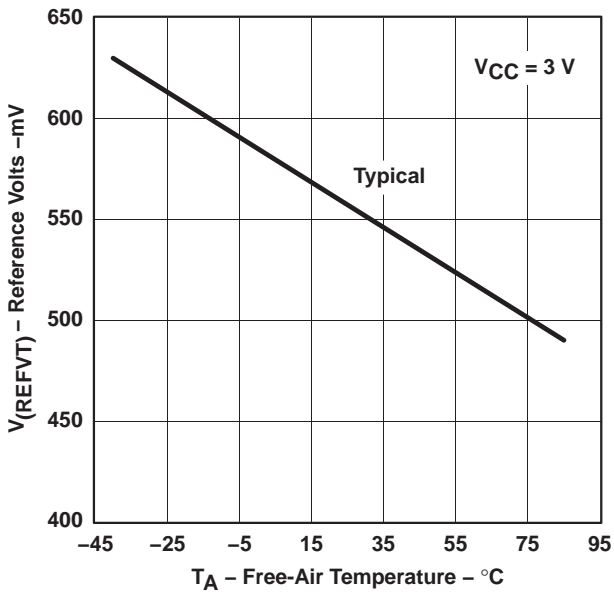


Figure 6. V(REFVT) vs Temperature, V_{CC} = 3 V

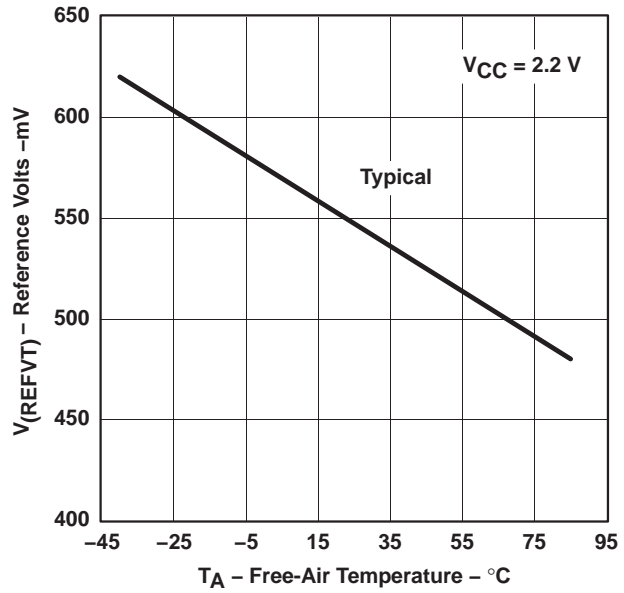


Figure 7. V(REFVT) vs Temperature, V_{CC} = 2.2 V

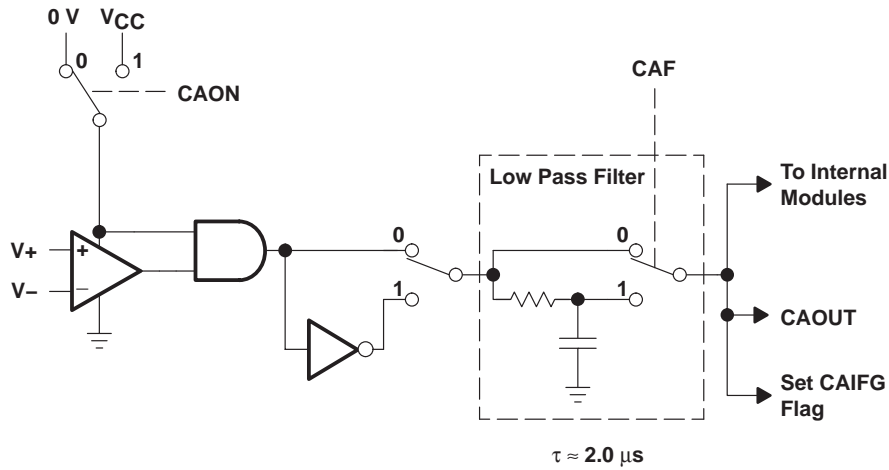


Figure 8. Block Diagram of Comparator_A Module

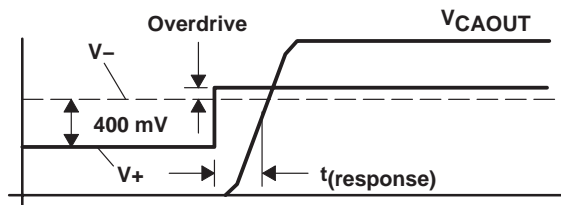


Figure 9. Overdrive Definition

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

PUC/POR

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(POR_Delay)}$	Internal time delay to release POR		150	250	μs
V_{POR}	V_{CC} threshold at which POR release delay time begins (see Note 1)	$T_A = -40^\circ C$		1.8	V
		$T_A = 25^\circ C$		1.5	V
		$T_A = 85^\circ C$		1.2	V
$V_{(min)}$	V_{CC} threshold required to generate a POR (see Note 2)	$V_{CC} dV/dt \geq 1V/ms$		0.2	V
$t_{(reset)}$	\overline{RST}/NMI low time for PUC/POR	Reset is accepted internally		2	μs

- NOTES: 1. V_{CC} rise time $dV/dt \geq 1V/ms$.
 2. When driving V_{CC} low in order to generate a POR condition, V_{CC} should be driven to 200mV or lower with a dV/dt equal to or less than $-1V/ms$. The corresponding rising V_{CC} must also meet the dV/dt requirement equal to or greater than $+1V/ms$.

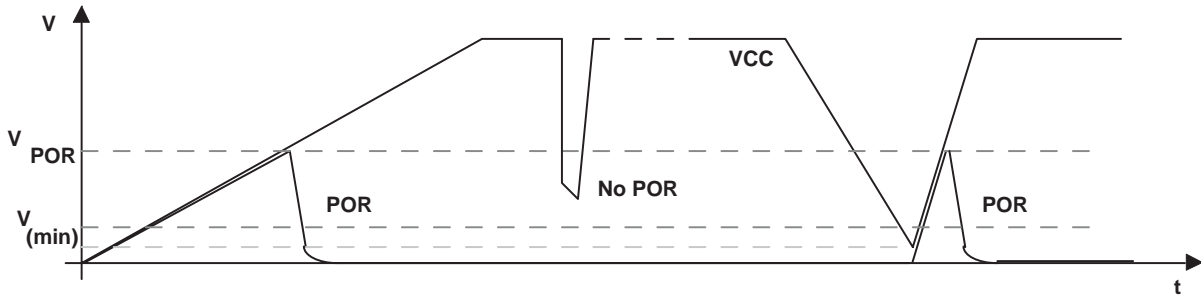


Figure 10. Power-On Reset (POR) vs Supply Voltage

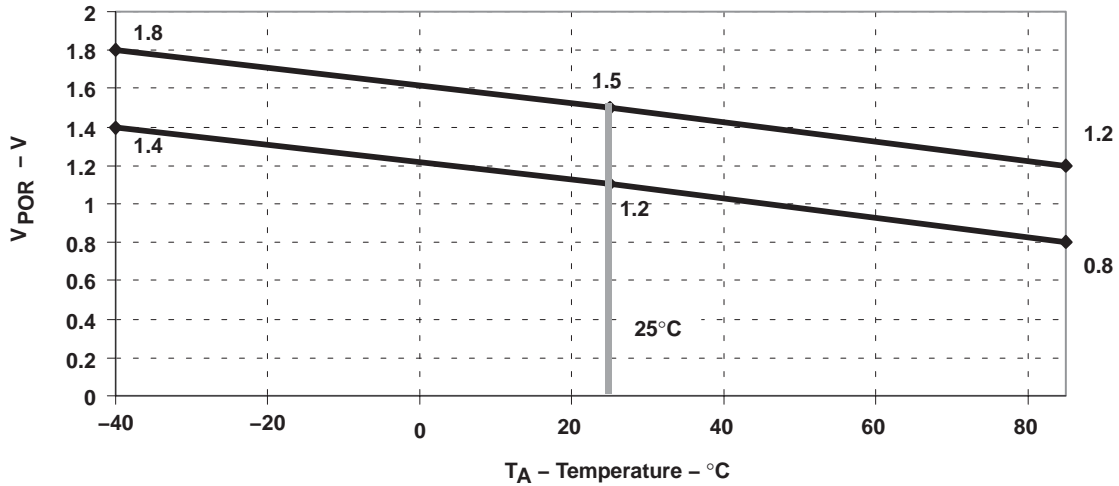


Figure 11. V_{POR} vs Temperature

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

DCO (see Note 1)

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT	
f(DCO03)	R _{sel} = 0, DCO = 3, MOD = 0, DCOR = 0, T _A = 25°C	V _{CC} = 2.2 V	0.08	0.12	0.15	MHz
		V _{CC} = 3 V	0.08	0.13	0.16	
f(DCO13)	R _{sel} = 1, DCO = 3, MOD = 0, DCOR = 0, T _A = 25°C	V _{CC} = 2.2 V	0.14	0.19	0.23	MHz
		V _{CC} = 3 V	0.14	0.18	0.22	
f(DCO23)	R _{sel} = 2, DCO = 3, MOD = 0, DCOR = 0, T _A = 25°C	V _{CC} = 2.2 V	0.22	0.30	0.36	MHz
		V _{CC} = 3 V	0.22	0.28	0.34	
f(DCO33)	R _{sel} = 3, DCO = 3, MOD = 0, DCOR = 0, T _A = 25°C	V _{CC} = 2.2 V	0.37	0.49	0.59	MHz
		V _{CC} = 3 V	0.37	0.47	0.56	
f(DCO43)	R _{sel} = 4, DCO = 3, MOD = 0, DCOR = 0, T _A = 25°C	V _{CC} = 2.2 V	0.61	0.77	0.93	MHz
		V _{CC} = 3 V	0.61	0.75	0.90	
f(DCO53)	R _{sel} = 5, DCO = 3, MOD = 0, DCOR = 0, T _A = 25°C	V _{CC} = 2.2 V	1	1.2	1.5	MHz
		V _{CC} = 3 V	1	1.3	1.5	
f(DCO63)	R _{sel} = 6, DCO = 3, MOD = 0, DCOR = 0, T _A = 25°C	V _{CC} = 2.2 V	1.6	1.9	2.2	MHz
		V _{CC} = 3 V	1.69	2.0	2.29	
f(DCO73)	R _{sel} = 7, DCO = 3, MOD = 0, DCOR = 0, T _A = 25°C	V _{CC} = 2.2 V	2.4	2.9	3.4	MHz
		V _{CC} = 3 V	2.7	3.2	3.65	
f(DCO47)	R _{sel} = 4, DCO = 7, MOD = 0, DCOR = 0, T _A = 25°C	V _{CC} = 2.2 V/3 V	f _{DCO40} × 1.7	f _{DCO40} × 2.1	f _{DCO40} × 2.5	MHz
f(DCO77)	R _{sel} = 7, DCO = 7, MOD = 0, DCOR = 0, T _A = 25°C	V _{CC} = 2.2 V	4	4.5	4.9	MHz
		V _{CC} = 3 V	4.4	4.9	5.4	
S(Rsel)	SR = f _{Rsel+1} / f _{Rsel}	V _{CC} = 2.2 V/3 V	1.35	1.65	2	
S(DCO)	SDCO = f _{DCO+1} / f _{DCO}	V _{CC} = 2.2 V/3 V	1.07	1.12	1.16	
D _t	Temperature drift, R _{sel} = 4, DCO = 3, MOD = 0 (see Note 2)	V _{CC} = 2.2 V	-0.31	-0.36	-0.40	%/°C
		V _{CC} = 3 V	-0.33	-0.38	-0.43	
D _V	Drift with V _{CC} variation, R _{sel} = 4, DCO = 3, MOD = 0 (see Note 2)	V _{CC} = 2.2 V/3 V	0	5	10	%/V

NOTES: 1. The DCO frequency may not exceed the maximum system frequency defined by parameter processor frequency, f_(System).
2. This parameter is not production tested.

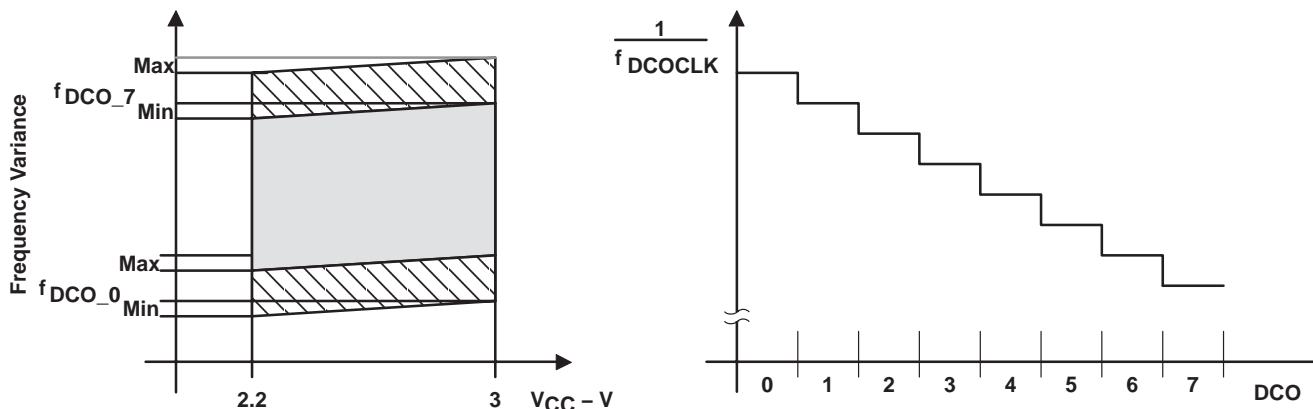


Figure 12. DCO Characteristics

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

main DCO characteristics

- Individual devices have a minimum and maximum operation frequency. The specified parameters for fDCOx0 to fDCOx7 are valid for all devices.
- All ranges selected by Rsel(n) overlap with Rsel(n+1): Rsel0 overlaps with Rsel1, ... Rsel6 overlaps with Rsel7.
- DCO control bits DCO0, DCO1, and DCO2 have a step size as defined by parameter SDCO.
- Modulation control bits MOD0 to MOD4 select how often fDCO+1 is used within the period of 32 DCOCLK cycles. The frequency f(DCO) is used for the remaining cycles. The frequency is an average equal to $f(\text{DCO}) \times (2^{\text{MOD}/32})$.

DCO when using R_{OSC} (see Note 1)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	NOM	MAX	UNIT
f _{DCO} , DCO output frequency	R _{sel} = 4, DCO = 3, MOD = 0, DCOR = 1, T _A = 25°C	2.2 V		1.8±15%		MHz
		3 V		1.95±15%		MHz
D _t , Temperature drift	R _{sel} = 4, DCO = 3, MOD = 0, DCOR = 1	2.2 V/3 V		±0.1		%/°C
D _v , Drift with V _{CC} variation	R _{sel} = 4, DCO = 3, MOD = 0, DCOR = 1	2.2 V/3 V		10		%/V

NOTES: 1. R_{OSC} = 100kΩ. Metal film resistor, type 0257. 0.6 watt with 1% tolerance and T_K = ±50ppm/°C.

crystal oscillator, LFXT1 oscillator (see Note 1)

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
C _{XIN} Integrated input capacitance	XTS=0; LF oscillator selected V _{CC} = 2.2 V/3 V		12		pF
	XTS=1; XT1 oscillator selected V _{CC} = 2.2 V/3 V		2		
C _{XOUT} Integrated output capacitance	XTS=0; LF oscillator selected V _{CC} = 2.2 V/3 V		12		pF
	XTS=1; XT1 oscillator selected V _{CC} = 2.2 V/3 V		2		
V _{IL}	Input levels at XIN V _{CC} = 2.2 V/3 V (see Note 2)	V _{SS}		0.2 × V _{CC}	V
V _{IH}		0.8 × V _{CC}		V _{CC}	V

- NOTES: 1. The oscillator needs capacitors at both terminals, with values specified by the crystal manufacturer.
2. Applies only when using an external logic-level clock source. Not applicable when using a crystal or resonator.

crystal oscillator, XT2 oscillator (see Note 1)

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
C _{XT2IN} Input capacitance	V _{CC} = 2.2 V/3 V		2		pF
C _{XT2OUT} Output capacitance	V _{CC} = 2.2 V/3 V		2		pF
V _{IL}	Input levels at XT2IN V _{CC} = 2.2 V/3 V (see Note 2)	V _{SS}		0.2 × V _{CC}	V
V _{IH}		0.8 × V _{CC}		V _{CC}	V

- NOTES: 1. The oscillator needs capacitors at both terminals, with values specified by the crystal manufacturer.
2. Applies only when using an external logic-level clock source. Not applicable when using a crystal or resonator.

USART0, USART1 (see Note 1)

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
t _(τ) USART0/1: deglitch time	V _{CC} = 2.2 V	200	430	800	ns
	V _{CC} = 3 V	150	280	500	

NOTE 1: The signal applied to the USART0/1 receive signal/terminal (URXD0/1) should meet the timing requirements of t_(τ) to ensure that the URXS flip-flop is set. The URXS flip-flop is set with negative pulses meeting the minimum-timing condition of t_(τ). The operating conditions to set the flag must be met independently from this timing constraint. The deglitch circuitry is active only on negative transitions on the URXD0/1 line.

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, power supply and input range conditions (see Note 1)

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{AVCC} Analog supply voltage	V_{AVCC} and DV_{CC} are connected together V_{AVSS} and DV_{SS} are connected together $V_{(AVSS)} = V_{(DVSS)} = 0\text{ V}$	2.2		3.6	V
$V_{(P6.x/Ax)}$ Analog input voltage range (see Note 2)	All P6.0/A0 to P6.7/A7 terminals. Analog inputs selected in ADC12MCTLx register and P6Sel.x=1 $0 \leq x \leq 7; V_{(AVSS)} \leq V_{P6.x/Ax} \leq V_{(AVCC)}$	0		V_{AVCC}	V
I_{ADC12} Operating supply current into V_{AVCC} terminal (see Note 3)	$f_{ADC12CLK} = 5.0\text{ MHz}$ ADC12ON = 1, REFON = 0 SHT0=0, SHT1=0, ADC12DIV=0	2.2 V	0.65	1.3	mA
		3 V	0.8	1.6	
I_{REF+} Operating supply current into V_{AVCC} terminal (see Note 4)	$f_{ADC12CLK} = 5.0\text{ MHz}$ ADC12ON = 0, REFON = 1, REF2_5V = 1	3 V	0.5	0.8	mA
	$f_{ADC12CLK} = 5.0\text{ MHz}$ ADC12ON = 0, REFON = 1, REF2_5V = 0	2.2 V	0.5	0.8	mA
		3 V	0.5	0.8	
$C_i \dagger$ Input capacitance	Only one terminal can be selected at one time, P6.x/Ax	2.2 V		40	pF
$R_i \dagger$ Input MUX ON resistance	$0V \leq V_{Ax} \leq V_{AVCC}$	3 V		2000	Ω

\dagger Not production tested, limits verified by design

- NOTES: 1. The leakage current is defined in the leakage current table with P6.x/Ax parameter.
2. The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
3. The internal reference supply current is not included in current consumption parameter I_{ADC12} .
4. The internal reference current is supplied via terminal V_{AVCC} . Consumption is independent of the ADC12ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.

12-bit ADC, external reference (see Note 1)

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{eREF+} Positive external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 2)	1.4		V_{AVCC}	V
V_{REF-}/V_{eREF-} Negative external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 3)	0		1.2	V
$(V_{eREF+} - V_{REF-}/V_{eREF-})$ Differential external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 4)	1.4		V_{AVCC}	V
I_{VeREF+} Static input current	$0V \leq V_{eREF+} \leq V_{AVCC}$	2.2 V/3 V		± 1	μA
I_{VREF-}/V_{eREF-} Static input current	$0V \leq V_{eREF-} \leq V_{AVCC}$	2.2 V/3 V		± 1	μA

- NOTES: 1. The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_i , is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
2. The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
3. The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
4. The accuracy limits minimum differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, built-in reference

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT	
V_{REF+} Positive built-in reference voltage output	REF2_5V = 1 for 2.5 V $I_{VREF+} \leq I_{VREF+max}$	3 V	2.4	2.5	2.6	V
	REF2_5V = 0 for 1.5 V $I_{VREF+} \leq I_{VREF+max}$	2.2 V/3 V	1.44	1.5	1.56	
$AV_{CC(min)}$ AV_{CC} minimum voltage, Positive built-in reference active	REF2_5V = 0, $I_{VREF+} \leq 1mA$	2.2			V	
	REF2_5V = 1, $I_{VREF+} \leq 0.5mA$	$V_{REF+} + 0.15$				
	REF2_5V = 1, $I_{VREF+} \leq 1mA$	$V_{REF+} + 0.15$				
I_{VREF+} Load current out of V_{REF+} terminal		2.2 V	0.01	-0.5	mA	
		3 V		-1		
$I_{L(VREF)+} \dagger$ Load-current regulation V_{REF+} terminal	$I_{VREF+} = 500 \mu A \pm 100 \mu A$ Analog input voltage $\sim 0.75 V$; REF2_5V = 0	2.2 V		± 2	LSB	
		3 V		± 2		
	$I_{VREF+} = 500 \mu A \pm 100 \mu A$ Analog input voltage $\sim 1.25 V$; REF2_5V = 1	3 V		± 2	LSB	
$I_{DL(VREF)+} \ddagger$ Load current regulation V_{REF+} terminal	$I_{VREF+} = 100 \mu A \rightarrow 900 \mu A$, $C_{VREF+} = 5 \mu F$, ax $\sim 0.5 \times V_{REF+}$ Error of conversion result ≤ 1 LSB	3 V		20	ns	
C_{VREF+} Capacitance at pin V_{REF+} (see Note 1)	REFON = 1, $0 mA \leq I_{VREF+} \leq I_{VREF+max}$	2.2 V/3 V	5	10	μF	
$T_{REF+} \dagger$ Temperature coefficient of built-in reference	I_{VREF+} is a constant in the range of $0 mA \leq I_{VREF+} \leq 1 mA$	2.2 V/3 V		± 100	ppm/ $^{\circ}C$	
$t_{REFON} \dagger$ Settle time of internal reference voltage (see Figure 13 and Note 2)	$I_{VREF+} = 0.5 mA$, $C_{VREF+} = 10 \mu F$, $V_{REF+} = 1.5 V$, $V_{AVCC} = 2.2 V$			17	ms	

\dagger Not production tested, limits characterized

\ddagger Not production tested, limits verified by design

NOTES: 1. The internal buffer operational amplifier and the accuracy specifications require an external capacitor. All INL and DNL tests uses two capacitors between pins V_{REF+} and AV_{SS} and V_{REF-}/V_{eREF-} and AV_{SS} : 10 μF tantalum and 100 nF ceramic.

NOTES: 2. The condition is that the error in a conversion started after t_{REFON} is less than ± 0.5 LSB. The settling time depends on the external capacitive load.

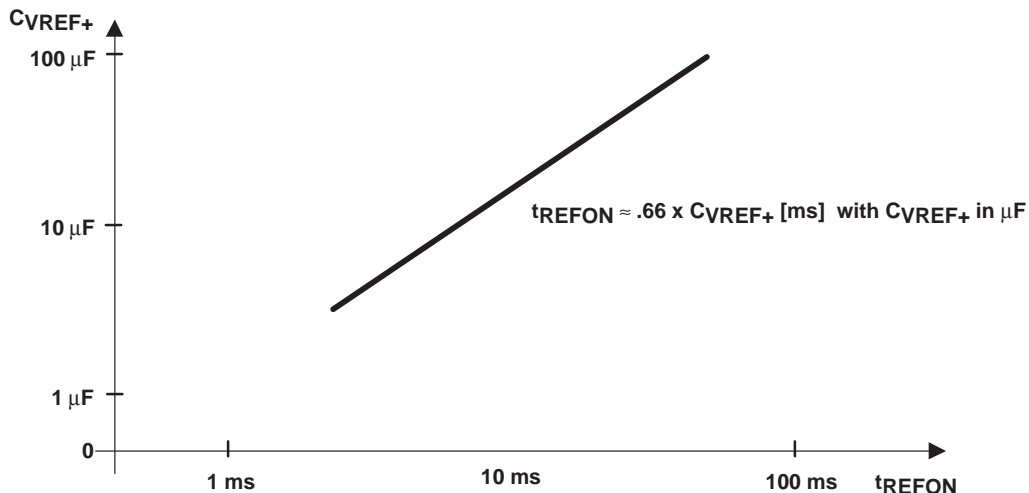


Figure 13. Typical Settling Time of Internal Reference t_{REFON} vs External Capacitor on V_{REF+}

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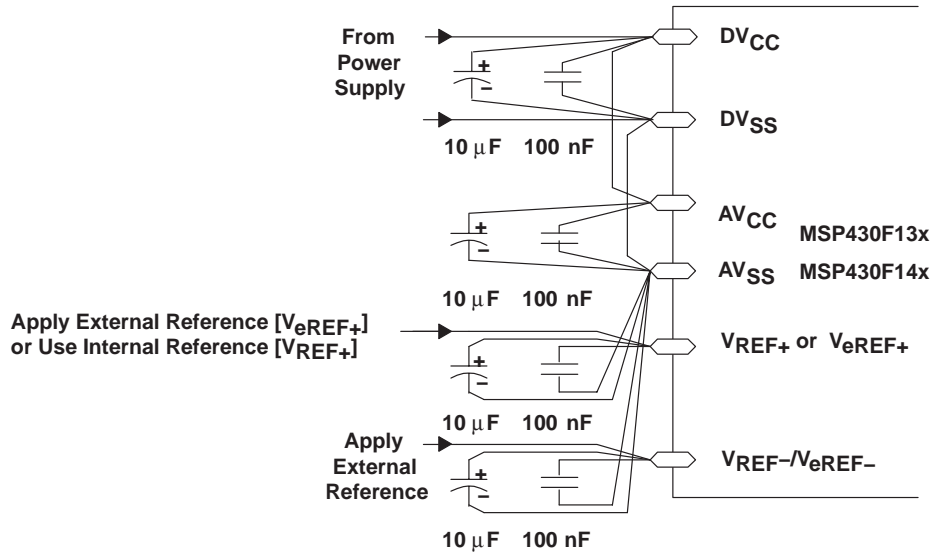


Figure 14. Supply Voltage and Reference Voltage Design V_{REF-}/V_{REF+} External Supply

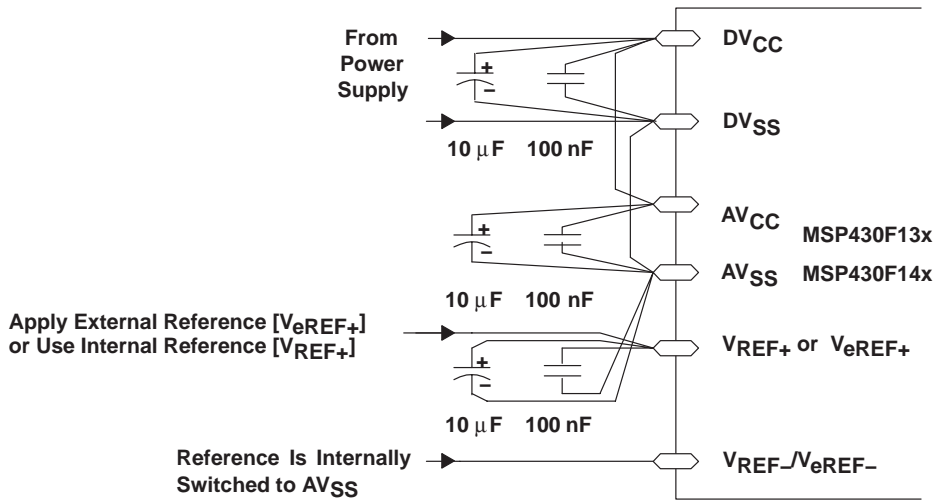


Figure 15. Supply Voltage and Reference Voltage Design $V_{REF-}/V_{REF+} = AV_{SS}$, Internally Connected

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, timing parameters

PARAMETER	TEST CONDITIONS		MIN	NOM	MAX	UNIT	
f _{ADC12CLK}	For specified performance of ADC12 linearity parameters		2.2V/3V	0.45	5	6.3	MHz
f _{ADC12OSC}	Internal ADC12 oscillator	ADC12DIV=0, f _{ADC12CLK} =f _{ADC12OSC}	2.2 V/3V	3.7		6.3	MHz
t _{CONVERT}	Conversion time	C _{VREF+} ≥ 5 μF, Internal oscillator, f _{ADC12OSC} = 3.7 MHz to 6.3 MHz	2.2 V/3 V	2.06		3.51	μs
		External f _{ADC12CLK} from ACLK, MCLK or SMCLK: ADC12SSEL ≠ 0		13×ADC12DIV× 1/f _{ADC12CLK}			μs
t _{ADC12ON} †	Turn on settling time of the ADC	(see Note 1)			100	ns	
t _{Sample} ‡	Sampling time	R _S = 400 Ω, R _I = 1000 Ω, C _I = 30 pF τ = [R _S + R _I] × C _I ; (see Note 2)	3 V	1220			ns
			2.2 V	1400			

† Not production tested, limits characterized

‡ Not production tested, limits verified by design

- NOTES: 1. The condition is that the error in a conversion started after t_{ADC12ON} is less than ±0.5 LSB. The reference and input signal are already settled.
2. Approximately ten Tau (τ) are needed to get an error of less than ±0.5 LSB:
t_{Sample} = ln(2ⁿ⁺¹) × (R_S + R_I) × C_I + 800 ns where n = ADC resolution = 12, R_S = external source resistance.

12-bit ADC, linearity parameters

PARAMETER	TEST CONDITIONS		MIN	NOM	MAX	UNIT	
E _I	Integral linearity error	1.4 V ≤ (V _{eREF+} - V _{REF-} /V _{eREF-}) min ≤ 1.6 V	2.2 V/3 V			±2	LSB
		1.6 V < (V _{eREF+} - V _{REF-} /V _{eREF-}) min ≤ [V(AVCC)]				±1.7	
E _D	Differential linearity error	(V _{eREF+} - V _{REF-} /V _{eREF-}) min ≤ (V _{eREF+} - V _{REF-} /V _{eREF-}), C _{VREF+} = 10 μF (tantalum) and 100 nF (ceramic)	2.2 V/3 V			±1	LSB
E _O	Offset error	(V _{eREF+} - V _{REF-} /V _{eREF-}) min ≤ (V _{eREF+} - V _{REF-} /V _{eREF-}), Internal impedance of source R _S < 100 Ω, C _{VREF+} = 10 μF (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±2	±4	LSB
E _G	Gain error	(V _{eREF+} - V _{REF-} /V _{eREF-}) min ≤ (V _{eREF+} - V _{REF-} /V _{eREF-}), C _{VREF+} = 10 μF (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±1.1	±2	LSB
E _T	Total unadjusted error	(V _{eREF+} - V _{REF-} /V _{eREF-}) min ≤ (V _{eREF+} - V _{REF-} /V _{eREF-}), C _{VREF+} = 10 μF (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±2	±5	LSB

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, temperature sensor and built-in V_{MID}

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
I_{SENSOR}	Operating supply current into AV_{CC} terminal (see Note 1)	REFON = 0, INCH = 0Ah, ADC12ON=NA, $T_A = 25^\circ\text{C}$	2.2 V	40	120	μA
			3 V	60	160	
V_{SENSOR}^\dagger		ADC12ON = 1, INCH = 0Ah, $T_A = 0^\circ\text{C}$	2.2 V	986	986±5%	mV
			3 V	986	986±5%	
TC_{SENSOR}^\dagger		ADC12ON = 1, INCH = 0Ah	2.2 V	3.55	3.55±3%	mV/°C
			3 V	3.55	3.55±3%	
$t_{SENSOR(\text{sample})}^\dagger$	Sample time required if channel 10 is selected (see Note 2)	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V	30		μs
			3 V	30		
I_{VMID}	Current into divider at channel 11 (see Note 3)	ADC12ON = 1, INCH = 0Bh	2.2 V		NA	μA
			3 V		NA	
V_{MID}	AV_{CC} divider at channel 11	ADC12ON = 1, INCH = 0Bh, V_{MID} is $\sim 0.5 \times V_{AVCC}$	2.2 V	1.1	1.1±0.04	V
			3 V	1.5	1.50±0.04	
$t_{VMID(\text{sample})}$	Sample time required if channel 11 is selected (see Note 4)	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V	1400		ns
			3 V	1220		

† Not production tested, limits characterized

- NOTES:
1. The sensor current I_{SENSOR} is consumed if (ADC12ON = 1 and REFON=1), or (ADC12ON=1 AND INCH=0Ah and sample signal is high). Therefore it includes the constant current through the sensor and the reference.
 2. The typical equivalent impedance of the sensor is 51 k Ω . The sample time required includes the sensor-on time $t_{SENSOR(\text{on})}$.
 3. No additional current is needed. The V_{MID} is used during sampling.
 4. The on-time $t_{VMID(\text{on})}$ is included in the sampling time $t_{VMID(\text{sample})}$; no additional on time is needed.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Flash Memory

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	NOM	MAX	UNIT
V _{CC} (PGM/ERASE)	Program and Erase supply voltage			2.7		3.6	V
f _{FTG}	Flash Timing Generator frequency			257		476	kHz
I _{PGM}	Supply current from DV _{CC} during program		2.7 V/ 3.6 V		3	5	mA
I _{ERASE}	Supply current from DV _{CC} during erase		2.7 V/ 3.6 V		3	7	mA
t _{CPT}	Cumulative program time	see Note 1	2.7 V/ 3.6 V			4	ms
t _{CMErase}	Cumulative mass erase time	see Note 2	2.7 V/ 3.6 V	200			ms
	Program/Erase endurance			10 ⁴	10 ⁵		cycles
t _{Retention}	Data retention duration	T _J = 25°C		100			years
t _{Word}	Word or byte program time	see Note 3			35		t _{FTG}
t _{Block, 0}	Block program time for 1 st byte or word				30		
t _{Block, 1-63}	Block program time for each additional byte or word				21		
t _{Block, End}	Block program end-sequence wait time				6		
t _{Mass Erase}	Mass erase time				5297		
t _{Seq Erase}	Segment erase time				4819		

- NOTES: 1. The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
 2. The mass erase duration generated by the flash timing generator is at least 11.1ms (= 5297x1/f_{FTG,max} = 5297x1/476kHz). To achieve the required cumulative mass erase time the Flash Controller's mass erase operation can be repeated until this time is met. (A worst case minimum of 19 cycles are required).
 3. These values are hardwired into the Flash Controller's state machine (t_{FTG} = 1/f_{FTG}).

JTAG Interface

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	NOM	MAX	UNIT
f _{TCK}	TCK input frequency	see Note 1	2.2 V	0		5	MHz
			3 V	0		10	MHz
R _{Internal}	Internal pull-up resistance on TMS, TCK, TDI/TCLK	see Note 2	2.2 V/ 3 V	25	60	90	kΩ

- NOTES: 1. f_{TCK} may be restricted to meet the timing requirements of the module selected.
 2. TMS, TDI/TCLK, and TCK pull-up resistors are implemented in all versions.

JTAG Fuse (see Note 1)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	NOM	MAX	UNIT
V _{CC} (FB)	Supply voltage during fuse-blow condition	T _A = 25°C		2.5			V
V _{FB}	Voltage level on TDI/TCLK for fuse-blow: F versions			6		7	V
I _{FB}	Supply current into TDI/TCLK during fuse blow					100	mA
t _{FB}	Time to blow fuse					1	ms

- NOTES: 1. Once the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

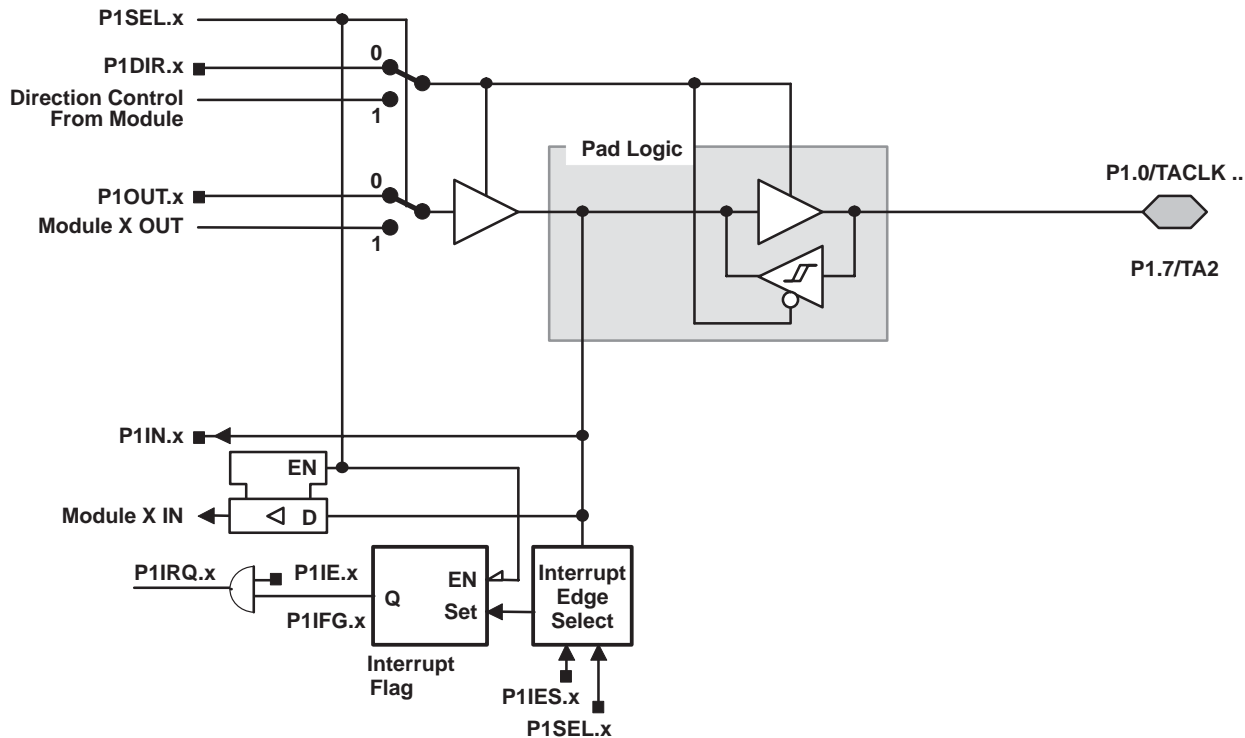
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APPLICATION INFORMATION

input/output schematic

port P1, P1.0 to P1.7, input/output with Schmitt-trigger



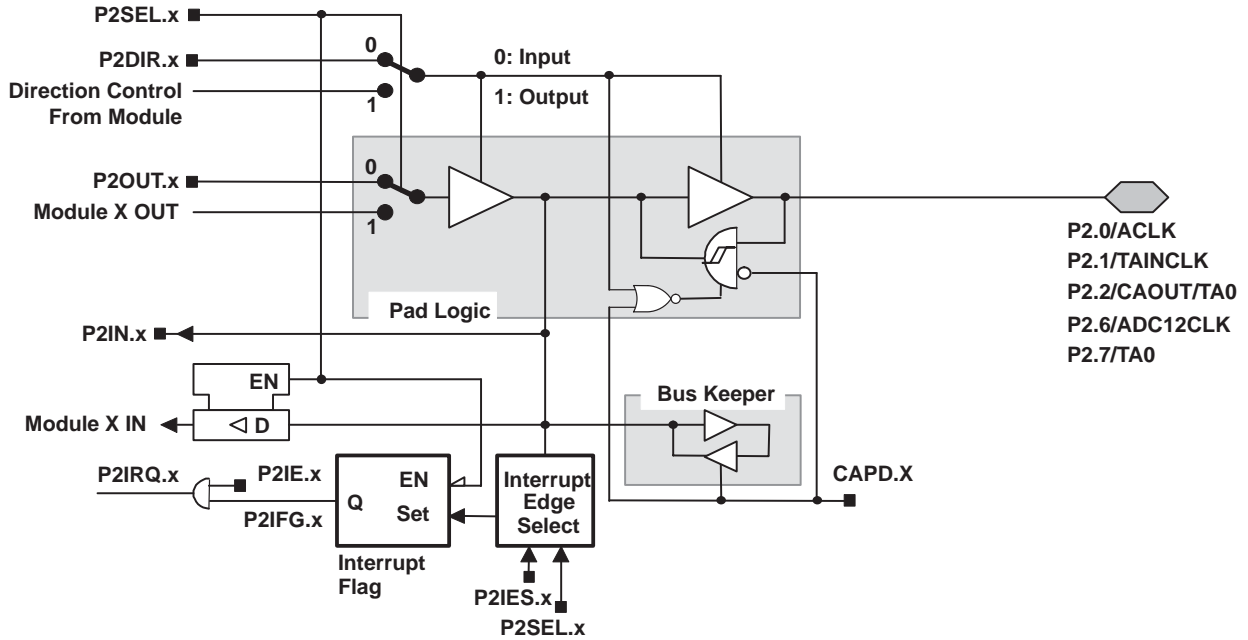
PnSel.x	PnDIR.x	Dir. CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P1Sel.0	P1DIR.0	P1DIR.0	P1OUT.0	DVSS	P1IN.0	TACLK†	P1IE.0	P1IFG.0	P1IES.0
P1Sel.1	P1DIR.1	P1DIR.1	P1OUT.1	Out0 signal†	P1IN.1	CC10A†	P1IE.1	P1IFG.1	P1IES.1
P1Sel.2	P1DIR.2	P1DIR.2	P1OUT.2	Out1 signal†	P1IN.2	CC11A†	P1IE.2	P1IFG.2	P1IES.2
P1Sel.3	P1DIR.3	P1DIR.3	P1OUT.3	Out2 signal†	P1IN.3	CC12A†	P1IE.3	P1IFG.3	P1IES.3
P1Sel.4	P1DIR.4	P1DIR.4	P1OUT.4	SMCLK	P1IN.4	unused	P1IE.4	P1IFG.4	P1IES.4
P1Sel.5	P1DIR.5	P1DIR.5	P1OUT.5	Out0 signal†	P1IN.5	unused	P1IE.5	P1IFG.5	P1IES.5
P1Sel.6	P1DIR.6	P1DIR.6	P1OUT.6	Out1 signal†	P1IN.6	unused	P1IE.6	P1IFG.6	P1IES.6
P1Sel.7	P1DIR.7	P1DIR.7	P1OUT.7	Out2 signal†	P1IN.7	unused	P1IE.7	P1IFG.7	P1IES.7

† Signal from or to Timer_A

APPLICATION INFORMATION

input/output schematic (continued)

port P2, P2.0 to P2.2, P2.6, and P2.7 input/output with Schmitt-trigger



x: Bit Identifier 0 to 2, 6, and 7 for Port P2

PnSel.x	PnDIR.x	Dir. CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.0	P2DIR.0	P2DIR.0	P2OUT.0	ACLK	P2IN.0	unused	P2IE.0	P2IFG.0	P2IES.0
P2Sel.1	P2DIR.1	P2DIR.1	P2OUT.1	DV _{SS}	P2IN.1	INCLK [†]	P2IE.1	P2IFG.1	P2IES.1
P2Sel.2	P2DIR.2	P2DIR.2	P2OUT.2	CAOUT [†]	P2IN.2	CCI0B [‡]	P2IE.2	P2IFG.2	P2IES.2
P2Sel.6	P2DIR.6	P2DIR.6	P2OUT.6	ADC12CLK [¶]	P2IN.6	unused	P2IE.6	P2IFG.6	P2IES.6
P2Sel.7	P2DIR.7	P2DIR.7	P2OUT.7	Out0 signal [§]	P2IN.7	unused	P2IE.7	P2IFG.7	P2IES.7

[†] Signal from Comparator_A

[‡] Signal to Timer_A

[§] Signal from Timer_A

[¶] ADC12CLK signal is output of the 12-bit ADC module

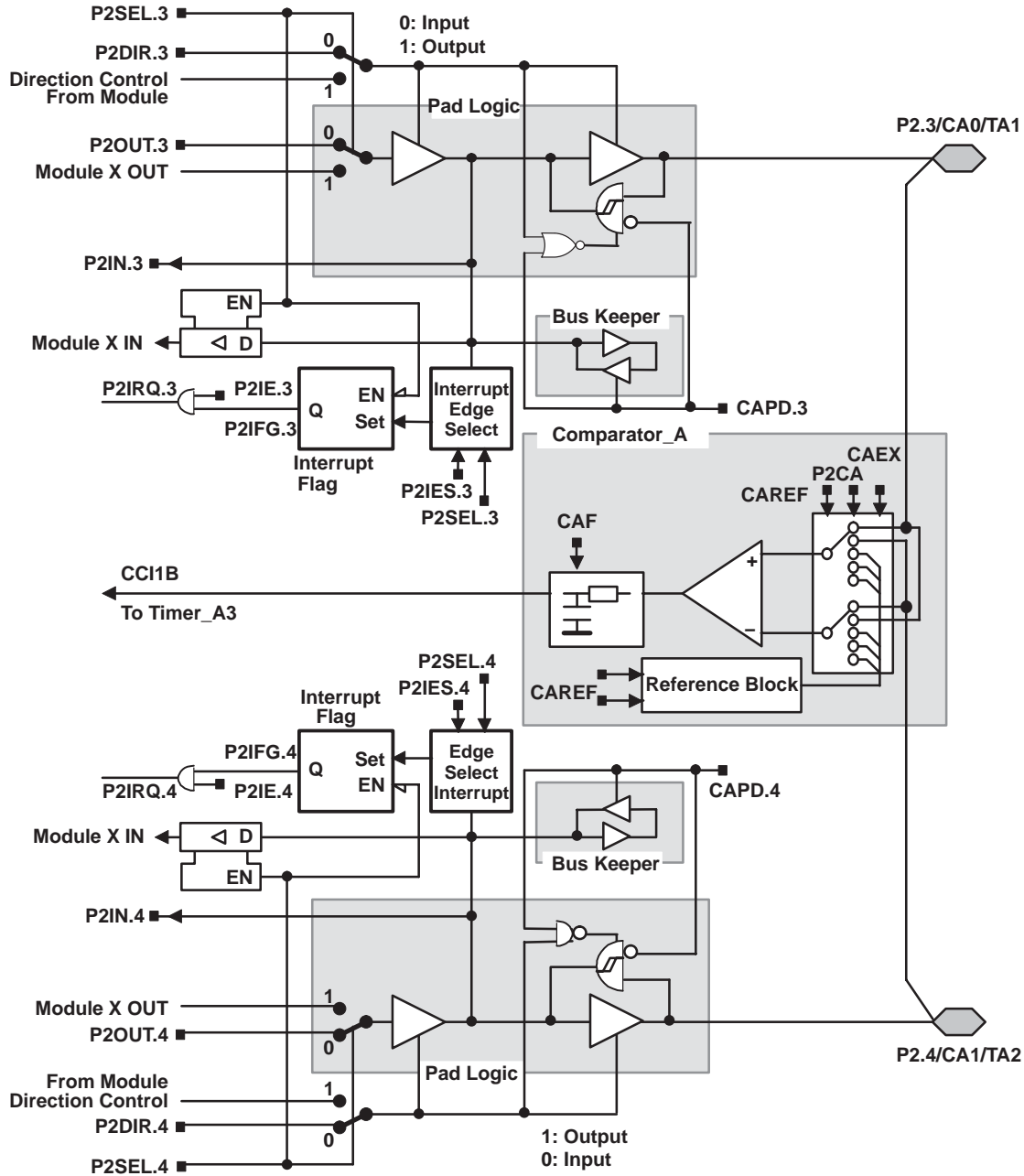
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APPLICATION INFORMATION

input/output schematic (continued)

port P2, P2.3 to P2.4, input/output with Schmitt-trigger



PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.3	P2DIR.3	P2DIR.3	P2OUT.3	Out1 signal†	P2IN.3	unused	P2IE.3	P2IFG.3	P2IES.3
P2Sel.4	P2DIR.4	P2DIR.4	P2OUT.4	Out2 signal†	P2IN.4	unused	P2IE.4	P2IFG.4	P2IES.4

† Signal from Timer_A

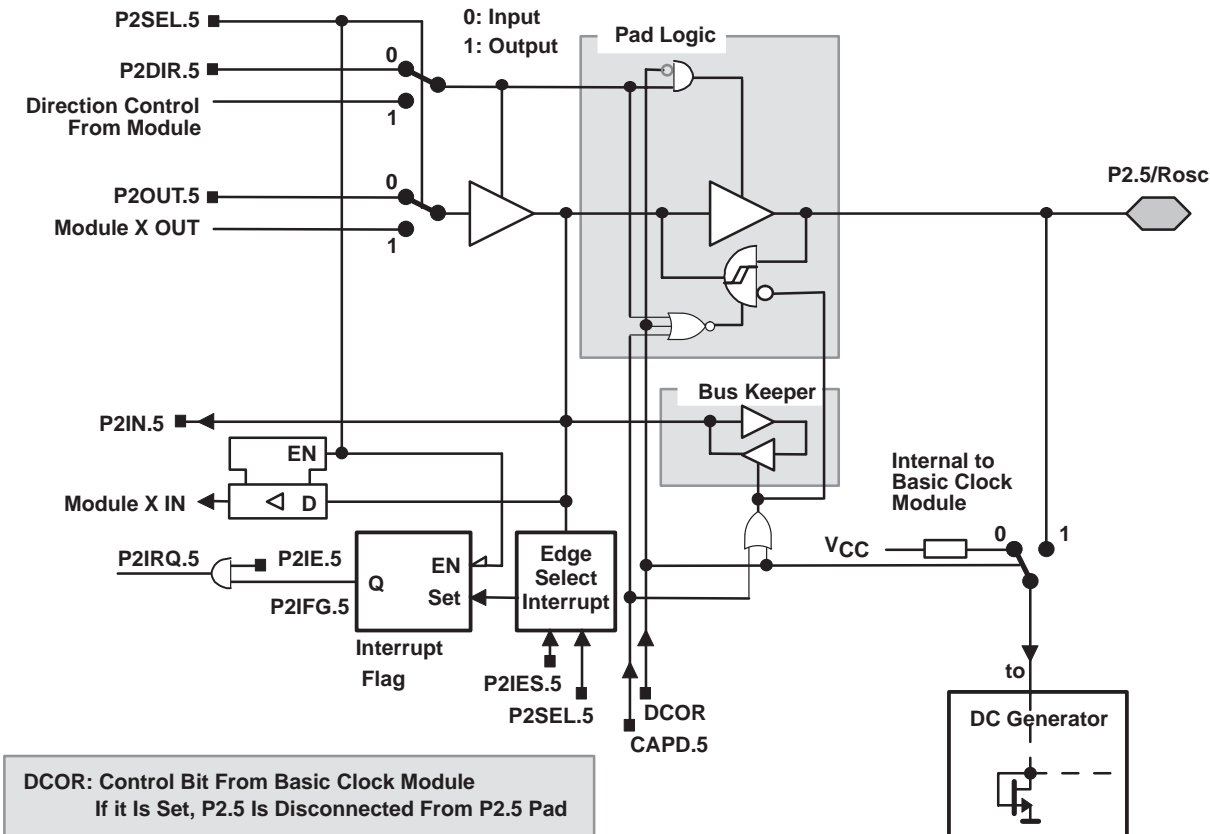


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APPLICATION INFORMATION

input/output schematic (continued)

port P2, P2.5, input/output with Schmitt-trigger and R_{Osc} function for the basic clock module



PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.5	P2DIR.5	P2DIR.5	P2OUT.5	DV _{SS}	P2IN.5	unused	P2IE.5	P2IFG.5	P2IES.5

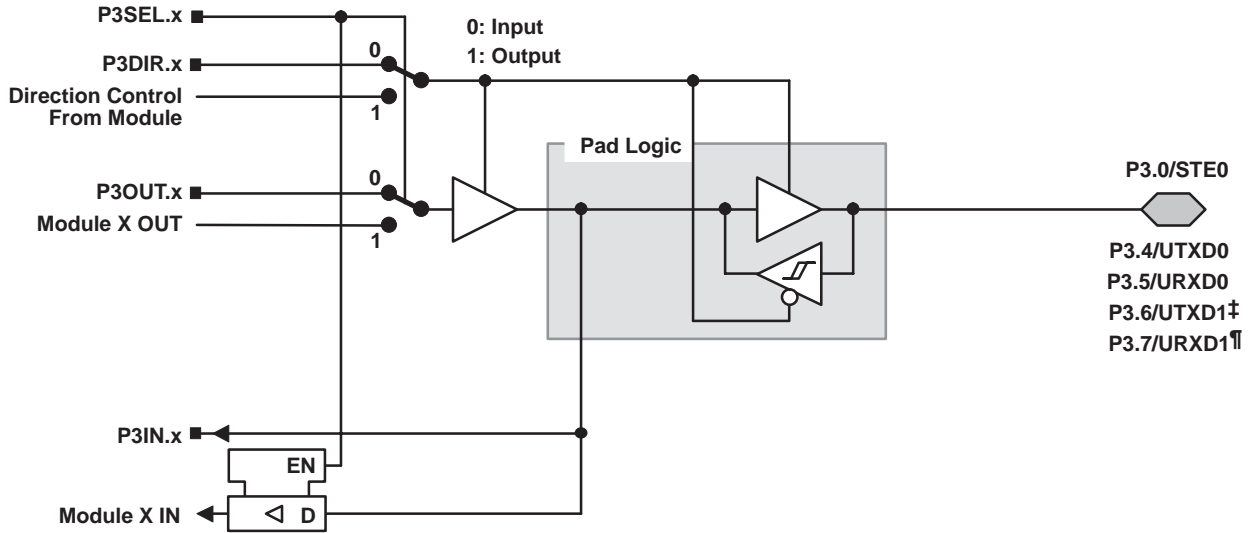
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APPLICATION INFORMATION

input/output schematic (continued)

port P3, P3.0 and P3.4 to P3.7, input/output with Schmitt-trigger



x: Bit Identifier, 0 and 4 to 7 for Port P3

PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PniN.x	MODULE X IN
P3Sel.0	P3DIR.0	DV _{SS}	P3OUT.0	DV _{SS}	P3IN.0	STE0
P3Sel.4	P3DIR.4	DV _{CC}	P3OUT.4	UTXD0†	P3IN.4	Unused
P3Sel.5	P3DIR.5	DV _{SS}	P3OUT.5	DV _{SS}	P3IN.5	URXD0§
P3Sel.6	P3DIR.6	DV _{CC}	P3OUT.6	UTXD1†	P3IN.6	Unused
P3Sel.7	P3DIR.7	DV _{SS}	P3OUT.7	DV _{SS}	P3IN.7	URXD1¶

† Output from USART0 module

‡ Output from USART1 module in x14x(1) configuration, DV_{SS} in x13x configuration

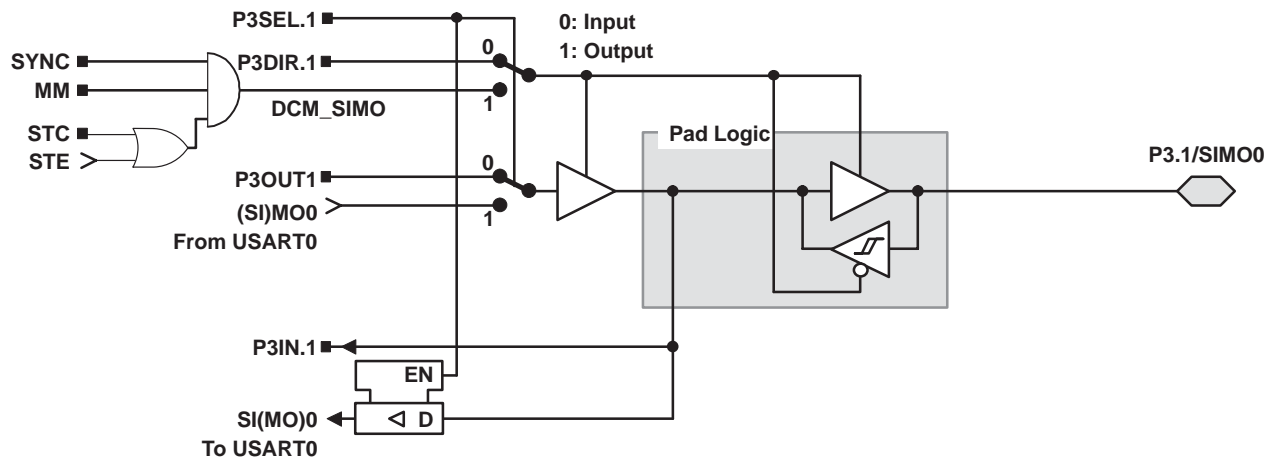
§ Input to USART0 module

¶ Input to USART1 module in x14x(1) configuration, unused in x13x configuration

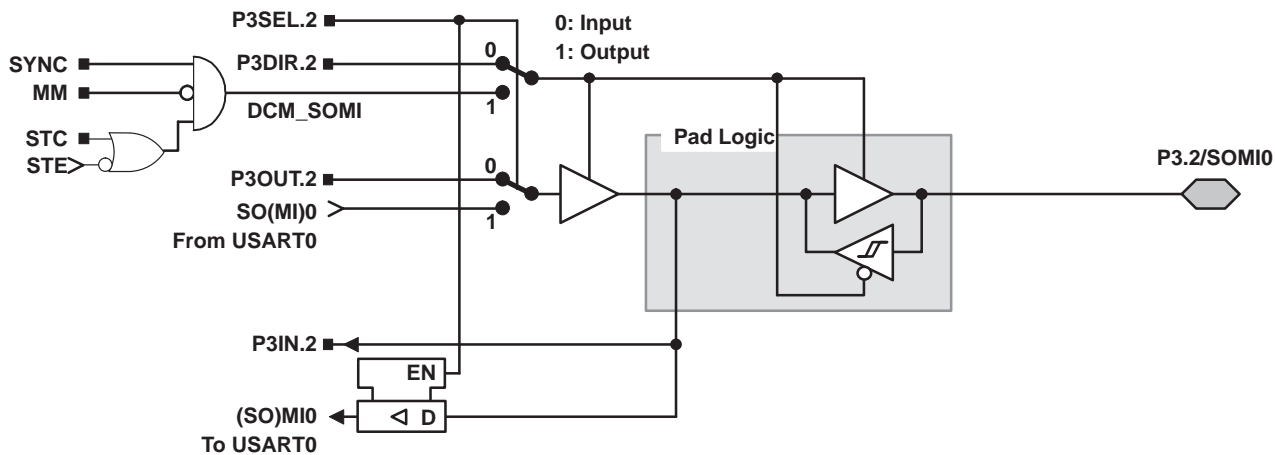
APPLICATION INFORMATION

input/output schematic (continued)

port P3, P3.1, input/output with Schmitt-trigger



port P3, P3.2, input/output with Schmitt-trigger



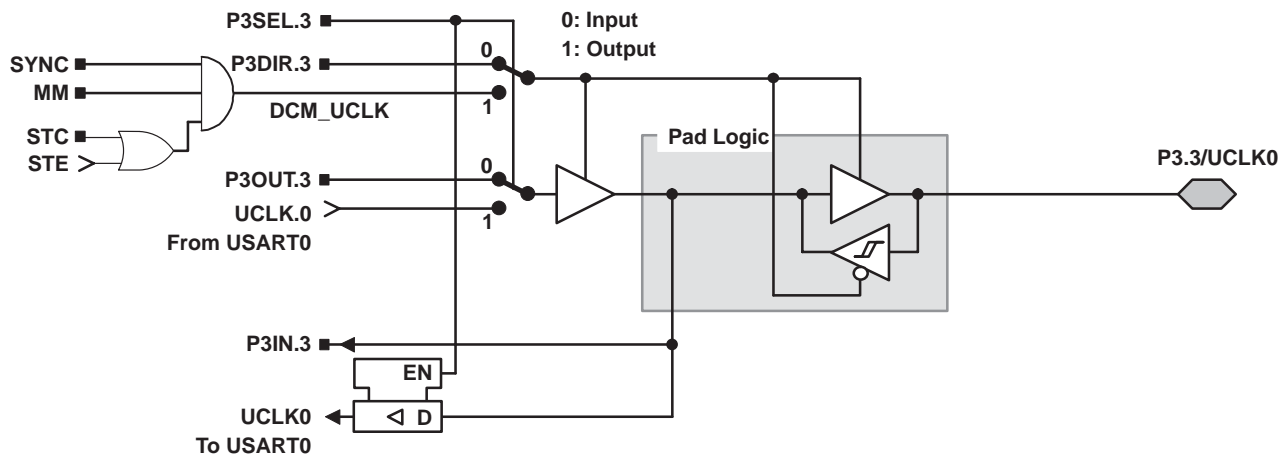
MSP430x13x, MSP430x14x, MSP430x14x1 MIXED SIGNAL MICROCONTROLLER

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APPLICATION INFORMATION

input/output schematic (continued)

port P3, P3.3, input/output with Schmitt-trigger

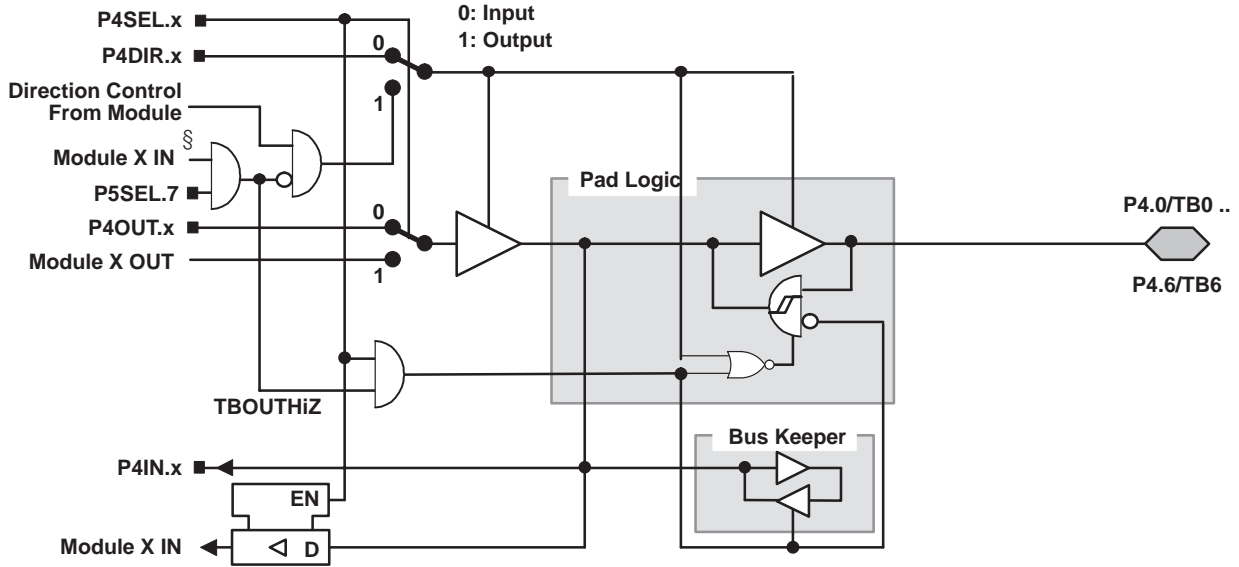


- NOTE: UART mode: The UART clock can only be an input. If UART mode and UART function are selected, the P3.3/UCLK0 is always an input.
- SPI, slave mode: The clock applied to UCLK0 is used to shift data in and out.
- SPI, master mode: The clock to shift data in and out is supplied to connected devices on pin P3.3/UCLK0 (in slave mode).

APPLICATION INFORMATION

input/output schematic (continued)

port P4, P4.0 to P4.6, input/output with Schmitt-trigger



x: bit identifier, 0 to 6 for Port P4

PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P4Sel.0	P4DIR.0	P4DIR.0	P4OUT.0	Out0 signal [†]	P4IN.0	CCI0A / CCI0B [‡]
P4Sel.1	P4DIR.1	P4DIR.1	P4OUT.1	Out1 signal [†]	P4IN.1	CCI1A / CCI1B [‡]
P4Sel.2	P4DIR.2	P4DIR.2	P4OUT.2	Out2 signal [†]	P4IN.2	CCI2A / CCI2B [‡]
P4Sel.3	P4DIR.3	P4DIR.3	P4OUT.3	Out3 signal [†]	P4IN.3	CCI3A / CCI3B [‡]
P4Sel.4	P4DIR.4	P4DIR.4	P4OUT.4	Out4 signal [†]	P4IN.4	CCI4A / CCI4B [‡]
P4Sel.5	P4DIR.5	P4DIR.5	P4OUT.5	Out5 signal [†]	P4IN.5	CCI5A / CCI5B [‡]
P4Sel.6	P4DIR.6	P4DIR.6	P4OUT.6	Out6 signal [†]	P4IN.6	CCI6A [‡]

[†] Signal from Timer_B

[‡] Signal to Timer_B

[§] From P5.7

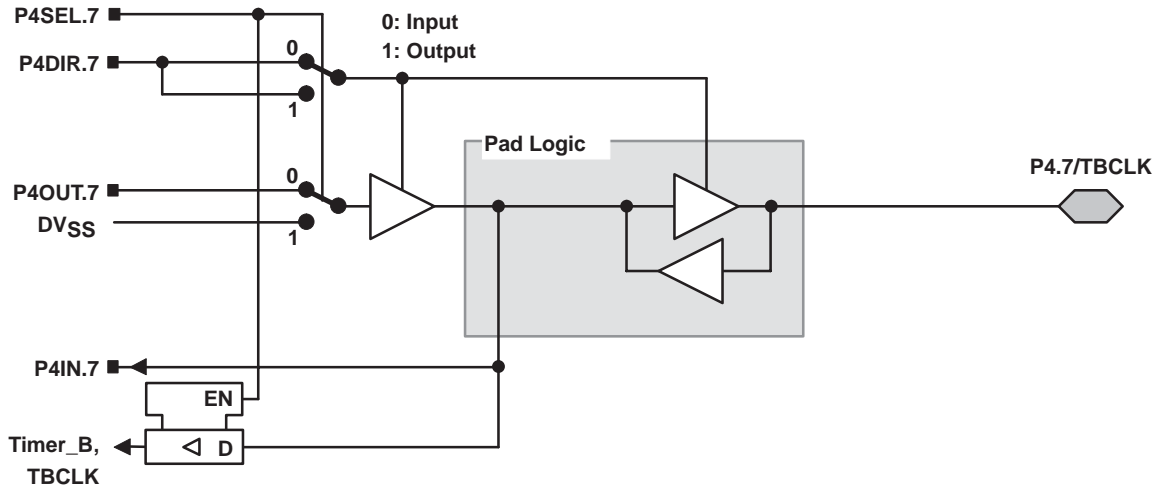
MSP430x13x, MSP430x14x, MSP430x14x1 MIXED SIGNAL MICROCONTROLLER

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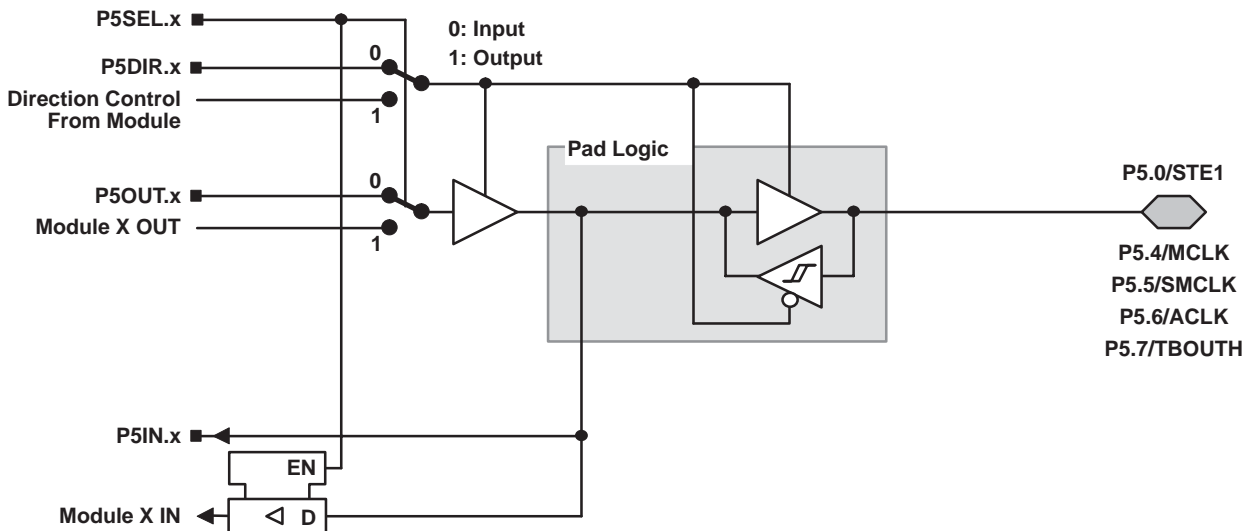
APPLICATION INFORMATION

input/output schematic (continued)

port P4, P4.7, input/output with Schmitt-trigger



port P5, P5.0 and P5.4 to P5.7, input/output with Schmitt-trigger



x: Bit Identifier, 0 and 4 to 7 for Port P5

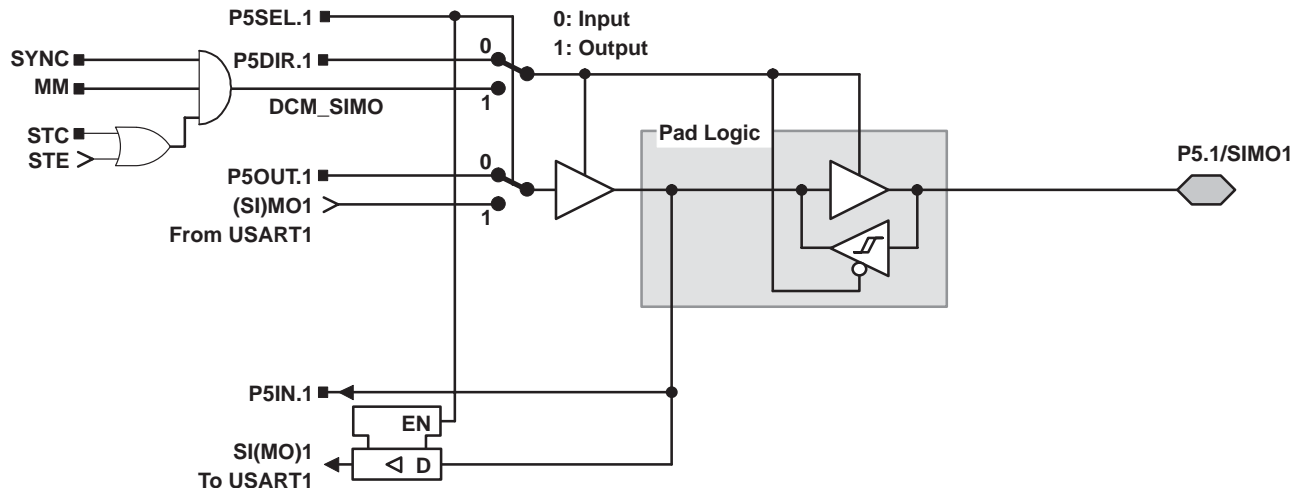
PnSel.x	PnDIR.x	Dir. CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P5Sel.0	P5DIR.0	DV _{SS}	P5OUT.0	DV _{SS}	P5IN.0	STE.1
P5Sel.4	P5DIR.4	DV _{CC}	P5OUT.4	MCLK	P5IN.4	unused
P5Sel.5	P5DIR.5	DV _{CC}	P5OUT.5	SMCLK	P5IN.5	unused
P5Sel.6	P5DIR.6	DV _{CC}	P5OUT.6	ACLK	P5IN.6	unused
P5Sel.7	P5DIR.7	DV _{SS}	P5OUT.7	DV _{SS}	P5IN.7	TBOUTHiZ

NOTE: TBOUTHiZ signal is used by port module P4, pins P4.0 to P4.6. The function of TBOUTHiZ is mainly useful when used with Timer_B7.

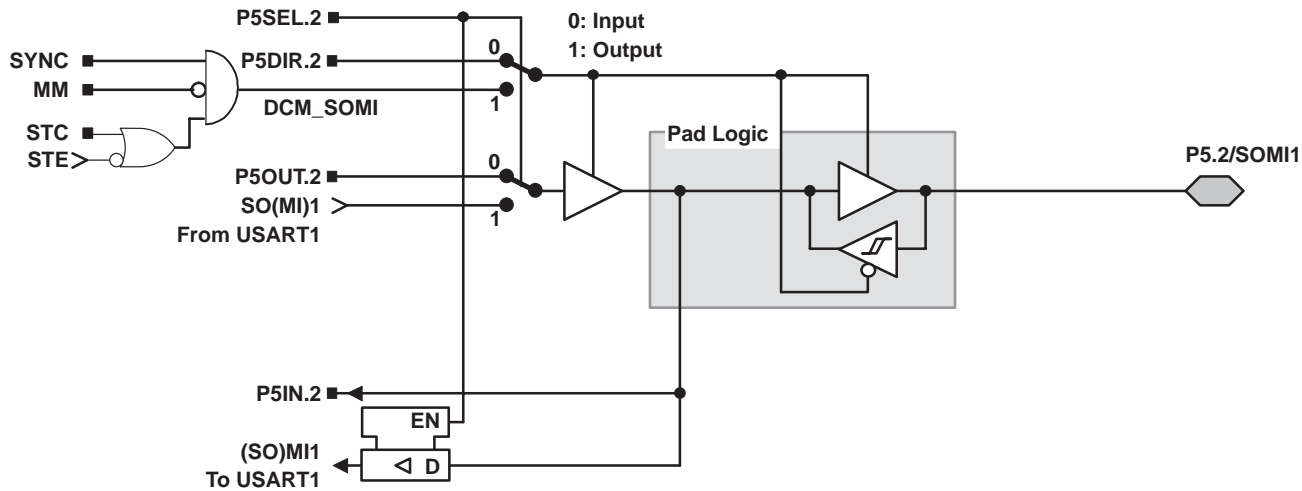
APPLICATION INFORMATION

input/output schematic (continued)

port P5, P5.1, input/output with Schmitt-trigger



port P5, P5.2, input/output with Schmitt-trigger



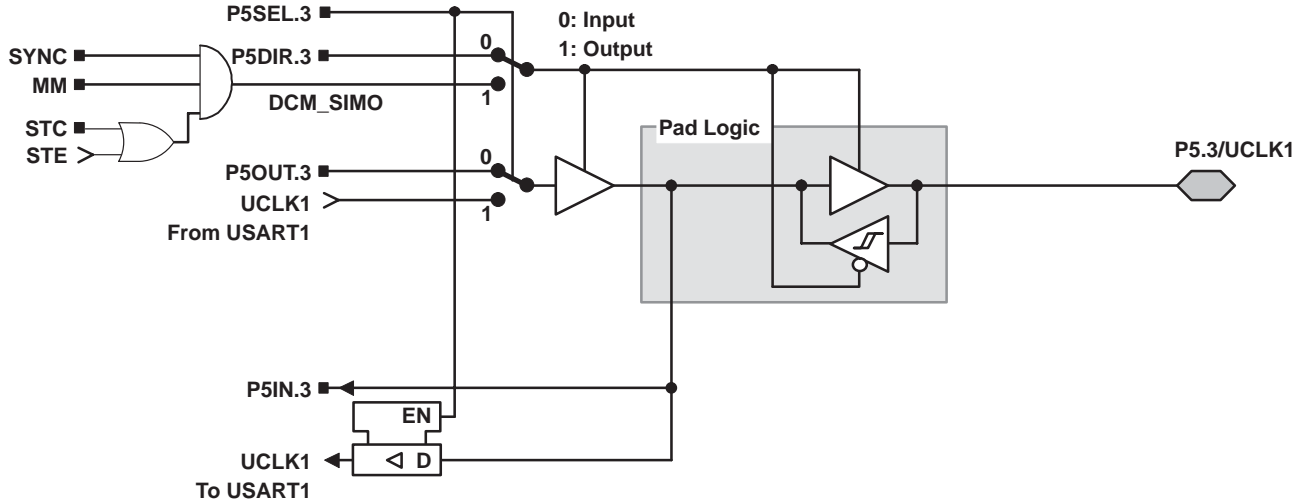
MSP430x13x, MSP430x14x, MSP430x14x1 MIXED SIGNAL MICROCONTROLLER

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APPLICATION INFORMATION

input/output schematic (continued)

port P5, P5.3, input/output with Schmitt-trigger

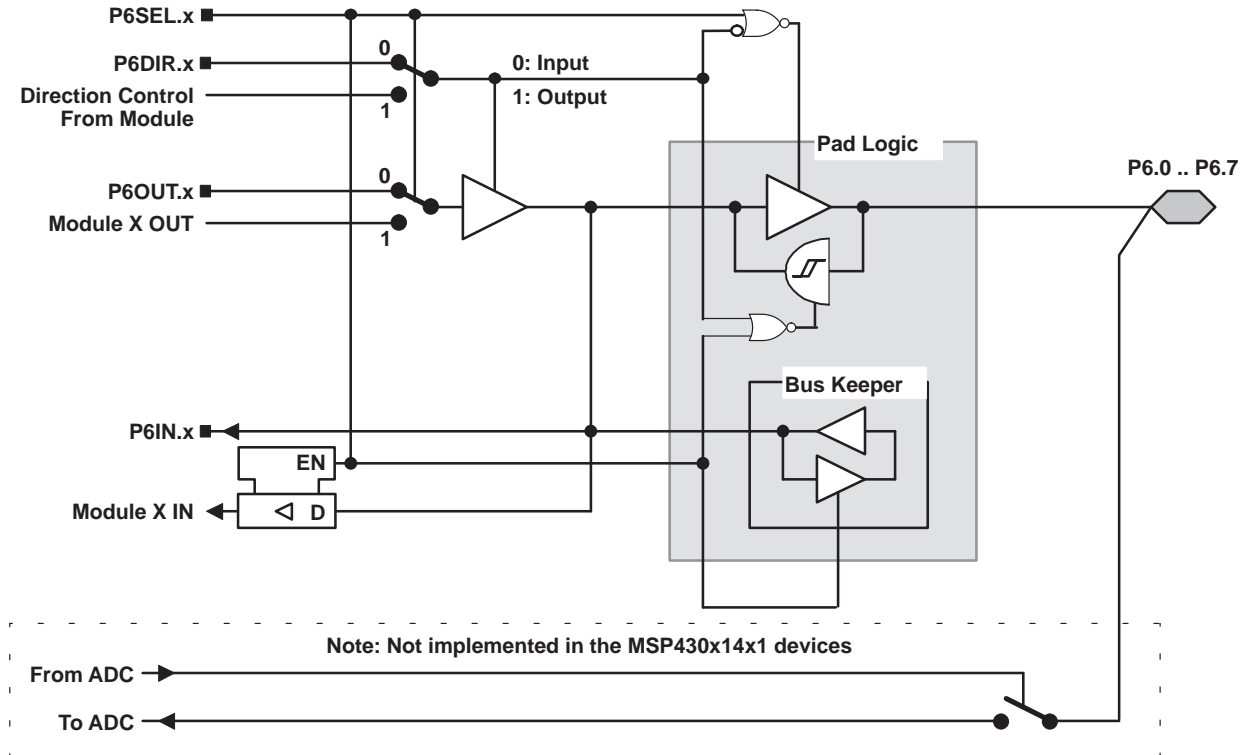


- NOTE: UART mode: The UART clock can only be an input. If UART mode and UART function are selected, the P5.3/UCLK1 direction is always input.
- SPI, slave mode: The clock applied to UCLK1 is used to shift data in and out.
- SPI, master mode: The clock to shift data in and out is supplied to connected devices on pin P5.3/UCLK1 (in slave mode).

APPLICATION INFORMATION

input/output schematic (continued)

port P6, P6.0 to P6.7, input/output with Schmitt-trigger



x: Bit Identifier, 0 to 7 for Port P6

NOTE: Analog signals applied to digital gates can cause current flow from the positive to the negative terminal. The throughput current flows if the analog signal is in the range of transitions 0→1 or 1→0. The value of the throughput current depends on the driving capability of the gate. For MSP430, it is approximately 100 μA.

Use P6SEL.x=1 to prevent throughput current. P6SEL.x should be set, even if the signal at the pin is not being used by the ADC12.

PnSel.x	PnDIR.x	DIR. CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P6Sel.0	P6DIR.0	P6DIR.0	P6OUT.0	DV _{SS}	P6IN.0	unused
P6Sel.1	P6DIR.1	P6DIR.1	P6OUT.1	DV _{SS}	P6IN.1	unused
P6Sel.2	P6DIR.2	P6DIR.2	P6OUT.2	DV _{SS}	P6IN.2	unused
P6Sel.3	P6DIR.3	P6DIR.3	P6OUT.3	DV _{SS}	P6IN.3	unused
P6Sel.4	P6DIR.4	P6DIR.4	P6OUT.4	DV _{SS}	P6IN.4	unused
P6Sel.5	P6DIR.5	P6DIR.5	P6OUT.5	DV _{SS}	P6IN.5	unused
P6Sel.6	P6DIR.6	P6DIR.6	P6OUT.6	DV _{SS}	P6IN.6	unused
P6Sel.7	P6DIR.7	P6DIR.7	P6OUT.7	DV _{SS}	P6IN.7	unused

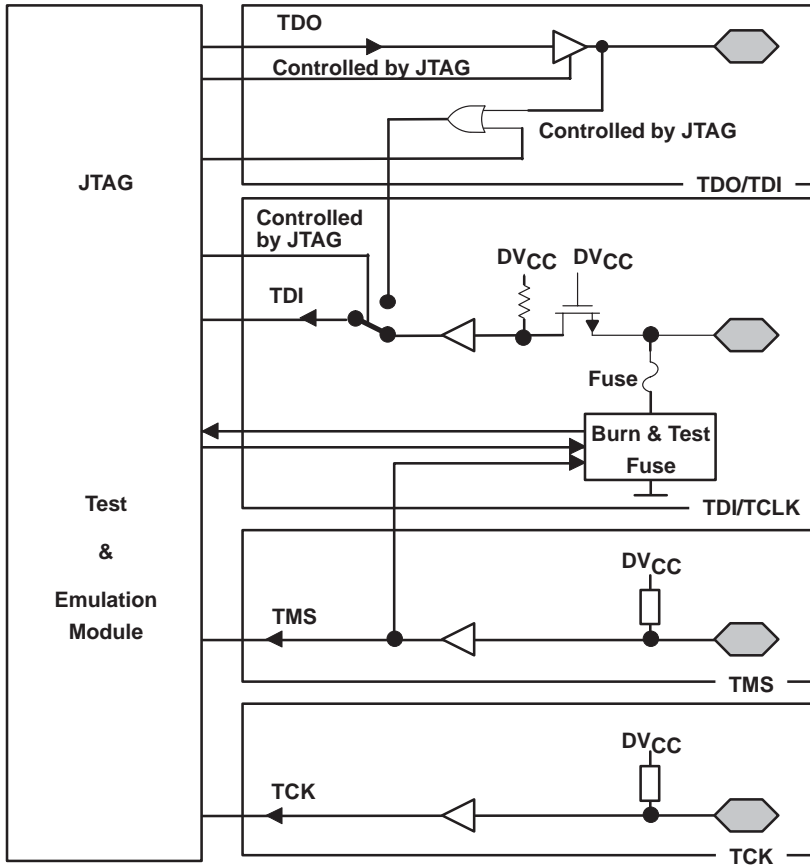
NOTE: The signal at pins P6.x/Ax is used by the 12-bit ADC module.

MSP430x13x, MSP430x14x, MSP430x14x1 MIXED SIGNAL MICROCONTROLLER

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APPLICATION INFORMATION

JTAG pins TMS, TCK, TDI/TCLK, TDO/TDI, input/output with Schmitt-trigger



During Programming Activity and During Blowing of the Fuse, Pin TDO/TDI Is Used to Apply the Test Input Data for JTAG Circuitry

APPLICATION INFORMATION

JTAG fuse check mode

MSP430 devices that have the fuse on the TDI/TCLK terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF} , of 1 mA at 3 V, 2.5 mA at 5 V can flow from the TDI/TCLK pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current will only flow when the fuse check mode is active and the TMS pin is in a low state (see Figure 16). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

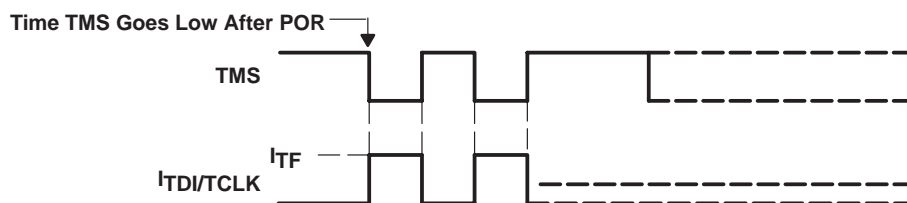


Figure 16. Fuse Check Mode Current: MSP430F13x, MSP430F14x(1)

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
MSP430A009IPMR	ACTIVE	LQFP	PM	64		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F133IPAG	ACTIVE	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR
MSP430F133IPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F133IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F133IRTDR	ACTIVE	VQFN	RTD	64	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F133IRTD	ACTIVE	VQFN	RTD	64	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F135IPAG	ACTIVE	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR
MSP430F135IPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F135IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F135IRTDR	ACTIVE	VQFN	RTD	64	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F135IRTD	ACTIVE	VQFN	RTD	64	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F1471IPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F1471IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F1471IPMRG	ACTIVE	LQFP	PM	64		TBD	Call TI	Call TI
MSP430F1471IPMRG4	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F1471IRTDR	ACTIVE	VQFN	RTD	64	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F1471IRTD	ACTIVE	VQFN	RTD	64	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F147IPAG	ACTIVE	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR
MSP430F147IPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F147IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F147IPMR-KAM	ACTIVE	LQFP	PM	64		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F147IPMRG4	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F147IRTDR	ACTIVE	VQFN	RTD	64	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F147IRTD	ACTIVE	VQFN	RTD	64	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F1481IPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
MSP430F1481IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F1481IRTDR	ACTIVE	VQFN	RTD	64	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F1481IRTD	ACTIVE	VQFN	RTD	64	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F1481PAG	ACTIVE	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR
MSP430F1481IPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F1481IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F1481IRTDR	ACTIVE	VQFN	RTD	64	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F1481IRTD	ACTIVE	VQFN	RTD	64	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F1491IPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F1491IPMG4	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F1491IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F1491IPMRG4	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F1491IRTDR	ACTIVE	VQFN	RTD	64	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F1491IRTD	ACTIVE	VQFN	RTD	64	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F1491IPAG	ACTIVE	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR
MSP430F1491PAGR	ACTIVE	TQFP	PAG	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR
MSP430F1491IPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F1491IPMG4	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F1491IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F1491IPMRG4	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F1491IRTDR	ACTIVE	VQFN	RTD	64	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F1491IRTD	ACTIVE	VQFN	RTD	64	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F133IPMR	LQFP	PM	64	1000	330.0	24.4	12.3	12.3	2.5	16.0	24.0	Q2
MSP430F135IPMR	LQFP	PM	64	1000	330.0	24.4	12.3	12.3	2.5	16.0	24.0	Q2
MSP430F1471IPMR	LQFP	PM	64	1000	330.0	24.4	12.3	12.3	2.5	16.0	24.0	Q2
MSP430F147IPMR	LQFP	PM	64	1000	330.0	24.4	12.3	12.3	2.5	16.0	24.0	Q2
MSP430F1481IPMR	LQFP	PM	64	1000	330.0	24.4	12.3	12.3	2.5	16.0	24.0	Q2
MSP430F148IPMR	LQFP	PM	64	1000	330.0	24.4	12.3	12.3	2.5	16.0	24.0	Q2
MSP430F1491IPMR	LQFP	PM	64	1000	330.0	24.4	12.3	12.3	2.5	16.0	24.0	Q2
MSP430F149IPAGR	TQFP	PAG	64	1500	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2
MSP430F149IPMR	LQFP	PM	64	1000	330.0	24.4	12.3	12.3	2.5	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS

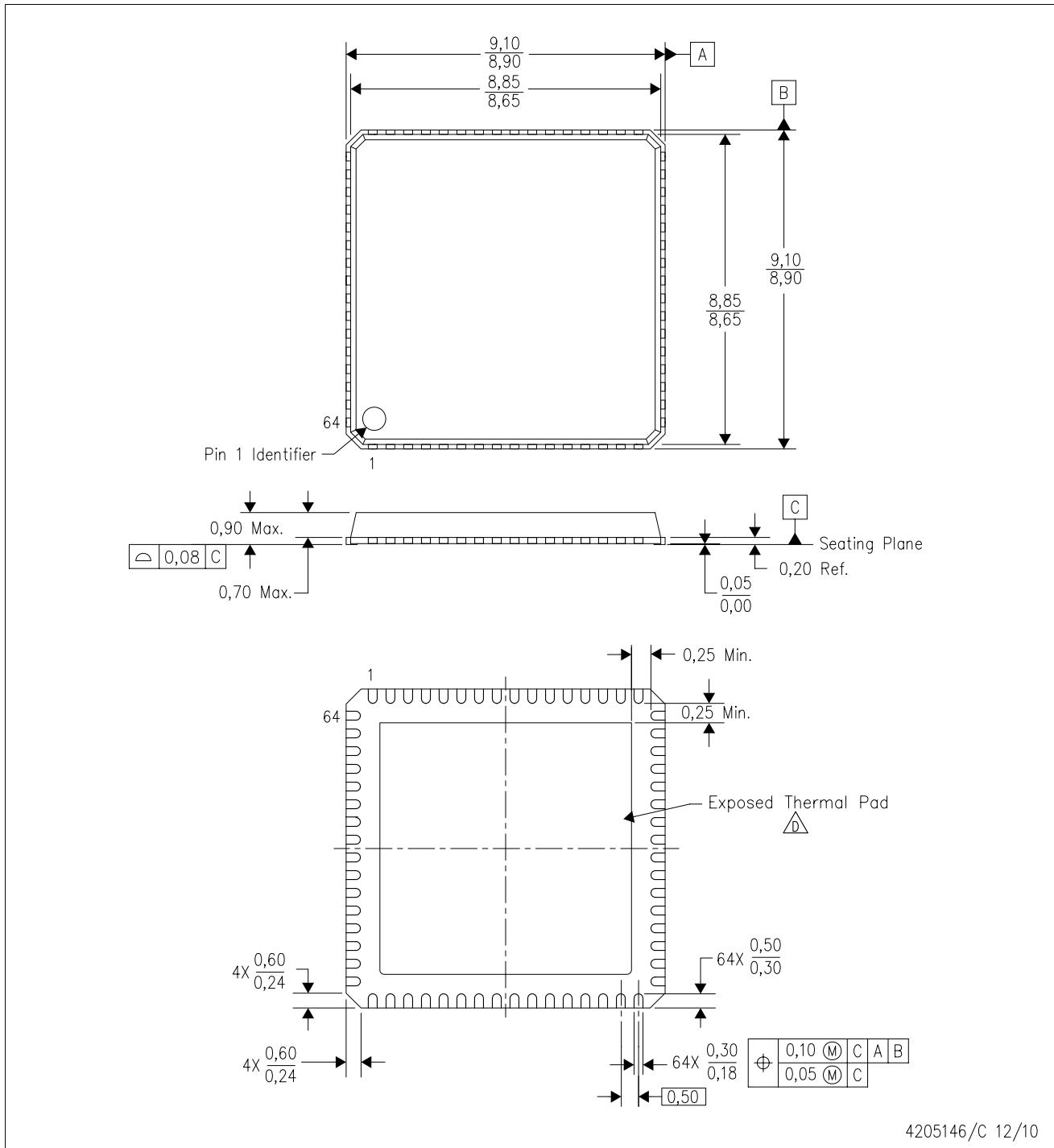

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F133IPMR	LQFP	PM	64	1000	333.2	345.9	41.3
MSP430F135IPMR	LQFP	PM	64	1000	333.2	345.9	41.3
MSP430F1471IPMR	LQFP	PM	64	1000	333.2	345.9	41.3
MSP430F147IPMR	LQFP	PM	64	1000	333.2	345.9	41.3
MSP430F1481IPMR	LQFP	PM	64	1000	333.2	345.9	41.3
MSP430F148IPMR	LQFP	PM	64	1000	333.2	345.9	41.3
MSP430F1491IPMR	LQFP	PM	64	1000	333.2	345.9	41.3
MSP430F149IPAGR	TQFP	PAG	64	1500	346.0	346.0	41.0
MSP430F149IPMR	LQFP	PM	64	1000	333.2	345.9	41.3


MECHANICAL DATA

RTD (S-PVQFN-N64)

PLASTIC QUAD FLATPACK NO-LEAD



4205146/C 12/10

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) Package configuration.
 -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

RTD (S-PVQFN-N64)

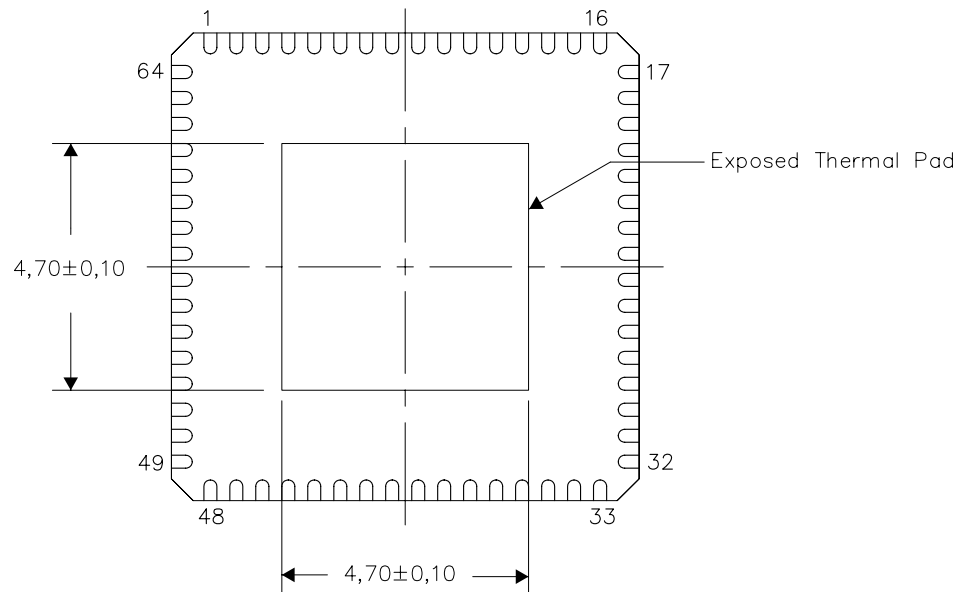
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

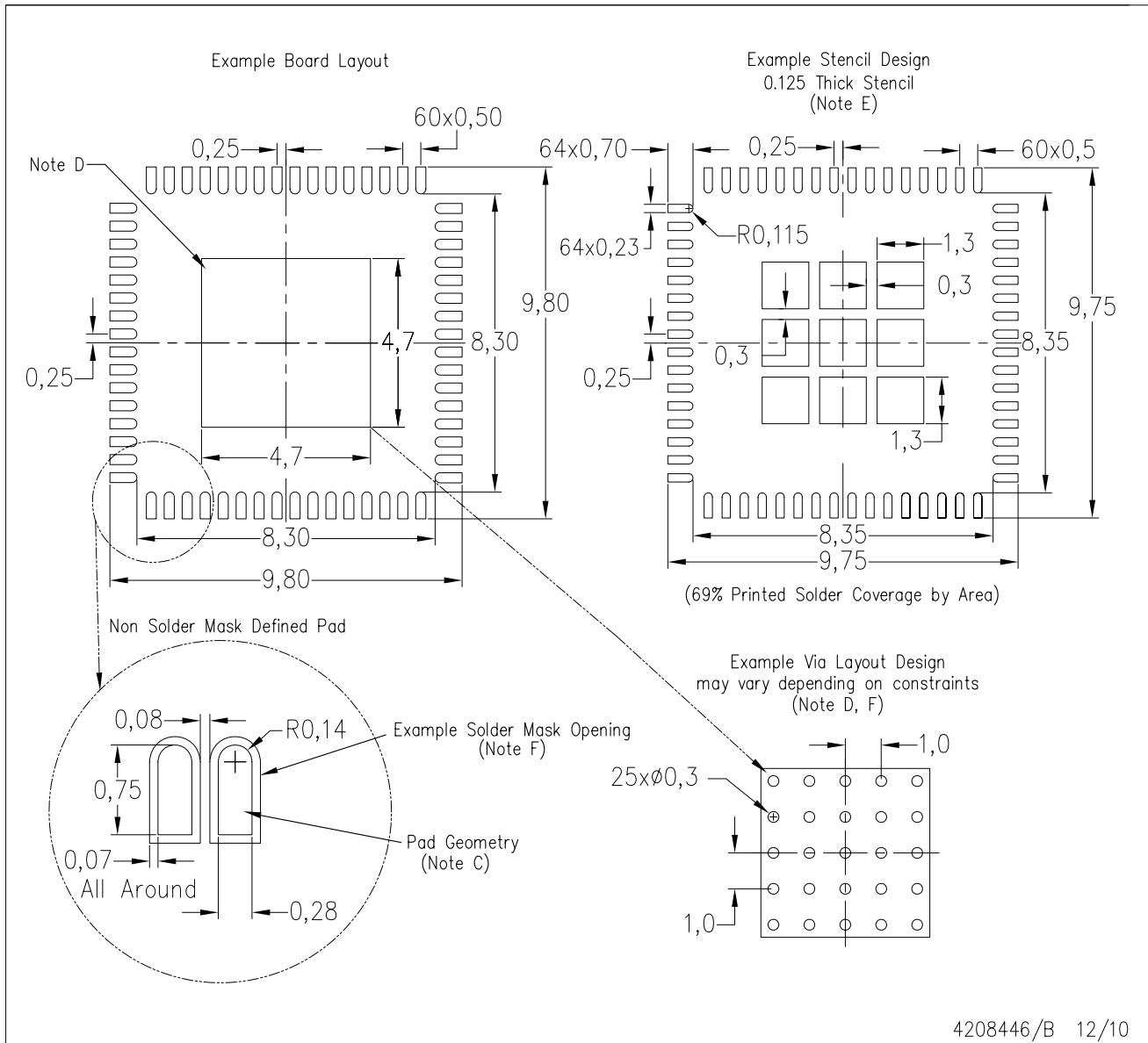
Exposed Thermal Pad Dimensions

4206338-3/E 12/10

NOTE: A. All linear dimensions are in millimeters

RTD (S-PVQFN-N64)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Package, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with electropolish and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customer should contact their board fabrication site for recommended solder mask tolerances and vias tenting recommendations for vias placed into the thermal pad.

PAG (S-PQFP-G64)

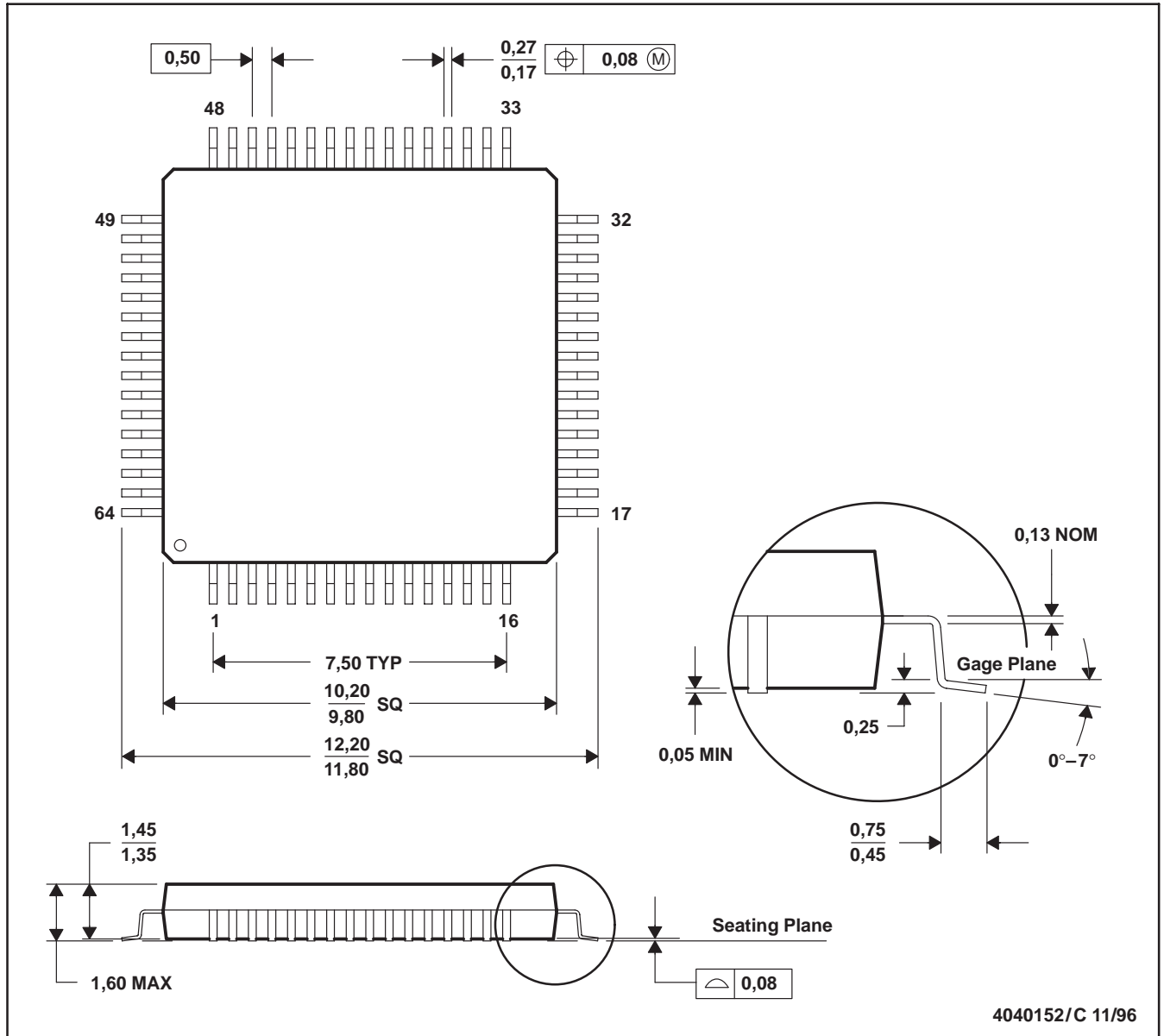
PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026

PM (S-PQFP-G64)

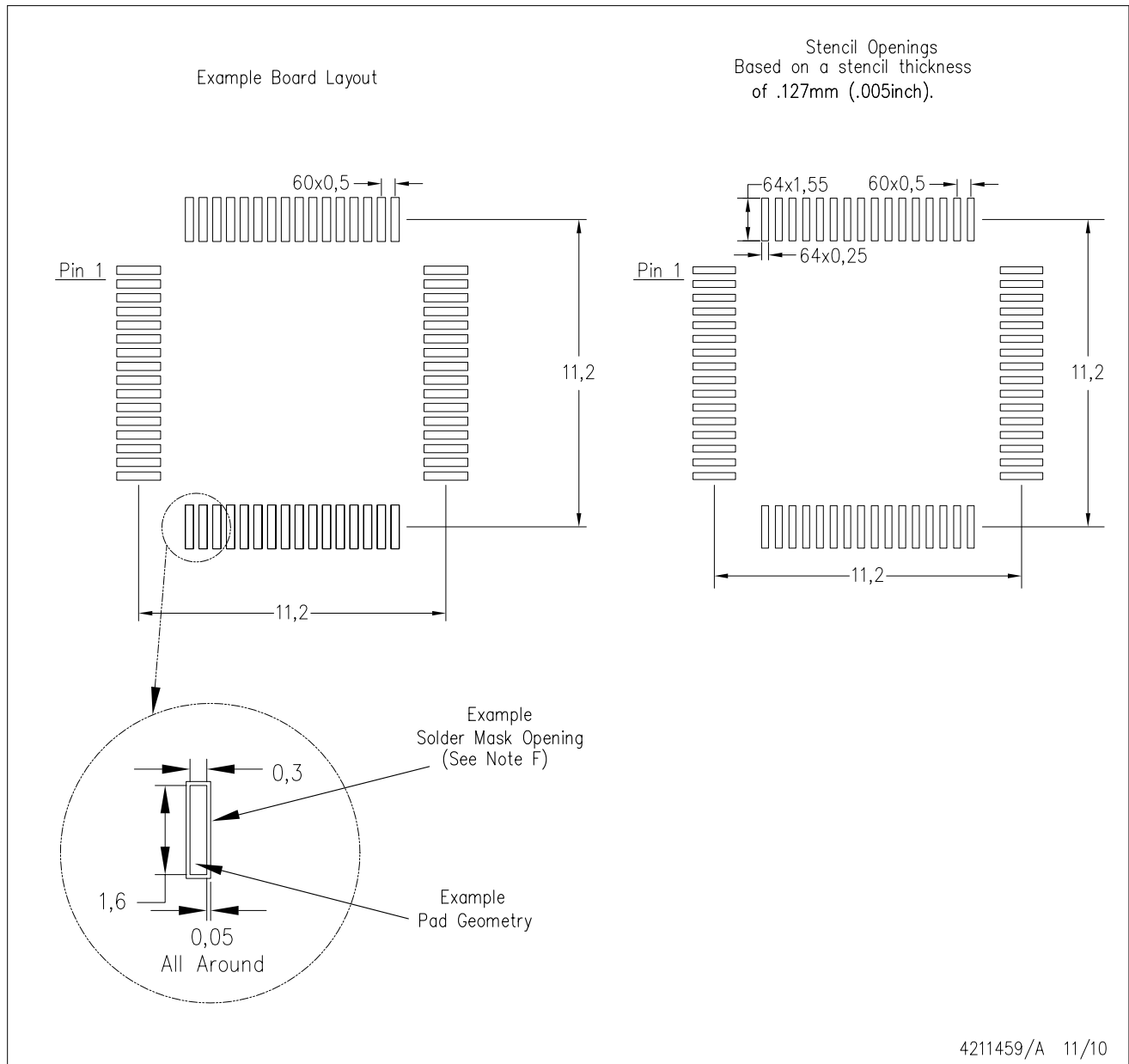
PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026
 D. May also be thermally enhanced plastic with leads connected to the die pads.

PM (S-PQFP-G64)

PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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