Feature

CAS Latency Frequency

Speed Sorts		DDR-333 -6K/-6KI	DDR400 -5T/-5TI	DDR500 -4T	Units
CL-tRCD-tRP		2.5-3-3	3-3-3	3-4-4	tCK
Speed	CL=2	266	266	-	Mbps
	CL=2.5	333	333	333	
	CL=3	333	400	500	

- Power Supply Voltage:
  $V_{DD}=V_{DDQ}=2.5V\pm0.2V$ (DDR-333)
  $V_{DD}=V_{DDQ}=2.6V\pm0.1V$ (DDR-400/500)
- 4 internal memory banks for concurrent operation.
- CAS Latency: 2, 2.5 and 3
- Double Data Rate Architecture
- Bidirectional data strobe (DQS) is transmitted and received with data, to be used in capturing data at the receiver.
- Industrial grade device support -40℃~85℃ Operating Temperature (-75I/-6KI/5TI)
- Commercial grade device support 0℃~70℃ Operating Temperature (-75/-6K/5T)
- 2KB page size for all configurations.
- DQS is edge-aligned with data for reads and is center-aligned with data for WRITEs
- Differential clock inputs (CK and $\overline{CK}$)
- Data mask (DM) for write data
- DLL aligns DQ and DQS transition with CK transitions.
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Burst Lengths: 2, 4 or 8
- Auto Precharge option for each burst access
- Auto-Refresh and Self-Refresh Mode
- 7.8 µs max. Average Periodic Refresh Interval
- 2.5V (SSTL_2 compatible) I/O
- RoHS and Halogen-Free compliance
- Packages: 66 pin TSOPII

Description

Nanya 512Mb SDRAMs is a high-speed CMOS Double Data Rate SDRAM containing 536,870,912 bits. It is internally configured as a qual-bank DRAM.

The 512Mb chip is organized as 16Mbit x 8 I/O x 4 bank or 8Mbit x 16 I/O x 4 bank device. These synchronous devices achieve high speed double-data-rate transfer rates of up to 500 (400, 333 or 266) MHz for general applications.

The 512Mb DDR SDRAM uses a double-data-rate architecture to achieve high speed operation. The double data rate architecture is essentially a 2η prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 512Mb DDR SDRAM effectively consists of a single *2n*-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during Reads and by the memory controller during Writes. DQS is edge-aligned with data for Reads and center-aligned with data for Writes.

The 512Mb DDR SDRAM operates from a differential clock (CK and $\overline{CK}$; the crossing of CK going high and $\overline{CK}$ going LOW is referred to as the positive edge of CK). Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active

command are used to select the bank and row to be accessed. The address bits registered coincident with the Read or Write command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable Read or Write burst lengths of 2, 4, or 8 locations. An Auto Precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided along with a power-saving Power Down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible.

The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

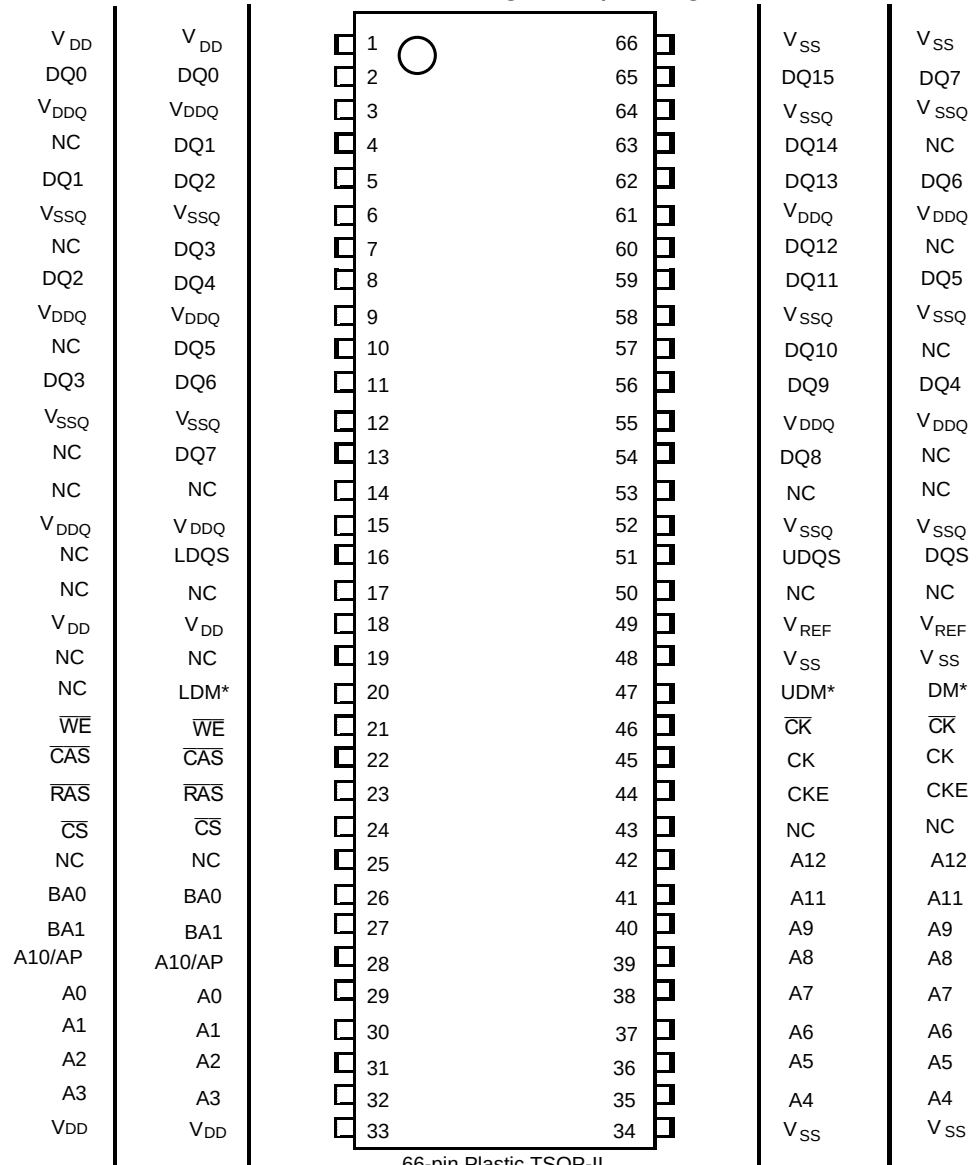
Ordering Information

Standard Grade				
Organization	**Part Number**	**Package**	**Speed[1]**	
			Clock (MHz)	**CL-T_{RCD}-T_{RP}**
64M x 8	NT5DS64M8DS – 6K	66 pin TSOP-II	166	2.5-3-3
	NT5DS64M8DS – 5T		200	3-3-3
32M x 16	NT5DS32M16DS – 6K		166	2.5-3-3
	NT5DS32M16DS – 5T		200	3-3-3
Industrial Grade				
Organization	**Part Number**	**Package**	**Speed[1]**	
			Clock (MHz)	**CL-T_{RCD}-T_{RP}**
64M x 8	NT5DS64M8DS – 6KI	66 pin TSOP-II	166	2.5-3-3
	NT5DS64M8DS – 5TI		200	3-3-3
32M x 16	NT5DS32M16DS – 6KI		166	2.5-3-3
	NT5DS32M16DS – 5TI		200	3-3-3

NOTE : The specification of high speed bin is backward compatible with low speed bin.

Pin Configuration – 400 mil TSOP II (x4 / x8 / x16)

< TOP View>
See the balls through the package

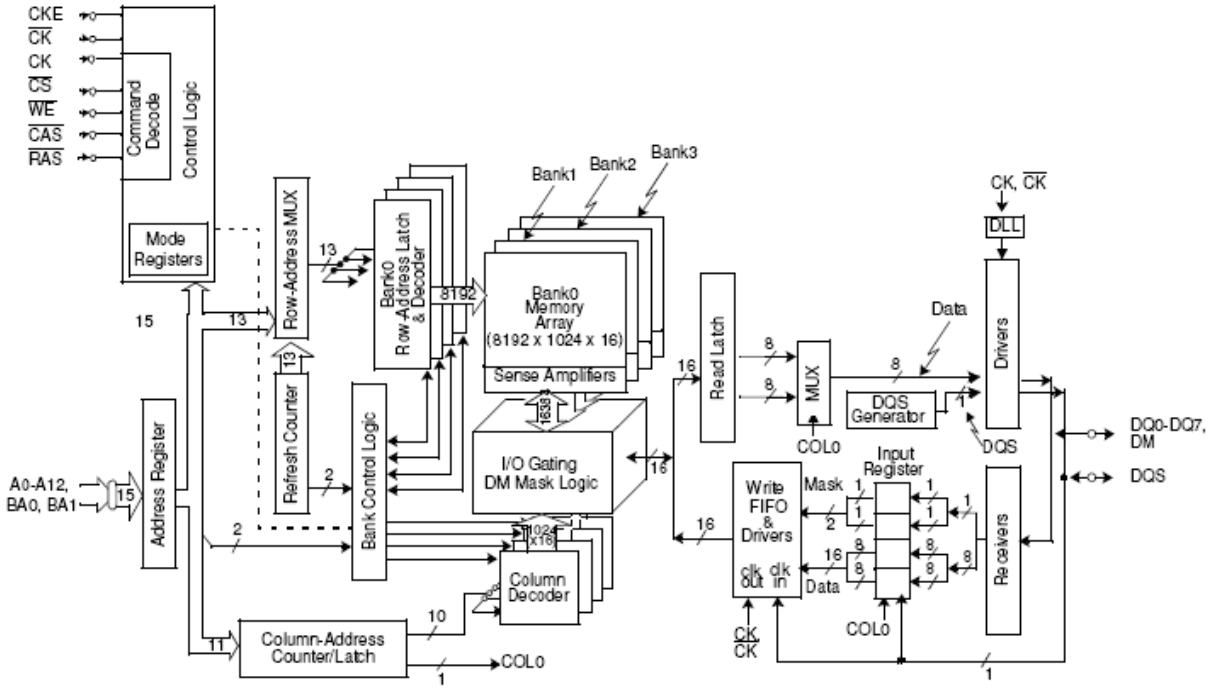


Organization	Column Address
64Mb x 8	A0-A9, A11
32Mb x 16	A0-A9

Input / Output Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER--DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER--DOWN (row ACTIVE in any bank). CKE is synchronous for POWER-- DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit, and for output disable. CKE must be maintained high throughout READ and WRITE accesses. Input buffers, excluding CK, CK and CKE are disabled during POWER--DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after Vdd is applied upon 1st power up. After VREF has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self--refresh entry and exit, VREF must be maintained to this input The standard pinout includes one CKE pin. Optional pinouts include CKE0 and CKE1 on different pins, to facilitate device stacking.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered high. $\overline{CS}$ provides for external rank selection on systems with multiple memory ranks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM, LDM, UDM	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For the X16, LDM corresponds to the data on DQ0--DQ7; UDM corresponds to the data on DQ8--DQ15. DM may be driven high, low, or floating during READs.
BA0 – BA1	Input	**Bank Address Inputs:** BA# defines to which bank an Active, Read, Write or Pre-charge command is being applied.
A0 – A12	Input	**Address Inputs:** Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op--code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS).
DQ	Input/output	**Data Bus:** Inputs/Output
DQS, ($\overline{DQS}$) LDQS, ($\overline{LDQS}$), UDQS,($\overline{UDQS}$)	Input/output	**Data Strobe:** Output with read data, input with write data. Edge--aligned with read data, centered in write data. Used to capture write data. For the X16, LDQS corresponds to the data on DQ0--DQ7; UDQS corresponds to the data on DQ8--DQ15.
RDQS, ($\overline{RDQS}$)	Input/output	**Read Data Strobe:** For x8 components a RDQS and $\overline{RDQS}$ pair can be enabled via EMRS(1) for real timing. RDQS and $\overline{RDQS}$ is not support x16 components. RDQS and $\overline{RDQS}$ are edge-aligned with real data. If enable RDQS and $\overline{RDQS}$ then DM function will be disabled.
NC		**No Connect:** No internal electrical connection is present.
V_{DDQ}	Supply	**DQ Power Supply:** 2.5V ± 0.2V (-6K/-6KI); VDD=VDDQ=2.6V±0.1V (-5T/-5TI/-4T)
V_{SSQ}	Supply	**DQ Ground**
V_{DD}	Supply	**Power Supply:** 2.5V ± 0.2V (-6K/-6KI); VDD=VDDQ=2.6V±0.1V (-5T/-5TI/-4T)
V_{SS}	Supply	**Ground**
V_{REF}	Supply	**SSTL_2 reference voltage**

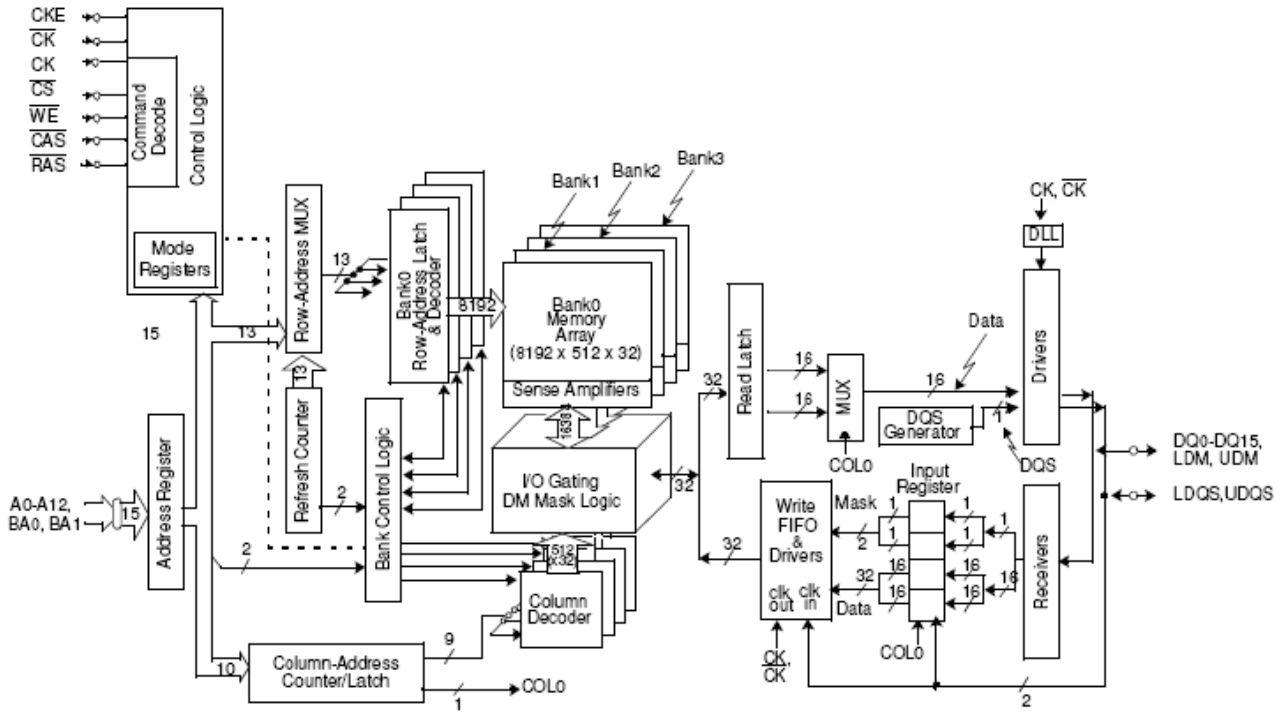
Block Diagram (64Mb x 8)



Note: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note: DM is a unidirectional signal (input only), but is internally loaded to match the load of the bidirectional DQ and DQS signals.

Block Diagram (32Mb x 16)



Note: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note: UDM and LDM are unidirectional signals (input only), but is internally loaded to match the load of the bidirectional DQ, UDQS, and LDQS signals.

Functional Description

The 512Mb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. The 512Mb DDR SDRAM is internally configured as a quad-bank DRAM.

The 512Mb DDR SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double-data-rate architecture is essentially a *2n* prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 512Mb DDR SDRAM consists of a single *2n*-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A12 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access.

Prior to normal operation, the DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Initialization

Only one of the following two conditions must be met.

• No power sequencing is specified during power up or power down given the following criteria:

V_{DD} and V_{DDQ} are driven from a single power converter output

V_{TT} meets the specification

A minimum resistance of 42 ohms limits the input current from the VTT supply into any pin and

V_{REF} tracks V_{DDQ} /2

or

• The following relationships must be followed:

V_{DDQ} is driven after or with V_{DD} such that $V_{DDQ} < V_{DD} + 0.3V$

V_{TT} is driven after or with V_{DDQ} such that $V_{TT} < V_{DDQ} + 0.3V$

V_{REF} is driven after or with V_{DDQ} such that $V_{REF} < V_{DDQ} + 0.3V$

The DQ and DQS outputs are in the High-Z state, where they remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200μs delay prior to applying an executable command.

Once the 200μs delay has been satisfied, a Deselect or NOP command should be applied, and CKE must be brought HIGH. Following the NOP command, a Precharge ALL command must be applied. Next a Mode Register Set command must be issued for the Extended Mode Register, to enable the DLL, and then a Mode Register Set command must be issued for the Mode Register, to reset the DLL, and to program the operating parameters. 200 clock cycles are required between the DLL reset and any read command. A Precharge ALL command should be applied, placing the device in the “all banks idle” state

Once in the idle state, two auto refresh cycles must be performed. Additionally, a Mode Register Set command for the Mode Register, with the reset DLL bit deactivated (i.e. to program operating parameters without resetting the DLL) must be performed. Following these cycles, the DDR SDRAM is ready for normal operation.

DDR SDRAM’s may be reinitialized at any time during normal operation by asserting a valid MRS command to either the base or extended mode registers without affecting the contents of the memory array. The contents of either the mode register or extended mode register can be modified at any valid time during device operation without affecting the state of the internal address refresh counters used for device refresh.

Register Definition

Mode Register

The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, and an operating mode. The Mode Register is programmed via the Mode Register Set command (with BA0 = 0 and BA1 = 0) and retains the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

Mode Register bits A0-A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4-A6 specify the CAS latency, and A7-A12 specify the operating mode.

The Mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements results in unspecified operation.

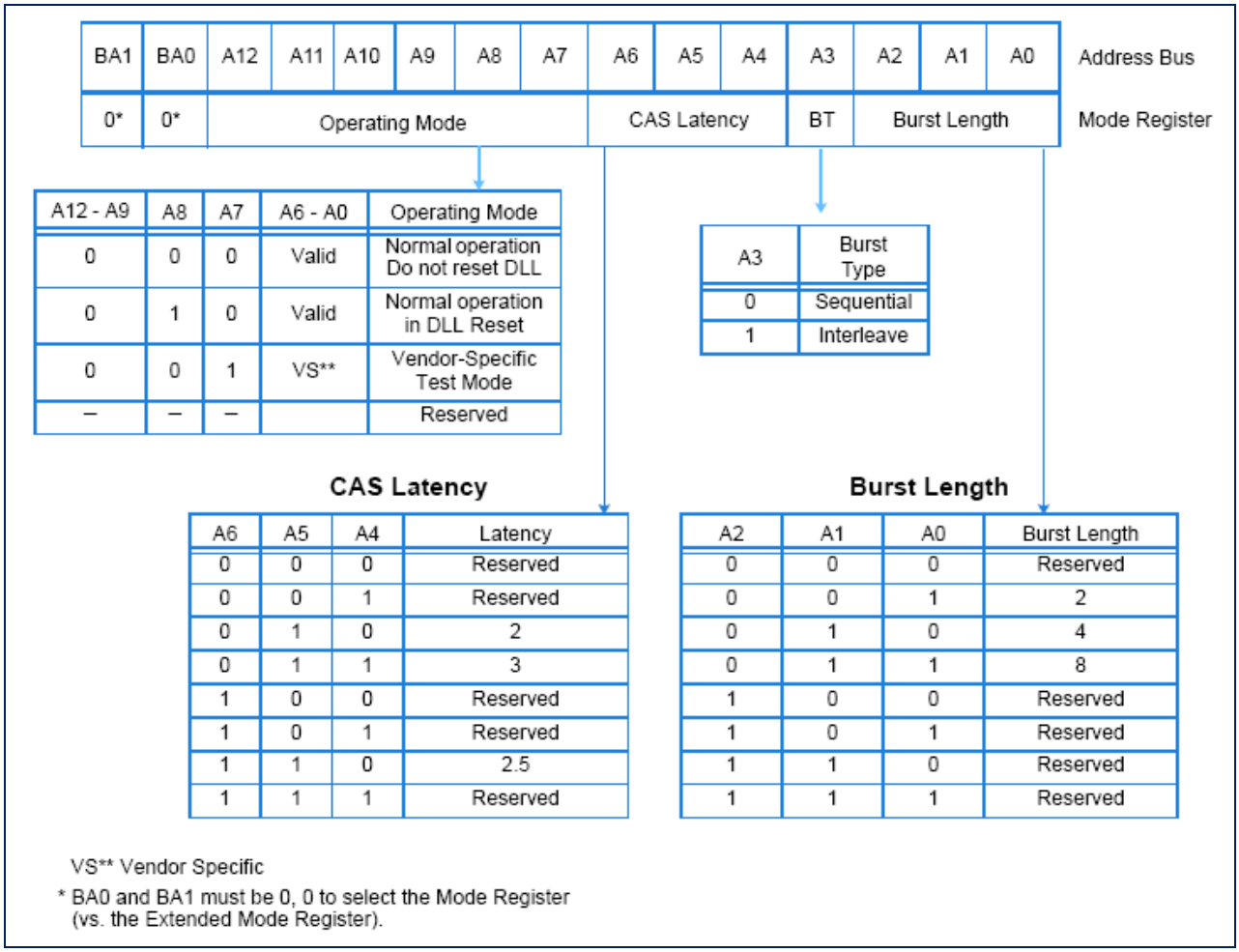
Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable. The burst length determines the maximum number of column locations that can be accessed for a given Read or Write command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a Read or Write command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst wraps within the block if a boundary is reached. The block is uniquely selected by A1-Ai when the burst length is set to two, by A_2-Ai when the burst length is set to four and by A_3-Ai when the burst length is set to eight (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both Read and Write bursts.

Mode Register Operation



BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
															Address Bus
0*	0*	Operating Mode						CAS Latency			BT	Burst Length			Mode Register

A12 - A9	A8	A7	A6 - A0	Operating Mode
0	0	0	Valid	Normal operation Do not reset DLL
0	1	0	Valid	Normal operation in DLL Reset
0	0	1	VS**	Vendor-Specific Test Mode
–	–	–		Reserved

A3	Burst Type
0	Sequential
1	Interleave

CAS Latency

A6	A5	A4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	2.5
1	1	1	Reserved

Burst Length

A2	A1	A0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

VS** Vendor Specific

* BA0 and BA1 must be 0, 0 to select the Mode Register (vs. the Extended Mode Register).

Burst Definition

Burst Length	Starting Colume Address			Order of Accesses Within a Burst	
	A2	A1	A0	Type=Sequential	Type=Interleaved
2	-	-	0	0-1	0-1
	-	-	1	1-0	1-0
4	-	0	0	0-1-2-3	0-1-2-3
	-	0	1	1-2-3-0	1-0-3-2
	-	1	0	2-3-0-1	2-3-0-1
	-	1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

Notes:

1. For a burst length of two, A1-A i selects the two-data-element block; A0 selects the first access within the block.
2. For a burst length of four, A2-A i selects the four-data-element block; A0-A1 selects the first access within the block.
3. For a burst length of eight, A3-A i selects the eight-data- element block; A0-A2 selects the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3. The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Burst Definition.

Read Latency

The Read latency, or CAS latency, is the delay, in clock cycles, between the registration of a Read command and the availability of the first burst of output data. The latency can be programmed 2 or 2.5 clocks for DDR266/333 and 3 clocks for DDR400/450/500.

If a Read command is registered at clock edge n, and the latency is *m* clocks, the data is available nominally coincident with clock edge *n* + m.

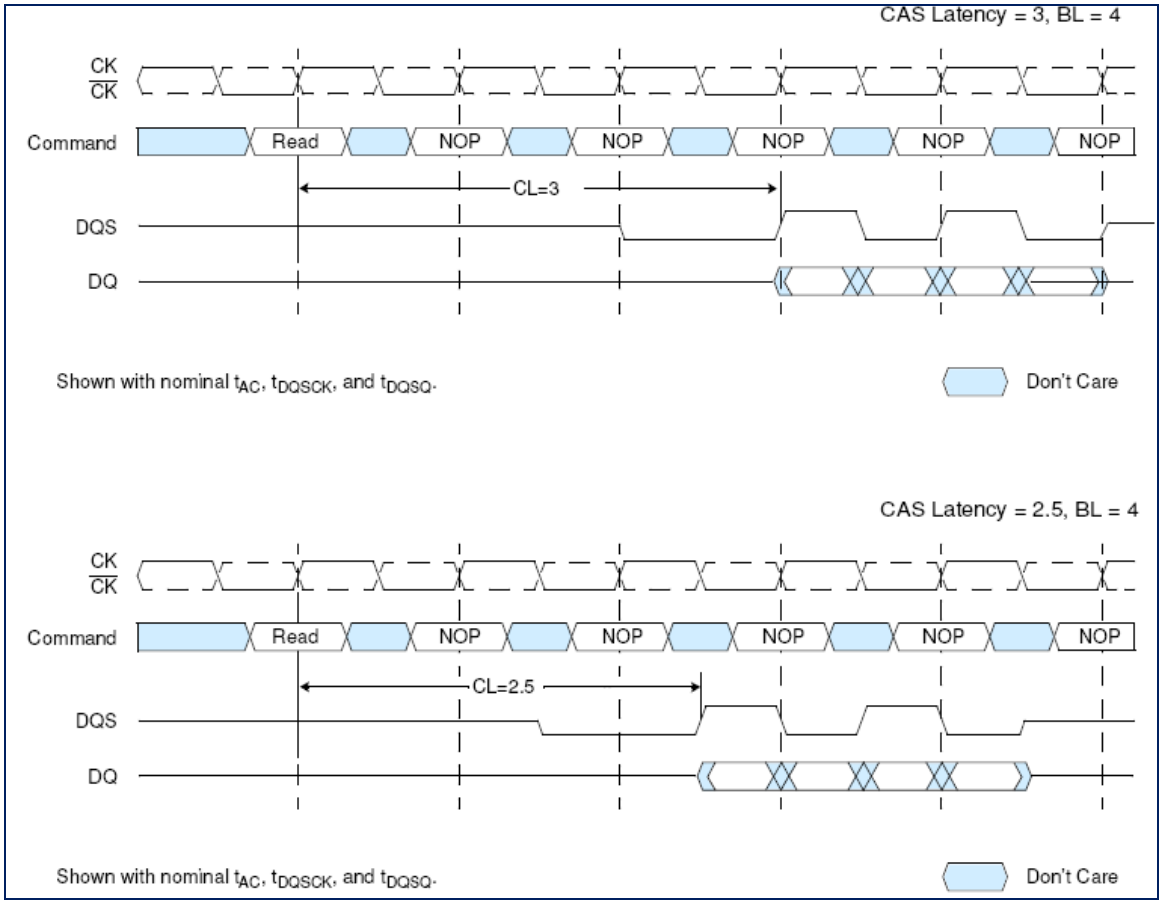
Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Operating Mode

The normal operating mode is selected by issuing a Mode Register Set Command with bits A7-A12 to zero, and bits A0-A6 set to the desired values. A DLL reset is initiated by issuing a Mode Register Set command with bits A7 and A9-A12 each set to zero, bit A8 set to one, and bits A0-A6 set to the desired values. A Mode Register Set command issued to reset the DLL should always be followed by a Mode Register Set command to select normal operating mode.

All other combinations of values for A7-A12 are reserved for future use and/or test modes. Test modes and reserved states should not be used as unknown operation or incompatibility with future versions may result.

CAS Latencies



Extended Mode Register

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable, bit A0; output drive strength selection, bit A1; and QFC output enable/disable, bit A2 (NTC optional). These functions are controlled via the bit settings shown in the Extended Mode Register Definition. The Extended Mode Register is programmed via the Mode Register Set command (with BA0 = 1 and BA1 = 0) and retains the stored information until it is programmed again or the device loses power. The Extended Mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements result in unspecified operation.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled, 200 clock cycles must occur to allow time for the internal clock to lock to the externally applied clock before a Read command can be issued. This is the reason for introducing timing parameter tXSRD for DDR SDRAM's (Exit Self Refresh to Read Command). Non- Read commands can be issued 2 clocks after the DLL is enabled via the EMRS command (tMRD) or 10 clocks after the DLL is enabled via self refresh exit command (tXSNR, Exit Self Refresh to Non-Read Command).

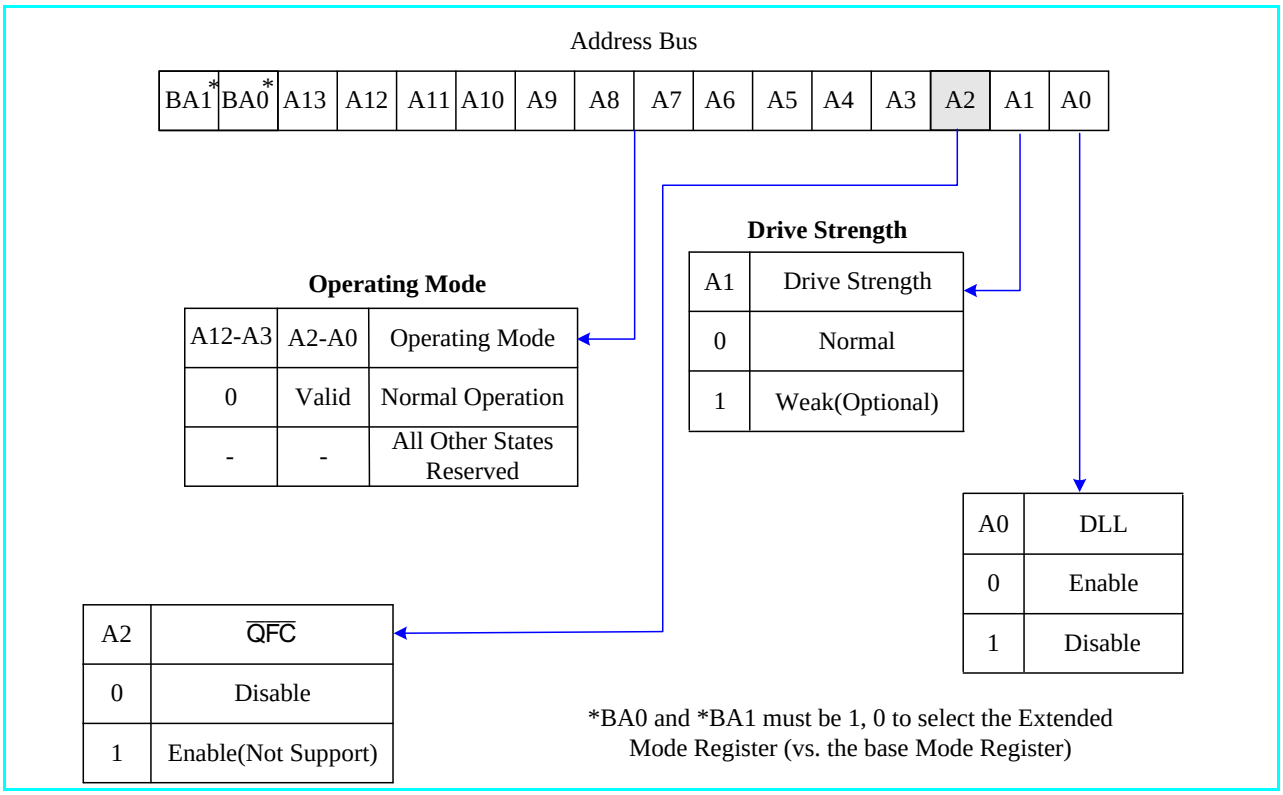
Output Drive Strength

The normal drive strength for all outputs is specified to be SSTL_2, Class II.

QFC Enable/Disable (Not support in this product; Only for information)

The QFC signal is an optional DRAM output control used to isolate module loads (DIMMs) from the system memory bus by means of external FET switches when the given module (DIMM) is not being accessed. The QFC function is an optional feature for NANYA and is not included on all DDR SDRAM devices.

Extended Mode Register Definition



Commands

Truth Tables 1a and 1b provide a reference of the commands supported by DDR SDRAM devices. A verbal description of each command follows.

Truth Table 1a Commands

Name (Function)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	MNE	Notes
Deselect (Nop)	H	X	X	X	X	NOP	1,9
No Operation (Nop)	L	H	H	H	X	NOP	1,9
Active (Select Bank and Activate Row)	L	L	H	H	Bank / Row	ACT	1,3
Read (Select Bank, Column and Start Read Burst)	L	H	L	H	Bank / Col	Read	1,4
Write (Select Bank, Column and Start Write Burst)	L	H	L	L	Bank / Col	Write	1,4
Burst Terminate	L	H	H	L	X	BST	1,8
Pre-Charge (Deactivate Row In Bank or Banks)	L	L	H	L	Code	PRE	1,5
Auto Refresh or Self Refresh (Enter Self Refresh Mode)	L	L	L	H	X	AR/SR	1,6,7
Mode Register Set	L	L	L	L	Op-Code	MRS	1,2

1. CKE is high for all commands shown except Self Refresh.
2. BA0, BA1 select either the Base or the Extended Mode Register (BA0 = 0, BA1 = 0 selects Mode Register; BA0 = 1, BA1 = 0 selects Extended Mode Register; other combinations of BA0-BA1 are reserved; A0-A12 provide the op-code to be written to the selected Mode Register.)
3. BA0-BA1 provides bank address and A0-A12 provides row address.
4. BA0, BA1 provide bank address; A0-A*i* provide column address (where *i* = 9 for x8 and 9, 11 for x4); A10 high enables the Auto Precharge feature (non-persistent), A10 low disables the Auto Precharge feature.
5. A10 LOW: BA0, BA1 determine which bank is precharged.
A10 HIGH: all banks are precharged and BA0, BA1 are “Don’t Care.”
6. This command is auto refresh if CKE is high; Self Refresh if CKE is low.
7. Internal refresh counter controls row and bank addressing; all inputs and I/Os are “Don’t Care” except for CKE.
8. Applies only to read bursts with Auto Precharge disabled; this command is undefined (and should not be used) for read bursts with AutoPrecharge enabled or for write bursts.
9. Deselect and NOP are functionally interchangeable.

Truth Table 1b: DM Operation

Name (Function)	DM	DQs	Note
Write Enable	L	Valid	1
Write Inhubit	H	X	1
1. Used to mask write data; provided coincident with the corresponding data.			

Deselect
The Deselect function prevents new commands from being executed by the DDR SDRAM. The DDR SDRAM is effectively deselected. Operations already in progress are not affected.

No Operation (NOP)
The No Operation (NOP) command is used to perform a NOP to a DDR SDRAM. This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

Mode Register Set
The mode registers are loaded via inputs A0-A12, BA0 and BA1 while issuing the Mode Register Set Command. See mode register descriptions in the Register Definition section. The Mode Register Set command can only be issued when all banks are idle and no bursts are in progress. A subsequent executable command cannot be issued until tMRD is met.

Active
The Active command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A12 selects the row. This row remains active (or open) for accesses until a Precharge (or Read or Write with Auto Precharge) is issued to that bank. A Precharge (or Read or Write with Auto Precharge) command must be issued and completed before opening a different row in the same bank.

Read
The Read command is used to initiate a burst read access to an active (open) row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-Ai, Aj (where [i = 9, j = don't care] for x8; where [i = 9, j = 11] for x4) selects the starting column location. The value on input A10 determines whether or not Auto Precharge is used. If Auto Precharge is selected, the row being accessed is precharged at the end of the Read burst; if Auto Precharge is not selected, the row remains open for subsequent accesses.

Write
The Write command is used to initiate a burst write access to an active (open) row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-Ai, Aj (where [i = 9, j = don't care] for x8; where [i = 9, j = 11] for x4) selects the starting column location. The value on input A10 determines whether or not Auto Precharge is used. If Auto Precharge is selected, the row being accessed is precharged at the end of the Write burst; if Auto Precharge is not selected, the row remains open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered low, the corresponding data is written to memory; if the DM signal is registered high, the corresponding data inputs are ignored, and a Write is not executed to that byte/column location.

Precharge
The Precharge command is used to deactivate (close) the open row in a particular bank or the open row(s) in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the Precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any Read or Write commands being issued to that bank. A precharge command is treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.

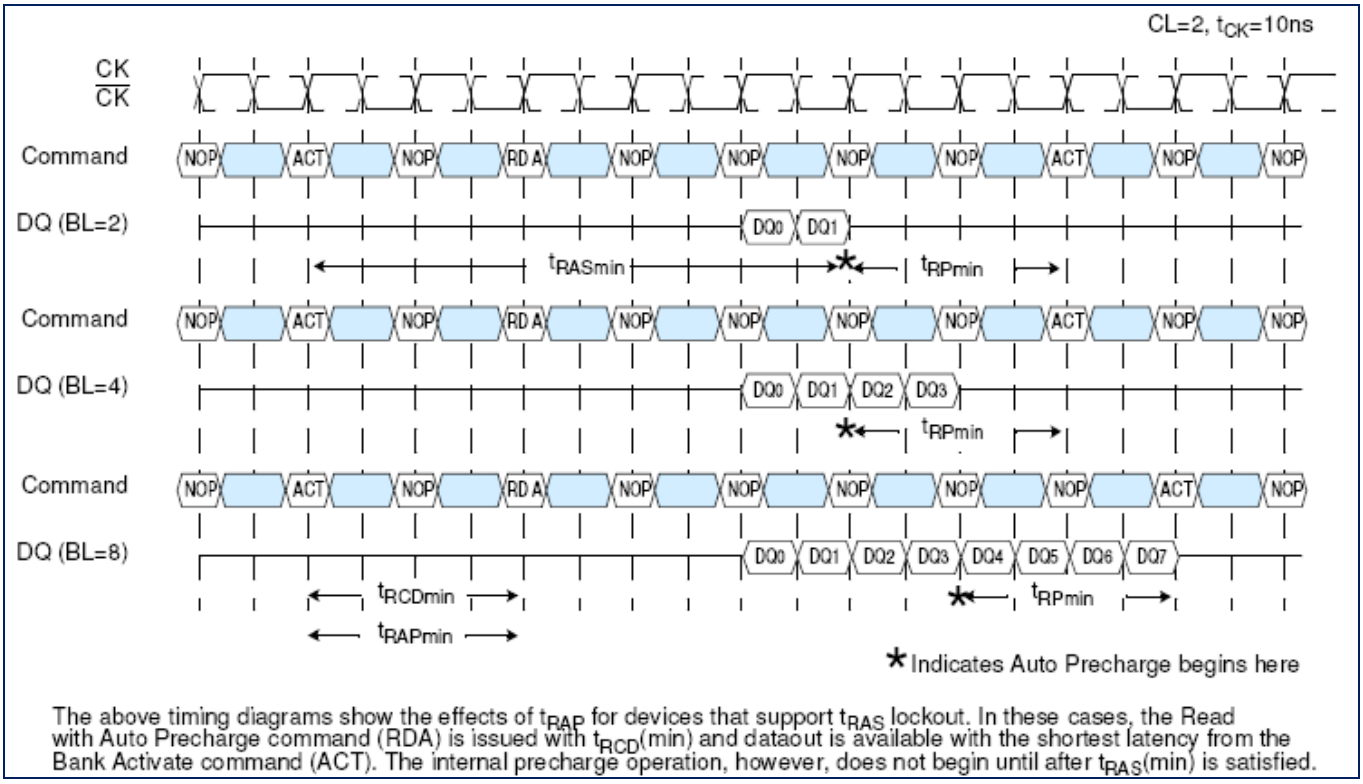
Auto Precharge

Auto Precharge is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable Auto Precharge in conjunction with a specific Read or Write command. A precharge of the bank/row that is addressed with the Read or Write command is automatically performed upon completion of the Read or Write burst. Auto Precharge is non-persistent in that it is either enabled or disabled for each individual Read or Write command. Auto Precharge ensures that the precharge is initiated at the earliest valid stage within a burst. This is determined as if an explicit Precharge command was issued at the earliest possible time without violating t_{RAS}(min). The user must not issue another command to the same bank until the precharge (t_{RP}) is completed.

The NTC DDR SDRAM device supports the optional t_{RAS} lockout feature. This feature allows a Read command with Auto Precharge to be issued to a bank that has been activated (opened) but has not yet satisfied the t_{RAS}(min) specification. The t_{RAS} lockout feature essentially delays the onset of the auto precharge operation until two conditions occur. One, the entire burst length of data has been successfully prefetched from the memory array; and two, t_{RAS}(min) has been satisfied.

As a means to specify whether a DDR SDRAM device supports the t_{RAS} lockout feature, a new parameter has been defined; t_{RAP} (RAS Command to Read Command with Auto Precharge or better stated Bank Activate to Read Command with Auto Precharge). For devices that support the t_{RAS} lockout feature, $t_{RAP} = t_{RCD}$(min). This allows any Read Command (with or without Auto Precharge) to be issued to an open bank once t_{RCD}(min) is satisfied.

t_{RAP} Definition



The above timing diagrams show the effects of t_{RAP} for devices that support t_{RAS} lockout. In these cases, the Read with Auto Precharge command (RDA) is issued with t_{RCD}(min) and dataout is available with the shortest latency from the Bank Activate command (ACT). The internal precharge operation, however, does not begin until after t_{RAS}(min) is satisfied.

Burst Terminate

The Burst Terminate command is used to truncate read bursts (with Auto Precharge disabled). The most re-cently registered Read command prior to the Burst Terminate command is truncated, as shown in the Operation section of this data sheet. Write burst cycles are not to be terminated with the Burst Terminate command.

Auto Refresh

Auto Refresh is used during normal operation of the DDR SDRAM and is analogous to CAS Before RAS (CBR) Refresh in previous DRAM types. This command is nonpersistent, so it must be issued each time a refresh is required.
The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an Auto Refresh command. The 512Mb DDR SDRAM requires Auto Refresh cycles at an average periodic interval of 7.8µs (maximum).

Self Refresh

The Self Refresh command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR SDRAM retains data without external clocking. The Self Refresh command is initiated as an Auto Refresh command coincident with CKE transitioning low. The DLL is automatically disabled upon entering Self Refresh, and is automatically enabled upon exiting Self Refresh (200 clock cycles must then occur before a Read command can be issued). Input signals except CKE (low) are "Don't Care" during Self Refresh operation.

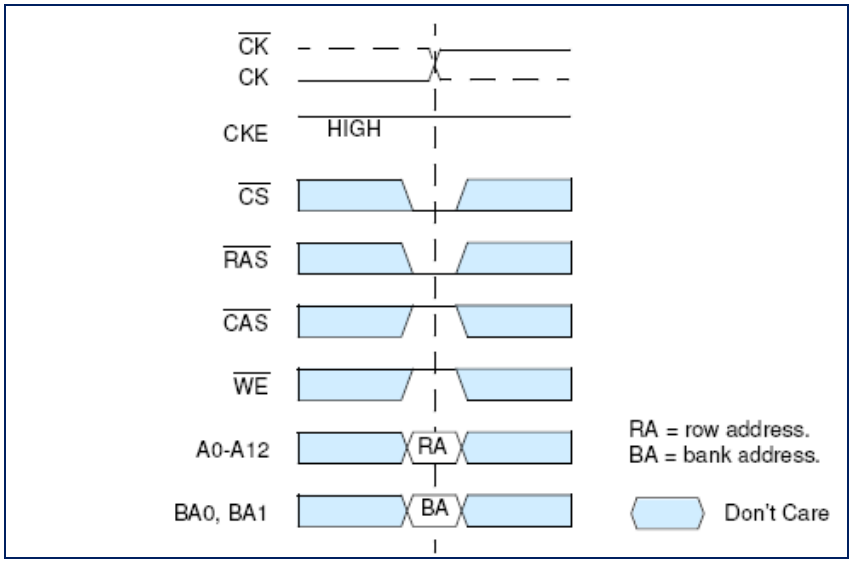
The procedure for exiting self refresh requires a sequence of commands. CK (and CK) must be stable prior to CKE returning high. Once CKE is high, the SDRAM must have NOP commands issued for tXSNR because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOPs for 200 clock cycles before applying any other command.

Operations

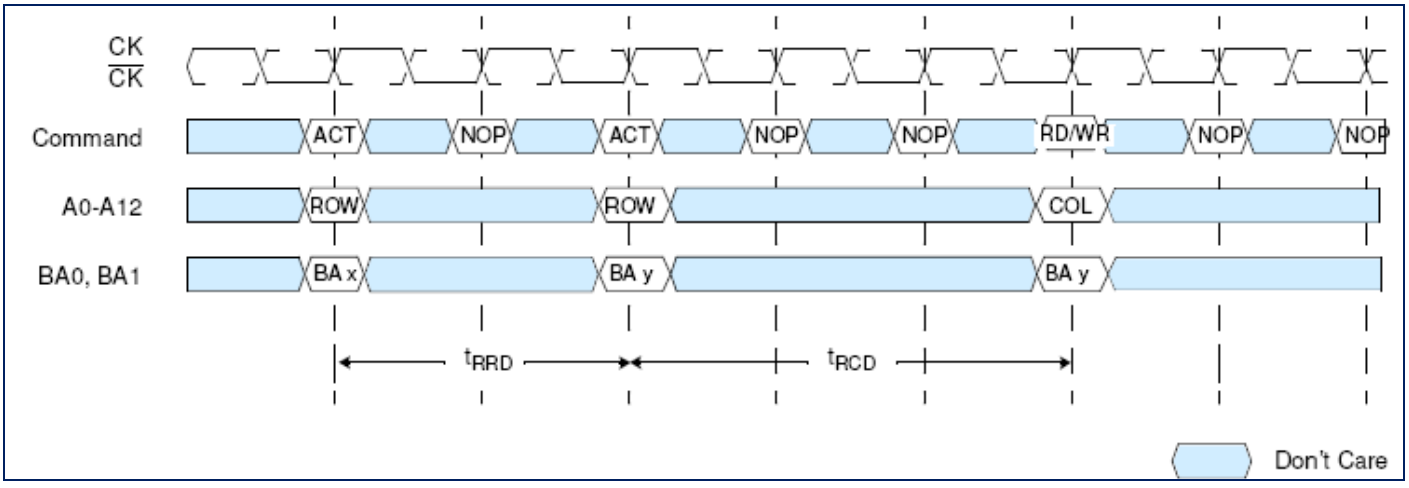
Bank/Row Activation

Before any Read or Write commands can be issued to a bank within the DDR SDRAM, a row in that bank must be "opened" (activated). This is accomplished via the Active command and addresses A0-A12, BA0 and BA1 (see Activating a Specific Row in a Specific Bank), which decode and select both the bank and the row to be activated. After opening a row (issuing an Active command), a Read or Write command may be issued to that row, subject to the t_{RCD} specification. A subsequent Active command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive Active commands to the same bank is defined by t_{RC}. A subsequent Active command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive Active commands to different banks is defined by t_{RRD}.

Activating a Specific Row in a Specific Bank



t_{RCD} and t_{RRD} Definition



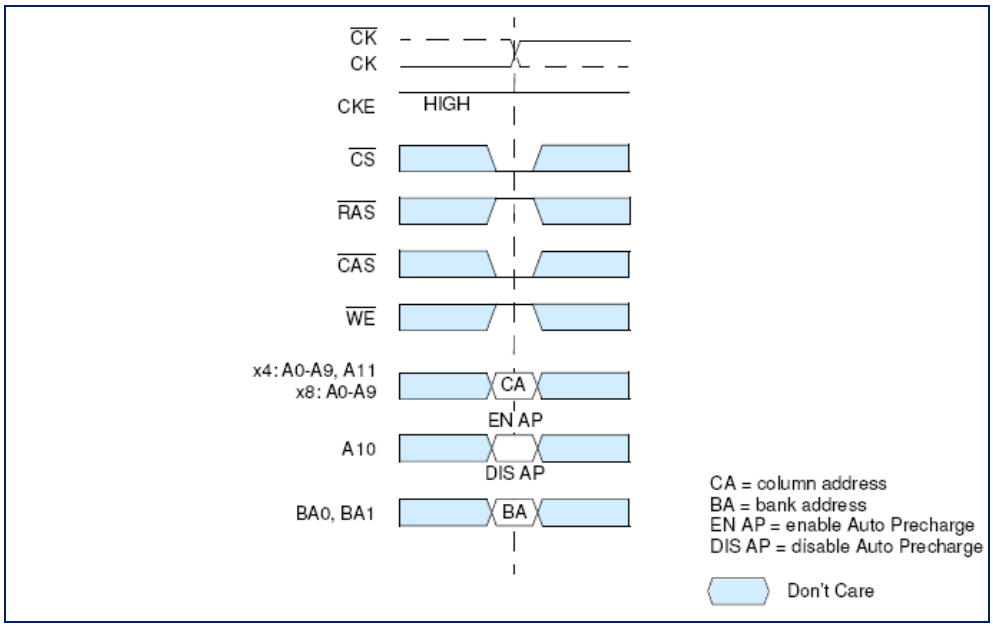
Reads

Subsequent to programming the mode register with CAS latency, burst type, and burst length, Read bursts are initiated with a Read command.

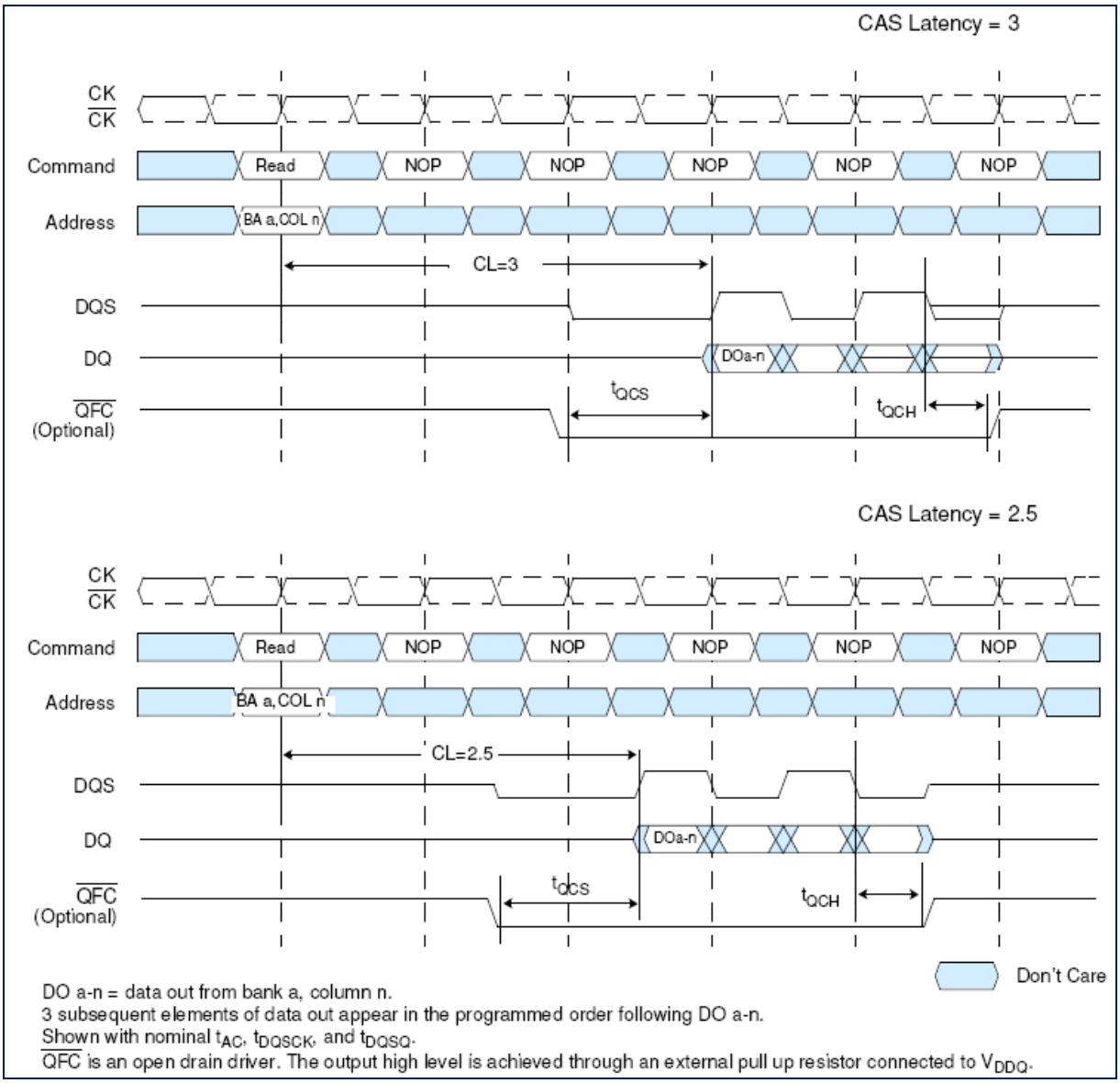
The starting column and bank addresses are provided with the Read command and Auto Precharge is either enabled or disabled for that burst access. If Auto Precharge is enabled, the row that is accessed starts precharge at the completion of the burst, provided t_{RAS} has been satisfied. For the generic Read commands used in the following illustrations, Auto Precharge is disabled.

During Read bursts, the valid data-out element from the starting column address is available following the CAS latency after the Read command. Each subsequent data-out element is valid nominally at the next positive or negative clock edge (i.e. at the next crossing of CK and CK). The following timing figure entitled “Read Burst: CAS Latencies (Burst Length=4)” illustrates the general timing for each supported CAS latency setting. DQS is driven by the DDR SDRAM along with output data. The initial low state on DQS is known as the read preamble; the low state coincident with the last data-out element is known as the read postamble. Upon completion of a burst, assuming no other commands have been initiated, the DQs and DQS goes High-Z. Data from any Read burst may be concatenated with or truncated with data from a subsequent Read command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new Read command should be issued x cycles after the first Read command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). This is shown in timing figure entitled “Consecutive Read Bursts: CAS Latencies (Burst Length =4 or 8)”. A Read command can be initiated on any positive clock cycle following a previous Read command. Nonconsecutive Read data is shown in timing figure entitled “Non-Consecutive Read Bursts: CAS Latencies (Burst Length = 4)”. Full-speed Random Read Accesses: CAS Latencies (Burst Length = 2, 4 or 8) within a page (or pages) can be performed.

Read Command

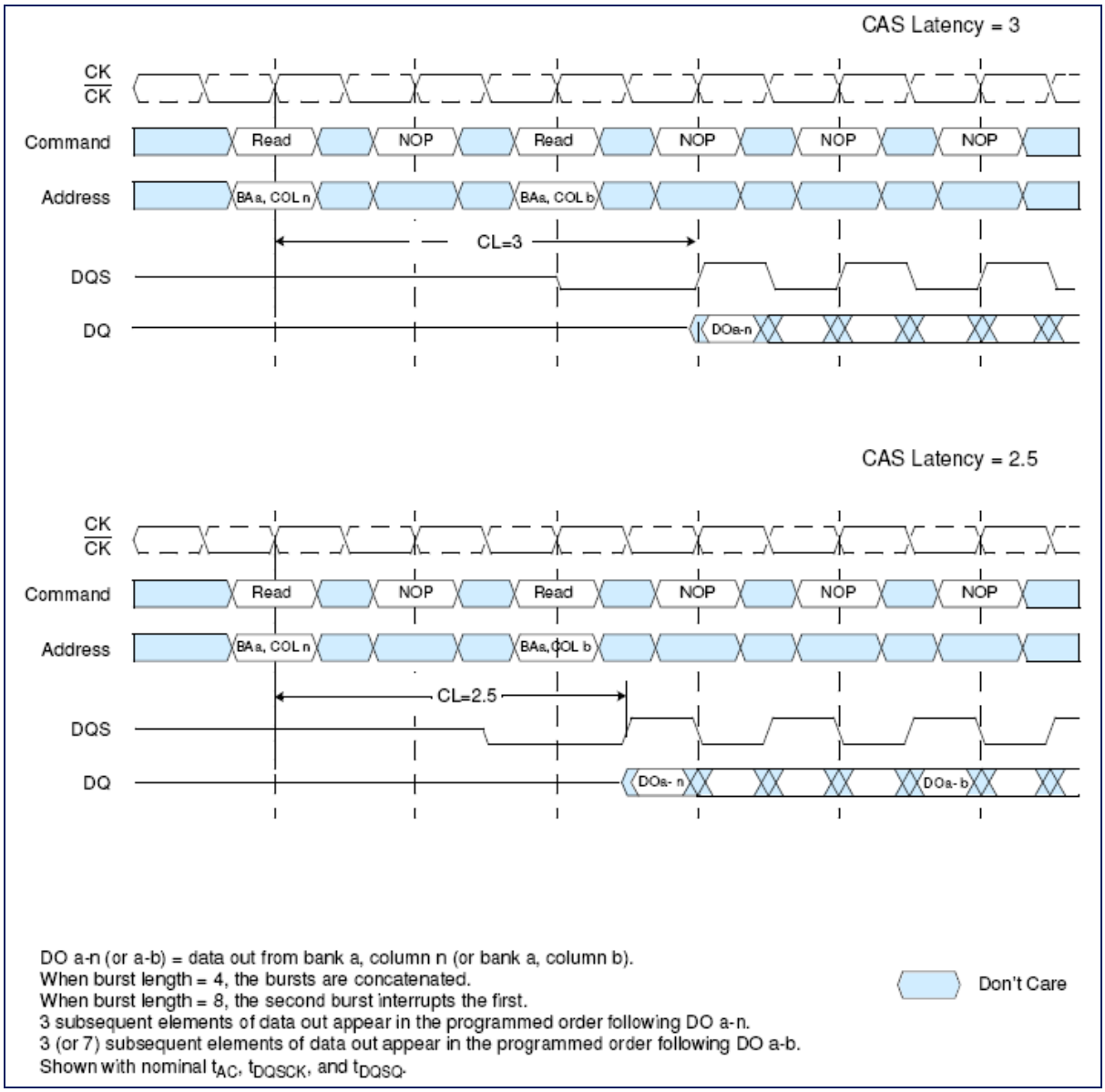


Read Burst: CAS Latencies (Burst Length = 4)

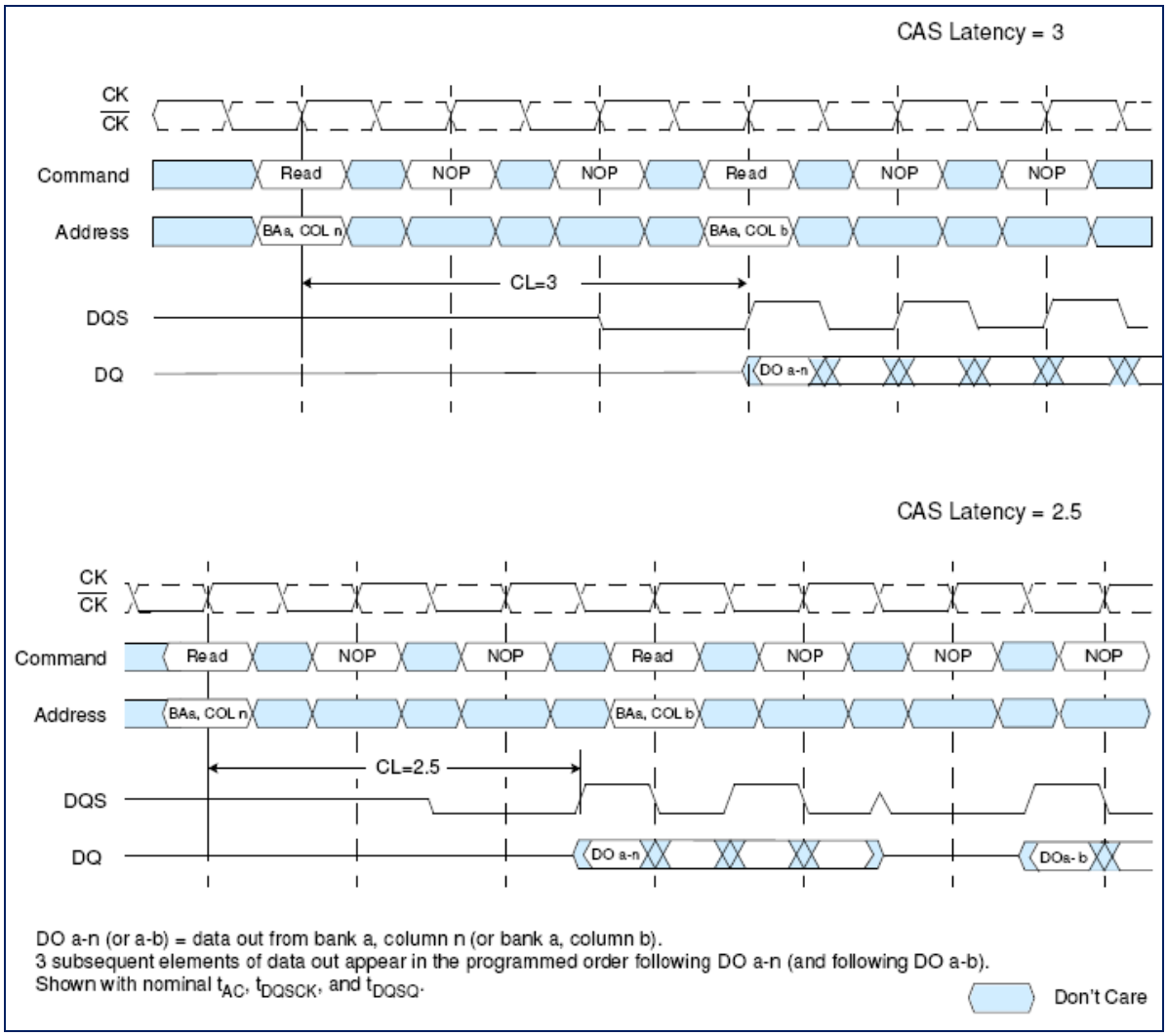


DO a-n = data out from bank a, column n.
3 subsequent elements of data out appear in the programmed order following DO a-n.
Shown with nominal t_{AC}, t_{DQSCK}, and t_{DQSQ}.
$\overline{QFC}$ is an open drain driver. The output high level is achieved through an external pull up resistor connected to V_{DDQ}.

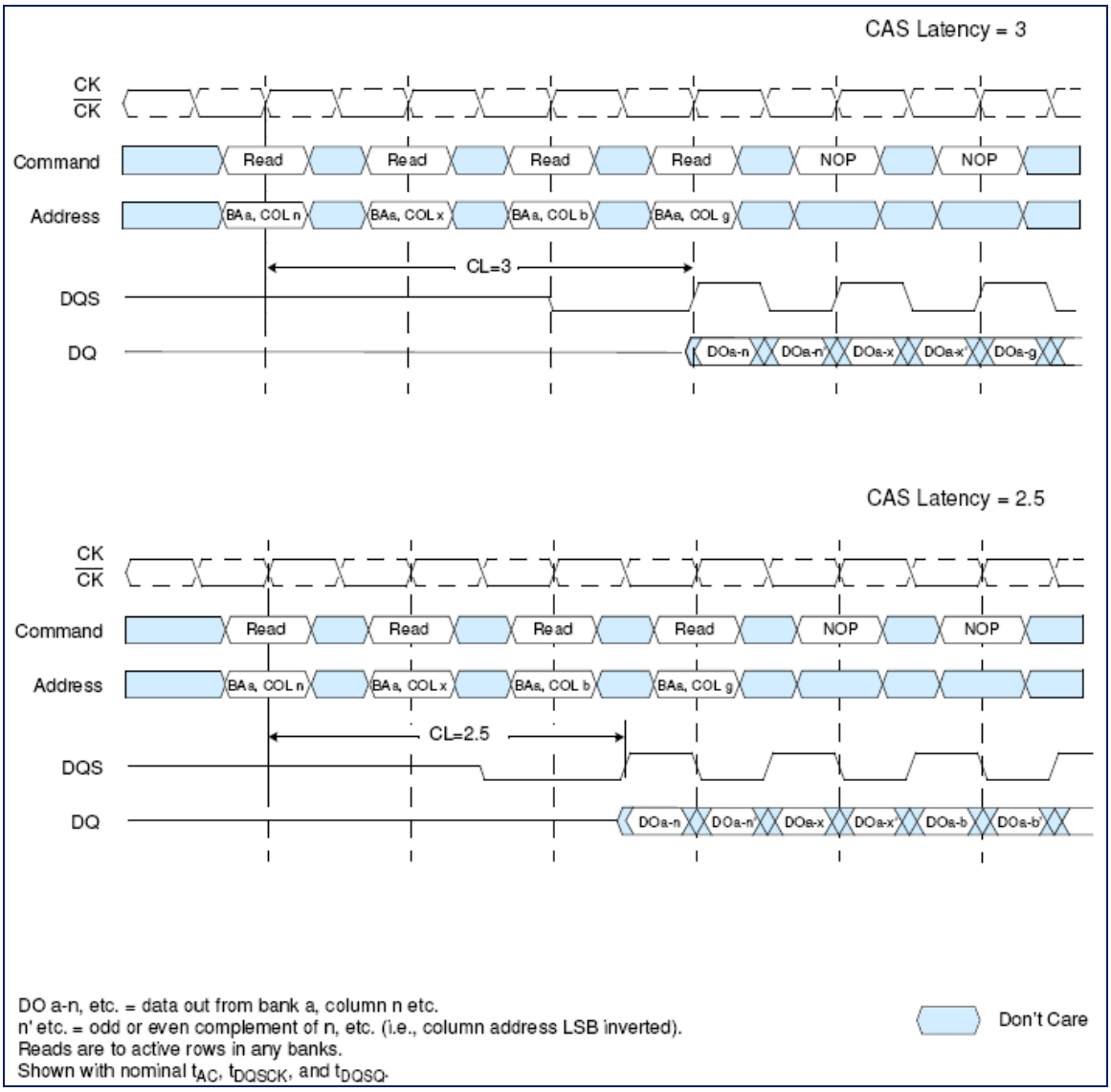
Consecutive Read Bursts: CAS Latencies (Burst Length = 4 or 8)



Non-Consecutive Read Bursts: CAS Latencies (Burst Length = 4)



Random Read Accesses: CAS Latencies (Burst Length = 2, 4 or 8)



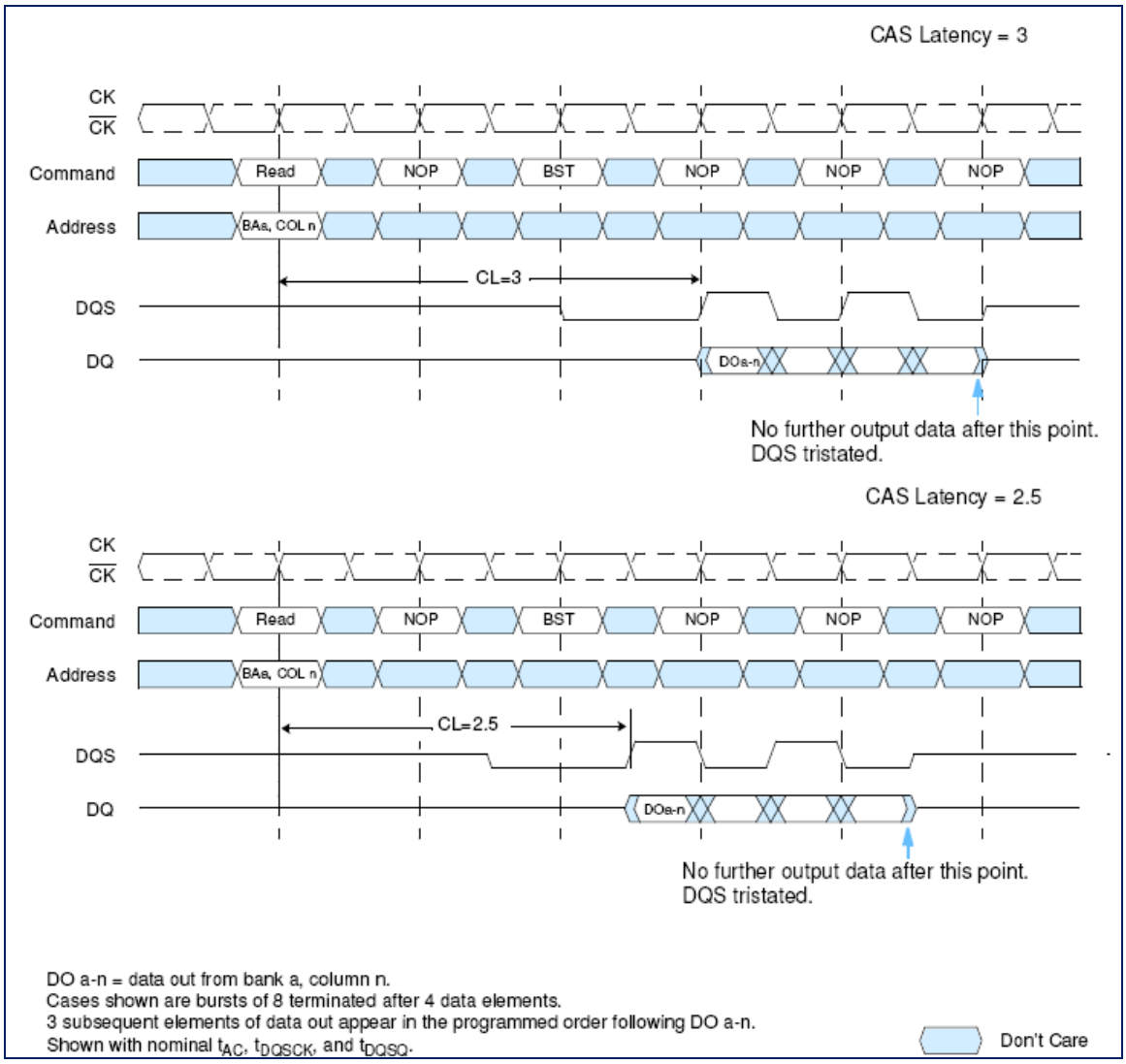
Data from any Read burst may be truncated with a Burst Terminate command, as shown in timing figure entitled *Terminating a Read Burst: CAS Latencies (Burst Length = 8)* on page 29. The Burst Terminate latency is equal to the read (CAS) latency, i.e. the Burst Terminate command should be issued x cycles after the Read command, where x equals the number of desired data element pairs.

Data from any Read burst must be completed or truncated before a subsequent Write command can be issued. If truncation is necessary, the Burst Terminate command must be used, as shown in timing figure entitled *Read to Write: CAS Latencies (Burst Length = 4 or 8)* on page 30. The example is shown for t_{DQSS}(min). The t_{DQSS}(max) case, not shown here, has a longer bus idle time. t_{DQSS}(min) and t_{DQSS}(max) are defined in the section on Writes.

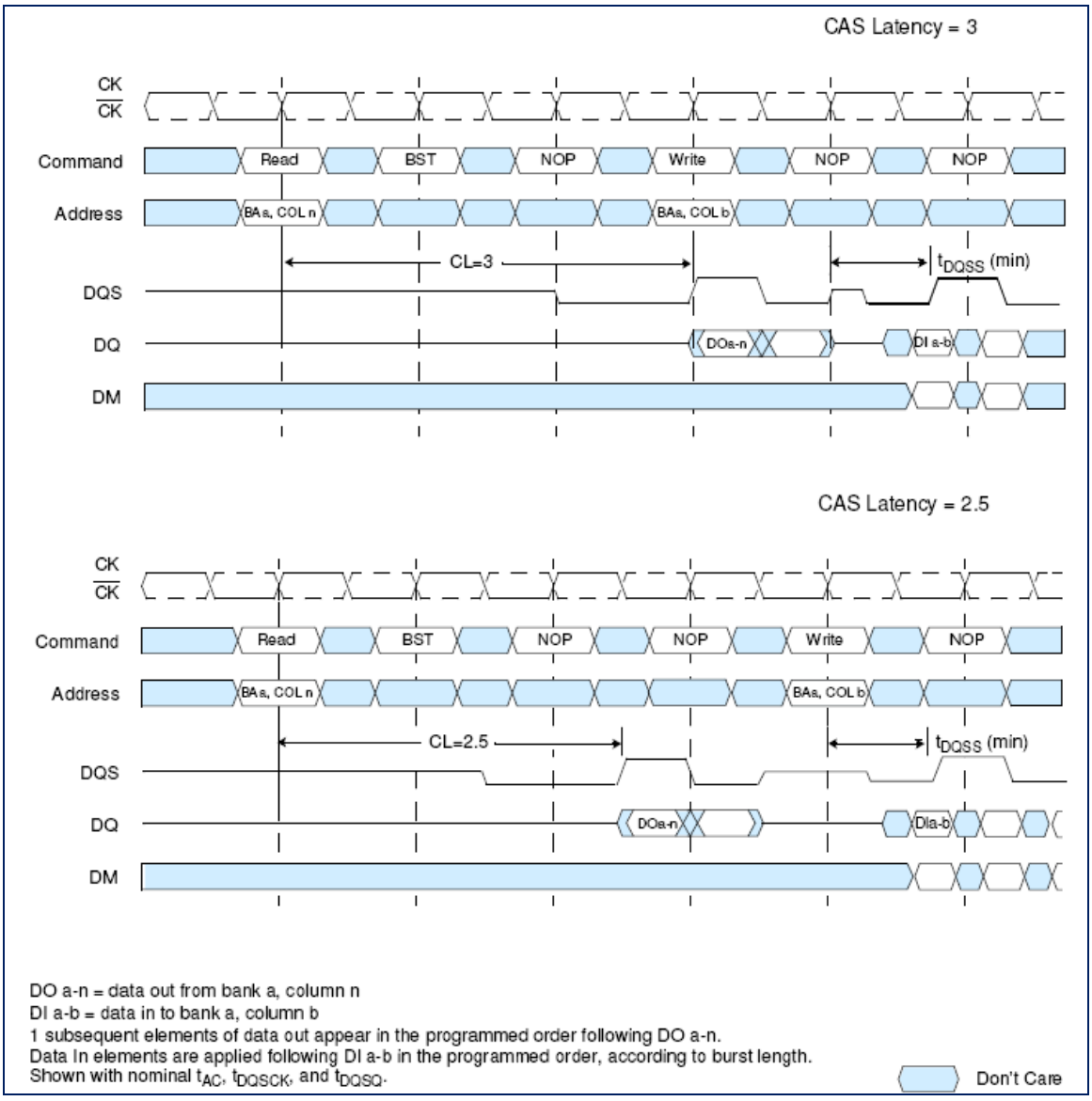
A Read burst may be followed by, or truncated with, a Precharge command to the same bank (provided that Auto Precharge was not activated). The Precharge command should be issued x cycles after the Read command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). This is shown in timing figure on page 24 for Read latencies of 3. Following the Precharge command, a subsequent command to the same bank cannot be issued until t_{RP} is met. Note that part of the row precharge time is hidden during the access of the last data elements.

In the case of a Read being executed to completion, a Precharge command issued at the optimum time (as described above) provides the same operation that would result from the same Read burst with Auto Precharge enabled. The disadvantage of the Precharge command is that it requires that the command and address busses be available at the appropriate time to issue the command. The advantage of the Precharge command is that it can be used to truncate bursts.

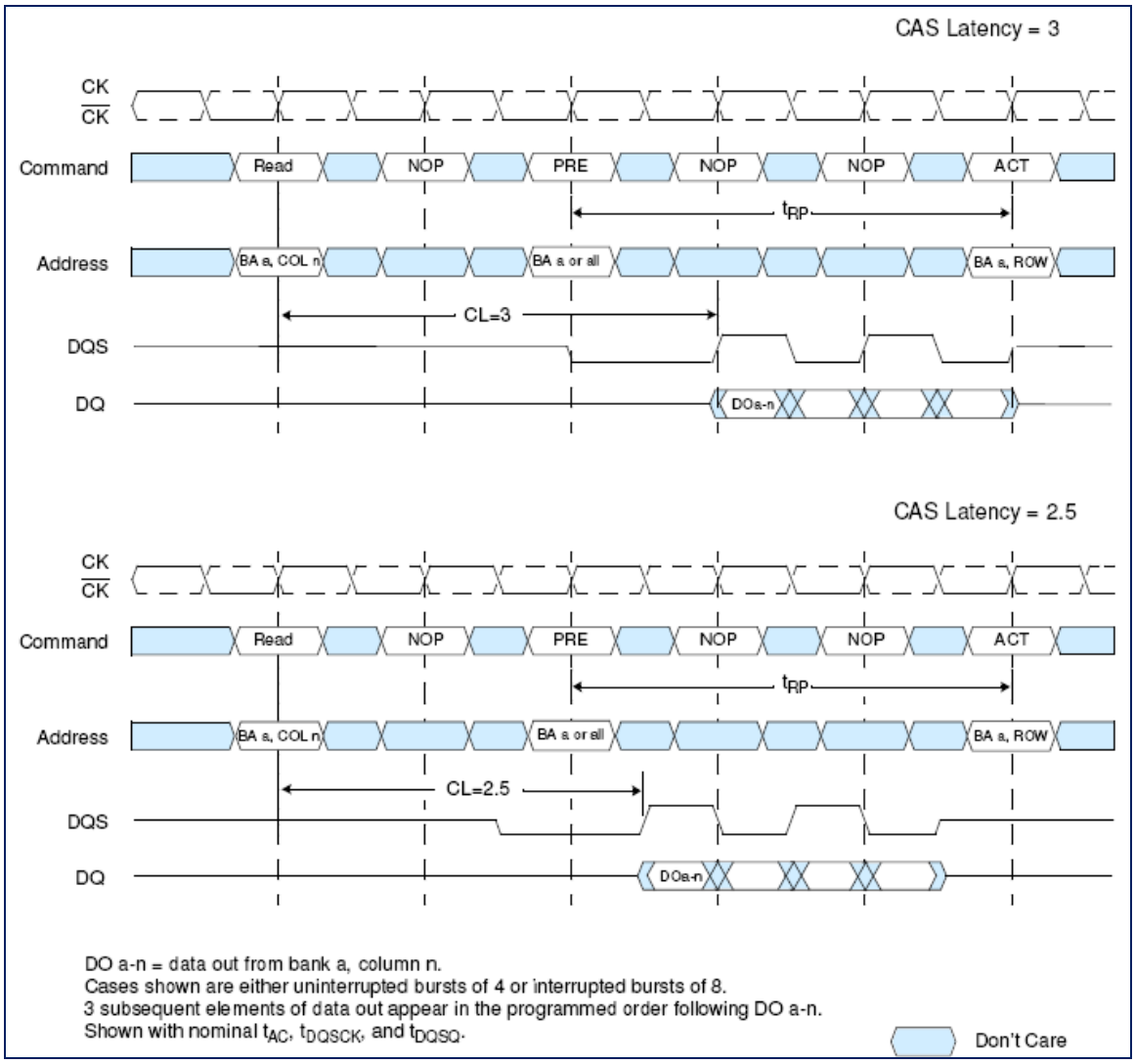
Terminating a Read Burst: CAS Latencies (Burst Length = 8)



Read to Write: CAS Latencies (Burst Length = 4 or 8)



Read to Precharge: CAS Latencies (Burst Length = 4 or 8)



Writes

Write bursts are initiated with a Write command, as shown in timing figure *Write Command* on this page.

The starting column and bank addresses are provided with the Write command, and Auto Precharge is either enabled or disabled for that access. If Auto Precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic Write commands used in the following illustrations, Auto Precharge is disabled.

During Write bursts, the first valid data-in element is registered on the first rising edge of DQS following the write command, and subsequent data elements are registered on successive edges of DQS. The Low state on DQS between the Write command and the first rising edge is known as the write preamble; the Low state on DQS following the last data-in element is known as the write postamble. The time between the Write command and the first corresponding rising edge of DQS (t_{DQSS}) is specified with a relatively wide range (from 75% to 125% of one clock cycle), so most of the Write diagrams that follow are drawn for the two extreme cases (i.e. t_{DQSS}(min) and t_{DQSS}(max)). Timing figure *Write Burst (Burst Length = 4)* on page 34 shows the two extremes of t_{DQSS} for a burst of four. Upon completion of a burst, assuming no other commands have been initiated, the DQs and DQS enters High-Z and any additional input data is ignored.

Data for any Write burst may be concatenated with or truncated with a subsequent Write command. In either case, a continuous flow of input data can be maintained. The new Write command can be issued on any positive edge of clock following the previous Write command. The first data element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new Write command should be issued x cycles after the first Write command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). Timing figure *Write to Write (Burst Length = 4)* on page 35 shows concatenated bursts of 4. An example of nonconsecutive Writes is shown in timing figure *Write to Write: Max DQSS, Non-Consecutive (Burst Length = 4)* on page 36. Fullspeed random write accesses within a page or pages can be performed as shown in timing figure *Random Write Cycles (Burst Length = 2, 4 or 8)* on page 37. Data for any Write burst may be followed by a subsequent Read command. To follow a Write without truncating the write burst, t_{WTR} (Write to Read) should be met as shown in timing figure *Write to Read: Non-Interrupting (CAS Latency = 3; Burst Length = 4)*.

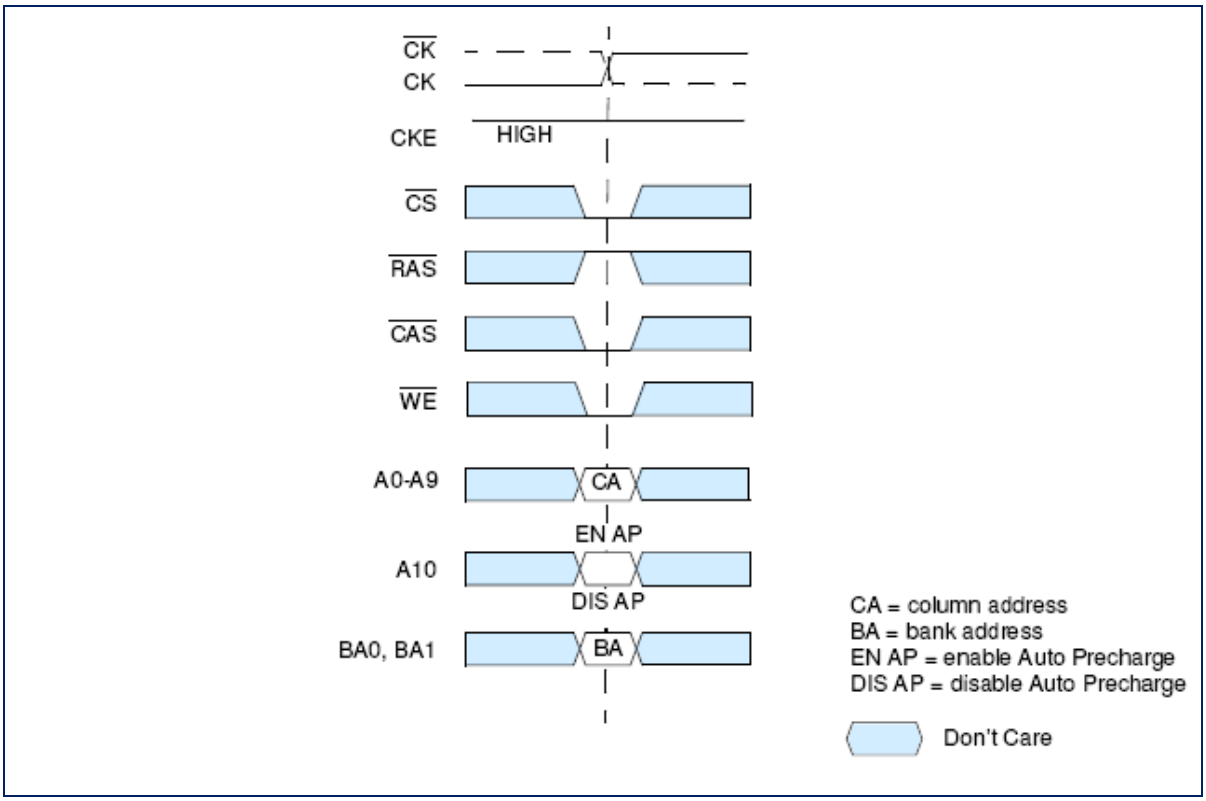
Data for any Write burst may be truncated by a subsequent (interrupting) Read command. This is illustrated in timing figures “Write to Read: Interrupting (CAS Latency =2; Burst Length = 8)”, “Write to Read: Minimum D_{QSS}, Odd Number of Data (3 bit Write), Interrupting (CAS Latency = 2; Burst Length = 8)”, and “Write to Read: Nominal D_{QSS}, Interrupting (CAS Latency = 2; Burst Length = 8)”. Note that only the data-in pairs that are registered prior to the t_{WTR} period are written to the internal array, and any subsequent data-in must be masked with DM, as shown in the diagrams noted previously.

Data for any Write burst may be followed by a subsequent Precharge command. To follow a Write without truncating the write burst, t_{WR} should be met as shown in timing figure *Write to Precharge: Non-Interrupting (Burst Length = 4).*

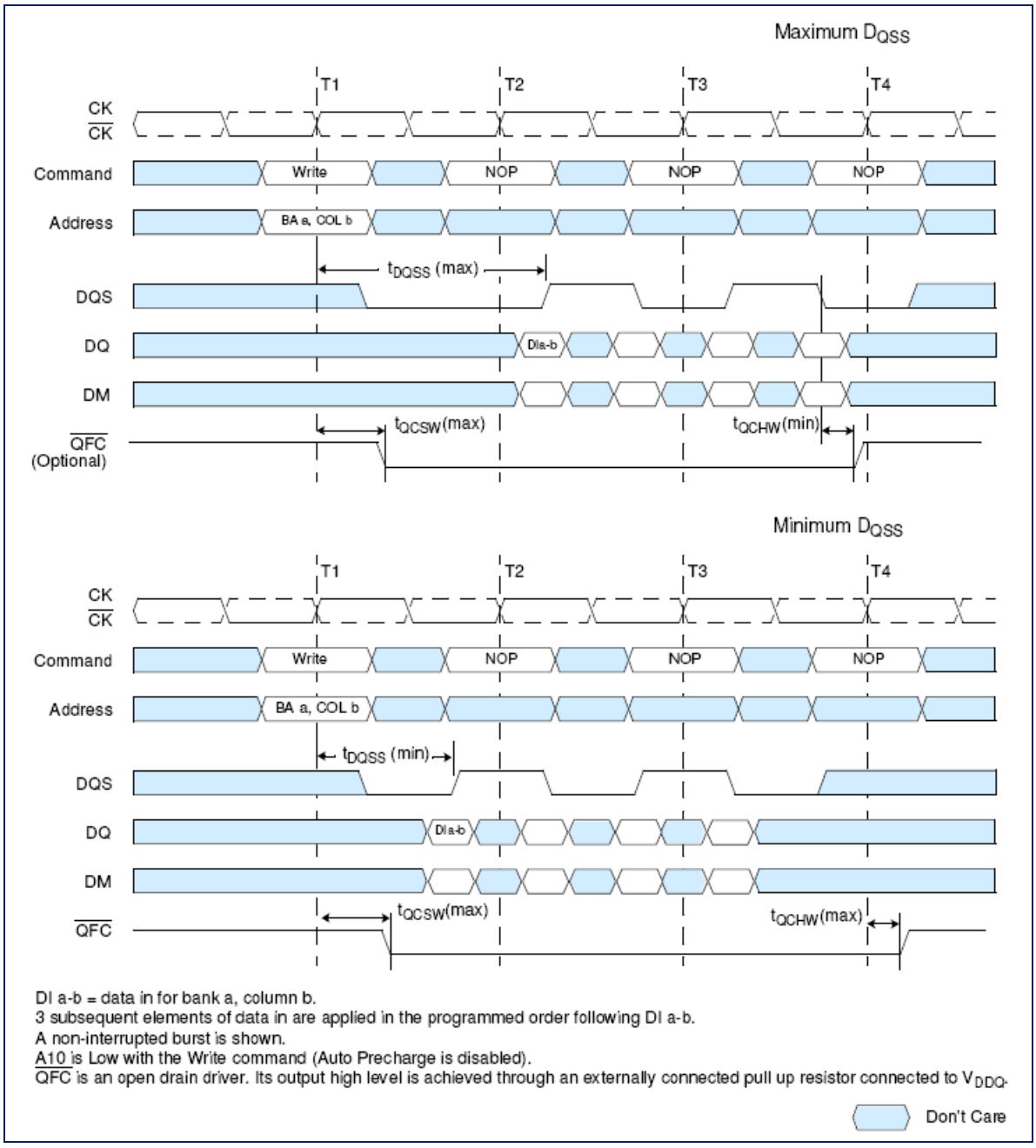
Data for any Write burst may be truncated by a subsequent Precharge command, as shown in timing figures *Write to Precharge: Interrupting (Burst Length = 4 or 8)* on page 43 to *Write to Precharge: Nominal DQSS (2 bit Write), Interrupting (Burst Length = 4 or 8)*. Note that only the data-in pairs that are registered prior to the t_{WR} period are written to the internal array, and any subsequent data in should be masked with DM. Following the Precharge command, a subsequent command to the same bank cannot be issued until t_{RP} is met.

In the case of a Write burst being executed to completion, a Precharge command issued at the optimum time (as described above) provides the same operation that would result from the same burst with Auto Precharge. The disadvantage of the Precharge command is that it requires that the command and address busses be available at the appropriate time to issue the command. The advantage of the Precharge command is that it can be used to truncate bursts.

Write Command



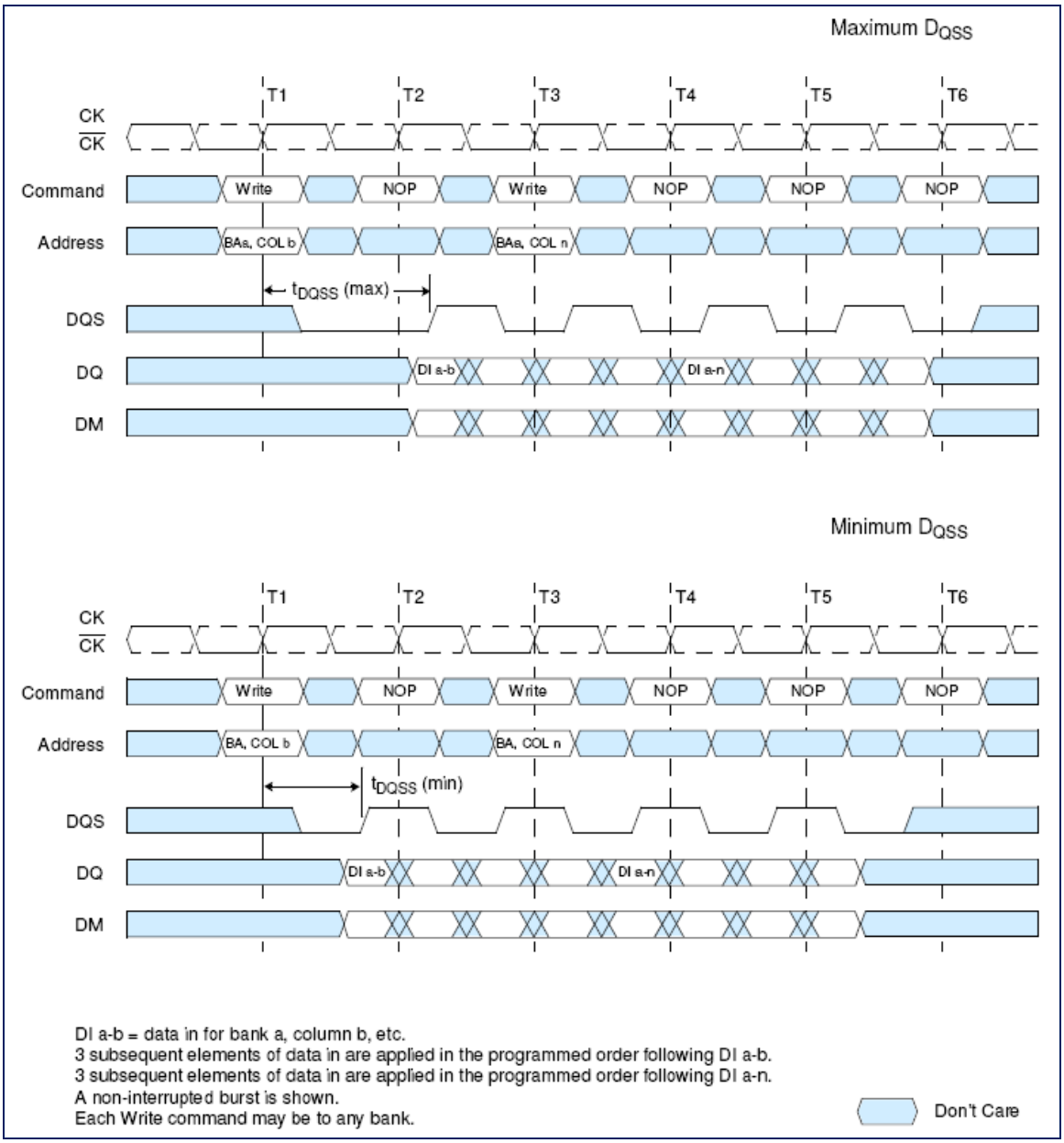
Write Burst (Burst Length = 4)



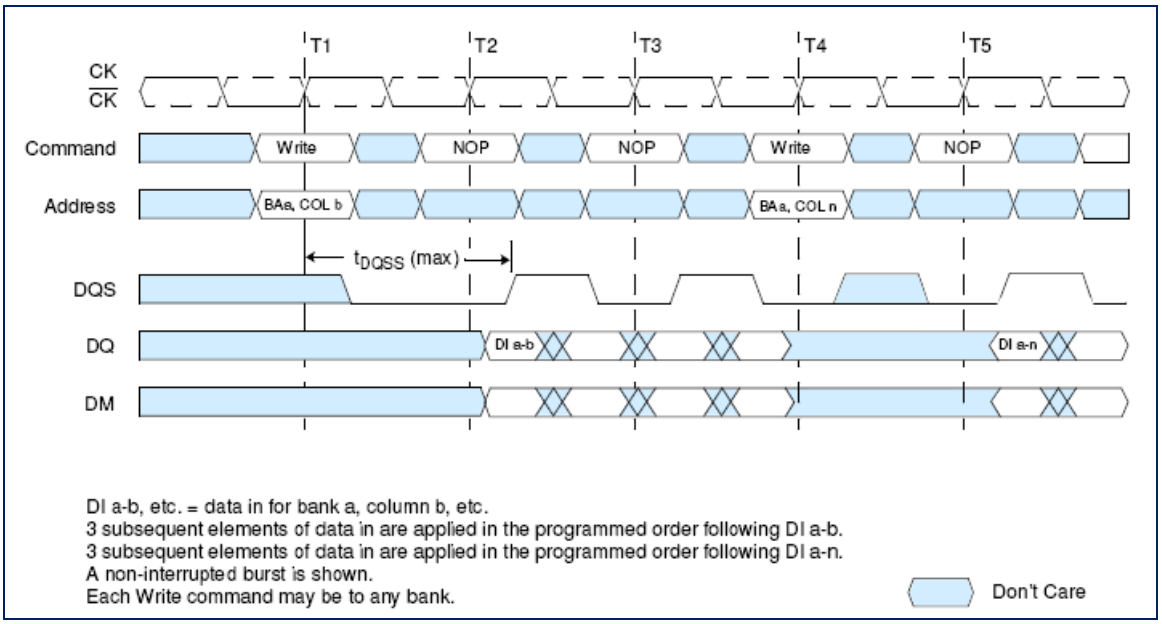
DI a-b = data in for bank a, column b.
3 subsequent elements of data in are applied in the programmed order following DI a-b.
A non-interrupted burst is shown.
$\overline{A10}$ is Low with the Write command (Auto Precharge is disabled).
$\overline{QFC}$ is an open drain driver. Its output high level is achieved through an externally connected pull up resistor connected to V_{DDQ}.

Don't Care

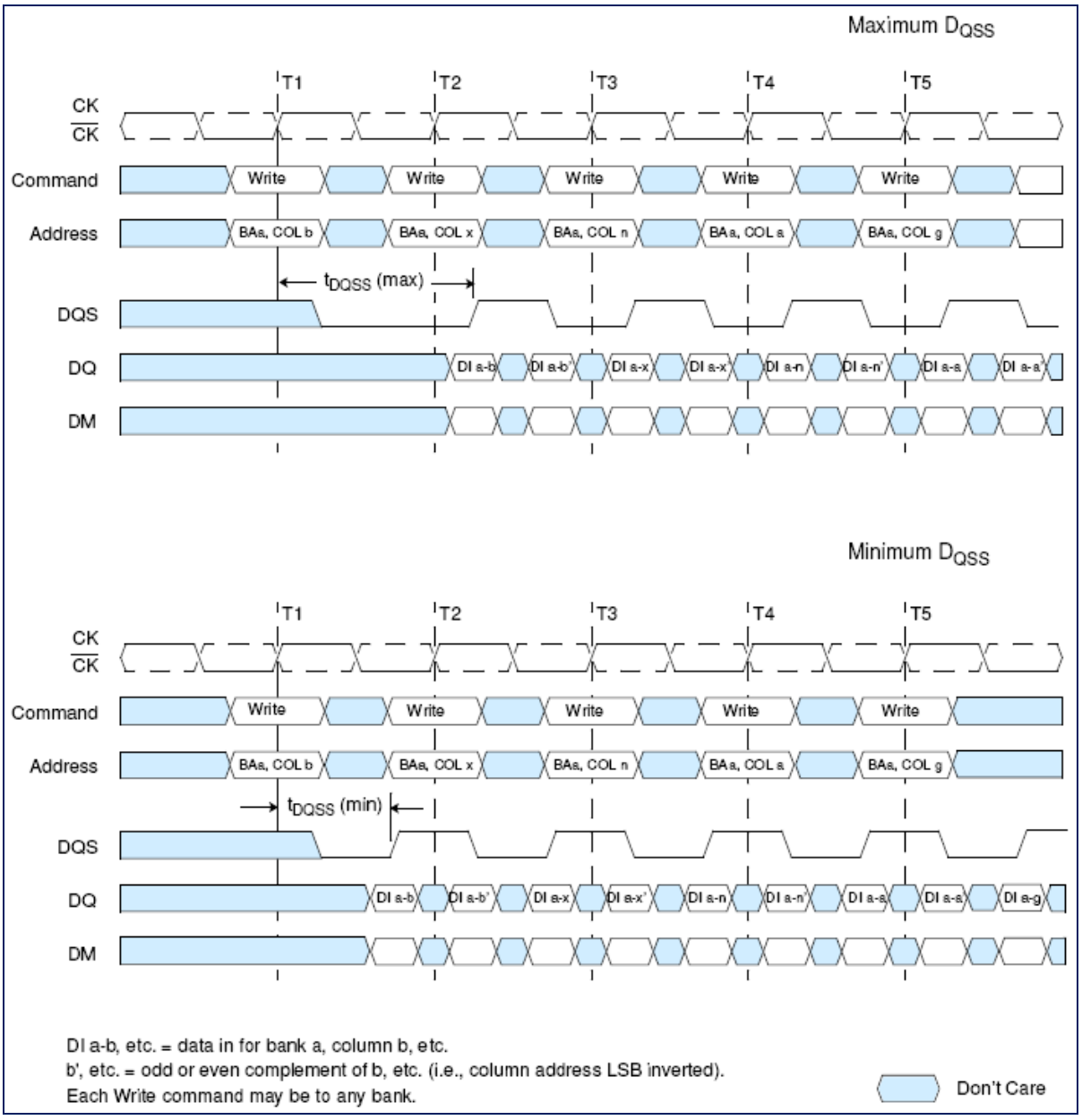
Write to Write (Burst Length = 4)



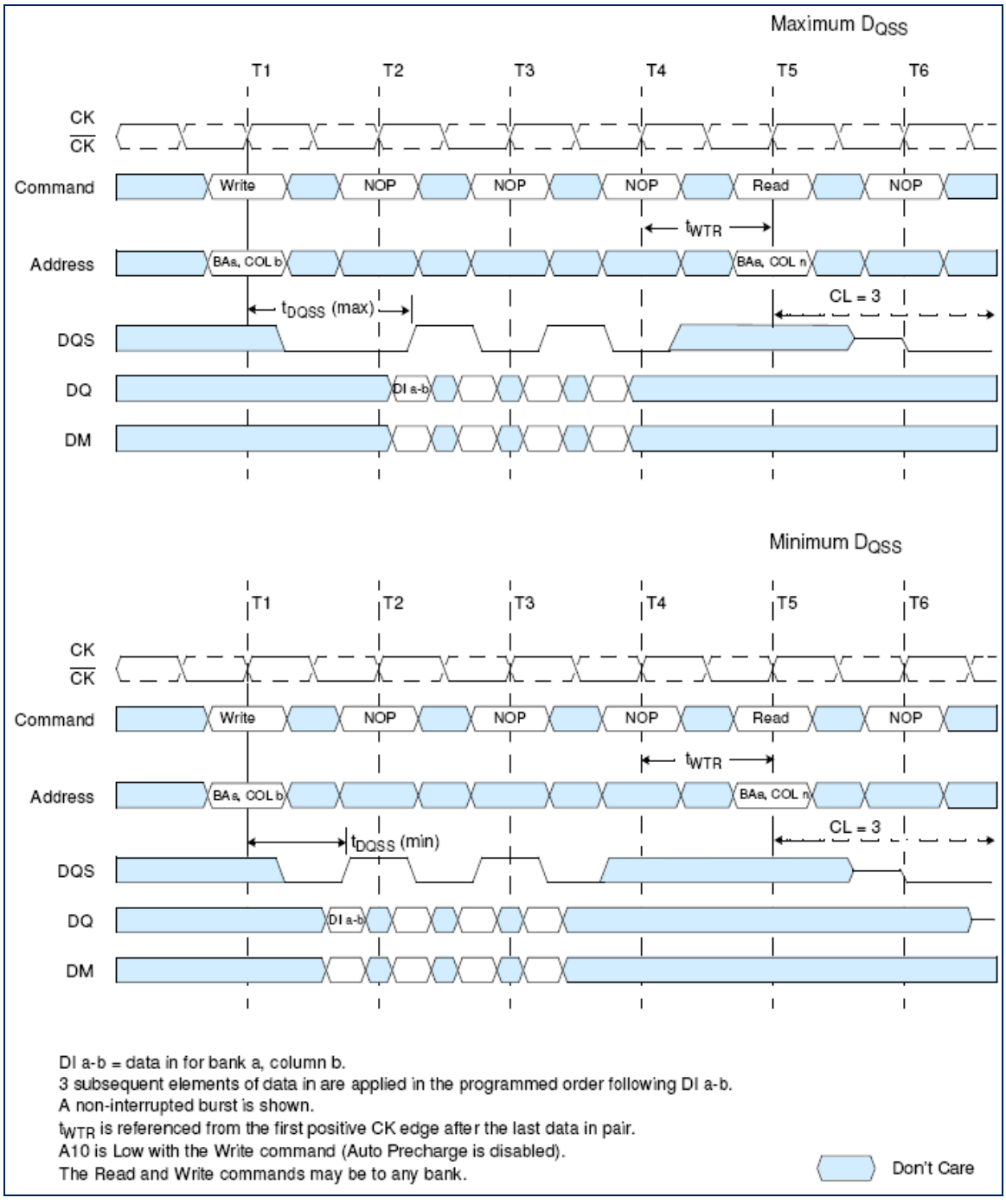
Write to Write: Max DQSS, Non-Consecutive (Burst Length = 4)



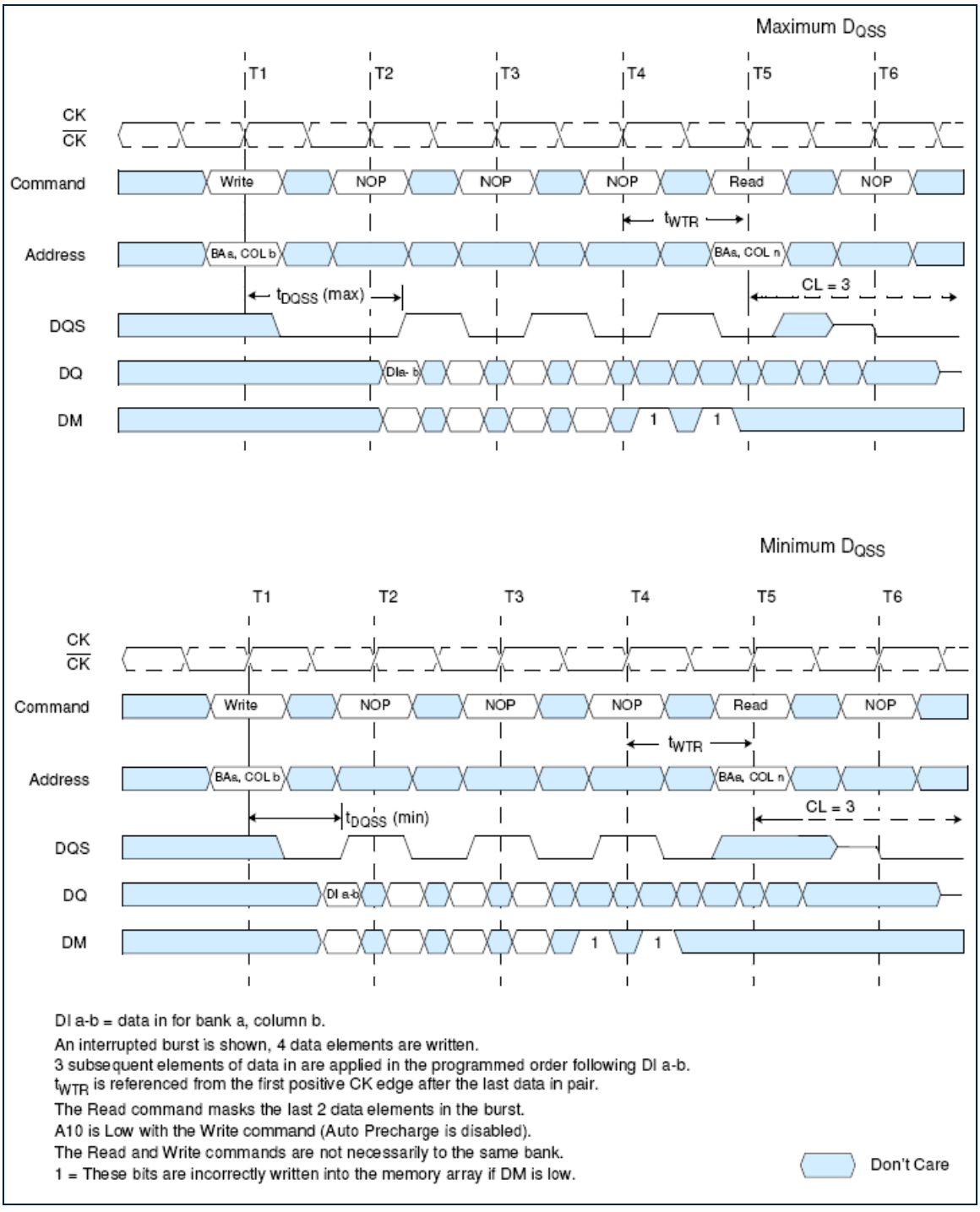
Random Write Cycles (Burst Length = 2, 4 or 8)



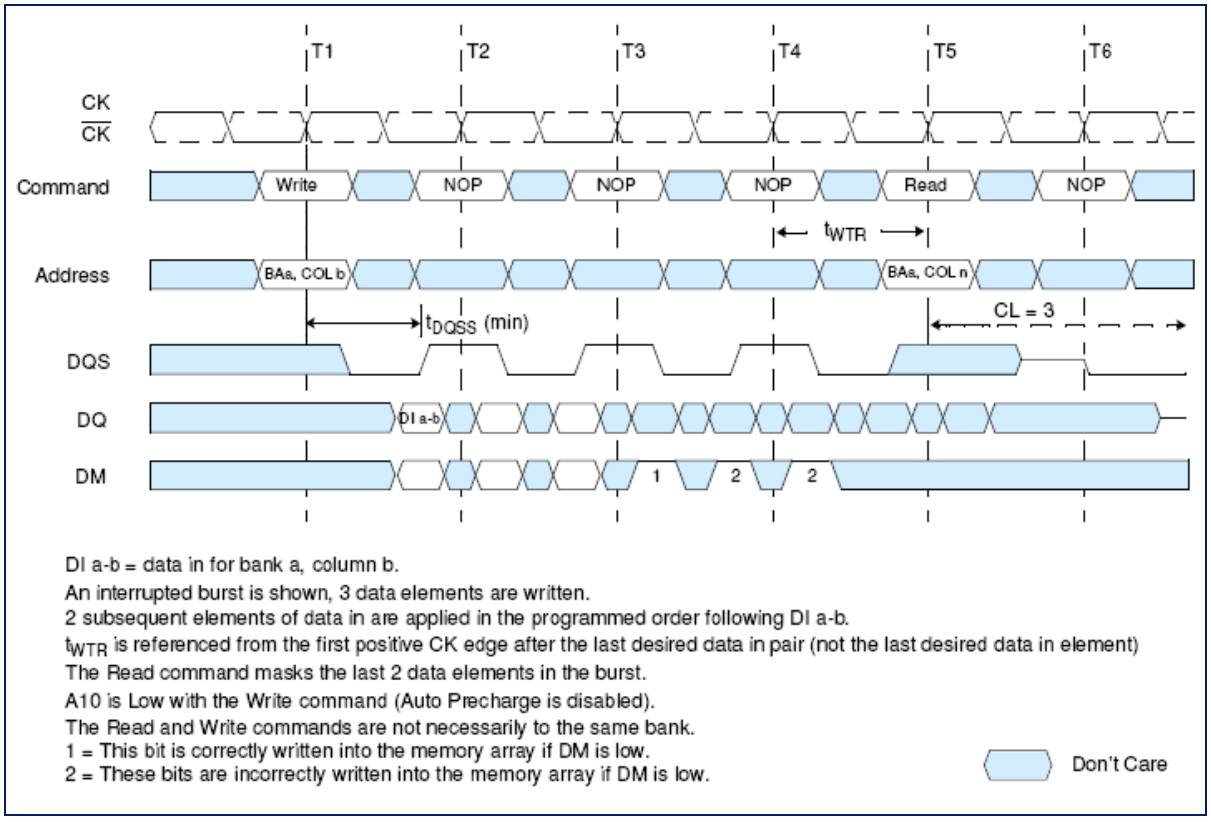
Write to Read: Non-Interrupting (CAS Latency = 3; Burst Length = 4)



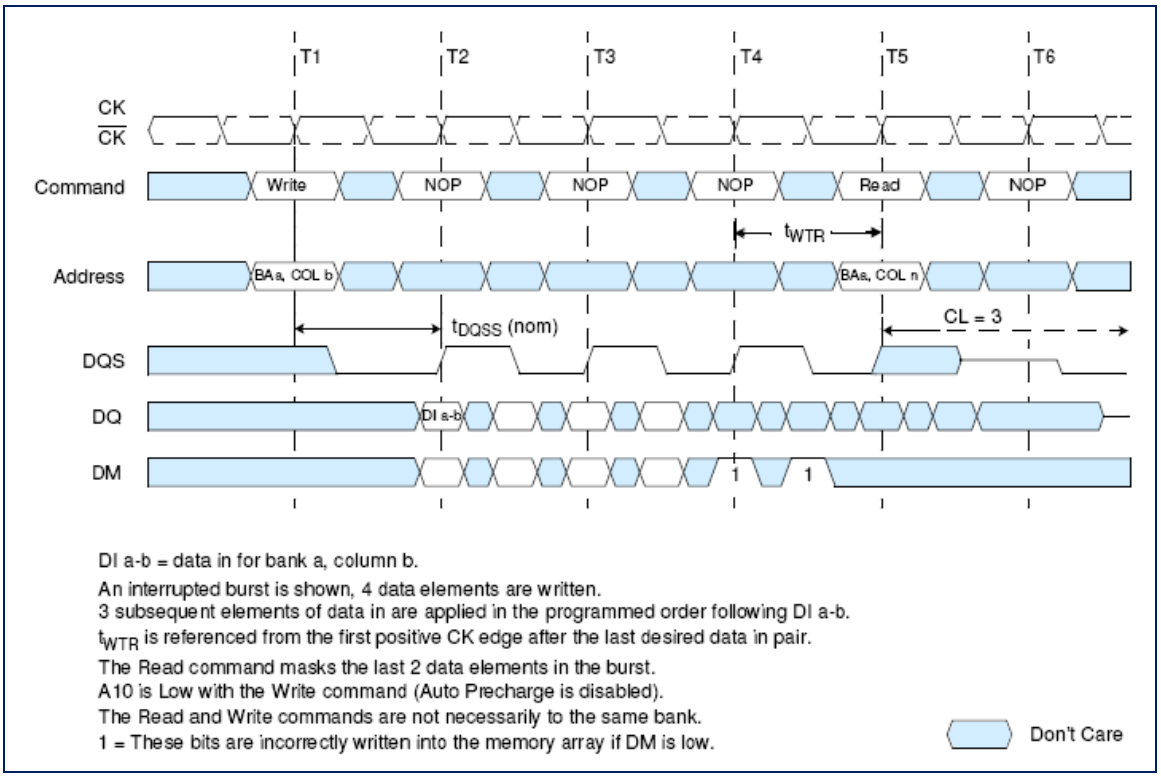
Write to Read: Interrupting (CAS Latency = 3; Burst Length = 8)



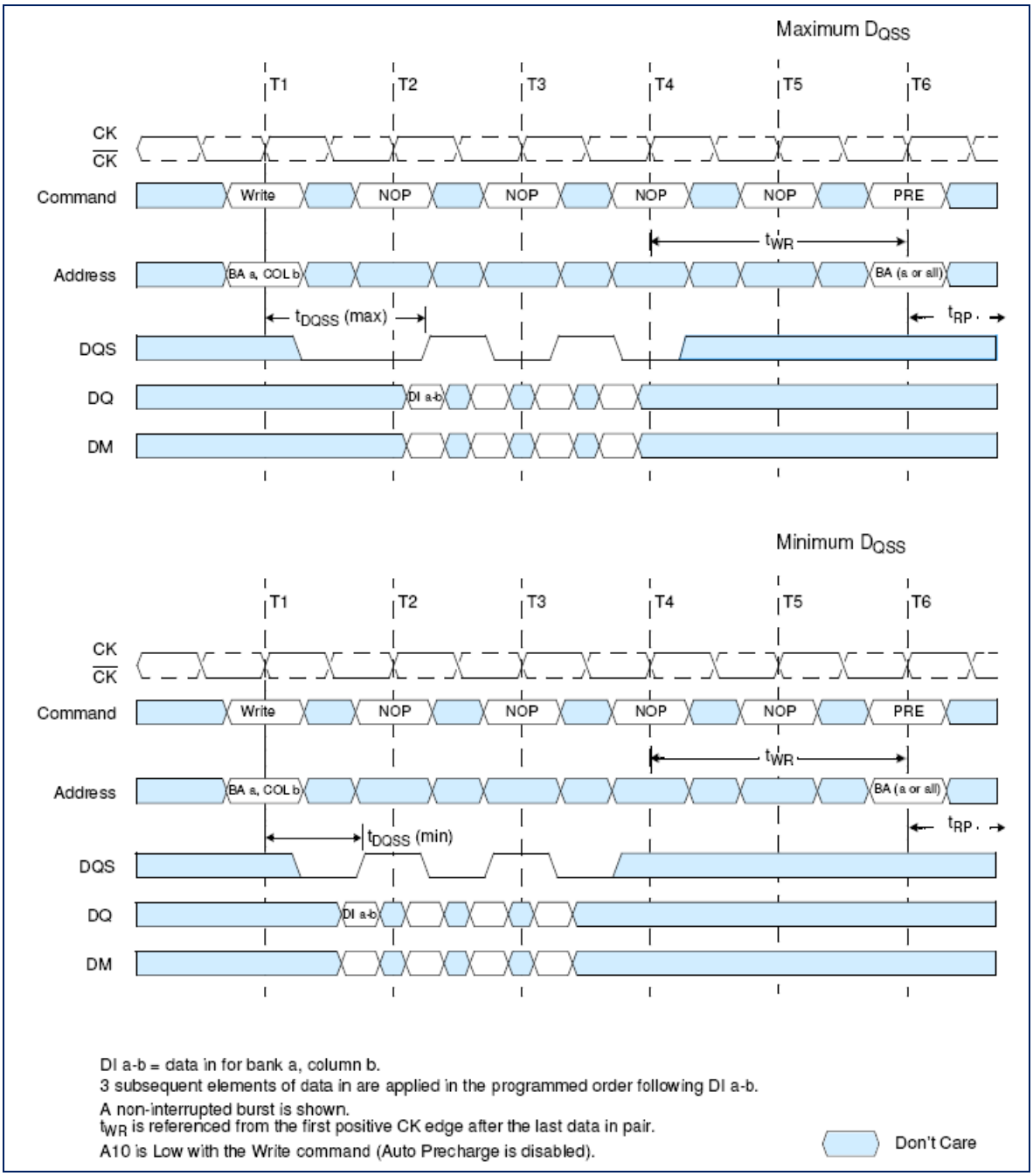
Write to Read: Minimum DQSS, Odd Number of Data (3 bit Write), Interrupting (CAS Latency = 3; Burst Length = 8)



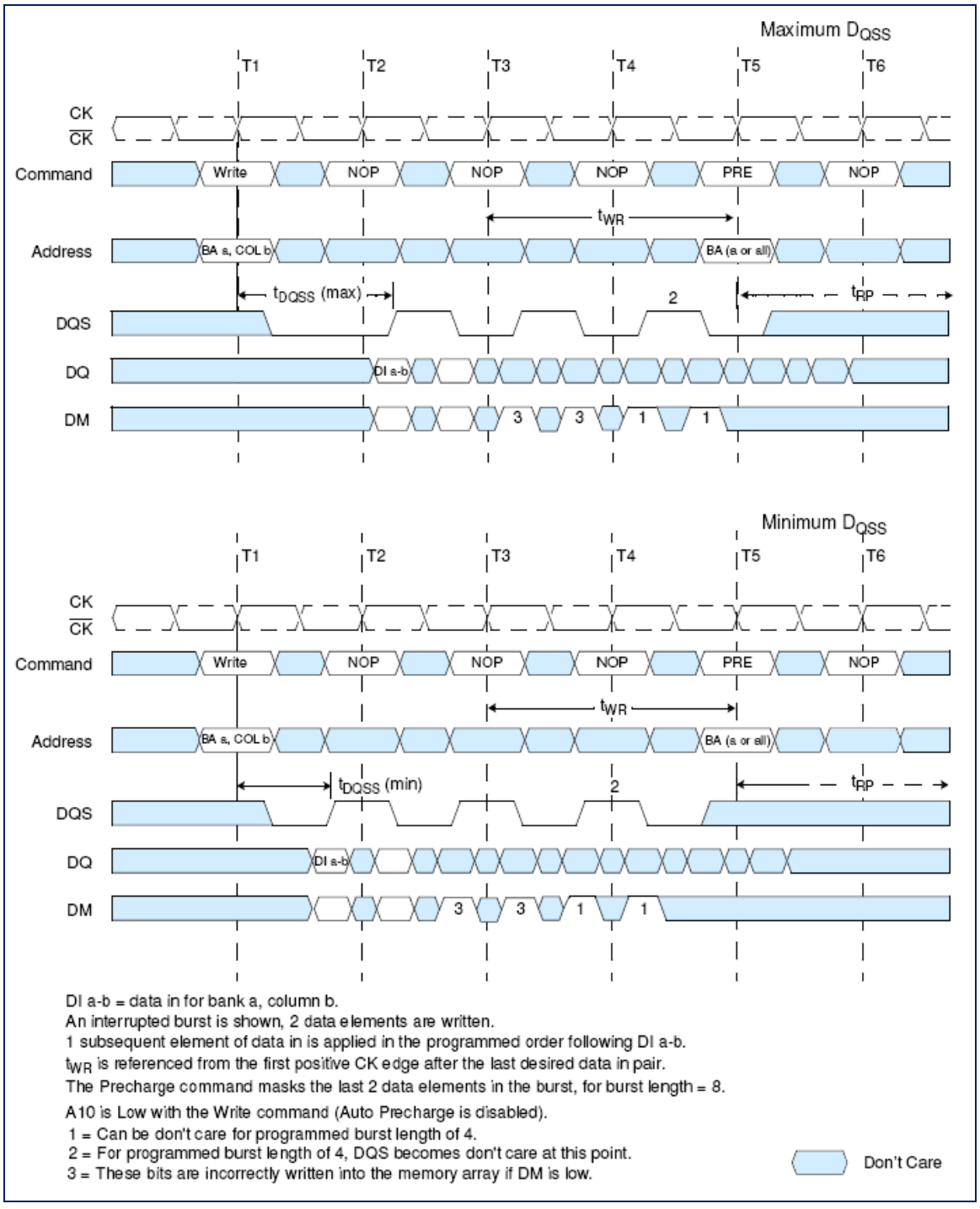
Write to Read: Nominal DQSS, Interrupting (CAS Latency = 3; Burst Length = 8)



Write to Precharge: Non-Interrupting (Burst Length = 4)



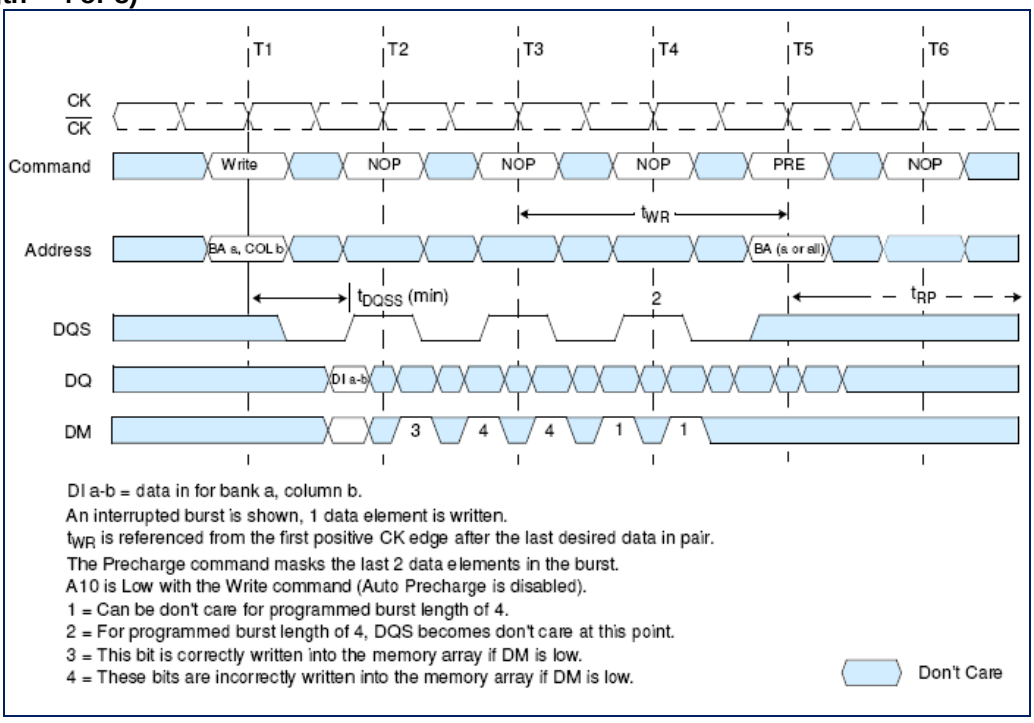
Write to Precharge: Interrupting (Burst Length = 4 or 8)



DI a-b = data in for bank a, column b.
An interrupted burst is shown, 2 data elements are written.
1 subsequent element of data in is applied in the programmed order following DI a-b.
t_{WR} is referenced from the first positive CK edge after the last desired data in pair.
The Precharge command masks the last 2 data elements in the burst, for burst length = 8.
A10 is Low with the Write command (Auto Precharge is disabled).
1 = Can be don't care for programmed burst length of 4.
2 = For programmed burst length of 4, DQS becomes don't care at this point.
3 = These bits are incorrectly written into the memory array if DM is low.

Don't Care

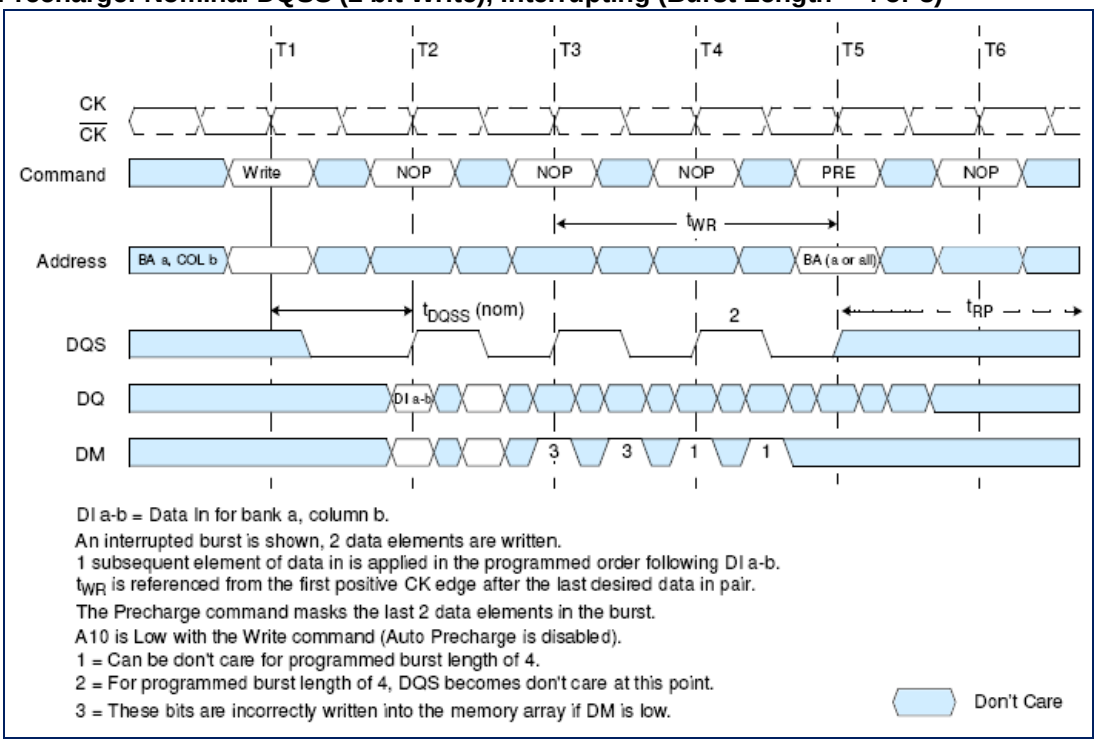
Write to Precharge: Minimum DQSS, Odd Number of Data (1 bit Write), Interrupting (Burst Length = 4 or 8)



DI a-b = data in for bank a, column b.
An interrupted burst is shown, 1 data element is written.
t_{WR} is referenced from the first positive CK edge after the last desired data in pair.
The Precharge command masks the last 2 data elements in the burst.
A10 is Low with the Write command (Auto Precharge is disabled).
1 = Can be don't care for programmed burst length of 4.
2 = For programmed burst length of 4, DQS becomes don't care at this point.
3 = This bit is correctly written into the memory array if DM is low.
4 = These bits are incorrectly written into the memory array if DM is low.

Don't Care

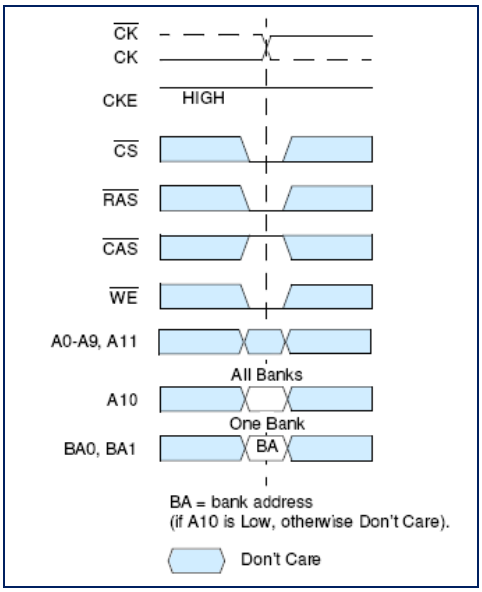
Write to Precharge: Nominal DQSS (2 bit Write), Interrupting (Burst Length = 4 or 8)



DI a-b = Data In for bank a, column b.
An interrupted burst is shown, 2 data elements are written.
1 subsequent element of data in is applied in the programmed order following DI a-b.
t_{WR} is referenced from the first positive CK edge after the last desired data in pair.
The Precharge command masks the last 2 data elements in the burst.
A10 is Low with the Write command (Auto Precharge is disabled).
1 = Can be don't care for programmed burst length of 4.
2 = For programmed burst length of 4, DQS becomes don't care at this point.
3 = These bits are incorrectly written into the memory array if DM is low.

Don't Care

Precharge Command



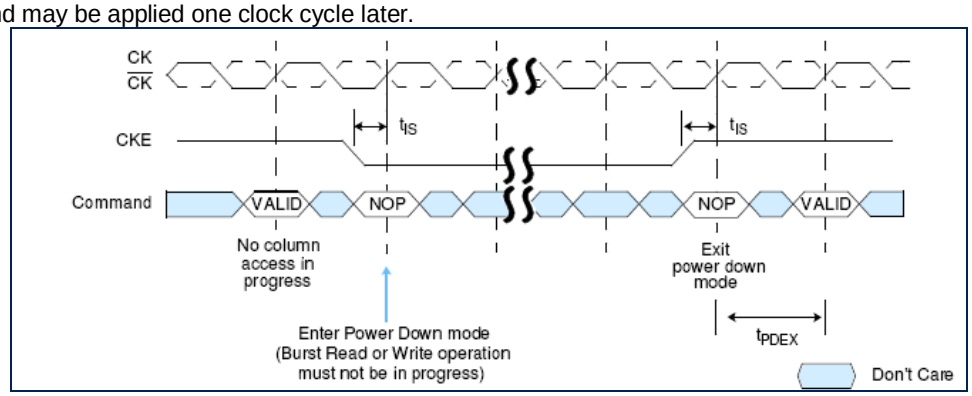
Precharge

The Precharge command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) is available for a subsequent row access some specified time (t_{RP}) after the Precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any Read or Write commands being issued to that bank.

Power Down

Power Down is entered when CKE is registered low (no accesses can be in progress). If Power Down occurs when all banks are idle, this mode is referred to as Precharge Power Down; if Power Down occurs when there is a row active in any bank, this mode is referred to as Active Power Down. Entering Power Down deactivates the input and output buffers, excluding CK, CK and CKE. The DLL is still running in Power Down mode, so for maximum power savings, the user has the option of disabling the DLL prior to entering Power Down. In that case, the DLL must be enabled after exiting Power Down, and 200 clock cycles must occur before a Read command can be issued. In Power Down mode, CKE Low and a stable clock signal must be maintained at the inputs of the DDR SDRAM, and all other input signals are "Don't Care". However, Power Down duration is limited by the refresh requirements of the device, so in most applications, the self refresh mode is preferred over the DLL-disabled Power Down mode.

The Power Down state is synchronously exited when CKE is registered high (along with a Nop or Deselect command). A valid, executable command may be applied one clock cycle later.



Truth Table 2: Clock Enable (CKE)

1. CKE n is the logic state of CKE at clock edge n: CKE n-1 was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR SDRAM immediately prior to clock edge n.
3. Command n is the command registered at clock edge n, and action n is a result of command n.
4. All states and sequences not shown are illegal or reserved.

Current State	CKE n-1	CKEn	Command n	Action n	Notes
	Previous Cycle	Current Cycle			
Self Refresh	L	L	X	Maintain Self-Refresh	
Self Refresh	L	H	Deselect or NOP	Exit Self-Refresh	
Power Down	L	L	X	Maintain Power Down	
Power Down	L	H	Deselect or NOP	Exit Power Down	
All Banks Idle	H	L	Deselect or NOP	Precharge Power Down Entry	
All Banks Idle	H	L	Auto Refresh	Self Refresh Entry	
Bank(s) Active	H	L	Deselect or NOP	Active Power Down Entry	
	H	H	See Truth Table 3		

1. Deselect or NOP commands should be issued on any clock edges occurring during the Self Refresh Exit (t_{XSNR}) period. A minimum of 200 clock cycles are needed before applying a read command to allow the DLL to lock to the input clock.

Truth Table 3: Current State Banks n – Command to Bank n (Same Bank)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command	Action	Notes
Any	H	X	X	X	Deselect	NOP. Continue previous operation	
	L	H	H	H	No Operation	NOP. Continue previous operation	
Idle	L	L	H	H	Active	Select and activate row	
	L	L	L	H	Auto Refresh	Auto Refresh	7
	L	L	L	L	Mode Register Set	Mode Register Set	7
Row Active	L	H	L	H	Read	Select column and start Read burst	10
	L	H	L	L	Write	Select column and start Write burst	10
	L	L	H	L	Precharge	Deactivates row in bank(s)	8
Read (Auto Precharge Disabled)	L	H	L	H	Read	Select column and start new Read burst	10
	L	H	L	L	Write	Select column and start new Write burst	10,12
	L	L	H	L	Precharge	Truncate Read burst, start precharge	8
	L	H	H	L	Burst Termination	Burst Terminate	9
Write (Auto Precharge Disabled)	L	H	L	H	Read	Select column and start Read burst	10,11
	L	H	L	L	Write	Select column and start Write burst	10
	L	L	H	L	Precharge	truncate Write burst, start precharge)	8,11

1. This table applies when CKE n-1 was high and CKE n is high (see Truth Table 2: Clock Enable (CKE) and after tXSNR / tXSRD has been met (if the previous state was self refresh).
2. This table is bank-specific, except where noted, i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.
3. Current state definitions:
   Idle: The bank has been precharged, and tRP has been met.
   Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Write: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank. DESELECT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Truth Table 3, and according to Truth Table 4.
   Precharging: Starts with registration of a Precharge command and ends when tRP is met. Once tRP is met, the bank is in the idle state.
   Row Activating: Starts with registration of an Active command and ends when tRCD is met. Once tRCD is met, the bank is in the "row active" state.
   Read w/Auto Precharge Enabled: Starts with registration of a Read command with Auto Precharge enabled and ends when tRP has been met. Once tRP is met, the bank is in the idle state.
   Write w/Auto Precharge Enabled: Starts with registration of a Write command with Auto Precharge enabled and ends when tRP has been met. Once tRP is met, the bank is in the idle state.
5. The following states must not be interrupted by any executable command; Deselect or NOP commands must be applied on each positive clock edge during these states.
   Refreshing: Starts with registration of an Auto Refresh command and ends when tRFC is met. Once tRFC is met, the DDR SDRAM is in the "all banks idle" state.
   Accessing Mode Register: Starts with registration of a Mode Register Set command and ends when tMRD has been met. Once tMRD is met, the DDR SDRAM is in the "all banks idle" state.
   Precharging All: Starts with registration of a Precharge All command and ends when tRP is met. Once tRP is met, all banks is in the idle state.
6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle.
8. May or may not be bank-specific; if all/any banks are to be precharged, all/any must be in a valid state for precharging.
9. Not bank-specific; Burst terminate affects the most recent Read burst, regardless of bank.
10. Reads or Writes listed in the Command/Action column include Reads or Writes with Auto Precharge enabled and Reads or Writes with Auto Precharge disabled.
11. Requires appropriate DM masking.
12. A WRITE command may be applied after the completion of the READ burst; otherwise, a Burst Terminate must be used to end the READ prior to asserting a WRITE command,
13 Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

Truth Table 4: Current State Banks n – Command to Bank m (dIFFERENT Bank)

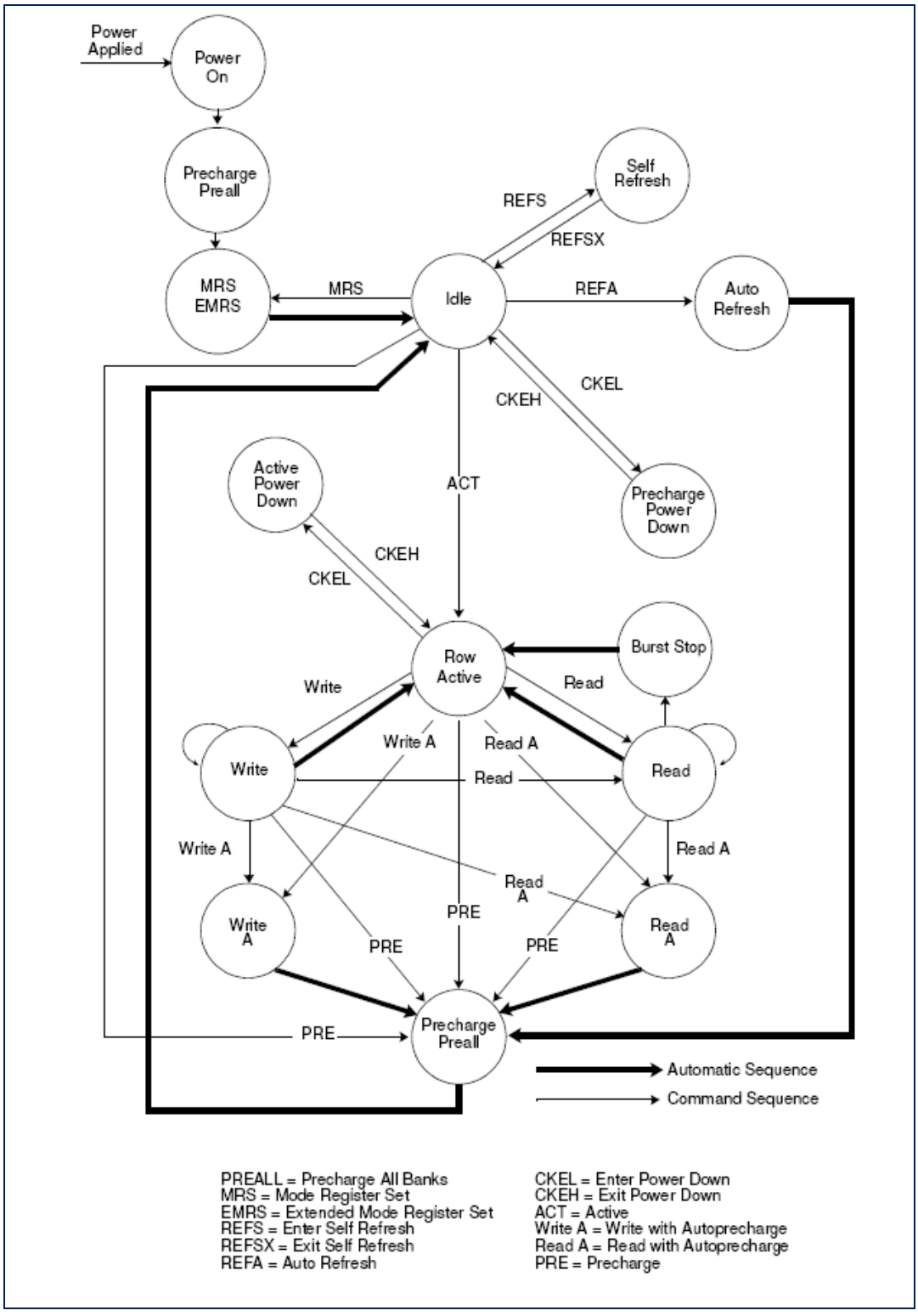
Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command	Action	Notes
Any	H	X	X	X	Deselect	NOP. Continue previous operation	
	L	H	H	H	No Operation	NOP. Continue previous operation	
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank m		
Row Activating, Active or Precharge	L	L	H	H	Active	Select and active Row	
	L	H	L	H	Read	Select column and start Read burst	7
	L	H	L	L	Write	Select column and start Write burst	7
	L	L	H	L	Precharge		
Read (Auto Precharge Disabled)	L	L	H	H	Active	Select and activate row	
	L	H	L	H	Read	Select column and start new Read burst	7
	L	H	L	L	Write	Select column and start new Write burst	7,9
	L	L	H	L	Precharge		
Write (Auto Precharge Disabled)	L	L	H	H	Active	Select and active Row	
	L	H	L	H	Read	Select column and start Read burst	7,8
	L	H	L	L	Write	Select column and start Write burst	7
	L	L	H	L	Precharge		
Read (with Auto Precharge)	L	L	H	H	Active	Select and active Row	
	L	H	L	H	Read	Select column and start Read burst	3a,7
	L	H	L	L	Write	Select column and start Write burst	3a,7,9
	L	L	H	L	Precharge		
Write (with Auto Precharge)	L	L	H	H	Active	Select and active Row	
	L	H	L	H	Read	Select column and start Read burst	3a,7
	L	H	L	L	Write	Select column and start Write burst	3a,9
	L	L	H	L	Precharge		

1. This table applies when CKE n-1 was high and CKE n is high (see Truth Table 2: Clock Enable (CKE) and after tXSNR / tXSRD has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted, i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:
   Idle: The bank has been precharged, and tRP has been met.
   Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Write: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Read with Auto Precharge Enable: See following text, notes 3a, 3b, and 3c:
   Write with Auto Precharge Enable: See following text, notes 3a, 3b, and 3c:
   3a. For devices which *do not support* the optional "concurrent auto precharge" feature, the Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states can each be broken into two parts: the access period and the precharge period. For Read with Auto Precharge, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For Write with Auto Precharge, the precharge period begins when tWR ends, with tWR measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or tRP) begins. During the precharge period of the Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states, ACTIVE, PRECHARGE, READ and WRITE commands to the other bank may be applied; during the access period, only ACTIVE and PRECHARGE commands to the other bank may be applied. In either case, all other related limitations apply (e.g., contention between READ data and WRITE data must be avoided).
   3b. For devices which *do support* the optional "concurrent auto precharge" feature, a read with auto precharge enabled, or a write with auto precharge enabled, may be followed by any command to the other banks, as long as that command does not interrupt the read or write data transfer, and all other related limitations apply (e.g., contention between READ data and WRITE data must be avoided.)
   3c. The minimum delay from a read or write command with auto precharge enable, to a command to a different bank, is summarized below, for both cases of "concurrent auto precharge," supported or not:

From Command	To Command (Different bank)	Minimum Delay Without Concurrent Auto Precharge Support	Minimum Delay WithConcurrent Auto Precharge Support	Units
Write w/AP	Read or Read w/AP	1+(BL/2) + (tWR/tCK) (rounded up)	1+(BL/2) + tWTR	tCK
	Write or Write w/AP	1+(BL/2) + (tWR/tCK) (rounded up)	BL/2	
	Precharge or Activate	1		
Read w/AP	Read or Read w/AP	BL/2		
	Write or Write w/AP	CL (rounded up) + (BL/2)		
	Precharge or Activate	1		

4. AUTO REFRESH and MODE REGISTER SET commands may only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs listed in the Command/Action column include READs or WRITEs with AUTO PRECHARGE enabled and READs or WRITEs with AUTO PRECHARGE disabled.
8. Requires appropriate DM masking.
9. A WRITE command may be applied after the completion of data output, otherwise a Burst Terminate must be used to the READ prior to asserting a WRITE command..
10. Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

Simplified State Diagram



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
VIN, VOUT	Voltage on I/O pins relative to VSS	-0.5 to VDDQ+ 0.5	V
VIN	Voltage on Inputs relative to VSS	-1.0 to +3.6	V
VDD	Voltage on VDD supply relative to VSS	-1.0 to +3.6	V
VDDQ	Voltage on VDDQ supply relative to VSS	-1.0 to +3.6	V
TA	Operating Temperature (Ambient)	0 to +70 (Commercial Grade)	℃
		-40 to +85 (Industrial Grade)	℃
TSTG	Storage Temperature (Plastic)	-55 to +150	℃
PD	Power Dissipation	1.0	W
IOUT	Short Circuit Output Current	50	mA

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Capacitance

Paramester	Symbol	Min.	Max.	Units	Notes
Input Capacitance: CK, $\overline{CK}$	CI1	2.0	3.0	pF	1
Delta Input Capacitance: CK, $\overline{CK}$	delta CI1	-	0.25	pF	1
Input Capacitance: All other input-only pins (except DM)	CI2	2.0	3.0	pF	1
Delta Input Capacitance: All other input-only pins (except DM)	delta CI2	-	0.5	pF	1
Input/Output Capacitance: DQ, DQS, DM	CIO	4.0	5.0	pF	1,2
Delta Input/Output Capacitance: DQ, DQS, DM	delta CIO	-	0.5	pF	1

1. VDDQ = VDD = 2.5V ± 0.2V(DDR266/333); 2.6V ± 0.1V(DDR400/450/500) (minimum range to maximum range), f = 100MHz, TA = 25°C, VODC = VDDQ/2, VOPeak -Peak = 0.2V.
2. Although DM is an input-only pin, the input capacitance of this pin must model the input capacitance of the DQ and DQS pins. This is required to match input propagation times of DQ, DQS and DM in the system.

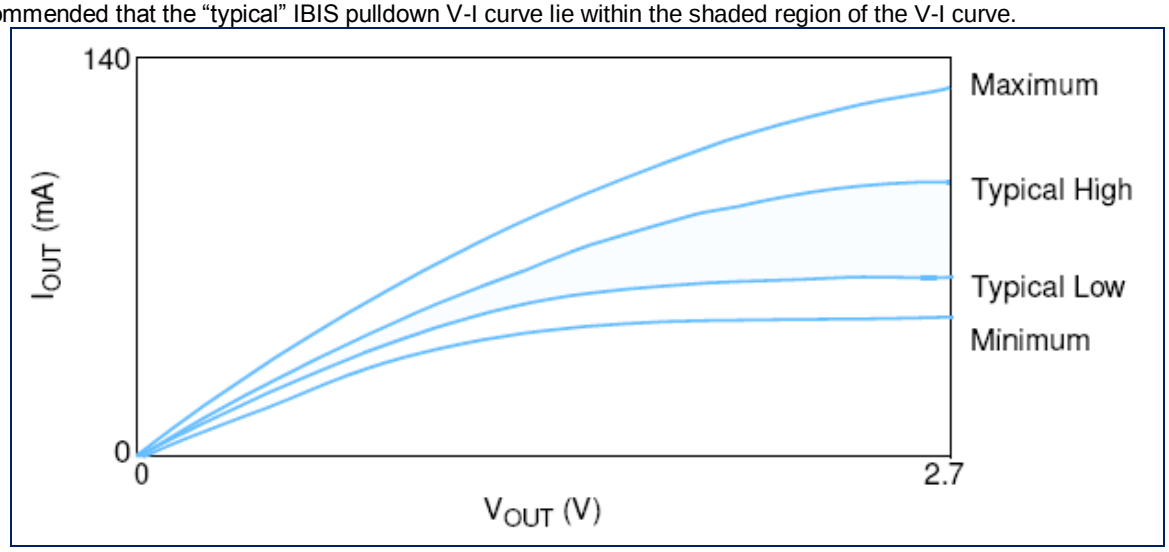
DC Electrical Characteristics and Operating Conditions

Symbol	Paramester	Min		Max	Units	Notes
VDD	Supply Voltage	DDR 266/333	DDR 400/450/500	2.7	V	1
		2.3	2.5			
VDDQ	I/O Supply Voltage	2.3	2.5	2.7	V	1
VREF	I/O Reference Voltage	0.49 x VDDQ		0.51 x VDDQ	V	1,2
VTT	I/O Termination Voltage (System)	VREF - 0.04		VREF + 0.04	V	1,3
VIH(DC)	Input High (Logic1) Voltage	VREF + 0.15		VDDQ + 0.3	V	1
VIL(DC)	Input Low (Logic0) Voltage	- 0.3		VREF - 0.15	V	1
VIN(DC)	Input Voltage Level, CK and $\overline{CK}$ Inputs	- 0.3		VDDQ + 0.3	V	1
VID(DC)	Input Differential Voltage, CK and $\overline{CK}$ Inputs	0.36		VDDQ + 0.6	V	1,4
VIX(DC)	Input Crossing Point Voltage, CK and $\overline{CK}$ Inputs	0.30		VDDQ + 0.6	V	1,4
VIRatio	V-I Matching Pullup Current to Pulldown Current Ratio	0.71		1.4		5
II	Input Leakage Current Any input 0V ≦ VIN ≦ VDD; (All other pins not under test = 0V)	-2		2	µA	
IOZ	Output Leakage Current (DQs are disabled; 0V ≦ Vout ≦ VDDQ	-5		5	µA	1
IOH	Output Current: Nominal Strength Driver High current (VOUT= VDDQ -0.373V, min VREF, min VTT) Low current (VOUT= 0.373V, max VREF, max VTT)	-16.2			mA	1
IOL		16.2				

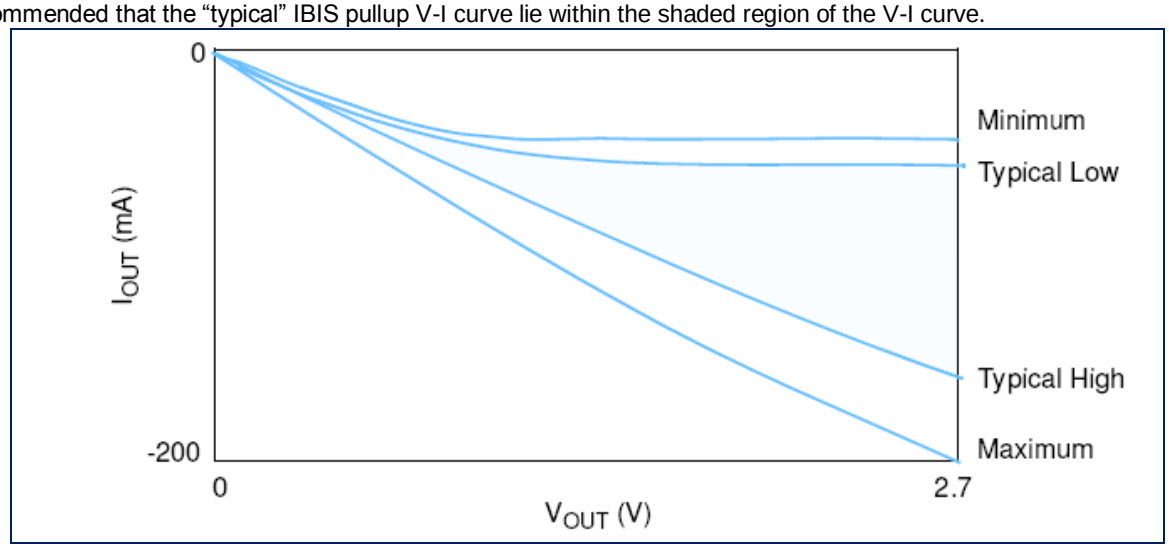
1. Inputs are not recognized as valid until V_{REF} stabilizes.
2. V_{REF} is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed ± 2% of the DC value.
3. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
4. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK.
5. The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages for 0.25 volts to 1.0 volts. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.

Normal Strength Driver Pulldown and Pullup Characteristics

1. The full variation in driver pulldown current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve.
2. It is recommended that the “typical” IBIS pulldown V-I curve lie within the shaded region of the V-I curve.



3. The full variation in driver pullup current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve.
4. It is recommended that the “typical” IBIS pullup V-I curve lie within the shaded region of the V-I curve.



5. The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1.7, for device drain to source voltages from 0.1 to 1.0.
6. The full variation in the ratio of the “typical” IBIS pullup to “typical” IBIS pulldown current should be unity + 10%, for device drain to source voltages from 0.1 to 1.0. This specification is a design objective only. It is not guaranteed.
7. These characteristics are intended to obey the SSTL_2 class II standard.
8. This specification is intended for DDR SDRAM only.

Normal Strength Driver Pulldown and Pullup Currents

Voltage (V)	Pull Down Current (mA)				Pullup Current (mA)			
	Typical Low	Typical High	Min	Max	Typical Low	Typical High	Min	Max
0.1	6.0	6.8	4.6	9.6	-6.1	-7.6	-4.6	-10.0
0.2	12.2	13.5	9.2	18.2	-12.2	-14.5	-9.2	-20.0
0.3	18.1	20.1	13.8	26.0	-18.1	-21.2	-13.8	-29.8
0.4	24.1	26.6	18.4	33.9	-24.0	-27.7	-18.4	-38.8
0.5	29.8	33.0	23.0	41.8	-29.8	-34.1	-23.0	-46.8
0.6	34.6	39.1	27.7	49.4	-34.3	-40.5	-27.7	-54.4
0.7	39.4	44.2	32.2	56.8	-38.1	-46.9	-32.2	-61.8
0.8	43.7	49.8	36.8	63.2	-41.1	-53.1	-36.0	-69.5
0.9	47.5	55.2	39.6	69.9	-43.8	-59.4	-38.2	-77.3
1.0	51.3	60.3	42.6	76.3	-46.0	-65.5	-38.7	-85.2
1.1	54.1	65.2	44.8	82.5	-47.8	-71.6	-39.0	-93.0
1.2	56.2	69.9	46.2	88.3	-49.2	-77.6	-39.2	-100.6
1.3	57.9	74.2	47.1	93.8	-50.0	-83.6	-39.4	-108.1
1.4	59.3	78.4	47.4	99.1	-50.5	-89.7	-39.6	-115.5
1.5	60.1	82.3	47.7	103.8	-50.7	-95.5	-39.9	-123.0
1.6	60.5	85.9	48.0	108.4	-51.0	-101.3	-40.1	-130.4
1.7	61.0	89.1	48.4	112.1	-51.1	-107.1	-40.2	-136.7
1.8	61.5	92.2	48.9	115.9	-51.3	-112.4	-40.3	-144.2
1.9	62.0	95.3	49.1	119.6	-51.5	-118.7	-40.4	-150.5
2.0	62.5	97.2	49.4	123.3	-51.6	-124.0	-40.5	-156.9
2.1	62.9	99.1	49.6	126.5	-51.8	-129.3	-40.6	-163.2
2.2	63.3	100.9	49.8	129.5	-52.0	-134.6	-40.7	-169.6
2.3	63.8	101.9	49.9	132.4	-52.2	-139.9	-40.8	-176.0
2.4	64.1	102.8	50.0	135.0	-52.3	-145.2	-40.9	-181.3
2.5	64.6	103.8	50.2	137.3	-52.5	-150.5	-41.0	-187.6
2.6	64.8	104.6	50.4	139.2	-52.7	-155.3	-41.1	-192.9
2.7	65.0	105.4	50.5	140.8	-52.8	-160.1	-41.2	-198.2

Normal Strength Driver Evaluation Conditions

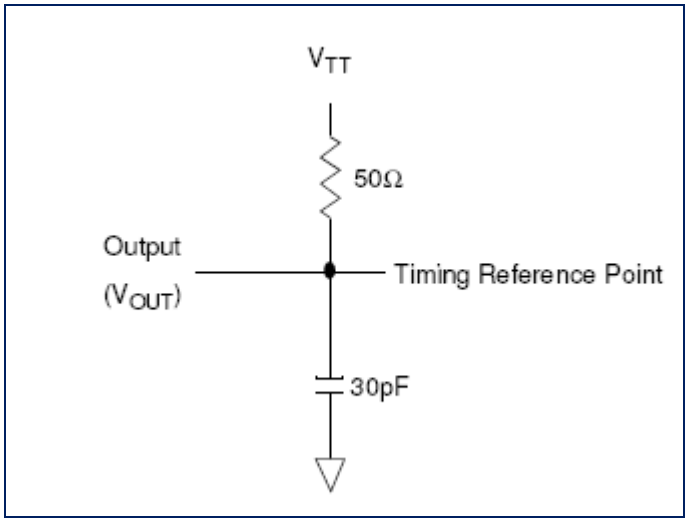
Item	Typical	Minimum	Maximum
Temperature ($T_{ambient}$)	25℃	70℃	0℃
V_{DDQ}	2.5V	2.3V	2.7V
Process conditions	Typical Process	slow-slow process	fast-fast process

AC Characteristics

(Notes 1-5 apply to the following Tables; Electrical Characteristics and DC Operating Conditions, AC Operating Conditions, IDD Specifications and Conditions, and Electrical Characteristics and AC Timing.)

1. All voltages referenced to VSS.
2. Tests for AC timing, IDD, and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load. Refer to the AC Output Load Circuit below.
4. AC timing and IDD tests may use a VIL to VIH swing of up to 1.5V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK, CK), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1V/ns in the range between VIL(AC) and VIH(AC).
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver effectively switches as a result of the signal crossing the AC input level, and remains in that state as long as the signal does not ring back above (below) the DC input low (high) level.

AC Output Load Circuit Diagrams



AC Input Operating Conditions

(0 °C ≤ TA ≤ 70 °C; VDDQ = VDD = + 2.5V ± 0.2V (DDR266/333); VDDQ = VDD =+ 2.6V ± 0.1V (DDR400/450/500);

Symbol	Parameter / Condition	Min	Max	Unit	Note
VIH(AC)	Input High (Logic 1) Voltage, DQ, DQS, and DM Signals	VREF + 0.31	-	V	1,2
VIL(AC)	Input Low (Logic 0) Voltage, DQ, DQS, and DM Signals	-	VREF – 0.31	V	1,2
VID(AC)	Input Differential Voltage, CK and CK Inputs	0.7	VDDQ + 0.6	V	1,2,3
VIX(AC)	Input Crossing Point Voltage, CK and CK Inputs	0.5*VDDQ – 0.2	0.5*VDDQ + 0.2	V	1,2,4

1. Input slew rate = 1V/ns.
2. Inputs are not recognized as valid until VREF stabilizes.
3. VID is the magnitude of the difference between the input level on CK and the input level on CK.
4. The value of VIX is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the DC level of the same.

IDD Specifications and Conditions

(0 °C ≤ TA ≤ 70 °C; VDDQ = VDD = + 2.5V ± 0.2V (DDR266/333); VDDQ = VDD =+ 2.6V ± 0.1V (DDR400/450/500);; See AC Characteristics)

Symbol	Parameter/Condition	I/O	DDR333		DDR400		DDR500		Unit	Notes
			-6K/6KI		-5T/5TI		-4T			
			Typ	Max	Typ	Max	Typ	Max		
IDD0	**Operating Current**: one bank; active / precharge; tRC = tRC (min); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cyc	x8 x16	53 61	61 67	61 69	70 75	TBD	TBD	mA	1,2
IDD1	**Operating Current**: one bank; active / read / precharge; Burst = 2; tRC = tRC (min); CL = 2.5; IOUT = 0mA; address and control inputs changing once per clock cycle	x8 x16	48 55	56 63	54 63	64 71	TBD	TBD	mA	1,2
IDD2P	**Precharge Power Down Standby Current**: all banks idle; Power Down mode; CKE ≦ VIL (max)	All	4	9	4	10	TBD	TBD	mA	1
IDD2F	**Idle Standby Current:** $\overline{CS}$ ≧ VIH (min); all banks idle; CKE ³ VIH (min); address and control inputs changing once per clock cycle	All	22	27	24	29	TBD	TBD	mA	1
IDD2Q	**Precharge floating standby current:** $\overline{CS}$ ≧VIH (min); all banks idle; CKE ≧ VIH (min); address and control inputs changing once per clock cycle	All	17	27	18	28	TBD	TBD	mA	1
IDD3P	**Active Power Down Standby Current**: one bank active; Power Down mode; CKE ≦ VIL(max)	All	9	14	10	15	TBD	TBD	mA	1
IDD3N	**Active Standby Current**: one bank; active / precharge; $\overline{CS}$ ≧ VIH (min);CKE ≧ VIH (min); tRC = tRAS (max); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	x8 x16	27 33	33 39	30 38	36 43	TBD	TBD	mA	1,2
IDD4R	**Operating Current:** one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; IOUT = 0mA	x8 x16	57 68	69 88	66 78	78 97	TBD	TBD	mA	1,2
IDD4W	**Operating Current**: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL = 2.5	x8 x16	58 65	68 76	66 73	77 90	TBD	TBD	mA	1,2
IDD5	**Auto-Refresh Current**: tRC = tRFC (min)	All	104	112	108	192	TBD	TBD	mA	1
IDD6	**Self-Refresh Current**: CKE ≦0.2V	All	4	9	4	10	TBD	TBD	mA	1
IDD7	**Operating curren**t: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; t RC = t RC (min); I OUT = 0mA.	x8 x16	160 177	187 250	186 205	218 290	TBD	TBD	mA	1,2

1. IDD specifications are tested after the device is properly initialized.
2. Enables on-chip refresh and address counters. Values are averaged from high and low temp values using x16 devices.

Electrical Characteristics & AC Timing - Absolute Specifications

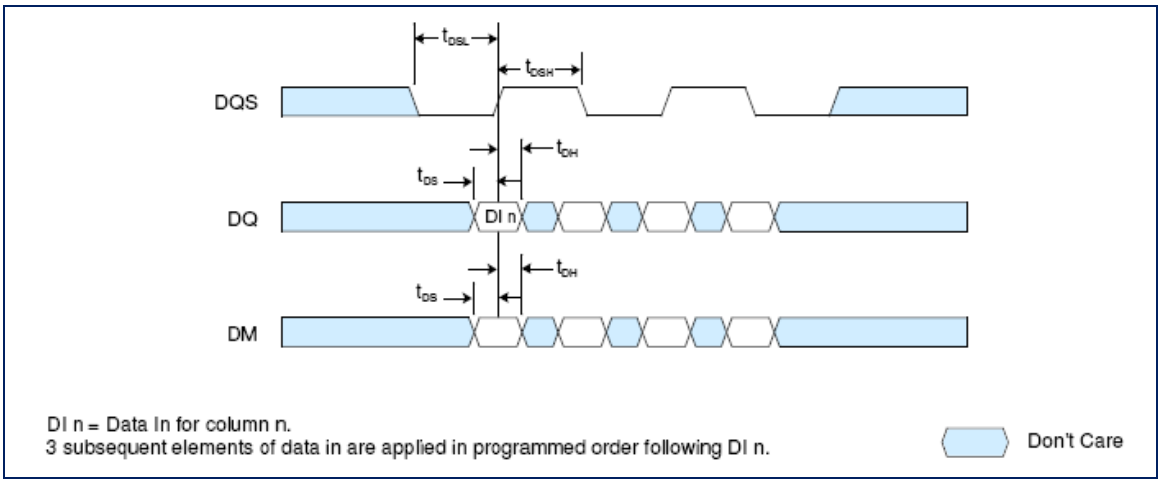
(0 °C ≤ T_A ≤ 70 °C Commercial grade; –40°C ≤ T_A ≤ 85 °C Industrial grade V_{DDQ} = V_{DD} = + 2.5V ± 0.2V (DDR266/333); V_{DDQ} = V_{DD} =+ 2.6V ± 0.1V (DDR400/450/500) ; See AC Characteristics)

Symbol	Parameter		DDR266 (-75A/-75I)		DDR333 (-6K/-6KI)		DDR400 (-5T/-5TI)		DDR450 (-45)		DDR500 (-5T)		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
tAC	DQ output access time from CK/CK		– 0.75	+ 0.75	– 0.70	0.7	– 0.70	+ 0.7	– 0.65	0.65	– 0.70	0.7	ns	
tDQSCK	DQS output access time from CK/CK		– 0.75	+ 0.75	– 0.60	+ 0.60	– 0.60	+ 0.60	– 0.65	0.65	– 0.7	0.7	ns	
tCH	CK high-level width		0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
tCL	CK low-level width		0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
tHP	CK half period		min (tCL, tCH)		min (tCL, tCH)		min (tCL, tCH)		min (tCL, tCH)		min (tCL, tCH)		ns	
tCK	Clock cycle time	CL=3					5	7.5	5	7.5	5	7.5	ns	3
		CL=2.5	7.5	12	6	12	6	12	6	12	6	12		
		CL=2	7.5	12	7.5	12	7.5	12	7.5	12	7.5	12		
tDH	DQ and DM input hold time		0.5		0.45		0.4		0.4		0.4		ns	4
tDS	DQ and DM input setup time		0.5		0.45		0.4		0.4		0.4		ns	4
tIPw	Input pulse width		2.2		2.2		2.2		2.2		2.2		ns	5
tDIPw	DQ and DM input pulse width (each input)		1.75		1.75		1.75		1.75		1.75		ns	5
tHZ	Data-out high-impedance time from CK/CK			0.75		0.7		0.7		0.7		0.7	ns	6
tLZ	Data-out low-impedance time from CK/CK		– 0.75	0.75	– 0.7	0.7	– 0.7	0.7	– 0.7	0.7	– 0.7	0.7	ns	6
tDQSQ	DQS-DQ skew (DQS & associated DQ signa)-TSOP			0.5		0.45		0.4		0.5		0.4	ns	
	DQS-DQ skew (DQS & associated DQ signals)-BGA			0.5		0.4		0.4		0.5		0.4	ns	
tQH	Data output hold time from DQS		tHP - tQHS		tHP - tQHS		tHP - tQHS		tHP - tQHS		tHP - tQHS		ns	
tQHS	Data hold Skew Factor-TSOP			0.75		0.55		0.5		0.5		0.4	ns	
tDQSS	write command to 1st DQS latching		0.75	1.25	0.75	1.25	0.72	1.25	0.75	1.25	0.85	1.15	tCK	
tDQSH	DQS input high pulse width (write cycle)		0.35		0.35		0.35		0.4		0.4		tCK	
tDQSL	DQS input low pulse width (write cycle)		0.35		0.35		0.35		0.4		0.4		tCK	
tDSS	DQS falling edge to CK setup time (write cycle)		0.2		0.2		0.2		0.2		0.2		tCK	
tDSH	DQS falling edge hold time from CK (write cycle)		0.2		0.2		0.2		0.2		0.2		tCK	
tMRD	Mode register set command cycle time		2		2		2		2		2		tCK	
twPRES	write preamble setup time		0		0		0		0		0		ns	
twPST	write postamble		0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	9
twPRE	write preamble		0.25		0.25		max(0.25 *tCK, 1.5 ns)		0.25		max(0.25 *tCK, 1.5 ns)		ns	8
tIH	Address and control input hold time (fast slew rate)		0.9		0.75		0.6		0.75		0.6		ns	5, 10-12
tIS	Address and control input setup time (fast slew rate)		0.9		0.75		0.6		0.75		0.6		ns	5, 10-12
tIH	Address and control input hold time (slow slew rate)		1		0.8		0.7		0.8		0.7		ns	5, 11-13
tIS	Address and control input setup time (slow slew rate)		1		0.8		0.7		0.8		0.7		ns	5, 11-13
tRPRE	Read preamble		0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK	14
tRPRES	Read preamble setup time (Optional CL=1.5)			N/A		N/A		N/A		N/A		N/A	ns	
tRPST	Read postamble		0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
tRAS	Active to Precharge		45	120K	42	70K	40	70K	40	70K	40	70K	ns	
tRC	Active to Active/Auto-refresh command period		60		60		55		55		55		ns	
tRFC	Auto-refresh to Active/Auto-refresh command period		75		72		70		72		70		ns	
tRCD	Active to Read or write delay		20		18		15		15		15		ns	
tRP	Precharge command period		20		18		15		15		15		ns	
tRAP	Active to Read Command with Autoprecharge		(tRCD, tRAS)		(tRCD, tRAS)		(tRCD, tRAS)		(tRCD, tRAS)		(tRCD, tRAS)		ns	
tRRD	Active bank A to Active bank B command		15		12		10		10		8		ns	
twR	write recovery time		15		15		15		15		15		ns	
tDAL	Auto precharge write recovery + precharge time		--		--		--		--		--		tCK	15
twTR	Internal write to read command delay		1		1		2		2		2		tCK	
tXSNR	Exit self-refresh to non-read command		75		75		75		75		75		ns	16
tXSRD	Exit self-refresh to read command		200		200		200		200		200		tCK	
tREFI	Average Periodic Refresh Interval			7.8		7.8		7.8		7.8		7.8	µs	4-17

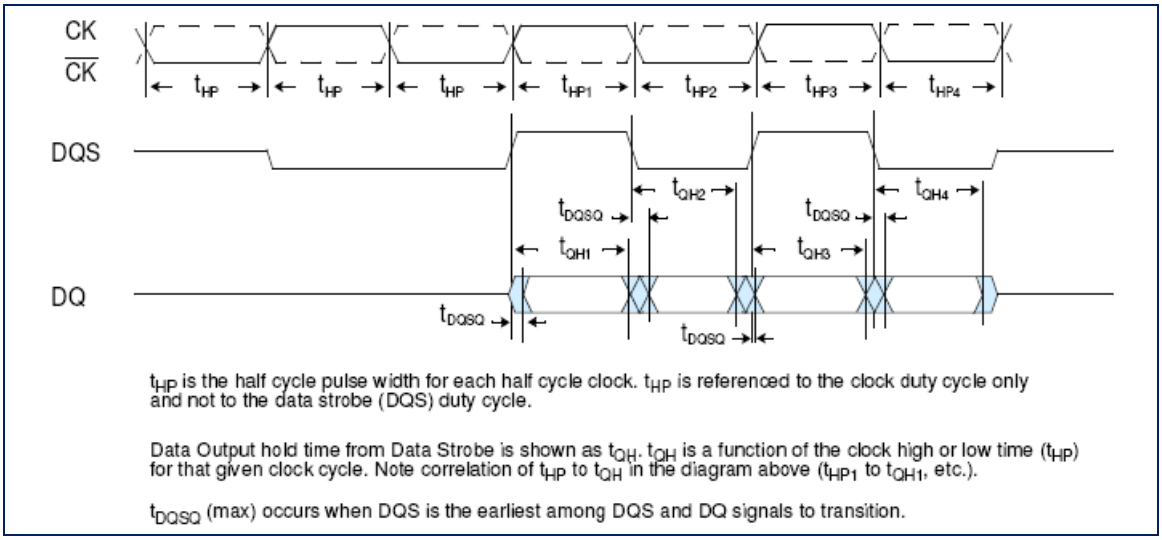
Component Notes

1. Min (tCL, tCH) referes to the smaller of the actual clock low time and actual clock high time as provided to the device. (i.e. this value can be greater than the minimum specification limits for tCL and tCH).
2. tQH = tHP - tQHS, where tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS accounts for 1) The pulse duration distortion of on-chip clock circuits; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
3. The only time that the clock frequency is allowed to change is during self-refresh mode.
4. If refresh time or tDS/tDH is viloated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.
5. These parameters quarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.
6. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These arameters are reference to a specific voltage level that specifies when the device output is no longer driving (tHZ) or begins driving (tLZ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.
7. tDQSQ consists of datapin skew and output pattern effects and p-channel to n-channel variation of the output drivers for any given cycle.
8. The specific requirement is that DQS be valid (High, Low, or at same point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic Low. If a previous write was in process, DQS could be HIGH, LOW, or transitioning from High to Low at this time, depending on DQSS.
9. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turn-arround) will degrade accordingly.
10. For command/address input slew rate >= 1.0V/ns.
11. For CK & CK slew rate >= 1.0V/ns (single-ended).
12. Slew Rate is measured between VOH(ac) and VOL(ac).
13. For command/address input slew rate >= 0.5V/ns and <1.0V/ns.
14. tRPST end point and tRPRE begin point are not reference to a specific voltage level but specify when the device output is no longer driving (tRPRE) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.
15. tDAL = (tWR/tCK) + (tRP/tCK)
16. In all circumstances, tXSNR can be satisfied using tXSNR = tRFCmin + 1*tCK.
17. A maximum of eight Auto Refresh commands can be posted to any given DDR SDRAM.

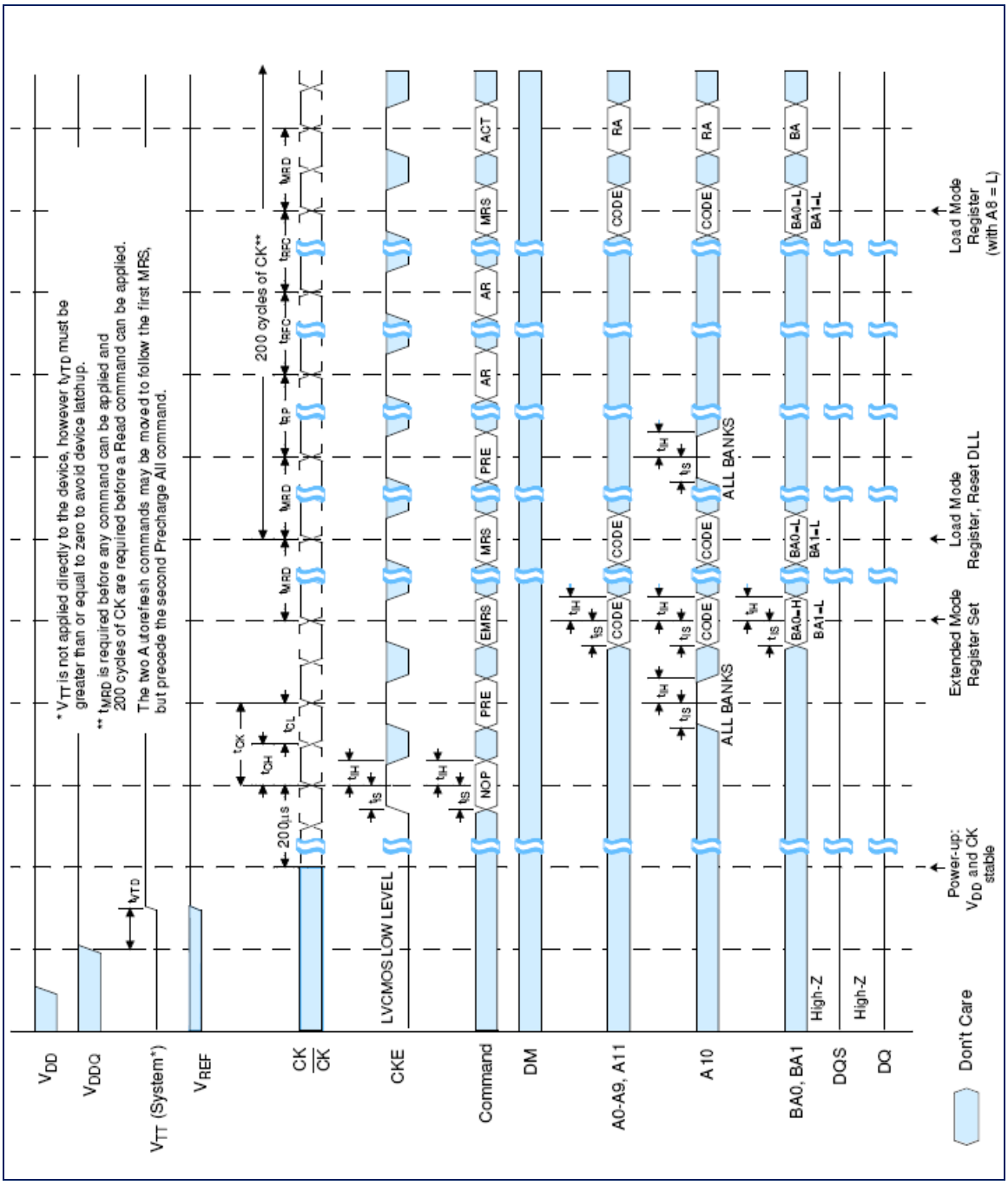
Dada Input (Write) (Timing Burst Length =4)



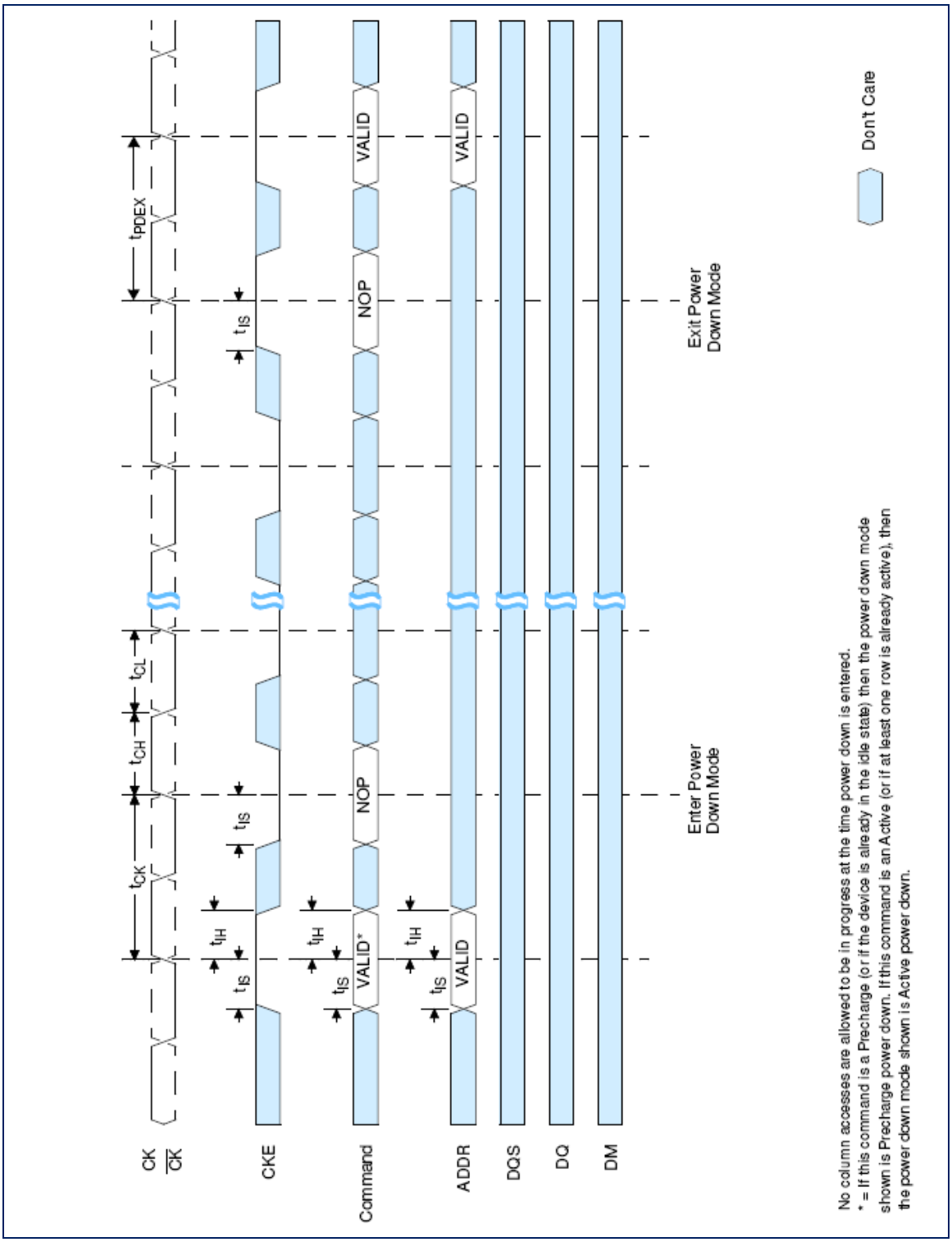
Dada Output (Read) (Timing Burst Length =4)



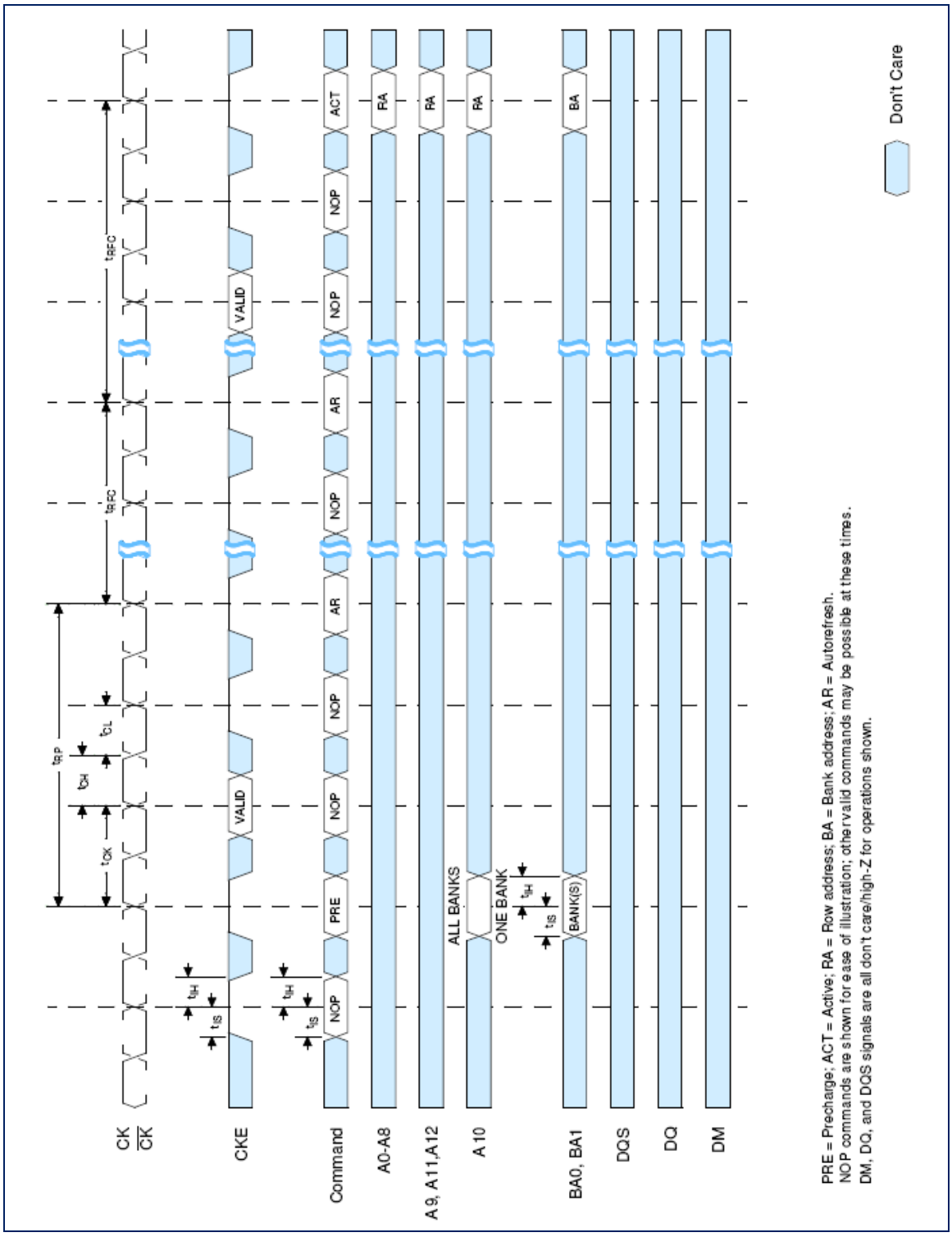
Initialize and Mode Register Set



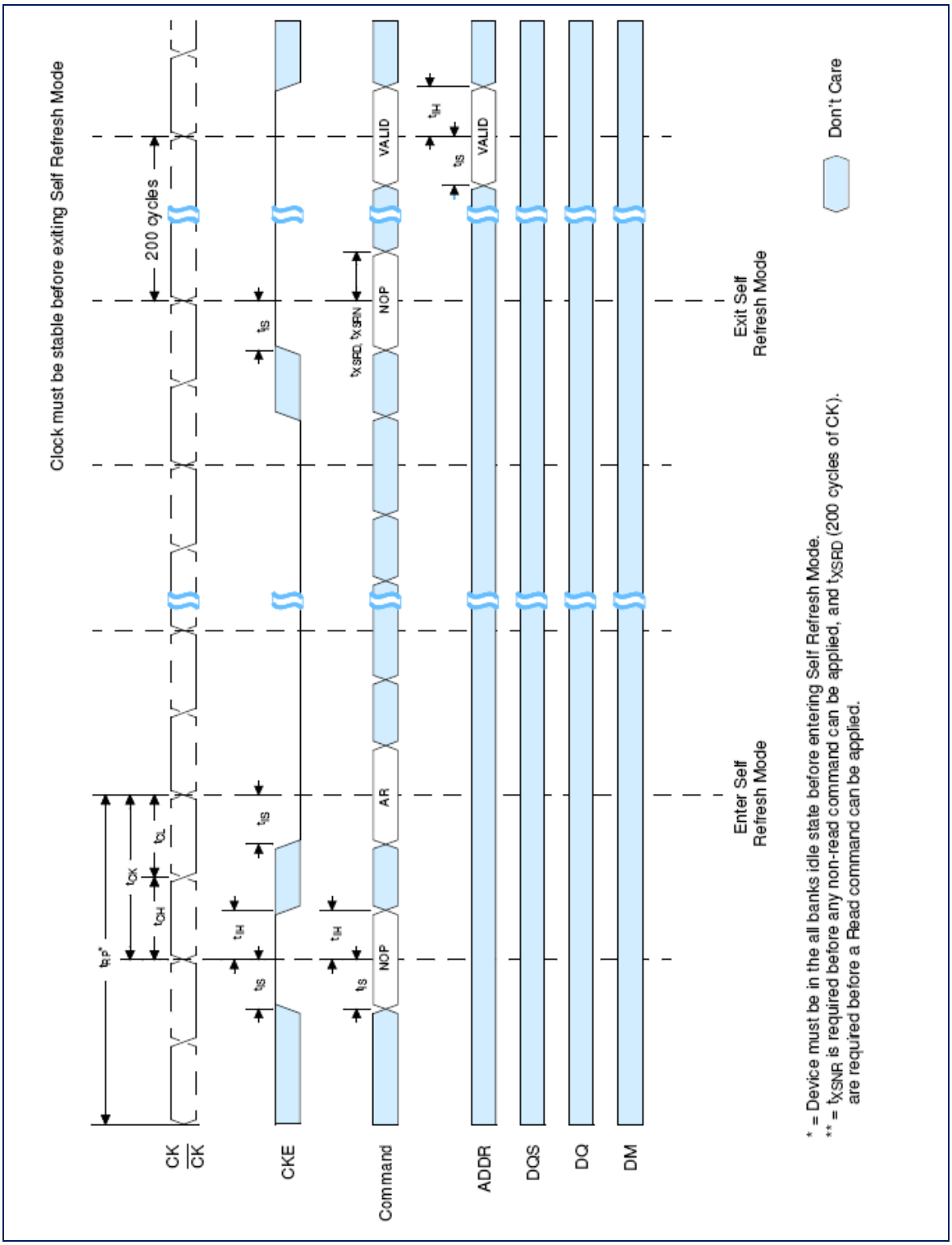
Power Down Mode



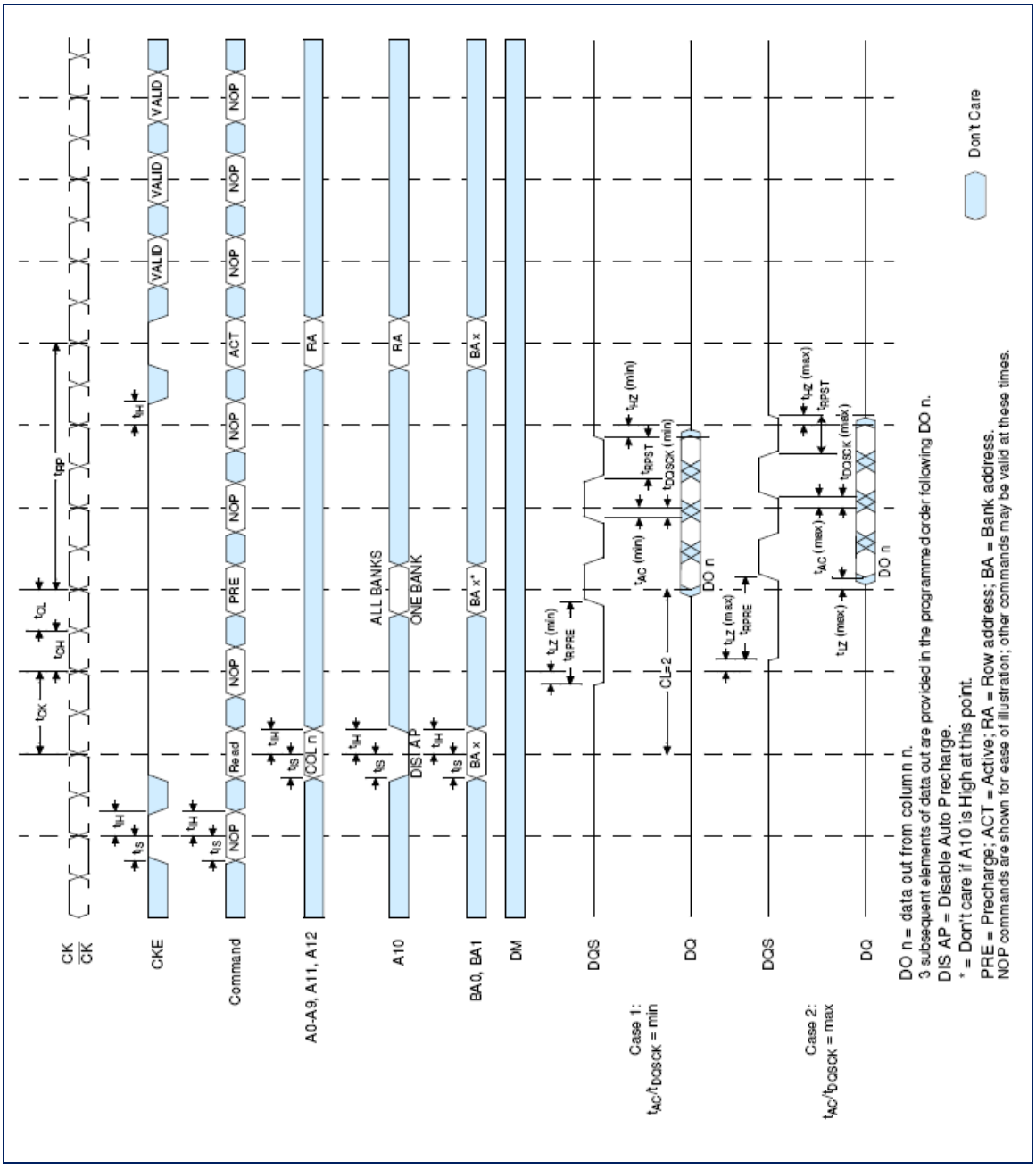
Auto Refresh



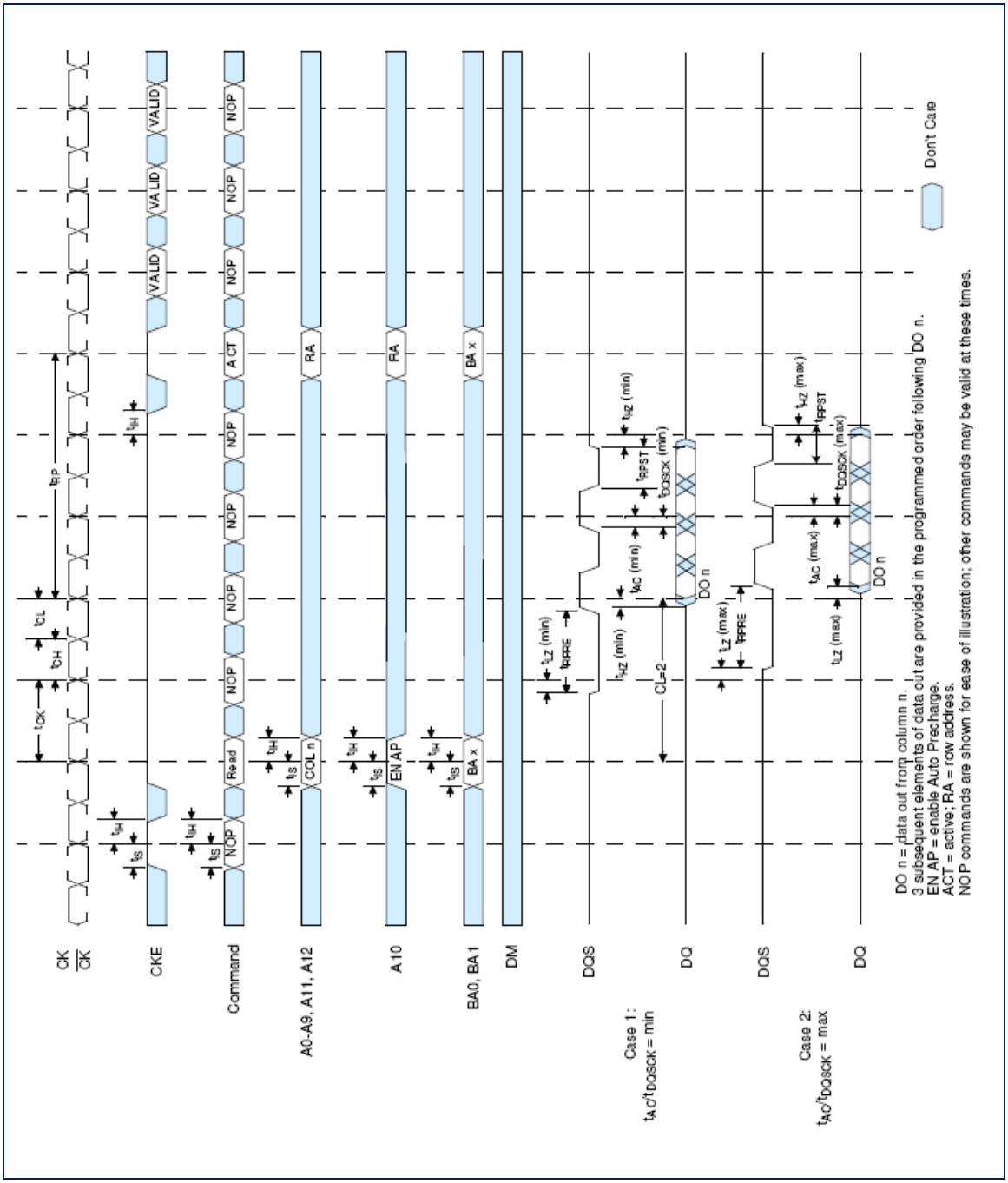
Self Refresh Mode



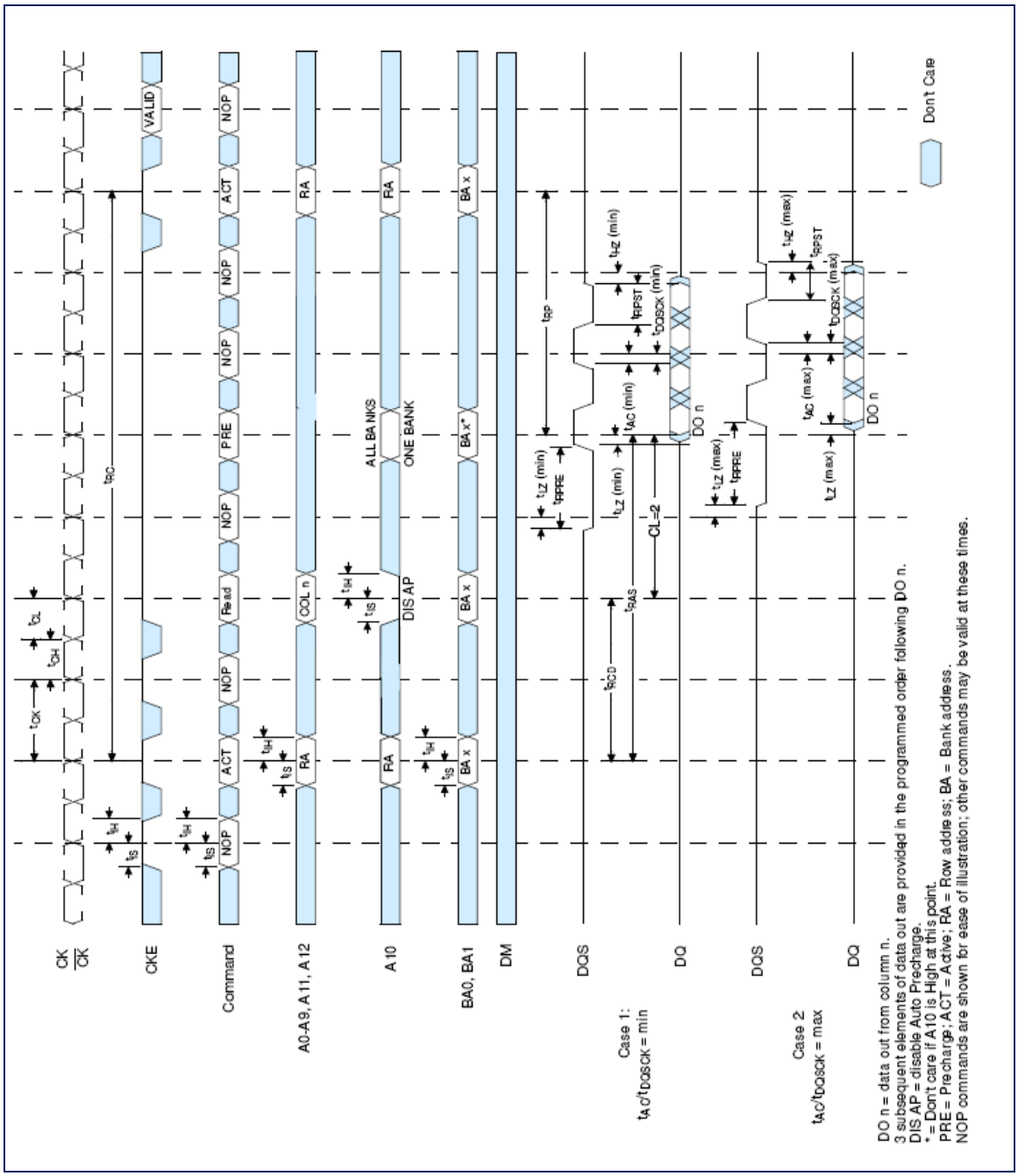
Read without Auto Precharge (Burst Length = 4)



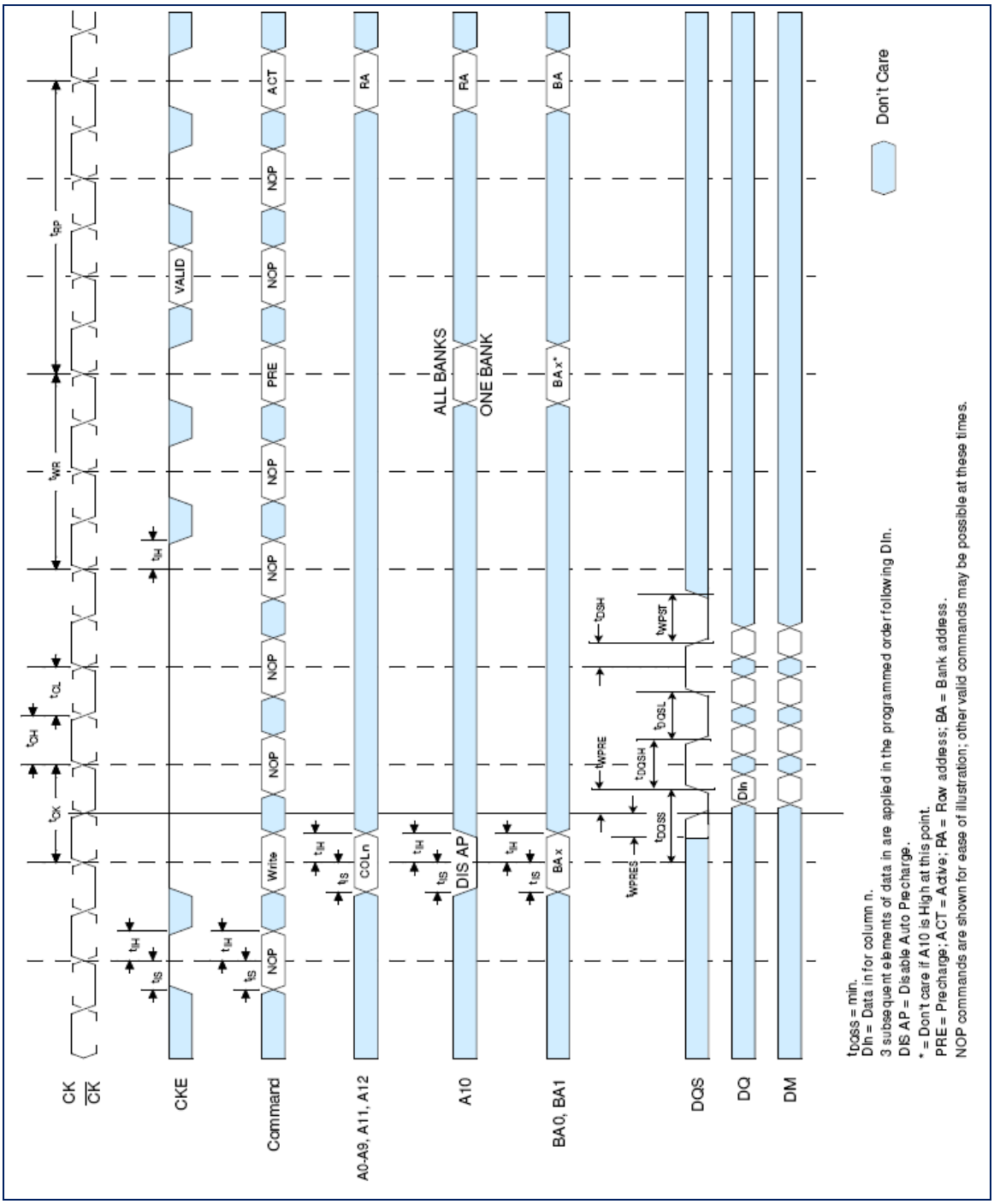
Read with Auto Precharge (Burst Length = 4)



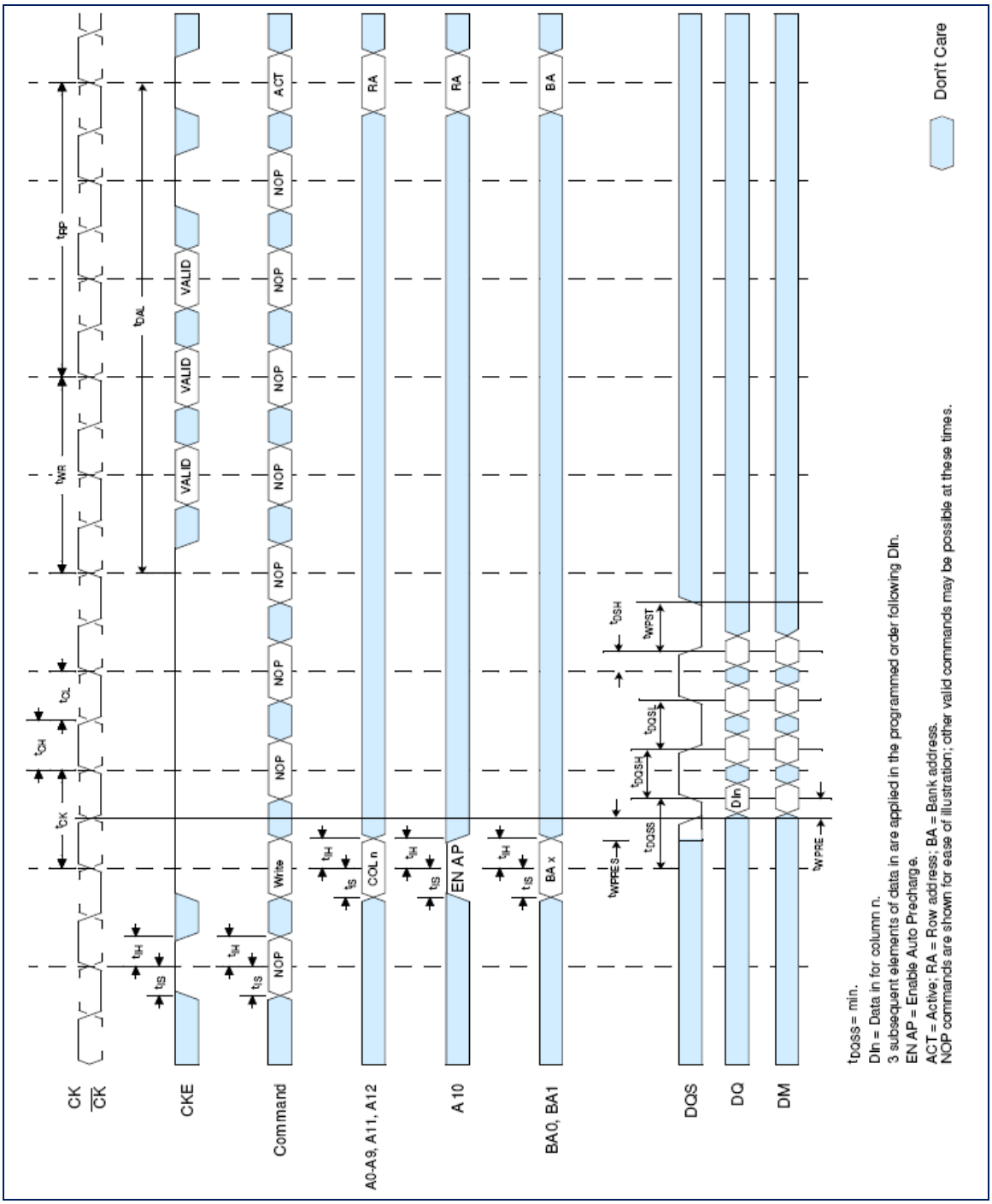
Bank Read Access (burst Length = 4)



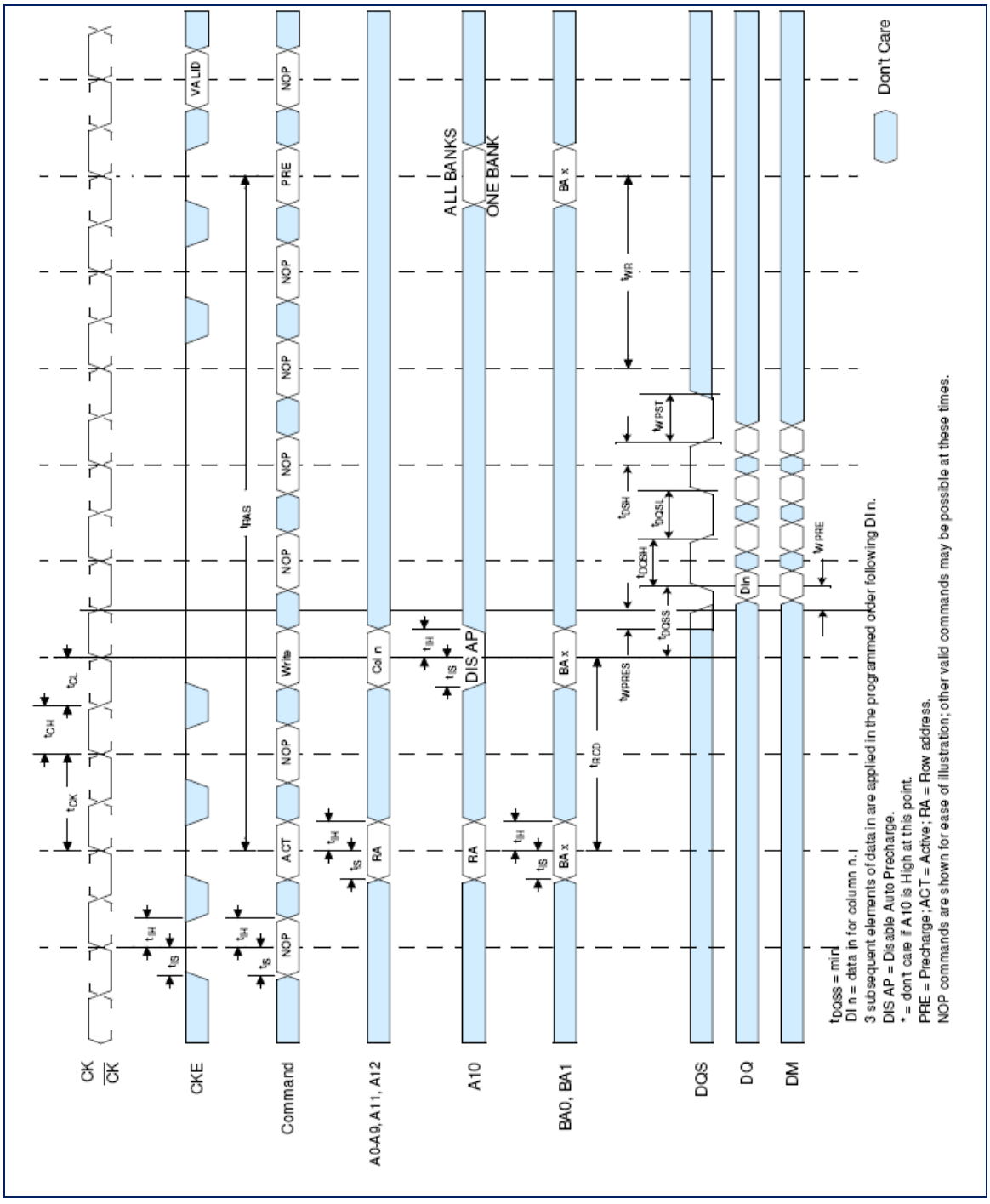
Write without Auto Prechareg (Burst Length = 4)



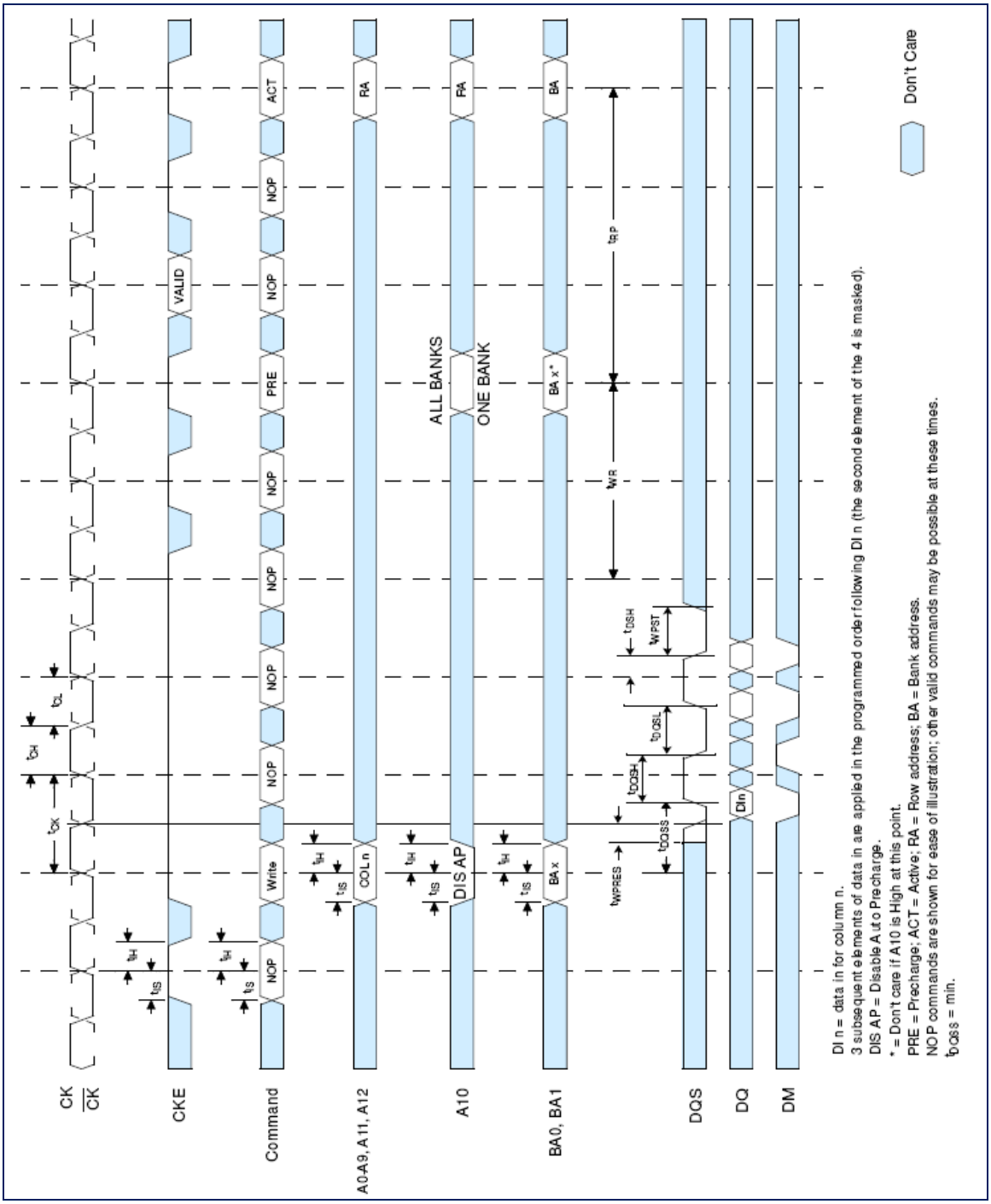
Write with Auto Precharge (Burst Length = 4)



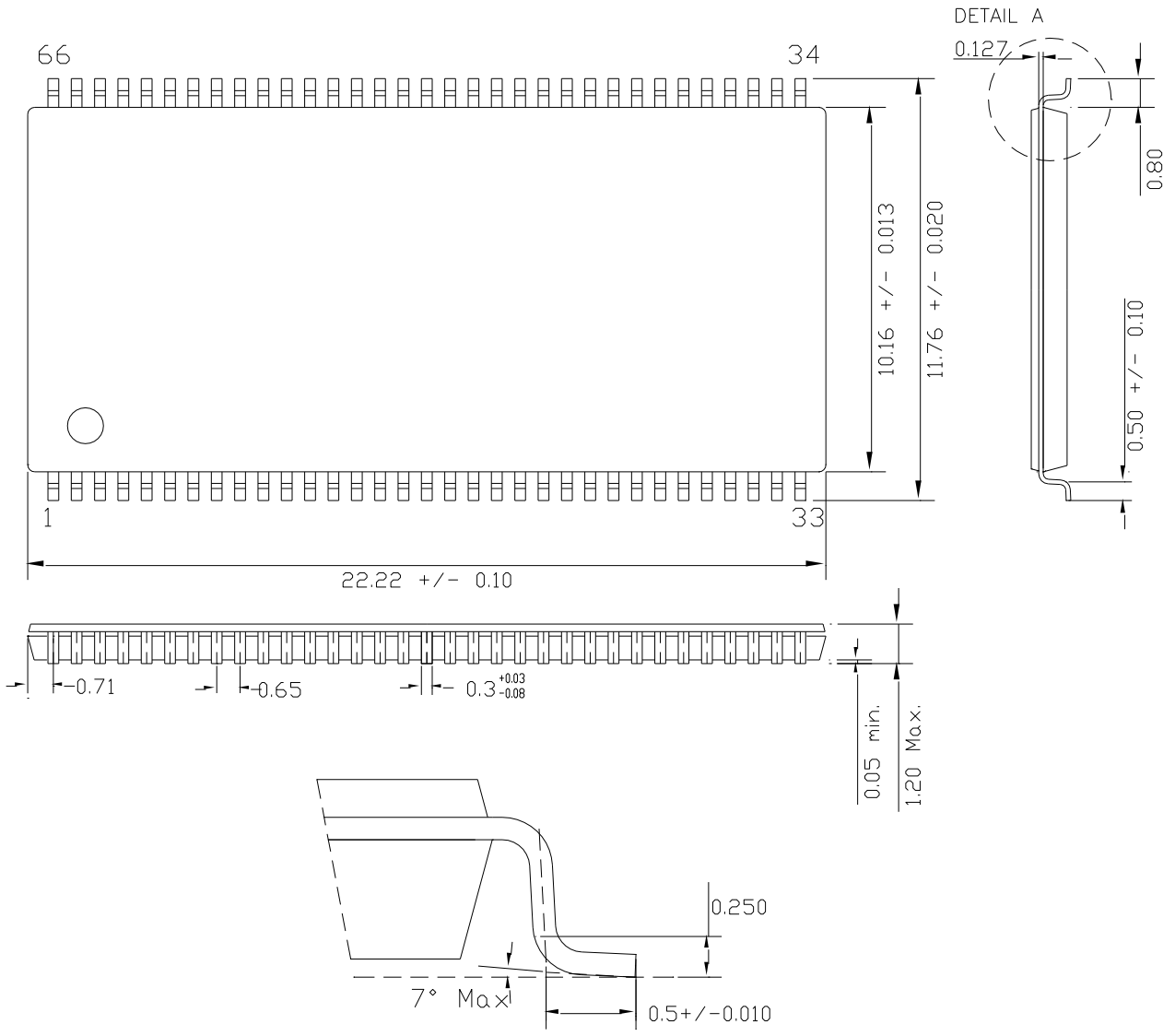
Bank Write Access (Burst Length = 4)



Write DM Operation (Burst Length = 4)



Package Dimensions (400mil; 66 pin TSOP Package)



Revision Log

DCC Version	Rev	Date	Modification
1.0	0.1	Jul 2010	Preliminary Edition
1.0	0.2	Dec 2010	Revised t_{CK} (Max.) of DDR400 and DDR450
1.0	0.3	Jan 2011	Added t_{CK} parameters to CL=3/2.5/2
1.0	1.0	Jun 2011	Official Release
1.0	1.1	Jul 2011	Added I_{DD2Q} parameters and Removed -4T from Ordering Information
1.0	1.2	Aug 2011	Revised IT-grade T_A Range
1.0	1.3	Sep 2011	Revised t_{RRD} of DDR400 and DDR450
1.0	1.4	Oct 2011	Added Weak(Optional) to Drive Strength Mode
1.0	1.5	Oct 2011	Revised V_{DD} at DDR400
1.0	1.6	Jan 2012	Revised Pin 19 Description of Pin Configuration
1.0	1.7	May 2012	Revised V_{DDQ} = V_{DD} at DDR400 on the description of AC Timing Table
1.1	1.1	Sep. 2013	correct the min thickness of POD: 0.05mm(was:0.06mm)
1.2	1.2	Dec. 2013	1. Add note 1 on page 3: speed backward compatible. 2.Correct the typo on page 18: 7.8µs (was:7.8ms)

Printed in Taiwan, R.O.C., 2012

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