Product Brief
January 2002

ORCA® Series 2 Field-Programmable Gate Arrays

Features

- High-performance, cost-effective, low-power 0.35 µm CMOS technology (OR2CxxA), 0.3 µm CMOS technology (OR2TxxA), and 0.25 µm CMOS technology (OR2TxxB), (four-input look-up table (LUT) delay less than 1.0 ns with -8 speed grade)
- High density (up to 43,200 usable, logic-only gates; or 99,400 gates including RAM)
- Up to 480 user I/Os (OR2TxxA and OR2TxxB I/Os are 5 V tolerant to allow interconnection to both 3.3 V and 5 V devices, selectable on a per-pin basis)
- Four 16-bit look-up tables and four latches/flip-flops per PFU, nibble-oriented for implementing 4-, 8-, 16-, and/or 32-bit (or wider) bus structures
- Eight 3-state buffers per PFU for on-chip bus structures
- Fast on-chip user SRAM has features to simplify RAM design and increase RAM speed:
  — Asynchronous single port: 64 bits/PFU
  — Synchronous single port: 64 bits/PFU
  — Synchronous dual port: 32 bits/PFU
- Improved ability to combine PFUs to create larger RAM structures using write-port enable and 3-state buffers
- Fast, dense multipliers can be created with the multiplier mode (4 x 1 multiplier/PFU):
  — 8 x 8 multiplier requires only 16 PFUs
  — 30% increase in speed
- Flip-flop/latch options to allow programmable priority of synchronous set/reset vs. clock enable
- Enhanced cascadable nibble-wide data path capabilities for adders, subtractors, counters, multipliers, and comparators including internal fast-carry operation
- Innovative, abundant, and hierarchical nibble-oriented routing resources that allow automatic use of internal gates for all device densities without sacrificing performance
- Upward bit stream compatible from the *ORCA* ATT2Cxx/ATT2Txx series of devices
- Pinout-compatible with new *ORCA* Series 3 FPGAs
- TTL or CMOS input levels programmable per pin for the OR2CxxA (5 V) devices
- Individually programmable drive capability: 12 mA sink/6 mA source or 6 mA sink/3 mA source
- Built-in boundary scan (*IEEE* †1149.1 JTAG) and TS_ALL testability function to 3-state all I/O pins.
- Multiple configuration options, including simple, low pin-count serial ROMs, and peripheral or JTAG modes for in-system programming (ISP)
- Full PCI bus compliance for all devices
- Supported by industry-standard CAE tools for design entry, synthesis, and simulation with *ORCA* Foundry Development System support (for back-end implementation)
- New added features (OR2TxxB) provide:
  — More I/O per package than the OR2TxxA family.
  — No dedicated 5 V supply (VDD5).
  — Faster configuration speed (40 MHz).
  — Full PCI bus compliance in both 5 V and 3.3 V PCI systems. Pin selectable I/O clamping diodes provide 5 V or 3.3 V PCI compliance and 5 V tolerance.

* *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Table 1. *ORCA* Series 2 FPGAs

Device	Usable Gates*	LUTs	Registers	Max User RAM Bits	User I/Os	Array Size
OR2C04A/OR2T04A	4,800—11,000	400	400	6,400	160	10 x 10
OR2C06A/OR2T06A	6,900—15,900	576	576	9,216	192	12 x 12
OR2C08A/OR2T08A	9,400—21,600	784	724	12,544	224	14 x 14
OR2C10A/OR2T10A	12,300—28,300	1024	1024	16,384	256	16 x 16
OR2C12A/OR2T12A	15,600—35,800	1296	1296	20,736	288	18 x 18
OR2C15A/OR2T15A/OR2T15B	19,200—44,200	1600	1600	25,600	320	20 x 20
OR2C26A/OR2T26A	27,600—63,600	2304	2304	36,864	384	24 x 24
OR2C40A/OR2T40A/OR2T40B	43,200—99,400	3600	3600	57,600	480	30 x 30

* The first number in the usable gates column assumes 48 gates per PFU (12 gates per four-input LUT/FF pair) for logic-only designs. The second number assumes 30% of a design is RAM. PFUs used as RAM are counted at four gates per bit, with each PFU capable of implementing a 16 x 4 RAM (or 256 gates) per PFU.

Description

The *ORCA* Series 2 series of SRAM-based FPGAs are an enhanced version of the ATT2C/2T architecture. The latest *ORCA* series includes patented architectural enhancements that make functions faster and easier to design while conserving the use of PLCs and routing resources.

The Series 2 devices can be used as drop-in replacements for the ATT2Cxx/ATT2Txx series, respectively, and they are also bit stream compatible with each other. The usable gate counts associated with each series are provided in Table 1. All devices are offered in a variety of packages, speed grades, and temperature ranges.

ORCA FPGAs consist of two basic elements: programmable logic cells (PLCs) and programmable input/output cells (PICs). An array of PLCs is surrounded by PICs as shown in Figure 1. Each PLC contains a programmable function unit (PFU). The PLCs and PICs also contain routing resources and configuration RAM. All logic is done in the PFU. Each PFU contains four 16-bit look-up tables (LUTs) and four latches/flip-flops (FFs).

The LUTs can be programmed to operate in one of three modes: combinatorial, ripple, or memory. In combinatorial mode, the LUTs can be programmed to realize any four-, five-, or six-input logic functions. In ripple mode, the high-speed carry logic is used for arithmetic functions, the multiplier function, or the enhanced data path functions. In memory mode, the LUTs can be used as a 16 x 4 read/write or read-only memory (asynchronous mode or synchronous mode) or a 16 x 2 dual-port memory.

The PLC architecture provides a balanced mix of logic and routing that allows a higher utilized gate/PFU than alternative architectures. The routing resources carry logic signals between PFUs and I/O pads. The routing in the PLC is symmetrical about the horizontal and vertical axes. This improves routability by allowing a bus of signals to be routed into the PLC from any direction.

Each PIC (shown in Figures 2A and 2B) is comprised of I/O drivers, I/O pads, and routing resources. Each I/O can be programmed to be either an input, output, or bidirectional signal. Other options include variable output slew rates and pull-up or pull-down resistors.

OR2TxxA and OR2TxxB I/Os are 5 V tolerant to allow interconnection to both 3.3 V and 5 V devices, selectable on a per-pin basis.

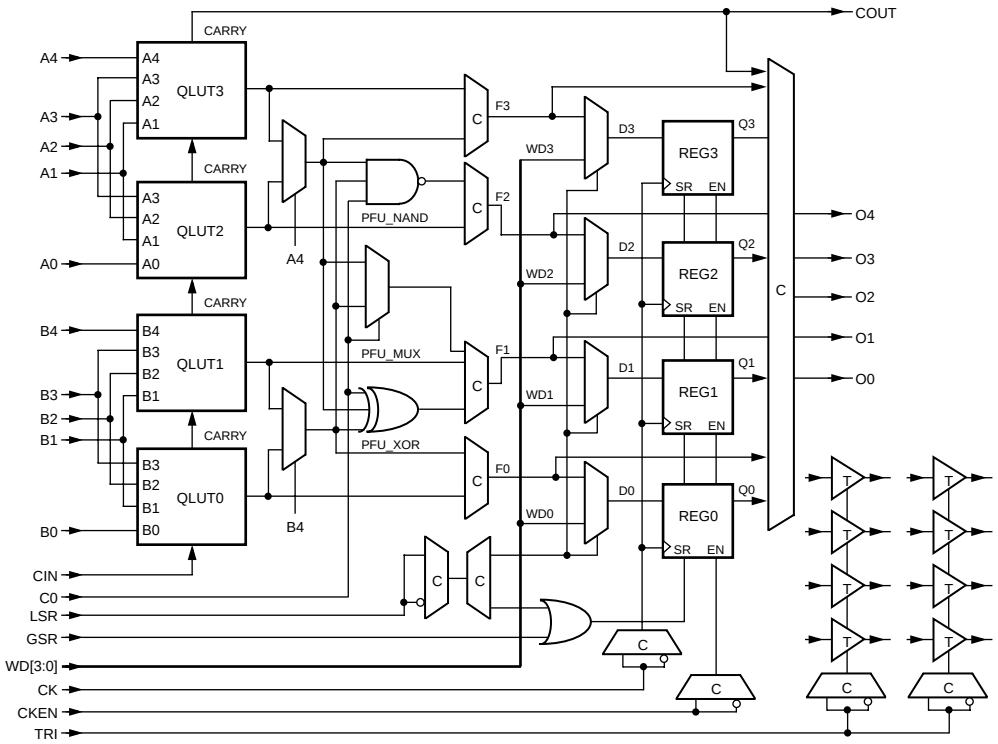

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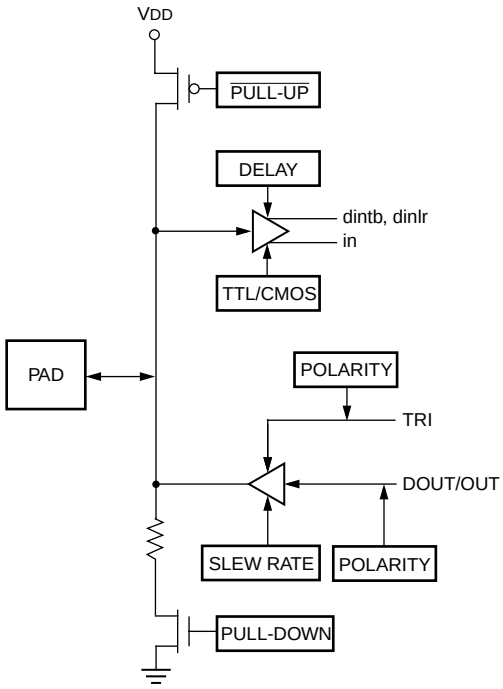
Figure 1. PFU Block Diagram

Description (continued)



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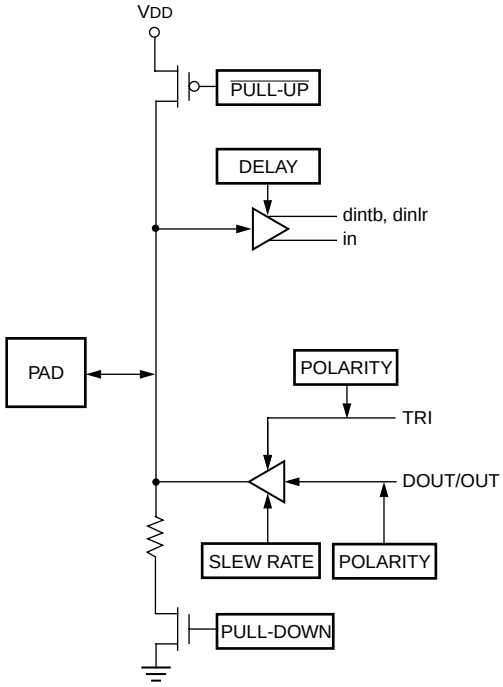
A. Simplified Diagram of OR2CxxA Programmable I/O Cell



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B. Simplified Diagram of OR2TxxA/OR2TxxB Programmable I/O Cell

Figure 2. Series 2 Diagrams

Description (continued)

The *ORCA* Foundry Development System is used to process a design from a netlist to a configured FPGA. This system is used to map your design onto the *ORCA* architecture and then place and route it using *ORCA* Foundry's timing-driven tools. The development system also includes interfaces and libraries to popular CAE tools for design entry, synthesis, and simulation. Some examples of the resources required and the performance that can be achieved using these devices are represented in Table 2.

The FPGA's functionalitiy is determined by internal configuration RAM. The FPGA's internal initialization/configuration circuitry loads the configuration data at powerup or under system control. The RAM is loaded by using one of several configuration modes. The configuration data resides externally in an EEPROM, EPROM, or ROM on the circuit board, or any other storage media. Serial ROMs provide a simple, low pin count method for configuring FPGAs, while the peripheral and JTAG configuration modes allow for easy, in-system programming (ISP).

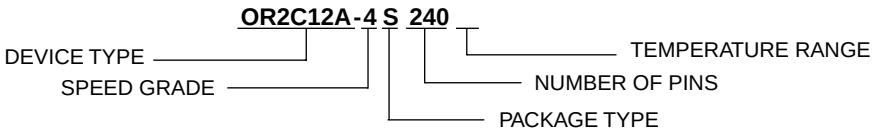
Table 2. *ORCA* Series 2 System Performance

Function	# PFUs	Speed Grade								Unit
		-2A	-3A	-4A	-5A	-6A	-7A	-7B	-8B	
16-bit Loadable Up/Down Counter	4	51.0	66.7	87.0	104.2	129.9	144.9	131.6	149.3	MHz
16-bit Accumulator	4	51.0	66.7	87.0	104.2	129.9	144.9	131.6	149.3	MHz
8 x 8 Parallel Multiplier:										
Multiplier Mode, Unpipelined[1]	22	14.2	19.3	25.1	31.0	36.0	40.3	37.7	44.8	MHz
ROM Mode, Unpipelined[2]	9	41.5	55.6	71.9	87.7	107.5	122.0	103.1	120.5	MHz
Multiplier Mode, Pipelined[3]	44	50.5	69.0	82.0	103.1	125.0	142.9	123.5	142.9	MHz
32 x 16 RAM (synchronous):										
Single Port (read and write/	9	21.8	28.6	36.2	45.5	53.8	62.5	57.5	69.4	MHz
cycle)[4]	9	38.2	52.6	69.0	86.2	92.6	96.2	97.7	112.4	MHz
Single Port[5]	16	38.2	52.6	83.3	90.9	92.6	96.2	97.7	112.4	MHz
Dual Port[6]										
36-bit Parity Check (internal)	4	13.9	11.0	9.1	7.4	5.6	5.2	6.1	5.1	ns
32-bit Address Decode (internal)	3.25	12.3	9.5	7.5	6.1	4.6	4.3	4.8	4.0	ns

1. Implemented using 4 x 1 multiplier mode (unpipelined), register-to-register, two 8-bit inputs, one 16-bit output.
2. Implemented using two 16 x 12 ROMs and one 12-bit adder, one 8-bit input, one fixed operand, one 16-bit output.
3. Implemented using 4 x 1 multiplier mode (fully pipelined), two 8-bit inputs, one 16-bit output (28 of 44 PFUs contain only pipelining registers).
4. Implemented using 16 x 4 synchronous single-port RAM mode allowing both read and write per clock cycle, including write/read address multiplexer.
5. Implemented using 16 x 4 synchronous single-port RAM mode allowing either read or write per clock cycle, including write/read address multiplexer.
6. Implemented using 16 x 2 synchronous dual-port RAM mode.
7. OR2TxxB available in -7 and -8 speeds only.

Ordering Information

Example:



OR2C12A, -4 speed grade, 240-pin shrink quad flat pack, commercial temperature.

Table 3. FPGA Voltage Options

Device	Voltage
OR2CxxA	5.0 V
OR2TxxA	3.3 V
OR2TxxB	3.3 V

Table 4. FPGA Temperature Options

Symbol	Description	Temperature
(Blank)	Commercial	0 °C to 70 °C
I	Industrial	–40 °C to +85 °C

Table 5. FPGA Package Options

Symbol	Description
BA	Plastic Ball Grid Array (PBGA)
BC	Enhanced Ball Grid Array (EBGA)
J	Quad Flat Package (QFP)
M	Plastic Leaded Chip Carrier (PLCC)
PS	Power Quad Shrink Flat Package (SQFP2)
S	Shrink Quad Flat Package (SQFP)
T	Thin Quad Flat Package (TQFP)

Ordering Information (continued)

Table 6. *ORCA* OR2CxxA/OR2TxxA Series Package Matrix

Packages	84-Pin PLCC	100-Pin TQFP	144-Pin TQFP	160-Pin QFP	208-Pin EIAJ SQFP/ SQFP2	240-Pin EIAJ SQFP/ SQFP2	256-Pin PBGA	304-Pin EIAJ SQFP/ SQFP2	352-Pin PBGA	432-Pin EBGA
	M84	T100	T144	J160	S208/ PS208	S240/ PS240	BA256	S304/ PS304	BA352	BC432
OR2C/2T04A	CI	CI	CI	CI	CI	—	—	—	—	—
OR2C/2T06A	CI	CI	CI	CI	CI	CI	CI	—	—	—
OR2C/2T08A	CI	—	—	CI	CI	CI	CI	—	—	—
OR2C/2T10A	CI	—	—	CI	CI	CI	CI	—	CI	—
OR2C/2T12A	CI	—	—	—	CI	CI	CI	CI	CI	—
OR2C/2T15A	CI	—	—	—	CI	CI	CI	CI	CI	CI
OR2C/2T26A	—	—	—	—	CI	CI	—	CI	CI	CI
OR2C/2T40A	—	—	—	—	CI	CI	—	CI	CI	CI

Key: C = commercial, I = industrial.

Table 7. *ORCA* OR2TxxB Series Package Matrix

Packages	84-Pin PLCC	100-Pin TQFP	144-Pin TQFP	160-Pin QFP	208-Pin EIAJ SQFP/ SQFP2	240-Pin EIAJ SQFP/ SQFP2	256-Pin PBGA	304-Pin EIAJ SQFP/ SQFP2	352-Pin PBGA	432-Pin EBGA
	M84	T100	T144	J160	S208/ PS208	S240/ PS240	BA256	S304/ PS304	BA352	BC432
OR2T15B	—	—	—	—	CI	CI	CI	—	CI	—
OR2T40B	—	—	—	—	CI	CI	—	—	CI	CI

Key: C = commercial, I = industrial.

Notes:
The package options with the SQFP/SQFP2 designation in the table above use the SQFP package for all densities up to and including the OR2C/T15A/B, while the OR2C/T26A and the OR2C/2T40A/B use the SQFP2.

The OR2TxxA and OR2TxxB series is not offered in the 304-pin SQFP/SQFP2 packages.

The OR2C40A is not offered in a 352-pin PBGA.

January 2002
PN99-072FPGA (Replaces PN98-018FPGA)

Lattice Semiconductor Corporation