February 2003

PNI Corporation

PNI-11096

3 – Axis Magneto-Inductive Sensor Driver and Controller with SPI Serial Interface

General Description

The PNI-11096 is a low cost magnetic measurement Application Specific Integrated Circuit (ASIC) designed for use with PNI Corp's magneto-inductive sensors. The PNI-11096 can control and measure three independent magneto-inductive sensors. Each sensor is individually selectable for measurement, and can also be individually configured for measurement resolution. The PNI-11096 communicates through an SPI port, effectively creating a 3 - axis magnetometer that can be easily connected to most all microprocessors. In addition, the PNI-11096 has diagnostic modes and outputs to test the oscillator and counter circuits.

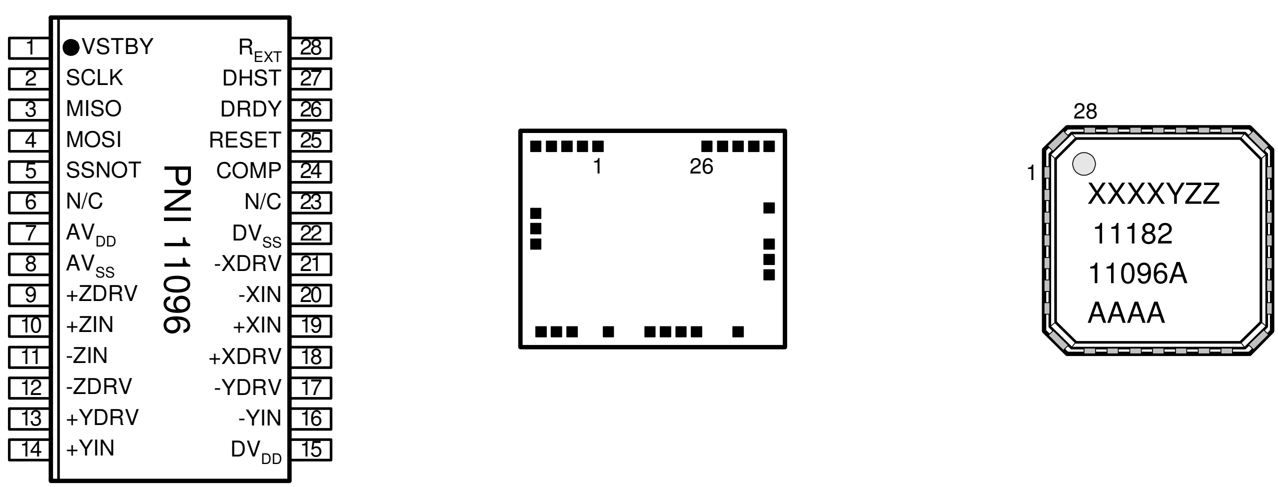
The PNI-11096 contains the entire measurement circuit—both analog and digital sections. The sensors change inductance with an applied change in magnetic field parallel to the sensor. In order to make a measurement, the sensor is switched into an LR oscillator circuit. The bipolar differential measurement scheme used by the PNI-11096 makes the magnetic measurement inherently temperature independent. It also has the benefit of transforming the measurement range into a zero centered, positive/negative value.

Features

- o Complete 3-axis magnetic sensor measurement system on a single chip
- o DIE form has ultra low magnetic signature
- o Low voltage Supply
- o Low supply current
  - 1.5mA - conversion rate
  - <1uA - idle mode
- o Acquisition speeds up to 200samples/sec
- o 96dB dynamic range
- o SPI port select for port multiplexing

Applications

- Compassing
- Magnetometer instruments
- Magnetic object sensing
- Magnetic ink sensing



28 PIN SOIC 26 PAD DIE 28 PIN MLF

Pin Configuration

Absolute Maximum Rating

Symbol	Parameter	MIN	MAX	Units	Notes
V_{DD}	DC Suppy Voltage	-0.3	5.25	V	
V_{IN}	Input Pin Voltage	-0.3	VDD+0.3	V	
I_{IN}	Input Pin Current	-10.0	10.0	MA	25C
T_{strg}	Storage Temperature	-40	125	C	

Supply Operating Conditions

Symbol	Parameter	MIN	MAX	Units	Notes
V_{DD}	Digital DC Supply	2.2	5.0	V	
I_{DD}	On, RCOSC and LROSC Off		0.1	mA	Nominal
I_{DD}	On, RCOSC On, LROSC Off		.5	mA	Nominal
I_{DD}	On, RCOSC and LROSC On		1.5	mA	Nominal
ILkStby	I_{DD} @ VSTBY pin		100	nA	(1)
V_{SS}	Digital Ground	0.0	0.0	V	
Ta	Ambient Temperature	-20	70	C	

(1) VSTBY = 5.5V, AV_{DD}=DV_{DD}=AV_{SS}=DV_{SS}=0Volts, Temp=27C

Electrical Specifications

Parametric Voltage and Current Levels: Testing for the below currents assumes a static test setup with measurements performed while static data is applied to the device

Inputs

Test Type	Vil (18)	Vih (18)	Iil (9)		Iih (9)		Notes (10)
	V		Min uA	Max uA	Min uA	Max uA	
AIB	0.2	2.0	0.0	-1.0	0.0	1.0	Analog Input
IBA	0.25	0.8	0.0	-1.0	0.0	1.0	CMOS
IBT	0.2	0.8	0.0	-1.0	0.0	1.0	CMOS, SC Hsy = 1.0

(9) Iil and Iih are tested at VDD = 3.6 V. Not test at less than room temperature
(10) SC = Schmitt
(18) CMOS value are 'Vin * VDD'

Outputs

Test Type	Vol V	Voh V	Iol (14) mA Min	Ioh (14) mA Min	Notes
OB1	<0.4	>2.4	1.0	-1.0	V_{DD} = 4.5-5.0 Volts
OB2	<.4V	>2.4	1.0	-1.0	V_{DD} = 4.5-5.0 Volts
OB3	0.267	1.936	10.0	-10.0	V_{DD} = 2.2 Volts

(14) Polarity on currents indicated direction of current (+) for sinking (-) for sourcing

I/O Pins

Test Type	Vil (18) V	Vih (18) V	Vol (16) V	Voh (16) V	Iol (16) mA	Ioh (16) uA	Ioz** (17) uA Min	Ioz** (17) uA Max	Notes
IO1A	.030	.070	0.40	4.1	-.640	.150	39	217	CMOS

(16) Vol, Voh, Iol Ioh are tested at Vdd = 4.8 Volts.
(17) Ioz is tested with V_{DD} = 5.2 Volts.
(18) CMOS values are 'Vin * V_{DD}"
** Leakage on IO pins is typically checked for +/- 10uA with the output device turned off and no PU or PD

Pin Definition

Pin Number 28 SOIC	26 DIE	28 MLF	Pin Name	I/O Type (1)	Test Type Para-meters	Description	Notes
1	1	26	VSTBY	DP	V_{DD}	Input protection clamp diode common	Connect to VDD
2	2	27	SCLK	DI	IBT	Serial Clock input for SPI port	1Mhz Max (Rext=100K)
3	3	28	MISO	DO	OB2	Serial data output (Master In Slave Out)	
4	4	1	MOSI	DI	IBA	Serial data input (Master Out Slave In)	
5	5	3	SSNOT	DI	IBA	Active low Chip select for SPI port	
6		2	N/C			NOT CONNECTED	
7	6	4	AV_{DD}	AP	V_{DD}	Supply Voltage for analog section	
8	7	5	AV_{SS}	AP	V_{SS}	Ground pin for Analog section	
9	8	6	+ZDRV	DO	OB3	Z sensor drive output	
10	9	7	+ZIN	AI	AIB	Z sensor sense input	
11	10	8	-ZIN	AI	AIB	Z sensor sense input	
12	11	9	-ZDRV	DO	OB3	Z sensor drive output	
13	12	10	+YDRV	DO	OB3	Y sensor drive output	
14	13	11	+YIN	AI	AIB	Y sensor sense input	
15	14	12	DV_{DD}	DP	V_{DD}	Supply Voltage for digital section	
16	15	13	-YIN	AI	AIB	Y sensor sense input	
17	16	14	-YDRV	DO	OB3	Y sensor drive output	
18	17	15	+XDRV	DO	OB3	X sensor drive output	
19	18	16	+XIN	AI	AIB	X sensor sense input	
20	19	17	-XIN	AI	AIB	X sensor sense input	
21	20	18	-XDRV	DO	OB3	X sensor drive output	
22	21	19	DV_{SS}	DP	V_{SS}	Ground pin for digital section	
23		20	N/C			NOT CONNECTED	
24	22	21	COMP	DO	OB1	Comparator output	Used for diagnostics
25	23	22	RESET	DI	IBA	Reset Input	
26	24	23	DRDY	DO	OB1	Data Ready	
27	25	24	DHST	DIO	IO1A	High speed oscillator output (Output is ½ clock speed)	Used for diagnostics
28	26	25	REXT	AI	AIB	External timing resistor for high speed clock	100K Ohm Typical

(1) I/O types: D = Digital, A = Analog, I = Input, O = Output, IO = Bidirectional, P = Power pad

Operation

The PNI-11096 contains the entire measurement circuitry necessary to use PNI Corp's magneto-inductive sensors. The sensors change inductance with a change in magnetic field parallel to the sensor. To make a measurement, the sensor is switched into an LR oscillator circuit. One side of the sensor is grounded; the other side is alternately charged and discharged through the oscillator circuit ("forward bias"). The PNI-11096 will measure the amount of time it takes to make a certain number of oscillations. The PNI-11096 will then switch the bias connections to the sensor, and make another measurement. The side that was previously grounded is now charged and discharged; the other side is now ground ("reverse bias").

Figure 1 illustrates the change between these two measurements. The actual magnetic measurement is the difference between these two measurements. This measurement scheme is used to make the magnetic measurement temperature independent. It also has the benefit of transforming the measurement range into a zero centered, positive/negative value.

The PNI-11096 returns the data to the host microprocessor over the SPI interface. The microprocessor simply asks the PNI-11096 for data from a specific axis, and the PNI-11096 does the rest.

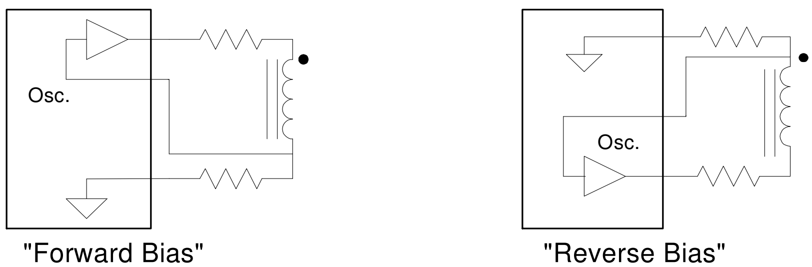


Figure 1. Forward Bias vs. Reverse Bias.

1. Connections

A typical connection configuration is shown in Figure 2. The PNI-11096 can control up to 3 sensors; if less are needed, the unneeded pins should be left to float.

Vstby pin must always be equal to or higher than any voltage present on any other pin on the PNI-11096. Vstby is connected to the cathode end of a diode array. The anode end of each diode in the array is connected to each of the digital interface signal pins. Leaving Vstby floating or connected to ground when other pins are potentially active, as in a multiplexed SPI network, will cause excessive current drain.

**** Rb value sufficient for evaluation:***

5VDC – 150 Ohm for SEN-L
56 Ohm for SEN-S

3VDC – 150 Ohm for SEN-L
33 Ohm for SEN-S

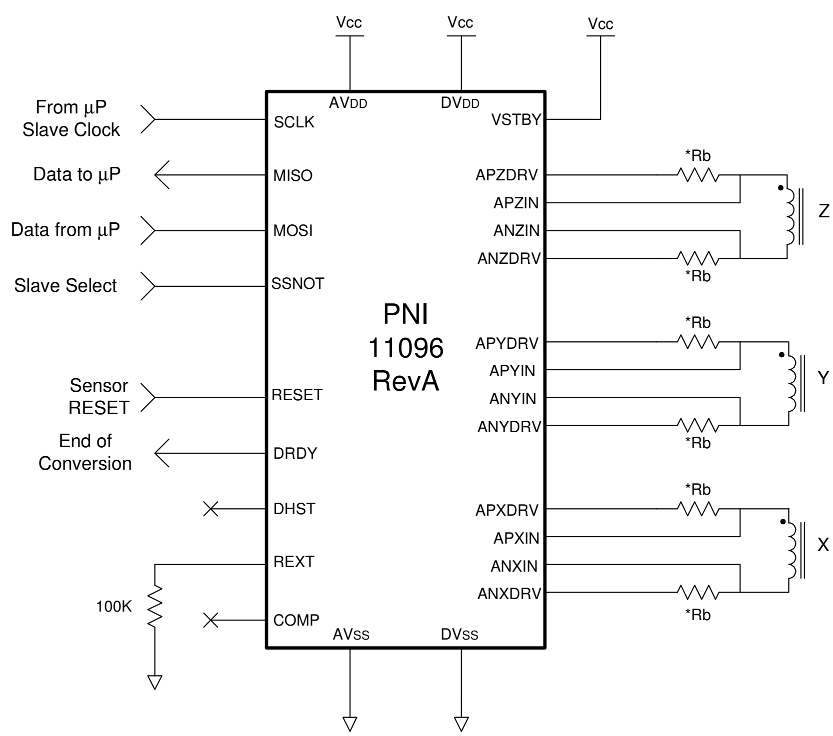


Figure 2 Typical Connection

2. Magnetic Measurements

The magnetic sensor operates in an oscillator circuit composed of the external sensors and external bias resistors along with digital gates and a comparator internal to the PNI-11096. Only one sensor can be measured at a time. The user sends a command byte to the PNI-11096 through the SPI port specifying the sensor axis to be measured. The PNI-11096 will return the result of a complete forward - reverse measurement of the sensor in a16-bit 2's Complement format.
(Range: -32768 to 32767)

2.1 Command Byte

The operation of the PNI-11096 is controlled by the data received into the SPI port. The command byte syntax is as follows:

Position	7	6	5	4	3	2	1	0
BIT	DHST	PS2	PS1	PS0	ODIR	MOT	AS1	AS0
RESET	0	0	0	0	0	0	0	0

2.1.1 AS0, AS1 Axis Select

The Axis select bits determine which axis is being measured.

Function	AS1	AS0
2 MHz Scaling	0	0
X axis	0	1
Y axis	1	0
Z axis	1	1

Note: When 2 MHz Scaling is selected, the magnetic sensor oscillator does not run. Instead, the internal 2 MHz oscillator is turned on. The 2 MHz clock cycles are counted until a command byte is sent disabling the scaling function. A reset stops the 2 MHz oscillator and clears all bits

2.1.2 MOT Magnetic Oscillator Test

When set, this bit causes the magnetic oscillator selected by AS0 and AS1 in the directions selected by ODIR to run continuously until PNI-11096 is reset, or a command byte is received to disable the test function. The MOT bit when set also enables the mag oscillator frequency to the Comp test pad.

2.1.3 ODIR Oscillator Direction

This bit determines the magnetic oscillator direction if MOT is set to 1. It has no effect on direction when the MOT bit is set to zero. This is used for debug purposes only, and will not be set in normal operation.

2.1.4 PS0, PS1, PS2 Period Select

These bits select the division ratio applied to the L/R oscillator output to set the period being measured.

PS2	PS1	PS0	Ratio
0	0	0	/32
0	0	1	/64
0	1	0	/128
0	1	1	/256
1	0	0	/512
1	0	1	/1024
1	1	0	/2048
1	1	1	/4096

2.1.5 DHST High Speed Oscillator Test

When this bit is set, the internal high speed clock is set to drive the DHST pad at ½ the clock speed. When this bit is 0, the DHST pad is set to DVDD.

2.2 SPI Port

All accesses to and from the PNI-11096 are through a synchronous serial port that adheres to the Motorola SPI protocol. The port consists of four signals; SCLK, MOSI, MISO and SSNOT.

2.2.1 SCLK Serial Clock

The serial clock (SCLK) is used to synchronize both the data in and out through the MISO and MOSI lines. SCLK is generated by a master device. SCLK should be 1 MHz or less. The PNI-11096 is configured to run as a slave device, so this is an input. One byte of data is exchanged over eight clock cycles. Data is captured by the master device on the rising edge of SCLK. Data is shifted out and presented to the PNI-11096 on the MOSI pin on the falling edge of SCLK.

2.2.2 SSNOT Slave Select

The slave select line (SSNOT) selects the PNI-11096 as the operating slave device. The SSNOT line must be low prior to data transfer and must stay low during the entire transfer. Once the command byte is received by the PNI-11096, and the PNI-11096 begins to execute the command, the SSNOT line can be deselected until the next SPI transfer.

2.2.3 MOSI Master Out, Slave In

The master out, slave in (MOSI) line is the data sent to the PNI-11096. Data is transferred most significant bit first. The MOSI line will accept data once the SPI is enabled by taking SSNOT low. Valid data must be presented at least 100 ns before the rising edge of the clock, and remain valid for 100 ns after the edge. New data may be presented to the MOSI pin on the falling edge of SCLK.

2.2.4 MISO Master In, Slave Out

The master in, slave out (MISO) line is the data sent from the PNI-11096 to the master. Data is transferred most significant bit first. The MISO line is placed in a high impedance state if the salve is not selected (SSNOT=1).

2.3 Operation

Basic operation will follow these steps.
(Reference Figures 3 and 4)

1. SSNOT is brought low.
2. Pulse RESET high (return to low state). You must RESET the PNI-11096 before every measurement.
3. Data is clocked in on the MOSI line. Once eight bits are read in, the PNI-11096 will execute the command.
4. The PNI-11096 will make the measurement. A measurement consists of forward biasing the sensor and making a period count; then reverse biasing the sensor and counting again; and finally, taking the difference between the two bias directions.
5. At the end of the measurement, the DRDY line is asserted to alert you that the data is ready. In response to the next 16 SCLK pulses, data is shift out on the MISO line.

If you need to make another measurement, go to step 2. You can send another command after the reset. In this case, keep SSNOT low. If you will not be using the PNI-11096, bring SSNOT high to disable the SPI port.

2.4 Pin Descriptions

SCLK -- serial clock for SPI port
MISO -- master in, slave out for SPI port
MOSI -- master out, slave in for SPI port
SSNOT -- slave select for SPI port. SSNOT must be low to select PNI-11096 for operation.
RESET -- PNI-11096 reset. You must toggle RESET low after every PNI-11096 command has been executed to enable next command.
DRDY -- Data ready. This pin is asserted after a measurement to signal that data is ready to clock out.

3. Application notes

3.1 Idle mode

The PNI-11096 does not initialize in the idle mode at power-up. The PNI-11096 must be in a data-ready state for the idle mode to occur. After power-up the PNI-11096 can be brought to the data-ready state simply by sending a read command to the PNI-11096. First bring SSNOT low, pulse the reset line and then send a command to the PNI-11096 to measure one of the sensors. The DRDY pin will eventually go high signifying that the PNI-11096 is in the data-ready state. The resultant data does not have to be read from the PNI-11096. Once the SSNOT pin is brought high again the PNI-11096 will go into the low power idle mode.

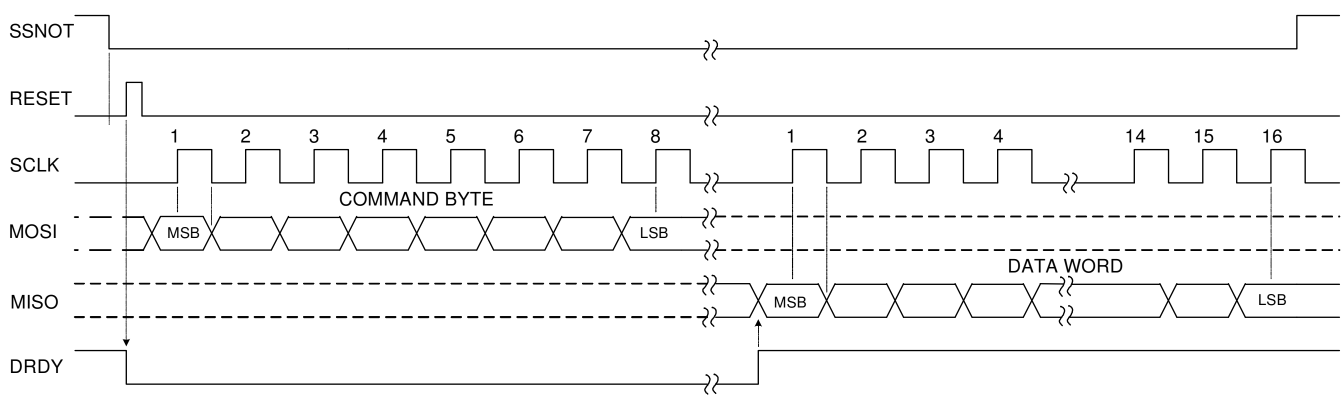


Figure 3
SPI Port Full Timing Sequence (cpol = 0)

3.2 SPI port usage tips

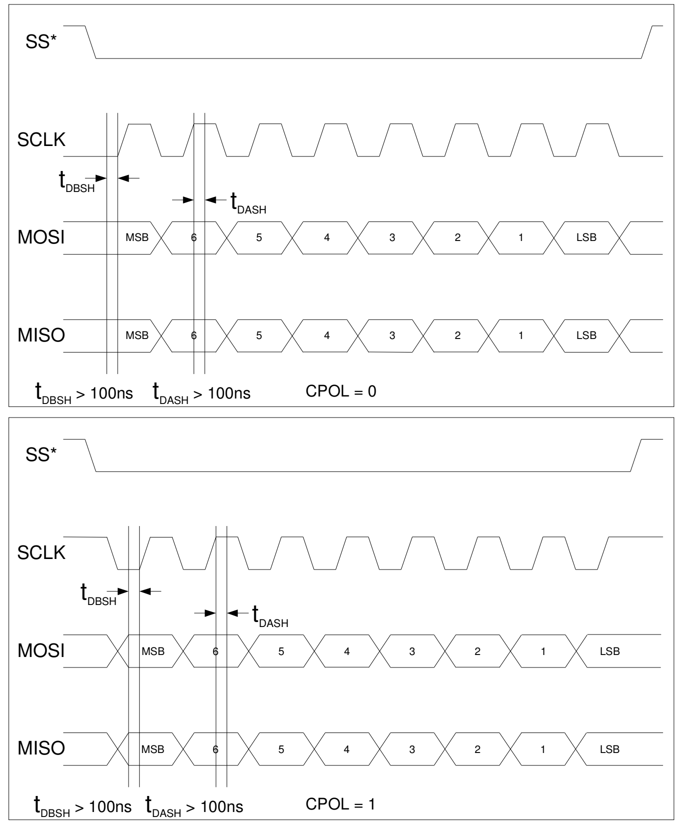
A SPI port can be implemented using different clock polarity options. The clock can be normally low (cpol = 0) or normally high (cpol = 1). Figure 4 graphically shows the timing sequence of the two clock polarity options when used to communicate with the PNI-11096. Regardless of the polarity chosen, data is always read in (into the PNI-11096) on the rising edge of the clock and sent out on the falling edge of the clock.

When implementing an SPI port, whether it be a dedicated hardware peripheral port, or a software implemented port using general purpose I/O (also known as *Bit-Banging*) the timing parameters given in Figure 4 must be met to ensure reliable communications. The clock set-up and hold times as depicted as t_{DBSH} and t_{DASH} (Time, Data Before SCLK High and Time, Data After SCLK High) must be greater than 100nS.

3.3 Sample Rates

Approximate sample rate limits for sampling 2 sensors based on Period Select settings are as follows:

Period Select	Max Samples per second
64	200
128	140
256	72
512	36



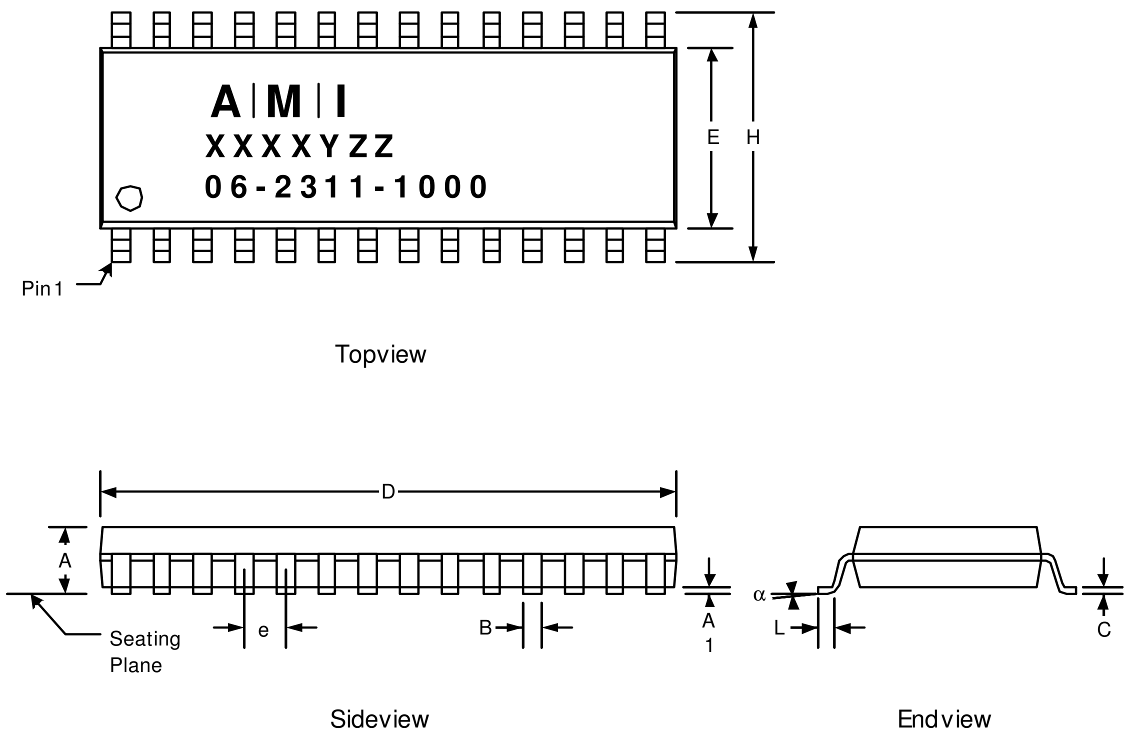
NOTE: DBSH = Data Before SCLK High DASH = Data After SCLK High

Figure 4
SPI Port timing parameters (cpol = 1 & cpol = 0)

Package Information

28 Pin SOIC Outline Dimensions

(Unit : mm)



SYMBOL	MIN	NOM	MAX
A	2.35	-	2.65
A1	0.10	-	0.30
B	0.33	-	0.51
C	0.23	-	0.32
D	17.70	-	18.10
E	7.40	-	7.60
e	1.27BSC		
H	10.00	-	10.65
L	0.40	-	1.27
α	0		8

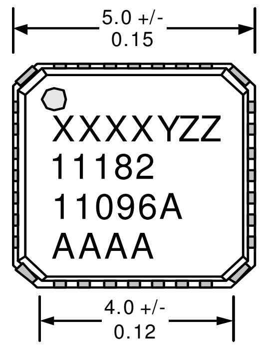
Markings

XXXX : Data Code
Y : Assembly Plant identifier
ZZ: Traceability Code
06-2311-1000 : PNI Part No. (can be use with PNI's alternate P/N:10175)

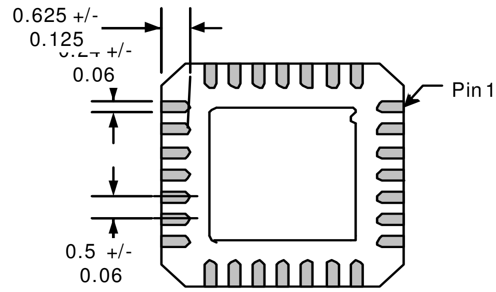
Package Information (continued)

28 Lead MLF(5x5mm) Outline dimensions

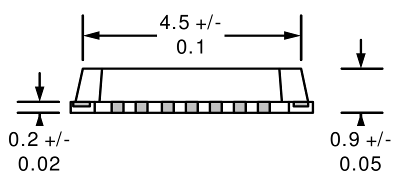
(Unit : mm)



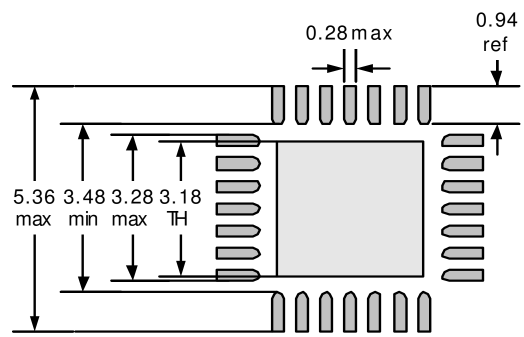
Topview



Bottom view



Sideview



PCB Land pattern

Markings

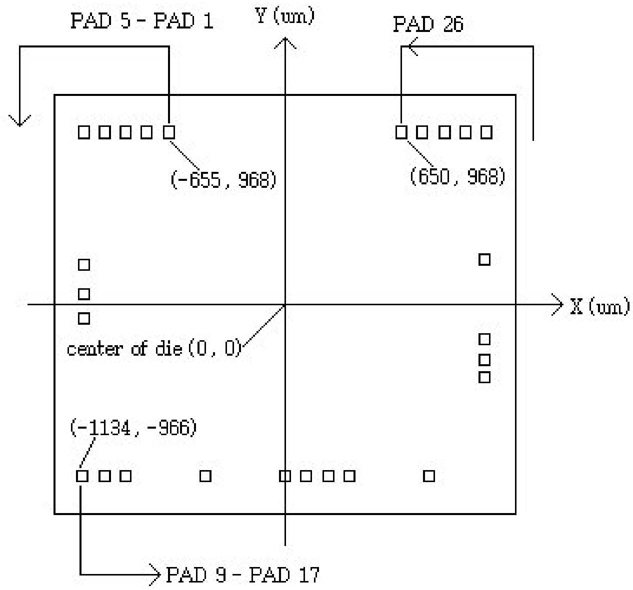
XXXX : Data Code
Y : Assembly Plant identifier
ZZ : Traceability Code
11182 : PNI Part No.
11096A : Revision No.
AAAA : Country of Assembly

Package materials

Lead Frame : C194H
Mold compound : 7351UL
Solderplating : 85/15 Sn/Pb
Marking : Laser

Package Information (continued)

Die Package Mechanical Specifications:



Remark : substrate floating

Die size is 2580 um X 2360 um (with scribe line).
Pad coordinates:
All X and Y coordinates refer to the center of the die.

PAD #	PAD NAME	X (um)	Y (um)
PAD 1	VSTBY	-655	968
PAD 2	SCLK	-755	968
PAD 3	MISO	-893	968
PAD 4	MOSI	-1012	968
PAD 5	SSNOT	-1128	968
PAD 6	AVDD	-1125	226
PAD 7	AVSS	-1125	62
PAD 8	APZDRV	-1125	-81
PAD 9	APZIN	-1134	-966
PAD 10	ANZIN	-1012	-966
PAD 11	ANZDRV	-893	-966
PAD 12	APYDRV	-448	-966
PAD 13	APYIN	-3	-966
PAD 14	DVDD	115	-966
PAD 15	ANYIN	237	-966
PAD 16	ANYDRV	357	-966
PAD 17	APXDRV	802	-966
PAD 18	APXIN	1118	-403
PAD 19	ANXIN	1118	-312
PAD 20	ANXDRV	1118	-189
PAD 21	DVSS	1118	225
PAD 22	COMP	1126	968
PAD 23	RESET	1008	968
PAD 24	DRDY	887	968
PAD 25	DHST	768	968
PAD 26	REXT	650	968

PNI part number index

PNI part number	Description
10174	26 pad Die
10175	28 pin SOIC
11182	28 pin MLF

PNI Sales information

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