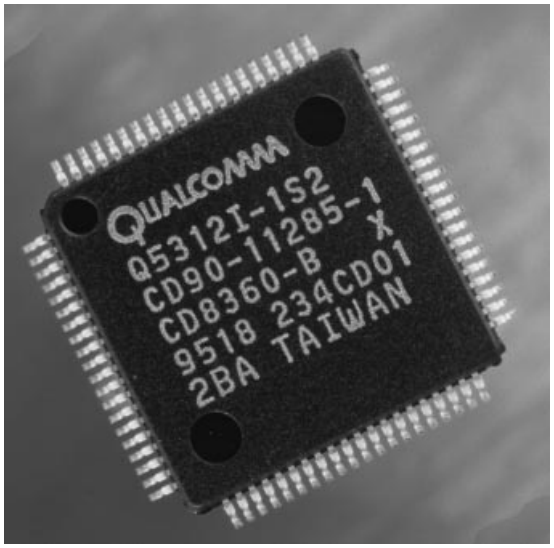
Q5312

ANALOG BASEBAND PROCESSOR BBA2



OVERVIEW

APPLICATION DESCRIPTION

The QUALCOMM Analog Baseband Processor (BBA2), also known as Q5312, is designed for use in dual-mode Code Division Multiple Access (CDMA) and FM portable cellular telephones. The BBA2 interfaces between the RF and the digital processing circuitry of the telephone. The BBA2 receive path circuitry converts analog IF (intermediate frequency) signals to the baseband frequency range, then converts the analog baseband signals into digital signals. The transmit path circuitry converts digital data into analog baseband signals which are then up-converted to the IF frequency range.

The BBA2 includes receive and transmit Voltage Controlled Oscillators (VCOs) and other clock synthesis and processing circuits. There is also a general purpose Analog-to-Digital Converter (ADC) included for battery and signal strength monitoring. The BBA2 is designed to interface directly with QUALCOMM's Mobile Station Modem (MSM) family of devices. The MSM is a CMOS VLSI Application Specific Integrated Circuit (ASIC) that performs all of the digital processing in the telephone. The MSM along with the BBA2 form the core of the portable CDMA/FM cellular telephone.

The BBA2 is fabricated on an advanced Bi-CMOS process which accommodates both precision analog circuitry and low-power CMOS functions. The device has been designed to operate from nominal power supply voltage of 3.3 V, with power control logic keeping power consumption to a minimum. Electrical performance parameters are guaranteed over a –30°C to 85°C range.

The BBA2 is packaged in an 80-lead Thin Plastic Quad Flat Pack (TQFP) package. With a lead pitch of 0.51 mm and a total above board thickness of 1.7 mm, the BBA2 is designed for very dense mechanical assemblies.

FEATURES

- Dual–mode for CDMA and FM operation
- Receive signal path includes:
  - IF-to-baseband down-conversion
  - Separate CDMA and FM filters and ADCs
  - Conversion of analog baseband to digital format
  - CDMA sampling clock synthesizer
  - Rx IF VCO for I-Q mixer
  - Offset control loop
- Transmit signal path includes:
  - Conversion of digital I-Q data to analog baseband signals
  - Separate CDMA and FM filters and DACs
  - Baseband-to-IF up-conversion
  - Tx IF VCO and PLL for I-Q mixer
- Mode Control Logic for RXTX, SLEEP, and IDLE modes
- General purpose ADC for system monitoring
- Low power consumption in all modes

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DEVICE APPLICATION

The BBA2 bridges the gap between the analog RF processing and digital processing sections of the cellular telephone. Figure 1 shows the general circuit blocks in the portable cellular telephone employing BBA2 and MSM.

The analog inputs and outputs of BBA2 interface directly with the IF transmit/receive circuitry of the telephone. The digital inputs and outputs of BBA2 interface directly with the MSM.

The RF receive circuitry acquires the low-level forward-link signal from the base station (cell site) and down-converts the signal to the IF frequency band. The RF transmit circuitry takes CDMA or FM modulated analog IF from BBA2, up-converts the IF signal to the channel frequency and outputs controlled reverse-link power levels to the antenna.

The MSM performs all digital signal processing in the CDMA/FM cellular telephone. It includes digital processors for CDMA modulation/demodulation, digital FM modulation/demodulation, voice processing and a keypad interface. The CODEC (coder-decoder) block interfaces the telephone microphone and earpiece to the MSM. The MSM also has direct connections to the RF/IF section of the telephone for AGC (automatic gain control) and calibration of the RF signal paths for receive and transmit.

The BBA2 receive signal path down-converts the acquired IF signal to baseband where it is then converted to digital data. The digital baseband signals are sent to the MSM for demodulation. When transmitting, the MSM sends modulated digital baseband signals to the BBA2 for up-conversion to the analog IF frequency.

GENERAL DESCRIPTION

The BBA2 consists of a receive signal path, a transmit signal path, clock synthesis and buffering circuits, mode control logic, and a general purpose ADC. The transmit and receive signal paths are shown in Figure 2.

Figure 1. Dual-Mode CDMA/FM Cellular Telephone Block Diagram

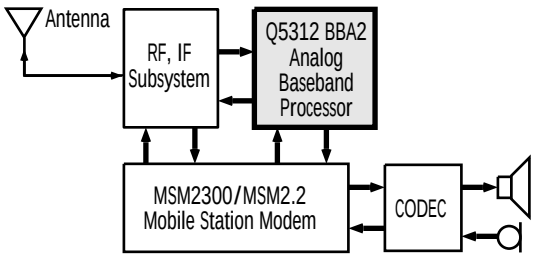
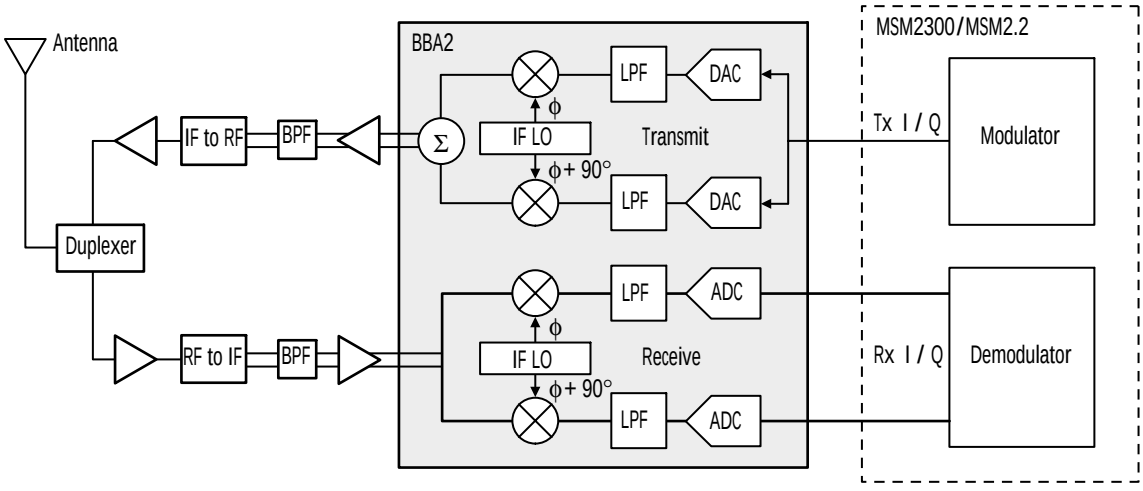


Figure 2. BBA2 Block Diagram



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CDMA RECEIVE SIGNAL PATH

The receive signal path shown in Figure 3 is designed to accept a differential IF signal with CDMA spread spectrum modulation extending ±630 kHz from the IF center frequency of 85.38 MHz. This IF center frequency is not fixed by the BBA2, but is set by external components chosen by the designer. The incoming IF is demodulated to I and Q baseband components by mixing with 85.38 MHz Local Oscillator (LO) signals in quadrature followed by low-pass filtering.

The 85.38 MHz I and Q LO signals are generated on the BBA2 device. The receive VCO is set to 170.76 MHz by an external varactor-tuned resonant tank circuit (inductor L and capacitor C connected in parallel). An external phase-lock loop and loop filter network provide feedback to varactors that tune the VCO to 170.76 MHz. A master-slave divide-by-two circuit generates I and Q signals in precise quadrature for the mixers.

CDMA LOW-PASS FILTERING

After mixing, the receive signal path splits into CDMA and FM sections. For CDMA, the baseband signal extends from 1 kHz to 630 kHz. Frequency components above 750 kHz are out-of-band for CDMA operation. The mixers and the subsequent CDMA low-pass filters combine to form the down-converter which outputs the CDMA baseband signals. The passband, transition band and rejection band characteristics of these low-pass filters, along with external IF bandpass filtering, enable the receiver to select the desired baseband signals from the jamming effects of unwanted signals.

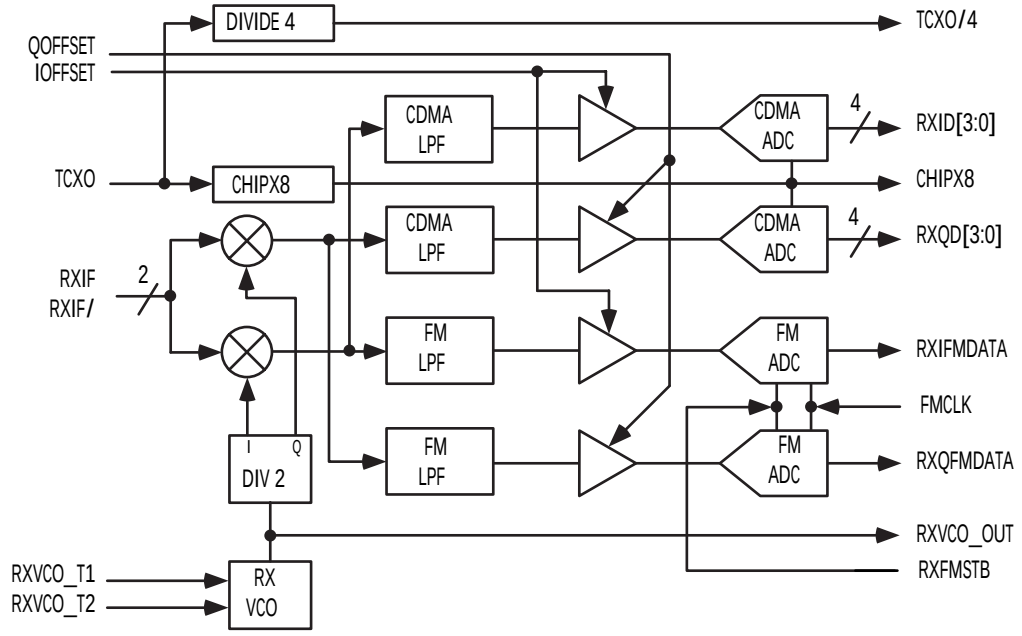
Controlling the offset at the inputs of the ADCs is critical to the receive signal path and MSM digital signal processing. The offset control inputs are provided for this purpose. These inputs are normally driven (through long time-constant RC filters) by the MSM which senses the offset of the digital baseband data and creates a Pulse Density Modulated (PDM) signal for compensation.

CDMA ANALOG-TO-DIGITAL CONVERSION

Analog I and Q baseband components are converted to digital signals by the two identical 4-bit flash (parallel) ADCs. The CDMA ADCs output a new digital value on each rising edge of the ADC clock signal, CHIPX8.

The CHIPX8 ADC clock frequency of 9.8304 MHz is synthesized from the system crystal oscillator frequency of 19.68 MHz. The system crystal oscillator frequency is applied to the TCXO input of BBA2.

Figure 3. BBA2 Receive Section Block Diagram



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FM RECEIVE SIGNAL PATH

The receive signal path for FM operation is similar to that for CDMA operation. There are differences in the characteristics of the I and Q low-pass filters and the ADCs. The IF frequency is the same as in CDMA (85.38 MHz), but the modulation can only extend ±15 kHz from the IF center frequency to form a 30 kHz wide channel. The low-pass filters for FM operation have a much lower bandwidth than those used in CDMA. The offset of the FM low-pass filters is controlled just like the CDMA low-pass filters by the offset control input pins.

The lower bandwidth of the FM baseband signal allows very low power 8-bit ADCs to be used. The FM I and Q analog baseband signals are sampled and held during the analog-to-digital (A/D) conversion process. The A/D conversion is initiated with a strobe from the MSM. A serial data stream is output beginning with the Most Significant Bit (MSB) of the result.

CDMA TRANSMIT SIGNAL PATH

The BBA2 transmit signal path (shown in Figure 4) accepts digital I and Q baseband data from the MSM, and outputs modulated IF centered at 130.38 MHz to the RF transmitter.

CDMA DIGITAL-TO-ANALOG CONVERSION AND FILTERS

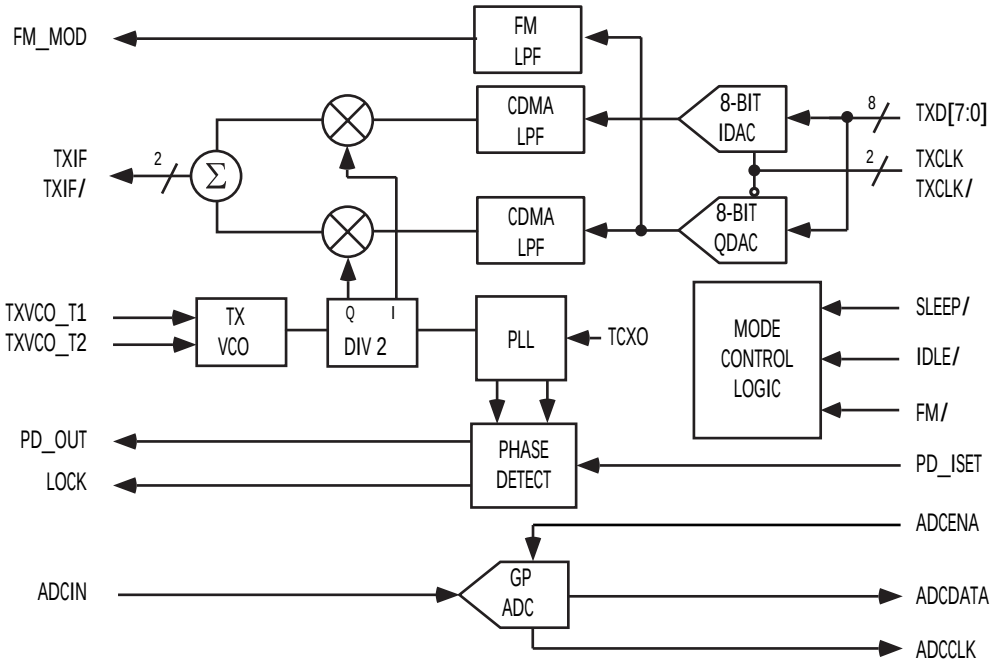
Eight bits of I and Q transmit data are multiplexed over an 8-bit input port into the BBA2 CDMA DACs. The transmit data rate is twice as fast as the differential transmit clock, TXCLK and TXCLK/. Incoming data that is valid during the rising edge of the transmit clock is registered into the I DAC. Incoming data that is valid during the falling edge of the transmit clock is registered into the Q DAC. I and Q transmit data values have been compensated in the MSM to account for their ½ clock cycle time difference.

The frequency spectrum at the output of the CDMA DACs contains unwanted frequency components due to DAC output transition edges and transients. The transmit clock frequency and harmonics are found in the spectrum and are also undesirable. Each CDMA DAC is followed by an anti-aliasing low-pass filter with a bandwidth of 630 kHz that reduces unwanted frequency components. Unlike the low-pass filters in the receive signal path, these low-pass filters do not require offset controls.

UP-CONVERTING TO IF

The BBA2 transmit path outputs a differential IF signal with CDMA spread spectrum modulation extending

Figure 4. BBA2 Transmit Section Block Diagram



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±630 kHz from the transmit IF center frequency of 130.38 MHz. The analog I and Q baseband components from the CDMA low-pass filters are mixed in quadrature with unmodulated I and Q signals at 130.38 MHz. After mixing, the I and Q IF components are summed and output differentially.

The 130.38 MHz I and Q LO signals are generated on the BBA2. The transmit VCO is set to 260.76 MHz by an external varactor-tuned resonant tank circuit. An internal phase-lock loop and external loop filter network provides the feedback to the varactors that tune the VCO precisely to 260.76 MHz. A master-slave divide-by-two circuit generates I and Q signals in precise quadrature for the mixers.

FM TRANSMIT SIGNAL PATH

An analog FM modulation signal is constructed from 8-bit digital data supplied by the MSM. Only the Q-channel DAC is used in the BBA2 in FM Mode. All other CDMA circuits are disabled. The DAC output is filtered by a low-pass anti-aliasing filter. The filtered DAC output is the analog FM modulation signal. This signal modulates the frequency of the BBA2 transmit VCO using external components when in FM RXTX Mode. The modulated VCO frequency is halved by divide-by-two circuitry and output on the transmit IF outputs.

OPERATING MODES

The telephone has several modes of operation that determine the circuit block activity level in the BBA2. The CDMA RXTX or FM RXTX Modes are in effect when the telephone is making a call. IDLE Mode is in effect when no call is in progress, but the telephone receiver is active (ready to answer a call). SLEEP Mode is a low-power mode in which the telephone cannot receive a call but where the digital processor and keypad are still enabled.

The telephone has an additional mode, called Slotted Paging Mode. When in this mode, the MSM toggles itself and the BBA2 between SLEEP and IDLE Modes using a programmable timing interval. This mode allows the telephone to be contacted by the base station without requiring the telephone to be continuously in IDLE Mode. Slotted Paging Mode consumes much less power than IDLE Mode.

The BBA2 operating modes are defined by the states of three digital inputs that come directly from the MSM. These logic signals minimize the power consumed by the BBA2 by disabling unused circuits. The selected circuits in BBA2 become active after the states of the operating mode controls are changed.

GENERAL PURPOSE ADC

The General Purpose (GP) ADC provides DC measurement capability to the telephone during all modes of operation. It is a low speed, 8-bit resolution, ADC. It is designed to digitize DC voltages applied to the ADC input pin from battery level, temperature and other low frequency control or monitoring sensors.

The ADC is in a power-down state during normal BBA2 operation. It is activated by a positive-going pulse on the ADC enable pin. When this input is driven high, the GP ADC powers up and begins a conversion. The DC voltage to be measured must be applied to the ADC input for the duration of the conversion. The ADC output is available from a serial digital interface. Each of the eight data bits is valid (MSB first) during the rising edge of the ADC clock output. When the Least Significant Bit (LSB) of the conversion has been clocked out, the conversion is complete and the ADC returns to a power down condition. The ADC clock and data outputs will be low before and after a conversion. Conversions can only be started when the ADC is inactive after a conversion has been completed. A rising edge of the ADC enable pin during a conversion will be ignored. ADC enable must be low and a conversion completed before a new conversion can be started.

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INPUT / OUTPUT SIGNALS

Figure 5 shows the functions provided by the BBA2's pins and the size of its 80-pin TQFP package. Table 1 provides descriptions of the pin functions.

Figure 5. Q5312 BBA2 Analog Baseband Processor Functional Diagram

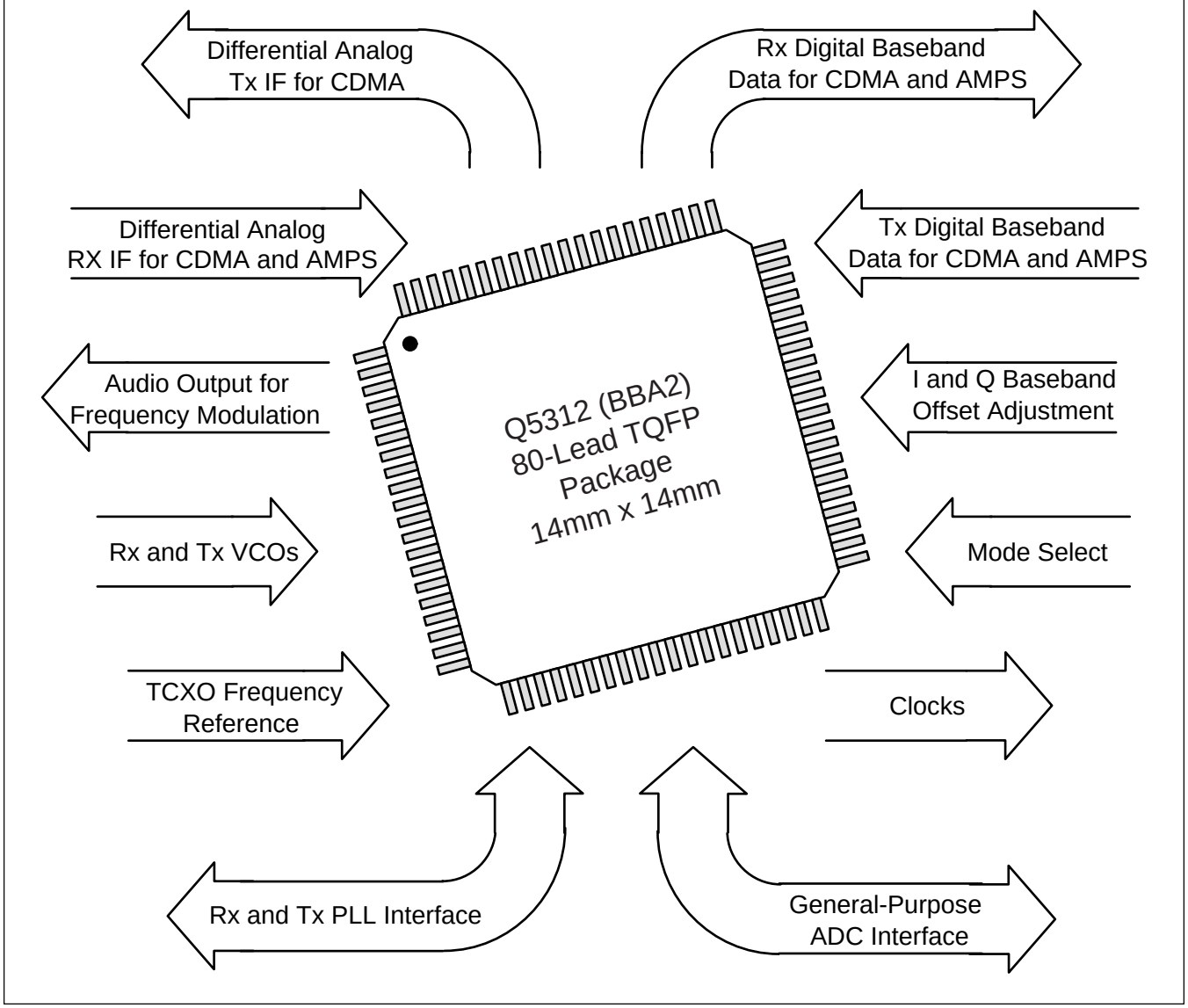

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Table 1. BBA2 Pin Functions

PIN FUNCTIONS	DESCRIPTION
Rx Digital Baseband Data for CDMA and AMPS	The BBA2 chip converts the receive IF signal from the RF subsystem of the subscriber unit to digital baseband data for both CDMA and AMPS.
Tx Digital Baseband Data for CDMA and AMPS	The MSM2300/MSM2.2 generates transmit digital baseband for the BBA2 chip. The BBA2 chip converts that data to an analog IF frequency of the subscriber unit.
I and Q Baseband Offset Adjustment	DC offsets in the receive signal path are removed by way of analog control signals from the MSM2300/MSM2.2. The MSM2300/MSM2.2 control signals use Pulse Density Modulation (PDM) which form DC control signals after being filtered with single-pole RC low-pass filters.
Mode Select	Digital controls from the MSM2300/MSM2.2 put the BBA2 into CDMA or FM Mode, IDLE (receive-only) Mode or SLEEP (minimum power consumption) Mode.
Clocks	The system frequency reference of 19.68 MHz is used to generate clocks for the MSM2300/MSM2.2. CHIPX8 (9.9304 MHz) and TCXO/4 a (4.92 MHz) are generated on the BBA2 chip.
General Purpose ADC Interface	The General-Purpose ADC is generally used for monitoring the subscriber unit battery voltage, RF power output level or temperature. The ADC interface is controlled by the MSM2300/MSM2.2.
Tx PLL Interface	The BBA2 includes a complete Transit Phase-Locked Loop for generating the TX IF frequency. The PLL includes a phase detector and requires a simple external loop filter.
Rx and Tx VCOs	The BBA2 chip includes all VCO circuits except the resonant tank. The VCOs operate differentially, reducing common mode noise and improving performance.
Audio Output for Frequency Modulation	In AMPS Mode, frequency-modulation is accomplished by a connection from the BBA2 to the varactor diodes of the transmit VCO.
Differential Analog Rx IF inputs and TXIF outputs	The receive IF inputs of the BBA2 are differential, improving performance and reducing cross-coupled noise.

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ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 2 shows the absolute maximim ratings of the Q5213 (BBA2). Operating the BBA2 under conditions that exceed those in the Absolute Maximum Ratings table may result in damage to the device. Absolute Maximum Ratings are limiting values, to be considered individually, while all the other parameters are within their specified operating ranges. Functional operation of the BBA2 under any of the conditions in the Absolute Maximum Rating table is not implied.

Table 2. Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNITS
V_{DD}, V_{DDD}	Power Supply Voltage	-0.5	+5.0	V
V_I	Voltage on any INPUT Pin	-0.5	V_{DD} + 0.5	V
V_{SC}	Short Circuit Duration, to GND or V_{DD}	–	1	sec
T_S	Storage Temperature	-55	+150	°C
I_{IN}	Current Into or Out of Any Pin	-200	+200	mA
T_L	Lead Soldering Temperature (10 sec Max.)	–	280	°C
V_{ESD}	ESD Voltage (each pin)	–	1500	V

RECOMMENDED OPERATING CONDITIONS

Table 3 shows the recommended operating conditions. Operating conditions include power supply voltage and ambient temperature parameters that are under the control of the user. The BBA2 meets all electrical, switching and system performance limits when operated in compliance with the recommended operating conditions.

Table 3. Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	MAX	UNITS
V_{DD}, V_{DDD}	Power Supply Voltage	3.13	3.47	V
T_A	Ambient Operating Temperature	-30	+85	°C

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ELECTRICAL CHARACTERISTICS

Table 4 shows the electrical characteristics. Electrical characteristics include both physical characteristics such as capacitance, resistance and impedance, and DC characteristics such as digital I/O levels, reference voltages and power supply current. In Table 4, values in the Typical column are based on a 25° C, 3.3 V power supply.

Table 4. Electrical Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
I_{DD1}	Power Supply Current. CDMA RXTX Mode.	–	53	75	mA
I_{DD2}	Power Supply Current. CDMA IDLE Mode.	–	31	38.1	mA
I_{DD3}	Power Supply Current. CDMA SLEEP Mode.	–	1.3	2.65	mA
I_{DD4}	Power Supply Current. FM RXTX Mode.	–	33	45	mA
I_{DD5}	Power Supply Current. FM IDLE Mode.	–	14	21	mA
V_{IH}	Logic High Input Voltage.	0.7 x V_{DD}	–	–	V
V_{IL}	Logic Low Input Voltage.	–	–	0.3 x V_{DD}	V
V_{OH}	Logic High Output Voltage. V_{DD} = 3.13 V. I_{OH} current = 300 µA. Larger current provided for digital output transactions.	2.7	–	–	V
V_{OL}	Logic Low Output Voltage. V_{DD} = 3.47 V. I_{OH} current = 100 µA. Larger current provided for digital output transactions.	–	–	0.4	V
I_{IL}	Logic Input Leakage Current. V_{DD} = MAX., V_{IN} = GND to V_{DD}.	–	–	±100	µA
C_{IND}	Input Capacitance, Digital Input.	–	–	15	pF
C_{LD}	Digital Output Load Capacitance.	–	–	20	pF
R_{INRX}	Input Resistance. RXIF to RXIF/ Differential.	400	550	740	Ω
C_{INRX}	Input Capacitance. RXIF and RXIF/ to Ground.	–	0.40	–	pF
Z_{OFF}	Offset Adjust Input Impedance. IOFFSET, QOFFSET.	100	–	–	kΩ
R_L	Load Resistance. TXIF to TXIF/ Differential.	495	500	505	Ω
C_L	Load Capacitance. TXIF, TXIF/ to Ground.	–	–	5	pF
Z_{TX}	Output Impedance. TXIF, TXIF/, Differential.	–	–	60	Ω
Z_{VCO}	VCO tuning circuit Input Impedance. RXVOC_T[1:2], TXVCO_T[1:2].	–	2	–	kΩ
Z_{PD}	PD_OUT Output Impedance. Within Compliance Range.	1	–	–	MΩ
LK_{VOL}	LOCK Output Logic Low Voltage. RLD ≥ 10 kΩ to V_{DD}.	–	–	0.4	V
LK_{IOH}	LOCK Output Leakage Current. V_{OUT} = V_{DD}.	–	–	10	µA
Z_{TC}	TCXO Input Impedance.	5	–	–	kΩ
Z_{INAD}	General-Purpose ADC Input Impedance. ADCIN.	20	–	–	kΩ
V_{INAD}	General-Purpose ADC Input Signal Range. V_{DD} = 3.3 V.	0.5	–	2.5	V
V_{OXO4}	TCXO/4 Output Signal Level. Into 10 kΩ load in parallel with 10 pF.	1.5	–	–	V_{PP}
R_{SAD}	General-Purpose ADC Source Resistance. Connected to ADCIN pin.	–	–	39	Ω

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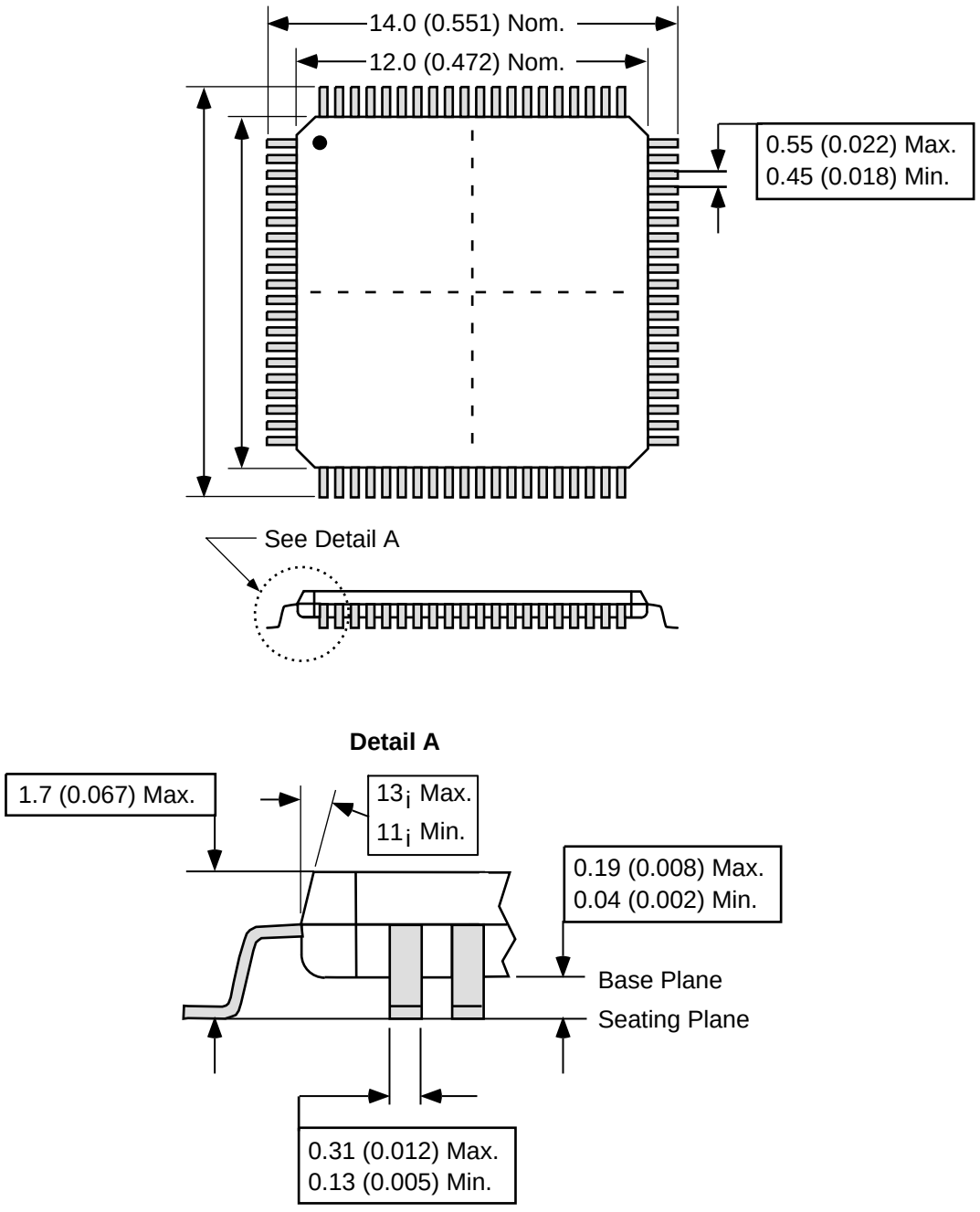
MECHANICAL SPECIFICATIONS

The Q5213 (BBA2) is packaged in an 80-pin Thin Quad Flat Pack (TQFP) package. The TQFP has 20-mil lead pitch and is no greater than 1.7 mm above the seating plane (JEDEC Publication 95 MS-026 Variation BDD). Figure 6 shows the package outline drawing.

Figure 6. 80-pin TQFP Package Outline Drawing



Dimensions: millimeters (inches)

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