

# RC2211A

## FSK Demodulator/Tone Decoder

### Features

- Wide frequency range – 0.01 Hz to 300 kHz
- Wide supply voltage range – 4.5V to 20V
- DTL/TTL/ECL logic compatibility
- FSK demodulation with carrier-detector
- Wide dynamic range – 2 mV to 3 VRMS
- Adjustable tracking range –  $\pm 1\%$  to  $\pm 80\%$
- Excellent temperature stability – 20 ppm/°C typical

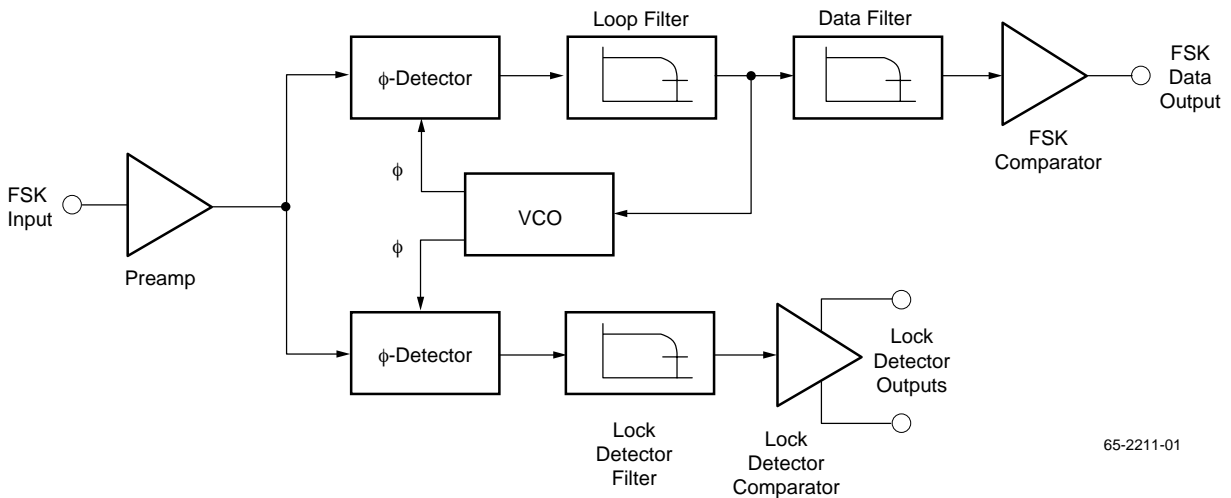
### Applications

- FSK demodulation
- Data synchronization
- Tone decoding
- FM detection
- Carrier detection

### Description

The RC2211A is a monolithic phase-locked loop (PLL) system especially designed for data communications. It is particularly well-suited for FSK modem applications, and operates over a wide frequency range of 0.01 Hz to 300 kHz. It can accommodate analog signals between 2 mV and 3V, and can interface with conventional DTL, TTL and ECL logic families. The circuit consists of a basic PLL for tracking an input signal frequency within the passband, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set carrier frequency, bandwidth and output delay.

### Block Diagram



65-2211-01

## Functional Description

### Signal Input (Pin 2)

The input signal is AC coupled to this terminal. The internal impedance at pin 2 is 20 k $\Omega$ . Recommended input signal level is in the range of 10 mVRMS to 3 VRMS.

### Quadrature Phase Detector Output, Q (Pin 3)

This is the high impedance output of the quadrature phase detector, and is internally connected to the input of lock detector voltage comparator. In tone detection applications, pin 3 is connected to ground through a parallel combination of  $R_D$  and  $C_D$  (see Figure 1) to eliminate chatter at the lock detector outputs. If this tone detector section is not used, pin 3 can be left open circuited.

### Lock Detector Output, Q (Pin 5)

The output at pin 5 is at a “high” state when the PLL is out of lock and goes to a “low” or conducting state when the PLL is locked. It is an open collector output and requires a pull-up resistor,  $R_L$ , to  $+V_S$  for proper operation. In the “low” state it can sink up to 5 mA of load current.

### Lock Detector Complement, $\bar{Q}$ (Pin 6)

The output at pin 6 is the logic complement of the lock detector output at pin 5. This output is also an open collector type stage which can sink 5 mA of load current in the low or “on” state.

### FSK Data Output (Pin 7)

This output is an open collector stage which requires a pull-up resistor,  $R_L$ , to  $+V_S$  for proper operation. It can sink 5 mA of load current. When decoding FSK signals the FSK data output will switch to a “high” or off state for low input frequency, and will switch to a “low” or on state for high input frequency. If no input signal is present, the logic state at pin 7 is indeterminate.

### FSK Comparator Input (Pin 8)

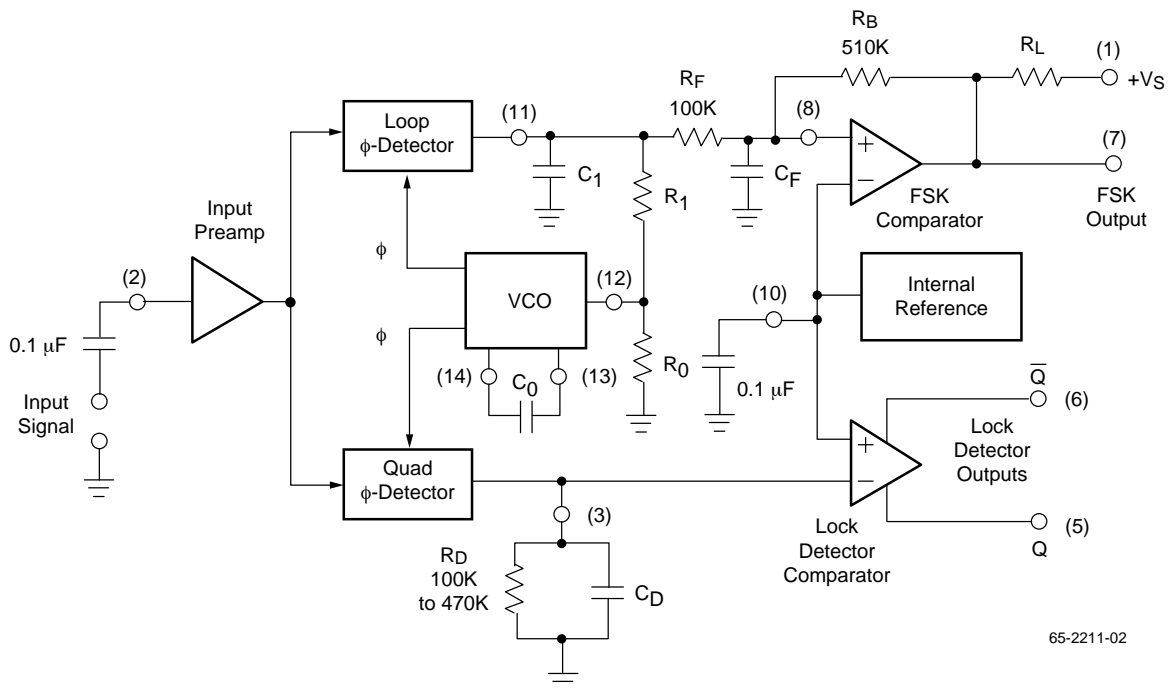
This is the high impedance input to the FSK voltage comparator. Normally, an FSK post detection or data filter is connected between this terminal and the PLL phase detector output (pin 11). This data filter is formed by  $R_F$  and  $C_F$  of Figure 1. The threshold voltage of the comparator is set by the internal reference voltage,  $V_R$ , available at pin 10.

### Reference Bypass (Pin 9)

This pin can have an optional 0.1  $\mu\text{F}$  capacitor connected to the ground.

### Reference Voltage, $V_R$ (Pin 10)

This pin is internally biased at the reference voltage level,  $V_R$ ;  $V_R = +V_S/2 - 650 \text{ mV}$ . The DC voltage level at this pin forms an internal reference for the voltage levels at pin 3, 8, 11 and 12. Pin 10 must be bypassed to ground with a 0.1  $\mu\text{F}$  capacitor.



65-2211-02

Figure 1. Generalized Circuit Connection for FSK and Tone Detection

### Loop Phase Detector Output (Pin 11)

This terminal provides a high impedance output for the loop phase detector. The PLL loop filter is formed by R1 and C1 connected to pin 11 (see Figure 1). With no input signal, or with no phase error within the PLL, the DC level at pin 11 is very nearly equal to VR. The peak voltage swing available at the phase detector output is equal to ±VR.

### VCO Control Input (Pin 12)

VCO free running frequency is determined by external timing resistor, R0, connected from this terminal to ground. The VCO free running frequency, F0 is given by:

$$F_0(\text{Hz}) = \frac{1}{R_0 C_0}$$

where C0 is the timing capacitor across pins 13 and 14. For optimum temperature stability R0 must be in the range of 10 kΩ to 100 kΩ (see Typical Performance Characteristics).

This terminal is a low impedance point, and is internally biased at a DC level equal to VR. The maximum timing current drawn from pin 12 must be limited to ≤3 mA for proper operation of the circuit.

### VCO Timing Capacitor (Pins 13 and 14)

VCO frequency is inversely proportional to the external timing capacitor, C0, connected across these terminals. C0 must be non-polarized, and in the range of 200 pF to 10 μF.

### VCO Frequency Adjustment

VCO can be fine tuned by connecting a potentiometer, Rx, in series with R0 at pin 12 (see Figure 2).

### VCO Free-Running Frequency, F0

The RC2211A does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase detector sections of the circuit. However, for set-up or adjustment purposes, the VCO freerunning frequency can be measured at pin 3 (with CD disconnected) with no input and with pin 2 shorted to pin 10.

## Design Equations

See Figure 1 for Definitions of Components.

1. VCO Center Frequency, F0:

$$F_0(\text{Hz}) = \frac{1}{R_0 C_0}$$

2. Internal Reference Voltage, VR (measured at pin 10)

$$V_R = \left(\frac{+V_S}{2}\right) - 650 \text{ mV}$$

3. Loop Lowpass Filter Time Constant, τ

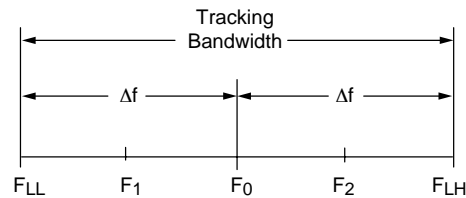
$$\tau = R_1 C_1$$

4. Loop Dampening, ζ:

$$\zeta = \left(\sqrt{\frac{C_0}{C_1}}\right) \left(\frac{1}{4}\right)$$

5. Loop Tracking Bandwidth, ±Δf/F0:

$$\Delta f/F_0 = R_0/R_1$$



65-2211-03

6. FSK Data Filter Time Constant, τF:

$$\tau_F = R_F C_F$$

7. Loop Phase Detector Conversion Gain, Kφ (Kφ is the differential DC voltage across pins 10 and 11, per unit of phase error at phase-detector input):

$$k\phi(\text{in volts per radian}) = \frac{(-2)(V_R)}{\pi}$$

8. VCO Conversion Gain, K0 is the amount of change in VCO frequency per unit of DC voltage change at pin 11:

$$K_0(\text{in Hertz per volt}) = \frac{-1}{C_0 R_1 V_R}$$

9. Total Loop Gain, KT:

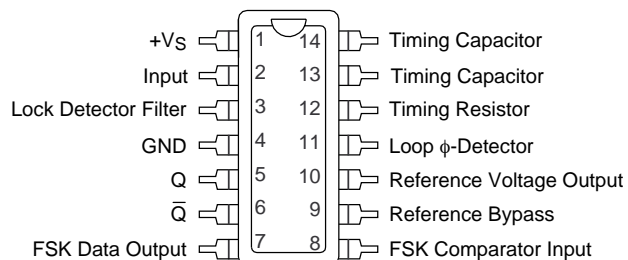
$$K_T(\text{in radians per second per volt}) = 2 \pi K\phi K_0$$

$$= \frac{4}{C_0 R_1}$$

10. Peak Phase Detector Current, IA:

$$I_A(\text{mA}) = \frac{V_R}{25}$$

## Pin Assignments



65-2211-04

## Absolute Maximum Ratings

Parameter	Conditions	Min.	Max.	Unit
Supply Voltage			+20	V
Input Signal Level			3	VRMS
Storage Temperature Range		-65	+150	°C
Operating Temperature Range	RV2211A	-25	+85	°C
	RC2211A	0	+70	°C
Junction Temperature			+125	°C
Lead Soldering Temperature (60 sec.)			+300	°C
Max. PD $T_A < 50^\circ\text{C}$			468	mW

## Thermal Characteristics

Parameter	14 Lead Plastic DIP	14 Lead SOIC
Therm. Res. $\theta_{JA}$	92°C/W	150°C/W

## Electrical Characteristics

(Test Conditions  $+V_S = +12V$ ,  $T_A = +25^\circ C$ ,  $R_0 = 30\text{ k}\Omega$ ,  $C_0 = 0.033\text{ }\mu\text{F}$ . See Figure 1 for component designations.)

Parameters	Test Conditions	RV2211A			RC2211A			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
<b>General</b>								
Supply Voltage <sup>2</sup>		4.5		20	4.5		20	V
Supply Current	$R_0 \geq 10\text{ k}\Omega$		5.0	11.0		5.0	11	mA
<b>Oscillator</b>								
Frequency Accuracy	Deviation from $f_0 = 1/R_0C_0$		$\pm 1.0$	$\pm 3.0$		$\pm 1.0$	$\pm 5$	%
Frequency Stability <sup>1</sup>								
Temperature Coefficient	$R_1 = \infty$		$\pm 20$			$\pm 20$		ppm/ $^\circ C$
Power Supply Rejection	$+V_S = 12 \pm 1V$ $+V_S = 5 \pm 0.5V$		0.05 0.2	0.5	0.2	0.05	0.5	%/V %/V
Upper Frequency Limit	$R_0 = 8.2\text{ k}\Omega$ , $C_0 = 400\text{ pF}$	100	300			300		kHz
Lowest Practical Operating Frequency <sup>1</sup>	$R_0 = 2\text{ M}\Omega$ , $C_0 = 50\text{ }\mu\text{F}$		0.01			0.01		Hz
Timing Resistor, $R_0$								
Operating Range		5.0		2000	5.0		2000	k $\Omega$
Recommended Range		15		100	15		100	k $\Omega$
<b>Loop Phase Detector</b>								
Peak Output Current	Measured at pin 11	$\pm 150$	$\pm 200$	$\pm 300$	$\pm 100$	$\pm 200$	$\pm 300$	$\mu\text{A}$
Output Offset Current			$\pm 1.0$			$\pm 2.0$		$\mu\text{A}$
Output Impedance			1.0			1.0		M $\Omega$
Maximum Swing	Ref. to pin 10	$\pm 4.0$	$\pm 5.0$		$\pm 4.0$	$\pm 5.0$		V
<b>Quadrature Phase Detector</b>								
Peak Output Current <sup>3</sup>	Measured at pin 3	100	150			150		$\mu\text{A}$
Output Impedance			1.0			1.0		M $\Omega$
Maximum Swing			11			11		V <sub>P-P</sub>
<b>Input Preamp</b>								
Input Impedance	Measured at pin 2		18			18		k $\Omega$
Input Signal Voltage Required to Cause Limiting <sup>3</sup>	$V_S = +6V$ $f = 1.7\text{ kHz}$	2.0	1.0		2.0	1.0		mV <sub>RMS</sub>
<b>Voltage Comparator</b>								
Input Impedance	Measured at pins 3 & 8		2.0			2.0		M $\Omega$
Input Bias Current			100			100		nA
Voltage Gain <sup>1</sup>	$R_L = 5.1\text{ k}\Omega$	55	70		55	70		dB
Output Voltage Low	$I_C = 3\text{ mA}$		300			300		mV
Output Leakage Current	$V_0 = 12V$		0.01			0.01		$\mu\text{A}$
<b>Internal Reference</b>								
Voltage Level	Measured at pin 10	4.9	5.3	5.7	4.75	5.3	5.85	V
Output Impedance			100			100		$\Omega$

### Notes:

1. Guaranteed by design.
2. Individual applications may need special circuitry to function at  $<12V$ .
3. Sample tested.

### Typical Performance Characteristics

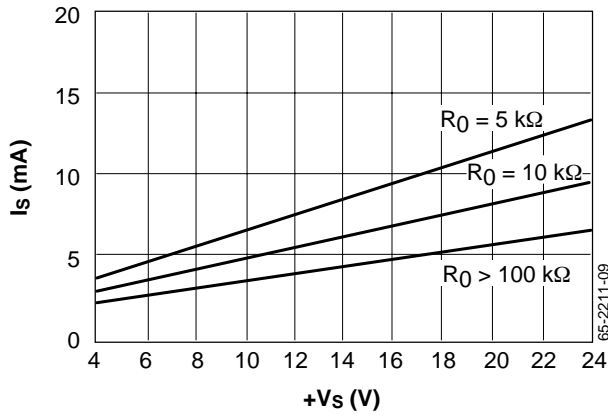


Figure 6. Supply Current vs. Supply Voltage (Logic Outputs Open Circuited)

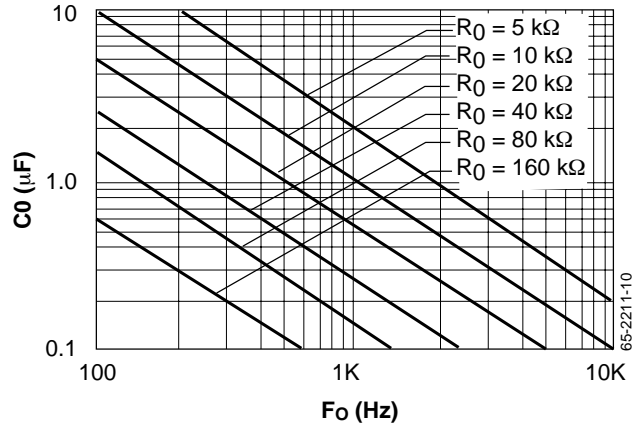


Figure 7. Timing Resistor with Timing Capacitor vs. VCO Frequency

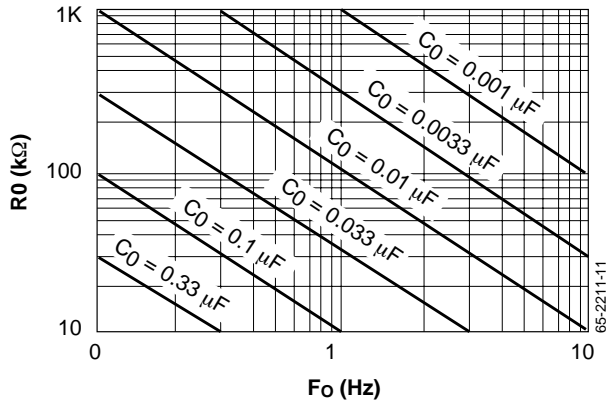


Figure 8. Timing Capacitor with Timing Resistor vs. VCO Frequency

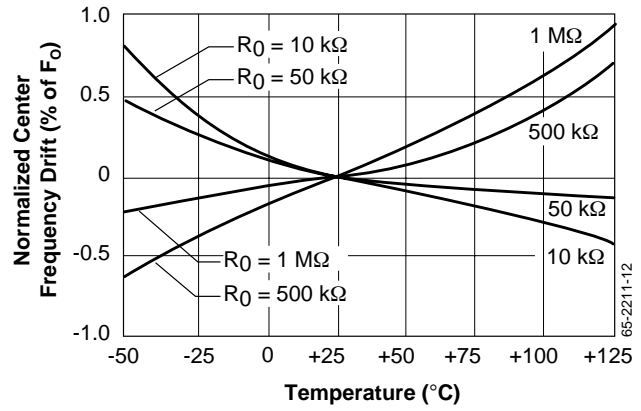


Figure 9. Center Frequency Drift vs. Temperature

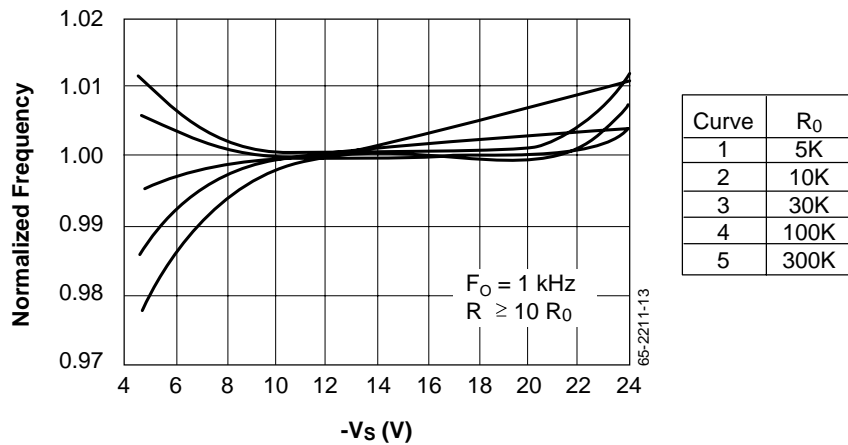


Figure 10. VCO Frequency vs. Supply Voltage

# Applications Discussion

## FSK Decoding

Figure 2 shows the basic circuit connection for FSK decoding. With reference to Figures 1 and 2, the functions of external components are defined as follows: R<sub>0</sub> and C<sub>0</sub> set the PLL center frequency, R<sub>1</sub> sets the system bandwidth, and C<sub>1</sub> sets the loop filter time constant and the loop damping factor. C<sub>F</sub> and R<sub>F</sub> form a one pole post-detection filter for the FSK data output. The resistor R<sub>B</sub> (510 kΩ) from pin 7 to pin 8 introduces positive feedback across FSK comparator to facilitate rapid transition between output logic states.

Recommended component values for some of the most commonly used FSK bauds are given in Table 1.

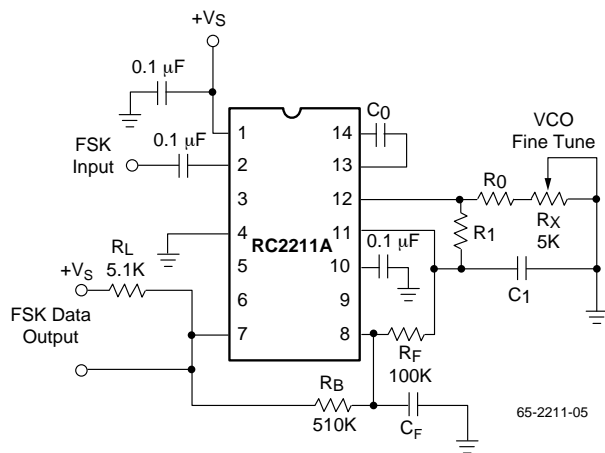


Figure 2. Circuit Connection for FSK Decoding

Table 1. Recommended Component Values for Commonly Used FSK Bands (see Circuit of Figure 2)

FSK Band	Component Values
<b>300 Baud</b> F <sub>1</sub> = 1070 Hz F <sub>2</sub> = 1270 Hz	C <sub>0</sub> = 0.039 μF, C <sub>F</sub> = 0.005 μF C <sub>1</sub> = 0.01 μF, R <sub>0</sub> = 18 kΩ R <sub>1</sub> = 100 kΩ
<b>300 Baud</b> F <sub>1</sub> = 2025 Hz F <sub>2</sub> = 2225 Hz	C <sub>0</sub> = 0.022 μF, C <sub>F</sub> = 0.005 μF C <sub>1</sub> = 0.0047 μF, R <sub>0</sub> = 18 kΩ R <sub>1</sub> = 200 kΩ
<b>1200 Baud</b> F <sub>1</sub> = 1200 Hz F <sub>2</sub> = 2200 Hz	C <sub>0</sub> = 0.027 μF, C <sub>F</sub> = 0.0022 μF C <sub>1</sub> = 0.01 μF, R <sub>0</sub> = 18 kΩ R <sub>1</sub> = 30 kΩ

## Design Instructions

The circuit of Figure 2 can be tailored for any FSK decoding application by the choice of five key circuit components: R<sub>0</sub>, R<sub>1</sub>, C<sub>0</sub>, C<sub>1</sub> and C<sub>F</sub>. For a given set of FSK mark and space frequencies, F<sub>1</sub> and F<sub>2</sub>, these parameters can be calculated as follows:

1. Calculate PLL center frequency, F<sub>0</sub>

$$F_0 = \frac{F_1 + F_2}{2}$$

2. Choose a value of timing resistor R<sub>0</sub> to be in the range of 10 kΩ to 100 kΩ. This choice is arbitrary. The recommended value is R<sub>0</sub> = 20 kΩ. The final value of R<sub>0</sub> is normally finetuned with the series potentiometer, R<sub>X</sub>.

3. Calculate value of C<sub>0</sub> from Design Equation No. 1 or from Typical Performance Characteristics:

$$C_0 = 1/R_0F_0$$

4. Calculate R<sub>1</sub> to give a Δf equal to the markspace deviation:

$$R_1 = R_0 [F_0/(F_1 - F_2)]$$

5. Calculate C<sub>1</sub> to set loop damping. (See Design Equation No. 4)

Normally, ζ ≈ 1/2 is recommended  
Then: C<sub>1</sub> = C<sub>0</sub>/4 for ζ = 1/2

6. Calculate Data Filter Capacitance, C<sub>F</sub>:  
For R<sub>F</sub> = 100 kΩ, R<sub>B</sub> = 510 kΩ, the recommended value of C<sub>F</sub> is:

$$C_F(\text{in } \mu\text{F}) = \frac{3}{\text{Baud Rate}}$$

**Note:** All calculated component values except R<sub>0</sub> can be rounded off to the nearest standard value, and R<sub>0</sub> can be varied to fine-tune center frequency through a series potentiometer, R<sub>X</sub> (see Figure 2).

## Design Example

75 Baud FSK demodulator with mark space frequencies of 1110/1170 Hz:

Step 1: Calculate F<sub>0</sub>:

$$F_0 = (1110 + 1170) / 2 = 1140 \text{ Hz}$$

Step 2: Choose R<sub>0</sub> = 20 kΩ (18 kΩ fixed resistor in series with 5 kΩ potentiometer)

Step 3: Calculate C<sub>0</sub> from VCO Frequency vs. Timing Capacitor: C<sub>0</sub> = 0.044 μF

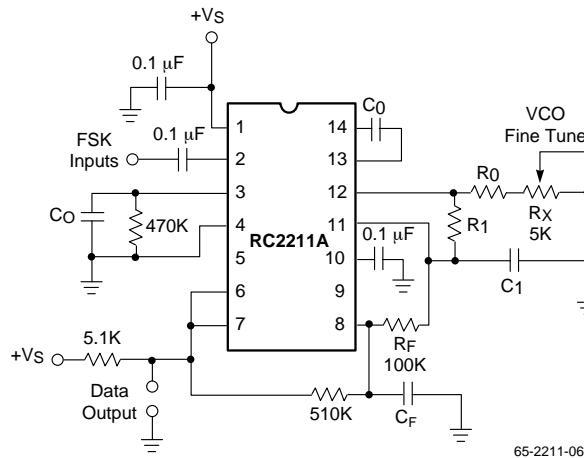
Step 4: Calculate R<sub>1</sub>: R<sub>1</sub> = R<sub>0</sub> (1140/60) = 380 kΩ

Step 5: Calculate C<sub>1</sub>: C<sub>1</sub> = C<sub>0</sub>/4 = 0.011 μF

**Note:** All values except R<sub>0</sub> can be rounded off to nearest standard value.

## FSK Decoding with Carrier Detector

The lock detector section of the RC2211A can be used as a carrier detector option for FSK decoding. The recommended circuit connection for this application is shown in Figure 3. The open-collector lock detector output, pin 6, is shorted to the data output (pin 7). Thus, the data output will be disabled at “low” state, until there is a carrier within the detection band of the PLL, and the pin 6 output goes “high” to enable the data output.



**Note:** Data output is “low” when no carrier is present.

**Figure 3. External Connections for FSK Demodulation with Carrier Detector Capability**

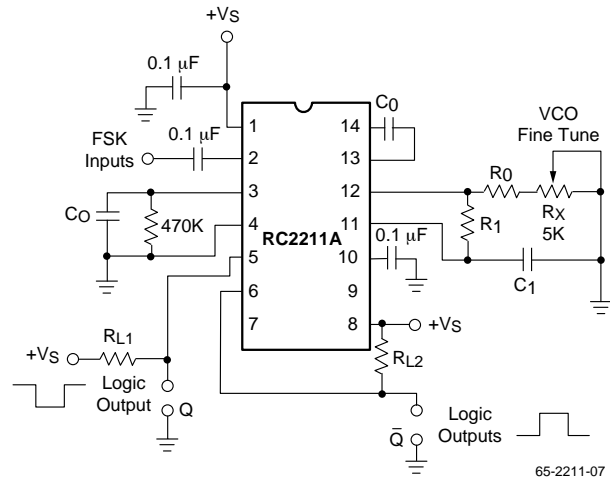
The minimum value of the lock detector filter capacitance  $C_D$  is inversely proportional to the capture range,  $\pm\Delta f C$ . This is the range of incoming frequencies over which the loop can acquire lock and is always less than the tracking range. It is further limited by  $C_1$ . For most applications,  $\Delta f C < \Delta f / 2$ . For  $R_D = 470 \text{ k}\Omega$ , the approximate minimum value of  $C_D$  can be determined by:

$$C_D(\mu\text{F}) \geq 16/\text{capture range in Hz}$$

With values of  $C_D$  that are too small, chatter can be observed on the lock detector output as an incoming signal frequency approaches the capture bandwidth. Excessively large values of  $C_D$  will slow the response time of the lock detector output.

## Tone Detection

Figure 4 shows the generalized circuit connection for tone detection. The logic outputs,  $Q$  and  $\bar{Q}$  at pins 5 and 6 are normally at “high” and “low” logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these outputs becomes reversed to the duration of the input tone. Each logic output can sink 5 mA of load current.



**Figure 4. Circuit Connection for Tone Detection**

Both logic outputs at pins 5 and 6 are open-collector type stages, and require external pull-up resistors  $R_{L1}$  and  $R_{L2}$  as shown in Figure 4.

With reference to Figures 1 and 4, the function of the external circuit components can be explained as follows:  $R_0$  and  $C_0$  set VCO center frequency,  $R_1$  sets the detection bandwidth,  $C_1$  sets the lowpass-loop filter time constant and the loop dampening factor, and  $R_{L1}$  and  $R_{L2}$  are the respective pull-up resistors for the  $Q$  and  $\bar{Q}$  logic outputs.

## Design Instructions

The circuit of Figure 4 can be optimized for any tone-detection application by the choice of five key circuit components:  $R_0$ ,  $R_1$ ,  $C_0$ ,  $C_1$  and  $C_D$ . For a given input tone frequency,  $F_S$ , these parameters are calculated as follows:

1. Choose  $R_0$  to be in the range of 15 k $\Omega$  to 100 k $\Omega$ . This choice is arbitrary.
2. Calculate  $C_0$  to set center frequency,  $f_0$  equal to  $F_S$ :  $C_0 = 1/R_0 F_S$ .
3. Calculate  $R_1$  to set bandwidth  $\pm\Delta f$  (see Design Equation No. 5):  $R_1 = R_0(F_0/\Delta f)$ . Note: The total detection bandwidth covers the frequency range of  $F_0 \pm \Delta f$ .
4. Calculate value of  $C_1$  for a given loop damping factor:
 
$$C_1 = C_0 / 16\zeta^2$$

Normally  $\zeta = 1/2$  is optimum for most tone detector applications, giving  $C_1 = 0.25 C_0$ .

Increasing  $C_1$  improves the out-of-band signal rejection, but increases the PLL capture time.

5. Calculate value of filter capacitor  $C_D$ . To avoid chatter at the logic output, with  $R_D = 470\Omega$ ,  $C_D$  must be:

$$C_D(\mu\text{F}) \geq (16/\text{capture range in Hz})$$

Increasing  $C_D$  slows the logic output response time.





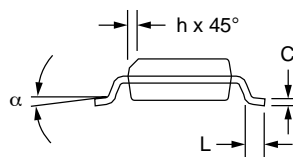
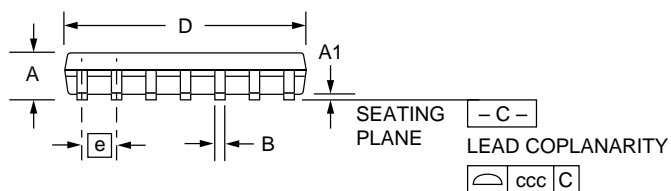
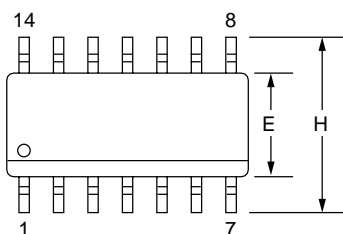
# Mechanical Dimensions

## 14-Pin SOIC Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.19	0.25	5
D	.336	.345	8.54	8.76	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	14		14		6
$\alpha$	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

**Notes:**

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.



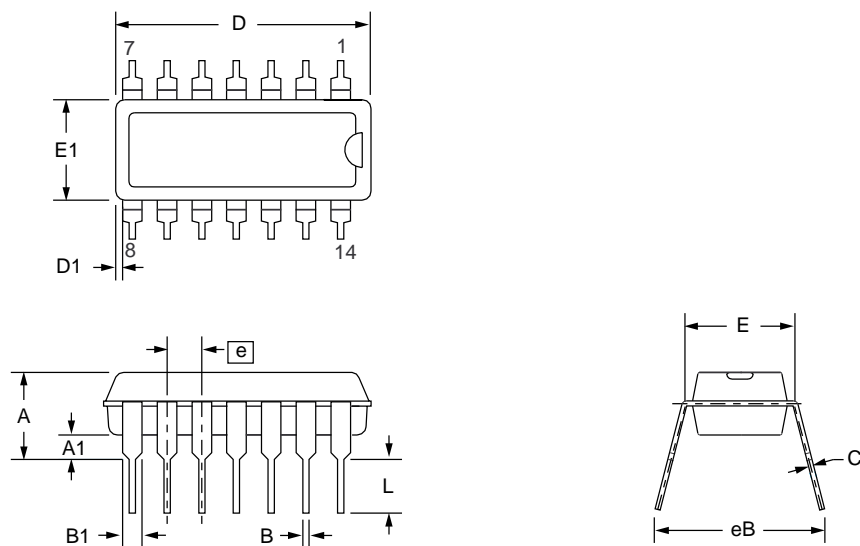
# Mechanical Dimensions (continued)

## 14-Lead Plastic DIP Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.725	.795	18.42	20.19	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.200	2.92	5.08	
N	14		14		5

**Notes:**

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are shown for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.



## Ordering Information

Part Number	Package	Operating Temperature Range
RC2211AN	14-Lead Plastic DIP	0°C to +70°C
RC2211AM	14-Lead Plastic SOIC	0°C to +70°C
RV2211AN	14-Lead Plastic DIP	-25°C to +85°C
RV2211AM	14-Lead Plastic SOIC	-25°C to +85°C

### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.