RC6564A

IF-to-Digital™ Converter

Features

- Integrated IF-to-Digital™ conversion
- IF bandwidth from 30 to 80MHz
- 40MHz 8 bit ADC
- Operating range between 8.5V to 13.2V
- Demodulation of 64QAM constellations
- Simple interface to SAW filter and digital demodulator
- Tuner control feature interfaces with variety of tuners
- Low phase noise LO generation
- Crystal oscillator for fundamental or 3rd overtone mode
- 63dB peak conversion gain from IF to baseband
- 30dB minimum AGC range
- 45dB IMD3 end-to-end
- On-chip 2V stable voltage reference
- 44-pin PLCC package

Applications

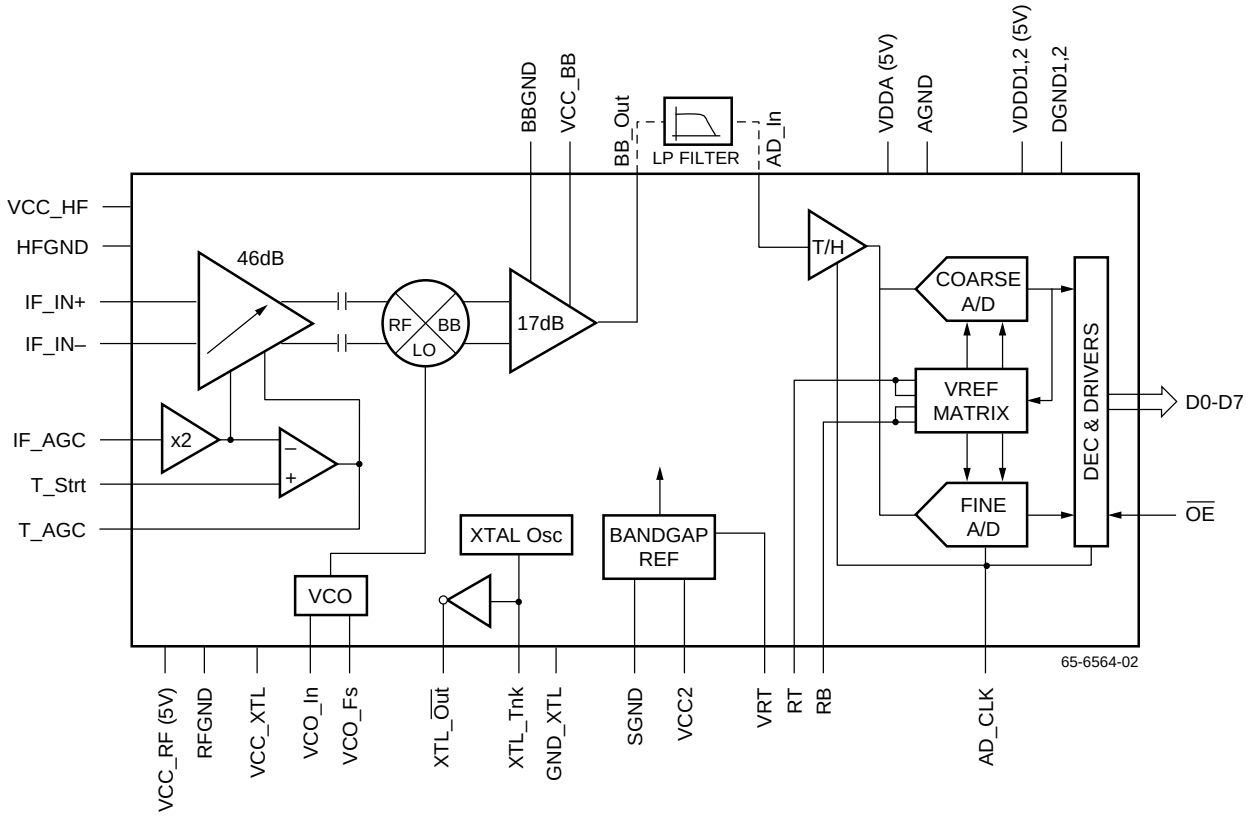
- QAM receivers
- Set-top receivers for digital cable
- Internet surf-boards
- Cable modems
- Desktop video conferencing
- IF sampling decoders

General Description

The RC6564A is a single chip solution for downconverting and digitizing QAM signals that can be decoded in the digital domain by custom DSP demodulators. The RC6564A performs IF amplification with gain control, frequency down conversion, frequency synthesis for mixer Local Oscillator (LO) and system clock generation, and baseband quantization with an Analog to Digital converter. The input can directly interface to a SAW filter and maintain low noise figure. Depending on the signal input level the gain may be controlled over a 30dB range through an external analog input signal. The gain reduction is done in two stages and orchestrated in such a manner as to minimize noise figure and signal distortion. The IF output is then down converted and filtered using a double balanced mixer. This output can be filtered even further, externally, before being quantized by the on-chip A/D converter.The digital data output can be processed to derive information for automatic gain control (AGC) and automatic frequency control (AFC). RC6564A is optimized to work with DSP decoders based on IF sampling. The RC6564A also provides an optimum tuner AGC control voltage useful for controlling the front-end tuner gain.

The IF and mixer section works at 9V. The oscillator works on 5V supply. The A/D converter has one analog 5V supply and two digital 5V supplies. The RC6564A is available in a 44 pin PLCC package.

Block Diagram



Functional Description

The RC6564A performs all the IF and baseband signal processing/conversion with minimal external components. As shown in the Block Diagram, the RC6564A consists of three general sections:

1. IF Gain blocks with Gain Control
2. IF down conversion with LO & Clock Generation
3. Analog to Digital Conversion

The IF Section

The signal input is fed into a variable gain amplifier capacitively coupled to the subsequent stages. The gain is directly proportional to IF_AGC voltage. To minimize the noise figure degradation with gain reduction the gains in various stages are not reduced simultaneously. The transition point is set by the voltage on T_Strt pin. T_Strt sets the T_AGC trigger to control the front tuner gain.

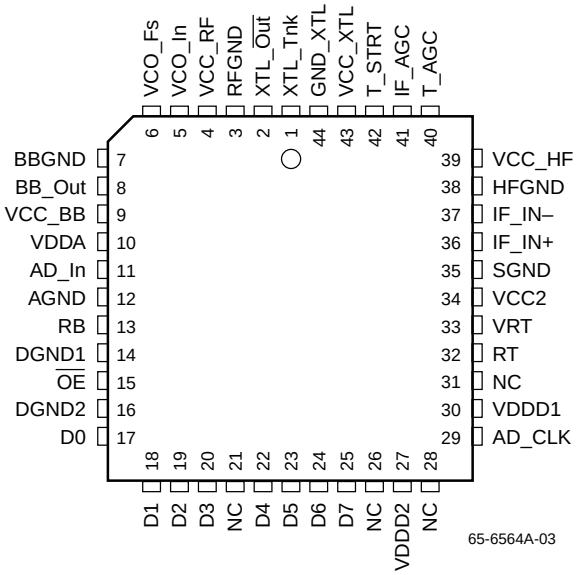
IF Down Conversion & Frequency Synthesis

This section consists of a double balanced linear mixer. The output of the front-end gain stage is capacitively coupled to the input (RF port) of the mixer. The mixer output is further amplified. The signals for the Local Oscillator (LO) port of the mixer can be directly driven or synthesized through the VCO (Voltage Controlled Oscillator). The mixer output is partially filtered on-chip but may need to be further filtered externally before being fed to the A/D input. The RC6564A also has a crystal oscillator circuit that can be used for generating a master clock for frequency synthesis.

Analog-to-Digital Converter

The analog-to-digital converter employs a two-step 9-bit architecture to convert analog signals into digital words at sample rates up to 40 Msps (Mega samples per second). An integral Track/Hold circuit delivers excellent performance on signals with full-scale components up to 12MHz. A dynamic performance of more than 7.4 effective bits is delivered at the outputs D0 through D7. The A/D digital outputs are three-state and TTL/CMOS compatible. The down converted output at BB_OUT can be externally filtered and directly connected to the A/D input. Sampling of the applied input signals takes place on the falling edge of the AD_CLK. The output word is delayed by 2.5 AD_CLK cycles. An output enable control $\overline{OE}$ places the outputs in high impedance state when HIGH. The outputs are enabled when $\overline{OE}$ is LOW as described in the Timing Diagrams section.

Pin Assignments



Pin Descriptions

Pin Name	Pin Number	Pin Function Description
AD_CLK	29	Clock Input for A/D Converter. AD_In sampled on the falling edge.
AGND	12	Analog Ground Connection for A/D.
AD_In	11	Analog Input to the A/D Converter Section.
BBGND	7	Ground Connection for IF.
BB_Out	8	Base-band Voltage Output.
D0-D3	17, 18, 19, 20	Output Lower Significant Bits. Valid data on rising edge of AD_CLK.
D4-D7	22, 23, 24, 25	Output Upper Significant Bits. Valid data on rising edge of AD_CLK.
DGND1	14	Ground Connection for A/D.
DGND2	16	Ground Connection for A/D.
GND_XTL	44	Crystal Oscillator Ground for IF.
HFGND	38	Analog Ground Connection for IF.
IF_AGC	41	Input Voltage for IF Front End Gain Control
IF_IN+, IF_IN–	36, 37	IF Inputs.
N/C	21, 26, 28, 31	No Connection
$\overline{OE}$	15	Input for Enabling Digital Outputs. When LOW, D0-D7 are enabled. When HIGH D0-D7 are in high impedance state.
RB	13	Bottom Input Reference for A/D.
RFGND	3	Ground Connection for High Frequency Mixed Signal Sections for IF.
RT	32	Top Input Reference Voltage for A/D.
SGND	35	Analog Ground Connection for IF.
T_AGC	40	Output Voltage for Tuner Gain Control.
T_STRT	42	Threshold Voltage Input for Starting Tuner Gain Control.
VCC_BB	9	Baseband Supply Voltage. Typically 9V for IF.

Pin Descriptions (continued)

Pin Name	Pin Number	Pin Function Description
VCC2	34	Analog Supply Voltage (9V) for IF.
VCC_HF	39	Analog Supply Voltage (9V) for IF.
VCC_RF	4	Supply Voltage (5V) for High Frequency Mixed Signal Sections for IF.
VCC_XTL	43	Supply voltage for Crystal Oscillator for IF.
VCO_Fs	6	VCO External Frequency Select Circuit Connection.
VCO_In	5	VCO Input. Can be used for directly feeding external LOW.
VDDD1	30	+5V Digital Supply for A/D.
VDDD2	27	+5V Digital Supply for A/D.
VDDA	10	+5V Power Supply Voltage for A/D.
VRT	33	Output Reference Voltage from IF for Top of A/D Input Range.
XTL_$\overline{\text{Out}}$	2	Crystal Oscillator Output (inverted).
XTL_Tnk	1	Crystal Oscillator Frequency Select Circuit Connection.

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter		Conditions	Min	Typ	Max	Units
IF_IN+, IF_IN–, IF_AGC, T_Strt	Input Voltages		Gnd–0.3		V_{CC}+0.3	V
AD_IN	A/D input voltage		AGND		VDDA	V
VCC_RF, VCC_BB, VCC_HF, VCC2, VCC_XTL	Analog Supply Voltages				13.5	V
VDDA, VDDD 1,2	Digital Supply Voltages				7	V
Tstg	Storage Temperature		-40		125	°C

Note:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter		Min	Typ	Max	Units
V_{CC}	Analog Supply Voltage	8.5	9	13.2	V
VCC_RF, VCC_XTL	Supply Voltage for IF and Mixer, Supply Voltage for XTLOSC and VCO	4.75	5	5.25	V
VDDA,D	Digital Supply Voltages	4.75	5	5.25	V
T	Temperature	0		70	°C
RT	A/D Top Reference Voltage	1	2.5		V
RB	A/D Bottom Reference Voltage		0	0.7	V
VIN	Analog Input to A/D	RB		RT	V
VIH	Digital Inputs – Logic HIGH	0.7VDDD		VDDD	V
VIL	Digital Input – Logic LOW	GND		0.3VDDD	V
θJA	Thermal Coefficient Junction to Ambient		43		°C/W
θJC	Thermal Coefficient Junction to Case		16		°C/W

DC Electrical Characteristics

V_{CCRF}, VCC_XTL = 5V; V_{CCHF}, VCC_BB, VCC2 = 9V; T_A = 0 to 70°C, unless otherwise specified.

Parameter		Conditions	Min	Typ	Max	Units
PWIF	Power Consumption in IF			0.4	0.5	W
PWAD	Power Consumption in ADC	ADCLK = 20 Msps		0.1	0.16	W
ICCDD	Digital Supply Current	5V, 20Msps		20	30	mA
ICCHF	Front End Supply Current	9V Supply		20	25	mA
		12V Supply		27	35	
ICCBB	Back and Baseband Current	9V Supply		21	25	mA
ICCRF	RF Supply Current	5V Supply		6	10	mA
VRT	Reference Output Voltage		1.95	2.05	2.15	V
ΔVBBo	Base-band DC Output Swing		3.5			Vpp
Tagc_hi	Tuner AGC for Maximum Gain	IF_AGC = 5V		7.5		V
Tagc_lo	Tuner AGC for Minimum Gain	IF_AGC = 2V		2		V
RAD_IN	A/D Input Impedance		500	1000		KΩ
VOH	Output Voltage, HIGH, D0-D7	Ioh = 2.5mA	3.5			V
VOL	Output Voltage, LOW, D0-D7	Iol = 4mA			0.4	V
IOZ	Hi-Z Output Leakage	Maximum Reference Current Output			±5	μA

AC Electrical Characteristics

VCC_XTL, VCC_RF = 5V; VCC_HF, VCC_BB = 9V; IF_AGC = 2V; AD_CLK = 20Msps; Tstrt = 5V; T_A = 0 to 70°C, unless otherwise specified.

Parameter		Conditions	Min	Typ	Max	Units
ZIFin	AC Input Impedance	@43.75MHz	2			K Ω
CIFin	AC Equivalent Input Cap	IF_IN±		6		pF
Vis	Input Sensitivity at Maximum Gain			250		μV
IMD3	Two Tone Intermod	f1/f2 = 43.75 /42.75 Mhz, IF_IN= -16dBm, VCO_IN = 0.1Vpp, LO = 38.75MHz, See Note 1		45		dB
G	IF to Baseband Gain	IF_AGC = 2V	35	40		dB
NF	Noise Figure (Maximum Gain)			9		dB
Ragc	AGC Gain Control Range	IF_AGC = 0.8V–4V	30	35		dB
Sagc	AGC Sensitivity Average Slope	T_Strt = 5V, IF_AGC = 0.8V–4V		10		dB/V
BW_IF	IF Bandwidth	0.1dB for 10MHz Bands 0.1dB for 5MHz Bands	30 30	43.75	75 80	MHz
fLO	Down Conversion Frequency	VCO_IN = 0.1Vpp			100	MHz
ϕnLO	VCO Phase Noise	@ ±10KHz Offset			-100	dBC/Hz
ϕnXTL	XTAL OSC Phase Noise	@ ±10KHz Offset			-100	dBC/Hz
CAD	ADC Input Capacitance			4		pF
Eli	Integral Linearity Error			±0.5	±0.75	LSB
Eld	Differential Linearity Error			±0.3	±0.5	LSB

AC Electrical Characteristics (continued)

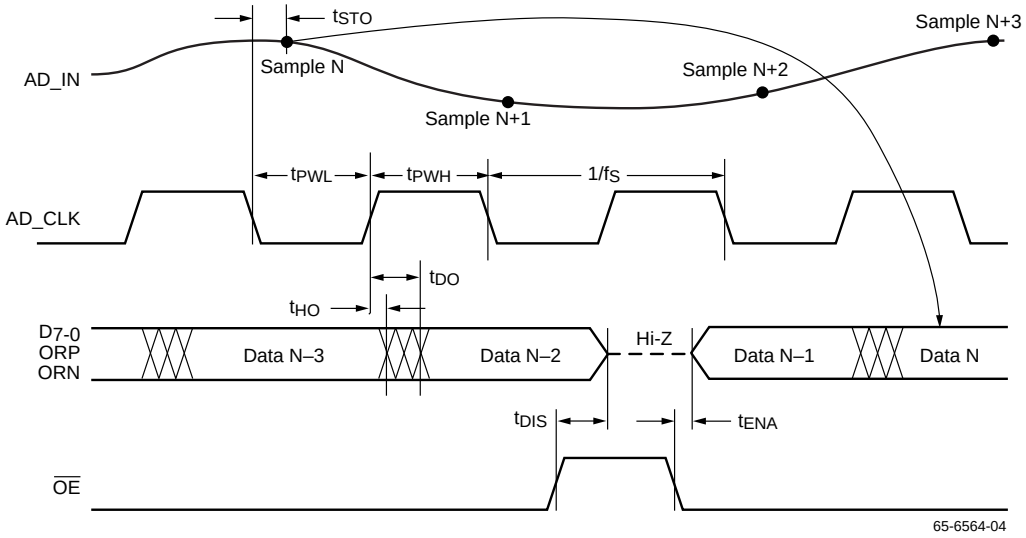
VCC_XTL, VCC_RF = 5V; VCC_HF, VCC_BB = 9V; IF_AGC = 2V; AD_CLK = 20Msps; Tstrt = 5V;
T_A = 0 to 70°C, unless otherwise specified.

Parameter		Conditions	Min	Typ	Max	Units
BW	A/D sine wave Bandwidth				12	MHz
Eap	Aperture Error			30		pS
SNR	Signal-to-Noise ratio	AD_CLK = 20MSPS, AD_IN = 5MHz		45		dB
tHO	Output Hold time	Cload = 15pF	5			nS
tDO	Output Delay time	Cload = 15pF			20	nS
tSTO	Sampling time offset		2	5	8	nS

Notes:

1. With the application of antialiasing filter as load and 2Vpp at A/D input.

Analog to Digital Conversion Timing Diagram



Typical Performance Characteristics

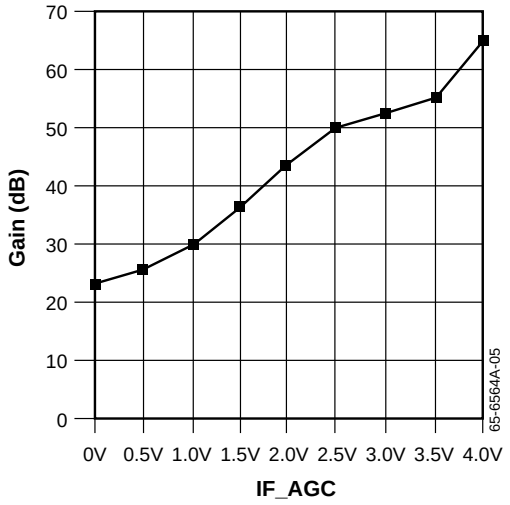


Figure 1. Typical IF AGC Control Characteristics

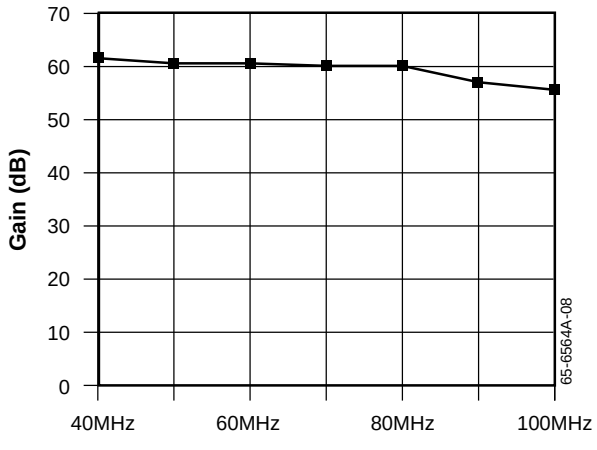


Figure 2. IF Input Bandwidth

Typical Performance Characteristics (Continued)

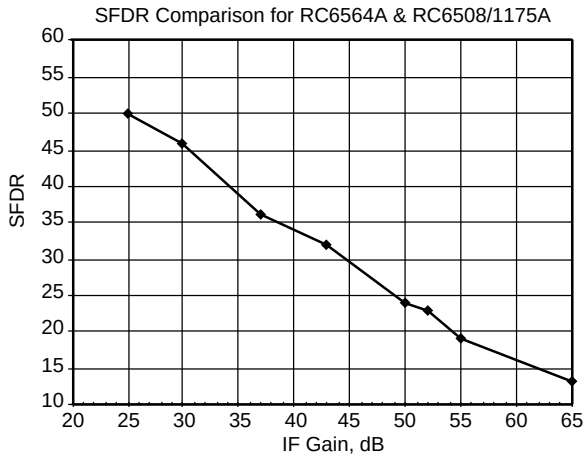
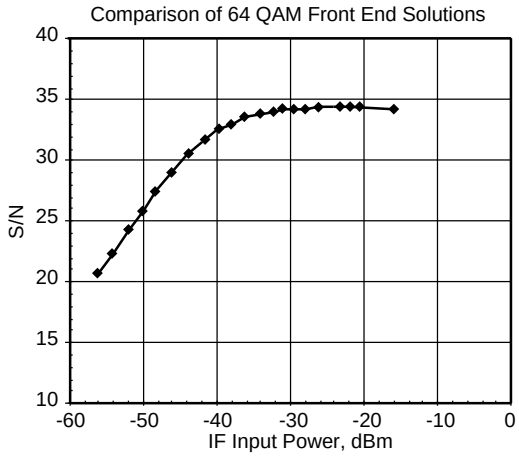


Figure 3. SFDR vs RC6564A (Fairchild Semiconductor Demo Board with 64 QAM demodulator)



S/N vs. IF Input Power RC6564 (Fairchild Semiconductor Demo Board with 64 QAM demodulator)

Applications

The RC6564A is specially suited for use in set-top boxes and cable modems for decoding QAM modulated signals based on IF sampling techniques. The RC6564A simplifies the front-end design and makes it more cost effective by integrating in a single chip the IF-to-Digital functionality. The other major components required for the front-end of the modem are the tuner, a SAW filter and the appropriate DSP demodulator/decoder.

Modem Applications

Figure 4 below shows the application of RC6564A in IF bandpass sampling decoding for cable access. The on-chip VCO provides low-phase noise characteristics. The VCO can be pulled by the voltage control on VCO_CNTRL. The sampling clock for the A/D conversion can be derived from the master clock through external frequency synthesis. The full scale reference signal for A/D is conveniently derived from the VRT output. The baseband output is referenced such that the filtered output is automatically in the mid-scale of the A/D input. The filtered output can be a.c. coupled to the AD_In. In the application below an external low-pass filter is used to bandlimit the signals before conversion. The gain is adjusted by the average voltage on the IF_AGC line to keep the signal in the optimum range of the A/D input. The T_AGC output is used to control the tuner gain when the input levels into the RC6564A are too high.

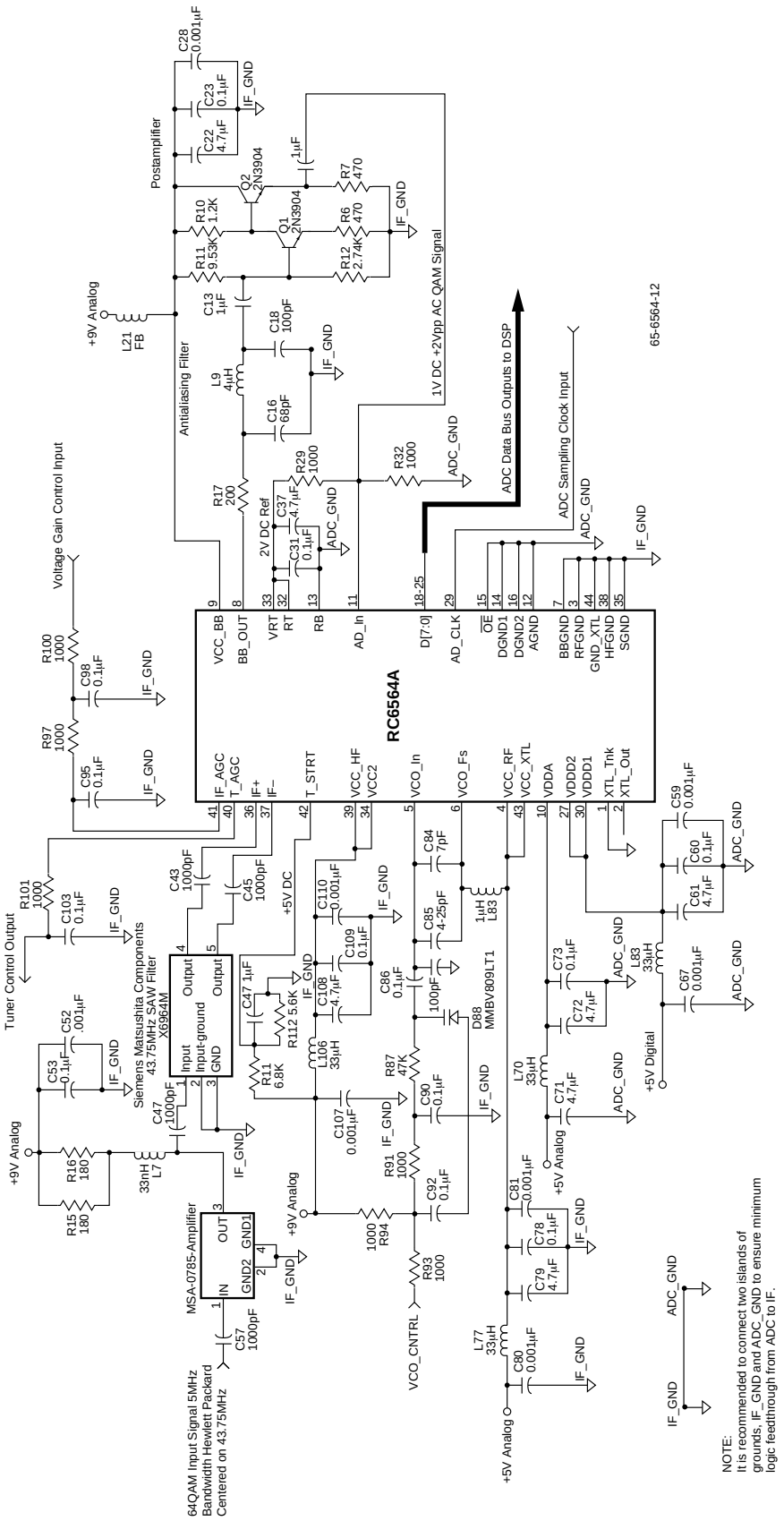
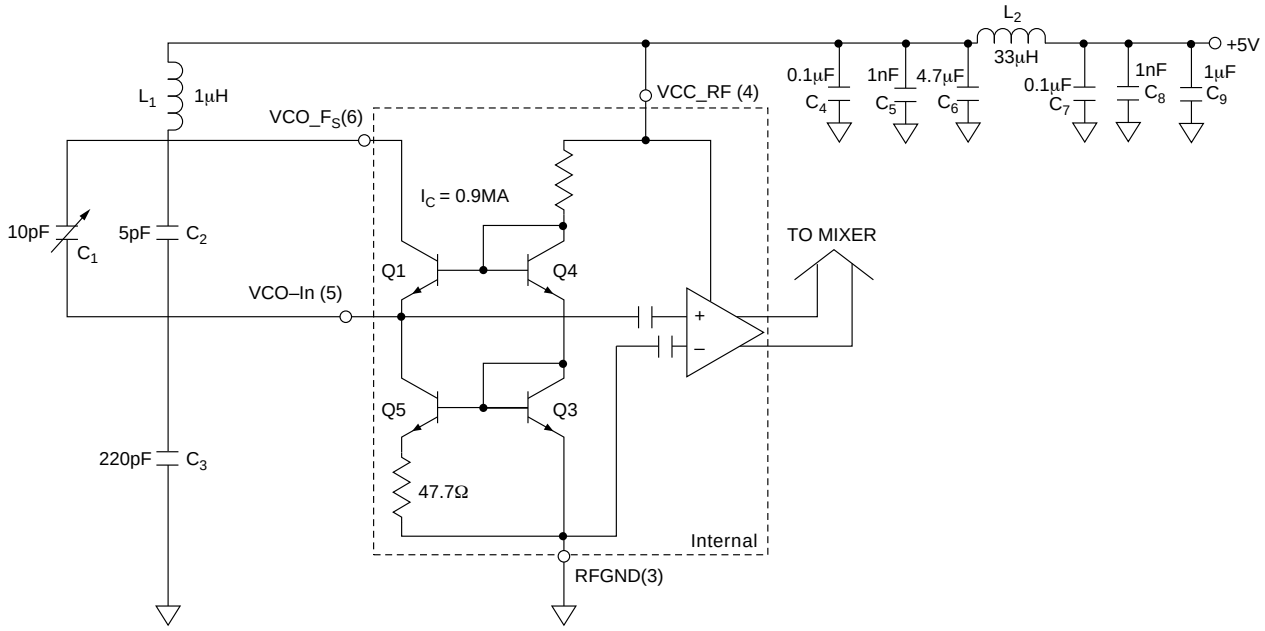


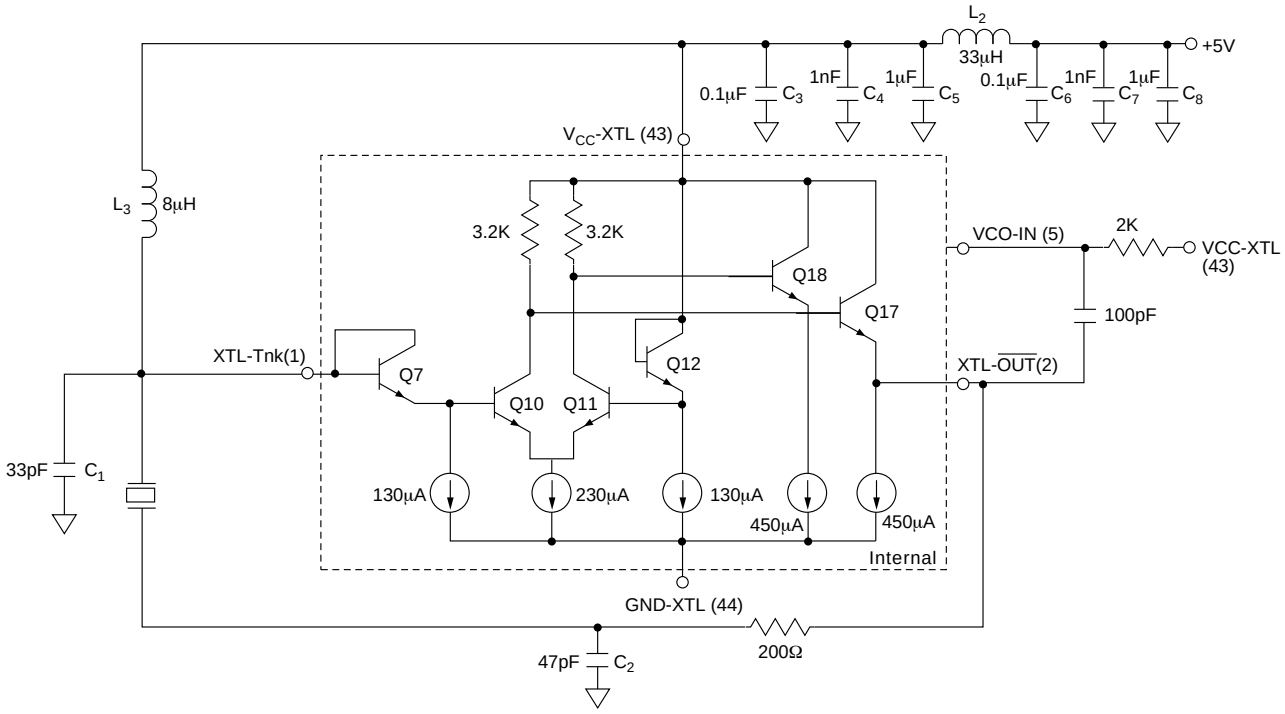
Figure 4. Application of RC6564A in Cable Modem Receivers (Fairchild Semiconductor Demo Board with 64 QAM demodulator)

VCO Internal Schematic



The VCO can be designed as a Colpitts oscillator. The above circuit application shows VCO with adjustable typical value of 38.75 MHz. The frequency is controlled by the external resonance circuit. The oscillating transistor is Q1 in common base configuration. To inject signal in the mixer in place of LO, the VCO_Fs must be open. The signal on the pin VCO_In should be under 100mVp-p and AC coupled.

Crystal Oscillator Internal Schematic



The crystal oscillator is an ECL inverter. It is necessary to bias the XTL-Tnk with a choke to 5V VCC_XTL power supply. The output is about 0.7V DC lower than VCC_XTL with an approximate swing of 0.5Vpp at the output. If the oscillator is not used, it is good to ground XTL_Tnk pin.

Logic Feedthrough

The Logic Feedthrough in the IF section can be minimized by taking the following precautions:

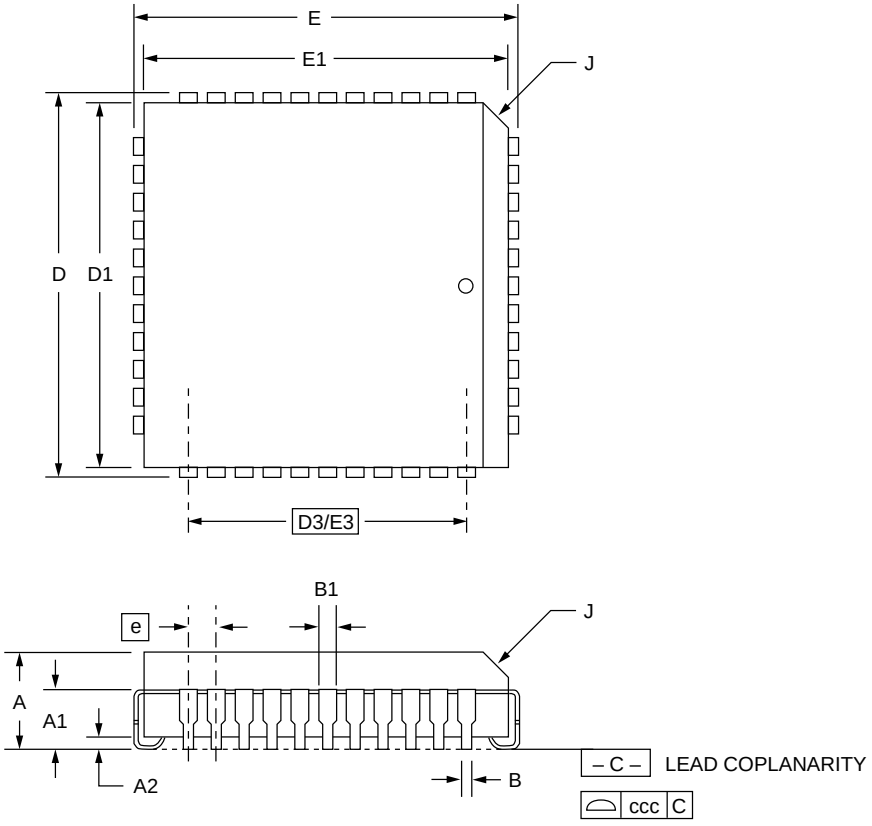
1. It is recommended to have a separate isle for the IF section and the A/D section.
2. All logic circuits in the neighborhood of RC6564A must be isolated. This can be accomplished by carefully decoupling all power supplies and all logic layout signals.
3. It is recommended to have as much ground plane as possible on the top and bottom of the board.

Mechanical Dimensions – 44-Lead PLCC (QB) Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.05	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.685	.695	17.40	17.65	
D1/E1	.650	.656	16.51	16.66	3
D3/E3	.500 BSC		12.7 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.056	1.07	1.42	2
ND/NE	11		11		
N	44		44		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Corner and edge chamfer (J) = 45°
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm)



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC6564AV	0 °C – 70 °C	Commercial	44-Lead PLCC	RC6564AV

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