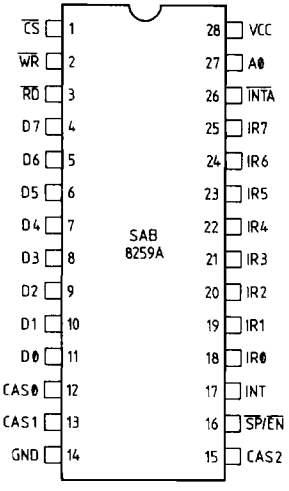
SAB 8259A, SAB 8259A-2 Programmable Interrupt Controller

- Compatible with SAB 8086/88, SAB 80186/188 and SAB 80286 processor families
- Eight-level priority controller
- Expandable to 64 levels
- Programmable interrupt modes
- Individual request mask capability
- Single +5 V supply (no clocks)
- 28-pin dual-in-line package

Pin Configuration



Pin Names

D7-D0	Data Bus (Bidirectional)
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A0	Command Select Address
$\overline{CS}$	Chip Select
CAS2-CAS0	Cascade Lines
$\overline{SP}/\overline{EN}$	Slave Programm/Enable Buffer
INT	Interrupt Output
$\overline{INTA}$	Interrupt Acknowledge Input
IR0-IR7	Interrupt Request Inputs

The SAB 8259A programmable interrupt controller handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without requiring additional circuitry. The SAB 8259A is fabricated in +5 V advanced N-channel, silicon gate Siemens MYMOS technology and packaged in a 28-pin DIP. The circuitry is static, requiring no clock input.

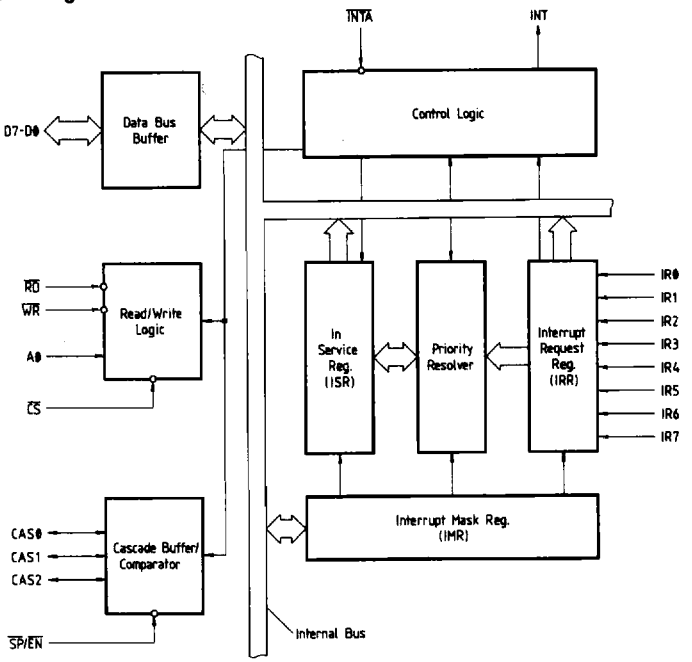
The SAB 8259A is designed to minimize the software and real-time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

Pin Definitions and Functions

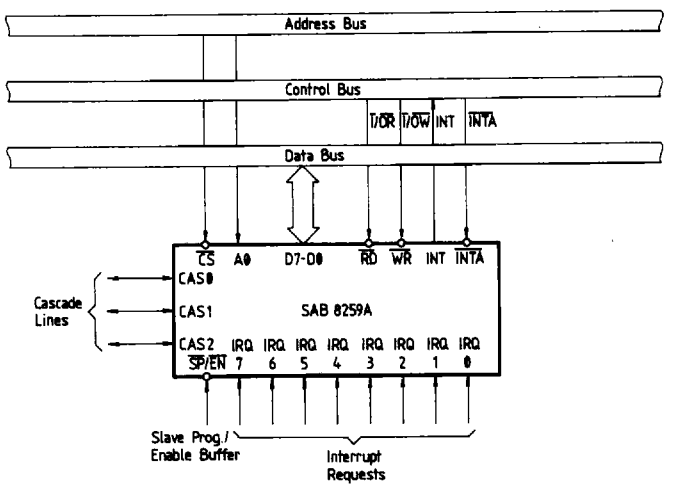
Symbol	Pin	Input (I) Output (O)	Function
$\overline{CS}$	1	I	CHIP SELECT A low on this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the SAB 8259A. $\overline{INTA}$ functions are independent of $\overline{CS}$.
$\overline{WR}$	2	I	$\overline{WRITE}$ A low on this pin when $\overline{CS}$ is low, enables the SAB 8259A to accept command words from the CPU.
$\overline{RD}$	3	I	$\overline{READ}$ A low on this pin when $\overline{CS}$ is low, enables the SAB 8259A to release status onto the data bus for the CPU.
D7-D0	4-11	I/O	BIDIRECTIONAL DATA BUS Control, status and interrupt vector information is transferred via this bus.
CAS0-CAS1	12, 13, 15	I/O	CASCADE LINES The CAS lines form a private SAB 8259A bus to control a multiple SAB 8259A structure. These pins are outputs for a master SAB 8259A and inputs for a slave SAB 8259A.
$\overline{SP/EN}$	16	I/O	$\overline{SLAVE\ PROGRAM/ENABLE\ BUFFER}$ This is a dual function pin. When in buffered mode it can be used as an output to control buffer transceivers (EN). When not in buffered mode it is used as an input to designate a master (SP = 1) or slave (SP = 0).
INT	17	O	INTERRUPT [1] This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
IR0-IR7	18-25	I	INTERRUPT REQUESTS Asynchronous inputs. An interrupt request can be generated by raising an IR input (low to high) and holding it high until it is acknowledged (edge triggered mode), or just by a high level on an IR input (level triggered mode).
$\overline{INTA}$	26	I	$\overline{INTERRUPT\ ACKNOWLEDGE}$ This pin is used to enable SAB 8259A interrupt-vector data onto the data bus. This is done by a sequence of interrupt acknowledge pulses issued by the CPU.
A0	27	I	A0 ADDRESS LINE This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ pins. It is used by the SAB 8259A to destinguish between various command words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A0 address line (A1 for SAB 8086/80186/80286).
VCC	28	I	POWER SUPPLY (+5 V)
GND	14	I	GROUND (0 V)

[1] An active low signal on $\overline{WR}$ during an INT high signal may force INT to low.

Functional Block Diagram



Interface to Standard System Bus



Functional Description

General

The SAB 8259A is a device specifically designed for use in real-time, interrupt-driven microcomputer systems. It manages eight levels or requests and has built-in features for expandability to other SAB 8259A's (up to 64 levels). It is programmed by the system's software as an I/O peripheral.
A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the SAB 8259A can be configured to match his system requirements. The priority modes can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment.

Interrupt Request Register (IRR) and In-Service Register (ISR)

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels which are requesting service, and the ISR is used to store all the interrupt levels which are being serviced.

Priority Resolver

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during an $\overline{INTA}$ pulse.

Interrupt Mask Register (IMR)

The IMR stores the bits which mask the interrupt lines to be masked. The IMR operates on the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

INT (Interrupt)

This output goes directly to the CPU interrupt input. The VOH level on this line is designed to be fully compatible with the SAB 8080A/8085A/8086/8088/80186/80188/80286.

$\overline{INTA}$ (Interrupt Acknowledge)

$\overline{INTA}$ pulses will cause the SAB 8259A to release vectoring information onto the data bus. The format of this data depends on the system mode (μPM) of the SAB 8259A.

Data Bus Buffer

This tristate, bidirectional 8-bit buffer is used to interface the SAB 8259A to the system data bus. Control words and status information are transferred through the data bus buffer.

Read/Write Control Logic

The function of this block is to accept output commands from CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the SAB 8259A to be transferred onto the data bus.

$\overline{CS}$ (Chip Select)

A low on this input enables the SAB 8259A. No reading or writing of the chip will occur unless the device is selected.

$\overline{WR}$ (Write)

A low on this input enables the CPU to write control words (ICWs and OCWs) to the SAB 8259A.

$\overline{RD}$ (Read)

A low on this input enables the SAB 8259A to send the status of the Interrupt Request Register (IRR), In-Service Register (ISR), the Interrupt Mask Register (IMR), or the interrupt level onto the data bus.

A0

This input signal is used in conjunction with $\overline{WR}$ and $\overline{RD}$ signals to write commands into the various command registers, as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.

The Cascade Buffer/Comparator

This function block stores and compares the IDs of all SAB 8259As used in the system. The associated three I/O pins (CAS0-2) are outputs when the SAB 8259A is used as a master and are inputs when the SAB 8259A is used as a slave. As a master, the SAB 8259A sends the ID of the interrupting slave device onto the CAS0-2 lines. The slave thus selected will send its preprogrammed subroutine address onto the data bus during the next one or two consecutive $\overline{INTA}$ pulses.

Interrupt Sequence

The powerful features of the SAB 8259A in a microcomputer system are its programmability and the interrupt routine addressing capability. The latter allows direct or indirect jumping to the specific interrupt routine requested without any polling of the interrupting devices. The normal sequence of events during an interrupt depends on the type of CPU being used.

The events occur as follows in an SAB 8080/85 system:

1. One or more of the INTERRUPT REQUEST lines (IR7-0) are raised high, setting the corresponding IRR bit(s).
2. The SAB 8259A evaluates these requests, and sends an INT to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an $\overline{\text{INTA}}$ pulse.
4. Upon receiving an $\overline{\text{INTA}}$ from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The SAB 8259A will also release a CALL instruction code (11001101) onto the 8-bit data bus through its D7-0 pins.
5. This CALL instruction will initiate two more $\overline{\text{INTA}}$ pulses to be sent to the SAB 8259A from the CPU group.
6. These two $\overline{\text{INTA}}$ pulses allow the SAB 8259A to release its preprogrammed subroutine address onto the data bus. The lower 8-bit address is released at the first $\overline{\text{INTA}}$ pulse and the higher 8-bit address is released at the second $\overline{\text{INTA}}$ pulse.
7. This completes the 3-byte CALL instruction released by the SAB 8259A. In the AEOI[1] mode the ISR bit is reset at the end of the third $\overline{\text{INTA}}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

The events occurring in an SAB 8086/8088/80186/80188/80286 system are the same until step 4.

4. Upon receiving an $\overline{\text{INTA}}$ from the CPU group, the highest priority ISR bit is set and the corresponding IRR bit is reset. The SAB 8259A does not drive the data bus during this cycle.
5. The CPU will initiate a second $\overline{\text{INTA}}$ pulse. During this pulse, the SAB 8259A releases an 8-bit pointer onto the data bus where it is read by the CPU.
6. This completes the interrupt cycle. In the AEOI mode the ISR bit is reset at the end of the second $\overline{\text{INTA}}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

If no interrupt request is present at step 4 of either sequence (i.e. the request was too short in duration) the SAB 8259A will issue an interrupt level 7. Both the vectoring bytes and the CAS lines will look like an interrupt level 7 was requested.

[1] Automatic End of Interrupt

Absolute Maximum Ratings [1]

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground	−0.5 to 7V
Power dissipation	1W

DC Characteristics

TA = 0 to 70°C; VCC = 5V ±10%

Symbol	Parameter	Limit values		Unit	Test conditions
		min.	max.		
VIL	Input low voltage	−0.5	0.8	V	–
VIH	Input high voltage	2.0	VCC +0.5V		
VOL	Output low voltage	–	0.45		IOL = 2.2 mA
VOH	Output high voltage	2.4	–		IOH = −400 µA
VOH (INT)	Interrupt output high voltage	3.5			IOH = −100 µA
		2.4			IOH = −400 µA
ILI	Input load current	–	±10	µA	0V ≤ VIN ≤ VCC
ILOL	Output leakage current				0.45V ≤ VOUT ≤ VCC
ICC	VCC supply current		85	mA	All outputs open
ILIR	IR input load current		−300	µA	VIN = 0V
			10		VIN = VCC

Capacitance

TA = 25°C; VCC = GND = 0V

Symbol	Parameter	Limit values		Unit	Test conditions
		min.	max.		
CIN	Input capacitance	–	10	pF	fC = 1 MHz
CI/O	I/O capacitance		20		Unmeasured pins returned to GND

[1] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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AC Characteristics

TA = 0 to 70°C; VCC = 5 V ±10%

Timing Requirements

Symbol	Parameter	Limit values				Unit	Test conditions
		SAB 8259A		SAB 8259A-2			
		min.	max.	min.	max.		
TAHRL	A0/$\overline{CS}$ setup to $\overline{RD}$/$\overline{INTA}\downarrow$	0		0			
TRHAX	A0/$\overline{CS}$ hold after $\overline{RD}$/$\overline{INTA}\uparrow$						
TRLRH	$\overline{RD}$ pulse width	235		160			
TAHWL	A0/$\overline{CS}$ setup to $\overline{WR}\downarrow$	0		0			–
TWHAX	A0/$\overline{CS}$ hold after $\overline{WR}\uparrow$						
TWLWH	$\overline{WR}$ pulse width	290		190			
TDVWH	Data setup to $\overline{WR}\uparrow$	240		160			
TWHDX	Data hold after $\overline{WR}\uparrow$	0		0			
TJLJH	Interrupt request width (low)	100		100			[1]
TCVIAL	Cascade setup to second or third $\overline{INTA}\downarrow$ (slave only)	55	–	40	–	ns	
TRHRL	End of $\overline{RD}$ to next $\overline{RD}$ End of $\overline{INTA}$ to next $\overline{INTA}$ within an $\overline{INTA}$ sequence only	160		160			–
TWHRL	End of $\overline{WR}$ to next $\overline{WR}$	190		190			
TCHCL [2]	End of command to next command (not same command type)	210		210			
	End of $\overline{INTA}$ sequence to next $\overline{INTA}$ sequence	500		500			

Timing Responses

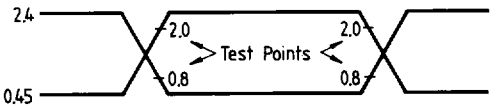
Symbol	Parameter	Limit values				Unit	Test conditions
		SAB 8259A		SAB 8259A-2			
		min.	max.	min.	max.		
TRLDV	Data valid from $\overline{RD}$/$\overline{INTA}\downarrow$	–	200	–	120		C of data bus:
TRHDZ	Data float after $\overline{RD}$/$\overline{INTA}\uparrow$	10	100	10	85		max. test C =
TJHIH	Interrupt output delay		350		300		100 pF
TIALCV	Cascade valid from first $\overline{INTA}\downarrow$ (master only)		565		360		min. test C = 15 pF
TRLEL	Enable active from $\overline{RD}\downarrow$ or $\overline{INTA}\downarrow$	–	125	–	100	ns	CINT = 100 pF
TRHEH	Enable inactive from $\overline{RD}\uparrow$ or $\overline{INTA}\uparrow$		150		150		C cascade = 100 pF
TAHDV	Data valid from stable address		200		200		
TCVDV	Cascade valid to valid data		300				

[1] This is the low time required to clear the input latch in the edge-triggered mode.

[2] Worst-case timing for TCHCL in an actual microprocessor system is typically much greater than 500 ns.

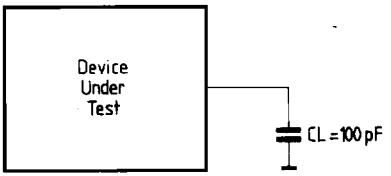
AC Testing Input, Output Waveform

Input/Output



AC testing: inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

AC Testing Load Circuit



CL includes jig capacitance

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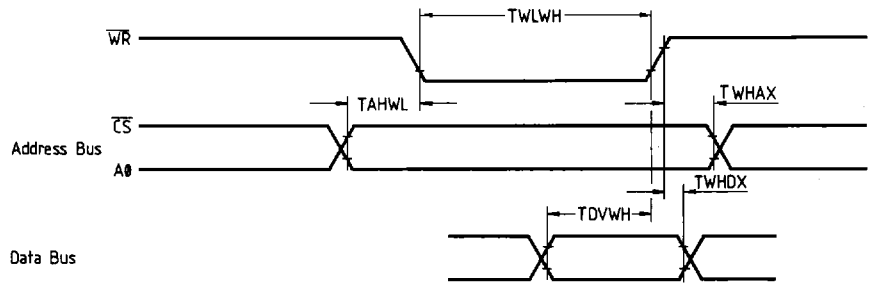
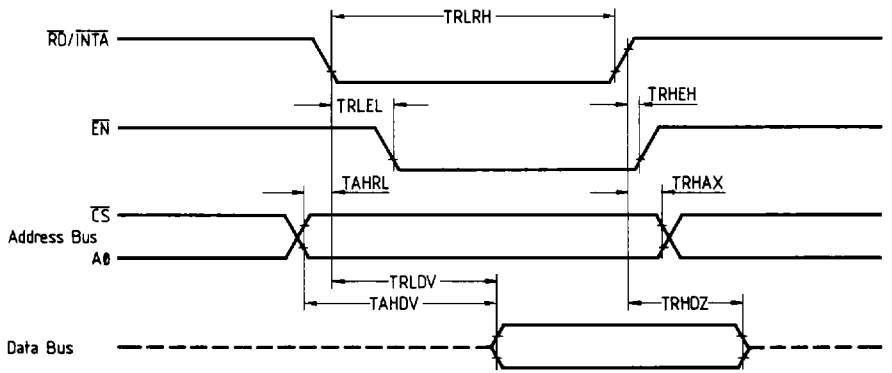
Waveforms

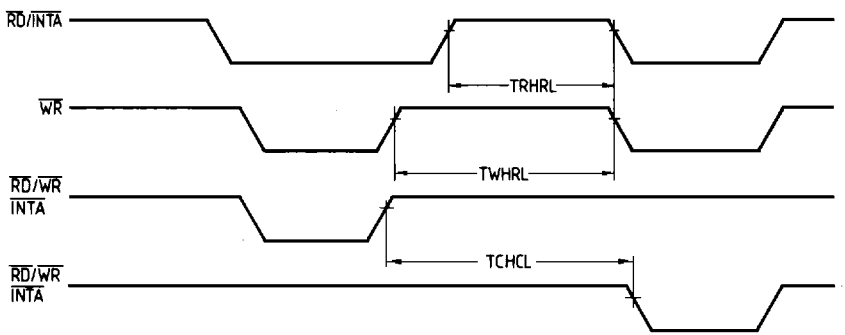
Write



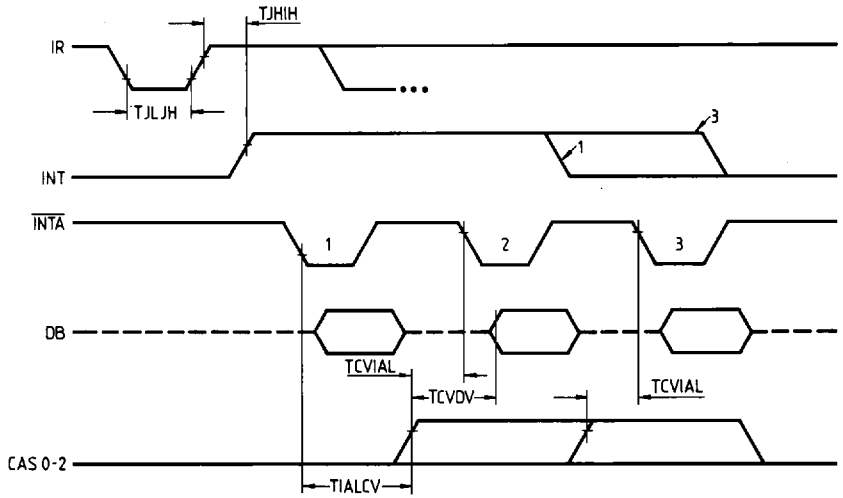
Read/INTA



Other Timings



$\overline{\text{INTA}}$ Sequence



Notes: Interrupt output must remain high at least until leading edge of first $\overline{\text{INTA}}$.
[1]) Cycle 1 in SAB 8086/88 systems, the data bus is not active.
[2]) Cycle 2.
[3]) Cycle 3 in SAB 8085 systems only.

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