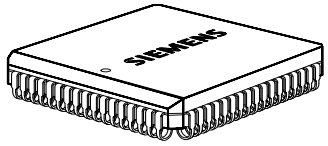
SIEMENS

Triple 8-Bit Analog-to-Digital-Converter SDA 9205-2

Preliminary Data **CMOS IC**

Features

- Three equivalent CMOS A/D converters on chip
- 30-MHz sample rate
- 8-bit resolution
- No external sample & hold required
- On-chip input buffer for each analog channel
- Internal clamping circuits for each of the ADCs
- Different digital output multiplex formats:
  - 3 independent unmultiplexed 8-bit outputs
  - Multiplexed formats compatible to inputs of all Siemens Featureboxes and Siemens TV-SAM
  - CCIR 656 output format
- Overflow and underflow outputs



P-LCC-68-1

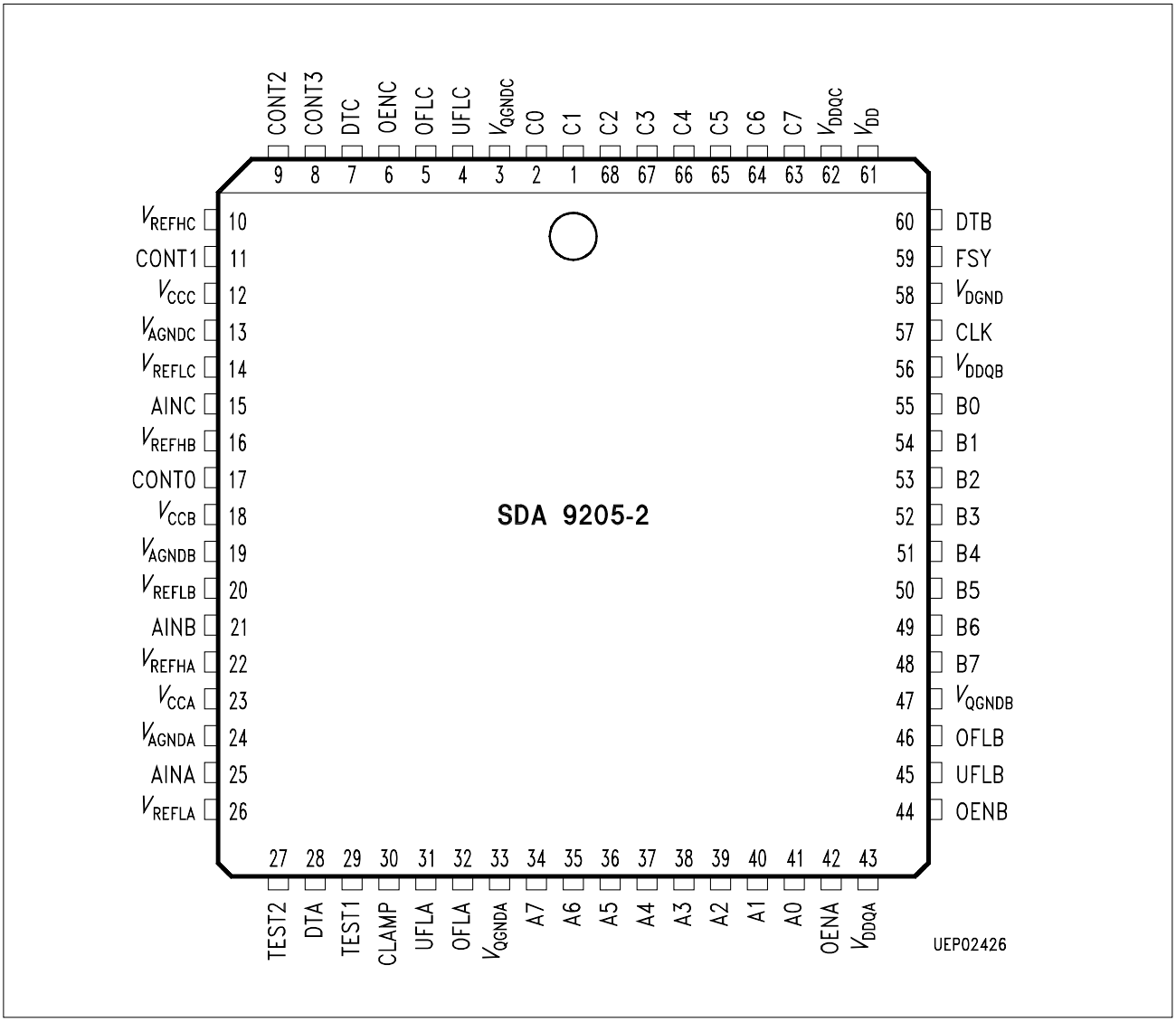
Type	Ordering Code	Package
SDA 9205-2	Q67100-H5069	P-LCC-68-1 (SMD)

General Description

The SDA 9205-2 is a single monolithic IC containing three separate 8-bit analog to digital converters for video (YUV) applications. It utilizes an advanced VLSI 1.2 µm CMOS process providing 30-MHz sampling rates at 8 bits. Different digital output multiplex formats are selectable on chip via several control inputs, compatible to inputs of all Siemens Featureboxes, Siemens TV-SAM, and CCIR 656 output format.

The ADCs have no missing codes over the full operating temperature range of 0 to + 70 °C. Operation is from + 5 V DC-power supply.

Pin Configuration
(top view)



Pin Definitions and Functions

Pin No.	Symbol	Function
63 to 2	C7 to C0	Digital outputs of ADC C (port C) C0 least significant bit
3	V_{QGNDC}	Output stages supply ground of port C
4	UFLC	Underflow data output of ADC C
5	OFLC	Overflow data output of ADC C
6	OENC	Output enable of port C
7	DTC	$\overline{\text{Binary}}$/two's complement output port C
8/9/11/17	CONT3-CONT0	Control inputs for different digital output multiplex formats – refer to logic table
10	V_{REFHC}	Reference voltage high of ADC C (+ 2.5 V)
12	V_{CCC}	Analog positive supply voltage of ADC C (+5 V)
13	V_{AGNDC}	Analog ground of ADC C
14	V_{REFLC}	Reference voltage low of ADC C (+ 5 V)
15	AINC	Analog voltage input of ADC C
16	V_{REFHB}	Reference voltage high of ADC B (+ 2.5 V)
18	V_{CCB}	Analog positive supply voltage of ADC B (+ 5 V)
19	V_{AGNDB}	Analog ground of ADC B
20	V_{REFLB}	Reference voltage low of ADC B (+ 0.5 V)
21	AINB	Analog voltage input of ADC B
22	V_{REFHA}	Reference voltage high of ADC A (+ 2.5 V)
23	V_{CCA}	Analog positive supply voltage of ADC A (+ 5 V)
24	V_{AGNDA}	Analog ground of ADC A
25	AINA	Analog voltage input of ADC A
26	V_{REFLA}	Reference voltage low of ADC A (+ 0.5 V)
27/29	TEST	Factory use only, connect to 0 V
28	DTA	$\overline{\text{Binary}}$/two's complement output of port A
30	CLAMP	Clamp input for all three channels
31	UFLA	Underflow data output of ADC A
32	OFLA	Overflow data output of ADC A
33	V_{QGNDA}	Output stages supply ground of port A
34 to 41	A7 to A0	Digital outputs of ADC A (port A) A0 least significant bit
42	OENA	Output enable of port A
43	V_{DDQA}	Output stages supply voltage of port A

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Function
44	OENB	Output enable of port B
45	UFLB	Underflow data output of ADC B
46	OFLB	Overflow data output of ADC B
47	V_{QGNDB}	Output stages supply ground of port B
48 to 55	B7 to B0	Digital outputs of ADC B (port B) B0 least significant bit
56	V_{DDQB}	Output stages supply voltage of port B
57	CLK	Clock input
58	V_{DGND}	Digital ground
59	FSY	Format sync input
60	DTB	$\overline{\text{Binary}}$/two's complement output of port B
61	V_{DD}	Digital positive supply voltage (+ 5 V)
62	V_{DDQC}	Output stages supply voltage of port C

Circuit Description

Analog to Digital Converter

The SDA 9205-2 implements 3 independent 8-bit analog-to-digital converters.

They are two step converters with a coarse comparator block and two fine comparator blocks each using pipeline architecture for high speed sampling performance. During the first clock cycle, the coarse comparator samples and determines 4 MSBs and one of the fine comparator blocks samples the input voltage. During the second clock cycle this fine comparator block makes its decision for the 4 LSBs. So the coarse comparator block makes its decisions at each clock cycle, the fine comparator blocks make the comparison alternating every two clock cycles.

The converter uses the redundancy principle to correct fine conversion. The sample and hold function has been distributed in each comparator due to the two step conversion principle.

Clamping

An internal clamping circuit is provided in each of three analog channels. The analog pins AINA, AINB, AINC are switched simultaneously to on chip generated clamping levels by an active high pulse on pin 30 (CLAMP).

Clamping Levels

Analog Channel	Dual Code	Components
AINA	00010000	(Y)
AINB, AINC	10000000	(U, V)

The external clamping capacitance is loaded by on chip current sources (typ. 200 µA) during clamping. So the loading time depends on the values of $C_{ext\ cl}$.

The loading time for a complete loading cycle is 1200 CLK pulses typical (44 µs with 27 MHz CLK and $C_{ext\ cl}$ = 10 nF) as shown in **figure 1**.

$C_{ext\ cl}$ = 10 nF, R_S = 50 Ω

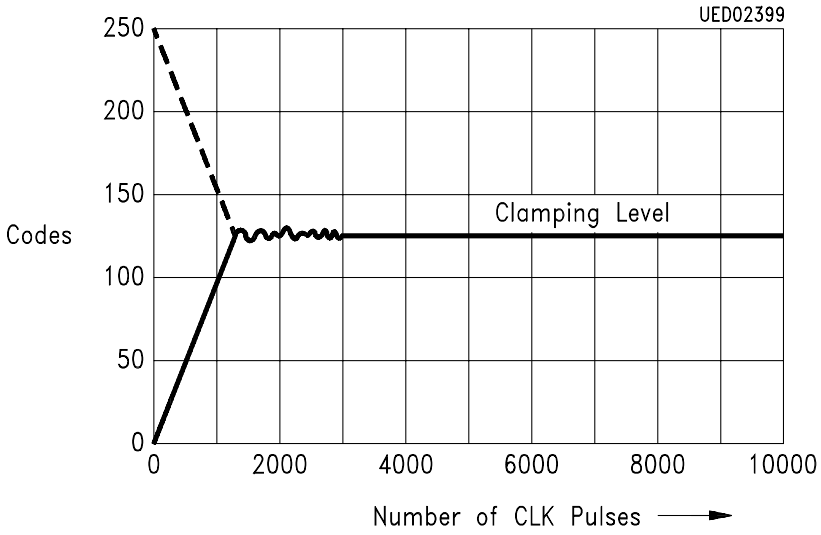


Figure 1
Typical Clamp Timing Diagram

Digital Signal Processing

The digital signal processing block performs averaging of sampled data. The α, β, γ 8-bit busses represent the results of DSP function with input data from a, b, c, 8-bit busses. A special DSP function in combination with a special output coding format is defined by four control pins CONT0 … CONT3 (see Output Coding).

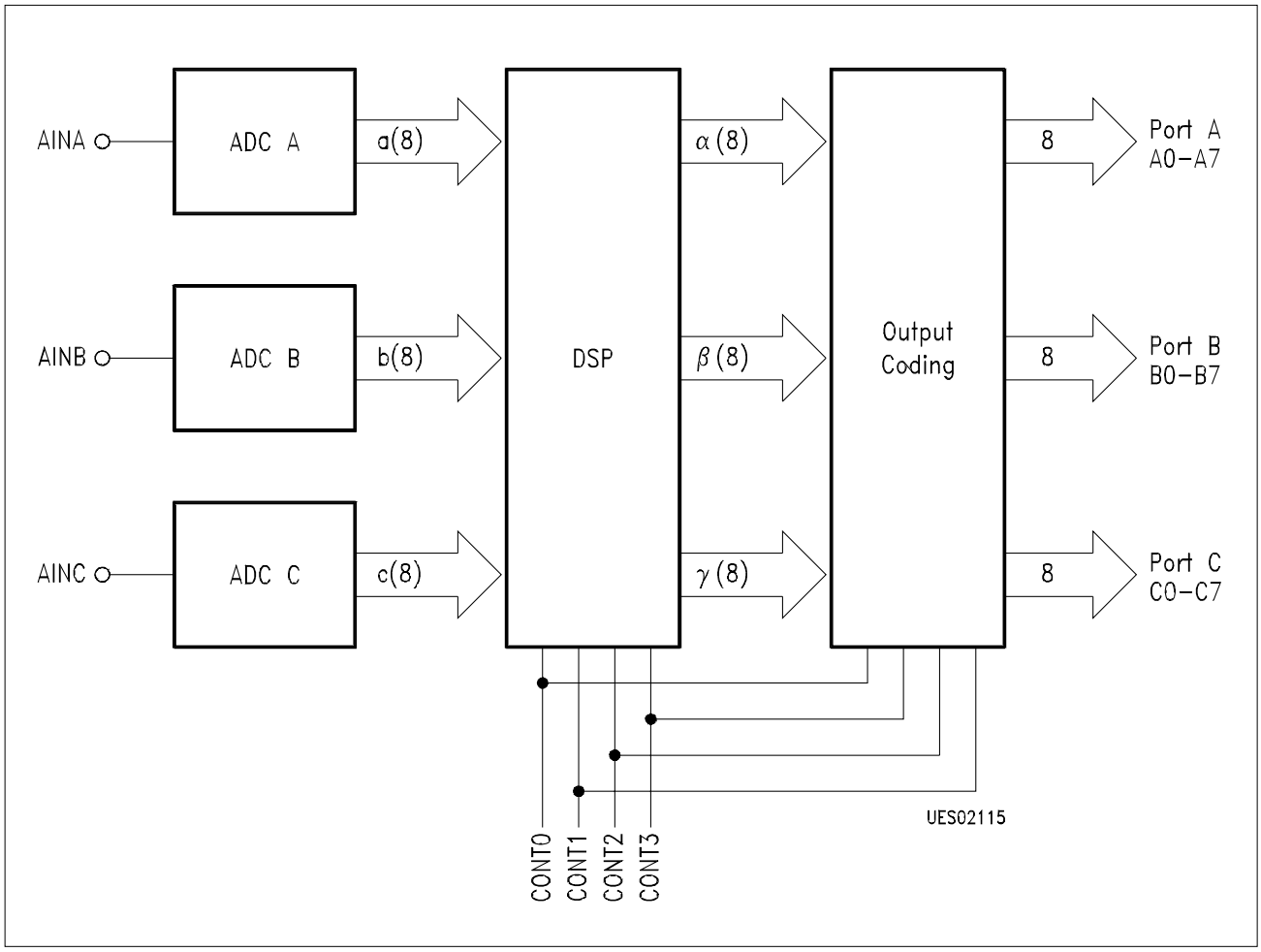


Figure 2
Interfaces of ADC-, DSP- and Output Coding Block

The following DSP functions are available

(1.0)	$\alpha_n = a_{n-3}$			**ADC A**
(1.1)	$\alpha_n = 1/2\ (a_{n-4} + a_{n-3})$	n = sampling point		
(2.0)	$\beta_n = b_{n-3}$			**ADC B**
(2.1)	$\beta_n = 1/2\ (b_{n-4} + b_{n-3})$			
(2.2)	$\beta_{4n} = 1/4\ (b_{4n-5} + b_{4n-4} + b_{4n-3} + b_{4n-2n})$,	$\beta_{4n-3,2,1}$	arbitrarily	
(2.3)	$\beta_{8n} = 1/8\ (b_{8n-7} + b_{8n-6} + ... + b_{8n})$,	$\beta_{8n-7,6,5,4,3,2,1}$	arbitrarily	
(2.0)	$\gamma_n = c_{n-3}$			**ADC C**
(2.1)	$\gamma_n = 1/2\ (c_{n-4} + c_{n-3})$			
(2.2)	$\gamma_{4n} = 1/4\ (c_{4n-5} + c_{4n-4} + c_{4n-3} + c_{4n-2})$	$\gamma_{4n-3,2,1}$	arbitrarily	
(2.3)	$\gamma_{8n} = 1/8\ (c_{8n-7} + c_{8n-6} + ... + c_{8n})$	$\gamma_{8n-7,6,5,4,3,2,1}$	arbitrarily	

Averaged results are rounded to eight bits ($X \leq 0.5 \rightarrow 0$; $X > 0.5 \rightarrow 1$)

A group delay of 0.5 CLK cycles exists between DSP (1.0, 2.0) and the other DSP functions.

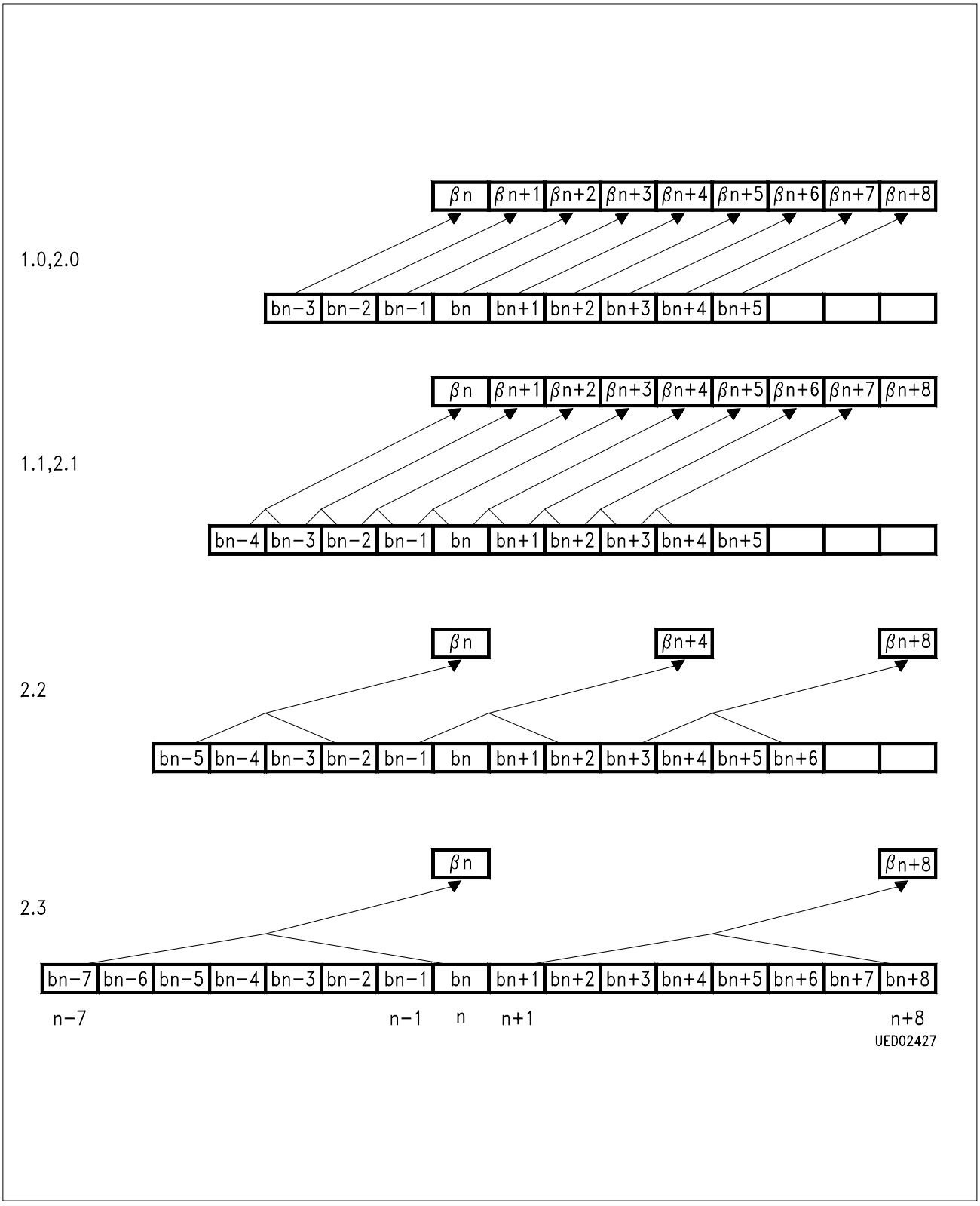


Figure 3
DSP Function

Detailed function of DSP block is shown in **figure 3**.

Output Coding

Eight different digital output multiplex formats are available. They are selectable via four control lines CONT0 … CONT3. These multiplexed formats perform combinations of DSP functions of the several converters (A, B, C).

DSP functions – output coding combinations

Format	DSP	CONT3	CONT2	CONT1	CONT0
8:8:8	1.0 + 2.0	0	0	0	0
	1.1 + 2.1	0	0	0	1
8:4:4	1.0 + 2.0	0	0	1	0
	1.1 + 2.1	0	0	1	1
8:2:2	1.0 + 2.0	0	1	0	0
	1.1 + 2.2	0	1	0	1
8:1:1	1.0 + 2.0	0	1	1	0
	1.1 + 2.3	0	1	1	1
4:8:8	1.0 + 2.0	1	0	0	0
	1.1 + 2.1	1	0	0	1
4:4:4	1.0 + 2.0	1	0	1	0
	1.1 + 2.1	1	0	1	1
4:2:2	1.0 + 2.0	1	1	0	0
	1.1 + 2.2	1	1	0	1
4:1:1	1.0 + 2.0	1	1	1	0
	1.1 + 2.3	1	1	1	1

The digital output data are synchronized by the FSY signal. The first high of FSY defines the first output format byte and is synchronized to CLK. In case of asynchronism the first (in formats 8:1:1, 4:1:1 the first and the second) output format byte after FSY had gone high does not contain valid data. Timing of FSY, CLK and output data is shown in **figure 4** with output format 4:1:1.

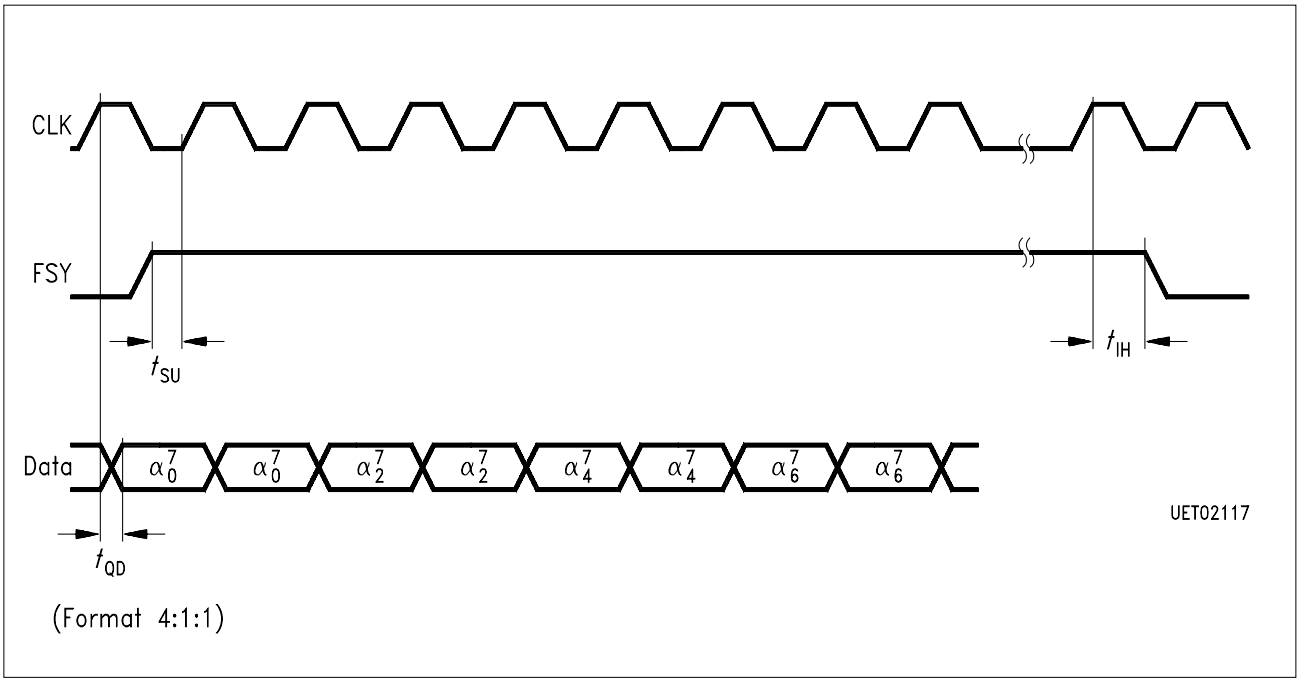
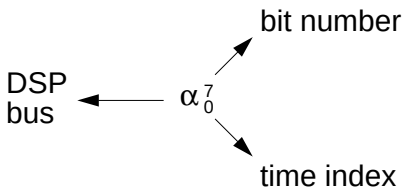


Figure 4

Format 8:8:8

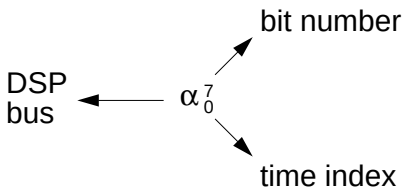
DSP Function	Coding			
	CONT3	CONT2	CONT1	CONT0
1.0 + 2.0	0	0	0	0
1.1 + 2.1	0	0	0	1



Port	Bit	Data							
A	A7	α_0^7	α_1^7	α_2^7	α_3^7	α_4^7	α_5^7	α_6^7	α_7^7
	A6	α_0^6	α_1^6	α_2^6	α_3^6	α_4^6	α_5^6	α_6^6	α_7^6
	A5	α_0^5	α_1^5	α_2^5	α_3^5	α_4^5	α_5^5	α_6^5	α_7^5
	A4	α_0^4	α_1^4	α_2^4	α_3^4	α_4^4	α_5^4	α_6^4	α_7^4
	A3	α_0^3	α_1^3	α_2^3	α_3^3	α_4^3	α_5^3	α_6^3	α_7^3
	A2	α_0^2	α_1^2	α_2^2	α_3^2	α_4^2	α_5^2	α_6^2	α_7^2
	A1	α_0^1	α_1^1	α_2^1	α_3^1	α_4^1	α_5^1	α_6^1	α_7^1
	A0	α_0^0	α_1^0	α_2^0	α_3^0	α_4^0	α_5^0	α_6^0	α_7^0
B	B7	β_0^7	β_1^7	β_2^7	β_3^7	β_4^7	β_5^7	β_6^7	β_7^7
	B6	β_0^6	β_1^6	β_2^6	β_3^6	β_4^6	β_5^6	β_6^6	β_7^6
	B5	β_0^5	β_1^5	β_2^5	β_3^5	β_4^5	β_5^5	β_6^5	β_7^5
	B4	β_0^4	β_1^4	β_2^4	β_3^4	β_4^4	β_5^4	β_6^4	β_7^4
	B3	β_0^3	β_1^3	β_2^3	β_3^3	β_4^3	β_5^3	β_6^3	β_7^3
	B2	β_0^2	β_1^2	β_2^2	β_3^2	β_4^2	β_5^2	β_6^2	β_7^2
	B1	β_0^1	β_1^1	β_2^1	β_3^1	β_4^1	β_5^1	β_6^1	β_7^1
	B0	β_0^0	β_1^0	β_2^0	β_3^0	β_4^0	β_5^0	β_6^0	β_7^0
C	C7	γ_0^7	γ_1^7	γ_2^7	γ_3^7	γ_4^7	γ_5^7	γ_6^7	γ_7^7
	C6	γ_0^6	γ_1^6	γ_2^6	γ_3^6	γ_4^6	γ_5^6	γ_6^6	γ_7^6
	C5	γ_0^5	γ_1^5	γ_2^5	γ_3^5	γ_4^5	γ_5^5	γ_6^5	γ_7^5
	C4	γ_0^4	γ_1^4	γ_2^4	γ_3^4	γ_4^4	γ_5^4	γ_6^4	γ_7^4
	C3	γ_0^3	γ_1^3	γ_2^3	γ_3^3	γ_4^3	γ_5^3	γ_6^3	γ_7^3
	C2	γ_0^2	γ_1^2	γ_2^2	γ_3^2	γ_4^2	γ_5^2	γ_6^2	γ_7^2
	C1	γ_0^1	γ_1^1	γ_2^1	γ_3^1	γ_4^1	γ_5^1	γ_6^1	γ_7^1
	C0	γ_0^0	γ_1^0	γ_2^0	γ_3^0	γ_4^0	γ_5^0	γ_6^0	γ_7^0
Time Index		n	n + 1	n + 2	n + 3	n + 4	n + 5	n + 6	n + 7

Format 8:4:4

DSP Function	Coding			
	CONT3	CONT2	CONT1	CONT0
1.0 + 2.0	0	0	1	0
1.1 + 2.1	0	0	1	0

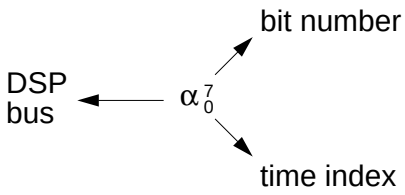


Port	Bit	Data							
A	A7	α_0^7	α_1^7	α_2^7	α_3^7	α_4^7	α_5^7	α_6^7	α_7^7
	A6	α_0^6	α_1^6	α_2^6	α_3^6	α_4^6	α_5^6	α_6^6	α_7^6
	A5	α_0^5	α_1^5	α_2^5	α_3^5	α_4^5	α_5^5	α_6^5	α_7^5
	A4	α_0^4	α_1^4	α_2^4	α_3^4	α_4^4	α_5^4	α_6^4	α_7^4
	A3	α_0^3	α_1^3	α_2^3	α_3^3	α_4^3	α_5^3	α_6^3	α_7^3
	A2	α_0^2	α_1^2	α_2^2	α_3^2	α_4^2	α_5^2	α_6^2	α_7^2
	A1	α_0^1	α_1^1	α_2^1	α_3^1	α_4^1	α_5^1	α_6^1	α_7^1
	A0	α_0^0	α_1^0	α_2^0	α_3^0	α_4^0	α_5^0	α_6^0	α_7^0
B	B7	β_0^7	γ_0^7	β_2^7	γ_2^7	β_4^7	γ_4^7	β_6^7	γ_6^7
	B6	β_0^6	γ_0^6	β_2^6	γ_2^6	β_4^6	γ_4^6	β_6^6	γ_6^6
	B5	β_0^5	γ_0^5	β_2^5	γ_2^5	β_4^5	γ_4^5	β_6^5	γ_6^5
	B4	β_0^4	γ_0^4	β_2^4	γ_2^4	β_4^4	γ_4^4	β_6^4	γ_6^4
	B3	β_0^3	γ_0^3	β_2^3	γ_2^3	β_4^3	γ_4^3	β_6^3	γ_6^3
	B2	β_0^2	γ_0^2	β_2^2	γ_2^2	β_4^2	γ_4^2	β_6^2	γ_6^2
	B1	β_0^1	γ_0^1	β_2^1	γ_2^1	β_4^1	γ_4^1	β_6^1	γ_6^1
	B0	β_0^0	γ_0^0	β_2^0	γ_2^0	β_4^0	γ_4^0	β_6^0	γ_6^0
C	C7	T	T	T	T	T	T	T	T
	C6	T	T	T	T	T	T	T	T
	C5	T	T	T	T	T	T	T	T
	C4	T	T	T	T	T	T	T	T
	C3	T	T	T	T	T	T	T	T
	C2	T	T	T	T	T	T	T	T
	C1	T	T	T	T	T	T	T	T
	C0	T	T	T	T	T	T	T	T*
Time Index		n	n + 1	n + 2	n + 3	n + 4	n + 5	n + 6	n + 7

* T … Tristate

Format 8:2:2

DSP Function	Coding			
	CONT3	CONT2	CONT1	CONT0
1.0 + 2.0	0	1	0	0
1.1 + 2.2	0	1	0	1

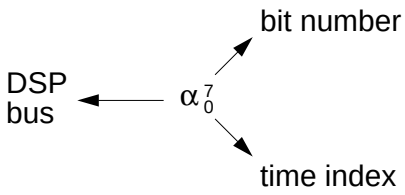


Port	Bit	Data							
A	A7	α_0^7	α_1^7	α_2^7	α_3^7	α_4^7	α_5^7	α_6^7	α_7^7
	A6	α_0^6	α_1^6	α_2^6	α_3^6	α_4^6	α_5^6	α_6^6	α_7^6
	A5	α_0^5	α_1^5	α_2^5	α_3^5	α_4^5	α_5^5	α_6^5	α_7^5
	A4	α_0^4	α_1^4	α_2^4	α_3^4	α_4^4	α_5^4	α_6^4	α_7^4
	A3	α_0^3	α_1^3	α_2^3	α_3^3	α_4^3	α_5^3	α_6^3	α_7^3
	A2	α_0^2	α_1^2	α_2^2	α_3^2	α_4^2	α_5^2	α_6^2	α_7^2
	A1	α_0^1	α_1^1	α_2^1	α_3^1	α_4^1	α_5^1	α_6^1	α_7^1
	A0	α_0^0	α_1^0	α_2^0	α_3^0	α_4^0	α_5^0	α_6^0	α_7^0
B	B7	β_0^7	β_0^5	β_0^3	β_0^1	β_4^7	β_4^5	β_4^3	β_4^1
	B6	β_0^6	β_0^4	β_0^2	β_0^0	β_4^6	β_4^4	β_4^2	β_4^0
	B5	γ_0^7	γ_0^5	γ_0^3	γ_0^1	γ_4^7	γ_4^5	γ_4^3	γ_4^1
	B4	γ_0^6	γ_0^4	γ_0^2	γ_0^0	γ_4^6	γ_4^4	γ_4^2	γ_4^0
	B3	T	T	T	T	T	T	T	T
	B2	T	T	T	T	T	T	T	T
	B1	T	T	T	T	T	T	T	T
	B0	T	T	T	T	T	T	T	T
C	C7	T	T	T	T	T	T	T	T
	C6	T	T	T	T	T	T	T	T
	C5	T	T	T	T	T	T	T	T
	C4	T	T	T	T	T	T	T	T
	C3	T	T	T	T	T	T	T	T
	C2	T	T	T	T	T	T	T	T
	C1	T	T	T	T	T	T	T	T
	C0	T	T	T	T	T	T	T	T*
Time Index		n	n + 1	n + 2	n + 3	n + 4	n + 5	n + 6	n + 7

* T … Tristate

Format 8:1:1

DSP Function	Coding			
	CONT3	CONT2	CONT1	CONT0
1.0 + 2.0	0	1	1	0
1.1 + 2.3	0	1	1	1

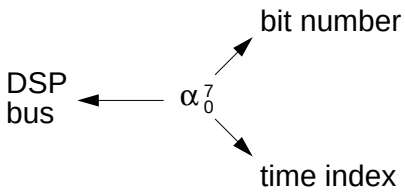


Port	Bit	Data							
A	A7	α_0^7	α_1^7	α_2^7	α_3^7	α_4^7	α_5^7	α_6^7	α_7^7
	A6	α_0^6	α_1^6	α_2^6	α_3^6	α_4^6	α_5^6	α_6^6	α_7^6
	A5	α_0^5	α_1^5	α_2^5	α_3^5	α_4^5	α_5^5	α_6^5	α_7^5
	A4	α_0^4	α_1^4	α_2^4	α_3^4	α_4^4	α_5^4	α_6^4	α_7^4
	A3	α_0^3	α_1^3	α_2^3	α_3^3	α_4^3	α_5^3	α_6^3	α_7^3
	A2	α_0^2	α_1^2	α_2^2	α_3^2	α_4^2	α_5^2	α_6^2	α_7^2
	A1	α_0^1	α_1^1	α_2^1	α_3^1	α_4^1	α_5^1	α_6^1	α_7^1
	A0	α_0^0	α_1^0	α_2^0	α_3^0	α_4^0	α_5^0	α_6^0	α_7^0
B	B7	β_0^7	β_0^7	β_0^5	β_0^5	β_0^3	β_0^3	β_0^1	β_0^1
	B6	β_0^6	β_0^6	β_0^4	β_0^4	β_0^2	β_0^2	β_0^0	β_0^0
	B5	γ_0^7	γ_0^7	γ_0^5	γ_0^5	γ_0^3	γ_0^3	γ_0^1	γ_0^1
	B4	γ_0^6	γ_0^6	γ_0^4	γ_0^4	γ_0^2	γ_0^2	γ_0^0	γ_0^0
	B3	T	T	T	T	T	T	T	T
	B2	T	T	T	T	T	T	T	T
	B1	T	T	T	T	T	T	T	T
	B0	T	T	T	T	T	T	T	T
C	C7	T	T	T	T	T	T	T	T
	C6	T	T	T	T	T	T	T	T
	C5	T	T	T	T	T	T	T	T
	C4	T	T	T	T	T	T	T	T
	C3	T	T	T	T	T	T	T	T
	C2	T	T	T	T	T	T	T	T
	C1	T	T	T	T	T	T	T	T
	C0	T	T	T	T	T	T	T	T*
Time Index		n	n + 1	n + 2	n + 3	n + 4	n + 5	n + 6	n + 7

* T … Tristate

Format 4:8:8

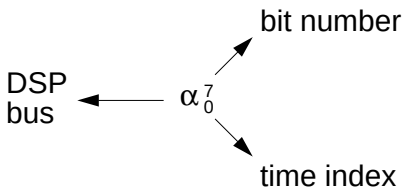
DSP Function	Coding			
	CONT3	CONT2	CONT1	CONT0
1.0 + 2.0	1	0	0	0
1.1 + 2.1	1	0	0	1



Port	Bit	Data							
A	A7	α_0^7	α_0^7	α_2^7	α_2^7	α_4^7	α_4^7	α_6^7	α_6^7
	A6	α_0^6	α_0^6	α_2^6	α_2^6	α_4^6	α_4^6	α_6^6	α_6^6
	A5	α_0^5	α_0^5	α_2^5	α_2^5	α_4^5	α_4^5	α_6^5	α_6^5
	A4	α_0^4	α_0^4	α_2^4	α_2^4	α_4^4	α_4^4	α_6^4	α_6^4
	A3	α_0^3	α_0^3	α_2^3	α_2^3	α_4^3	α_4^3	α_6^3	α_6^3
	A2	α_0^2	α_0^2	α_2^2	α_2^2	α_4^2	α_4^2	α_6^2	α_6^2
	A1	α_0^1	α_0^1	α_2^1	α_2^1	α_4^1	α_4^1	α_6^1	α_6^1
	A0	α_0^0	α_0^0	α_2^0	α_2^0	α_4^0	α_4^0	α_6^0	α_6^0
B	B7	β_0^7	β_1^7	β_2^7	β_3^7	β_4^7	β_5^7	β_6^7	β_7^7
	B6	β_0^6	β_1^6	β_2^6	β_3^6	β_4^6	β_5^6	β_6^6	β_7^6
	B5	β_0^5	β_1^5	β_2^5	β_3^5	β_4^5	β_5^5	β_6^5	β_7^5
	B4	β_0^4	β_1^4	β_2^4	β_3^4	β_4^4	β_5^4	β_6^4	β_7^4
	B3	β_0^3	β_1^3	β_2^3	β_3^3	β_4^3	β_5^3	β_6^3	β_7^3
	B2	β_0^2	β_1^2	β_2^2	β_3^2	β_4^2	β_5^2	β_6^2	β_7^2
	B1	β_0^1	β_1^1	β_2^1	β_3^1	β_4^1	β_5^1	β_6^1	β_7^1
	B0	β_0^0	β_1^0	β_2^0	β_3^0	β_4^0	β_5^0	β_6^0	β_7^0
C	C7	γ_0^7	γ_1^7	γ_2^7	γ_3^7	γ_4^7	γ_5^7	γ_6^7	γ_7^7
	C6	γ_0^6	γ_1^6	γ_2^6	γ_3^6	γ_4^6	γ_5^6	γ_6^6	γ_7^6
	C5	γ_0^5	γ_1^5	γ_2^5	γ_3^5	γ_4^5	γ_5^5	γ_6^5	γ_7^5
	C4	γ_0^4	γ_1^4	γ_2^4	γ_3^4	γ_4^4	γ_5^4	γ_6^4	γ_7^4
	C3	γ_0^3	γ_1^3	γ_2^3	γ_3^3	γ_4^3	γ_5^3	γ_6^3	γ_7^3
	C2	γ_0^2	γ_1^2	γ_2^2	γ_3^2	γ_4^2	γ_5^2	γ_6^2	γ_7^2
	C1	γ_0^1	γ_1^1	γ_2^1	γ_3^1	γ_4^1	γ_5^1	γ_6^1	γ_7^1
	C0	γ_0^0	γ_1^0	γ_2^0	γ_3^0	γ_4^0	γ_5^0	γ_6^0	γ_7^0
Time Index		n	n + 1	n + 2	n + 3	n + 4	n + 5	n + 6	n + 7

Format 4:4:4

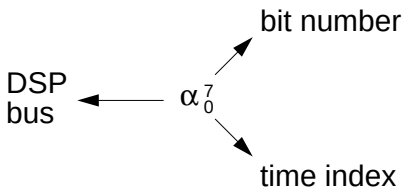
DSP Function	Coding			
	CONT3	CONT2	CONT1	CONT0
1.0 + 2.0	1	0	1	0
1.1 + 2.1	1	0	1	0



Port	Bit	Data							
A	A7	α_0^7	α_0^7	α_2^7	α_2^7	α_4^7	α_4^7	α_6^7	α_6^7
	A6	α_0^6	α_0^6	α_2^6	α_2^6	α_4^6	α_4^6	α_6^6	α_6^6
	A5	α_0^5	α_0^5	α_2^5	α_2^5	α_4^5	α_4^5	α_6^5	α_6^5
	A4	α_0^4	α_0^4	α_2^4	α_2^4	α_4^4	α_4^4	α_6^4	α_6^4
	A3	α_0^3	α_0^3	α_2^3	α_2^3	α_4^3	α_4^3	α_6^3	α_6^3
	A2	α_0^2	α_0^2	α_2^2	α_2^2	α_4^2	α_4^2	α_6^2	α_6^2
	A1	α_0^1	α_0^1	α_2^1	α_2^1	α_4^1	α_4^1	α_6^1	α_6^1
	A0	α_0^0	α_0^0	α_2^0	α_2^0	α_4^0	α_4^0	α_6^0	α_6^0
B	B7	β_0^7	β_0^7	β_2^7	β_2^7	β_4^7	β_4^7	β_6^7	β_6^7
	B6	β_0^6	β_0^6	β_2^6	β_2^6	β_4^6	β_4^6	β_6^6	β_6^6
	B5	β_0^5	β_0^5	β_2^5	β_2^5	β_4^5	β_4^5	β_6^5	β_6^5
	B4	β_0^4	β_0^4	β_2^4	β_2^4	β_4^4	β_4^4	β_6^4	β_6^4
	B3	β_0^3	β_0^3	β_2^3	β_2^3	β_4^3	β_4^3	β_6^3	β_6^3
	B2	β_0^2	β_0^2	β_2^2	β_2^2	β_4^2	β_4^2	β_6^2	β_6^2
	B1	β_0^1	β_0^1	β_2^1	β_2^1	β_4^1	β_4^1	β_6^1	β_6^1
	B0	β_0^0	β_0^0	β_2^0	β_2^0	β_4^0	β_4^0	β_6^0	β_6^0
C	C7	γ_0^7	γ_0^7	γ_2^7	γ_2^7	γ_4^7	γ_4^7	γ_6^7	γ_6^7
	C6	γ_0^6	γ_0^6	γ_2^6	γ_2^6	γ_4^6	γ_4^6	γ_6^6	γ_6^6
	C5	γ_0^5	γ_0^5	γ_2^5	γ_2^5	γ_4^5	γ_4^5	γ_6^5	γ_6^5
	C4	γ_0^4	γ_0^4	γ_2^4	γ_2^4	γ_4^4	γ_4^4	γ_6^4	γ_6^4
	C3	γ_0^3	γ_0^3	γ_2^3	γ_2^3	γ_4^3	γ_4^3	γ_6^3	γ_6^3
	C2	γ_0^2	γ_0^2	γ_2^2	γ_2^2	γ_4^2	γ_4^2	γ_6^2	γ_6^2
	C1	γ_0^1	γ_0^1	γ_2^1	γ_2^1	γ_4^1	γ_4^1	γ_6^1	γ_6^1
	C0	γ_0^0	γ_0^0	γ_2^0	γ_2^0	γ_4^0	γ_4^0	γ_6^0	γ_6^0
Time Index		n	n + 1	n + 2	n + 3	n + 4	n + 5	n + 6	n + 7

Format 4:2:2

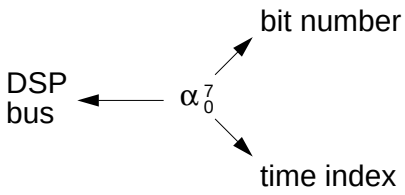
DSP Function	Coding			
	CONT3	CONT2	CONT1	CONT0
1.0 + 2.0	1	1	0	0
1.1 + 2.2	1	1	0	1



Port	Bit	Data							
A	A7	α_0^7	α_0^7	α_2^7	α_2^7	α_4^7	α_4^7	α_6^7	α_6^7
	A6	α_0^6	α_0^6	α_2^6	α_2^6	α_4^6	α_4^6	α_6^6	α_6^6
	A5	α_0^5	α_0^5	α_2^5	α_2^5	α_4^5	α_4^5	α_6^5	α_6^5
	A4	α_0^4	α_0^4	α_2^4	α_2^4	α_4^4	α_4^4	α_6^4	α_6^4
	A3	α_0^3	α_0^3	α_2^3	α_2^3	α_4^3	α_4^3	α_6^3	α_6^3
	A2	α_0^2	α_0^2	α_2^2	α_2^2	α_4^2	α_4^2	α_6^2	α_6^2
	A1	α_0^1	α_0^1	α_2^1	α_2^1	α_4^1	α_4^1	α_6^1	α_6^1
	A0	α_0^0	α_0^0	α_2^0	α_2^0	α_4^0	α_4^0	α_6^0	α_6^0
B	B7	β_0^7	β_0^7	γ_0^7	γ_0^7	β_4^7	β_4^7	γ_4^7	γ_4^7
	B6	β_0^6	β_0^6	γ_0^6	γ_0^6	β_4^6	β_4^6	γ_4^6	γ_4^6
	B5	β_0^5	β_0^5	γ_0^5	γ_0^5	β_4^5	β_4^5	γ_4^5	γ_4^5
	B4	β_0^4	β_0^4	γ_0^4	γ_0^4	β_4^4	β_4^4	γ_4^4	γ_4^4
	B3	β_0^3	β_0^3	γ_0^3	γ_0^3	β_4^3	β_4^3	γ_4^3	γ_4^3
	B2	β_0^2	β_0^2	γ_0^2	γ_0^2	β_4^2	β_4^2	γ_4^2	γ_4^2
	B1	β_0^1	β_0^1	γ_0^1	γ_0^1	β_4^1	β_4^1	γ_4^1	γ_4^1
	B0	β_0^0	β_0^0	γ_0^0	γ_0^0	β_4^0	β_4^0	γ_4^0	γ_4^0
C	C7	β_0^7	α_0^7	γ_0^7	α_2^7	β_4^7	α_4^7	γ_4^7	α_6^7
	C6	β_0^6	α_0^6	γ_0^6	α_2^6	β_4^6	α_4^6	γ_4^6	α_6^6
	C5	β_0^5	α_0^5	γ_0^5	α_2^5	β_4^5	α_4^5	γ_4^5	α_6^5
	C4	β_0^4	α_0^4	γ_0^4	α_2^4	β_4^4	α_4^4	γ_4^4	α_6^4
	C3	β_0^3	α_0^3	γ_0^3	α_2^3	β_4^3	α_4^3	γ_4^3	α_6^3
	C2	β_0^2	α_0^2	γ_0^2	α_2^2	β_4^2	α_4^2	γ_4^2	α_6^2
	C1	β_0^1	α_0^1	γ_0^1	α_2^1	β_4^1	α_4^1	γ_4^1	α_6^1
	C0	β_0^0	α_0^0	γ_0^0	α_2^0	β_4^0	α_4^0	γ_4^0	α_6^0
Time Index		n	n + 1	n + 2	n + 3	n + 4	n + 5	n + 6	n + 7

Format 4:1:1

DSP Function	Coding			
	CONT3	CONT2	CONT1	CONT0
1.0 + 2.0	1	1	1	0
1.1 + 2.3	1	1	1	1



Port	Bit	Data							
A	A7	α_0^7	α_0^7	α_2^7	α_2^7	α_4^7	α_4^7	α_6^7	α_6^7
	A6	α_0^6	α_0^6	α_2^6	α_2^6	α_4^6	α_4^6	α_6^6	α_6^6
	A5	α_0^5	α_0^5	α_2^5	α_2^5	α_4^5	α_4^5	α_6^5	α_6^5
	A4	α_0^4	α_0^4	α_2^4	α_2^4	α_4^4	α_4^4	α_6^4	α_6^4
	A3	α_0^3	α_0^3	α_2^3	α_2^3	α_4^3	α_4^3	α_6^3	α_6^3
	A2	α_0^2	α_0^2	α_2^2	α_2^2	α_4^2	α_4^2	α_6^2	α_6^2
	A1	α_0^1	α_0^1	α_2^1	α_2^1	α_4^1	α_4^1	α_6^1	α_6^1
	A0	α_0^0	α_0^0	α_2^0	α_2^0	α_4^0	α_4^0	α_6^0	α_6^0
B	B7	β_0^7	β_0^7	β_0^5	β_0^5	β_0^3	β_0^3	β_0^1	β_0^1
	B6	β_0^6	β_0^6	β_0^4	β_0^4	β_0^2	β_0^2	β_0^0	β_0^0
	B5	γ_0^7	γ_0^7	γ_0^5	γ_0^5	γ_0^3	γ_0^3	γ_0^1	γ_0^1
	B4	γ_0^6	γ_0^6	γ_0^4	γ_0^4	γ_0^2	γ_0^2	γ_0^0	γ_0^0
	B3	T	T	T	T	T	T	T	T
	B2	T	T	T	T	T	T	T	T
	B1	T	T	T	T	T	T	T	T
	B0	T	T	T	T	T	T	T	T
C	C7	T	T	T	T	T	T	T	T
	C6	T	T	T	T	T	T	T	T
	C5	T	T	T	T	T	T	T	T
	C4	T	T	T	T	T	T	T	T
	C3	T	T	T	T	T	T	T	T
	C2	T	T	T	T	T	T	T	T
	C1	T	T	T	T	T	T	T	T
	C0	T	T	T	T	T	T	T	T*
Time Index		n	n + 1	n + 2	n + 3	n + 4	n + 5	n + 6	n + 7

* T … Tristate

Output Coding for Binary/Two's Complement Mode

Binary or two's complement output coding is selectable for each separate output port (A, B, C) via control inputs DTA, DTB, DTC. This coding is independent from selected formats (8:8:8, 8:4:4, 8:2:2, 8:1:1, 4:8:8, 4:4:4, 4:2:2, 4:1:1).

Table 1
Output Coding for Formats 8:8:8, 8:4:4, 8:2:2, 8:1:1, 4:8:8, 4:4:4, 4:2:2, 4:1:1

Table 1 is valid for V_{REFL} = 0.5 V and V_{REFH} = 2.5 V

Step	VIN Converter A	VIN Converter B, C	OFL Bit	UFL Bit	Binary Output 7 6 5 4 3 2 1 0	Two's Complement 7 6 5 4 3 2 1 0
Underflow	< V_{CA} – 0.125 V	< $V_{CB,C}$ – 1 V	0	1	0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0
0	V_{CA} – 0.125 V	$V_{CB,C}$ – 1 V	0	0	0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0
1	V_{CA} – 0.117 V	$V_{CB,C}$ – 0.992 V	0	0	0 0 0 0 0 0 0 1	1 0 0 0 0 0 0 1
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
254	V_{CA} + 1.867 V	$V_{CB,C}$ + 0.992 V	.	.	1 1 1 1 1 1 1 0	0 1 1 1 1 1 1 0
255	V_{CA} + 1.875 V	$V_{CB,C}$ + 1 V	0	0	1 1 1 1 1 1 1 1	0 1 1 1 1 1 1 1
Overflow	> V_{CA} + 1.875 V	> $V_{CB,C}$ + 1 V	1	0	1 1 1 1 1 1 1 1	0 1 1 1 1 1 1 1

V_{CA} = ext. clamping level during CLAMP high pulse at $C_{ext\ cl}$ on channel AINA.
$V_{CB,C}$ = ext. clamping level during CLAMP high pulse at $C_{ext\ cl}$ on channel AINB and AINC.

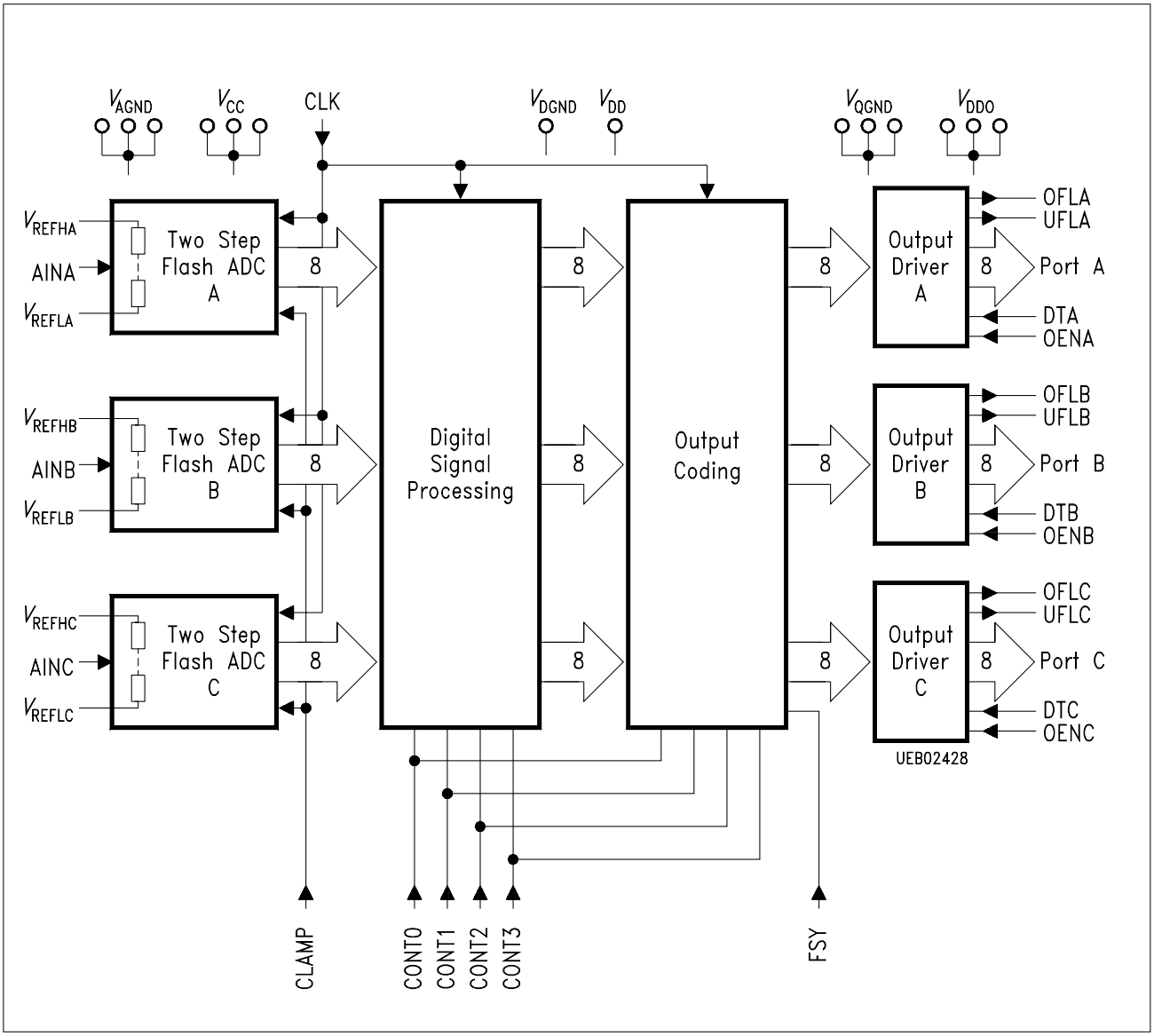
In output format 4:2:2 a special suppression of code 0 and code 255 is provided in the binary output mode.

Table 2
Output Coding for Format 4:2:2

Table 2 is valid for V_{REFL} = 0.5 V and V_{REFH} = 2.5 V

Step	VIN Converter A	VIN Converter B, C	OFL Bit	UFL Bit	Binary Output 7 6 5 4 3 2 1 0	Two's Complement 7 6 5 4 3 2 1 0
Underflow	< V_{CA} – 0.125 V	< $V_{CB, C}$ – 1 V	0	1	0 0 0 0 0 0 0 1	1 0 0 0 0 0 0 0
0	V_{CA} – 0.125 V	$V_{CB, C}$ – 1 V	0	0	0 0 0 0 0 0 0 1	1 0 0 0 0 0 0 0
1	V_{CA} – 0.117 V	$V_{CB, C}$ – 0.992 V	0	0	0 0 0 0 0 0 0 1	1 0 0 0 0 0 0 1
2	.	.	0	.	0 0 0 0 0 0 1 0	1 0 0 0 0 0 1 0
.	.	.	.	.	.	
.	.	.	.	.	.	
253	.	.	0	0	1 1 1 1 1 1 0 1	
254	V_{CA} + 1.867 V	$V_{CB, C}$ + 0.992 V	0	0	1 1 1 1 1 1 1 0	
255	V_{CA} + 1.875 V	$V_{CB, C}$ + 1 V	0	0	1 1 1 1 1 1 1 0	
Overflow	> V_{CA} + 1.875 V	> $V_{CB, C}$ + 1 V	1	0	1 1 1 1 1 1 1 0	

V_{CA} = ext. clamping level during CLAMP high pulse at $C_{ext\ cl}$ on channel AINA.
$V_{CB, C}$ = ext. clamping level during CLAMP high pulse at $C_{ext\ cl}$ on channel AINB and AINC.



Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltages[1)]	V_{CC}, V_{DD}		6.5	V
Input voltage range all inputs	V_I	– 0.3	V_{CC} + 0.3	V
Ambient temperature	T_A	0	70	°C
Storage temperature	T_{stg}	– 55	125	°C

1) All voltage values are with respect to network ground terminal

Characteristics

V_{DD} = 5 V ± 5 %, V_{CC} = 5 V ± 5 %, V_{REFH} = 2.5 V, V_{REFL} = 0.5 V, V_{GND} = 0 V
f_{CLK} = 27 MHz, all specifications min (T_A) to max (T_A) unless otherwise noted

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Power Requirements						
Analog supply voltage	V_{CC}	4.75	5	5.25	V	Pins 12, 18, 23
Digital supply voltage	V_{DD}	4.75	5	5.25	V	Pin 61
Output stage supply voltage	V_{DDQ}	4.75	5	5.25	V	Pins 43, 56, 62
Analog supply current	I_{CC}			160	mA	Sum of all V_{CC} pins
Digital supply current	I_{DD}			20	mA	Sum of all V_{DD} pins
Output stages supply current	I_{DDQ}			40	mA	Sum of all V_{DDQ} pins
Supply voltage differential	$V_{CC} - V_{DD}$	– 0.25		0.25	V	
Supply voltage differential	$V_{DDQ} - V_{DD}$	– 0.25		0.25	V	
Reference Inputs						
Reference voltage high	V_{REFH}			2.5	V	Pins 10, 16, 22
Reference voltage low	V_{REFL}	0.4	0.5		V	Pins 14, 20, 26
Reference current	I_{REF}		8		mA	Pins 10, 16, 22
Reference ladder resistance	R_{REF}		250		Ω	each
Analog Inputs						
Input range	V_I		2		Vpp	Single-ended, DC-15 MHz
Analog input capacitance	C_I		5		pF	AINA, AINB, AINC, each
Required ext clamp capacitance	$C_{ext\ cl}$		10		nF	AINA, AINB, AINC, each
Required signal source resistance	R_S			200	Ω	
Analog input current	I_{AIN}		5	100	nA	AINA, AINB, AINC, each

Characteristics (cont'd)

V_{DD} = 5 V ± 5 %, V_{CC} = 5 V ± 5 %, V_{REFH} = 2.5 V, V_{REFL} = 0.5 V, V_{GND} = 0 V
f_{CLK} = 27 MHz, all specifications min (T_A) to max (T_A) unless otherwise noted

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Digital Inputs						
L-input voltage H-input voltage	V_{IL} V_{IH}	0 2.0		0.8 V_{DD}	V V	
Input current	I_I	– 10	5	10	µA	V_I = 0 V, V_{CC}
Digital Outputs						
L-output voltage H-output voltage	V_{QL} V_{QH}	 2.4		0.4	V V	I_{SINK} = 1.6 mA I_{SOURCE} = 400 mA
High impedance state output current	I_{QZ}	– 20		20	µA	V_Q = 0 V, V_{CC}
Performance						
Sampling rate			27	30	MSPS	
Full power bandwidth (– 3 dB)	BW	10			MHz	
Diff. linearity (D.C.)	$DNLE$			± 0.5	LSB	
Int. linearity (D.C.)	$INLE$		± 0.5	± 1	LSB	
Clamping level accuracy	CLA		± 1	± 3	LSB	
Gain error	GE			± 3	LSB	
Differential gain[1)]	DG			3	%	f_I = 3.6/4.4 MHz AIN = 1/10 FSR[2)]
Differential phase[1)]	DP			3	degree	
Signal-to-noise ratio 4.4 MHz sinus	$\alpha_{S/N}$	42	46		dB	without harmonics 4:1:1 mode DSP 1.0
Harmonic Distorsion						
2./4. order 3. order 5./6. order				– 40 – 40 – 46	dB dB dB	4.4 MHz fundamental 4.4 MHz fundamental 4.4 MHz fundamental
Supply voltage rejection				2.5	%FSR/V[2)]	

1) Sample test
2) Full scale range (FSR) = 2 V as specified

Characteristics (cont'd)

V_{DD} = 5 V ± 5 %, V_{CC} = 5 V ± 5 %, V_{REFH} = 2.5 V, V_{REFL} = 0.5 V, V_{GND} = 0 V
f_{CLK} = 27 MHz, all specifications min (T_A) to max (T_A) unless otherwise noted

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Timing (see figure 5)						
Output data delay time	t_{QD}			25	ns	C_L = 15 pF
Output data hold time	t_{QH}	6			ns	C_L = 15 pF
CLK pulse width	t_{WH}; t_{WL}	10			ns	C_L = 15 pF
CLK rise time	t_{TLH}			5	ns	C_L = 15 pF
CLK fall time	t_{THL}			5	ns	C_L = 15 pF
Input data setup time	t_{SU}	7			ns	C_L = 15 pF
Input data hold time	t_{IH}	6			ns	C_L = 15 pF
Clamp input pulse width	t_{Ci}	10			CLK cycles	1 nF ext. clamp cap.

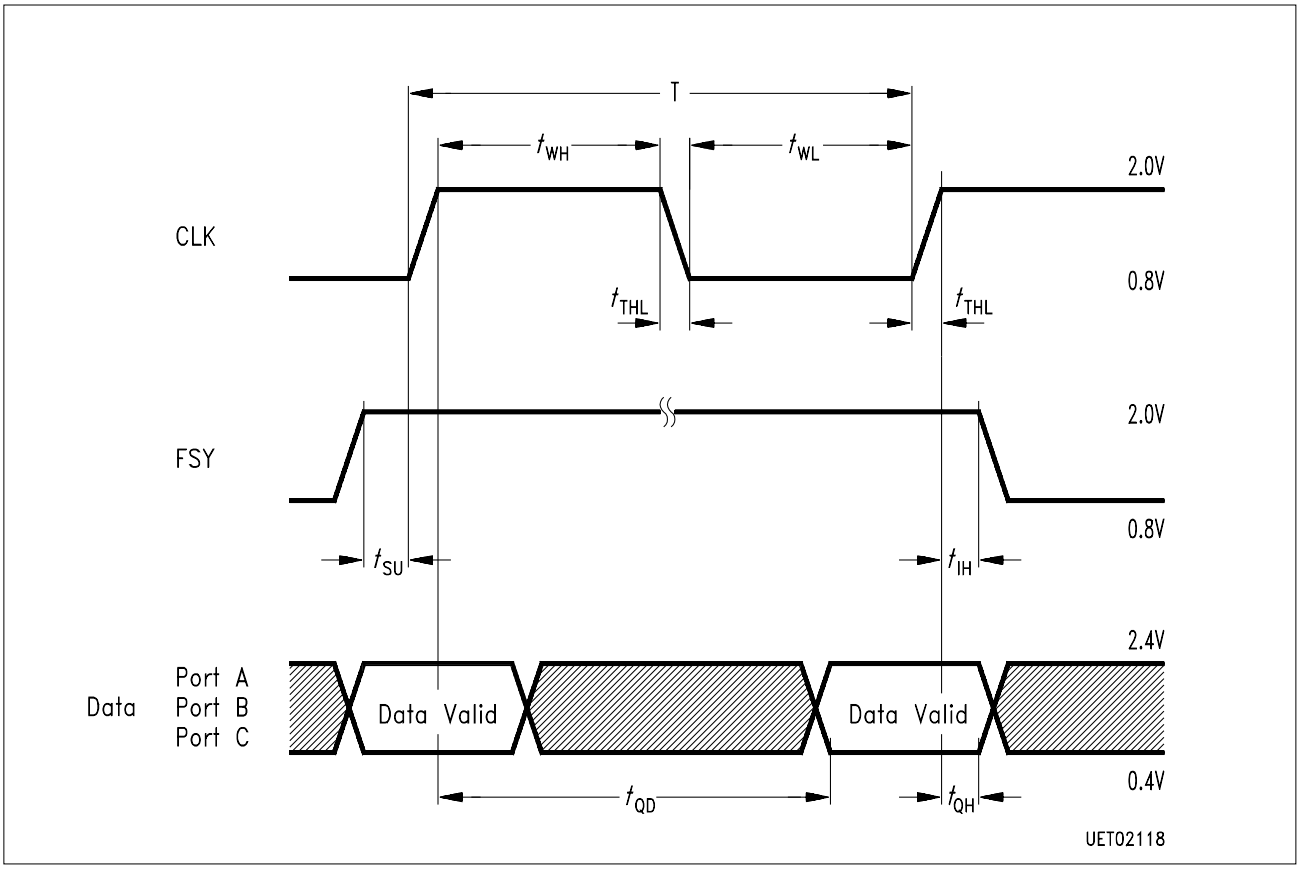


Figure 5
Timing Diagram Port A, B, C

Sample output data-delay is shown on format 8:8:8 with DSP function 1.0 + 2.0

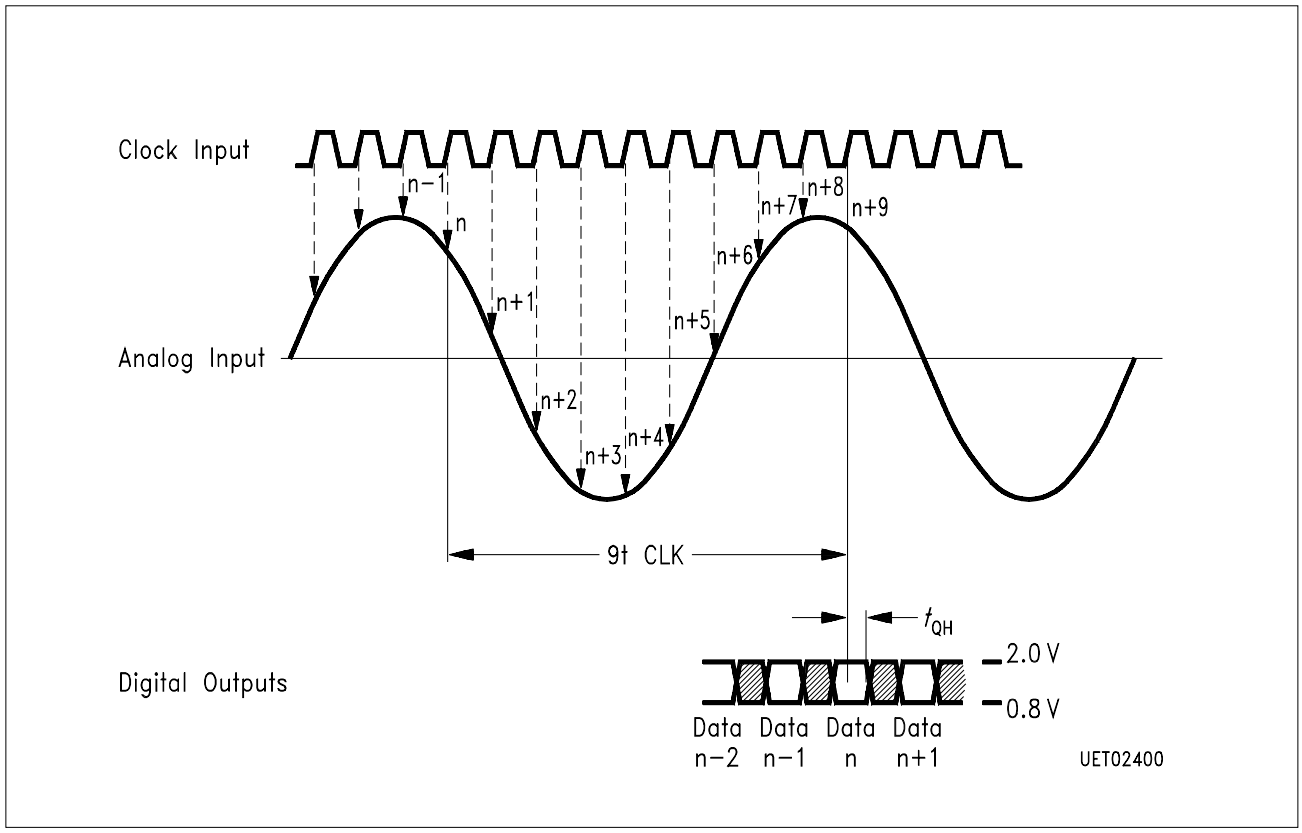
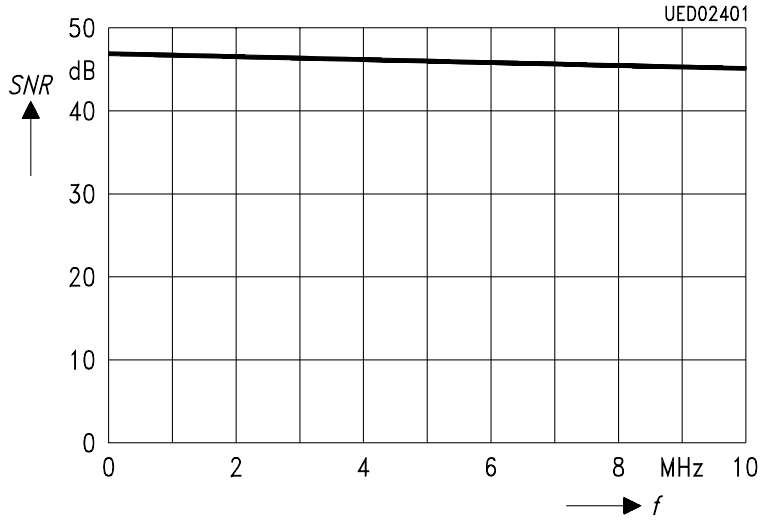


Figure 6
Diagram of Complete Timing

There is a delay of 9 clock cycles between sampling of an analog input signal and the corresponding digital output signal.

Figure 7
Typ. *SNR* (without harmonics) versus Analog Frequency (411 Mode DSP 1.0)



References

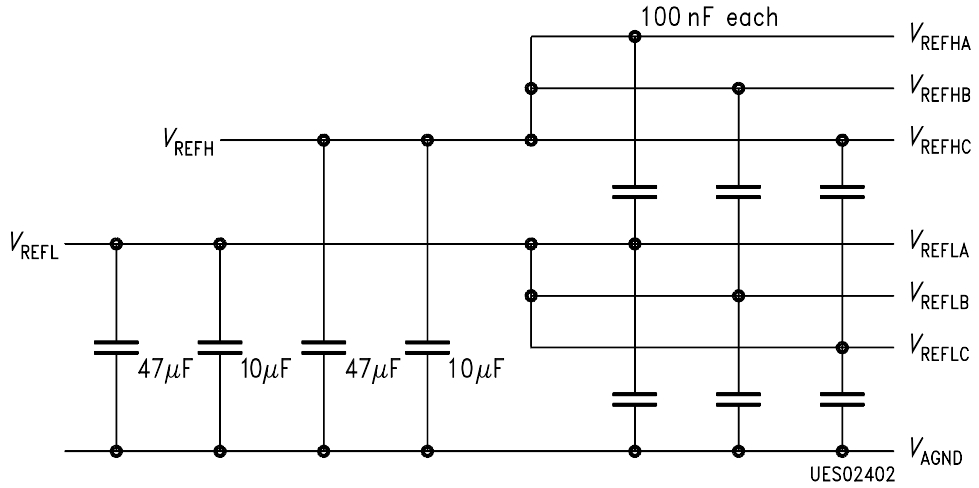
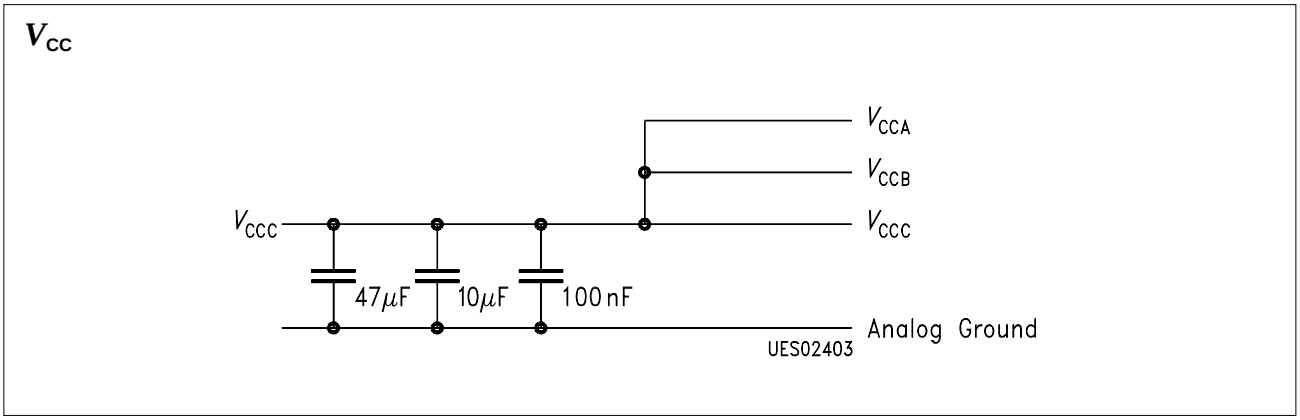
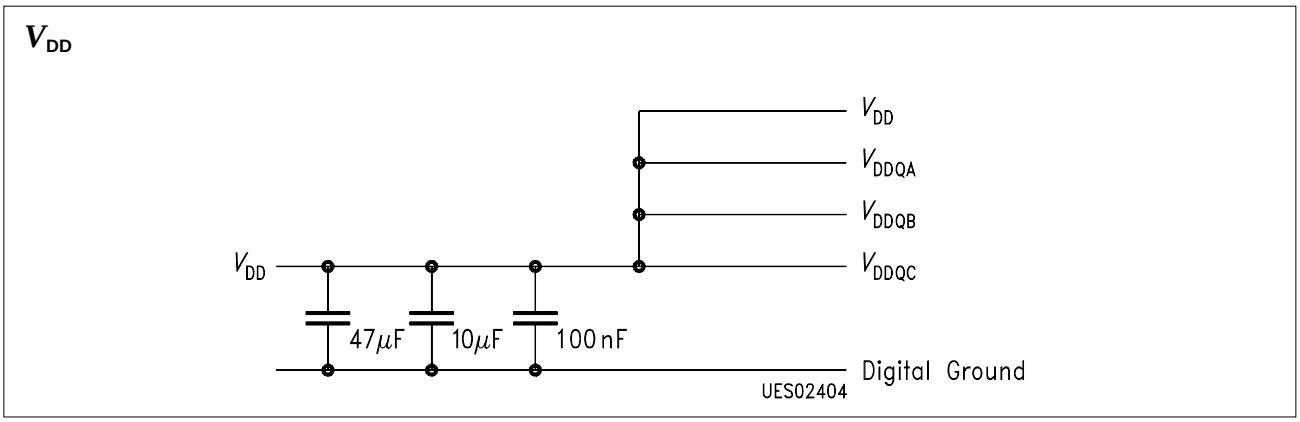


Figure 8
Blocking the SDA 9205-2

Capacitors: 100 nF - Ceramic
10 nF - Tantal
47 µF - Elko





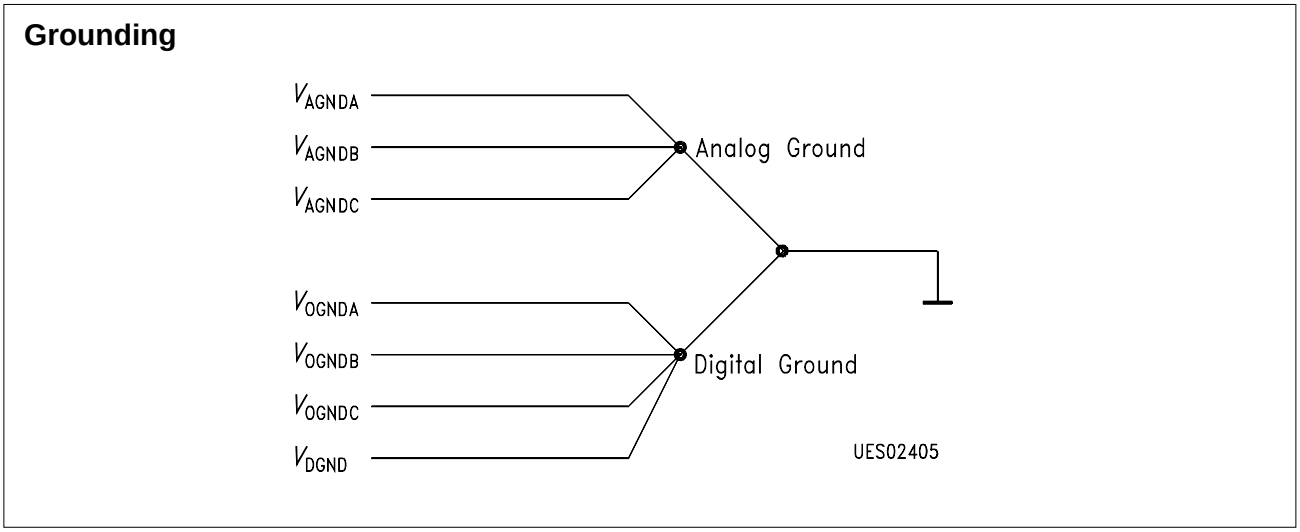


Figure 8 (cont'd)
Blocking the SDA 9205-2

Chip Capacitors 100 nF (as near as possible to the socket)

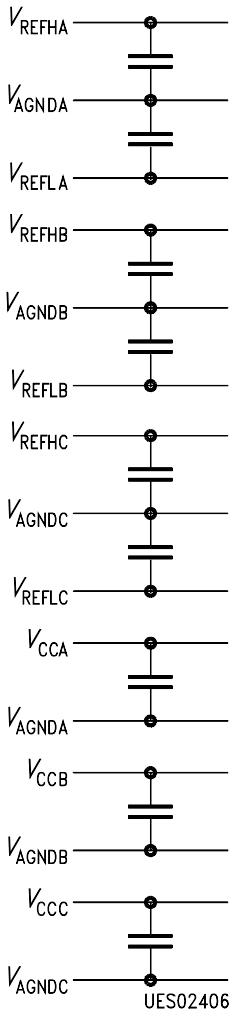


Figure 8 (cont'd)
Blocking the SDA 9205-2

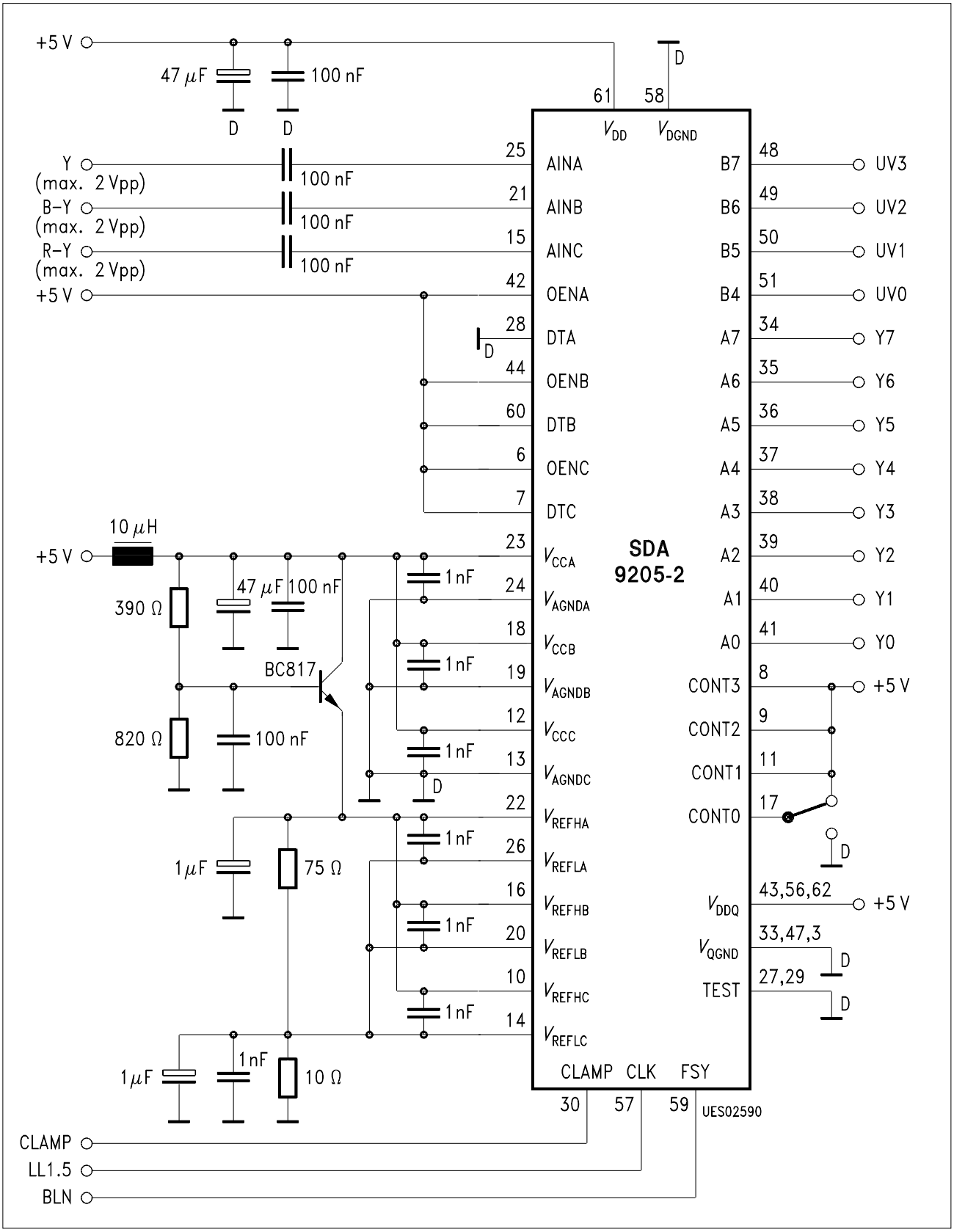
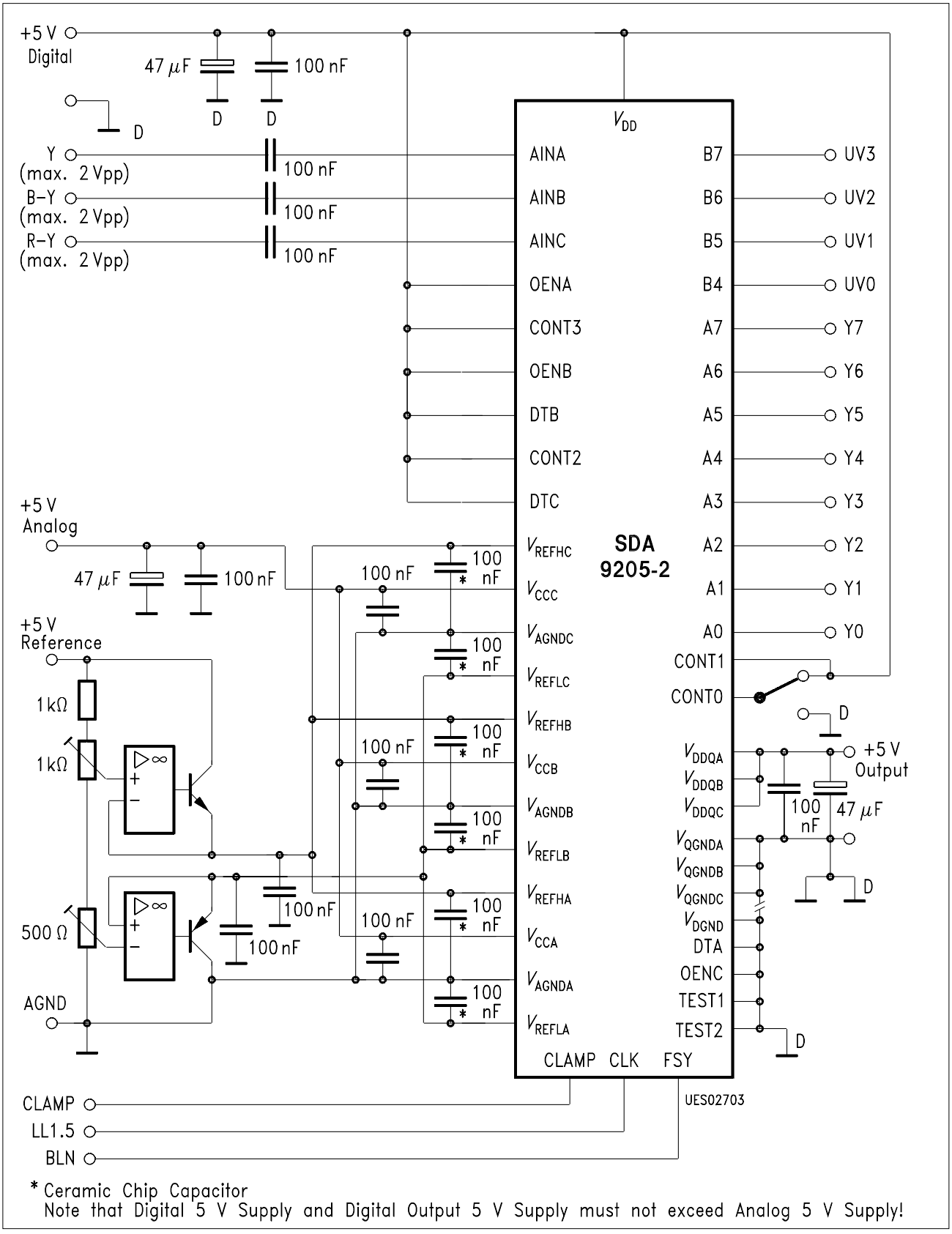


Figure 9
Application Circuit 1 (4:1:1 Format, for Siemens Featurebox)


+5 V
Digital
47 µF
100 nF
D
D
D
Y
(max. 2 Vpp)
B-Y
(max. 2 Vpp)
R-Y
(max. 2 Vpp)
100 nF
100 nF
100 nF
+5 V
Analog
47 µF
100 nF
+5 V
Reference
1 kΩ
1 kΩ
500 Ω
AGND
100 nF
100 nF
100 nF