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The SP5512 is a single-chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. The device has six controllable open-collector output ports (P2-P7), each capable of sinking 20mA. In addition, P6 is a 3-bit 5-level ADC input. The information on these ports can be read via the I²C BUS.

The device has one fixed I²C BUS address and three programmable addresses, allowing two or more synthesisers to be used in a system.

FEATURES

- Complete 1.3GHz Single Chip System
 - Programmable via the I²C BUS
 - Low Power Consumption (215mW Typ.)
 - Low Radiation
 - Phase Lock Detector
 - Varactor Drive Amp Disable
 - 6 Controllable Outputs, 5 Bi-directional
 - 5-Level ADC
 - Variable I²C BUS Address for Picture in Picture TV
 - ESD Protection *
- * Normal ESD handling precautions should be observed.

DS2384

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Ordering Information
 SP5512DS/KG/MPAS (Tubes)
 SP5512DS/KG/MPAD (Tape & Reel)
 (16-lead miniature plastic package)

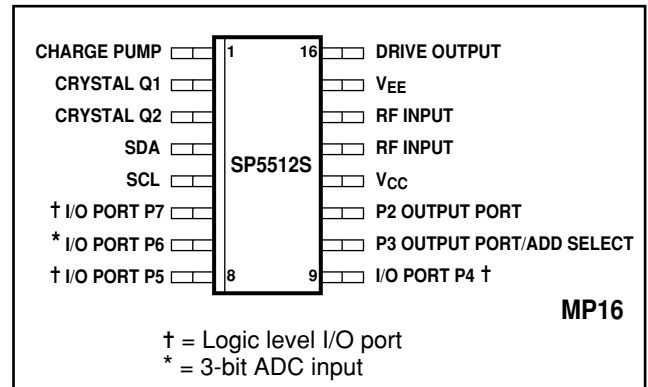


Fig. 1 Pin connections – top view

APPLICATIONS

- Cable Tuning Systems
- VCRs

ELECTRICAL CHARACTERISTICS

$T_{AMB} = -10^{\circ}\text{C}$ to $+80^{\circ}\text{C}$, $V_{CC} = +4.5\text{V}$ to $+5.5\text{V}$.

These Characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated. Reference frequency 4MHz unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	12		43	53	mA	$V_{CC} = 5\text{V}$ 50MHz to 1GHz 1.3GHz, see Fig. 5
Prescaler input voltage	13,14	12.5		300	mVrms	
		30		300	mVrms	
Prescaler input impedance	13,14		50		Ω	
Prescaler input capacitance			2		pF	
SDA, SCL						
Input high voltage	4,5	3		5.5	V	Input voltage = V_{CC} Input voltage = 0V When $V_{CC} = 0\text{V}$
Input low voltage	4,5	0		1.5	V	
Input high current	4,5			10	μA	
Input low current	4,5			-10	μA	
Leakage current	4,5			10	μA	
SDA						
Output voltage	4			0.4	V	Sink current = 3mA
Charge pump current low	1		± 50		μA	Byte 4, bit 2 = 0, pin 1 = 2V
Charge pump current high	1		± 170		μA	
Charge pump output leakage current	1			± 5	nA	Byte 4, bit 4 = 1, pin 1 = 2V V pin 16 = 0.7V
Charge pump drive output current	16	500				
Charge pump amplifier gain			6400			Parallel resonant crystal (note 2)
Recommended crystal series resistance		10		200	Ω	
Crystal oscillator drive level			40		mV p-p	
Crystal oscillator negative resistance	2	750			Ω	
Output Ports						
P2-P7 sink current (see note 1)	6-11	20			mA	$V_{OUT} = 0.7\text{V}$, see note 1 $V_{OUT} = 13.2\text{V}$
P2-P7 leakage current (see note 1)	6-11			10	μA	
Input Ports						
P3 input current high	10			-10	μA	V pin 10 = 13.2V V pin 10 = 0V
P3 input current low	10			-10	μA	
P4, P5, P7 input voltage low	6,8,9			0.8	V	See Table 3 for ADC levels
P4, P5, P7 input voltage high	6,8,9	2.7			V	
P6 input current high	7			+10	μA	
P6 input current low	7			-10	μA	

NOTES

1. Source impedance between all output ports and ground is approximately 5 Ω . This should be taken into account when calculating output port saturation voltages.
2. The recommended crystal series resistance quoted refers to all conditions including start-up.

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} and pin 3 at 0V.

Parameter	Pin	Value		Units	Conditions
		Min.	Max.		
Supply voltage	12	-0.3	7	V	
RF input voltage	13,14		2.5	V p-p	
Port voltage	6-11	-0.3	14	V	Port in off state
		-0.3	6	V	Port in on state
Total port output current	6-11		50	mA	
RF input DC offset	13-14	-0.3	$V_{CC}+0.3$	V	
Charge pump DC offset	1	-0.3	$V_{CC}+0.3$	V	
Drive output DC offset	16	-0.3	$V_{CC}+0.3$	V	
Crystal oscillator DC offset	2	-0.3	$V_{CC}+0.3$	V	
SDA, SCL input voltage	4,5	-0.3	$V_{CC}+0.3$	V	With V_{CC} applied
		-0.3	5.5	V	V_{CC} not applied
Storage temperature		-55	+150	°C	
Junction temperature			+150	°C	
MP16 thermal resistance, chip-to-ambient			111	°C/W	
MP16 thermal resistance, chip-to-case			41	°C/W	
Power consumption at 5.5V			321	mW	

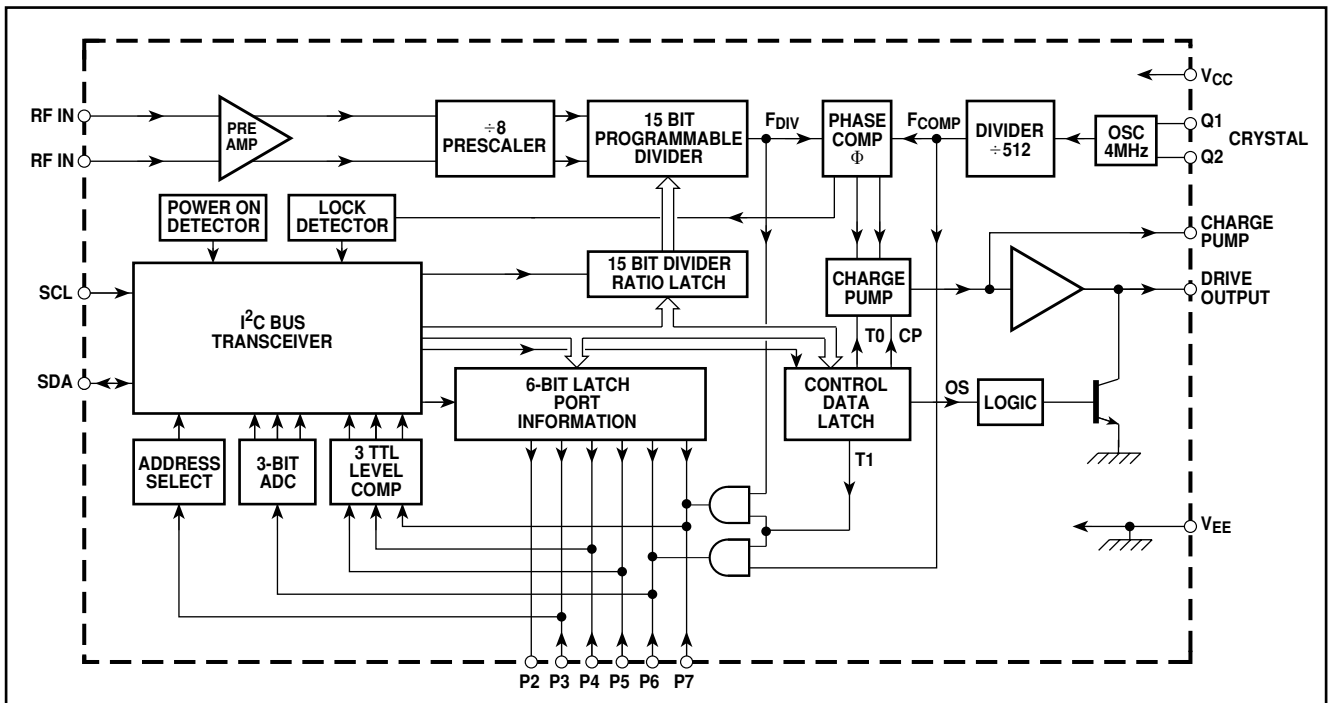


Fig. 2 Block diagram

FUNCTIONAL DESCRIPTION

The SP5512 is programmed from an I²C BUS. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I²C Bus format. The synthesiser can either accept new data (write mode) or send data (read mode). The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I²C BUS system. Table 4 shows how the address is selected by applying a voltage to P3. The LSB of the address byte (R/W) sets the device into read mode if it is high and write mode if it is low. When the SP5512 receives a correct address byte it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data bytes are programmed. When the SP5512 is programmed into the read mode the controlling device accepting the data must pull down the SDA line during the following acknowledge period to read another status byte.

WRITE MODE (FREQUENCY SYNTHESIS)

When the device is in the write mode Bytes 2+3 select the synthesised frequency while Bytes 4+5 select the output port states and charge pump information.

Once the correct address is received and acknowledged, the first bit of the next byte determines whether that byte is interpreted as Byte 2 or 4, a logic 0 for frequency information and a logic 1 for charge pump and output port information. Additional data bytes can be entered without the need to re-address the device until an I²C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid-byte (e.g., by another device on the bus) then the previously programmed byte is maintained.

Frequency data from Bytes 2 and 3 is stored in a 15-bit shift register and is used to control the division ratio of the 15-bit programmable divider which is preceded by a divide-by-8 prescaler and amplifier to give excellent sensitivity at the local oscillator input; see Fig 5. The input impedance is shown in Fig. 7.

The programmed frequency can be calculated by multiplying the programmed division ratio by 8 times the comparison frequency F_{COMP} .

When frequency data is entered, the phase comparator, via the charge pump and varactor drive amplifier, adjusts the

local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2 or provided by an on-chip 4MHz crystal controlled oscillator.

Note that the comparison frequency is 7.8125kHz when a 4MHz reference is used.

Bit 2 of Byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for $\pm 170\mu A$ and a logic 0 for $\pm 50\mu A$, allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. Bit 4 of Byte 4 (T0) disables the charge pump if set to a logic 1. Bit 8 of Byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1. Bit 3 of Byte 4 (T1) selects a test mode where the phase comparator inputs are available on P6 and P7, a logic 1 connects F_{COMP} to P6 and F_{DIV} to P7.

Byte 5 programs the output ports P2-P7, a logic 0 for a high impedance output, logic 1 for low impedance (on).

READ MODE

When the device is in the read mode the status data read from the device on the SDA line takes the form shown in Table 2.

Bit 1 (POR) is the power on reset indicator and is set to a logic 1 if the power supply to the device has dropped below a nominal 3V and the programmed information lost (e.g., when the device is initially turned on). The POR is set to 0 when the read sequence is terminated by a stop command. The outputs are all set to high impedance when the device is initially powered up. Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked and a logic 0 if the device is unlocked.

Bits 3, 4 and 5 (I2, I1, I0) show the status of the I/O Ports P7, P5 and P4 respectively. A logic 0 indicates a low level and a logic 1 a high level. If the ports are to be used as inputs they should be programmed to a high impedance state (logic 1). These inputs will then respond to data complying with standard TTL voltage levels. Bits 6, 7 and 8 (A2, A1, A0) combine to give the output of the 5-level ADC.

The 5-level ADC can be used to feed AFC information to the microprocessor from the IF section of the television, as illustrated in Fig. 4.

	MSB					LSB				
Address	1	1	0	0	0	MA1	MA0	0	A	Byte 1
Programmable divider	0	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	A	Byte 2
Programmable divider	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	A	Byte 3
Charge pump and test bits	1	CP	T1	T0	1	1	1	OS	A	Byte 4
I/O port control bits	P7	P6	P5	P4	P3	P2	X	X	A	Byte 5

Table 1 Write data format (MSB transmitted first)

Address	1	1	0	0	0	MA1	MA0	1	A	Byte 1
Status byte	POR	FL	I2	I1	I0	A2	A1	A0	A	Byte 2

Table 2 Read data format

A2	A1	A0	Voltage input to P6
1	0	0	0·6V _{CC} to 13·2V
0	1	1	0·45V _{CC} to 0·6V _{CC}
0	1	0	0·3V _{CC} to 0·45V _{CC}
0	0	1	0·15V _{CC} to 0·3V _{CC}
0	0	0	0V to 0·15V _{CC}

Table 3 ADC levels

MA1	MA0	Voltage input to P3
0	0	0V to 0·2V _{CC}
0	1	Always valid
1	0	0·3V _{CC} to 0·7V _{CC}
1	1	0·8V _{CC} to 13·2V

Table 4 Address selection

- A** : Acknowledge bit
- MA1, MA0** : Variable address bits (see Table 4)
- CP** : Charge Pump current select
- T1** : Test mode selection
- T0** : Charge pump disable
- OS** : Varactor drive Output disable Switch
- P7, P6, P5, P4, P3, P2** : Control output port states
- POR** : Power On Reset indicator
- FL** : Phase lock detect flag
- I2, I1, I0** : Digital information from ports P7, P5 and P4 respectively
- A2, A1, A0** : 5-level ADC data from P6 (see Table 3)
- X** : Don't care

Fig. 3 Data formats

APPLICATION

A typical application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6.

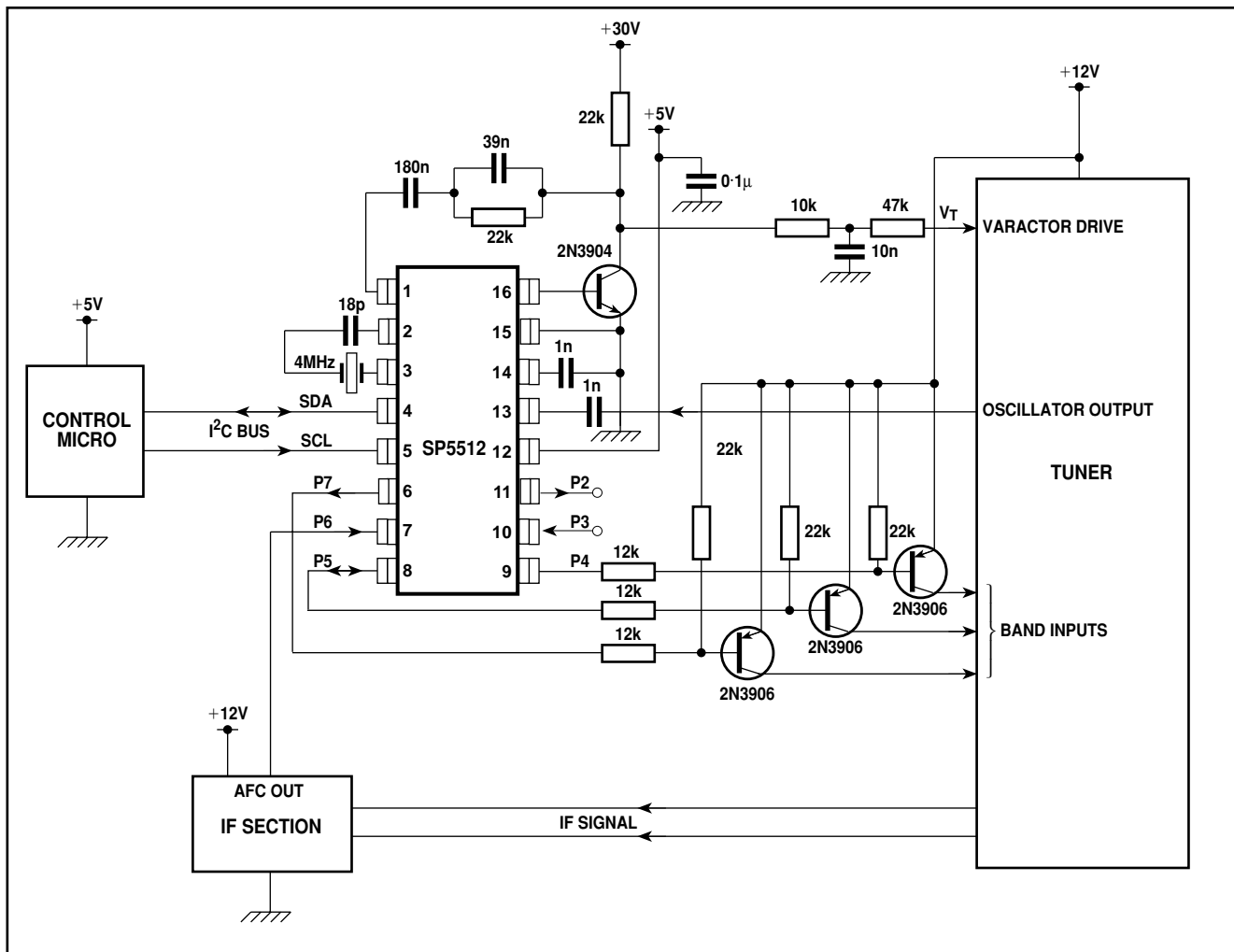


Fig. 4 Typical application

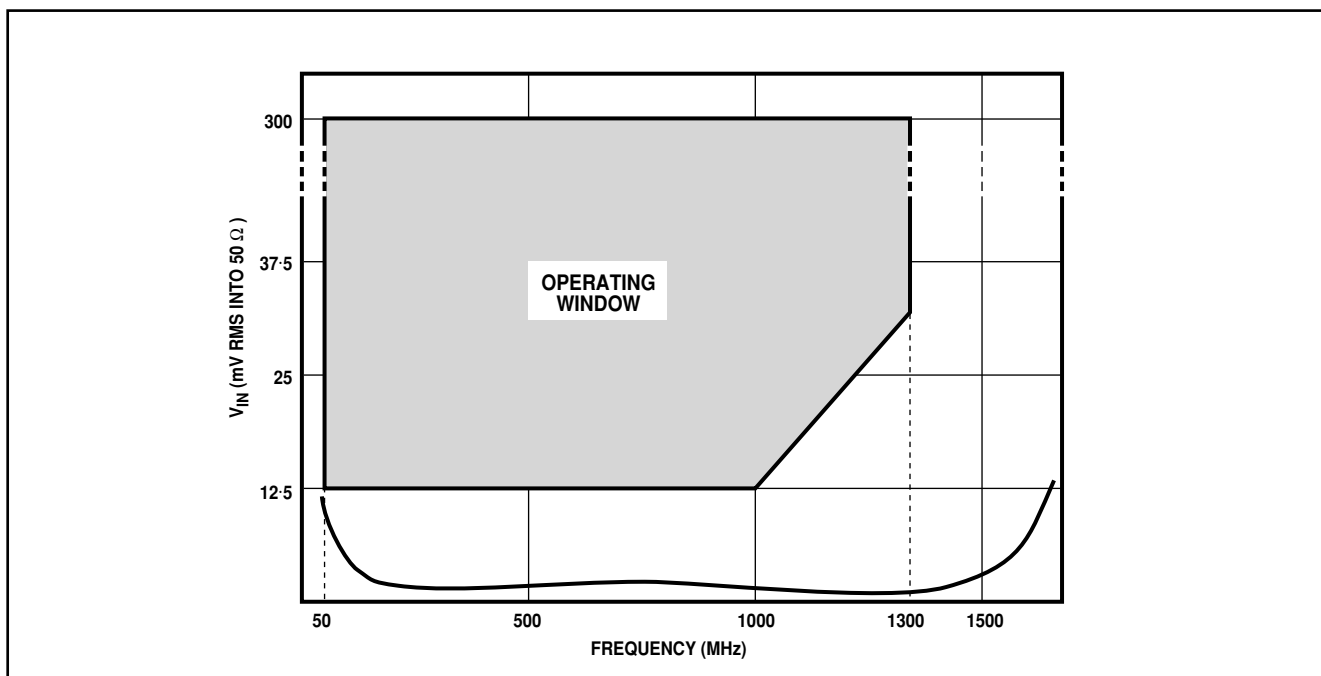


Fig. 5 Typical input sensitivity

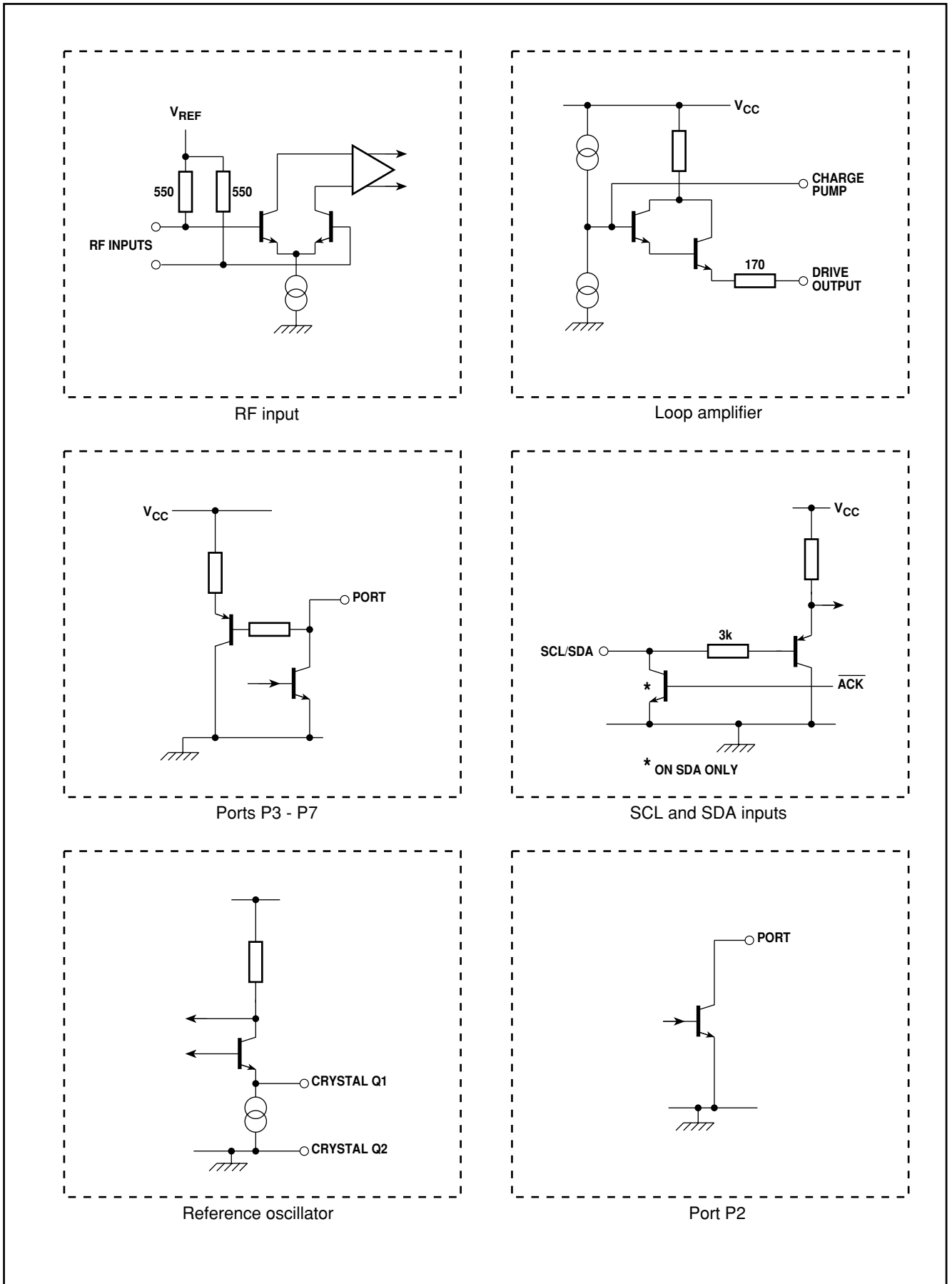


Fig. 6 Input/output interface circuits

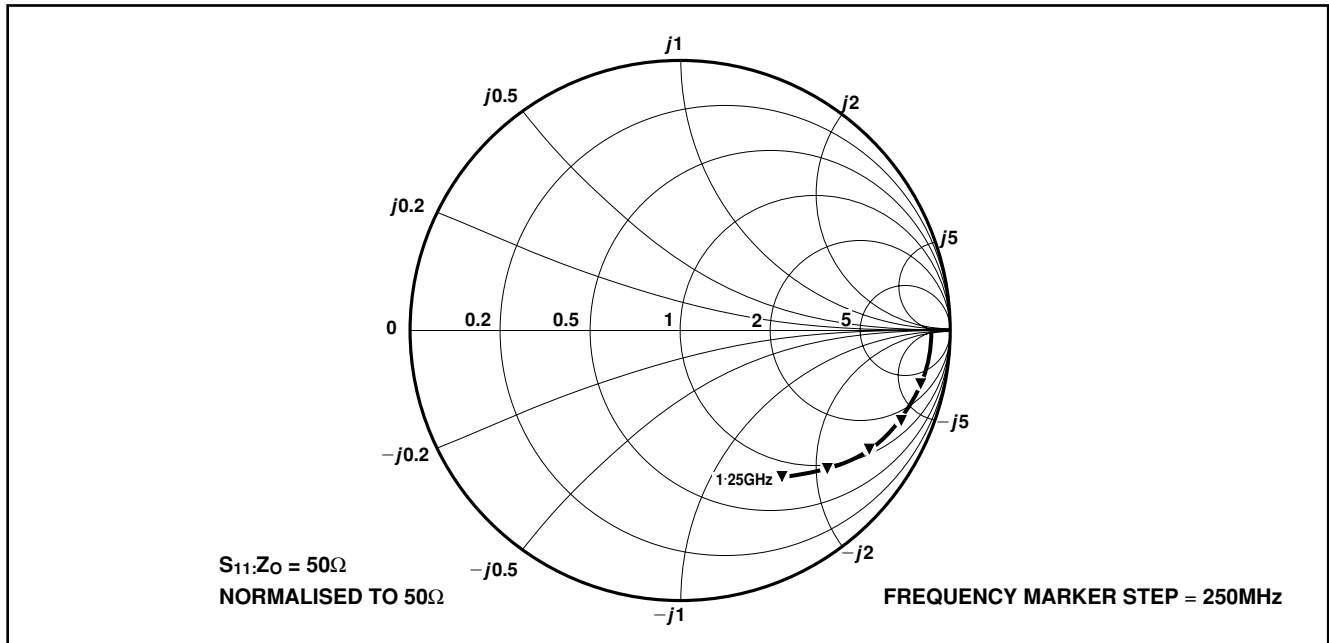
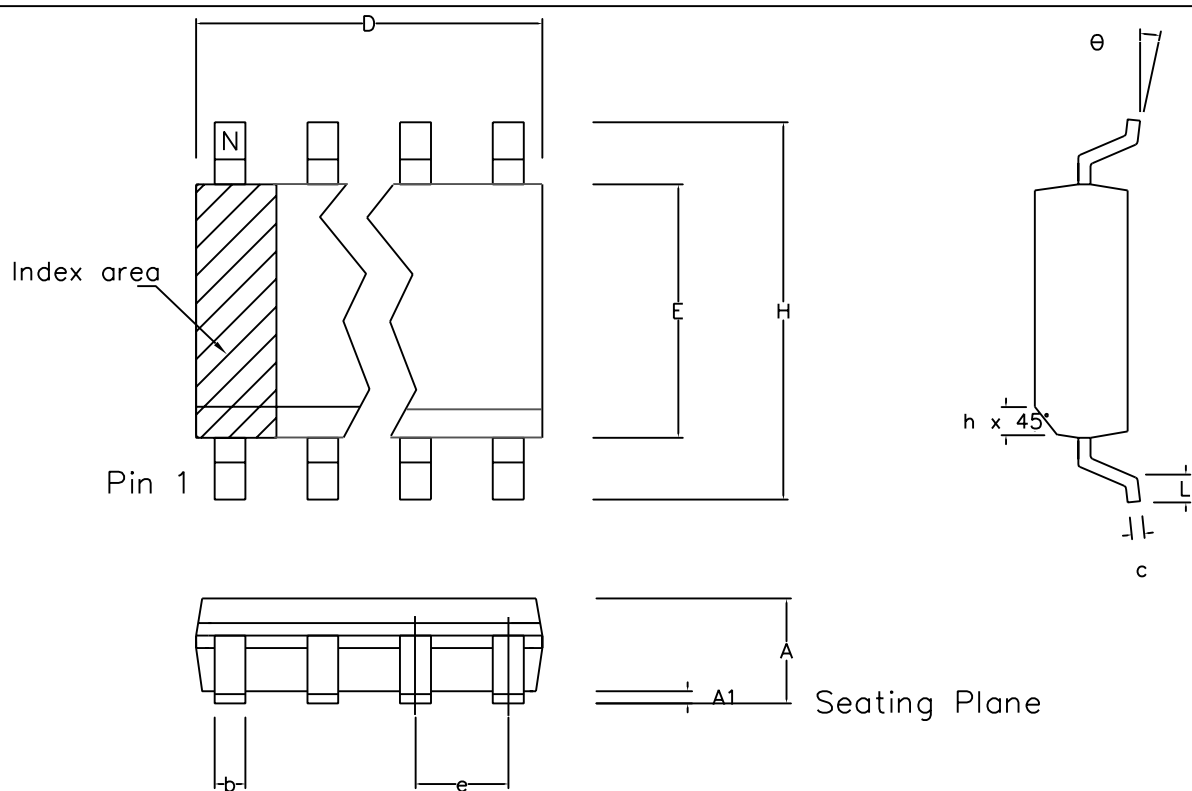


Fig. 7 Typical input impedance



	Min mm	Max mm	Min inch	Max inch
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	9.80	10.00	0.386	0.394
H	5.80	6.20	0.228	0.244
E	3.80	4.00	0.150	0.157
L	0.40	1.27	0.016	0.050
e	1.27 BSC		0.050 BSC	
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
O	0°	8°	0°	8°
h	0.25	0.50	0.010	0.020
Pin Features				
N	16		16	
Conforms to JEDEC MS-012AC Iss. C				

Notes:

1. The chamfer on the body is optional. If not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in inches.
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion / intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

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	Package Code DC
Previous package codes MP / S	Package Outline for 16 lead SOIC (0.150" Body Width)
	GPD00012



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