SP5658

2.7GHz 3-Wire Bus Controlled Frequency Synthesiser

Advance Information

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The SP5658 is a single chip frequency synthesiser designed for tuning systems up to 2.7GHz.

The RF preamplifer contains a divide by two prescaler which can be disabled for applications up to 2GHz so enabling a step size equal to the comparison frequency up to 2GHz and twice the comparison frequency up to 2.7GHz.

Comparison frequencies are obtained either from a crystal controlled on–chip oscillator or from an external source.

The device contains two switching ports, in the 14 pin version and four in the 16 pin, together with an ‘‘in–lock” flag output. The device also contains a varactor line disable and charge pump disable facility.

FEATURES

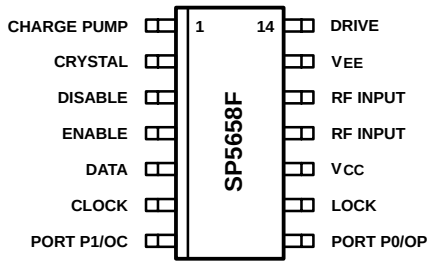
- Complete 2.7GHz single chip system
- Optimised for low phase noise
- Selectable divide by two prescaler
- Selectable reference division ratio
- Charge pump disable
- Varactor line disable
- ‘In–lock’ flag
- Two switching ports in 14 pin version
- Four switching ports in 16 pin version
- Pin compatible with SP5659 I 2 C bus low phase noise synthesiser
- ESD protection (Normal ESD handling procedures should be observed)

APPLICATIONS

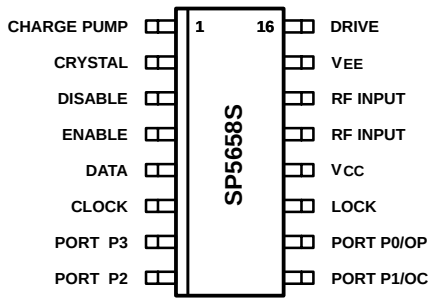
- SAT, TV, VCR and Cable tuning systems
- Communications systems

Ordering Information

SP5658F/KG/MP1S (Tubes, 14 lead SO)
SP5658S/KG/MP2S (Tubes, 16 lead SO)
SP5658F/KG/MP1T (Tape and Mounted)
SP5658S/KG/MP2T (Tape and Mounted)



MP14



MP16

Fig. 1 Pin connections – top view

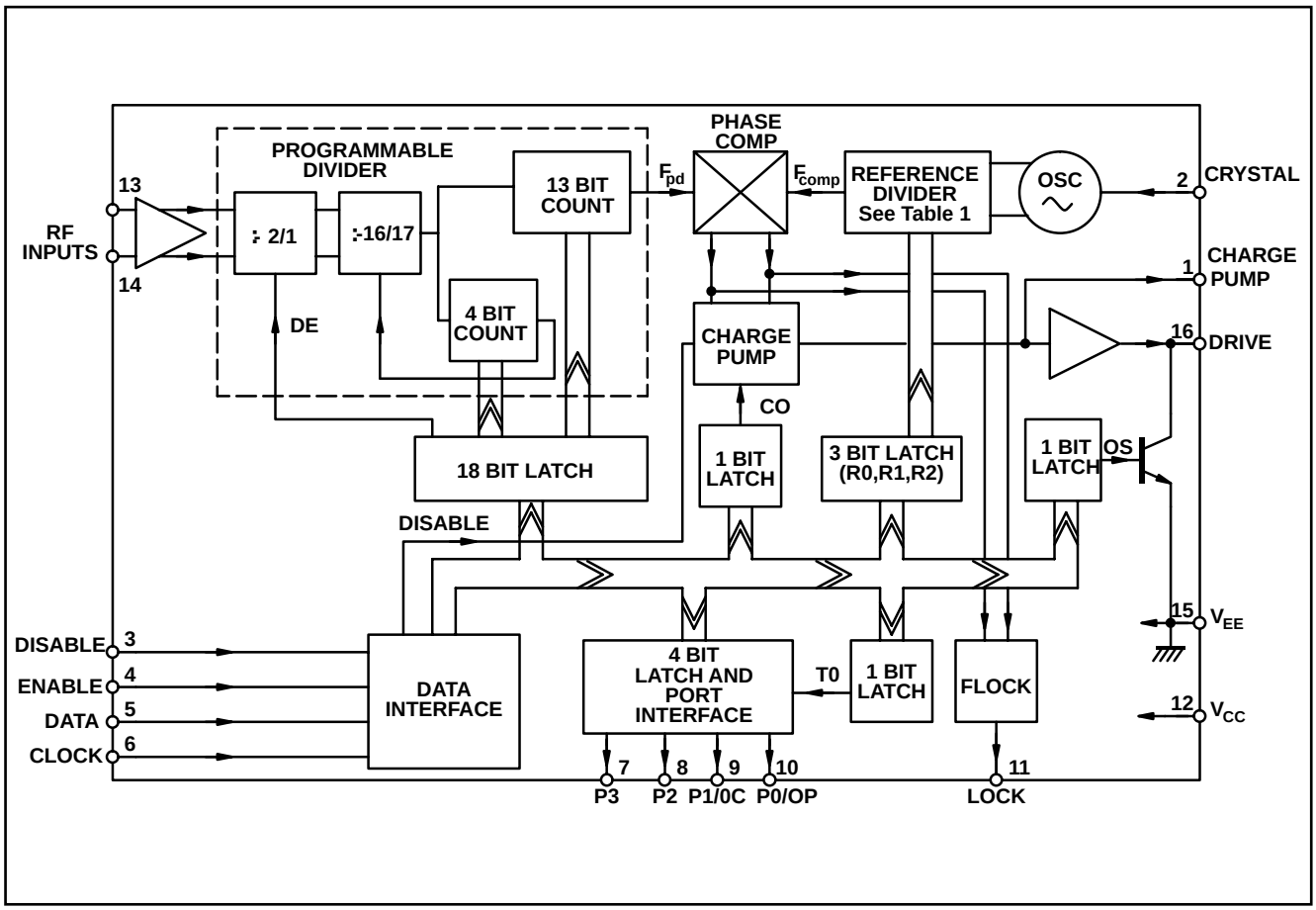


Fig. 2 SP5658S block diagram

ELECTRICAL CHARACTERISTICS

T amb = –20°C to + 80°C, V_{CC} = + 4.5V to + 5.5V. Reference frequency = 4MHz. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin (SP5658S)	Value			Units	Conditions
		Min	Typ	Max		
Supply current, I_{CC}	12		59 52	74 65	mA mA	V_{CC} =5V Prescaler enabled, DE=1 V_{CC} =5V Prescaler disabled, DE=0
RF input voltage	13, 14	40		300	mV_{rms}	300MHz to 2.7GHz Prescaler enabled, DE=1, See Fig. 5b
	13,14	100		300	mV_{rms}	80MHz Prescaler enabled, DE=1, See Fig. 5b.
	13, 14	40		300	mV_{rms}	100MHz to 2.0GHz Prescaler disabled, DE=0, See Fig. 5a
	13,14	50		300	mV_{rms}	80MHz Prescaler disabled, DE=0, See Fig. 5a.
RF input impedance	13, 14		50		Ω	Refer to Fig. 4
RF input capacitance	13, 14	2			pF	Refer to Fig. 4
Data, Clock, Enable & Disable	3,4,5,6					
Input high voltage		3		V_{CC}	V	
Input low voltage		0		0.7	V	
Input high current				10	µA	Input voltage = V_{CC}
Input low current				–10	µA	Input voltage = V_{EE}
Clock Rate	6			500	kHz	
Clock data & enable input hysteresis	4,5,6		0.4		V	

ELECTRICAL CHARACTERISTICS

T amb = –20°C to + 80°C, V_{CC} = + 4.5V to + 5.5V. Reference frequency = 4MHz. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin (SP5658S)	Value			Units	Conditions
		Min	Typ	Max		
Bus Timing	4,5,6					
Data set up, $\mathbf{t}_{SU}$		300			ns	See Fig. 3
Data hold, $\mathbf{t}_{HD}$		600			ns	See Fig. 3
Enable set up, $\mathbf{t}_{ES}$		300			ns	See Fig. 3
Enable hold, $\mathbf{t}_{EH}$		600			ns	See Fig. 3
Clock to enable, $\mathbf{t}_{CE}$		300			ns	See Fig. 3
Charge pump output current	1					See Table 3, V_{PIN1} = 2V
Charge pump output leakage	1		± 3	± 10	nA	V_{PIN1} = 2V
Charge pump drive output current	16	1			mA	V_{PIN16} = 0.7V
Oscillator temperature stability	2			2	ppm/°C	
Oscillator supply voltage stability	2			2	ppm/V	
External reference input frequency	2	2		20	MHz	AC coupled sinewave
External reference input amplitude	2	200		500	mV_{PP}	AC coupled sinewave
Crystal frequency	2	4		12	MHz	
Crystal oscillator drive level	2		45		mV_{PP}	
Recommended crystal series resistance		100		200	Ω	Applies to 4MHz crystal only. ‘‘Parallel resonant” crystal. Figure quoted is under all conditions including start up.
Crystal oscillator negative resistance	2	400			Ω	Includes temperature and process tolerances.
Comparison frequency				2	MHz	
Phase noise at phase detector			–142		dBC/Hz	6kHz loop BW, phase comparator freq 250kHz. Figure measured @ 1kHz offset, DSB (within loop band width).
RF division ratio		240		131071		Prescaler disabled, DE=0
		480		262142		Prescaler enabled, DE=1
Reference division ratio						See Table 1
Output ports P0–P3 #	7,8,9,10					
Sink current		10			mA	V_{PORT} =0.7V
Leakage current				10	µA	V_{PORT} =13.2V
Lock output	11					
Sink current		1			mA	V_{LOCK} =0.7V, ‘out of lock’
Leakage current				10	µA	‘in lock’

Ports P2 and P3 are not available on the SP5658F.

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V EE at 0V

Characteristics	Pin (SP5658S)	Min	Max	Units	Conditions
Supply voltage, V_{CC}	12	–0.3	7	V	
RF input voltage	13, 14		2.5	V_{p-p}	AC coupled as per application
RF input DC offset	13, 14	–0.3	V_{CC} +0.3	V	
Port voltage	7 – 10	–0.3	14	V	Port in off state
	7 – 10	–0.3	6	V	Port in on state
Total port current	7 – 10		50	mA	
Lock output DC offset	11	–0.3	V_{CC} +0.3	V	
Charge pump DC offset	1	–0.3	V_{CC} +0.3	V	
Drive DC offset	16	–0.3	V_{CC} +0.3	V	
Crystal DC offset	2	–0.3	V_{CC} +0.3	V	
Data, Clock, Enable & Disable DC offset	3 – 6	–0.3	V_{CC} +0.3	V	
Storage temperature		–55	+125	°C	
Junction temperature			150	°C	
MP14 Thermal Resistance					
Chip to ambient 123 °C/W					
Chip to case 45 °C/W					
MP16 Thermal Resistance					
Chip to ambient			111	°C/W	
Chip to case			41	°C/W	
Power consumption at V_{CC} =5.5V			407	mW	All ports off, prescaler enabled
ESD protection	ALL	2		kV	MIL–STD 883 TM 3015

FUNCTIONAL DESCRIPTION

The SP5658 contains all the elements necessary, with the exception of a frequency reference, loop filter and external high voltage transistor, to control a varicap tuned local oscillator, so forming a complete PLL frequency synthesised source. The device allows for operation with a high comparison frequency and is fabricated in high speed logic, which enables the generation of a loop with good phase noise performance. The RF preamplifier contains a selectable divide by two for operation above 2.0GHz. Up to 2GHz the RF input interfaces directly with the programmable divider, so eliminating degradation in phase noise due to the prescaler action. The block diagram is shown in Fig.2.

The SP5658 is controlled by a standard 3–wire bus comprising data, clock and enable inputs. The programming word for the 16 pin variant contains 28 bits, four of which are used for port selection, 18 to set the programmable divider ratio and enable/disable the prescaler, bit DE, three bits to select the reference division ratio, bits R0–R2, one bit to set charge pump current, bit C0, and the remaining two bits to access test modes, bit T0, and to disable the varactor drive, bit OS. The data word for 14 pin variant is identical to 16 pin except 26 bits only are required, two of which are used for port selection. The programming format is shown in Fig. 3.

The clock input is disabled by an enable low signal, data is therefore only clocked into the internal shift registers during an enable high and is loaded into the controlling buffers by an enable high to low transition. This load is also synchronised with the programmable divider so giving smooth fine tuning.

The RF signal is fed to an internal preamplifier, which provides gain and reverse isolation from the divider signals. The output of the preamplifier is fed to the 2/1 selectable prescaler and then to the 17 bit fully programmable divider, which is of MN+A architecture. The M counter is 13 bit and the A counter 4. If bit DE is set to a 0 the prescaler is disabled; Note that the control function DE cannot be used dynamically.

The output of the programmable divider is fed to the phase comparator where it is compared in both phase and frequency domain with the comparison frequency. This frequency is derived either from the on board crystal controlled oscillator or from an external source. In both cases the reference frequency is divided down to the comparison frequency by the reference divider which is programmable into 1 of 8 ratios as described in Table 1.

The output of the phase comparator feeds the charge pump and loop amplifier section, which when used with an external high voltage transistor and loop filter integrates the current pulses into the varactor line voltage. The charge pump can be disabled to a high impedance state by the DISABLE input. The varactor drive output can also be disabled by the OS bit within the data word, so switching the external transistor 'OFF' and allowing an external voltage to be written to the varactor line for tuner alignment purposes.

The phase comparator also drives the lock detect circuit which generates a lock flag. 'In–lock' is indicated by a high impedance state on the lock output.

The programmable divider output divided by 2, $F_{pd}/2$ and the comparison frequency, F_{comp} can be switched to ports P0 and P1 respectively by switching the device into test mode. The test modes are described in Table 2.

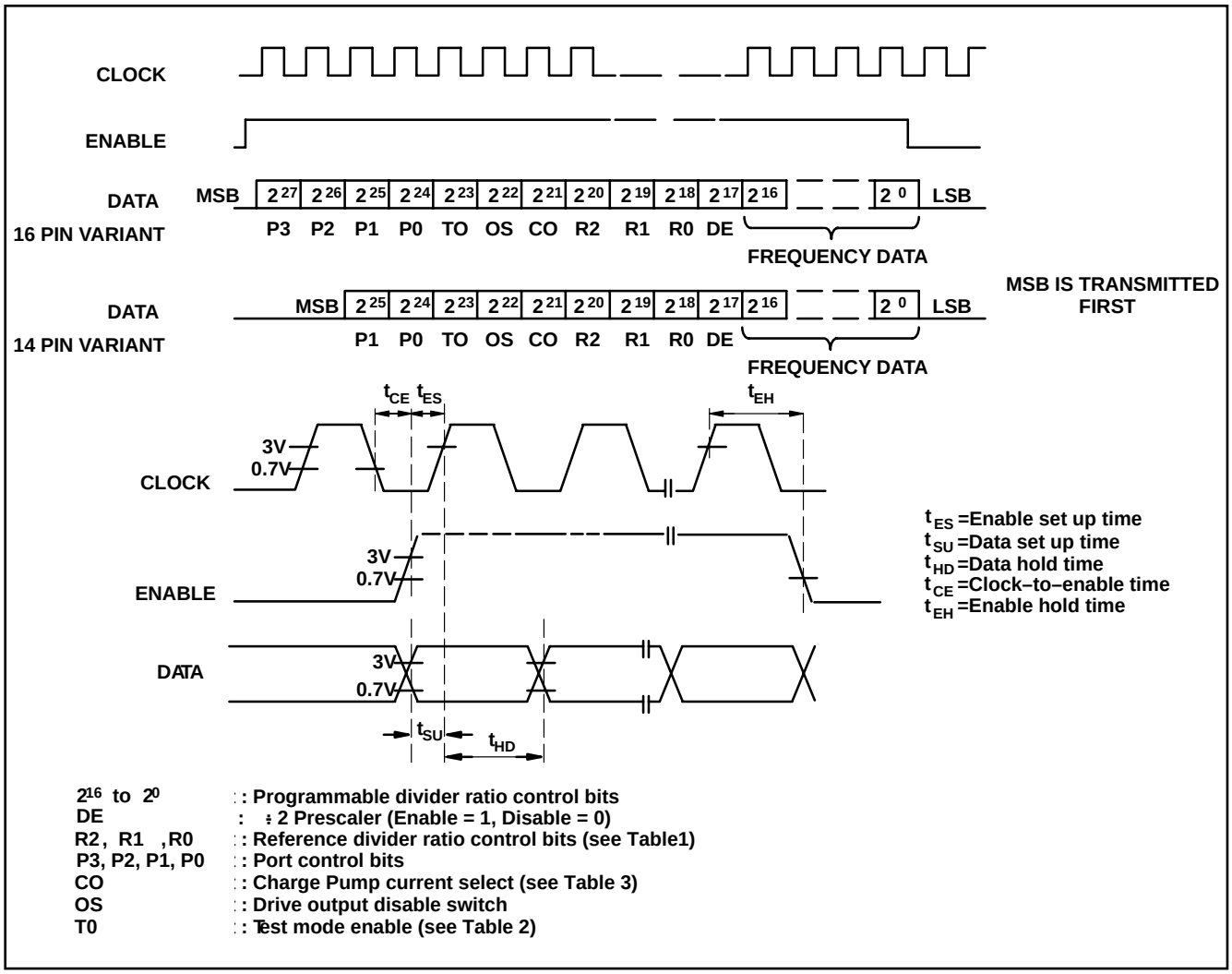


Fig. 3 Data format and timing

R2	R1	R0	RATIO	Comparison Frequency with a 4MHz external reference.
0	0	0	2	2MHz
0	0	1	4	1MHz
0	1	0	8	500kHz
0	1	1	16	250kHz
1	0	0	32	125kHz
1	0	1	64	62.5kHz
1	1	0	128	31.25kHz
1	1	1	256	15.625kHz

Table 1 Reference division ratios

TO	OS	DIS	P0/OP	P1/0C	FUNCTIONAL DESCRIPTION
0	0	0	#	#	NORMAL OPERATION
0	0	1	#	#	CHARGE PUMP DISABLE
1	0	0	F pd/2	F comp	NORMAL OPERATION
0	1	0	#	#	VARACTOR LINE DISABLE
0	1	1	#	#	CHARGE PUMP AND VARACTOR LINE DISABLE
1	X	1	–	–	NOT PERMITTED
# CONTROLLED BY BITS P0 AND P1 WITHIN DATA WORD					

Table 2 Test modes

C0	CURRENT IN mA		
	MIN	TYP	MAX
0	0.23	0.3	0.37
1	0.68	0.9	1.12

Table 3 Charge pump current

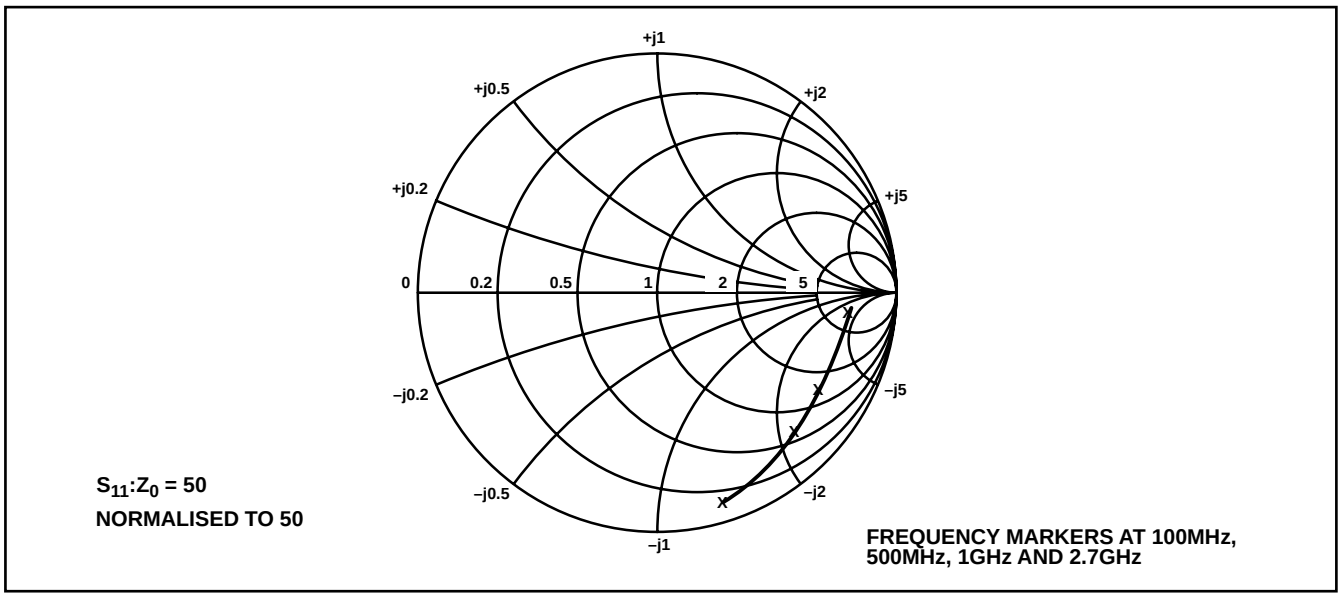


Fig. 4 Typical input impedance

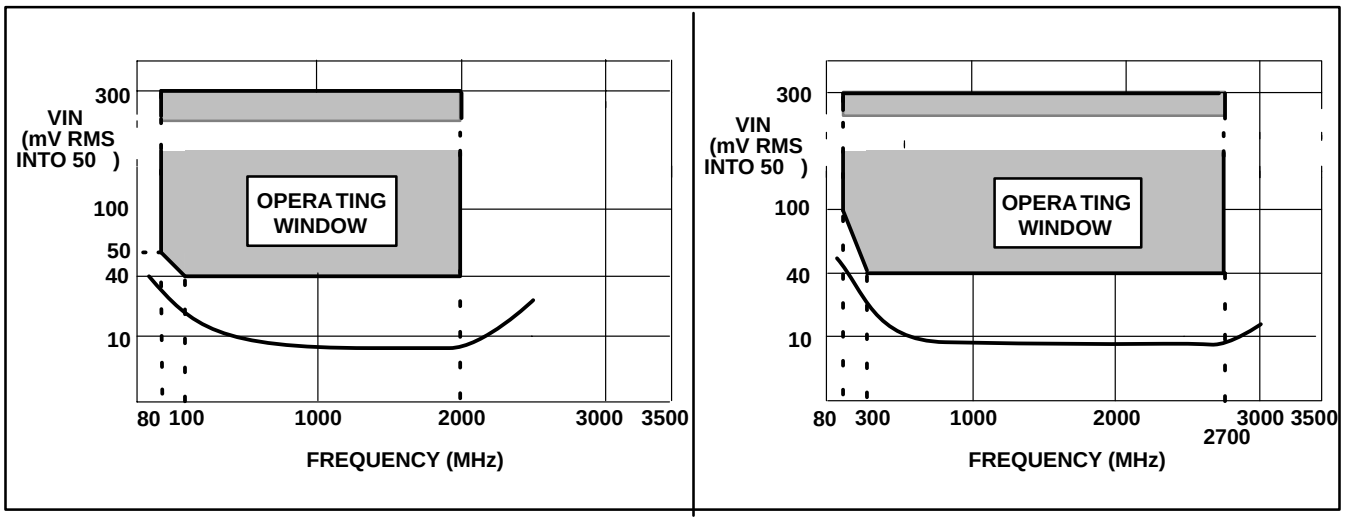


Fig. 5a Typical input sensitivity (Prescaler disabled, DE=0)

Fig. 5b Typical input sensitivity (Prescaler enabled, DE=1)

DOUBLE CONVERSION TUNER SYSTEMS

The high 2.7GHz maximum operating frequency and excellent noise characteristics of the SP5658 enables the construction of double conversion high IF tuners.

A typical system shown in Fig.7 will use the SP5658 as the first LO control for full band upconversion to an IF of greater than 1GHz. The wide range of reference division ratios allows the SP5658 to be used both for the up converter LO with a high phase comparator frequency (hence low phase noise) and the down converter which utilises the device in a lower comparison frequency mode (which offers a fine step size).

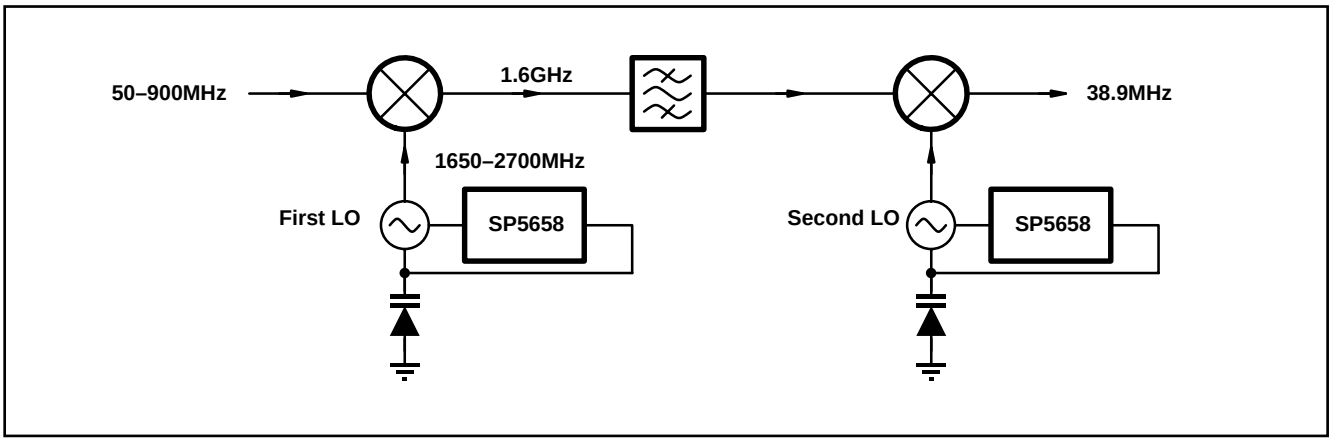


Fig. 6 Example of double conversion from VHF/UHF frequencies to TV IF

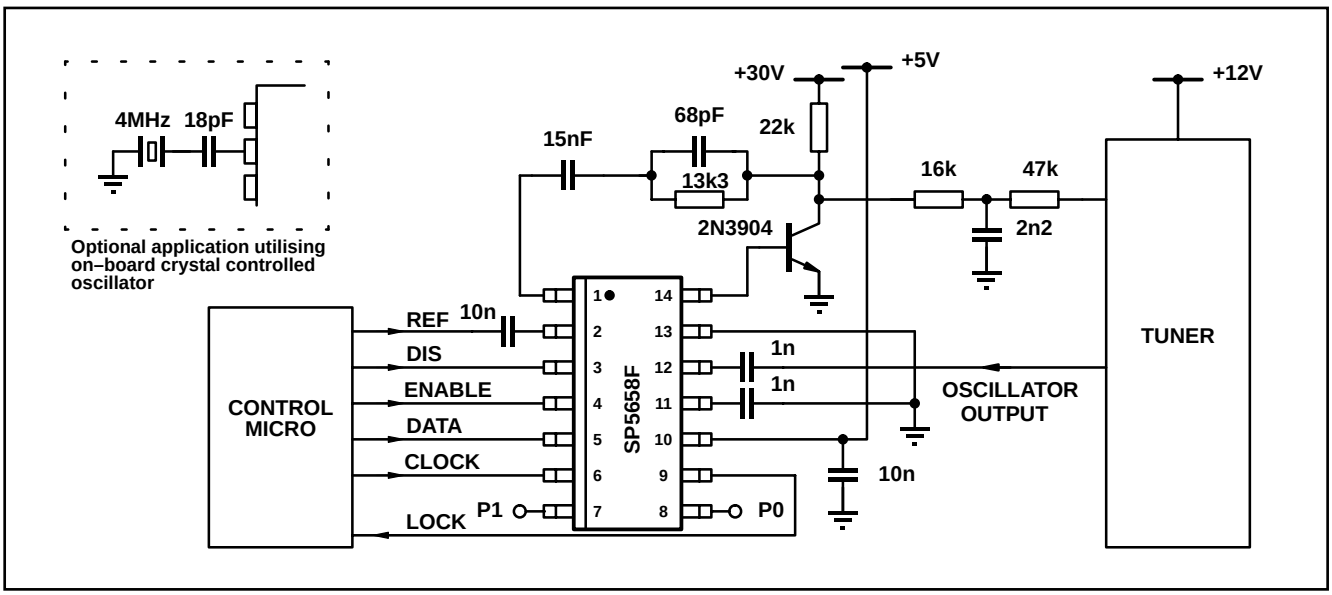


Fig. 7 Typical application, SP5658F

APPLICATION NOTES

A generic set of application notes AN168 for designing with synthesisers such as the SP5658 has been written. This covers aspects such as loop filter design and decoupling. This application note is also featured in the Media IC Handbook.

A generic test/demo board has been produced which can be used for the SP5658. A circuit diagram and layout for the board is shown in Figs. 8 and 9.

The board can be used for the following purposes:
(A) measuring RF sensitivity performance.
(B) Indicating port function.
(C) Synthesising a voltage controlled oscillator.
(D) Testing of external reference sources.

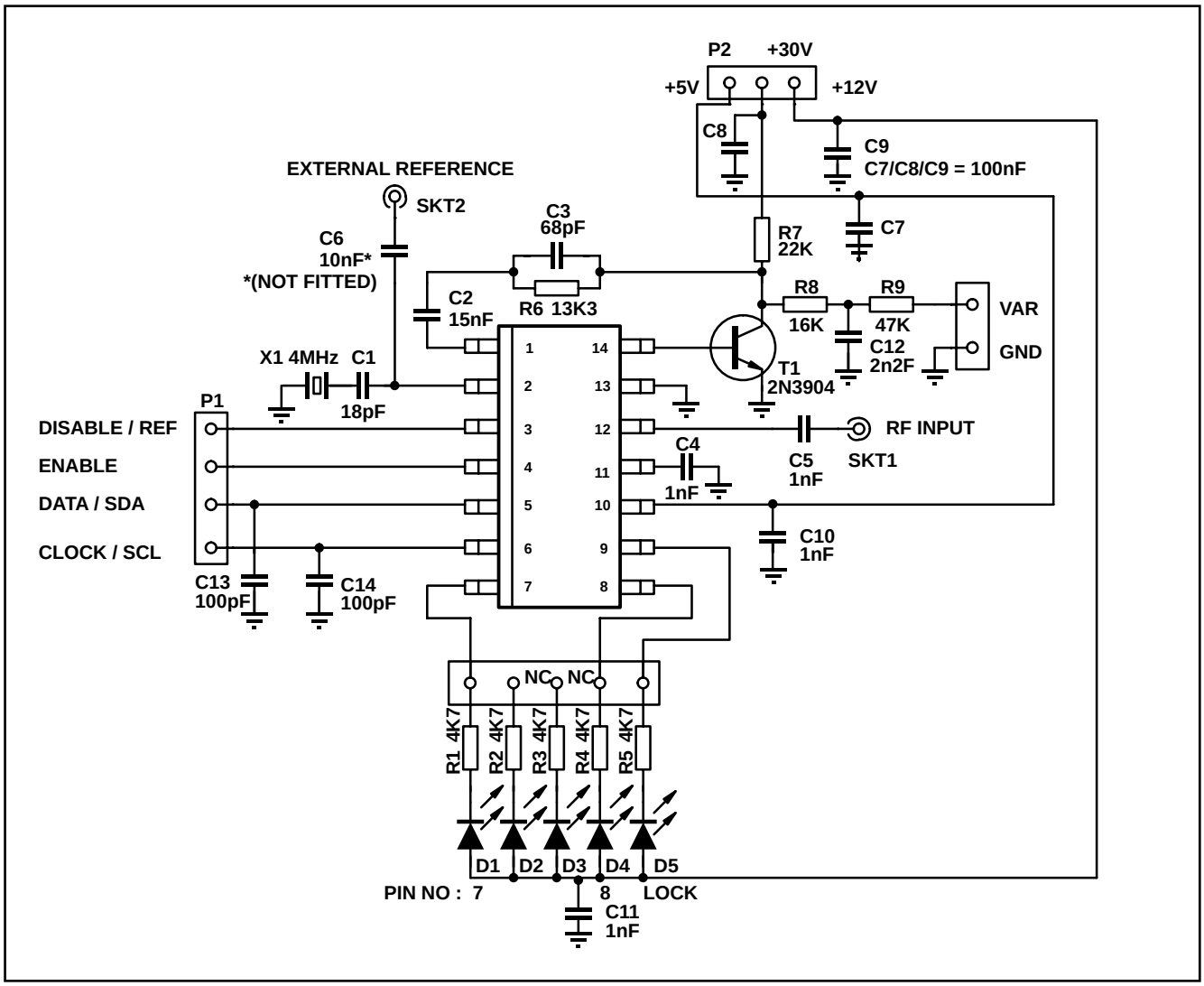


Fig. 8 Test board

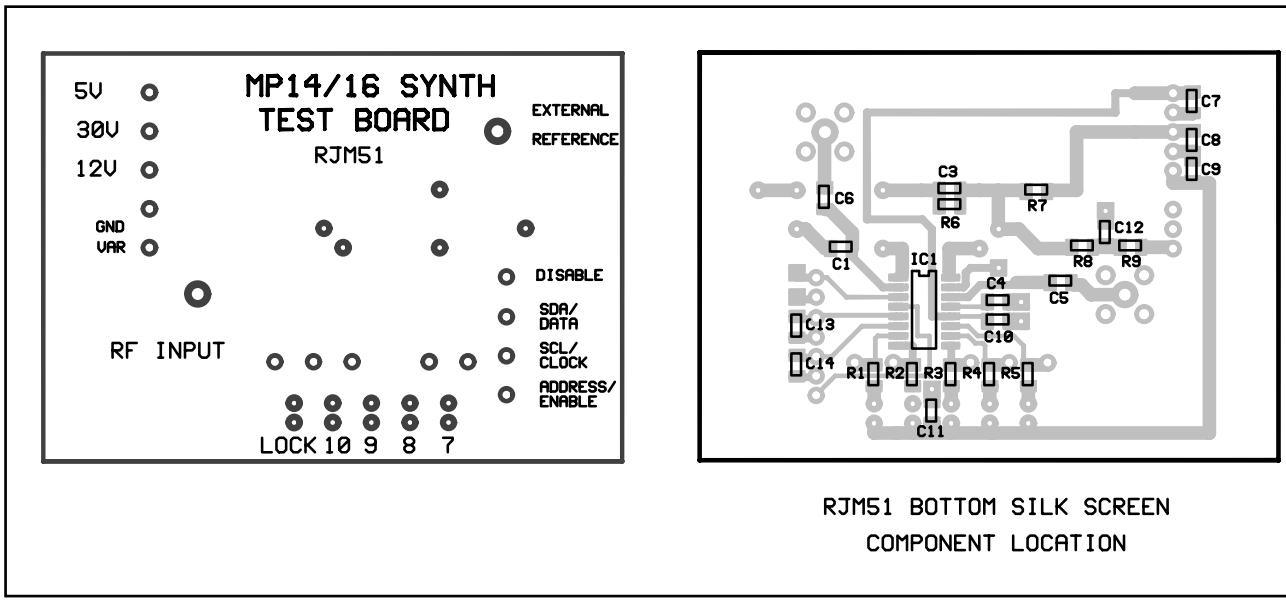


Fig. 9 Test board (layout)

LOOP BANDWIDTH

The majority of applications for which the SP5658 is intended require a loop filter bandwidth of between 2kHz and 10kHz.

Typically the VCO phase noise will be specified at both 1kHz and10kHz offset. It is common practice to arrange the loop filter bandwidth such that the 1kHz figure lies within the loop bandwidth. Thus the phase noise depends on the synthesiser comparator noise floor, rather than the VCO.

The 10kHz offset figure should depend on the VCO providing the loop is designed correctly, and is not underdamped.

REFERENCE SOURCE

The SP5658 offers optimal LO phase noise performance when operated with a large step size. This is due to the fact that the LO phase noise within the loop bandwidth is:

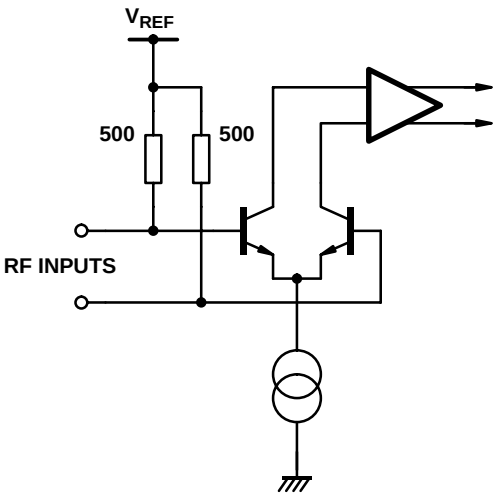
$$\text{phase comparator noise floor} \quad + 20 \log_{10} \left(\frac{\text{LO frequency}}{\text{phase comparator frequency}} \right)$$

Assuming the phase comparator noise floor is flat irrespective of sampling frequency, this means that the best performance will be achieved when the overall LO to phase comparator division ratio is a minimum.

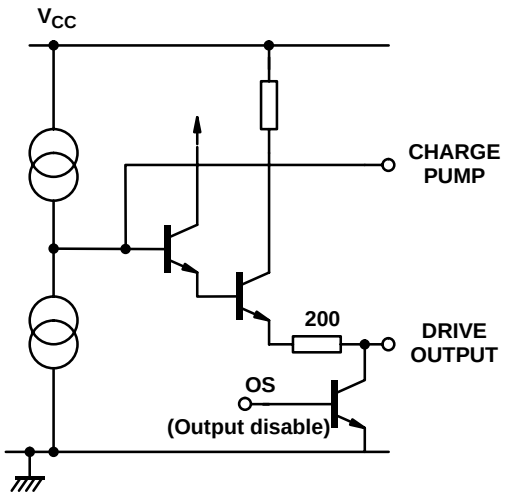
There are two ways of achieving a higher phase comparator sampling frequency:–

A) Reduce the division ratio between the reference source and the phase comparator
B) use a higher reference source frequency.

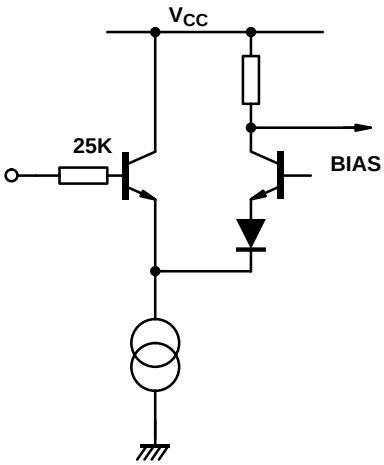
Approach B) may be preferred for best performance since it is possible that the noise floor of the reference oscillator may degrade the phase comparator performance if the reference division ratio is very small.



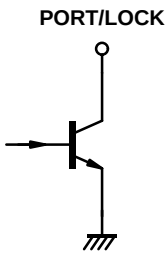
RF inputs



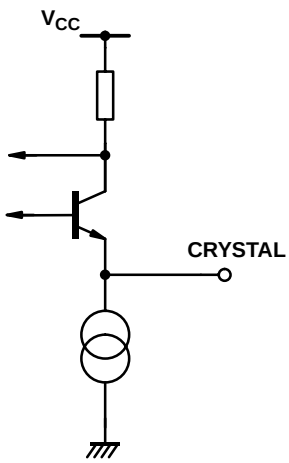
Loop amplifier



Disable, Enable, Data and Clock inputs

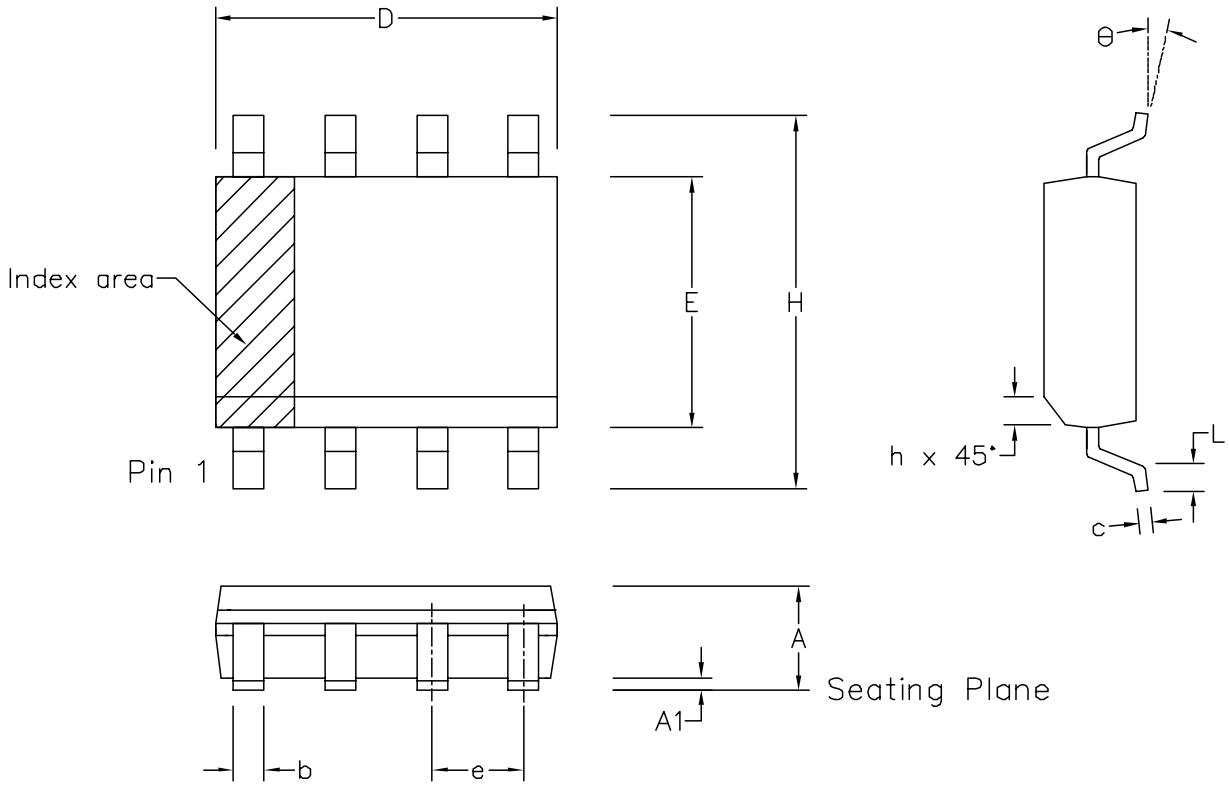


Output Ports and Lock Output



Reference oscillator

Fig. 10 Input/Output interface circuits



	Min mm	Max mm	Min inch	Max inch
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	9.80	10.00	0.386	0.394
H	5.80	6.20	0.228	0.244
E	3.80	4.00	0.150	0.157
L	0.40	1.27	0.016	0.050
e	1.27 BSC		0.050 BSC	
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
Θ	0°	8°	0°	8°
h	0.25	0.50	0.010	0.020
	Pin Features			
N	16		16	
Conforms to JEDEC MS-012AC Iss. C				

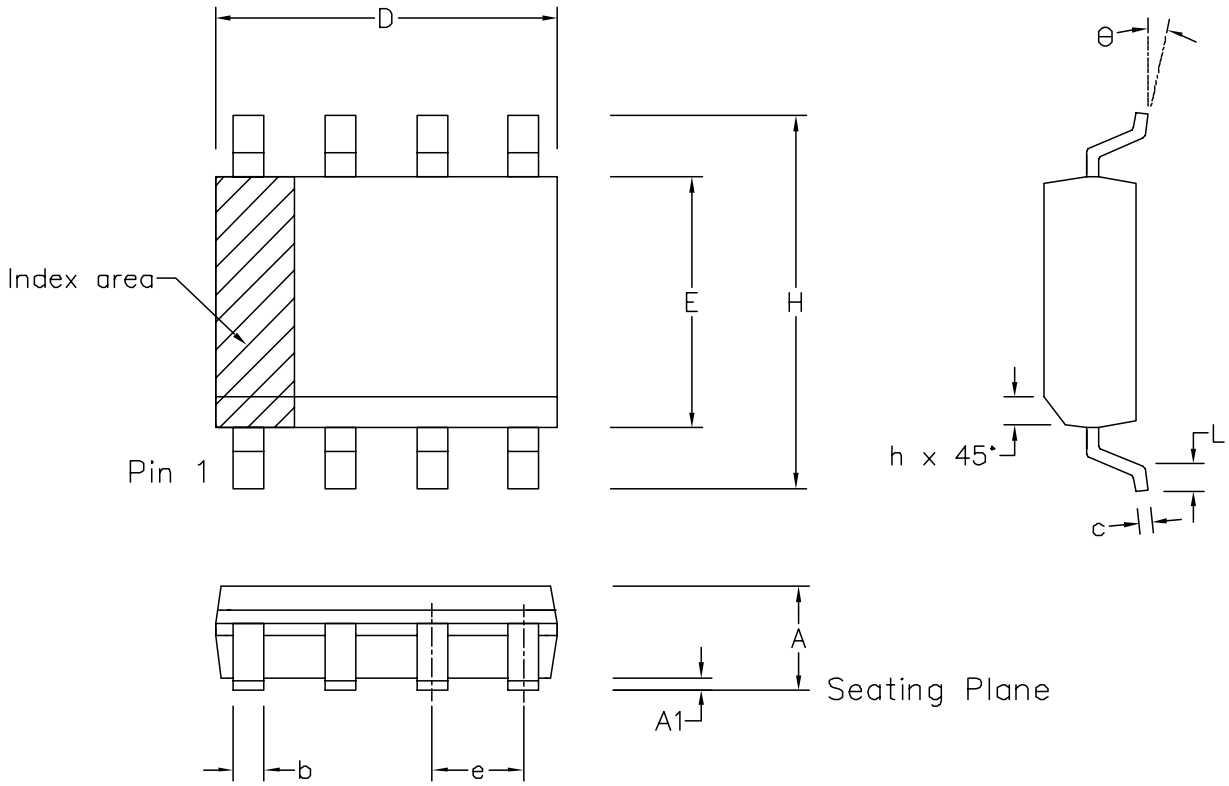
Notes:
1. The chamfer on the body is optional. If it not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in inches.
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion/intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

ISSUE	1	2	3	4	
ACN	006745	201938	202597	203706	
DATE	7APR95	27FEB97	12JUN97	9DEC97	
APPROVED					

ORIGINATING SITE: SWINDON

Title: Package Outline Drawing for 16 lds SOIC(N)-0.150" Body Width (MP)

Drawing Number
GPD00012



	Min mm	Max mm	Min inch	Max inch
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	8.55	8.75	0.337	0.344
H	5.80	6.20	0.228	0.244
E	3.80	4.00	0.150	0.157
L	0.40	1.27	0.016	0.050
e	1.27 BSC		0.050 BSC	
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
Θ	0°	8°	0°	8°
h	0.25	0.50	0.010	0.020
	Pin Features			
N	14		14	
Conforms to JEDEC MS-012AB Iss. C				

Notes:
1. The chamfer on the body is optional. If it not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in inches.
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ISSUE	1	2	3	4	
ACN	006745	201937	202596	203707	
DATE	7APR95	27FEB97	12JUN97	9DEC97	
APPROVED					

ORIGINATING SITE: SWINDON

Title: Package Outline Drawing for 14 lds SOIC(N)-0.150" Body Width (MP)

Drawing Number
GPD00011

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