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Interfacing 16Cxxx UARTs to a CPU

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Introduction

Due to the variety of CPUs that can be used in conjunction with UARTs, an understanding of a UART's CPU interface is useful. This allows establishing the compatibility of a particular CPU bus and the design for minimal glue logic as well as optimized bus cycle timing.

UARTs are usually driven by a CPU. EXAR's 16Cxxx UART family (16C45x, 16C55x, 16C65x and 16C85x 16C145x, 16C155x, 16C245x, 16C255x series) directly supports the INTEL bus interface. INTEL-derived CPUs are commonly interfaced to these UARTs despite data-, address- and control-bus timing variations from CPU type to CPU type.

It is possible to control UARTs by programmable logic, like FPGAs, instead of a CPU or microcontroller. This also affords a clear understanding of the interface logic.

Control Logic

Internal to the 16Cxxx UARTs, the CPU-bus control signals IOR#, IOW# and CS# are logically associated as shown in Figure 1.

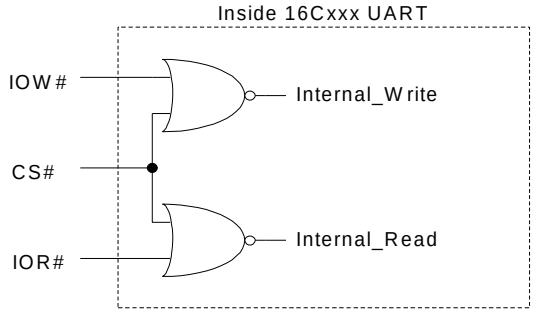

Figure 1

Hence the sequence of applying IOR# and CS# during a Read Cycle and IOW# and CS# during a Write Cycle is unimportant. The following discussion thus refers to the internal UART signals (IOR# +CS#) and (IOW# + CS#) instead of IOR#, IOW# and CS#.

Read Cycle

In order for the CPU to perform a Read of the UART's registers, the bus signal sequence should conform to the timing shown in Figure 2.

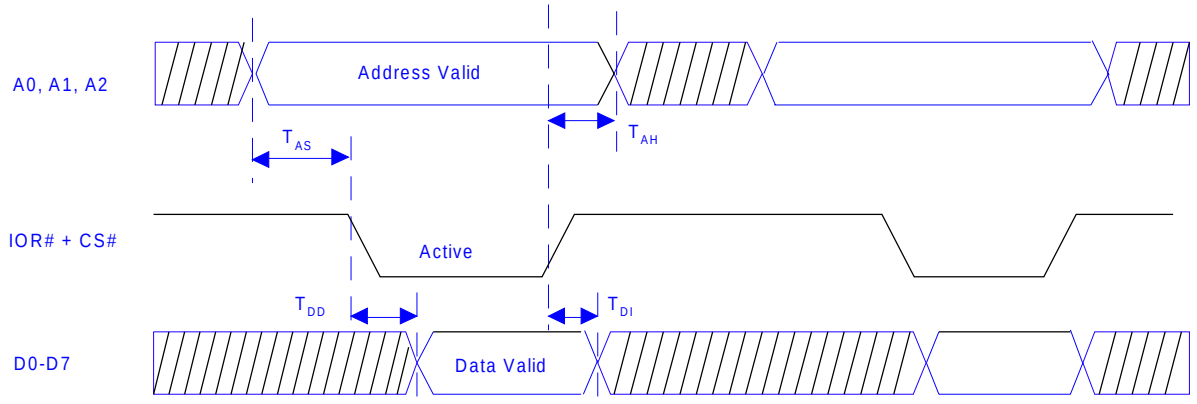

Figure 2: Read Cycle

The address stable time has to span the (IOR# + CS#) active period – even if the data is read early in this period. The reason being that the address bus is not latched edge triggered, but is level sensitive. Hence, changing the address during the IOR/CS active period may cause a read of another register – whose contents could subsequently change.

An example of this is the case for an unintended read of the ISR register when an interrupt is pending. This would clear the interrupt.

Write Cycle

The Write Timing of the 16Cxxx UARTs should comply with the timing shown in Figure. 3.

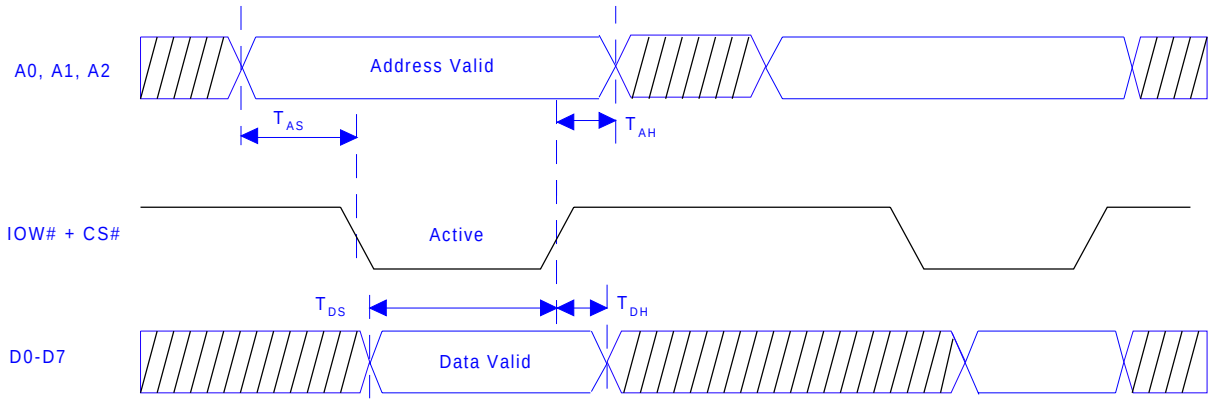

Figure 3: Write Cycle

The UART latches the data on the (IOW# + CS#) rising edge. The address bus needs to be stable during the whole (IOW# + CS#) active period.

Timing Parameters

The values of the Timing Parameters shown in the above Figures are specified in the Electrical Characteristics Table, Figure 4. These are common to all of EXAR's 16Cxxx family of UARTs and are representative of the design and technology of UARTs manufactured since early 1997.

Symbol	Parameter	Limits 3.3V Min	Limits 3.3V Max	Limits 5V Min	Limits 5V Max	Units	Conditions
T_{AS}	Address Setup Time	10		5		ns	
T_{AH}	Address Hold Time	10		5		ns	
T_{DY}	Data Delay Time		50		35	ns	100pF load
T_{DI}	Data Disable Time		35		25	ns	100pF load
T_{DS}	Data Setup Time	10		5		ns	
T_{DH}	Data Hold Time	10		5		ns	

Figure 4: Timing Parameter Specifications

The Data Delay Time, T_{DY}, and the Data Disable Time, T_{DI}, depend on the data bus loading that the UARTs sees during the write cycle. Hence a lighter load will result in faster times.

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