

## FSK power line transceiver

### General features

- Half-duplex frequency shift keying (FSK) transceiver
- Integrated power line driver with programmable voltage and current control
- Programmable mains access:
  - Synchronous
  - Asynchronous
- Single supply voltage (from 7.5V up to 13.5V)
- Very low power consumption ( $I_q = 5\text{mA}$ )
- Integrates 5V voltage regulator (up to 50mA) with short circuit protection
- Integrated 3.3V voltage regulator (up to 50mA) with short circuit protection
- 3.3V or 5V digital supply
- 8 Programmable transmission frequencies
- Programmable baud rate up to 4800BPS
- Receiving sensitivity up to  $250\mu\text{V}_{\text{RMS}}$
- Suitable for applications in accordance with EN 50065 Cenelec specification
- Carrier or preamble detection
- Band in use detection
- Programmable control register
- Watchdog timer
- 8 or 16 Bit header recognition
- ST7537 and ST7538 compatible
- UART/SPI host interface



### Description

The ST7540 is a Half Duplex synchronous/asynchronous FSK Modem designed for power line communication network applications. It operates from a single supply voltage and integrates a line driver and two linear regulators for 5V and 3.3V. The device operation is controlled by means of an internal register, programmable through the synchronous serial interface. Additional functions as watchdog, clock output, output voltage and current control, preamble detection, time-out and band in use are included. Realized in Multipower BCD5 technology that allows to integrate DMOS, Bipolar and CMOS structures in the same chip.

### Order codes

| Part number | Package                | Packaging     |
|-------------|------------------------|---------------|
| ST7540      | HTSSOP28 (Exposed Pad) | Tube          |
| ST7540TR    | HTSSOP28 (Exposed Pad) | Tape and reel |

# Contents

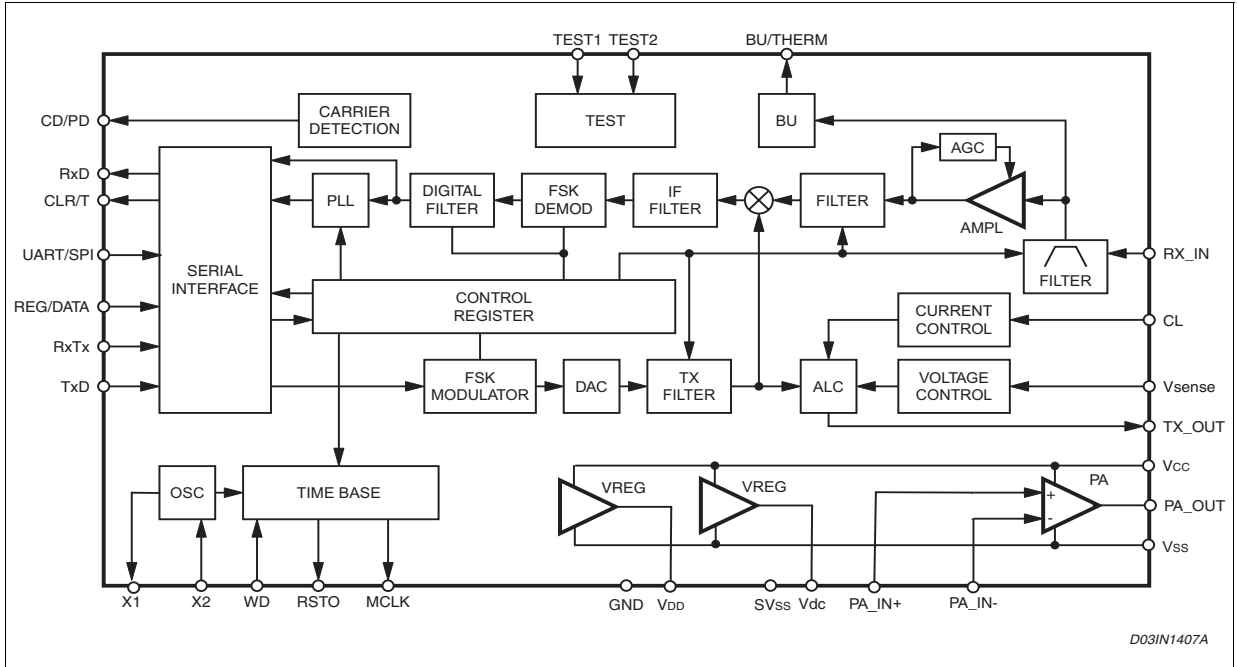
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# 1 Block diagram

Figure 1. Block diagram

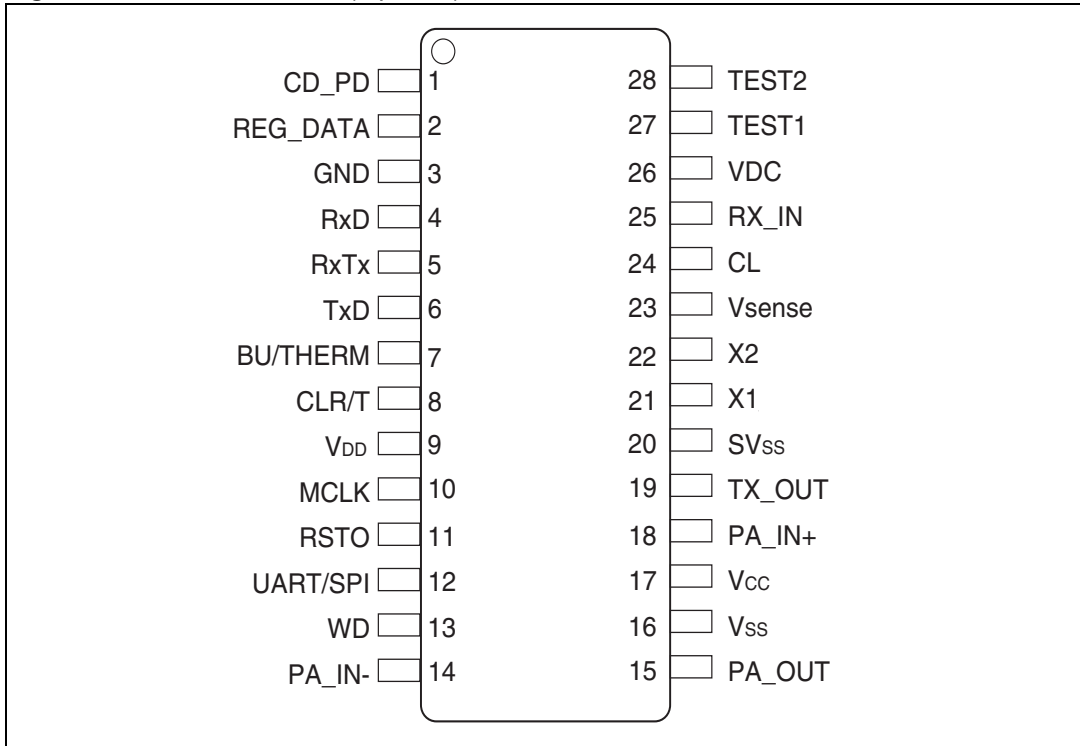


D03IN1407A

## 2 Pin settings

### 2.1 Pin connection

Figure 2. Pin connection (top view)



### 2.2 Pin description

Table 1. Pin description

| N° | Name     | Type                                     | Description   |
|----|----------|--|---|
| 1  | CD_PD    | Digital/Output                           | Carrier, preamble or frame header detect output.<br>"1" No carrier, preamble or frame header detected<br>"0" Carrier, preamble or frame header detected |
| 2  | REG_DATA | Digital/Input<br>with internal pull-down | Mains or control register access selector<br>"1" - Control register access<br>"0" - Mains access  |
| 3  | GND      | Supply                                   | Digital ground  |
| 4  | RxD      | Digital/Output                           | RX data output.   |
| 5  | RxTx     | Digital/Input<br>with internal pull-up   | Rx or Tx mode selection input.<br>"1" - RX Session<br>"0" - TX Session  |
| 6  | TxD      | Digital/Input<br>with internal pull-down | TX data input.  |

Table 1. Pin description (continued)

| N° | Name                              | Type                                  | Description  |
|----|-----------------------------------|---------------------------------------|--|
| 7  | BU/THERM                          | Digital/Output                        | Band in use/Thermal Shutdown event detection output.<br>In Rx mode:<br>"1" Signal within the programmed band<br>"0" No signal within the programmed band<br>In Tx mode:<br>"1" - Thermal Shutdown event occurred<br>"0" - No Thermal Shutdown event occurred<br>(signal not latched) |
| 8  | CLR/T                             | Digital/Output                        | Synchronous mains access clock or control register access clock  |
| 9  | V <sub>DD</sub>                   | Supply/Power                          | Digital supply voltage or 3.3V voltage regulator output  |
| 10 | MCLK                              | Digital/Output                        | Master clock output  |
| 11 | RSTO                              | Digital/Output                        | Power ON or watchdog reset output  |
| 12 | UART/SPI                          | Digital/Input with internal pull-down | Interface type:<br>"0" - Serial peripheral interface<br>"1" - UART interface   |
| 13 | WD                                | Digital/Input with internal pull-up   | Watchdog input. The internal watchdog counter is cleared on the falling edges.   |
| 14 | PA_IN-                            | Analog/Input                          | Power line amplifier inverting input   |
| 15 | PA_OUT                            | Power/Output                          | Power line amplifier output  |
| 16 | V <sub>SS</sub>                   | Supply                                | Power analog ground  |
| 17 | V <sub>CC</sub>                   | Supply                                | Power supply voltage   |
| 18 | PA_IN+                            | Analog/Input                          | Power line amplifier not inverting input   |
| 19 | TX_OUT                            | Analog/Output                         | Small signal analog transmit output  |
| 20 | SV <sub>SS</sub>                  | Supply                                | Analog signal ground   |
| 21 | X1                                | Analog/Output                         | Crystal oscillator output  |
| 22 | X2                                | Analog/Input                          | Crystal oscillator input - or external clock input   |
| 23 | V <sub>SENSE</sub> <sup>(1)</sup> | Analog/Input                          | Output voltage sensing input for the voltage control loop  |
| 24 | CL <sup>(2)</sup>                 | Analog/Input                          | Current limiting feedback.<br>A resistor between CL and SV <sub>SS</sub> sets the PLI current limiting value. An integrated 80pF filtering input capacitance is present on this pin.   |
| 25 | RX_IN                             | Analog/Input                          | Receiving analog input   |
| 26 | VDC                               | Power                                 | 5V voltage regulator output  |
| 27 | TEST1                             | Digital/Input with internal pull-down | Test input. Must be connected to GND.  |
| 28 | TEST2                             | Analog/Input                          | Test input. Must be connected SV <sub>SS</sub>   |

1. Cannot be left floating

2. Cannot be left floating

## 3 Electrical data

### 3.1 Maximum ratings

**Table 2. Absolute maximum ratings**

| Symbol                                | Parameter  | Value                             | Unit              |
|---------------------------------------|--|-----------------------------------|-------------------|
| $V_{CC}$                              | Power supply voltage   | -0.3 to + 14                      | V                 |
| $V_{DD}$                              | Digital supply voltage   | -0.3 to +5.5                      | V                 |
| $SV_{SS}/GND$                         | Voltage between $SV_{SS}$ and GND  | -0.3 to +0.3                      | V                 |
| $V_I$                                 | Digital input voltage  | GND - 0.3 to $V_{DD} + 0.3$       | V                 |
| $V_O$                                 | Digital output voltage   | GND - 0.3 to $V_{DD} + 0.3$       | V                 |
| $I_O$                                 | Digital output current   | -2 to +2                          | mA                |
| $V_{sense}, X2, PA\_IN-, PA\_IN+, CL$ | Voltage range at $V_{sense}, X2, PA\_IN-, PA\_IN+, CL$ Inputs                              | $SV_{SS} - 0.3$ to 5.6            | V                 |
| RX_IN                                 | Voltage range at RX_IN input   | -5.6 to 5.6                       | V                 |
| TX_OUT, X1                            | Voltage range at TX_OUT, X1 outputs  | $SV_{SS} - 0.3$ to 5.6            | V                 |
| PA_OUT                                | Voltage range at powered PA_OUT Output   | $V_{SS} - 0.3$ to $+V_{CC} + 0.3$ | V                 |
| $I(PA\_OUT)$                          | Power line driver output current <sup>(1)</sup>  | 650                               | mA <sub>rms</sub> |
| $T_A$                                 | Operating ambient temperature  | -40 to +85                        | °C                |
| $T_{STG}$                             | Storage temperature  | -50 to 150                        | °C                |
| RxD, PA_OUT Pin                       | Maximum withstanding voltage range<br>Test condition: CDF-AEC-Q100-002- "Human Body Model" | ±1750                             | V                 |
| Other pins                            | Acceptance criteria: "Normal Performance"  | ±2000                             | V                 |

1. This current is intended as not repetitive pulse current

### 3.2 Thermal data

**Table 3. Thermal data**

| Symbol      | Parameter   | HTSSOP28 Exposed Pad | Unit |
|-------------|---|----------------------|------|
| $R_{thJA1}$ | Maximum thermal resistance junction-ambient steady state <sup>(1)</sup> | 35                   | °C/W |
| $R_{thJA2}$ | Maximum thermal resistance junction-ambient Steady State <sup>(2)</sup> | 70                   | °C/W |

1. Mounted on Multilayer PCB with a dissipating surface on the bottom side of the PCB

2. It is the same condition of the point above, without any heatsinking surface on the board.

### 3.3 Recommended operating conditions

**Table 4. Recommended operating conditions**

| Symbol            | Parameter   | Test Condition   | Value        | Unit     |
|-------------------|---|--|--------------|----------|
| $V_{CC}$          | Max allowed slope during Power-up   |  | 100          | V/ms     |
| $I(V_{CC})$       | Powered analog supply Current with digital supply provided externally             | Maximum total current  | 650          | mArms    |
| $V_{CC} - V_{DD}$ | Maximum voltage Difference between $V_{CC}$ and $V_{DD}$ during power-up sequence | $V_{DD} < 4.75V$ with 5V Digital supply provided externally                        | 1.2          | V        |
| $V_{PA\_OUT}$     | Output voltage swing for PA_OUT pin   |  | $V_{CC}-4.5$ | $V_{PP}$ |
| $I(PA\_OUT)$      | Maximum output transmitting current in programmable current limiting              | $R_{cl} = 1.4k\Omega$ ; $R_{LOAD} = 1\Omega$<br>(as in <a href="#">Figure 17</a> ) | 500          | mArms    |



## 4 Electrical characteristics

**Table 5. Electrical characteristics**

( $V_{DD} = +5V$ ,  $V_{CC} = +9V$ ,  $V_{SS} = SV_{SS} = GND = 0V$ ,  $-40^{\circ}C \leq T_A \leq 85^{\circ}C$ ,  $T_J < 125^{\circ}C$ , unless otherwise specified)

| Symbol              | Parameter  | Test condition                                       | Min. | Typ. | Max. | Unit  |
|---------------------|--|--|------|------|------|-------|
| $V_{DD}$            | Digital supply voltages                                      | 5V Digital supply provided externally                | 4.75 | 5    | 5.25 | V     |
| $V_{CC}$            | Power supply voltage   |  | 7.5  |      | 13.5 | V     |
| $I(V_{DD})$         | Digital input supply current                                 | Transmission & receiving mode (MCLK = 4MHz), no load |      |      | 3.5  | mA    |
|                     |  | Transmission & Receiving mode (MCLK = OFF), no load  |      |      | 1.5  | mA    |
| $I(V_{CC})$         | Power supply current with digital supply provided externally | TX mode, no load                                     |      |      | 60   | mArms |
|                     |  | RX mode  |      |      | 5    | mArms |
| UVLO                | Under voltage lock out Threshold on $V_{CC}$                 |  | 3.7  | 3.9  | 4.1  | V     |
| UVLO <sub>HYS</sub> | UVLO Hysteresis on $V_{CC}$                                  |  |      | 340  |      | mV    |

### Digital I/O

|            |                             |  |      |     |      |            |
|------------|-----------------------------|--|------|-----|------|------------|
| $R_{down}$ | Internal pull down resistor |  | -30% | 100 | +30% | k $\Omega$ |
| $R_{up}$   | Internal pull up resistor   |  | -30% | 100 | +30% | k $\Omega$ |

### Digital I/O - 5V digital supply

|          |                                 |                 |                 |  |           |   |
|----------|---------------------------------|-----------------|-----------------|--|-----------|---|
| $V_{IH}$ | High logic level input voltage  |                 | 2               |  |           | V |
| $V_{IL}$ | Low logic level input voltage   |                 |                 |  | 1.2       | V |
| $V_{OH}$ | High logic level output voltage | $I_{OH} = -2mA$ | $V_{DD} - 0.45$ |  |           | V |
| $V_{OL}$ | Low logic level output voltage  | $I_{OL} = 2mA$  |                 |  | GND + 0.3 | V |

### Digital I/O - 3.3V digital supply

|          |                                |  |     |  |     |   |
|----------|--------------------------------|--|-----|--|-----|---|
| $V_{IH}$ | High logic level input voltage |  | 1.4 |  |     | V |
| $V_{IL}$ | Low logic level input voltage  |  |     |  | 0.8 | V |

**Table 5. Electrical characteristics** (continued)

( $V_{DD} = +5V$ ,  $V_{CC} = +9V$ ,  $V_{SS} = SV_{SS} = GND = 0V$ ,  $-40^{\circ}C \leq T_A \leq 85^{\circ}C$ ,  $T_J < 125^{\circ}C$ , unless otherwise specified)

| Symbol                | Parameter   | Test condition                                       | Min.            | Typ.     | Max.      | Unit      |
|-----------------------|---|--|-----------------|----------|-----------|-----------|
| $V_{OH}$              | High logic level output voltage                             | $I_{OH} = -2mA$                                      | $V_{DD} - 0.75$ |          |           | V         |
| $V_{OL}$              | Low logic level output voltage                              | $I_{OL} = 2mA$                                       |                 |          | GND + 0.4 | V         |
| <b>Oscillator</b>     |   |  |                 |          |           |           |
| External Clock        | X2 voltage swing  | External clock. <a href="#">Figure 4</a>             |                 | 5        |           | $V_{pp}$  |
| External Clock        | X2 DC voltage level   | External clock. <a href="#">Figure 4</a>             |                 | 2.5      |           | V         |
| DC                    | XTAL Clock duty cycle                                       | External clock.                                      | 40              |          | 60        | %         |
| Xtal                  | Crystal oscillator frequency                                | fundamental  | 16              |          |           | MHz       |
| $Xtal_{ESR}$          | External oscillator esr resistance                          |  |                 |          | 40        | $\Omega$  |
| $Xtal_{CL}$           | External oscillator stabilization capacitance               | <a href="#">Figure 6</a>                             |                 |          | 16        | pF        |
| <b>Transmitter</b>    |   |  |                 |          |           |           |
| $I_{TX\_OUT}$         | Output transmitting current on TX_OUT                       |  |                 |          | 1         | mArms     |
| $V_{TX\_OUT}$         | Max carrier output AC voltage                               | $R_{CL} = 1.4k\Omega$<br>$V_{sense} = 0V$            | 1.75            | 2.3      | 3.5       | $V_{PP}$  |
| $V_{TX\_OUTDC}$       | Output DC voltage on TX_OUT                                 |  | 1.7             | 2.1      | 2.5       | V         |
| HD2 <sub>TX_OUT</sub> | Second harmonic distortion on TX_OUT                        | $V_{TX\_OUT} = 2V_{PP}$ ;<br>$F_c = 86KHz$ , no load |                 |          | -42       | $dB_c$    |
| HD3 <sub>TX_OUT</sub> | Third harmonic distortion on TX_OUT                         | $V_{TX\_OUT} = 2V_{PP}$ ;<br>$F_c = 86KHz$ , no load |                 |          | -49       | $dB_c$    |
| G accuracy            | Accuracy on voltage control loop active                     | $R_{CL} = 0\Omega$                                   | -1              |          | +1        | GST       |
| $G_{ST}$              | ALC gain step control loop gain step                        |  | 0.6             | 1        | 1.4       | dB        |
| DRNG                  | ALC dynamic range   |  |                 | 30       |           | dB        |
| $C_{CL}$              | Input capacitance on CL pin                                 |  |                 | 80       |           | pF        |
| $V_{senseTH}$         | Voltage control loop reference threshold on $V_{sense}$ pin | <a href="#">Figure 17</a>                            | 160             | 180      | 200       | $mV_{PK}$ |
| $V_{senseHYST}$       | Hysteresis on voltage loop reference threshold              | <a href="#">Figure 17</a>                            |                 | $\pm 18$ |           | mV        |

**Table 5. Electrical characteristics** (continued)

( $V_{DD} = +5V$ ,  $V_{CC} = +9V$ ,  $V_{SS} = SV_{SS} = GND = 0V$ ,  $-40^{\circ}C \leq T_A \leq 85^{\circ}C$ ,  $T_J < 125^{\circ}C$ , unless otherwise specified)

| Symbol                 | Parameter   | Test condition                    | Min. | Typ.     | Max. | Unit       |
|------------------------|---|-----------------------------------|------|----------|------|------------|
| $V_{SENSE}$            | $V_{SENSE}$ Input impedance   |                                   |      | 36       |      | k $\Omega$ |
| $CL_{TH}$              | Current control loop reference threshold on CL pin                          | Figure 17                         | 1.80 | 1.90     | 2.00 | V          |
| $CL_{HYST}$            | Hysteresis on current loop reference threshold                              | Figure 17                         | 210  | 250      | 290  | mV         |
| $T_{RxTx}$             | Carrier activation time   | Figure 21 - 600 Baud Xtal = 16MHz |      |          | 1.6  | ms         |
|                        |   | Figure 21- 1200 Baud Xtal = 16MHz |      |          | 800  | $\mu$ s    |
|                        |   | Figure 21- 2400 Baud Xtal = 16MHz |      |          | 400  | $\mu$ s    |
|                        |   | Figure 21- 4800 Baud Xtal = 16MHz |      |          | 200  | $\mu$ s    |
| $T_{ALC}$              | Carrier stabilization time from STEP 16 to zero or from step 16 to step 31, | Figure 21 Xtal = 16MHz            |      |          | 3.2  | ms         |
| $T_{ST}$               | Tstep   | Figure 21 Xtal = 16MHz            |      |          | 200  | $\mu$ s    |
| <b>Power amplifier</b> |   |                                   |      |          |      |            |
| $PA_{IN(Offset)}$      | Input terminals OFFSET  |                                   |      | $\pm 18$ |      | mV         |
| GBWP                   | Gain bandwidth product  |                                   | 100  |          |      | MHz        |
| $R_{IN}$               | Input resistance at PA_IN+ and PA_IN- pins                                  | PA_IN+ vs. Vss <sup>(1)</sup>     | 1    |          |      | M $\Omega$ |
|                        |   | PA_IN- vs. Vss <sup>(1)</sup>     | 1    |          |      | M $\Omega$ |
| $C_{IN}$               | Input capacitance at PA_IN+ and PA_IN- pins                                 | PA_IN+ vs. Vss <sup>(1)</sup>     |      | 5        |      | pF         |
|                        |   | PA_IN- vs. Vss <sup>(1)</sup>     |      | 5        |      | pF         |
| CMRR                   | Common mode rejection ratio   |                                   |      | 40       |      | dB         |

**Table 5. Electrical characteristics** (continued)

( $V_{DD} = +5V$ ,  $V_{CC} = +9V$ ,  $V_{SS} = SV_{SS} = GND = 0V$ ,  $-40^{\circ}C \leq T_A \leq 85^{\circ}C$ ,  $T_J < 125^{\circ}C$ , unless otherwise specified)

| Symbol                | Parameter                               | Test condition   | Min. | Typ. | Max. | Unit            |
|-----------------------|---|--|------|------|------|-----------------|
| HD2 <sub>PA_OUT</sub> | Second harmonic distortion on PA_OUT    | $V_{PA\_OUT} = 5.6V_{PP}$ ,<br>$V_{CC} = 12V$<br>$R_{LOAD} = 30\Omega$<br>Carrier frequency:<br>86KHz<br><i>Figure 3</i> |      |      | -63  | dB <sub>c</sub> |
| HD3 <sub>PA_OUT</sub> | Third harmonic distortion on PA_OUT pin | $V_{PA\_OUT} = 5.6V_{PP}$ ,<br>$V_{CC} = 12V$<br>$R_{LOAD} = 30\Omega$<br>Carrier frequency:<br>86KHz<br><i>Figure 3</i> |      |      | -63  | dB <sub>c</sub> |

**Receiver**

|                 |   |  |    |                 |     |                          |
|-----------------|---|--|----|-----------------|-----|--------------------------|
| V <sub>IN</sub> | Input sensitivity (Normal Mode)                       |  |    | 0.5             | 2   | mV <sub>rms</sub>        |
|                 | Input sensitivity (High Sens.)                        |  |    | 250             |     | μV <sub>rms</sub>        |
|                 | Input sensitivity (TxD line forced to "1")            |  |    | V <sub>BU</sub> |     | dB/<br>μV <sub>rms</sub> |
| V <sub>IN</sub> | Maximum input signal                                  |  |    |                 | 2   | V <sub>rms</sub>         |
| R <sub>IN</sub> | Input impedance                                       |  | 80 | 100             | 140 | kΩ                       |
| V <sub>CD</sub> | Carrier detection sensitivity (Normal Mode)           |  |    | 0.5             | 2   | mV <sub>rms</sub>        |
|                 | Carrier detection sensitivity (High Sensitivity Mode) |  |    | 250             |     | μV <sub>rms</sub>        |
|                 | Carrier detection sensitivity (TxD forced to "1")     |  |    | V <sub>BU</sub> |     | dB/<br>μV <sub>rms</sub> |
| V <sub>BU</sub> | Band in Use Detection Level                           |  |    | 83.5            | 86  | dB/<br>μV <sub>rms</sub> |

**Table 5. Electrical characteristics** (continued)

( $V_{DD} = +5V$ ,  $V_{CC} = +9V$ ,  $V_{SS} = SV_{SS} = GND = 0V$ ,  $-40^{\circ}C \leq T_A \leq 85^{\circ}C$ ,  $T_J < 125^{\circ}C$ , unless otherwise specified)

| Symbol                        | Parameter                                     | Test condition   | Min. | Typ.                                  | Max. | Unit                 |
|-------------------------------|---|--|------|---------------------------------------|------|----------------------|
| <b>5V Voltage regulator</b>   |   |  |      |                                       |      |                      |
| VDC                           | Linear regulator output voltage               | $0 < I_o < 50mA$<br>$7.5V < V_{CC} < 13.5V$                        | -5%  | 5.05                                  | +5%  | V                    |
| <b>3.3V Voltage regulator</b> |   |  |      |                                       |      |                      |
| V <sub>DD</sub>               | Linear regulator output voltage               | $0 < I_o < 50mA$<br>$7.5V < V_{CC} < 13.5V$                        | -5%  | 3.3                                   | +5%  | V                    |
| <b>Other functions</b>        |   |  |      |                                       |      |                      |
| T <sub>RSTO</sub>             | Reset time                                    | See <a href="#">Figure 23</a> ;<br>Xtal = 16MHz                    | 50   |                                       |      | ms                   |
| T <sub>WD</sub>               | Watch-dog pulse width                         | See <a href="#">Figure 23</a>                                      | 125  |                                       |      | ns                   |
| T <sub>WM</sub>               | Watch-dog pulse period                        | Minimum value.<br>See <a href="#">Figure 23</a>                    | 250  |                                       |      | ns                   |
|                               |   | Maximum value.<br>See <a href="#">Figure 23</a>                    |      |                                       | 1490 | ms                   |
| T <sub>WO</sub>               | Watch-dog time out                            | See <a href="#">Figure 23</a>                                      |      |                                       | 1.5  | s                    |
| T <sub>OUT</sub>              | TX time out                                   | Control register bit 7<br>and bit 8                                |      | 1<br>3                                |      | s                    |
| T <sub>OFF</sub>              | Time Out OFF time                             | <a href="#">Figure 22</a>  | 125  |                                       |      | ms                   |
| T <sub>OFFD</sub>             | RxTx 0->1 vs. time out delay                  | <a href="#">Figure 22</a>  |      |                                       | 20   | μs                   |
| T <sub>CD</sub>               | Carrier detection time selectable by register | Control register bit 9 and bit10<br><a href="#">Figure 14</a>      |      | 500<br>1<br>3<br>5                    |      | μs<br>ms<br>ms<br>ms |
| T <sub>DCD</sub>              | CD_PD Propagation delay                       | <a href="#">Figure 14</a>  |      | 300                                   | 500  | μs                   |
| M <sub>CLK</sub>              | Master clock output selectable by register    | Control register bit 15 and bit 16<br>See <a href="#">Table 12</a> |      | fclock<br>fclock/2<br>fclock/4<br>off |      | MHz                  |
| BAUD                          | Baud rate                                     | Control register bit 3 and bit 4<br>See <a href="#">Table 12</a>   |      | 600<br>1200<br>2400<br>4800           |      | Baud                 |

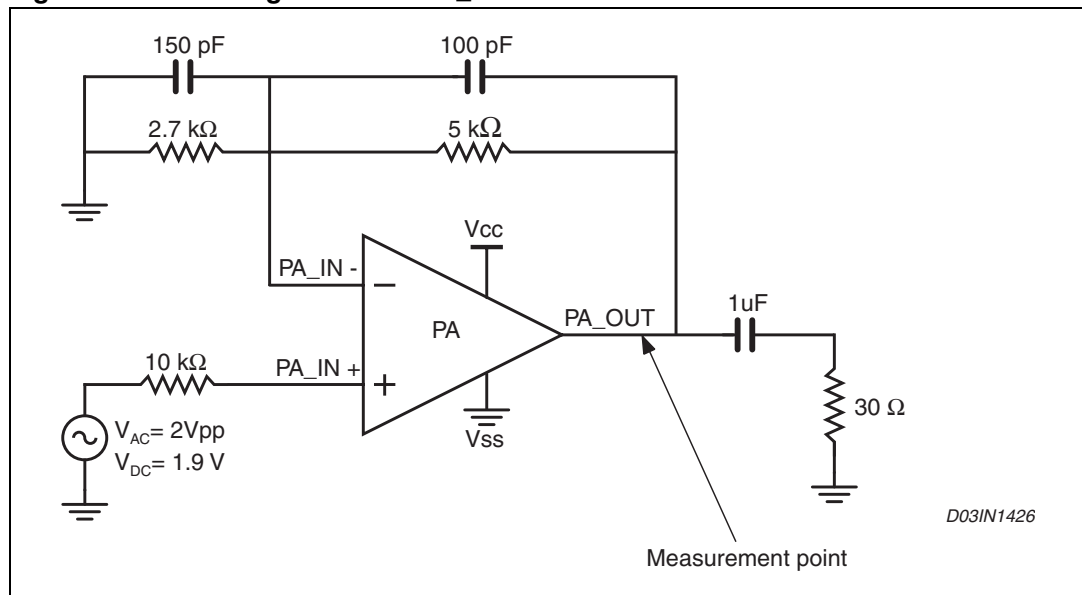
**Table 5. Electrical characteristics** (continued)

( $V_{DD} = +5V$ ,  $V_{CC} = +9V$ ,  $V_{SS} = SV_{SS} = GND = 0V$ ,  $-40^{\circ}C \leq T_A \leq 85^{\circ}C$ ,  $T_J < 125^{\circ}C$ , unless otherwise specified)

| Symbol                  | Parameter                   | Test condition  | Min.    | Typ.                      | Max.      | Unit    |
|-------------------------|-----------------------------|---|---------|---------------------------|-----------|---------|
| <b>Serial Interface</b> |                             |   |         |                           |           |         |
| $T_B$                   | Baud rate Bit Time (1/BAUD) | Control register bit 3 and bit 4 (See <a href="#">Figure 13</a> ) |         | 1667<br>833<br>417<br>208 |           | $\mu s$ |
| $T_s$                   | Setup time                  | see Figures 8, 9, 10, 11 & 12                                     |         |                           | 5         | ns      |
| $T_H$                   | Hold time                   | see Figures 8, 9, 10, 11 & 12                                     |         |                           | 2         | ns      |
| $T_{CR}$                | CLR/T vs. REG_DATA or RxTx  | see Figures 8, 9, 10, 11 & 12                                     |         |                           | $T_B/4$   |         |
| $T_{CC}$                | CLR/T vs. CLR/T             | see Figures 8, 9, 10, 11 & 12                                     | $T_B$   |                           | $2 * T_B$ |         |
| $T_{DS}$                | Setup time                  | see Figures 8, 9, 10, 11 & 12                                     | $T_B/4$ |                           | $T_B/2$   |         |
| $T_{DH}$                | Hold time                   | see Figures 8, 9, 10, 11 & 12                                     | $T_B/4$ |                           | $T_B/2$   |         |
| $T_{CRP}$               |                             |   | $T_H$   |                           | $T_B/2$   |         |

1. Not tested, guaranteed by design

**Figure 3. PLI configuration for PA\_OUT distortions measurement**



## 5 Crystal resonator and external clock

Figure 4. External clock waveform

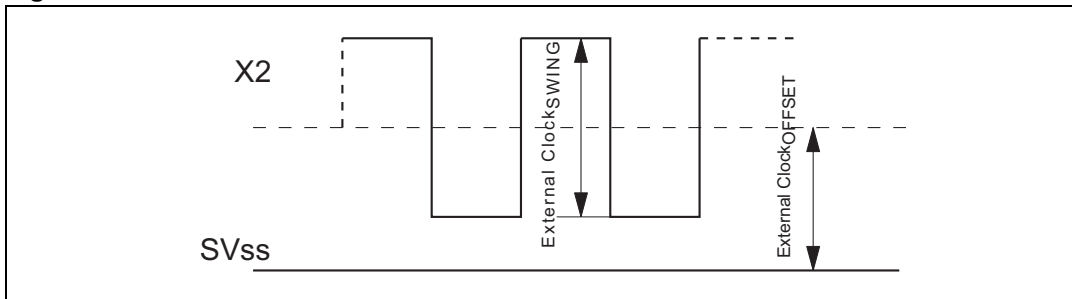
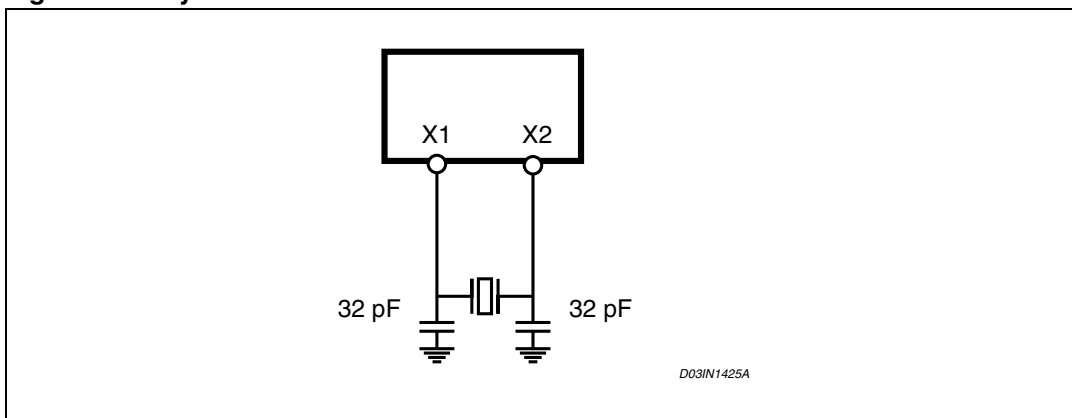


Figure 5. Crystal Resonator



## 6 Functional description

### 6.1 Carrier frequencies

ST7540 is a multi frequency device: eight programmable Carrier Frequencies are available (see [Table 6](#)).

Only one Carrier can be used a time. The communication channel could be varied during the normal working Mode to realize a multi frequency communication.

Selecting the desired frequency in the Control Register the Transmission and Reception filters are accordingly tuned.

**Table 6. Channels List**

| FCarrier          | F (KHz) |
|-------------------|---------|
| F0                | 60      |
| F1                | 66      |
| F2                | 72      |
| F3                | 76      |
| F4                | 82.05   |
| F5                | 86      |
| F6                | 110     |
| F7 <sup>(1)</sup> | 132.5   |

1. Default value

### 6.2 Baud rates

ST7540 is a multi Baud rate device: four Baud Rate are available (See [Table 8](#)).

**Table 7. ST7540 mark and space tones frequency distance Vs. baud rate and deviation**

| Baud Rate [Baud]    | $\Delta F$ <sup>(1)</sup> (Hz) | Deviation <sup>(2)</sup> |
|---------------------|--------------------------------|--------------------------|
| 600                 | 600                            | 1 <sup>(3)</sup>         |
| 1200                | 600<br>1200                    | 0.5<br>1                 |
| 2400 <sup>(4)</sup> | 1200 <sup>(4)</sup><br>2400    | 0.5<br>1                 |
| 4800                | 2400<br>4800                   | 0.5<br>1                 |

1. Frequency deviation

2. Deviation =  $\Delta F / (\text{Baud Rate})$

3. Deviation 0.5 not allowed

4. Default value



### 6.3 Mark and space frequencies

Mark and Space Communication Frequencies are defined by the following formula:

$$F ("0") = F_{\text{Carrier}} + [\Delta F]/2$$

$$F ("1") = F_{\text{Carrier}} - [\Delta F]/2$$

$\Delta F$  is the Frequency Deviation.

With Deviation = "0.5" the difference in terms of frequency between the mark and space tones is half the Baudrate value ( $\Delta F=0.5 \cdot \text{BAudrate}$ ). When the Deviation = "1" the difference is the Baudrate itself ( $\Delta F = \text{Baudrate}$ ). The minimal Frequency Deviation is 600Hz.

**Table 8. ST7540 synthesized frequencies**

| Carrier frequency (KHz) | Baud rate | Deviation | Exact frequency [Hz] (Clock=16MHz) |       | Carrier frequency (KHz) | Baud rate | Deviation | Exact frequency [Hz] (Clock=16MHz) |        |
|-------------------------|-----------|-----------|------------------------------------|-------|-------------------------|-----------|-----------|------------------------------------|--------|
|                         |           |           | "1"                                | "0"   |                         |           |           | "1"                                | "0"    |
| 60                      | 600       | --        |                                    |       | 82.05                   | 600       | --        |                                    |        |
|                         |           | 1         | 59733                              | 60221 |                         |           | 1         | 81706                              | 82357  |
|                         | 1200      | 0.5       | 59733                              | 60221 |                         | 1200      | 0.5       | 81706                              | 82357  |
|                         |           | 1         | 59408                              | 60547 |                         |           | 1         | 81380                              | 82682  |
|                         | 2400      | 0.5       | 59408                              | 60547 |                         | 2400      | 0.5       | 81380                              | 82682  |
|                         |           | 1         | 58757                              | 61198 |                         |           | 1         | 80892                              | 83171  |
|                         | 4800      | 0.5       | 58757                              | 61198 |                         | 4800      | 0.5       | 80892                              | 83171  |
|                         |           | 1         | 57617                              | 62337 |                         |           | 1         | 79590                              | 84473  |
| 66                      | 600       | --        |                                    |       | 86                      | 600       | --        |                                    |        |
|                         |           | 1         | 65755                              | 66243 |                         |           | 1         | 85775                              | 86263  |
|                         | 1200      | 0.5       | 65755                              | 66243 |                         | 1200      | 0.5       | 85775                              | 86263  |
|                         |           | 1         | 65430                              | 66569 |                         |           | 1         | 85449                              | 86589  |
|                         | 2400      | 0.5       | 65430                              | 66569 |                         | 2400      | 0.5       | 85449                              | 86589  |
|                         |           | 1         | 64779                              | 67220 |                         |           | 1         | 84798                              | 87240  |
|                         | 4800      | 0.5       | 64779                              | 67220 |                         | 4800      | 0.5       | 84798                              | 87240  |
|                         |           | 1         | 63639                              | 68359 |                         |           | 1         | 83659                              | 88379  |
| 72                      | 600       | --        |                                    |       | 110                     | 600       | --        |                                    |        |
|                         |           | 1         | 71777                              | 72266 |                         |           | 1         | 109701                             | 110352 |
|                         | 1200      | 0.5       | 71777                              | 72266 |                         | 1200      | 0.5       | 109701                             | 110352 |
|                         |           | 1         | 71452                              | 72591 |                         |           | 1         | 109375                             | 110677 |
|                         | 2400      | 0.5       | 71452                              | 72591 |                         | 2400      | 0.5       | 109375                             | 110677 |
|                         |           | 1         | 70801                              | 73242 |                         |           | 1         | 108724                             | 111165 |
|                         | 4800      | 0.5       | 70801                              | 73242 |                         | 4800      | 0.5       | 108724                             | 111165 |
|                         |           | 1         | 69661                              | 74382 |                         |           | 1         | 107585                             | 112467 |

**Table 8. ST7540 synthesized frequencies**

|    |      |     |       |       |       |      |     |        |        |
|----|------|-----|-------|-------|-------|------|-----|--------|--------|
| 76 | 600  | --  |       |       | 132.5 | 600  | --  |        |        |
|    |      | 1   | 75684 | 76335 |       |      | 1   | 132161 | 132813 |
|    | 1200 | 0.5 | 75684 | 76335 |       | 1200 | 0.5 | 132161 | 132813 |
|    |      | 1   | 75358 | 76660 |       |      | 1   | 131836 | 133138 |
|    | 2400 | 0.5 | 75358 | 76660 |       | 2400 | 0.5 | 131836 | 133138 |
|    |      | 1   | 74870 | 77148 |       |      | 1   | 131348 | 133626 |
|    | 4800 | 0.5 | 74870 | 77148 |       | 4800 | 0.5 | 131348 | 133626 |
|    |      | 1   | 73568 | 78451 |       |      | 1   | 130046 | 134928 |

## 6.4 ST7540 Mains access

ST7540 can access the Mains in two different ways:

- Synchronous access
- Asynchronous access

The choice between the two types of access can be performed by means of Control Register bit 14 (see [Table 12](#)) and affects the ST7540 data flow in Transmission Mode as in Reception Mode (for how to set the communication Mode, see [Section 6.5](#)).

### In data transmission mode:

- Synchronous Mains access: on clock signal provided by ST7540 (CLR/T line) rising edge, data transmission line (TxD line) value is read and sent to the FSK Modulator. ST7540 manages the Transmission timing according to the BaudRate Selected.
- Asynchronous Mains access: data transmission line (TxD line) value enters directly to the FSK Modulator. The Host Controller manages the Transmission timing (CLR/T line should be neglected).

### In data reception mode:

- Synchronous Mains access: on clock signal recovered by a PLL from ST7540 (CLR/T line) rising edge, value on FSK Demodulator is read and put to the data reception line (RxD line). ST7540 recovers the bit timing according to the BaudRate Selected.
- Asynchronous Mains access: Value on FSK Demodulator is sent directly to the data reception line (RxD line). The Host Controller recovers the communication timing (CLR/T line should be neglected).

## 6.5 Host processor interface

ST7540 exchanges data with the host processor through a serial interface.

The data transfer is managed by REG\_DATA and RxTx Lines, while data are exchanged using RxD, TxD and CLR/T lines.

Four are the ST7540 working modes:

- Data Reception
- Data Transmission
- Control Register Read
- Control Register Write

REG\_DATA and RxTx lines are level sensitive inputs.

**Table 9. Data and Control register access bits configuration**

|                        | REG_DATA | RxTx |
|------------------------|----------|------|
| Data Transmission      | 0        | 0    |
| Data Reception         | 0        | 1    |
| Control Register Read  | 1        | 1    |
| Control Register Write | 1        | 0    |

ST7540 features two type of Host Communication Interfaces:

- SPI
- UART

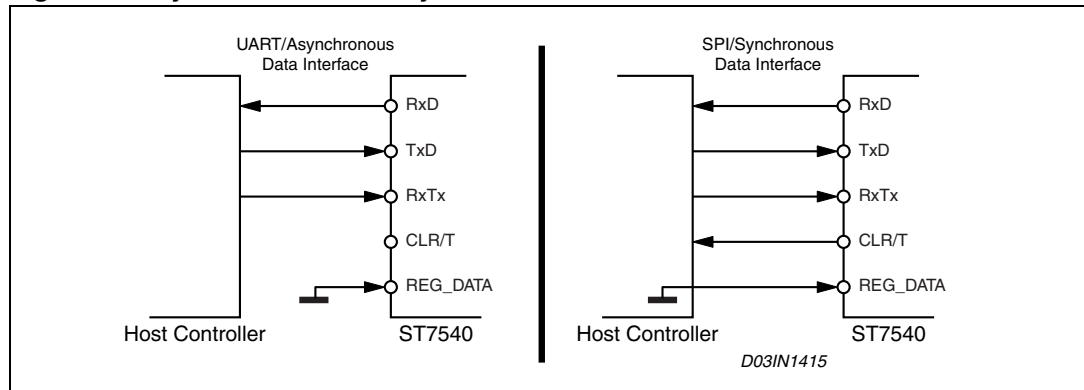
The selection can be done through the UART/SPI pin. If UART/SPI pin is forced to “0” SPI interface is selected while if UART/SPI pin is forced to “1” UART interface is selected. The type of interface affects the Data Reception by setting the idle state of RxD line. When ST7540 is in Receiving mode (REG\_DATA=“0” and RxTx =“1”) and no data are available on mains (or RxD is forced to an idle state, i.e. with a conditioned Detection Method), the RxD line is forced to “0” when UART/SPI pin is forced to “0” or it is forced to “1” when UART/SPI pin is forced to “1”.

The UART interface allows to connect an UART compatible device while SPI interface allows to connect an SPI compatible device. The allowed combinations of Host Interface/ST7540 Mains Access are:

**Table 10. Host interface / ST7540 mains access combinations**

| Host device interface type | UART/SPI pin | Communication mode | Mains access |             |
|----------------------------|--------------|--------------------|--------------|-------------|
|                            |              |                    | Asynchronous | Synchronous |
| UART                       | “1”          | Transmission       | X            |             |
| UART                       | “1”          | Reception          | X            |             |
| SPI                        | “0”          | Transmission       |              | X           |
| SPI                        | “0”          | Reception          |              | X           |

**Figure 6. Synchronous and Asynchronous ST7540/Host Controller interfaces**



ST7540 allows to interface the Host Controller using a five line interface (RxD, TxD, RxTx, CLR/T, & REG\_DATA) in case of Synchronous mains access or using a 3 line interface (RxD, TxD & RxTx) in Asynchronous mains access. Since Control Register is not accessible in Asynchronous mode, in this case REG\_DATA pin must be tied to GND.

### 6.5.1 Communication between Host and ST7540

The Host can achieve the Mains access by selecting REG\_DATA="0" and the choice between Data Transmission or Data Reception is performed by selecting RxTx line (if RxTx="1" ST7540 receives data from mains, if RxTx="0" ST7540 transmits data over the mains).

Communication between Host and ST7540 is different in Asynchronous and Synchronous mode:

- **Asynchronous mode:**

In Asynchronous Mode, data are exchanged without any data Clock reference. The host controller has to recover the clock reference in receiving Mode and control the Bit time in transmission mode.

If RxTx line is set to "1" & REG\_DATA="0" (Data Reception), ST7540 enters in an Idle State. After Tcc time the modem starts providing received data on RxD line.

If RxTx line is set to "0" & REG\_DATA="0" (Data Transmission), ST7540 enters in an Idle State and transmission circuitry is switched on. After Tcc time the modem starts transmitting data present on TxD line.

- **Synchronous mode:**

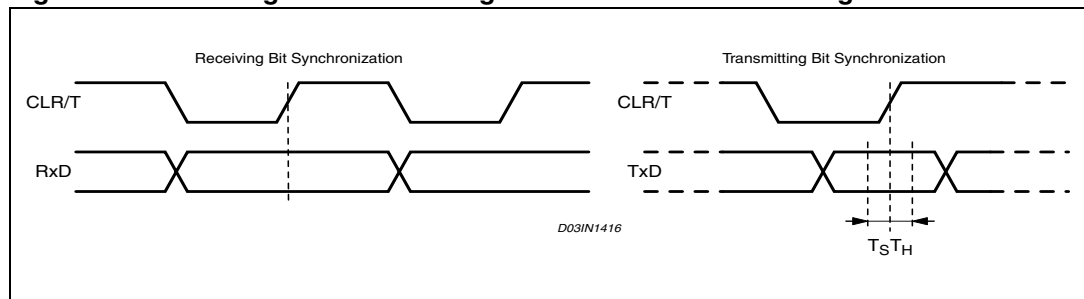
In Synchronous Mode ST7540 is always the master of the communication and provides the clock reference on CLR/T line. When ST7540 is in receiving mode an internal PLL recovers the clock reference. Data on RxD line are stable on CLR/T rising Edge.

When ST7540 is in transmitting mode the clock reference is internally generated and TxD line is sampled on CLR/T rising Edge.

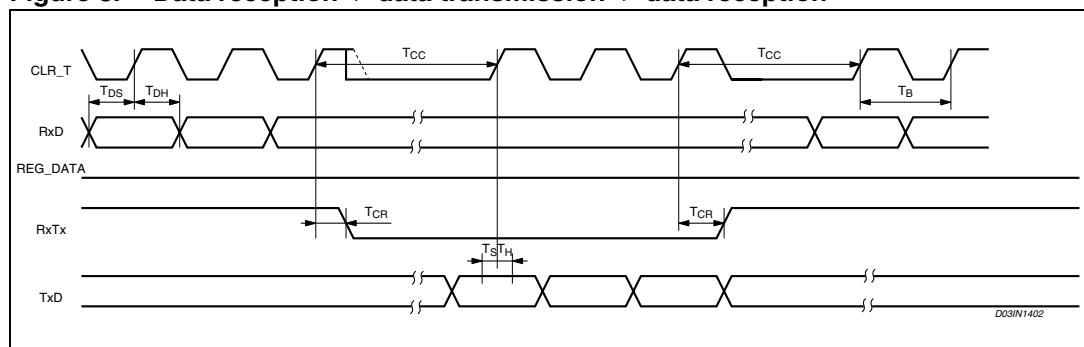
If RxTx line is set to "1" & REG\_DATA="0" (Data Reception), ST7540 enters in an Idle State and CLR/T line is forced Low. After T<sub>cc</sub> time the modem starts providing received data on RxD line.

If RxTx line is set to "0" & REG\_DATA="0" (Data Transmission), ST7540 enters in an Idle State and transmission circuitry is switched on. After T<sub>cc</sub> time the modem starts transmitting data present on TxD line (Figure 8).

**Figure 7. Receiving and transmitting data/recovered clock timing**



**Figure 8. Data reception -> data transmission -> data reception**



### 6.5.2 Control register access

The communication with ST7540 Control Register is always synchronous. The access is achieved using the same lines of the Mains interface (RxD, TxD, RxTx and CLR/T) plus REG\_DATA Line.

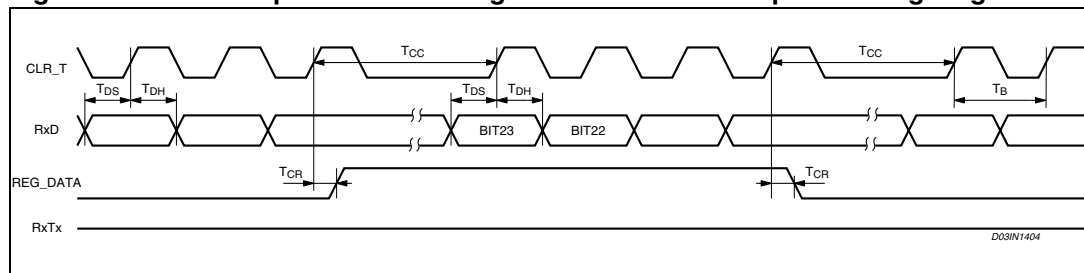
With REG\_DATA = 1 and RxTx = 0, the data present on TxD are loaded into the Control Register MSB first. The ST7540 samples the TxD line on CLR/T rising edges. The control Register content is updated at the end of the register access section (REG\_DATA falling edge).

In Normal Control Register mode (Control Register bit 21 = "0", see [Table 12](#)) if more than 24 bits are transferred to ST7540 only latest 24 bits are stored inside the Control Register. If less than 24 bits are transferred to ST7540 the Control Register writing is aborted.

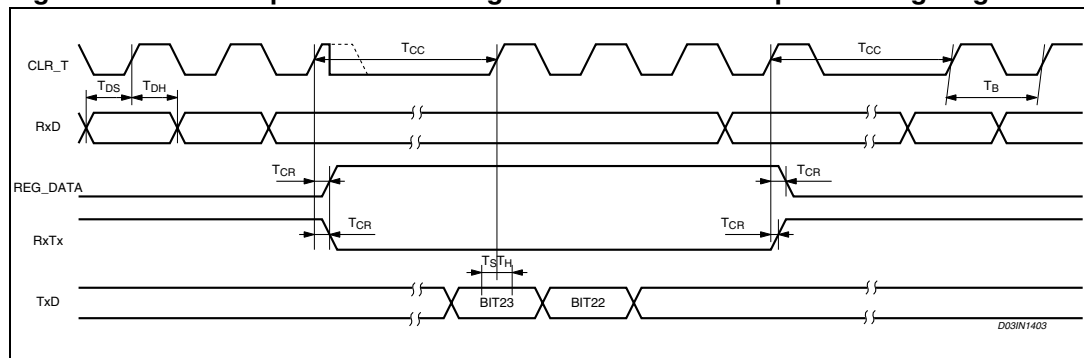
In order to avoid undesired Control Register writings caused by REG\_DATA line fluctuations (for example because of surge or burst on mains), in Extended Control Register mode (Control Register bit 21 = "1" see [Table 12](#)) exactly 24 or 48 bits must be transferred to ST7540 in order to properly write the Control Register, otherwise writing is aborted. If 24 bits are transferred, only the first 24 Control Register bits (from 23 to 0) are written.

With REG\_DATA = 1 and RxTx = 1, the content of the Control Register is sent on RxD port. The Data on RxD are stable on CLR/T rising edges MSB First. In Normal Control Register mode 24 bits are transferred from ST7540 to the Host. In Extended Control Register mode 24 or 48 bits are transferred from ST7540 to the Host depending on content of Control Register bit 18 (with bit 18 = "0" the first 24 bits are transferred, otherwise all 48 bits are transferred, see [Table 12](#)).

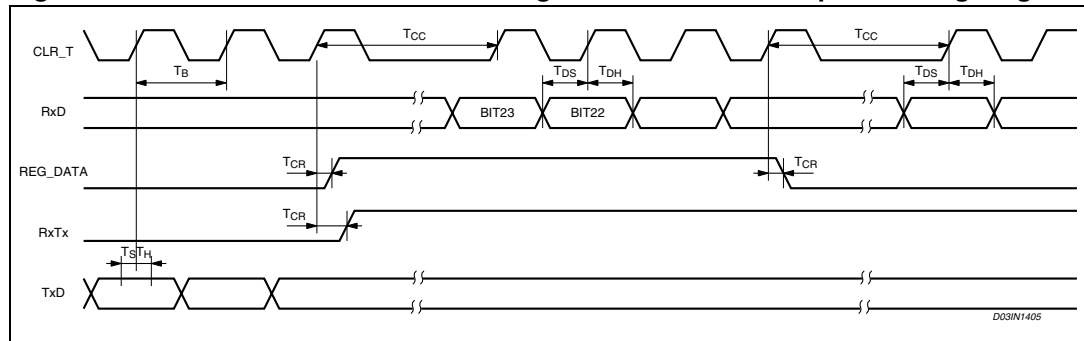
**Figure 9. Data reception → control register read → data reception timing diagram**



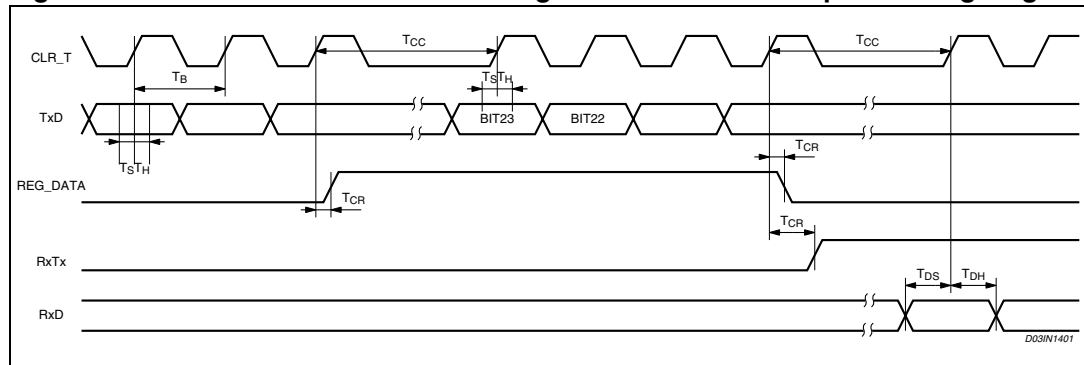
**Figure 10. data reception → control register write → data reception timing diagram**



**Figure 11. Data transmission → control register read → data reception timing diagram**



**Figure 12. Data transmission → control register write → data reception timing diagram**



## 6.6 Receiving mode

The receive section is active when RxD pin = "1" and REG\_DATA=0.

The input signal is read on RX\_IN Pin using SV<sub>SS</sub> as ground reference and then pre-filtered by a Band pass Filter (62kHz max bandwidth at -3dB). The Pre-Filter can be inserted setting one bit in the Control Register. The Input Stage features a wide dynamic range to receive Signal with a Very Low Signal to Noise Ratio. The Amplitude of the applied waveform is automatically adapted by an Automatic Gain Control block (AGC) and then filtered by a Narrow Band Band-Pass Filter centered around the Selected Channel Frequency (14kHz max at -3dB). The resulting signal is down-converted by a mixer using a sinewave generated by the FSK Modulator. Finally an Intermediate Frequency Band Pass-Filter (IF Filter) improves the Signal to Noise ration before sending the signal to the FSK demodulator. The FSK demodulator then send the signal to the RX Logic for final digital filtering. Digital filtering Removes Noise spikes far from the BAUD rate frequency and Reduces the Signal Jitter. RxD Line is forced to "0" or "1" (according the UART/SPI pin level) when neither mark or space frequencies are detected on RX\_IN Pin.

Mark and Space Frequency in Receiving Mode must be distant at least BaudRate/2 to have a correct demodulation.

While ST7540 is in Receiving Mode (RxD pin = "1"), the transmit circuitry, Power Line Interface included, is turned off. This allows the device to achieve a very low current consumption (5mA typ).

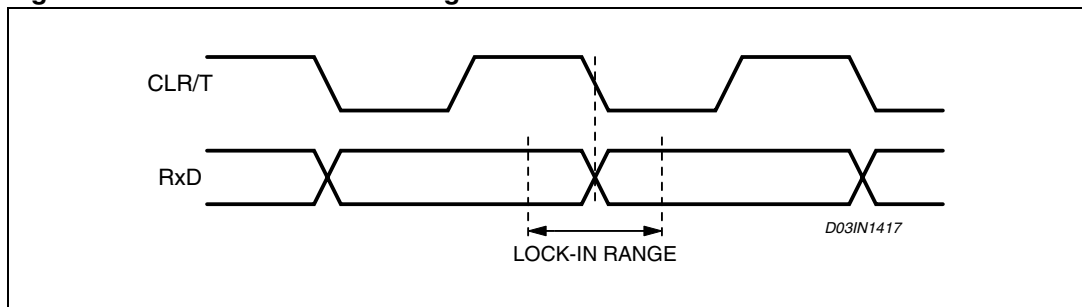
- **Receiving Sensitivity Level Selection**

It is possible to select the ST7540 Receiving Sensitivity Level by Control Register (see [Table 12](#)) or setting to '1' the TxD pin during reception phase (this condition overcomes the control register setting the sensitivity equal to BU threshold). Increasing the device sensitivity allows to improve the communication reliability when the ST7540 sensitivity is the limiting factor.

- **Synchronization Recovery System (PLL)**

ST7540 embeds a Clock Recovery System to feature a Synchronous data exchange with the Host Controller. The clock recovery system is realized by means of a second order PLL. In Synchronous mode, data on the data line (RxD) are stable on CLR/T line rising edge (CLR/T Falling edge synchronized to RxD line transitions  $\pm$  LOCK-IN Range). The PLL Lock-in and Lock-out Range is  $\pm\pi/2$ . When the PLL is in the unlock condition RxD line is forced to "0" or "1" according to the UART/SPI pin level and CLR/T is forced to "0" only if the Detection Method "Preamble Detection With Conditioning" is selected. When PLL is in unlock condition it is sensitive to RxD Rising and Falling Edges. The maximum number of transition required to reach the lock-in condition is 5. When in lock-in condition the PLL is sensitive only to RxD rising Edges to reduce the CLR/T Jitter. ST7540 PLL is forced in the un-lock condition, when more than 32 equal symbols are received. Due to the fact that the PLL, in lock-in condition, is sensitive only to RxD rising edge, sequences equal or longer than 15 equal symbols can put the PLL into the un-lock condition.

**Figure 13. ST7540 PLL lock-in range**



- **Carrier/Preamble Detection**

The Carrier/Preamble Block is a digital Frequency detector Circuit. It can be used to manage the MAINS access and to detect an incoming signal. Two are the possible setting:

- Carrier Detection
- Preamble Detection



- **Carrier Detection**

The Carrier/Preamble detection Block notifies to the host controller the presence of a Carrier when it detects on the RX\_IN Input a signal with an harmonic component close to the programmed Carrier Frequency. The CD\_PD signal sensitivity is identical to the data reception sensitivity (0.5mVrms Typ. in Normal Sensitivity Mode). When the device sensitivity is set by the TxD line (Sensitivity level equal to BU threshold) the CD\_PD signal is conditioned to the BU signal.

The CD\_PD line is forced to a logic level low when a Carrier is detected.

- **Preamble Detection**

The Carrier/Preamble detection Block notifies to the host controller the presence of a Carrier modulated at the Programmed Baud Rate for at least 4 Consecutive Symbols (“1010” or “0101” are the symbols sequences detected).

CD\_PD line is forced low till a Carrier signal is detected and PLL is in the lock-in range.

To reinforce the effectiveness of the information given by CD\_PD Block, a digital filtering is applied on Carrier or Preamble notification signal (see [Section 6.8: Control register](#)). The Detection Time Bits in the Control Register define the filter performance. Increasing the Detection Time reduced the false notifications caused by noise on main line. The Digital filter adds a delay to CD\_PD notification equal to the programmed Detection Time. When the carrier frequency disappears, CD\_PD line is held low for a period equal to the detection time and then forced high. During this time, some spurious data caused by noise can be demodulated and sent over RxD line.

- **Header Recognition**

In Control Register Extended Mode (Control Register bit 21="1", see [Table 12](#)) the CD\_PD line can be used to recognize if an header has been sent during the transmission. With Header Recognition function enable (Control Register bit 18="1", see [Table 12](#)), CD\_PD line is forced low when a Frame Header is detected. If Frame Length Count function is enabled, CD\_PD is held low and a number of 16 bit word equal to the Frame Length selected is sent to the host controller. In this case, CLR/T is forced to "0" and RxD is forced to "0" or "1" (according the UART/SPI pin level) when Header has not been detected or after the Frame Length has been reached.

If Frame Length Count function is disabled, an header recognition is signaled by forcing CD\_PD low for one period of CLR/T line. In this case, CLR/T and RxD signal are always present, even if no header has been recognized.

Figure 14. CD\_PD Timing during RX

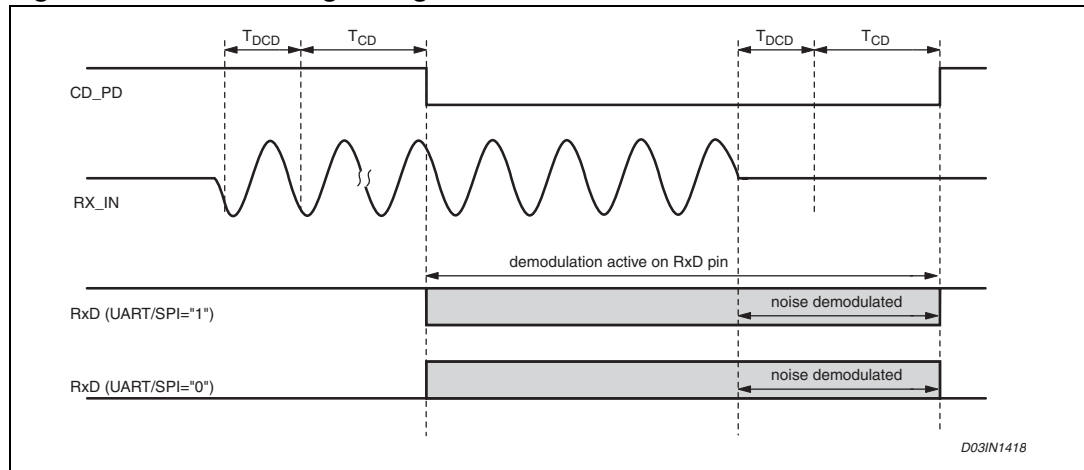
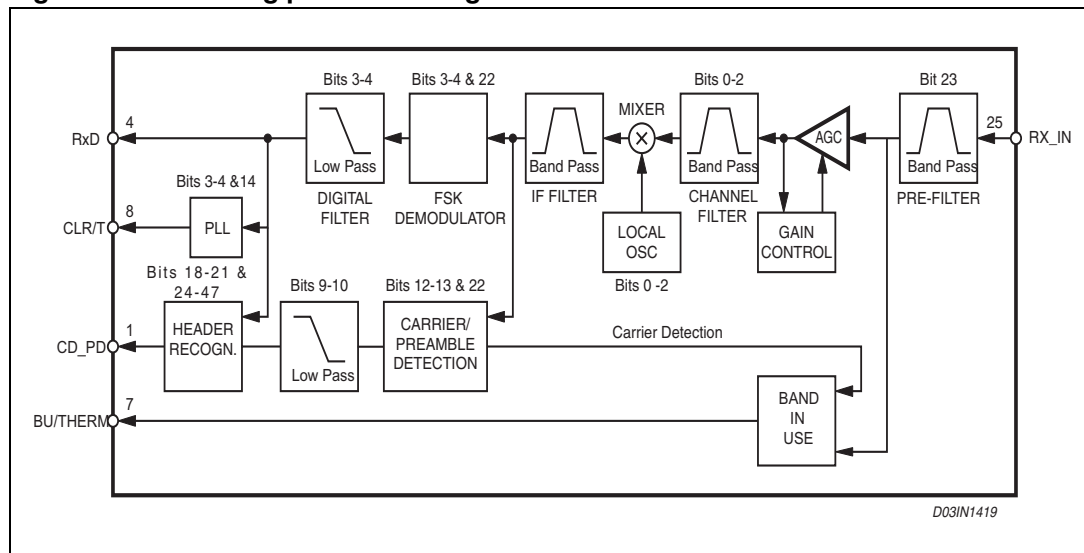


Figure 15. Receiving path block diagram



## 6.7 Transmission mode

The transmission mode is set when RxD Pin = "0" and REG\_DATA Pin = "0". In transmitting mode the FSK Modulator and the Power Line Interface are turned ON. The transmit Data (TxD) enter synchronously or asynchronously to the FSK modulator.

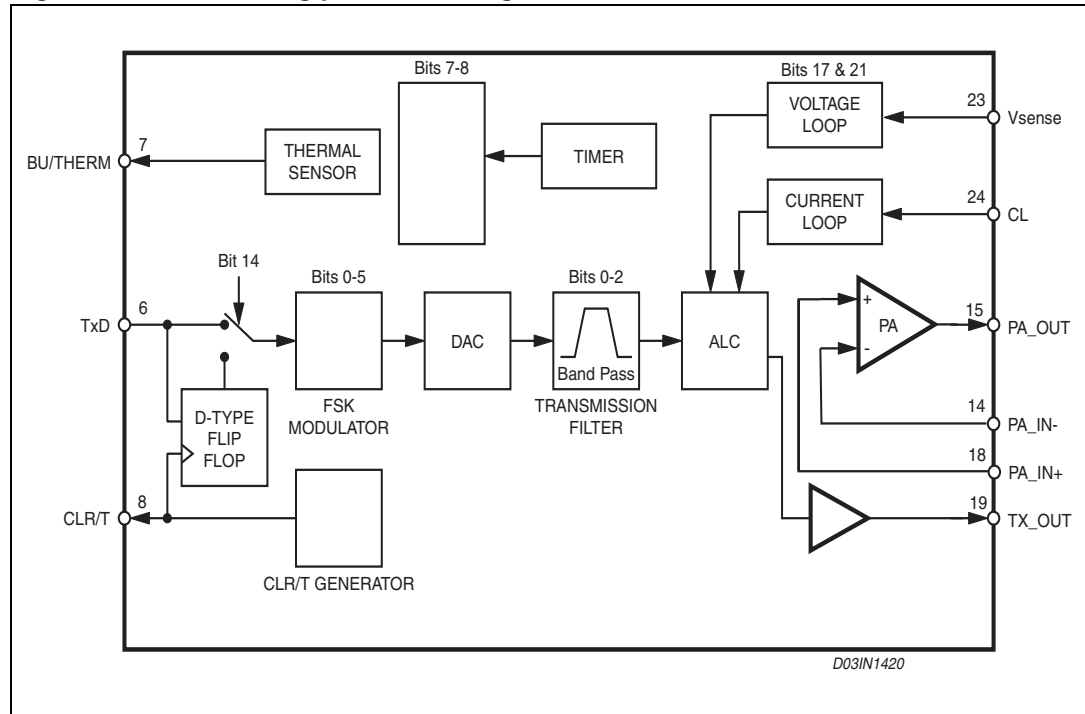
- Synchronous Mains access: on CLR/T rising edge, TxD Line Value is read and sent to the FSK Modulator. ST7540 manages the Transmission timing according to the BaudRate Selected
- Asynchronous Mains access: TxD data enter directly to the FSK Modulator. The Host Controller manages the Transmission timing

In both conditions no Protocol Bits are added by ST7540.

The FSK frequencies are synthesized in the FSK modulator from a 16 MHz crystal oscillator by direct digital synthesis technique. The frequencies Table in different Configuration is reported in [Table 8](#). The frequencies precision is same as external crystal one's.

In the analog domain, the signal is filtered in order to reduce the output signal spectrum and to reduce the harmonic distortion. The transition between a symbol and the following is done at the end of the on-going half FSK sinewave cycle.

**Figure 16. Transmitting path block diagram**



- **Automatic Level Control (ALC)**

The Automatic Level Control Block (ALC) is a variable gain amplifier (with 32 non linear discrete steps) controlled by two analog feed backs acting at the same time. The ALC gain range is 0dB to 30 dB and the gain change is clocked at 5KHz. Each step increases or reduces the voltage of 1dB (Typ).

Two are the control loops acting to define the ALC gain:

- A Voltage Control loop
- A Current Control Loop

The Voltage control loop acts to keep the Peak-to-Peak Voltage constant on Vsense. The gain adjustment is related to the result of a peak detection between the Voltage waveform on Vsense and two internal Voltage references. It is possible to protect the Voltage Control Loop against noise by freezing the output level (see [Section 7.5: Output voltage level freeze](#)).

- If  $V_{sense} < V_{sense_{TH}} - V_{sense_{HYST}}$  The next gain level is increased by 1 step
- If  $V_{sense_{TH}} - V_{sense_{HYST}} < V_{sense} < V_{sense_{TH}} + V_{sense_{HYST}}$  No Gain Change
- If  $V_{sense} > V_{sense_{TH}} + V_{sense_{HYST}}$  The next gain level is decreased by 1 step

The Current control loop acts to limit the maximum Peak Output current inside PA\_OUT.

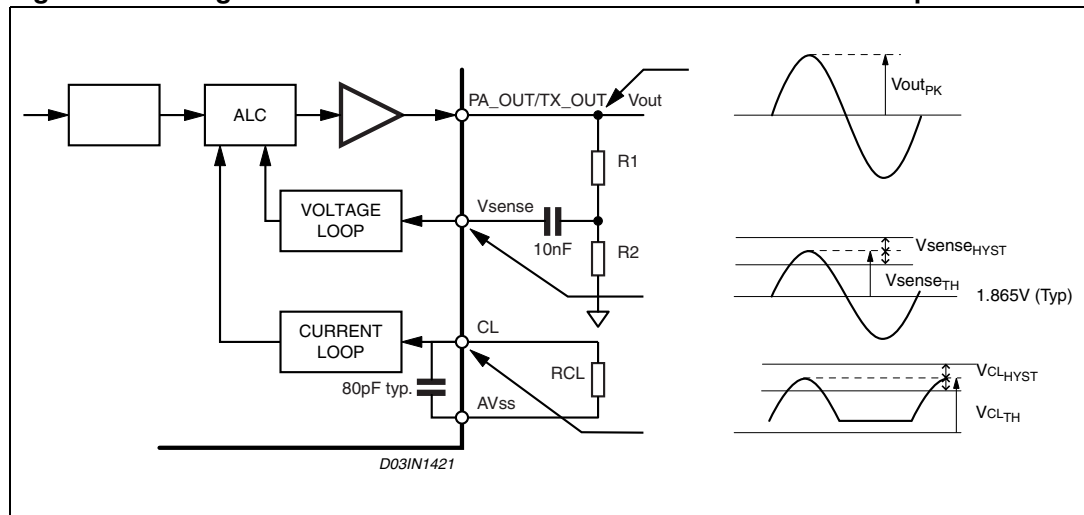
The current control loop acts through the voltage control loop decreasing the Output Peak-to-Peak Amplitude to reduce the Current inside the Power Line Interface.

The current sensing is done by mirroring the current in the High side MOS of the Power Amplifier (not dissipating current Sensing). The Output Current Limit (up to 500mrms), is set by means of an external resistor (R<sub>CL</sub>) connected between CL and V<sub>SS</sub>. The resistor converts the current sensed into a voltage signal. The Peak current sensing block works as the Output Voltage sensing Block:

- If V(CL) < CL<sub>TH</sub> - CL<sub>HYST</sub> Voltage Control Loop Acting
- If CL<sub>TH</sub> - CL<sub>HYST</sub> < V(CL) < CL<sub>TH</sub> + CL<sub>HYST</sub> No Gain Change
- If V(CL) > CL<sub>TH</sub> + CL<sub>HYST</sub> The next gain level is decreased by 1 step

Figure 17 shows the typical connection of Current and Voltage control loops.

**Figure 17. Voltage and current feedback external interconnection example**



Voltage Control Loop Formula

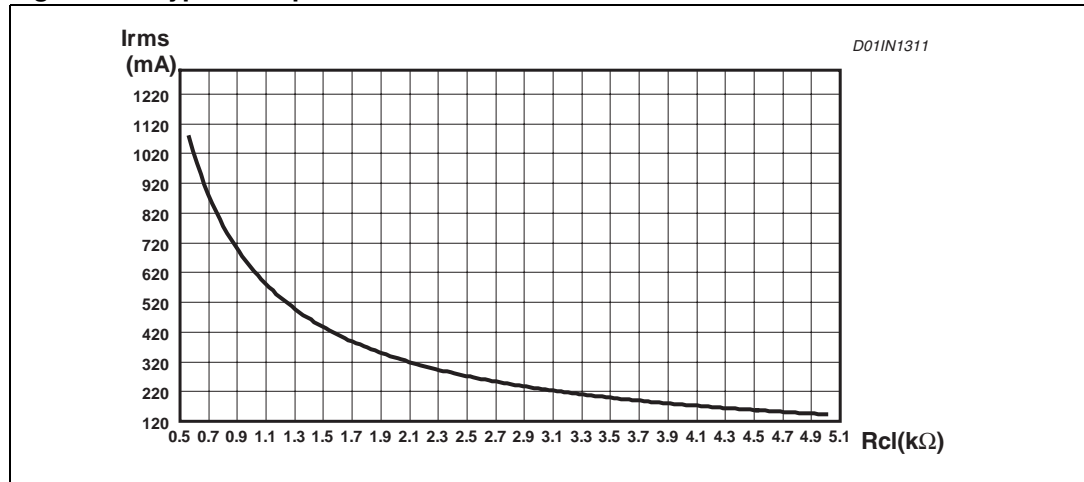
$$V_{OUTPK} \cong \frac{R_1 + R_2}{R_2} \cdot (V_{sense_{TH}} \pm V_{sense_{HYST}})$$

**Table 11. V<sub>OUT</sub> Vs. R1 & R2 resistors value**

| Vout (Vrms) | Vout (dBμV) | (R1+R2)/R2 | R2 (KΩ) | R1 (KΩ) |
|-------------|-------------|------------|---------|---------|
| 0.150       | 103.5       | 1.1        | 7.5     | 1.0     |
| 0.250       | 108.0       | 1.9        | 5.1     | 3.9     |
| 0.350       | 110.9       | 2.7        | 3.6     | 5.6     |
| 0.500       | 114.0       | 3.7        | 3.3     | 8.2     |
| 0.625       | 115.9       | 4.7        | 3.3     | 11.0    |
| 0.750       | 117.5       | 5.8        | 2.7     | 12.0    |
| 0.875       | 118.8       | 6.6        | 2.0     | 11.0    |
| 1.000       | 120.0       | 7.6        | 1.6     | 10.0    |
| 1.250       | 121.9       | 9.5        | 1.6     | 13.0    |
| 1.500       | 123.5       | 10.8       | 1.6     | 15.0    |

*Note:* Notes: The rate of R2 takes in account the input resistance on the V<sub>SENSE</sub> pin (36KΩ). 10nF capacitor effect has been neglected.

**Figure 18. Typical output current vs RCL**



● **Integrated Power Line Interface (PLI)**

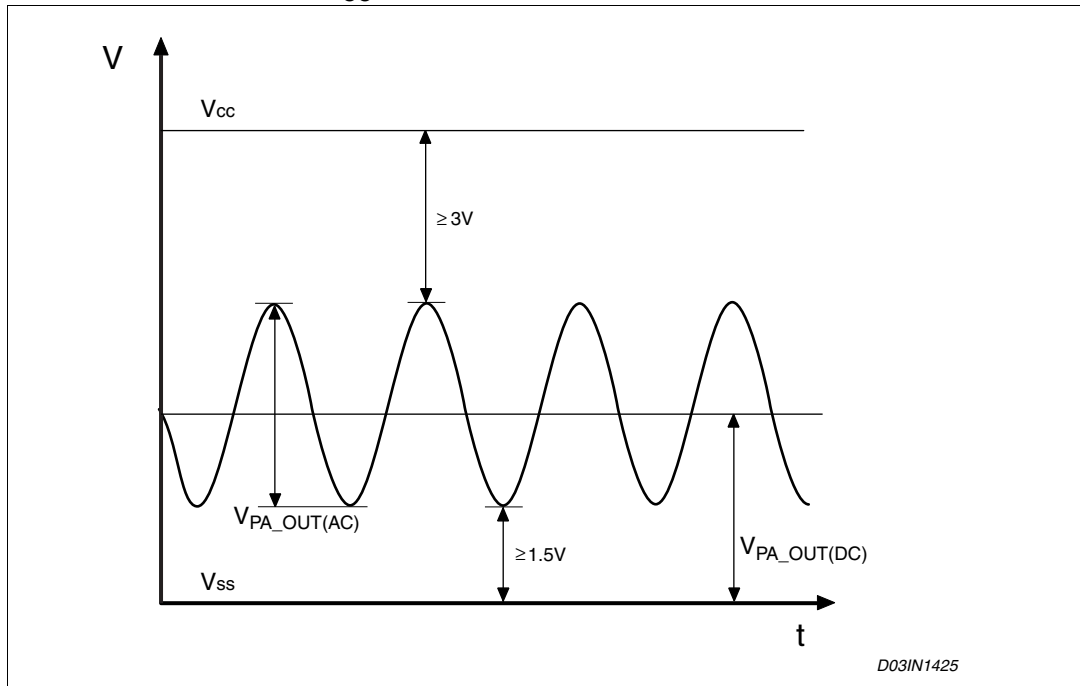
The Power Amplifier (PA) is a CMOS AB Class Power Amplifier. The PA requires, to ensure a proper

operation, a regulated and well filtered Supply Voltage. V<sub>CC</sub> Voltage and PA\_OUT Voltage must fulfil

the following formulas to work without clipping phenomena:

$$V_{CC} \geq \frac{V_{PAOUT(AC)}}{2} + V_{POUT(DC)} + 3V$$

$$V_{POUT(DC)} - \frac{V_{PAOUT(AC)}}{2} \geq 1.5V$$

Figure 19. PA\_OUT and  $V_{CC}$  relationship

Inputs and outputs of PA are available on pins PA\_IN-, PA\_IN+ and PA\_OUT. User can easily select an appropriate active filtering topology to filter the signal present on TX\_OUT pin. TX\_OUT output has a current capability much lower than PA\_OUT.

Figure 20. Power line interface topology

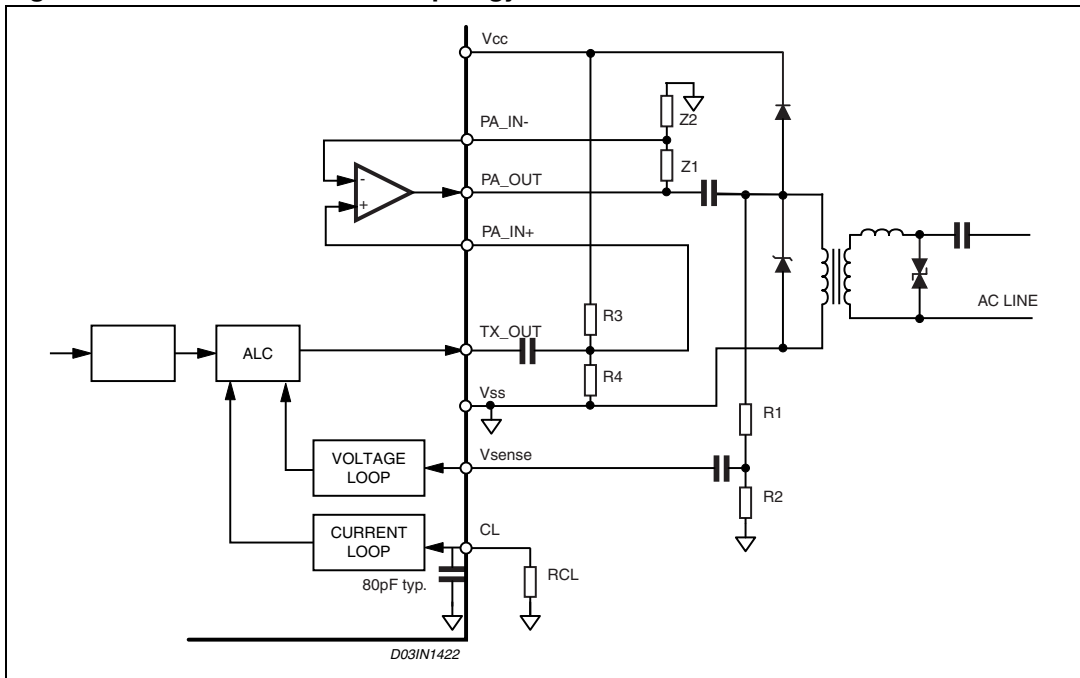
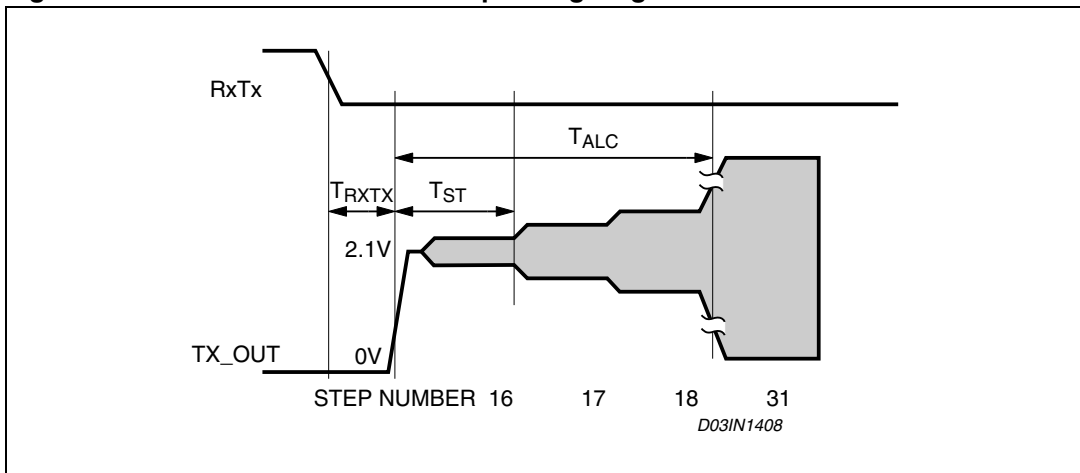


Figure 21. Power line interface startup timing diagram



## 6.8 Control register

The ST7540 is a multi-channel and multifunction transceiver. An internal 24 or 48 Bits (in Extended mode) Control Register allows to manage all the programmable parameters ([Table 12](#)).

The programmable functions are:

- Channel Frequency
- Baud Rate
- Deviation
- Watchdog
- Transmission Timeout
- Frequency Detection Time
- Detection Method
- Mains Interfacing Mode
- Output Clock
- Sensitivity Mode
- Input Pre-Filter

In addition to these functions the Extended mode provides 24 additional bits and others functions:

- Output Level Freeze
- Frame Header Recognizes (one 16 bits header or two 8 bits headers) with support to Frame Length Bit count



Table 12. Control register functions

|           | Function                 | Value           | Selection |       |       | Note                           | Default   |
|-----------|--------------------------|-----------------|-----------|-------|-------|--------------------------------|-----------|
| 0 to 2    | Frequencies              | 60 KHz          | 0         | 0     | 0     |                                | 132.5 kHz |
|           |                          | 66 KHz          | 0         | 0     | 1     |                                |           |
|           |                          | 72 KHz          | 0         | 1     | 0     |                                |           |
|           |                          | 76 KHz          | 0         | 1     | 1     |                                |           |
|           |                          | 82.05 KHz       | 1         | 0     | 0     |                                |           |
|           |                          | 86 KHz          | 1         | 0     | 1     |                                |           |
|           |                          | 110 KHz         | 1         | 1     | 0     |                                |           |
| 132.5 KHz | 1                        | 1               | 1         |       |       |                                |           |
| 3 to 4    | Baud rate                | 600             | Bit 4     |       | Bit 3 |                                | 2400      |
|           |                          | 1,200           | 0         | 0     |       |                                |           |
|           |                          | 2,400           | 0         | 1     |       |                                |           |
|           |                          | 4,800           | 1         | 0     |       |                                |           |
| 5         | Deviation                | 0.5             | Bit 5     |       |       | 0.5                            |           |
|           |                          | 1               | 0         | 1     |       |                                |           |
| 6         | Watchdog                 | Disabled        | Bit 6     |       |       | Enabled                        |           |
|           |                          | Enabled (1.5 s) | 0         | 1     |       |                                |           |
| 7 to 8    | Transmission time out    | Disabled        | Bit 8     | Bit 7 |       | 1 sec                          |           |
|           |                          | 1 s             | 0         | 0     |       |                                |           |
|           |                          | 3 s             | 0         | 1     |       |                                |           |
|           |                          | Not Used        | 1         | 0     |       |                                |           |
| 9 to 10   | Frequency detection time | 500 $\mu$ s     | 1         | 1     |       | 1 ms                           |           |
|           |                          | 1 ms            | 0         | 0     |       |                                |           |
|           |                          | 3 ms            | 0         | 1     |       |                                |           |
|           |                          | 5 ms            | 1         | 0     |       |                                |           |
| 11        | Reserved                 |                 |           |       |       | Do not force a different value | 0         |

Table 12. Control register functions

|          | Function                    | Value                                   | Selection |        | Note   | Default                                |
|----------|-----------------------------|---|-----------|--------|--|--|
|          |                             |   | Bit 13    | Bit 12 |  |  |
| 12 to 13 | Detection method            | Preamble detection without conditioning | 0         | 0      | Preamble detection notification on CD_PD Line CLR/T and RxD signal always present In UART Mode (UART/SPI pin set to 1) this configuration is not allowed.  | Carrier detection without conditioning |
|          |                             | Preamble detection with conditioning    | 0         | 1      | Preamble Detection notification on CD_PD Line. CLR/T and RxD line are forced to "0" when Preamble has not been detected or PLL is in Unlock condition. In UART Mode (UART/SPI pin set to 1) this configuration is not allowed. |  |
|          |                             | Carrier detection without conditioning  | 1         | 0      | Carrier detection notification on CD_PD Line CLR/T and RxD signal always present   |  |
|          |                             | Carrier detection with conditioning     | 1         | 1      | Carrier detection notification on CD_PD Line CLR/T Line is forced to "0" and RxD Line is forced to "0" or "1" (according the UART/SPI pin level) when carrier is not detected  |  |
| 14       | Mains Interfacing Mode      | Synchronous<br>Asynchronous             | Bit 14    |        |  | Asynchronous                           |
|          |                             |   | 0<br>1    |        |  |  |
| 15 to 16 | Output Clock                | 16 MHz<br>8 MHz<br>4 MHz<br>Clock OFF   | Bit 16    | Bit 15 |  | 4 MHz                                  |
|          |                             |   | 0         | 0      |  |  |
|          |                             |   | 0         | 1      |  |  |
|          |                             |   | 1         | 0      |  |  |
| 17       | Output Voltage Level Freeze | Enabled<br>Disabled                     | Bit 17    |        | Active only if extended control register is enable (Bit 21="1")  | Disabled                               |
|          |                             |   | 0<br>1    |        |  |  |
| 18       | Header Recognition          | Disabled<br>Enabled                     | Bit 18    |        | Active only if extended control register is enable (Bit 21="1")  | Disabled                               |
|          |                             |   | 0<br>1    |        |  |  |
| 19       | Frame Length Count          | Disabled<br>Enabled                     | Bit 19    |        | Active only if header recognition function (Bit 18="1") and extended control register (Bit 21="1") are enable  | Disabled                               |
|          |                             |   | 0<br>1    |        |  |  |

Table 12. Control register functions

|          | Function          | Value                                  | Selection | Note   | Default            |
|----------|-------------------|--|-----------|--|--------------------|
| 20       | Header Length     | 8 bits<br>16 bits                      | Bit 20    | Active only if Extended Control Register is enable (Bit 21="1")          | 16 bits            |
|          |                   |  | 0<br>1    |  |                    |
| 21       | Extended Register | Disable (24 bits)<br>Enabled (48 bits) | Bit 21    | Extended Register enables Functions on Bit 17, 18,19 and 20              | Disabled (24 bits) |
|          |                   |  | 0<br>1    |  |                    |
| 22       | Sensitivity Mode  | Normal Sensitivity<br>High Sensitivity | Bit 22    |  | Normal             |
|          |                   |  | 0<br>1    |  |                    |
| 23       | Input Filter      | Disabled<br>Enabled                    | Bit 23    |  | Disabled           |
|          |                   |  | 0<br>1    |  |                    |
| 24 to 39 | Frame Header      | from 0000h to FFFFh                    |           | One 16 bits Header or two 8 bits Headers (MSB first) depending on Bit 20 | 9B58h              |
| 40 to 47 | Frame Length      | from 01h to FFh                        |           | Number of 16 bits words expected   | 08h                |

## 7 Auxiliary analog and digital functions

### 7.1 Band in use

The Band in Use Block has a Carrier Detection like function but with a different Input Sensitivity (83.5 dB $\mu$ V Typ.) and with a different BandPass filter Selectivity (40dB/Dec).

BU/THERM line is forced High when a signal in band is detected.

To prevent BU/THERM line false transition, Band in Use signal is conditioned to Carrier Detection Internal Signal. This function is enabled only in Receiving mode (in Transmission mode the BU/THERM pin is used for Thermal shutdown signaling, see [Section 7.8: Thermal shutdown](#)).

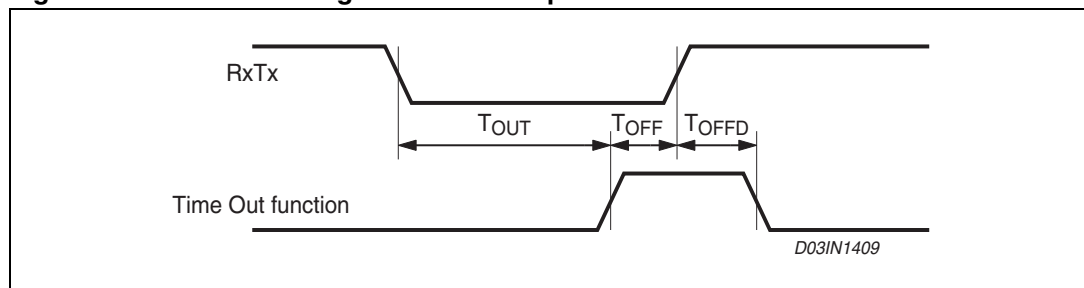
### 7.2 Time out

Time Out Function is a protection against a too long data transmission. When Time Out function is enabled after 1 or 3 second of continuous transmission the transceiver is forced in receiving mode. This function allows ST7540 to automatically manage the CENELEC Medium Access specification. When a time-out event occur, the transmission section is disabled for at least 125 ms. To Unlock the Time Out condition RxTx should be forced High. During the time out period only register access or reception mode are enabled.

During Reset sequence if RxTx line = "0" & REG\_DATA line = "0", Time Out protection is suddenly enabled and ST7540 must be configured in data reception after the reset event before starting a new data transmission.

Time Out time is programmable using Control Register bits 7 and 8 ([Table 12](#)).

**Figure 22. Time-out timing and unlock sequence**

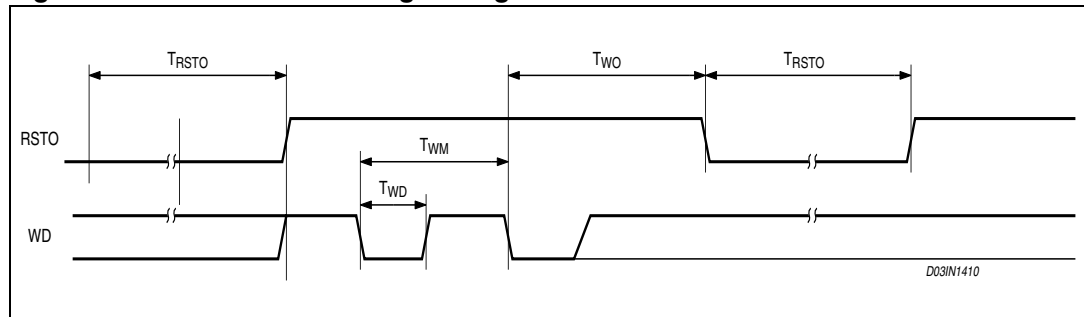


### 7.3 Reset & watchdog

RSTO Output is a reset generator for the application circuitry. During the ST7540 startup sequence is forced low. RSTO becomes high after a  $T_{RSTO}$  delay from the end of oscillator startup sequence.

Inside ST7540 is also embedded a watchdog function. The watchdog function is used to detect the occurrence of a software fault of the Host Controller. The watchdog circuitry generates an internal and external reset (RSTO low for  $T_{RSTO}$  time) on expiry of the internal watchdog timer. The watchdog timer reset can be achieved applying a negative pulse on WD pin (see [Figure 23](#)).

**Figure 23. Reset and Watchdog Timing**



### 7.4 Output clock

MCLK is the master clock output. The clock frequency sourced can be programmed through the Control Register to be a ratio of the crystal oscillator frequency ( $F_{osc}$ ,  $F_{osc}/2$ ,  $F_{osc}/4$ ). The transition between one frequency and another is done only at the end of the ongoing cycle. The oscillator can be disabled using Control Register bits 15 and 16 ([Table 12](#)).

### 7.5 Output voltage level freeze

The Output Level Freeze function, when enabled, turns off the Voltage Control Loop once the ALC stays in a stable condition for about 3 periods of control loop, and maintains a constant gain until the end of transmission. Output Level Freeze can be enabled using Control Register bit 17 ([Table 12](#)). This function is available only using the Extended Control Register (Control Register bit 21="1").

### 7.6 Extended control register

When Extended Control Register function is enabled, all the 48 bits of Control Register are programmable. Otherwise, only the first 24 bits of Control Register are programmable. The functions Header Recognition, Frame Bit Count and Output Voltage Freeze are available only if Extended Control Register function is enabled. Extended Control Register can be enabled using Control Register bit 21 ([Table 12](#)).

## 7.7 Under voltage lock out

The UVLO function turns off the device if the  $V_{CC}$  voltage falls under 4V. Hysteresis is 340mV typically.

## 7.8 Thermal shutdown

The ST7540 is provided of a thermal protection which turn off the PLI when the junction temperature exceeds  $170^{\circ}\text{C} \pm 10\%$  . Hysteresis is around  $30^{\circ}\text{C}$ .

When shutdown threshold is overcome, PLI interface is switched OFF.

Thermal Shutdown event is notified to the HOST controller using BU/THERM line. When BU/THERM line is High, ST7540 junction temperature exceed the shutdown threshold (Not Latched). This function is enabled only in Transmission mode (in Receiving mode the BU/THERM pin is used for Band in Use signaling, see Band in Use function [Section 7.1: Band in use](#)).

## 7.9 5V Voltage regulator

ST7540 has an embedded 5V linear regulator externally available (on pin VDC) to supply the application circuitry. The 5V linear regulator has a very low quiescent current ( $50\mu\text{A}$ ) and a current capability of 50mA. The regulator is protected against short circuitry events.

## 7.10 3.3V Voltage regulator

The  $V_{DD}$  pin can act either as 3.3V Voltage Output or as Input Digital Supply. When the  $V_{DD}$  pin is externally forced to 5V all the Digital I/Os operate at 5V, otherwise all the Digital I/Os are internally supplied at 3.3V. The  $V_{DD}$  pin can also source 3.3V voltage to supply external components. The 3.3V linear regulator has a very low quiescent current ( $50\mu\text{A}$ ) and a current capability of 50mA. The regulator is protected against short circuitry events.

## 7.11 Power-up procedure

To ensure ST7540 proper power-Up sequence,  $V_{CC}$  and  $V_{DD}$  Supply has to fulfil the following rules:

1.  $V_{CC}$  rising slope must not exceed 100V/ms.
2. When  $V_{DD}$  is below 5V/3.3V:  $V_{CC}-V_{DD} < 1.2\text{V}$ .

When  $V_{DD}$  supply is connected to VDC (5V Digital Supply) the above mentioned relation can be ignored if VDC load  $< 50\text{mA}$  and if the filtering capacitor on VDC  $< 100\mu\text{F}$ .

If  $V_{DD}$  is not forced to 5V, the Digital I/Os are internally supplied at 3.3 V and if  $V_{DD}$  load  $< 50\text{mA}$  and the filtering capacitor on  $V_{DD}$   $< 100\mu\text{F}$  the second relation can be ignored .

Figure 24. Power-up sequence

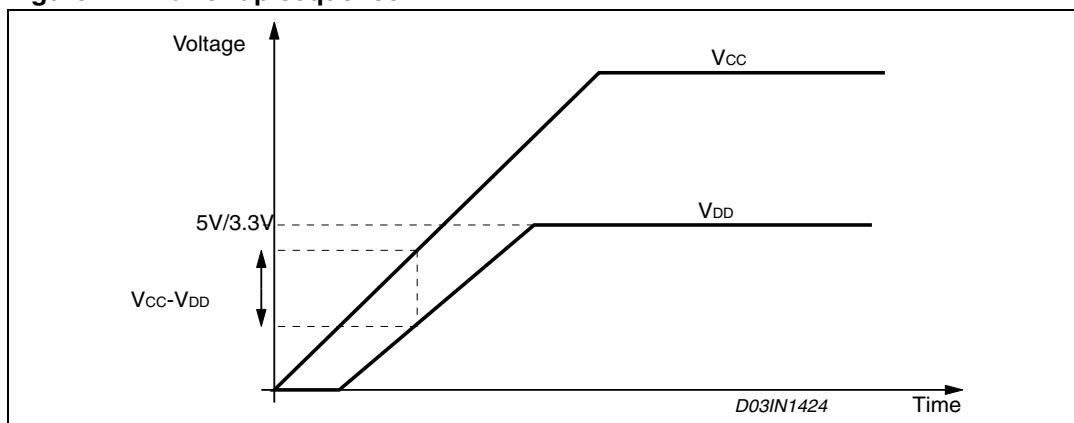
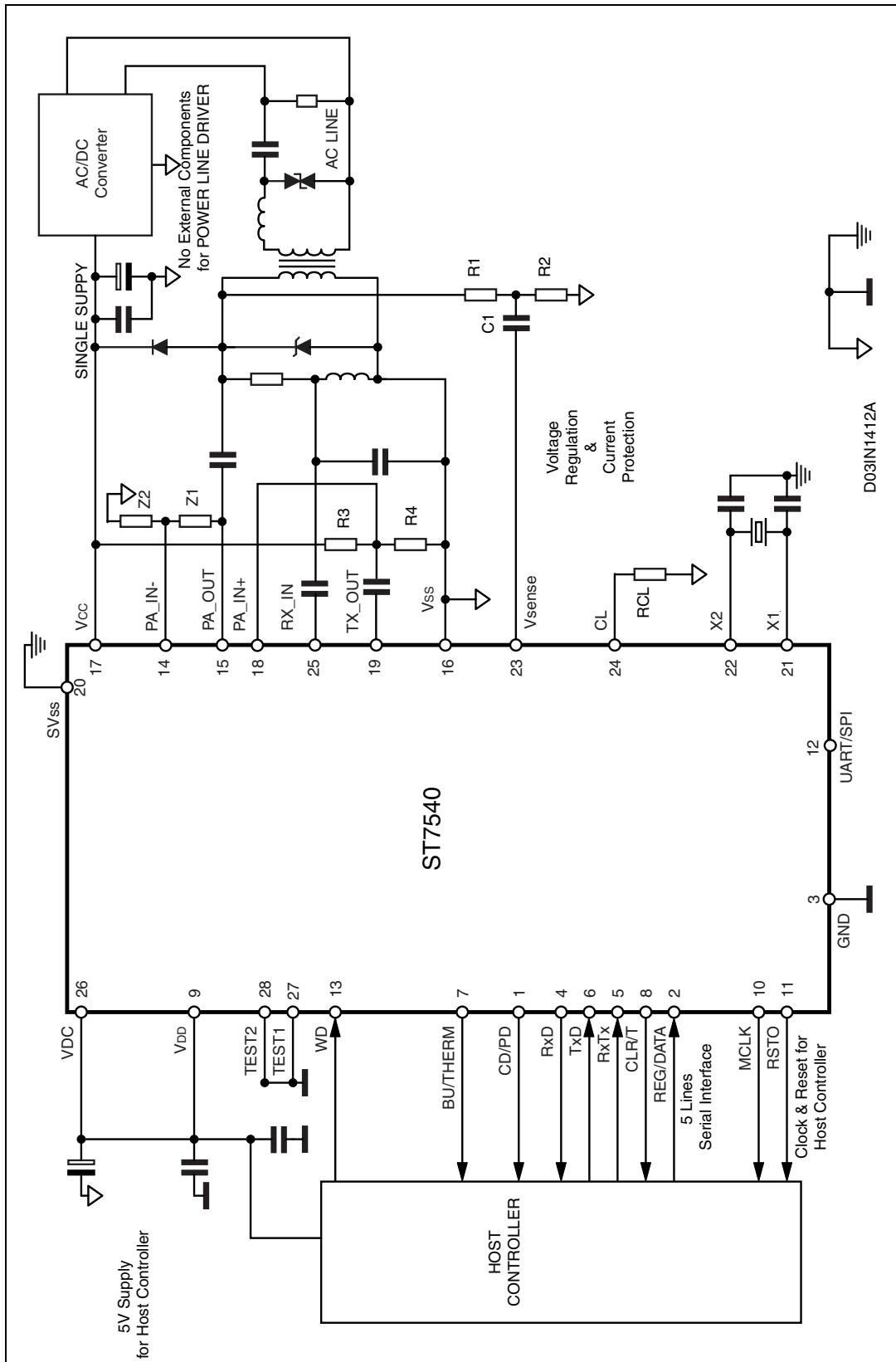


Figure 25. Application schematic example with coupling transformer.





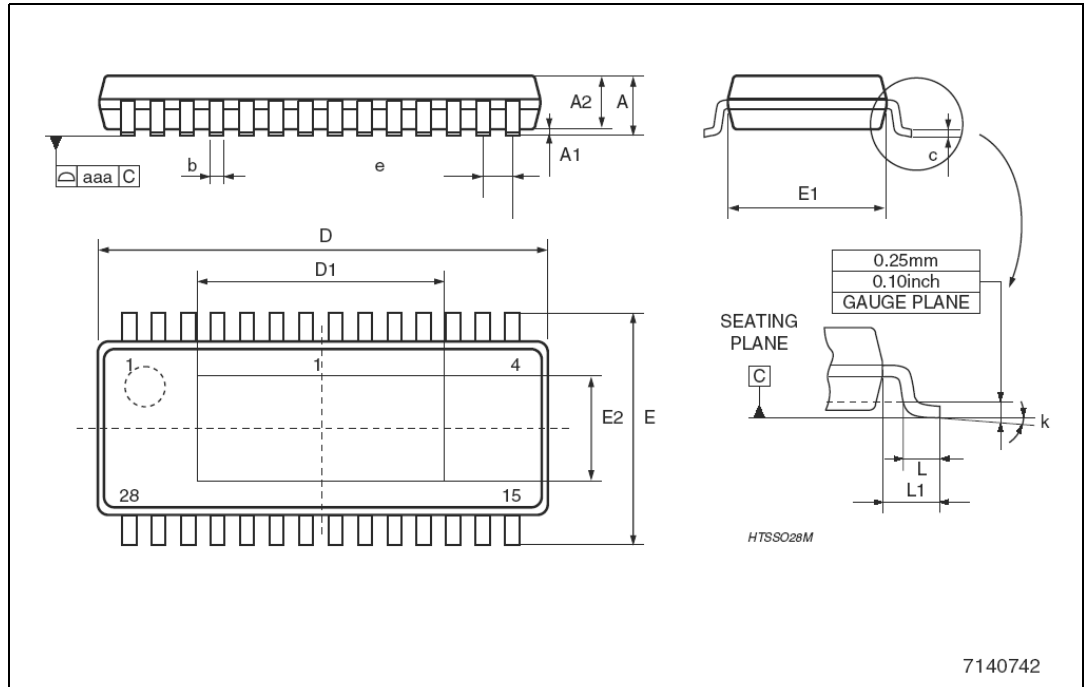
## 8 Mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

Table 13. HTSSOP28 Mechanical data

| Dim.   | mm.                |      |      | inch  |       |       |
|--------|--------------------|------|------|-------|-------|-------|
|        | Min.               | Typ. | Max. | Min.  | Typ.  | Max.  |
| A      |                    |      | 1.2  |       |       | 0.047 |
| A1     |                    |      | 0.15 |       |       | 0.006 |
| A2     | 0.8                | 1.0  | 1.05 | 0.031 | 0.039 | 0.041 |
| b      | 0.19               |      | 0.3  | 0.007 |       | 0.012 |
| c      | 0.09               |      | 0.2  | 0.003 |       | 0.008 |
| D (*)  | 9.6                | 9.7  | 9.8  | 0.377 | 0.382 | 0.385 |
| D1     | 3.3                |      |      | 0.130 |       |       |
| E      | 6.2                | 6.4  | 6.6  | 0.244 | 0.252 | 0.260 |
| E1 (*) | 4.3                | 4.4  | 4.5  | 0.169 | 0.173 | 0.177 |
| E2     | 1.5                |      |      |       |       |       |
| e      |                    | 0.65 |      |       | 0.026 |       |
| L      | 0.45               | 0.6  | 0.75 | 0.018 | 0.024 | 0.029 |
| L1     |                    | 1.0  |      |       | 0.039 |       |
| k      | 0° (min), 8° (max) |      |      |       |       |       |
| aaa    |                    | 0.1  |      |       | 0.004 |       |

Figure 26. Package dimensions



## 9 Revision history

Table 14. Revision history

| Date        | Revision | Changes  |
|-------------|----------|--|
| 15-Mar-2006 | 1        | Initial release.   |
| 25-Sep-2006 | 2        | Updated Electrical Characteristics and Power Amplifier description |

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