

Low Voltage / Low Power CMOS 16-bit Micro-controller

TMP91PW12F

1. OUTLINE AND DEVICE CHARACTERISTICS

TMP91PW12 is OTP type MCU which includes 128K byte One-time PROM. Using the adapter-socket, you can write and verify the data for TMP91PW12. TMP91PW12 has the same pin-assignment with TMP91CW12 (Mask ROM type).

Writing the program to Built-in PROM, TMP91PW12 operates as the same way with TMP91CW12.

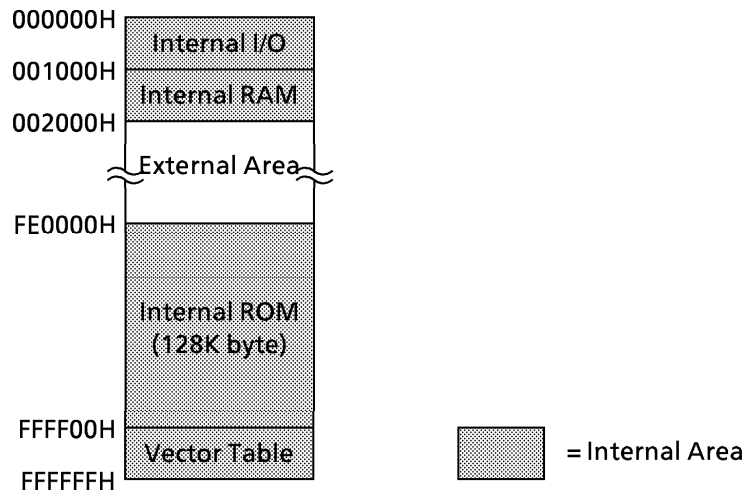


Figure 1 (1) Memory map of TMP91CW12 / PW12

MCU	ROM	RAM	Package	Adapter Socket
TMP91PW12F	OTP 128K-byte	4K-byte	LQFP100-P-1414-0.50C	BM11149

980901EBP1

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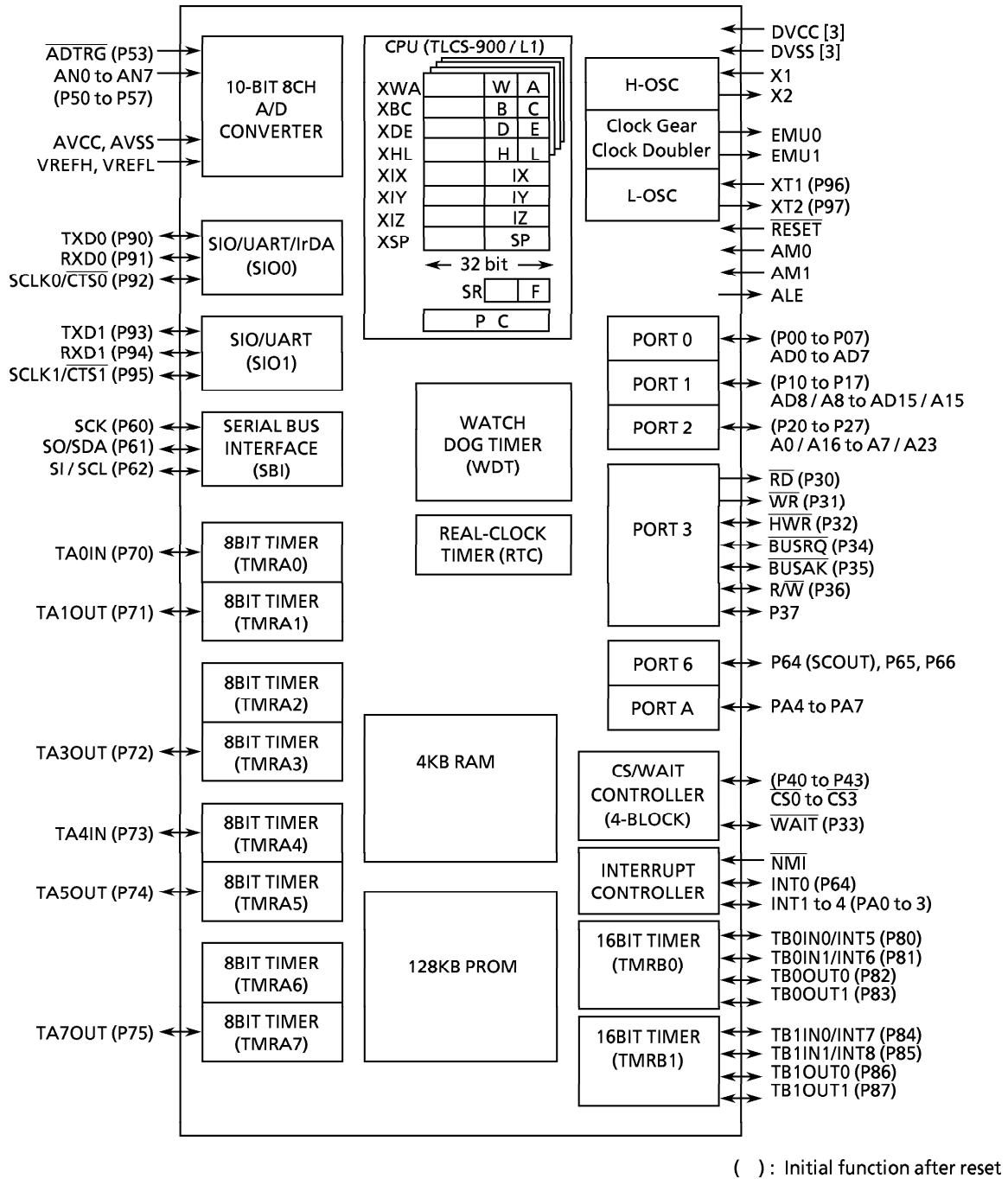


Figure 1 (2) TMP91PW12 Block Diagram

2. PIN ASSIGNMENT AND PIN FUNCTIONS

This section shows the TMP91PW12F pin assignment, and the names and an outline of the functions of the input/output pins.

2.1 Pin Assignment Diagram

Figure 2.1 is a pin assignment diagram for TMP91PW12F.

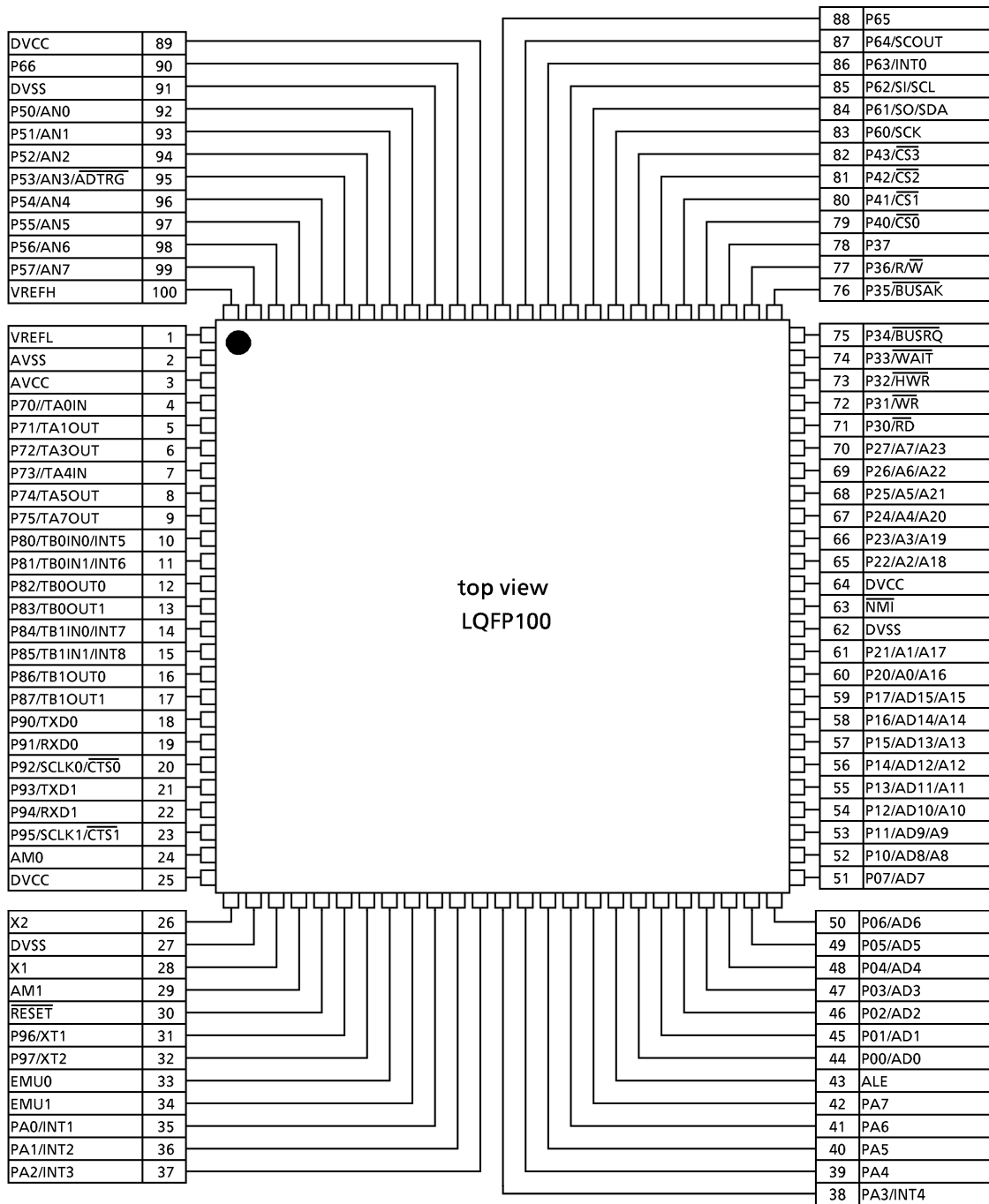


Figure 2.1 Pin Assignment Diagram (100-Pin LQFP)

## 2.2 Pin Names and Functions

The names of the input / output pins and their functions are described below.

Table 2.2 Pin Names and Functions.

Pin name	Number of pins	I/O	Functions
P00 to P07 AD0 to AD7	8	I/O Tri-state	Port 0: I/O port that allows I/O to be selected at the bit level Address and data (lower): Bits 0 to 7 for address and data bus
P10 to P17 AD8 to AD15 A8 to A15	8	I/O Tri-state Output	Port 1: I/O port that allows I/O to be selected at the bit level Address and data (upper): Bits 8 to 15 for address and data bus Address: Bits 8 to 15 for address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows to be selected at the bit level (with pull-down resistor) Address: Bits 0 to 7 for address bus Address: Bits 16 to 23 for address bus
P30 $\overline{RD}$	1	Output Output	Port 30: Output port Read: Strobe signal for reading external memory
P31 $\overline{WR}$	1	Output Output	Port 31: Output port Write: Strobe signal for writing data on pins AD0 to 7
P32 $\overline{HWR}$	1	I/O Output	Port 32: I/O port (with pull-up resistor) High write: Strobe signal for writing data on pins AD8 to 15
P33 $\overline{WAIT}$	1	I/O Input	Port 33: I/O port (with pull-up resistor) Wait: Pin used to request CPU bus wait
P34 $\overline{BUSRQ}$	1	I/O Input	Port 34: I/O port (with pull-up resistor) Bus request: Signal used to request bus release.
P35 $\overline{BUSA\overline{K}}$	1	I/O Output	Port 35: I/O port (with pull-up resistor) Bus acknowledge: Signal used to acknowledge bus release.
P36 $\overline{R/W}$	1	I/O Output	Port 36: I/O port (with pull-up resistor) Read/write: 1 represents read or dummy cycle; 0 represents write cycle.
P37	1	I/O	Port 37: I/O port (with pull-up resistor)
P40 $\overline{CS0}$	1	I/O Output	Port 40: I/O port (with pull-up resistor) Chip select 0: Outputs 0 when address is within specified address area.
P41 $\overline{CS1}$	1	I/O Output	Port 41: I/O port (with pull-up resistor) Chip select 1: Outputs 0 if address is within specified address area.
P42 $\overline{CS2}$	1	I/O Output	Port 42: I/O port (with pull-up resistor) Chip select 2: Outputs 0 if address is within specified address area.
P43 $\overline{CS3}$	1	I/O Output	Port 43: I/O port (with pull-up resistor) Chip select 3: Outputs 0 if address is within specified address area.
P50 to P57 AN0 to AN7 ADTRG	8	Input Input Input	Port 5: Pin used to input port Analog input: Pin used to input to A/D converter A/D trigger: Signal used to request A/D start.

Note : This device's built-in memory or built-in I/O cannot be accessed by an external DMA controller, using the  $\overline{BUSRQ}$  and  $\overline{BUSA\overline{K}}$  signals.

Pin name	Number of pins	I/O	Functions
P60 SCK	1	I/O I/O	Port 60: I/O Port Serial Bus Interface Clock at SIO mode.
P61 SO SDA	1	I/O Output I/O	Port 61: I/O Port Serial Bus Interface Output data at SIO mode. Serial Bus Interface Data at I2C mode.
P62 SI SCL	1	I/O Input I/O	Port 62: I/O Port Serial Bus Interface Input data at SIO mode. Serial Bus Interface Clock at I2C mode.
P63 INT0	1	I/O Input	Port 63: I/O Port Interrupt request pin 0: Interrupt request pin with programmable level / rising edge / falling edge
P64 SCOUT	1	I/O Output	Port 64: I/O Port System Clock Output: Output $f_{FPH}$ or $f_s$ clock
P65	1	I/O	Port 65: I/O Port
P66	1	I/O	Port 66: I/O Port
P70 TA0IN	1	I/O Input	Port 70: I/O Port Timer A0 input
P71 TA1OUT	1	I/O Output	Port 71: I/O Port Timer A1 output
P72 TA3OUT	1	I/O Output	Port 72: I/O Port Timer A3 output
P73 TA4IN	1	I/O Input	Port 73: I/O Port Timer A4 input
P74 TA5OUT	1	I/O Output	Port 74: I/O Port Timer A5 output
P75 TA7OUT	1	I/O Output	Port 75: I/O Port Timer A7 output
P80 TB0IN0  INT5	1	I/O Input  Input	Port 80: I/O Port Timer B0 input 0 Interrupt request pin 5: Interrupt request pin with programmable rising edge / falling edge
P81 TB0IN1 INT6	1	I/O Input Input	Port 81: I/O Port Timer B0 input 1 Interrupt request pin 6: Interrupt request pin with rising edge
P82 TB0OUT0	1	I/O Output	Port 82: I/O Port Timer B0 output 0
P83 TB0OUT1	1	I/O Output	Port 83: I/O Port Timer B0 output 1

Pin name	Number of pins	I/O	Functions
P84 TB1IN0 INT7	1	I/O Input Input	Port 84: I/O Port Timer B1 input 0 Interrupt request pin 7: Interrupt request pin with programmable rising edge / falling edge
P85 TB1IN1 INT8	1	I/O Input Input	Port 85: I/O Port Timer B1 input 1 Interrupt request pin 8: Interrupt request pin with rising edge
P86 TB1OUT0	1	I/O Output	Port 86: I/O Port Timer B1 output 0
P87 TB1OUT1	1	I/O Output	Port 87: I/O Port Timer B1 output 1
P90 TXD0	1	I/O Output	Port 90: I/O Port Serial send data 0
P91 RXD0	1	I/O Input	Port 91: I/O Port Serial receive data 0
P92 SCLK0 CTS0	1	I/O Input I/O	Port 92: I/O Port Serial clock I/O 0 Serial data send enable 0 (Clear to Send)
P93 TXD1	1	I/O Output	Port 93: I/O Port Serial send data 1
P94 RXD1	1	I/O Input	Port 94: I/O Port (with pull-up resistor) Serial receive data 1
P95 SCLK1 CTS1	1	I/O I/O Input	Port 95: I/O Port (with pull-up resistor) Serial clock I/O 1 Serial data send enable 1 (Clear to Send)
P96 XT1	1	I/O Input	Port 96: I/O port (Open Drain Output) Low Frequency Oscillator connecting pin
P97 XT2	1	I/O Output	Port 97: I/O port (Open Drain Output) Low Frequency Oscillator connecting pin
PA0 to PA3 INT1 to INT4	4	I/O Input	Port A0 to A3: I/O Port Interrupt request pin 1 to 4: Interrupt request pin with programmable rising edge / falling edge
PA4 to PA7	4	I/O	Port A4 to A7: I/O Port
ALE	1	Output	Address Latch Enable Can be disabled for reducing noise.
NMI	1	Input	Non-maskable interrupt request pin: Interrupt request pin with programmable falling edge or both edges.
AM0/AM1	2	Input	Address mode: The Vcc pin should be connected.
EMU0/EMU1	2	Output	Test pin: Open pins.
RESET	1	Input	Reset: Initializes TMP91CW12. (With pull-up resistor)

Pin name	Number of pins	I/O	Functions
VREFH	1	Input	Pin for reference voltage input to A/D converter (H)
VREFL	1	Input	Pin for reference voltage input to A/D converter (L)
X1/X2	2	I/O	High Frequency Oscillator connecting pin
AVCC	1		Power supply pin for A/D converter
AVSS	1		GND pin for A/D converter (0 V)
DVCC	3		Power supply pin (All Vcc pins should be connected with the power supply pin.)
DVSS	3		GND pin (0 V) (All Vss pins should be connected with GND (0 V).)

Note : All pins that have built-in pull-up resistors (other than the  $\overline{\text{RESET}}$  pin) can be disconnected from the built-in pull-up resistor by software.

2.3 PROM Mode

Table 2.2 (2) Name and function of PROM mode

Pin function	Pin number	Input / Output	Function	Pin name (MCU mode)
A7 to A0	8	Input	Memory address of program	P27 to P20
A15 to A8	8	Input		P17 to P10
A16	1	Input		P33
D7 to D0	8	I/O	Memory data of program	P07 to P00
$\overline{CE}$	1	Input	Chip enable	P32
$\overline{OE}$	1	Input	Output control	P30
$\overline{PGM}$	1	Input	Program control	P31
VPP	1	Power supply	12.75 V / 5 V (Power supply of program)	AM1
VCC	4	Power supply	6.25 V / 5 V	DVCC, AVCC
VSS	4	Power supply	0 V	DVSS, AVSS
Pin function	Pin number	Input / Output	Disposal of pin	
P34	1	Input	Fix to low level (security pin)	
$\overline{RESET}$	1	Input	Fix to low level (PROM mode)	
AM0	1	Input		
ALE	1	Output	Open	
X1	1	Input	Crystal	
X2	1	Output		
P42 to P40 P37 to P35 P75 to P70	12	Input	Fix to high level	
P43 P57 to P50 P66 to P60 P87 to P80 P97 to P90 PA7 to PA0 VREFH VREFL $\overline{NMI}$ EMU1, 0	51	I/O	open	



3. OPERATION

This section describes in blocks the functions and basic operations of TMP91PW12.

The TMP91PW12 has PROM in place of the mask ROM which is included in the TMP91CW12. The other configuration and functions are the same as the TMP91CW12. Regarding the function of the TMP91PW12, which is not described herein, see the TMP91CW12.

The TMP91PW12 has two operational modes: MCU mode and PROM mode.

3.1 MCU mode

(1) Mode-setting and function

The MCU mode is set by driving “High” the AM1 and AM0 pin. In the MCU mode, the operation is same as TMP91CW12.

3.2 Memory Map

Figure 3.2 (1), (2) are memory map of the TMP91PW12.

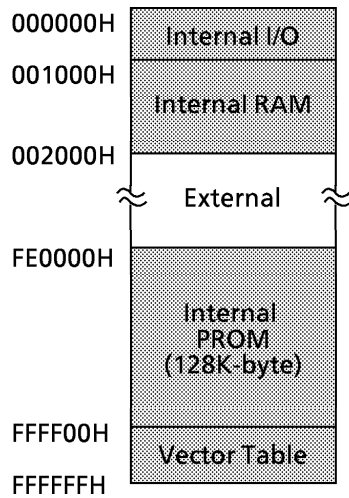


Figure 3.2 (1) Memory map in MCU mode

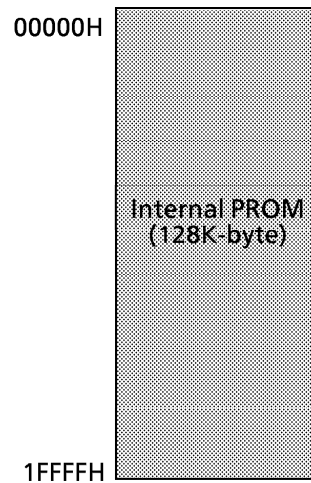


Figure 3.2 (2) Memory map in PROM mode

### 3.3 PROM Mode

#### (1) Mode setting and Function

PROM mode is set by setting the  $\overline{\text{RESET}}$  and AM0 pins to the “L” level, and set by setting the AM1 pin to “VPP” level. The programming and verification for the internal PROM is achieved by using a general PROM programmer with the adaptor socket.

- ① OTP adaptor  
BM11149 : TMP91PW12F adaptors
- ② Setting OTP adaptor  
Set the switch (SW1) to N side.
- ③ Setting PROM programmer
  - i) Set PROM type to TC571000D.  
Size : 1 M bit (128K×8 bit)  
VPP : 12.75 V  
tpw : 100  $\mu$ s

The electric signature mode (hereinafter referred to as “signature”) is not supported. Therefore if signature is used, the device is damaged because 12.75 V is applied to A9 of address. Do not use signature.

#### ii) Transferring the data (copy)

In TMP91PW12, PROM is placed on addresses 00000 to 1FFFFH in PROM mode, and addresses FE0000H to FFFFFFFH in MCU mode. Therefore data should be transferred to addresses 00000 to 1FFFFH in PROM mode using the object converter (tuconv) or the block transfer mode (see instruction manual of PROM programmer.) or making the object data.

#### iii) Setting the programming address

Start address : 00000H  
End address : 1FFFFH

④ Programming

Program/verify according to the procedures of PROM programmer.

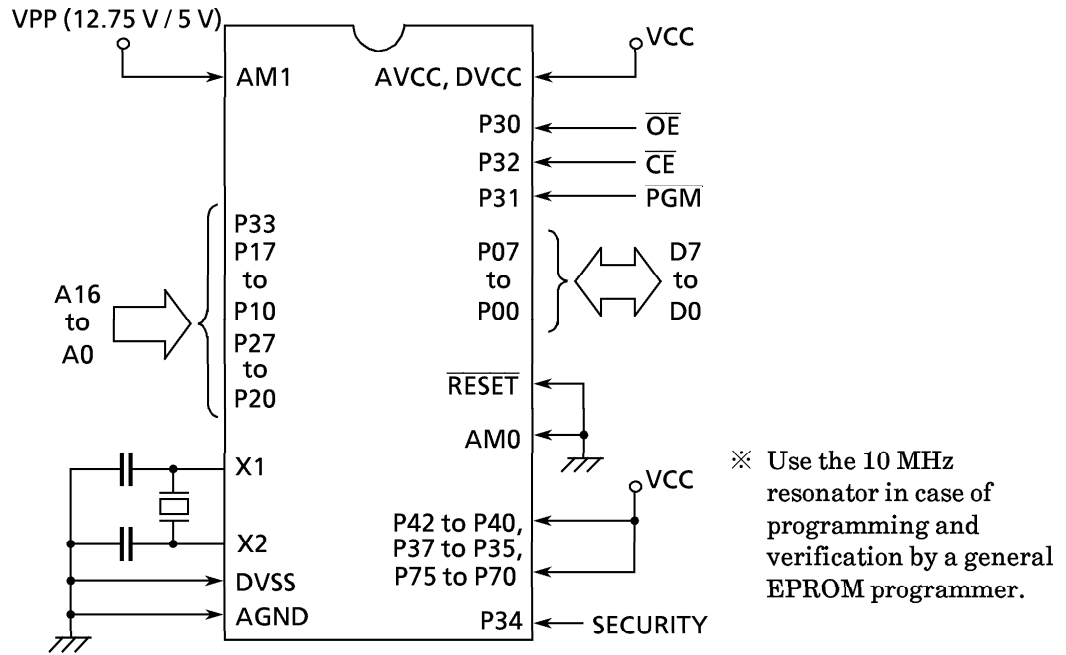


Figure 3.3 (1) PROM Mode Pin Setting

(2) Programming Flow Chart

The programming mode is set by applying 12.75 V (programming voltage) to the AM1 pin when the following pins are set as follows,

(VCC : 6.25 V,  $\overline{\text{RESET}}$  : "L" level, AM0 : "L" level).

While address and data are fixed and  $\overline{\text{CE}}$  pin is set to "L" level, 0.1 ms of "L" level pulse is applied to  $\overline{\text{PGM}}$  pin to program the data.

Then the data in the address is verified.

If the programmed data is incorrect, another 0.1 ms pulse is applied to  $\overline{\text{PGM}}$  pin.

This programming procedure is repeated until correct data is read from the address. (25 times maximum)

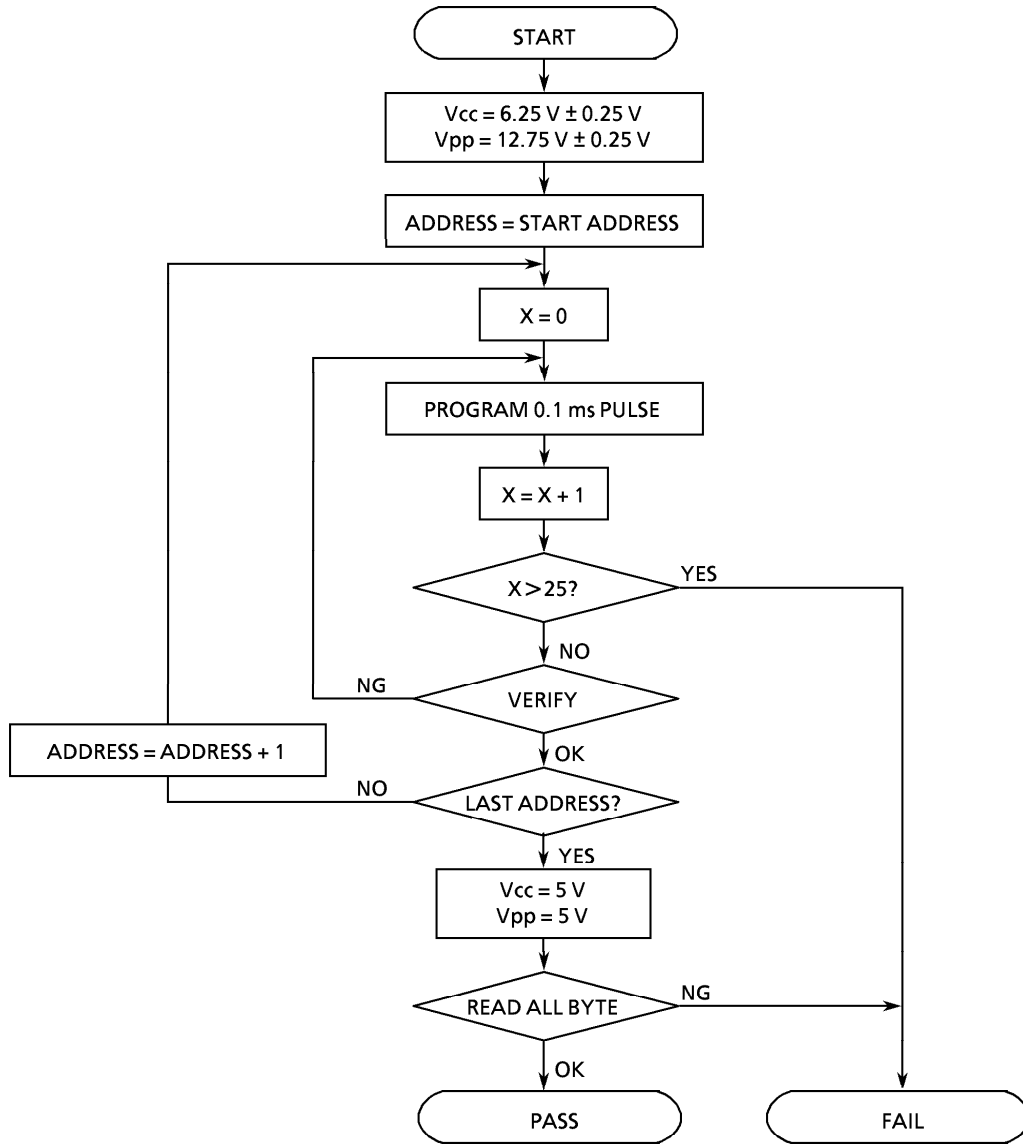
Subsequently, all data are programmed in all addresses.

The verification for all data is done under the condition of AM1 = Vcc = 5 V after all data were written.

Figure 3.3 (2) shows the programming flow chart.

High Speed Program Writing.

Flow chart



Note : V<sub>pp</sub> means AM1 pin.

Figure 3.3 (2) Flow chart

**(3) Security Bit**

The TMP91PW12 has a Security Bit.

If the Security Bit is programmed to “0”, the content of the PROM can not be read in PROM mode.  
(outputs data FFH)

How to program the Security Bit.

The difference from the programming procedures described in section 3.3 (1) are follows.

- ① Setting OTP adapter  
Set the switch (SW1) to S side.
- ② Setting PROM programmer
  - ii) Transferring the data
  - iii) Setting programming address

The security bit is in bit 0 of address 00000H.  
Set the start address 00000H and the end address 00000H.  
Set the data FEH at the address 00000H.

## 4. ELECTRICAL CHARACTERISTICS (TENTATIVE)

## 4.1 Absolute Maximum

Symbol	Parameter	Rating	Unit
V <sub>CC</sub>	Power Supply Voltage	- 0.5 to 6.5	V
V <sub>IN</sub>	Input Voltage	- 0.5 to V <sub>CC</sub> + 0.5	V
I <sub>OL</sub>	Output Current	2	mA
I <sub>OH</sub>	Output Current	- 2	mA
∑ I <sub>OL</sub>	Output Current (total)	80	mA
∑ I <sub>OH</sub>	Output Current (total)	- 80	mA
P <sub>D</sub>	Power Dissipation (Ta = 85 °C)	600	mW
T <sub>SOLDER</sub>	Soldering Temperature (10 s)	260	°C
T <sub>STG</sub>	Storage Temperature	- 65 to 150	°C
T <sub>OPR</sub>	Operating Temperature	- 40 to 85	°C

## 4.2 DC Characteristics (1/2)

Symbol	Parameter	Min.	Typ. (Note)	Max.	Unit	Condition
V <sub>CC</sub>	Power Supply Voltage (AV <sub>CC</sub> = DV <sub>CC</sub> ) (AV <sub>SS</sub> = DV <sub>SS</sub> = 0 V)	2.7 4.5		5.5	V	fc = 2 to 16 MHz    fs = 30 to 34 kHz fc = 4 to 25 MHz
V <sub>IL</sub>	Input Low Voltage	- 0.3		0.6	V	V <sub>CC</sub> < 4.5V
V <sub>IL1</sub>				0.8		V <sub>CC</sub> ≥ 4.5V
V <sub>IL2</sub>				0.3V <sub>CC</sub>		V <sub>CC</sub> = 2.7 to 5.5V
V <sub>IL3</sub>				0.25V <sub>CC</sub>		
V <sub>IL4</sub>				0.3		
V <sub>IH</sub>	Input High Voltage	2.0 2.2		V <sub>CC</sub> + 0.3	V	V <sub>CC</sub> < 4.5V
V <sub>IH1</sub>		0.7V <sub>CC</sub>				V <sub>CC</sub> ≥ 4.5V
V <sub>IH2</sub>		0.75V <sub>CC</sub>				V <sub>CC</sub> = 2.7 to 5.5V
V <sub>IH3</sub>		V <sub>CC</sub> - 0.3				
V <sub>IH4</sub>		0.8V <sub>CC</sub>				
V <sub>OL</sub>	Output Low Voltage			0.45	V	I <sub>OL</sub> = 1.6 mA (V <sub>CC</sub> = 2.7 to 5.5V)
V <sub>OH</sub>	Output High Voltage	2.4			V	I <sub>OH</sub> = - 400 μA (V <sub>CC</sub> = 3.0V ± 10%)
		4.2				I <sub>OH</sub> = - 400 μA (V <sub>CC</sub> = 5.0V ± 10%)

Note : Typical values are for Ta = 25 °C and V<sub>CC</sub> = 3.0 V unless otherwise noted.

## 4.2 DC Characteristics (2/2)

Symbol	Parameter	Min	Typ. (Note1)	Max	Unit	Condition	
$I_{LI}$	Input Leakage Current		0.02	$\pm 5$	$\mu A$	$0.0 \leq V_{IN} \leq V_{CC}$	
$I_{LO}$	Output Leakage Current		0.05	$\pm 10$		$0.2 \leq V_{IN} \leq V_{CC} - 0.2$	
$V_{STOP}$	Power Down Voltage (@ STOP, RAM Back up)	2.0		6.0	V	$V_{IL2} = 0.2 V_{CC}$ , $V_{IH2} = 0.8 V_{CC}$	
$R_{RST}$	RESET Pull Up Resister	100		400	$k\Omega$	$V_{CC} = 3 V \pm 10 \%$	
		50		230		$V_{CC} = 5 V \pm 10 \%$	
$C_{IO}$	Pin Capacitance			10	pF	$f_c = 1 \text{ MHz}$	
$V_{TH}$	Schmitt Width RESET, NMI, INTO	0.4	1.0		V		
$P_{KH}$	Programmable Pull Up Resister	100		400	$k\Omega$	$V_{CC} = 3 V \pm 10 \%$	
		50		230		$V_{CC} = 5 V \pm 10 \%$	
$I_{CC}$	NORMAL (Note2)		8.8	14.0	mA	$V_{CC} = 3 V \pm 10 \%$ $f_c = 16 \text{ MHz}$	
	IDLE2		3.0	4.5			
	IDLE1		0.9	1.8			
	NORMAL (Note2)		23.5	35.0	mA	$V_{CC} = 5 V \pm 10 \%$ $f_c = 25 \text{ MHz}$ (Typ. : $V_{CC} = 5.0 \text{ V}$ )	
	IDLE2		9.5	15.0			
	IDLE1		4.4	9.0			
	SLOW (Note2)		30.0	60.0	$\mu A$	$V_{CC} = 3 V \pm 10 \%$ $f_s = 32.768 \text{ kHz}$	
	IDLE2		11.0	25.0			
	IDLE1		8.0	15.0			
	STOP			0.2	10	$\mu A$	$T_a \leq 50^\circ C$
20					$T_a \leq 70^\circ C$		
50					$T_a \leq 85^\circ C$		
						$V_{CC} = 2.7 \text{ to } 5.5 \text{ V}$	

Note 1: Typical values are for  $T_a = 25^\circ C$  and  $V_{CC} = 3.0 \text{ V}$  unless otherwise noted.

Note 2:  $I_{CC}$  measurement condition (NORMAL, SLOW):

Only CPU is operational; output pins are open and input pins are fixed.

## 4.3 AC Characteristics

(1)  $V_{CC} = 3.0\text{ V} \pm 10\%$ 

No.	Symbol	Parameter	Variable		16 MHz		Unit
			Min	Max	Min	Max	
1	$t_{FPH}$	$f_{FPH}$ Period (= x)	62.5	31250	62.5		ns
2	$t_{AL}$	A0 to 15 Valid → ALE Fall	$0.5x - 26$		5		ns
3	$t_{LA}$	ALE Fall → A0 to 15 Hold	$0.5x - 26$		5		ns
4	$t_{LL}$	ALE High Width	$x - 52$		10		ns
5	$t_{LC}$	ALE Fall → $\overline{RD}/\overline{WR}$ Fall	$0.5x - 28$		3		ns
6	$t_{CLR}$	$\overline{RD}$ Rise → ALE Rise	$0.5x - 26$		5		
7	$t_{CLW}$	$\overline{WR}$ Rise → ALE Rise	$x - 26$		36		ns
8	$t_{ACL}$	A0 to 15 Valid → $\overline{RD}/\overline{WR}$ Fall	$x - 41$		21		ns
9	$t_{ACH}$	A0 to 23 Valid → $\overline{RD}/\overline{WR}$ Fall	$1.5x - 50$		43		ns
10	$t_{CAR}$	$\overline{RD}$ Rise → A0 to 23 Hold	$0.5x - 31$		0		
11	$t_{CAW}$	$\overline{WR}$ Rise → A0 to 23 Hold	$x - 31$		31		ns
12	$t_{ADL}$	A0 to 15 Valid → D0 to 15 Input		$3.0x - 87$		100	ns
13	$t_{ADH}$	A0 to 23 Valid → D0 to 15 Input		$3.5x - 98$		120	ns
14	$t_{RD}$	$\overline{RD}$ Fall → D0 to 15 Input		$2.0x - 75$		50	ns
15	$t_{RR}$	$\overline{RD}$ Low Width	$2.0x - 40$		85		ns
16	$t_{HR}$	$\overline{RD}$ Rise → D0 to 15 Hold	0		0		ns
17	$t_{RAE}$	$\overline{RD}$ Rise → A0 to 15 Output	$x - 25$		37		ns
18	$t_{WW}$	$\overline{WR}$ Low Width	$1.5x - 55$		39		ns
19	$t_{DW}$	D0 to 15 Valid → $\overline{WR}$ Rise	$1.5x - 78$		15		ns
20	$t_{WD}$	$\overline{WR}$ Rise → D0 to 15 Hold	$x - 49$		13		ns
21	$t_{AWH}$	A0 to 23 Valid → $\overline{WAIT}$ Input	$\left(\frac{1}{n} \overline{WAIT} + n \text{ mode}\right)$	$3.5x - 118$		100	ns
22	$t_{AWL}$	A0 to 15 Valid → $\overline{WAIT}$ Input	$\left(\frac{1}{n} \overline{WAIT} + n \text{ mode}\right)$	$3.0x - 117$		70	ns
23	$t_{CW}$	$\overline{RD}/\overline{WR}$ Fall → $\overline{WAIT}$ Hold	$\left(\frac{1}{n} \overline{WAIT} + n \text{ mode}\right)$	$2.0x + 0$	125		ns
24	$t_{APH}$	A0 to 23 Valid → PORT Input		$3.5x - 168$		50	ns
25	$t_{APH2}$	A0 to 23 Valid → PORT Hold	$3.5x$		218		ns
26	$t_{AP}$	A0 to 23 Valid → PORT Valid		$3.5x + 100$		319	ns

## AC Measuring Conditions

- Output Level : High 0.7 V<sub>CC</sub> / Low 0.3 V<sub>CC</sub>, CL = 50 pF
- Input Level : High 0.9 V<sub>CC</sub> / Low 0.1 V<sub>CC</sub>



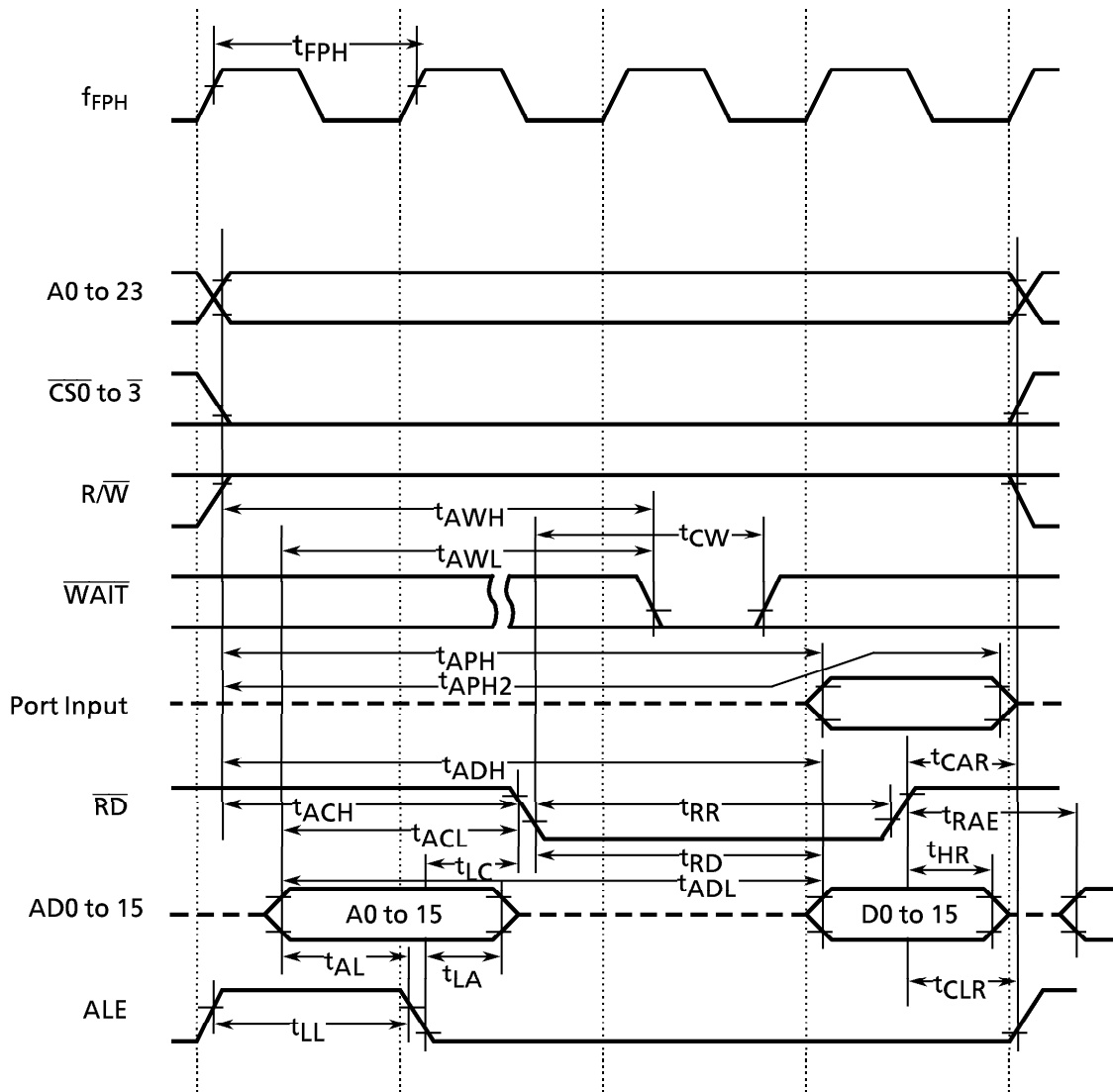
(2)  $V_{CC} = 5.0\text{ V} \pm 10\%$ 

No.	Symbol	Parameter	Variable		25 MHz		Unit
			Min	Max	Min	Max	
1	$t_{FPH}$	$f_{FPH}$ Period (= x)	40	31250	40		ns
2	$t_{AL}$	A0 to 15 Valid → ALE Fall	$0.5x - 15$		5		ns
3	$t_{LA}$	ALE Fall → A0 to 15 Hold	$0.5x - 15$		5		ns
4	$t_{LL}$	ALE High Width	$x - 20$		20		ns
5	$t_{LC}$	ALE Fall → $\overline{RD}/\overline{WR}$ Fall	$0.5x - 20$		0		ns
6	$t_{CLR}$	$\overline{RD}$ Rise → ALE Rise	$0.5x - 15$		5		
7	$t_{CLW}$	$\overline{WR}$ Rise → ALE Rise	$x - 15$		125		ns
8	$t_{ACL}$	A0 to 15 Valid → $\overline{RD}/\overline{WR}$ Fall	$x - 25$		15		ns
9	$t_{ACH}$	A0 to 23 Valid → $\overline{RD}/\overline{WR}$ Fall	$1.5x - 50$		10		ns
10	$t_{CAR}$	$\overline{RD}$ Rise → A0 to 23 Hold	$0.5x - 20$		0		
11	$t_{CAW}$	$\overline{WR}$ Rise → A0 to 23 Hold	$x - 20$		10		ns
12	$t_{ADL}$	A0 to 15 Valid → D0 to 15 Input		$3.0x - 45$		75	ns
13	$t_{ADH}$	A0 to 23 Valid → D0 to 15 Input		$3.5x - 35$		105	ns
14	$t_{RD}$	$\overline{RD}$ Fall → D0 to 15 Input		$2.0x - 40$		40	ns
15	$t_{RR}$	$\overline{RD}$ Low Width	$2.0x - 20$		40		ns
16	$t_{HR}$	$\overline{RD}$ Rise → D0 to 15 Hold	0		0		ns
17	$t_{RAE}$	$\overline{RD}$ Rise → A0 to 15 Output	$x - 15$		25		ns
18	$t_{WW}$	$\overline{WR}$ Low Width	$1.5x - 20$		25		ns
19	$t_{DW}$	D0 to 15 Valid → $\overline{WR}$ Rise	$1.5x - 50$		15		ns
20	$t_{WD}$	$\overline{WR}$ Rise → D0 to 15 Hold	$x - 15$		25		ns
21	$t_{AWH}$	A0 to 23 Valid → $\overline{WAIT}$ Input $\left(\begin{smallmatrix} 1 \\ +n \end{smallmatrix} \text{mode}\right)$		$3.5x - 90$		50	ns
22	$t_{AWL}$	A0 to 15 Valid → $\overline{WAIT}$ Input $\left(\begin{smallmatrix} 1 \\ +n \end{smallmatrix} \text{mode}\right)$		$3.0x - 80$		40	ns
23	$t_{CW}$	$\overline{RD}/\overline{WR}$ Fall → $\overline{WAIT}$ Hold $\left(\begin{smallmatrix} 1 \\ +n \end{smallmatrix} \text{mode}\right)$	$2.0x + 0$		80		ns
24	$t_{APH}$	A0 to 23 Valid → PORT Input		$3.5x - 120$		20	ns
25	$t_{APH2}$	A0 to 23 Valid → PORT Hold	$3.5x$		140		ns
26	$t_{AP}$	A0 to 23 Valid → PORT Valid		$3.5x + 100$		319	ns

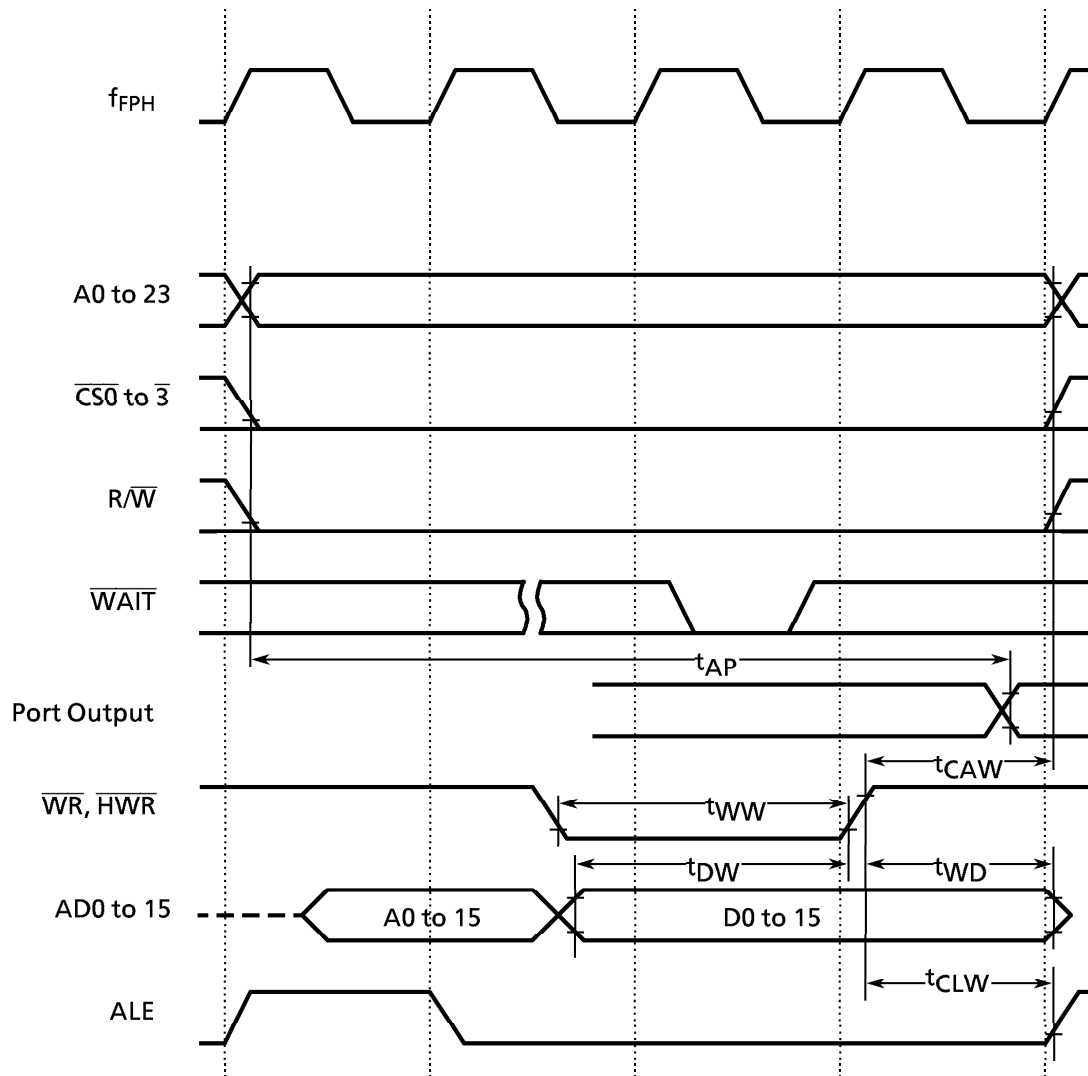
## AC Measuring Conditions

- Output Level : High 2.2 V / Low 0.8 V , CL = 50 pF
- Input Level : High 2.4 V / Low 0.45 V (AD0 to AD15)  
High 0.8 V<sub>CC</sub> / Low 0.2 V<sub>CC</sub> (except AD0 to AD15)

(1) Read Cycle



(2) Write Cycle



**4.4 A/D Conversion Characteristics**

$$AV_{CC} = V_{CC}, AV_{SS} = V_{SS}$$

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VREFH	Analog Reference Voltage (+)	$V_{CC} = 3V \pm 10\%$	$V_{CC} - 0.2V$	$V_{CC}$	$V_{CC}$	V
		$V_{CC} = 5V \pm 10\%$	$V_{CC} - 1.5V$	$V_{CC}$	$V_{CC}$	
VREFL	Analog Reference Voltage (-)	$V_{CC} = 3V \pm 10\%$	$V_{SS}$	$V_{SS}$	$V_{SS} + 0.2V$	
		$V_{CC} = 5V \pm 10\%$	$V_{SS}$	$V_{SS}$	$V_{SS} + 0.2V$	
VAIN	Analog Input Voltage Range		VREFL		VREFH	
IREF (VREFL = 0 V)	Analog Current for Analog Reference Voltage <VREFON> = 1	$V_{CC} = 3V \pm 10\%$		0.85	1.20	mA
		$V_{CC} = 5V \pm 10\%$		1.44	2.00	
		<VREFON> = 0	$V_{CC} = 2.7 \text{ to } 5.5V$		0.02	5.0
-	Error (not including quantizing errors)	$V_{CC} = 3V \pm 10\%$		$\pm 1.0$	$\pm 4.0$	LSB
		$V_{CC} = 5V \pm 10\%$		$\pm 1.0$	$\pm 4.0$	

Note 1:  $1LSB = (VREFH - VREFL) / 1024 [V]$

Note 2: The operation above is guaranteed for  $f_{FPH} \geq 4 \text{ MHz}$ .

Note 3: The value  $I_{CC}$  includes the current which flows through the  $AV_{CC}$  pin.

4.5 Serial Channel Timing (I/O Internal Mode)

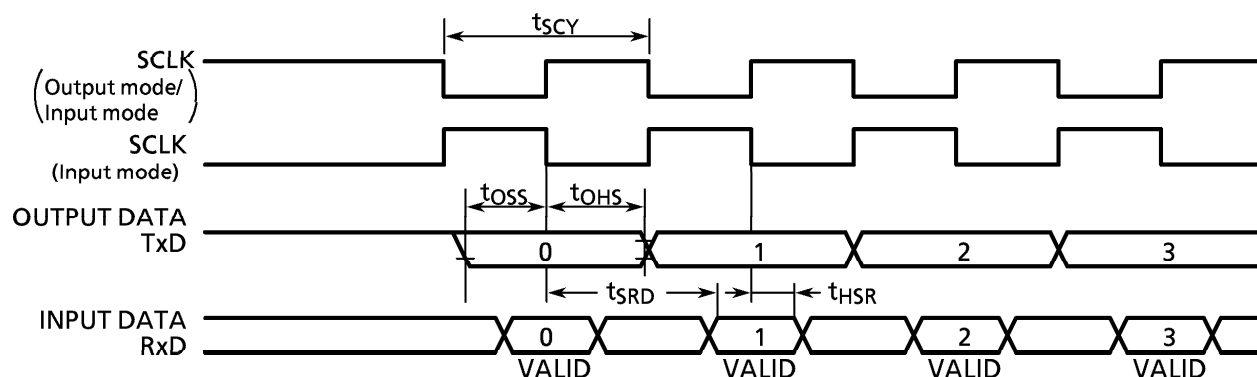
(1) SCLK Input Mode

Symbol	Parameter	Variable		25 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t <sub>SCY</sub>	SCLK Period	16X		0.64		1.0		μs
t <sub>OSS</sub>	Output Data → SCLK Rising / Falling Edge *	t <sub>SCY</sub> / 2 – 50		270		450		ns
t <sub>OHS</sub>	SCLK Rising / Falling Edge * → Output Data Hold	t <sub>SCY</sub> / 2 – 100		220		400		ns
t <sub>HSR</sub>	SCLK Rising / Falling Edge * → Input Data Hold	0		0		0		ns
t <sub>SRD</sub>	SCLK Rising / Falling Edge * → Valid Data Input		t <sub>SCY</sub> / 2 – 100		220		400	ns

\*) SCLK Rising/Falling Edge : The rising edge is used in SCLK rising mode.  
The falling edge is used in SCLK falling mode.

(2) SCLK Output Mode

Symbol	Parameter	Variable		25 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t <sub>SCY</sub>	SCLK Period (Programmable)	16X	8192X	0.64	327	1.0	512	μs
t <sub>OSS</sub>	Output Data → SCLK Rising Edge	t <sub>SCY</sub> / 2 – 150		170		350		ns
t <sub>OHS</sub>	SCLK Rising Edge → Output Data Hold	t <sub>SCY</sub> / 2 – 80		240		420		ns
t <sub>HSR</sub>	SCLK Rising Edge → Input Data Hold	0		0		0		ns
t <sub>SRD</sub>	SCLK Rising Edge → Valid Data Input		t <sub>SCY</sub> / 2 – 150		170		350	ns



4.6 Event Counter (TA0IN, TA4IN, TB0IN0, TB0IN1, TB1IN0, TB1IN1)

Symbol	Parameter	Variable		25 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t <sub>VCK</sub>	Clock Period	8X + 100		420		600		ns
t <sub>VCKL</sub>	Clock Low Level width	4X + 40		200		290		ns
t <sub>VCKH</sub>	Clock High Level width	4X + 40		200		290		ns

4.7 Interrupt, Capture

(1)  $\overline{\text{NMI}}$ , INT0 to 4 Interrupts

Symbol	Parameter	Variable		25 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t <sub>INTAL</sub>	$\overline{\text{NMI}}$ , INT0 to 4 Low level width	4X + 40		200		290		ns
t <sub>INTAH</sub>	$\overline{\text{NMI}}$ , INT0 to 4 High level width	4X + 40		200		290		ns

(2) INT5 to 8 Interrupt, Capture

The INT5 to 8 input width depends on the system clock select mode, prescaler clock mode.

System Clock selected <SYSCK>	Prescaler Clock selected <PRCK1, 0>	t <sub>INTBL</sub> (INT5 to 8 Low Level Width)		t <sub>INTBH</sub> (INT5 to 8 High Level Width)		Unit
		Variable	16 MHz	Variable	16 MHz	
		Min	Max	Min	Max	
0 (fc)	00 (f <sub>FPH</sub> )	8X + 100	600	8X + 100	600	ns
	10 (fc/16)	128Xc + 0.1	8.1	128Xc + 0.1	8.1	μs
1 (fs)	00 (f <sub>FPH</sub> )	8X + 0.1	244.3	8X + 0.1	244.3	

Note : Xc = Period of Clock fc

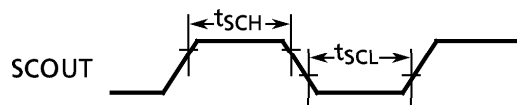
4.8 SCOUT pin AC characteristics

Symbol	Parameter	Variable		25 MHz		16 MHz		Condition	Unit
		Min	Max	Min	Max	Min	Max		
t <sub>sch</sub>	Low Level width	0.5T - 20		-		11		V <sub>CC</sub> = 3 V ± 10%	ns
		0.5T - 15		5		16		V <sub>CC</sub> = 5 V ± 10%	
t <sub>scl</sub>	High level width	0.5T - 20		-		11		V <sub>CC</sub> = 3 V ± 10%	ns
		0.5T - 15		5		16		V <sub>CC</sub> = 5 V ± 10%	

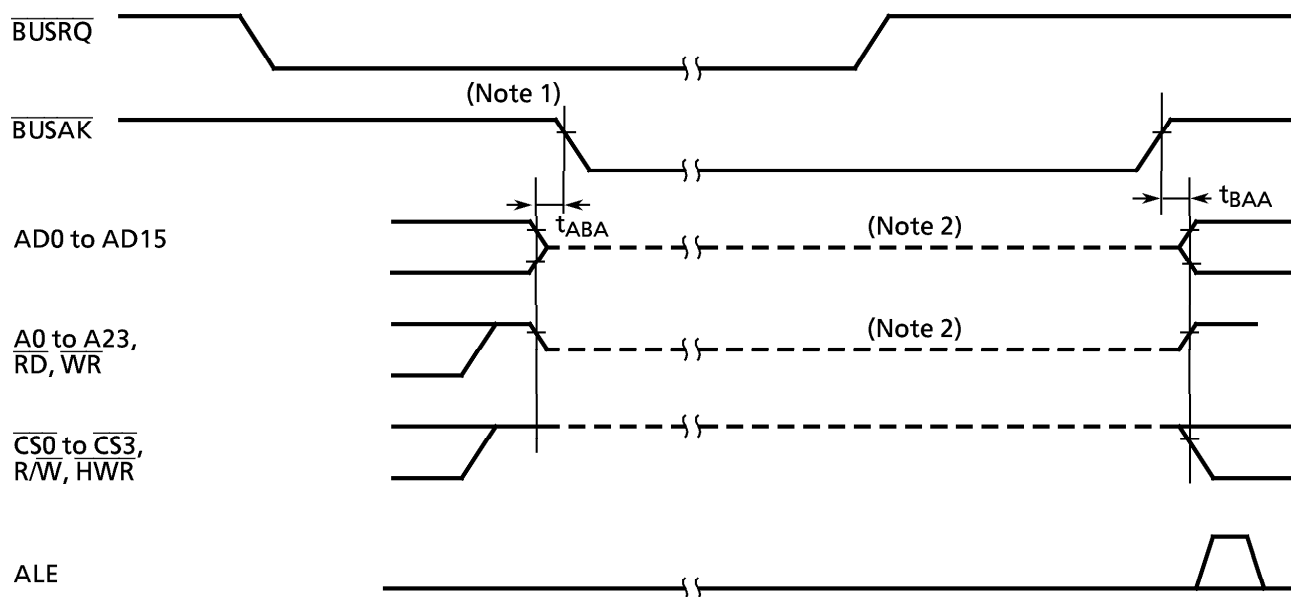
Note : T = Period of SCOUT

Measurement Condition

- Output Level : High 0.7 V<sub>CC</sub> / Low 0.3 V<sub>CC</sub>, CL = 10 pF



4.9 Bus Request / Bus Acknowledge



Symbol	Parameter	Variable		25 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t <sub>ABA</sub>	Output Buffer off to $\overline{\text{BUSAK}}$ Low	0	80	0	80	0	80	ns
t <sub>BAA</sub>	$\overline{\text{BUSAK}}$ High to Output Buffer on	0	80	0	80	0	80	ns

Note1 : Even if the  $\overline{\text{BUSRQ}}$  signal goes low, the bus will not be released while the  $\overline{\text{WAIT}}$  signal is low. The bus will only be released when  $\overline{\text{BUSRQ}}$  goes low while  $\overline{\text{WAIT}}$  is high.

Note2 : This line shows only that the output buffer is in the off state. It does not indicate that the signal level is fixed. Just after the bus is released, the signal level set before the bus was released is maintained dynamically by the external capacitance. Therefore, to fix the signal level using an external resistor during bus release, careful design is necessary, as fixing of the level is delayed. The internal programmable pull-up/pull-down resistor is switched between the active and non-active states by the internal signal.

## 4.10 Read operation in PROM mode

DC / AC characteristics

 $T_a = 25 \pm 5 \text{ }^\circ\text{C}$   $V_{CC} = 5 \text{ V} \pm 10 \%$ 

Symbol	Parameter	Condition	Min	Max	Unit
$V_{PP}$	$V_{PP}$ Read Voltage	–	4.5	5.5	V
$V_{IH1}$	Input High Voltage (A0 to A16, $\overline{CE}$ , $\overline{OE}$ , $\overline{PGM}$ )	–	2.2	$V_{CC} + 0.3$	V
$V_{IL1}$	Input Low Voltage (A0 to A16, $\overline{CE}$ , $\overline{OE}$ , $\overline{PGM}$ )	–	–0.3	0.8	V
$t_{ACC}$	Address to Output Delay	$C_L = 50 \text{ pF}$	–	$2.25TCYC + \alpha$	ns

TCYC = 400 ns (10 MHz Clock)

 $\alpha = 200 \text{ ns}$ 

## 4.11 Program operation in PROM mode

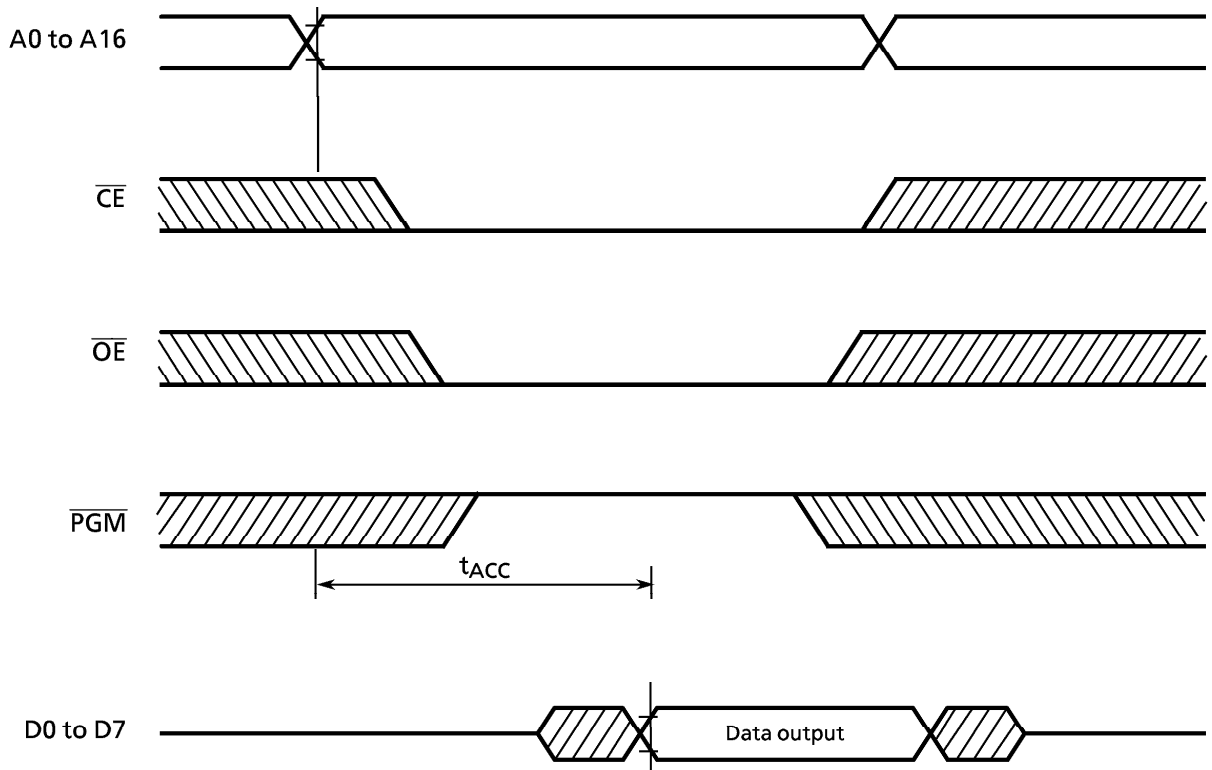
DC / AC characteristics

 $T_a = 25 \pm 5 \text{ }^\circ\text{C}$   $V_{CC} = 6.25 \text{ V} \pm 0.25 \text{ V}$ 

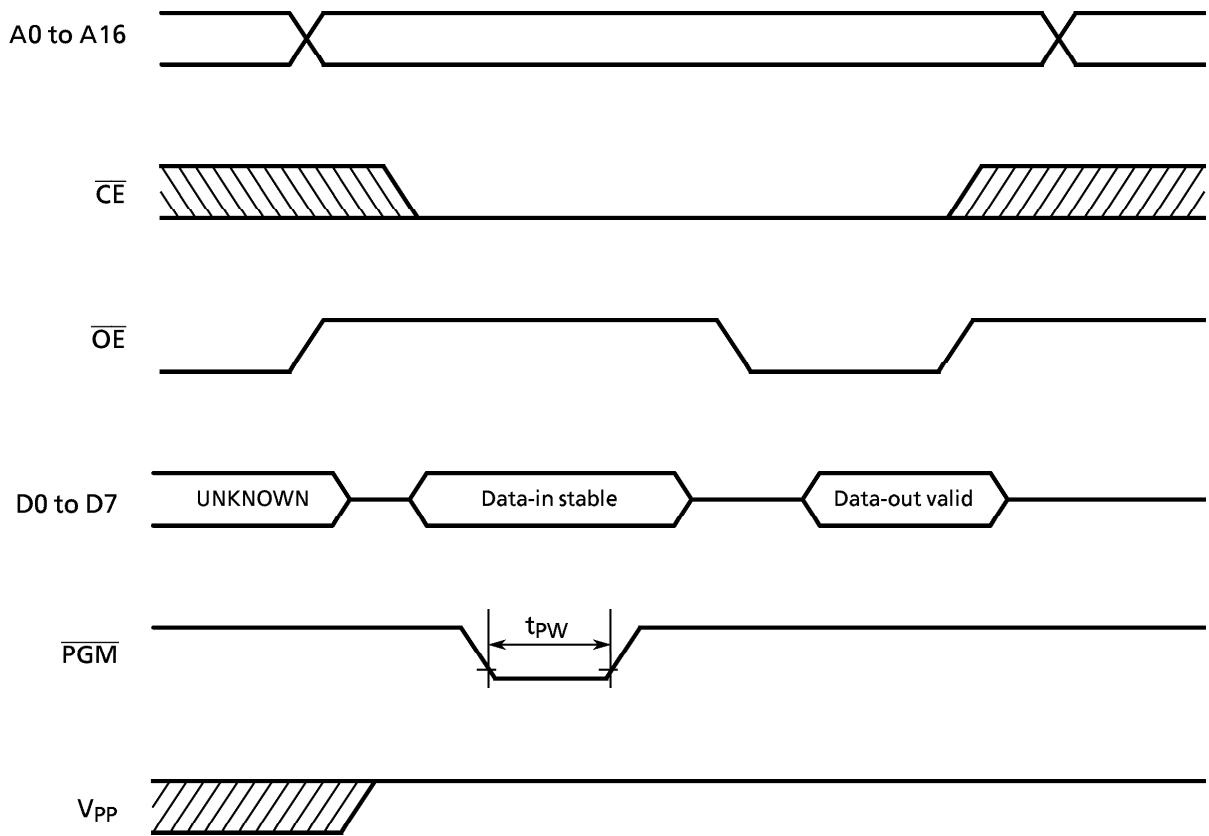
Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{PP}$	Programming Supply Voltage	–	12.50	12.75	13.00	V
$V_{IH}$	Input High Voltage (D0 to D7, A0 to A16, $\overline{CE}$ , $\overline{OE}$ , $\overline{PGM}$ )	–	2.6		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage (D0 to D7, A0 to A16, $\overline{CE}$ , $\overline{OE}$ , $\overline{PGM}$ )	–	–0.3		0.8	V
$I_{CC}$	$V_{CC}$ Supply Current	$f_c = 10 \text{ MHz}$	–		50	mA
$I_{PP}$	$V_{PP}$ Supply Current	$V_{PP} = 13.00 \text{ V}$	–		50	mA
$t_{PW}$	$\overline{PGM}$ Program Pulse Width	$C_L = 50 \text{ pF}$	0.095	0.1	0.105	ms



4.12 Timing chart of read operation in PROM mode



4.13 Timing chart of program operation in PROM mode



NOTE

1. The power supply of  $V_{PP}$  (12.75 V) must be turned on at the same time or the later time for a power supply of  $V_{CC}$  and must be turned off at the same time or early time for a power supply of  $V_{CC}$ .
2. The device suffers a damage taking out and putting in on the condition of  $V_{PP} = 12.75$  V.
3. The maximum spec of  $V_{PP}$  pin is 14.0 V. Be carefull a overshoot at the programming.