TVP5150PBS Ultralow-Power NTSC/PAL Video Decoder

Data Manual

Literature Number: SLES043A
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1 TVP5150 Features

- Accepts NTSC (N, 4.43), PAL (B, D, G, H, I, M, N) Video Data
- Supports ITU−R BT.601 Standard Sampling
- High-Speed 9-Bit A/D Converter
- Two Composite Inputs or One S-Video Input
- Fully Differential CMOS Analog Preprocessing Channels With Clamping and AGC For Best S/N Performance
- Ultralow Power Consumption: 113 mW Typical
- 32-Pin TQFP Package
- Power-Down Mode: <1 mW
- Brightness, Contrast, Saturation, Hue, and Sharpness Control Through I^2C
- Complementary 4-Line (3-H Delay) Adaptive Comb Filters For Both Cross-Luminance And Cross-Chrominance Noise Reduction
- Patented Architecture For Locking To Weak, Noisy, Or Unstable Signals
- Single 14.318-MHz Crystal for All Standards
- Internal PLL For Line-Locked Clock and Sampling
- Subcarrier Genlock Output For Synchronizing Color Subcarrier Of External Encoder. Standard Programmable Video Output Format:
  - ITU−R BT.656, 8-Bit 4:2:2 With Embedded Syncs
- Macrovision™ Copy Protection Detection
- Advanced Programmable Video Output Formats:
  - 2x Oversampled Raw VBI Data During Active Video
  - Sliced VBI Data During Horizontal Blanking Or Active Video
- VBI Modes Supported
  - Teletext (NABTS, WST) Closed-Caption Decode With FIFO
  - Wide Screen Signaling, Video Program System, CGMS, Vertical Interval Time Code
  - Custom Configuration Mode That Allows The User To Program The Slice Engine For Unique VBI Data Signals
- Power-on Reset

2 Introduction

2.1 Description

The TVP5150 device is an ultralow-power video decoder for NTSC and PAL video signals. Available in a space saving 32-pin TQFP package, the TVP5150 device converts NTSC and PAL video signals to 8-bit ITU−R BT.656 format. Discrete syncs are also available. The optimized architecture of the TVP5150 device allows for ultralow-power consumption. The device consumes 113 mW of power in typical operation and consumes less than 1 mW in power-down mode, considerably increasing battery life in portable applications. The device uses just one crystal for all supported standards. The TVP5150 device can be programmed using an I^2C serial interface. The device uses a 1.8-V supply for its analog and digital supplies, and a 3.3-V supply for its I/O.

The TVP5150 device converts baseband analog NTSC and PAL video into digital YUV 4:2:2 component video. Luminance/chrominance (Y/C) composite and S-video inputs are also supported. The TVP5150 device includes one 9-bit A/D converter with 2x sampling. Sampling is ITU−R BT.601 (27.0 MHz, generated off the 14.318-MHz crystal or oscillator input) and is line-locked for correct pixel alignment. The output formats can be 8-bit 4:2:2 or 8-bit ITU−R BT.656 with embedded synchronization.

The TVP5150 device utilizes Texas Instruments patented technology for locking to weak, noisy, or unstable signals. A chroma frequency control output is generated for synchronizing downstream video encoders.

Complementary 3-line or 4-line adaptive comb filtering is available for both the luma and chroma data paths to reduce both cross-luma and cross-chroma artifacts; a chroma trap filter is also available.

Video characteristics including hue, contrast, brightness, saturation, and sharpness may be programmed using the I^2C high speed serial interface. The TVP5150 device generates synchronization, blanking, field, lock, and clock signals in addition to digital video outputs. The TVP5150 device includes methods for advanced vertical blanking interval (VBI) data retrieval. The VBI data processor slices, parses, and performs error checking on Teletext, Closed Caption, and other data in several formats.

The TVP5150 device detects copy-protected input signals according to the Macrovision™ 7.1 standard.

The main blocks of the TVP5150 device include:

- A/D converter with analog processor
- Y/C separation
- Chrominance processor
- Luminance processor
- Video clock/timing processor and power-down control
- Output formatter
- I^2C interface
- VBI data processor
- Macrovision™ detection for composite and S-video

2.2 Applications

- Digital television
- PDA
- Notebook PCs
- Cell phones
- Video recorder/players
- Internet appliances/web pads
- Handheld games

2.3 Trademarks

- CompactPCI is a trademark of PICMG – PCI Industrial Computer Manufacturers Group, Inc.
- Intel is a trademark of Intel Corporation.
- TI and MicroStar BGA are trademarks of Texas Instruments
- Other trademarks are the property of their respective owners

2.4 Document Conventions

Throughout this data manual, several conventions are used to convey information. These conventions are listed below:

1. To identify a binary number or field, a lower case b follows the numbers. For example: 000b is a 3-bit binary field.
2. To identify a hexadecimal number or field, a lower case h follows the numbers. For example: 8AFh is a 12-bit hexadecimal field.
3. All other numbers that appear in this document that do not have either a b or h following the number are assumed to be decimal format.
4. If the signal or terminal name has a bar above the name (for example, $\overline{\text{RESETB}}$), then this indicates the logical NOT function. When asserted, this signal is a logic low, 0, or 0b.
5. RSVD indicates that the referenced item is reserved.

2.5 Ordering Information

T_A	PACKAGED DEVICES
	32TQFP-PBS
0°C to 70°C	TVP5150PBS

2.6 Functional Block Diagram

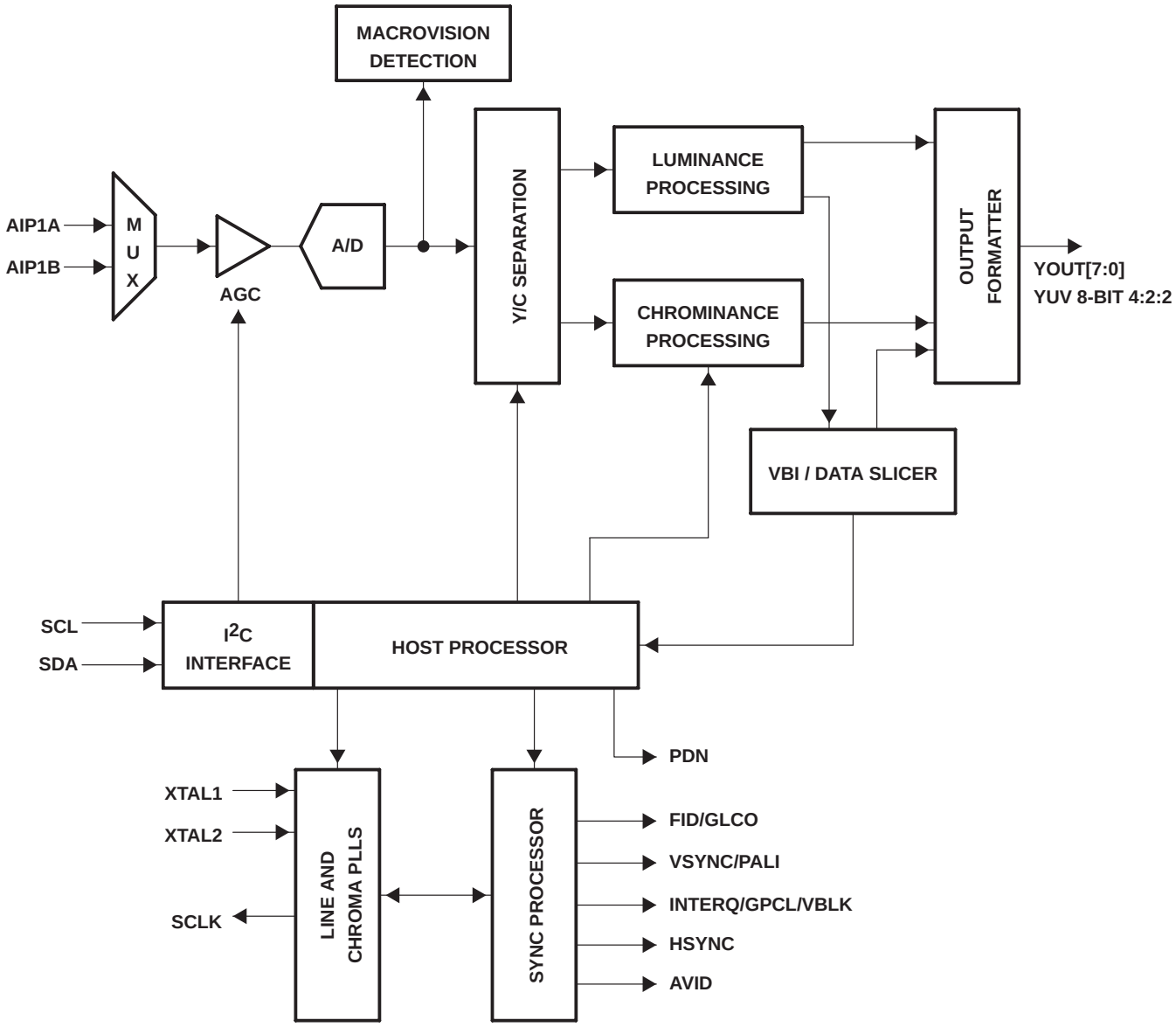


Figure 2−1. Functional Block Diagram

2.7 Terminal Assignments

The TVP5150 video decoder bridge is packaged in a 32-terminal PBS package. Figure 2−2 is the PBS-package terminal diagram. Table 2−1 gives a description of the terminals.

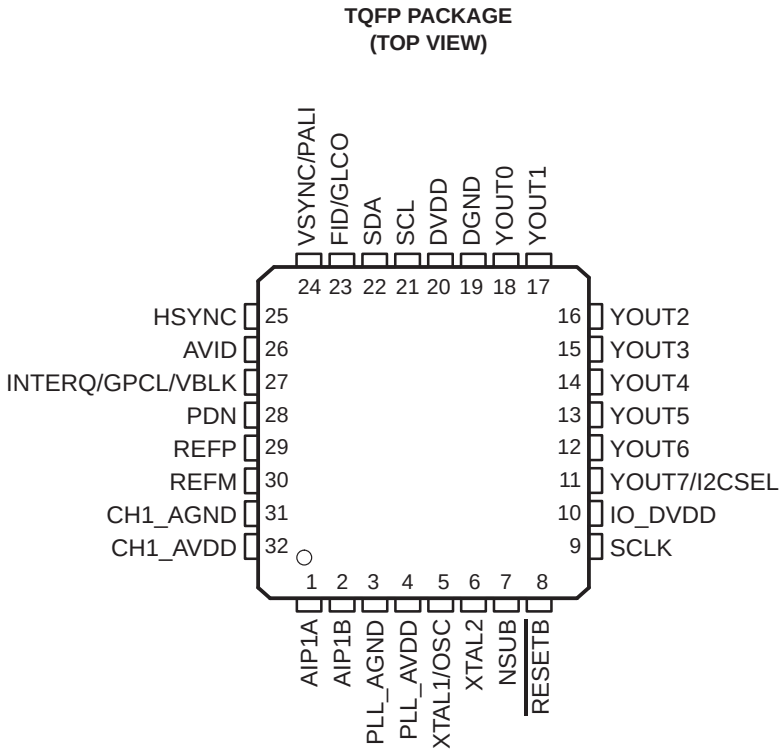


Figure 2−2. TVP5150 PBS-Package Terminal Diagram

Table 2−1. Terminal Functions

TERMINAL NAME	TERMINAL NUMBER	I/O	DESCRIPTION
Analog Section			
AIP1A	1	I	Analog input. Connect to the video analog input via 0.1-µF to 1-µF capacitor. The maximum input range is 0−0.75 V_{PP}, and may require an attenuator to reduce the input amplitude to the desired level. If not used, connect to AGND via 0.1-µF capacitor.
AIP1B	2	I	Analog input. Connect to the video analog input via 0.1-µF to 1-µF capacitor. The maximum input range is 0−0.75 V_{PP}, and may require an attenuator to reduce the input amplitude to the desired level. If not used, connect to AGND via 0.1-µF capacitor.
CH1_AGND	31	I	Analog ground
CH1_AVDD	32	I	Analog supply. Connect to 1.8-V analog supply.
NSUB	7	I	Substrate. Connect to analog ground.
PLL_AGND	3	I	PLL ground. Connect to analog ground.
PLL_AVDD	4	I	PLL supply. Connect to 1.8-V analog supply.
REFM	30	I	A/D reference ground. Connect to analog ground through 1-µF capacitor. Also recommended to connect directly to REFP through 1-µF capacitor.
REFP	29	I	A/D reference supply. Connect to analog ground through 1-µF capacitor.

Table 2−1. Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NUMBER	I/O	DESCRIPTION
Digital Section			
AVID	26	O	Active video indicator. This signal is high during the horizontal active time of the video output on the Y and UV terminals. AVID continues to toggle during vertical blanking intervals. This terminal can be placed in a high-impedance state.
DGND	19	I	Digital ground
DVDD	20	I	Digital supply. Connect to 1.8-V digital supply
FID/GLCO	23	O	FID: Odd/even field indicator or vertical lock indicator. For the odd/even indicator, a 1 indicates the odd field. GLCO: This serial output carries color PLL information. A slave device can decode the information to allow chroma frequency control from the TVP5150 device. Data is transmitted at the SCLK rate in Genlock mode. In RTC mode, SCLK/4 is used.
HSYNC	25	O	Horizontal synchronization signal
INTREQ/GPCL/ VBLK	27	I/O	INTREQ: Interrupt request output. GPCL: General-purpose control logic. This terminal has three functions: 1. General-purpose output. In this mode the state of GPCL is directly programmed via I^2C. 2. Vertical blank output. In this mode the GPCL terminal is used to indicate the vertical blanking interval of the output video. The beginning and end times of this signal are programmable via I^2C. 3. Sync lock control input. In this mode when GPCL is high, the output clock frequencies and the sync timing are forced to nominal values.
IO_DVDD	10	I	Digital supply. Connect to 3.3 V.
PDN	28	I	Power-down terminal (active low). Puts the device in standby mode. Preserves the value of the registers.
$\overline{\text{RESETB}}$	8	I	Active-low reset. $\overline{\text{RESETB}}$ can be used only when PDN = 1. When $\overline{\text{RESETB}}$ is pulled low, it resets all the registers, restarts the internal microprocessor.
SCL	21	I/O	I^2C serial clock (pullup to IO_DVDD with 1.2-kΩ resistor)
SCLK	9	O	System clock at either 1x or 2x the frequency of the pixel clock.
SDA	22	I/O	I^2C serial data (pullup to IO_DVDD with 1.2-kΩ resistor)
VSYNC/PALI	24	O	VSYNC: Vertical synchronization signal PALI: PAL line indicator or horizontal lock indicator For the PAL line indicator, a 1 indicates a noninverted line, and a 0 indicates an inverted line.
XTAL1 XTAL2	5 6	I O	External clock reference. The user may connect XTAL1 to an oscillator or to one terminal of a crystal oscillator. The user may connect XTAL2 to the other terminal of the crystal oscillator or not connect XTAL2 at all. One single 14.318-MHz crystal or oscillator is needed for ITU−R BT.601 sampling, for all supported standards.
YOUT[6:0]	12, 13, 14, 15, 16, 17, 18	I/O	Output decoded ITU−R BT.656 output/YUV 422 output with discrete sync.
YOUT(7)/I2CSEL	11	I/O	I2CSEL: Determines address for I^2C (sampled at startup). A pullup or pulldown register is needed (>1 kΩ) to program the terminal to the desired address. Logic 1: Address = 0xBA, Logic 0: Address = 0xB8 YOUT7: MSB of output decoded ITU−R BT.656 output/YUV 422 output.

3 Functional Description

3.1 Input Multiplexers and Buffers

The TVP5150 device has an analog input channel that accepts two video inputs, ac-coupled through 0.1-µF to 1-µF capacitors. The two analog input ports can be connected as follows:

- Two selectable composite video inputs or
- One S-video input

The internal video multiplexers can be configured via I^2C. The internal nodes are grounded for zero channel crosstalk. The input buffers are continuous time amplifiers that allow an input range of up to 0.75 V_{PP}. This allows the decoder to support input ranges of 0 to 1.5 V with an external attenuation of one-half.

3.2 Clamp

An internal clamping circuit restores the ac-coupled video signal to a fixed dc level. The clamping circuit provides line-by-line restoration of the video sync level to a fixed dc reference voltage. Two modes of clamping are provided, coarse and fine.

- In coarse mode, the most negative portion of the input signal (typically the sync tip) is clamped to a fixed dc level and remains on. This mode is used while the timing processor is searching for the horizontal sync.
- Fine clamp mode is enabled after the horizontal lock is achieved. This is enabled to prevent spurious level shifting caused by noise more negative than the sync tip on the input signal. If fine clamp mode is selected, then clamping is only enabled during the sync period.
  - When in bottom level mode, the sync tip of the input signal is set to output code 0 of the A/D converter (ADC).
  - When in mid-level mode, fine clamp restores the dc level of the signal to the mid-range of the ADC.

S-video requires the fine clamp mode on the chroma channel for proper operation. The clamp can be completely disabled using software registers.

3.3 Programmable Gain Amplifier and Automatic Gain Control Circuit

The programmable gain amplifier (PGA) and the automatic gain control (AGC) circuit work together to make sure that the input signal is amplified sufficiently to ensure the proper input range for the ADC. The gain is controlled by a 4-bit gain code.

Input video signal amplitude can vary significantly from the nominal level of 1 V_{PP} (140 IRE). An AGC circuit adjusts the signal amplitude to utilize the maximum range of the A/D converter without clipping. The AGC adjusts the gain to achieve the desired sync amplitude. The PGA has a range of 0 to 12 dB.

3.4 A/D Converter

The ADC has 9 bits of resolution and runs at a maximum speed of 27 MHz. The clock input for the ADC comes from the PLL. The data is aligned to the pixel clock supplied from the PLL and matched in delay. The ADC uses the REFM and REFP terminals as the internal reference generator. For configuration of these terminals, please refer to Figure 5−1.

3.5 Composite Processing Block Diagram

The composite processing block process NTSC/PAL signals into the YCbCr color space. Figure 3−1 explains the basic architecture of this processing block.

Figure 3−1 illustrates the luminance/chrominance (Y/C) separation process in the TVP5150 device. The composite video is multiplied by subcarrier signals in the quadrature modulator to generate color difference signals U and V. U and V are then low-pass filtered to achieve the desired bandwidth and to reduce crosstalk, by the color low-pass filters.

An adaptive 4-line comb filter separates UV from Y based on the unique property of color phase shift from line to line. Chroma is remodulated through another quadrature modulator and subtracted from the line-delayed composite video to generate luma. This form of Y/C separation is completely complementary and thus loses no information. However, in some applications, it is desirable to limit the U/V bandwidth to avoid crosstalk. In that case, notch filters can be turned on. To accommodate some viewing preferences, a peaking filter is also available in the luma path. Contrast, brightness, hue, saturation, and sharpness are programmable via I^2C.

The Y/C separation is bypassed for S-video input. For S-video, the remodulation path is disabled. Since Y and C are already separated at the inputs, the only requirement is to digitize them and enable the same processing as the composite signal after Y/C separation.

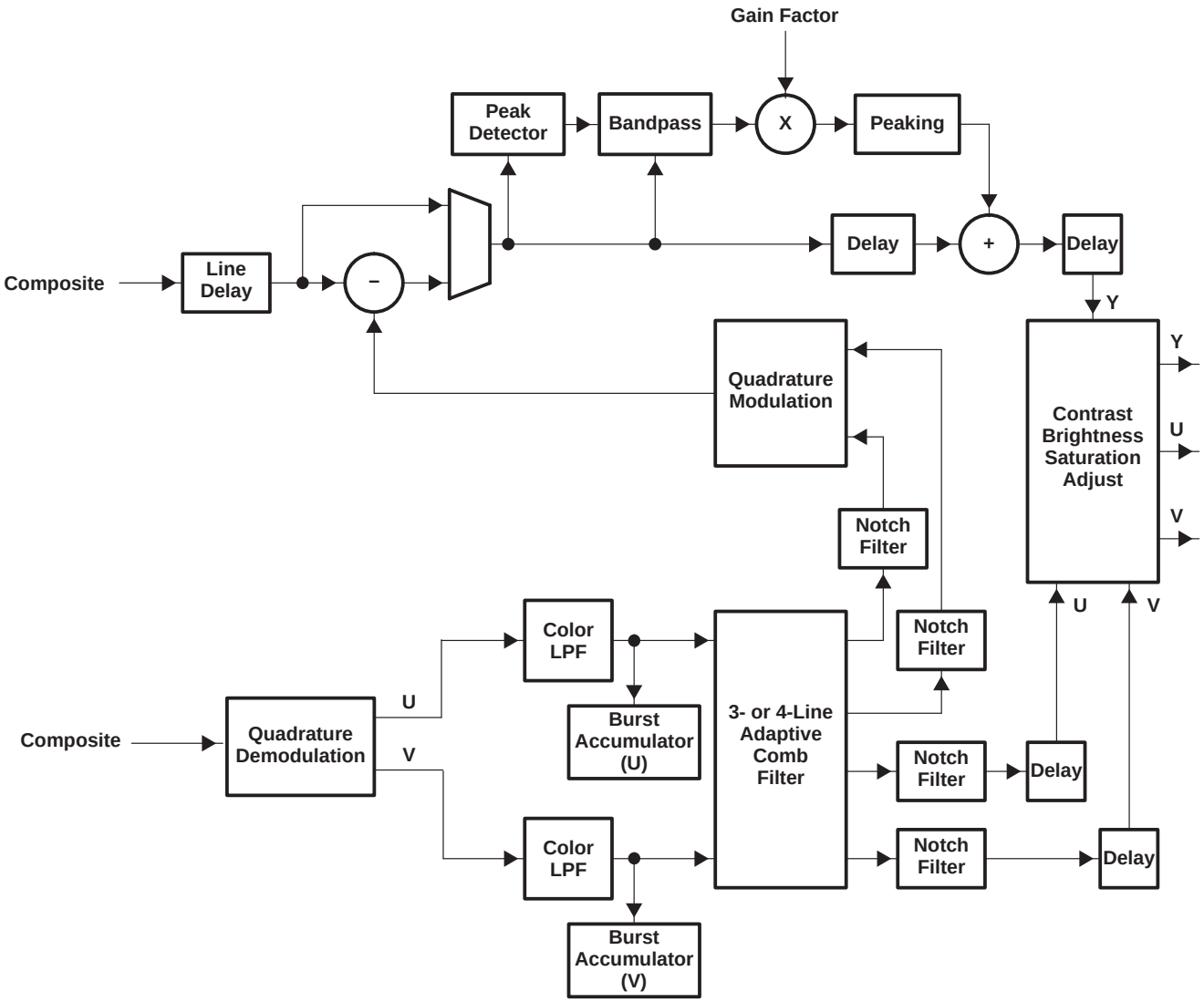


Figure 3−1. Composite Processing Block Diagram

3.6 Adaptive Comb Filtering

Y/C separation can be performed using adaptive 4-line (3-H delay), fixed 3-line, fixed 2-line comb filters, or a chroma trap filter. Characteristics of 4-line and 3-line comb filters are shown in Figure 3−2.

The filter frequency plots show that both 4-line and 3-line (with filter coefficients [1,3,3,1]/8 and [1,2,1]/4) comb filters have zeros at 1/2 of the horizontal line frequency to separate the interleaved Y/C spectrum in NTSC. The 4-line comb filter has less cross-luma and cross-chroma noise due to slightly sharper filter cutoff. The 4-line comb filter with filter coefficients [1,1,1,1]/4 has three zeros at 1/4, 2/4, and 3/4 of the horizontal line frequency. This is to be used for PAL only because of its 90° U/V phase shifting from line to line. The comb filter can be selectively bypassed in the luma or chroma path. If the comb filter is bypassed in the luma path, then chroma trap filters are used. TI's patented adaptive comb filter algorithm reduces artifacts such as hanging dots at color boundaries and detects and properly handles false colors in high frequency luminance images such as a multiburst pattern or circle pattern. Adaptive comb filtering is the recommended mode of operation. The complete comb filter selection is shown in the chrominance control #1 register (see Section 3.22.25).

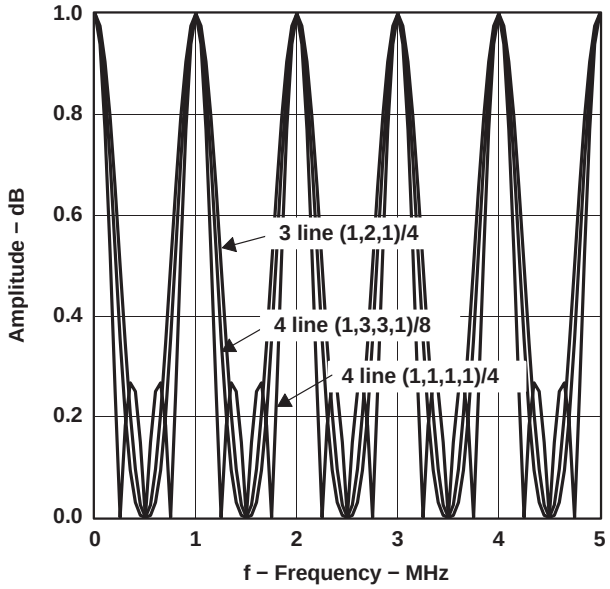


Figure 3–2. Comb Filters Frequency Response

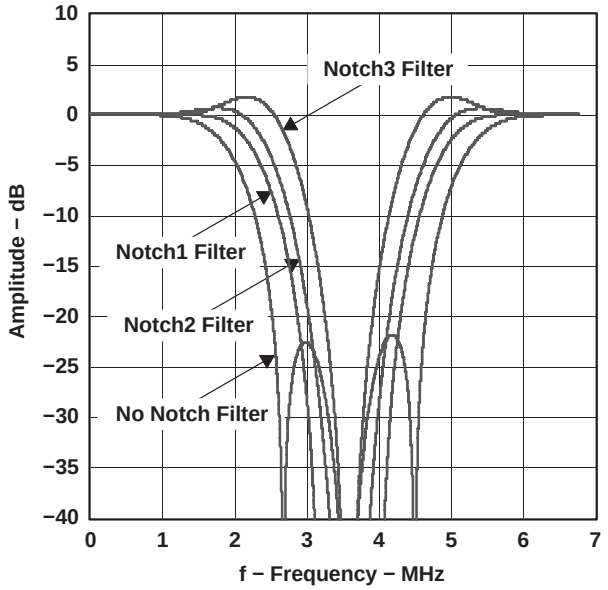


Figure 3−3. Chroma Trap Filter Frequency Response, NTSC ITU−R BT.601 Sampling

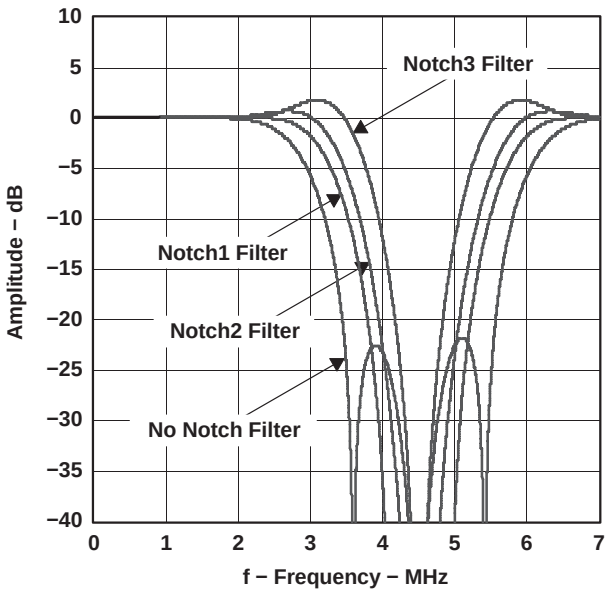


Figure 3−4. Chroma Trap Filter Frequency Response, PAL ITU−R BT.601 Sampling

3.7 Color Low-Pass Filter

In some applications, it is desirable to limit the U/V bandwidth to avoid crosstalk. This is especially true in case of nonstandard video signals that have asymmetrical U/V sidebands. In this case, notch filters are provided that limit the bandwidth of the U/V signals.

Notch filters are needed when the comb filtering turns off, due to extreme color transitions in the input image. The response of these notch filters is shown in Figure 3−5. The notch filters have three options that allow three different frequency responses based on the color frequency characteristics of the input video.

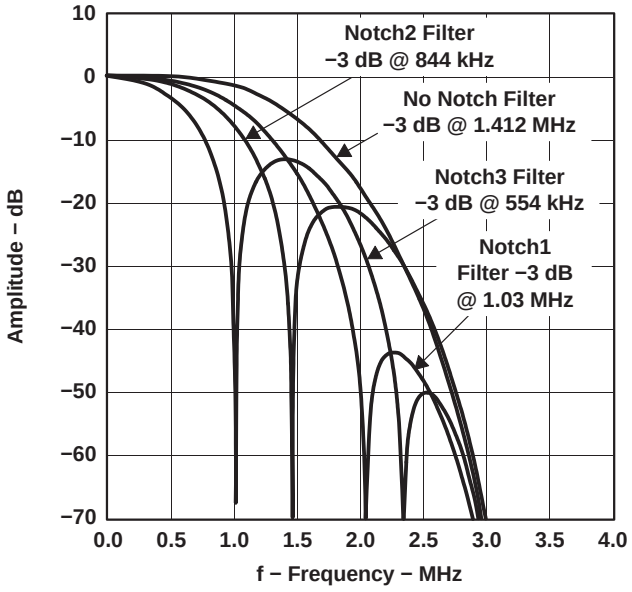


Figure 3−5. Color Low-Pass Filter With Notch Filter Characteristics, NTSC/PAL ITU−R BT.601 Sampling

3.8 Luminance Processing

The luma component is derived from the composite signal by subtracting the remodulated chroma information. A line delay exists in this path to compensate for the line delay in the adaptive comb filter in the color processing chain. The luma information is then fed into the peaking circuit, which enhances the high frequency components of the signal as shown in Figure 3−6.

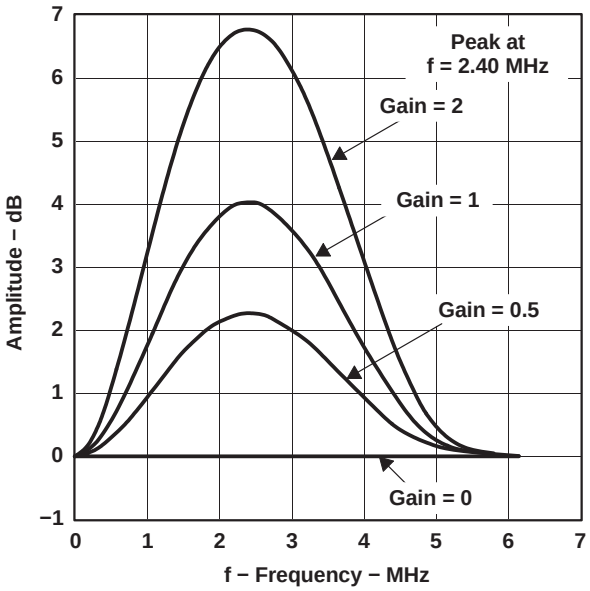


Figure 3−6. Peaking Filter Response, NTSC/PAL ITU−R BT.601 Sampling

3.9 Chrominance Processing

For PAL/NTSC formats, the color processing begins with a quadrature demodulator extracting U and V components from the composite signal. The U/V signals then pass through the gain control stage for chroma saturation adjustment. An adaptive comb filter is applied to both U and V to eliminate cross-chrominance noise. Hue control is achieved with phase shift of the digitally controlled oscillator. An automatic color killer circuit is also included in this block. The color killer suppresses the chroma processing when the color burst of the video signal is weak or not present.

3.10 Timing Processor

The timing processor is a combination of hardware and software running in the internal microprocessor that serves to control horizontal lock to the input sync pulse edge, AGC and offset adjustment in the analog front end, vertical sync detection, and Macrovision™ detection.

3.11 VBI Data Processor

The TVP5150 VBI data processor (VDP) slices various data services like Teletext (WST, NABTS), Closed Caption (CC), wide screen signaling (WSS), etc. These services are acquired by programming the VDP to enable a standard(s) in the vertical blank interval. The results are stored in a FIFO and/or registers. The Teletext results are stored in a FIFO only. Listed in Table 3−1 is a summary of the types of vertical blank interval data supported according to the video standard. It supports ITU−R BT. 601 sampling for each. Thirteen standard modes are currently supported.

Table 3−1. Data Types Supported by the VDP

LINE MODE REGISTER (D0h−FCh) BITS [3:0]	SAMPLING RATE (0Dh) BIT 7	NAME	DESCRIPTION
0000b	x	x	Reserved
0000b	x	x	Reserved
0001b	x	x	Reserved
0001b	1	WST PAL B 6	Teletext, PAL, System B, ITU−R BT.601
0010b	x	x	Reserved
0010b	1	WST PAL C 6	Teletext, PAL, System C, ITU−R BT.601
0011b	x	x	Reserved
0011b	1	WST, NTSC B 6	Teletext, NTSC, System B, ITU−R BT.601
0100b	x	x	Reserved
0100b	1	NABTS, NTSC C 6	Teletext, NTSC, System C, ITU−R BT.601
0101b	x	x	Reserved
0101b	1	NABTS, NTSC D 6	Teletext, NTSC, System D (Japan), ITU−R BT.601
0110b	x	x	Reserved
0110b	1	CC, PAL 6	Closed caption PAL, ITU−R BT.601
0111b	x	x	Reserved
0111b	1	CC, NTSC 6	Closed caption NTSC, ITU−R BT.601
1000b	x	x	Reserved
1000b	1	WSS, PAL 6	Wide-screen signal, PAL, ITU−R BT.601
1001b	x	x	Reserved
1001b	1	WSS, NTSC 6	Wide-screen signal, NTSC, ITU−R BT.601
1010b	x	x	Reserved
1010b	1	VITC, PAL 6	Vertical interval timecode, PAL, ITU−R BT.601
1011b	x	x	Reserved
1011b	1	VITC, NTSC 6	Vertical interval timecode, NTSC, ITU−R BT.601
1100b	x	x	Reserved
1100b	1	VPS, PAL 6	Video program system, PAL, ITU−R BT.601
1101b	x	x	Reserved
1110b	x	x	Reserved
1111b	x	Active Video	Active video/full field

At powerup the host interface is required to program the VDP-configuration RAM (VDP-CRAM) contents with the lookup table (see Section 3.22.54). This is done through port address C3h. Each read from or write to this address will auto increment an internal counter to the next RAM location. To access the VDP-CRAM, the line mode registers (D0h−FCh) must be programmed with FFh to avoid a conflict with the internal microprocessor and the VDP in both writing and reading. Full field mode must also be disabled.

Available VBI lines are from line 6 to line 27 of both field 1 and field 2. Each line can be any VBI mode. When changing modes, the VDP must allow the current transaction to complete through the delays of the VDP before switching the line mode register contents. It must also complete loading of the line mode registers before the next line starts processing. The switch pixel number is set through registers CBh and CCh (see Section 3.22.60).

Output data is available either through the VBI-FIFO (B0h) or through dedicated registers at 90h−AFh, both of which are available through the I^2C port.

3.12 VBI FIFO and Ancillary Data in Video Stream

Sliced VBI data can be output as ancillary data in the video stream in the ITU−R BT.656 mode. VBI data is output during the horizontal blanking period following the line from which the data was retrieved. Table 3−2 shows the header format and sequence of the ancillary data inserted into the video stream. This format is also used to store any VBI data into the FIFO. The size of FIFO is 512 bytes. Therefore, the FIFO can store up to 11 lines of teletext data with the NTSC NABTS standard.

Table 3−2. Ancillary Data Format and Sequence

BYTE NO.	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	DESCRIPTION	
0	0	0	0	0	0	0	0	0	Ancillary data preamble	
1	1	1	1	1	1	1	1	1		
2	1	1	1	1	1	1	1	1		
3	NEP	EP	0	1	0	DID2	DID1	DID0	Data ID (DID)	
4	NEP	EP	F5	F4	F3	F2	F1	F0	Secondary data ID (SDID)	
5	NEP	EP	N5	N4	N3	N2	N1	N0	Number of 32 bit data (NN)	
6	Video line # [7:0]								Internal Data ID0 (IDID0)	
7	0	0	0	Data error	Match #1	Match #2	Video line # [9:8]		Internal Data ID1 (IDID1)	
8	1. Data								Data byte	1st word
9	2. Data								Data byte	
10	3. Data								Data byte	
11	4. Data								Data byte	
:	:								:	
	m−1. Data								Data byte	Nth word
	m. Data								Data byte	
	NEP	EP	CS[5:0]						Check sum	
4(N+2)	1	0	0	0	0	0	0	0	Fill byte	

EP: Even parity for D0−D5 NEP: Negated even parity

DID: 91h: Sliced data of VBI lines of first field
53h: Sliced data of line 24 to end of first field
55h: Sliced data of VBI lines of second field
97h: Sliced data of line 24 to end of second field

SDID: This field holds the data format taken from the line mode register of the corresponding line.

NN: Number of Dwords beginning with byte 8 through 4(N+2). This value is the number of Dwords where each Dword is 4 bytes.

IDID0: Transaction video line number [7:0]

IDID1: Bit 0/1 = Transaction video line number [9:8]
Bit 2 = Match 2 flag
Bit 3 = Match 1 flag
Bit 4 = 1 if an error was detected in the EDC block. 0 if not.

CS: Sum of D0−D7 of DID through last data byte.

Fill byte: Fill bytes make a multiple of 4 bytes from byte 0 to last fill byte. For teletext modes, byte 8 is the sync pattern byte. Byte 9 is 1. Data (the first data byte).

3.13 Raw Video Data Output

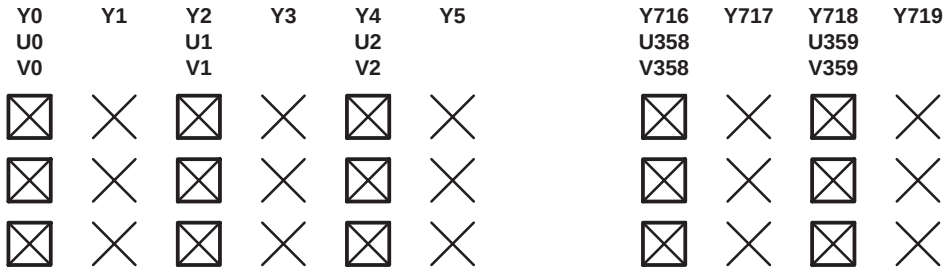
The TVP5150 device can output raw A/D video data at 2x sampling rate for external VBI slicing. This is transmitted as an ancillary data block during the active horizontal portion of the line and during vertical blanking.

3.14 Output Formatter

The YUV digital output can be programmed as 8-bit 4:2:2 or 8-bit ITU−R BT.656 parallel interface standard.

Table 3−3. Summary of Line Frequencies, Data Rates, and Pixel Counts

STANDARDS	HORIZONTAL LINE RATE (kHz)	PIXELS PER LINE	ACTIVE PIXELS PER LINE	SCLK FREQUENCY (MHz)
NTSC (M, 4.43), ITU−R BT.601	15.73426	858	720	27.00
PAL (B, D, G, H, I), ITU−R BT.601	15.625	864	720	27.00



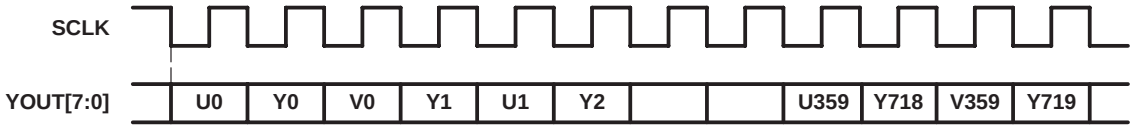
Timing is for 13.5-MHz sampling

Figure 3−7. 4:2:2 Sampling

The different formats that are supported and the corresponding sampling frequencies are listed as follows:

MODES	DATA CLOCK FREQUENCY	TERMINALS	EMBEDDED SYNCS, VBI DATA, RAW DATA	STANDARDS SUPPORTED
8-bit ITU−R BT.601	SCLK	Y(7−0) YCbCr	Syncs optional VBI optional (edge prog) Raw data optional	NTSC/PAL YUV output
8-bit 4:2:2	SCLK	Y(7−0) YCbCr	Syncs optional VBI optional (edge prog) Raw data optional	Any standard YUV output

The following diagram explains the different modes.



Numbering shown is for 13.5-MHz sampling

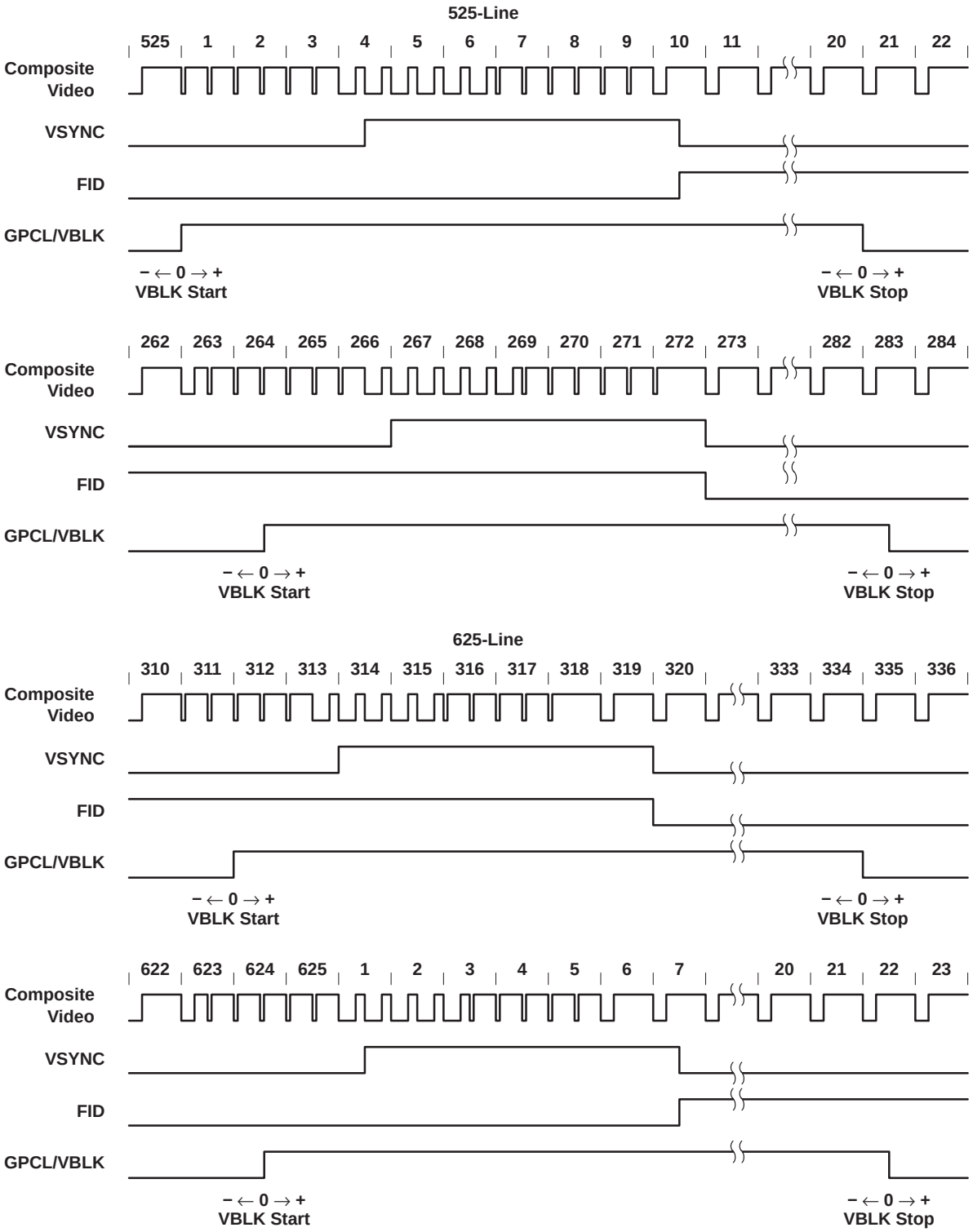
Figure 3−8. 8-Bit YCbCr 4:2:2 and ITU−R BT.656 Mode Timing

3.15 Synchronization Signals

Nondata stream embedded syncs are provided via the following signals:

- VSYNC (vertical sync)
- FID/VLK (field indicator or vertical lock indicator)
- GPCL/VBLK (general-purpose I/O or vertical blanking indicator)
- PALI/HLK (PAL switch indicator or horizontal lock indicator)
- HSYNC (horizontal sync)
- AVID (active video indicator)

In hardware, VSYNC, FID, PALI, and VBLK are software-set and programmable to the SCLK pixel count. This allows any possible alignment to the internal pixel count and line count. The proper settings for a 525-/625-line video output are given as an example below.

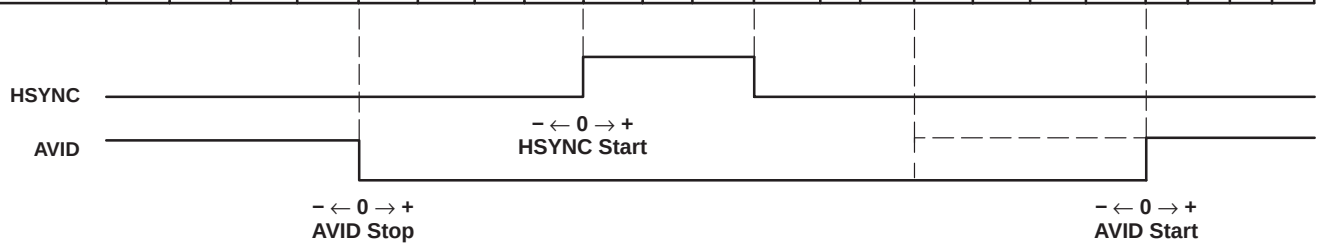


Notes: 1. Line numbering conforms to ITU−R BT.470

Figure 3−9. 8-bit 4:2:2, Timing With 2x Pixel Clock (SCLK) Reference

ITU−R BT.656 timing shown without embedded syncs.

NTSC 601	**1436**	**1437**	**1438**	**1439**	**1440**	**1441**	…	**1455**	**1456**	…	**1583**	**1584**	⋯	**1711**	**1712**	**1713**	**1714**	**1715**	**0**	**1**	**2**	**3**
PAL 601	**1436**	**1437**	**1438**	**1439**	**1440**	**1441**	…	**1459**	**1460**	…	**1587**	**1588**	⋯	**1723**	**1724**	**1725**	**1726**	**1727**	**0**	**1**	**2**	**3**
ITU 656 Datastream	**Cb 359**	**Y 718**	**Cr 359**	**Y 719**	**FF**	**00**	…	**10**	**80**	…	**10**	**80**	⋯	**10**	**FF**	**00**	**00**	**XX**	**Cb 0**	**Y 0**	**Cr 0**	**Y 1**



NOTE: AVID rising edge occurs 4 SCLK cycles early when in ITU−R BT.656 output mode.

Figure 3−10. Horizontal Synchronization Signals

3.16 AVID Cropping

AVID or active video cropping provides a means to decrease bandwidth of the video output. This is accomplished by horizontally blanking a number of AVID pulses and by vertically blanking a number of lines per frame. The horizontal AVID cropping is controlled using registers 11h and 12h for start pixels MSB and LSB, respectively.

Registers 13h and 14h provide access to stop pixels MSB and LSB, respectively. The vertical AVID cropping is controlled using the vertical blanking (VBLK) start and stop registers at addresses 18h and 19h. Figure 3−11 shows an AVID application.

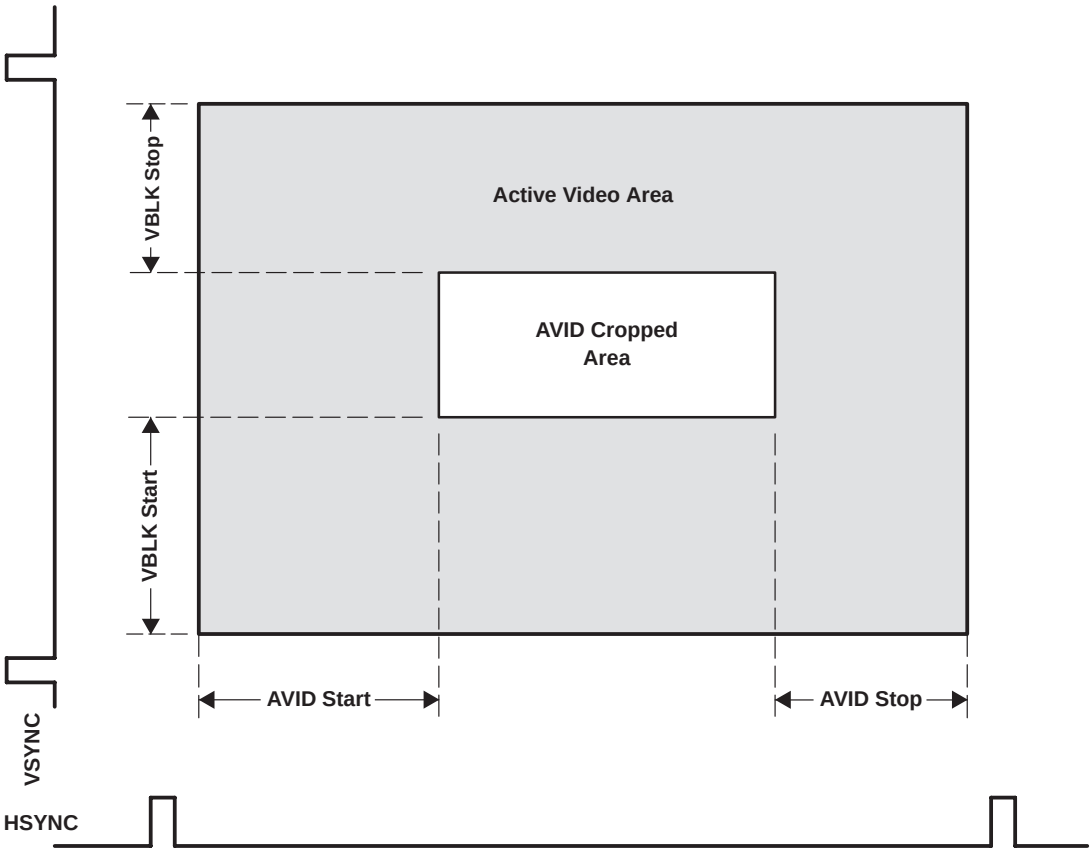


Figure 3−11. AVID Application

3.17 Embedded Syncs

Standards with embedded syncs insert SAV and EAV codes into the datastream on the rising and falling edges of AVID. These codes contain the V and F bits which also define vertical timing. F and V are software programmable and change after SAV but before EAV, so that the new value always appears on EAV first. Table 3−4 gives the format of the SAV and EAV codes.

H equals 1 always indicates EAV. H equals 0 always indicates SAV. The alignment of V and F to the line and field counter varies depending on the standard.

The P bits are protection bits:

P3 = V xor H
P2 = F xor H
P1 = F xor V
P0 = F xor V xor H

Table 3−4. EAV and SAV Sequence

	8-BIT DATA							
	D7 (MSB)	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Preamble	1	1	1	1	1	1	1	1
Preamble	0	0	0	0	0	0	0	0
Preamble	0	0	0	0	0	0	0	0
Status word	1	F	V	H	P3	P2	P1	P0

3.18 I²C Host Interface

The I²C standard consists of two signals, serial input/output data line (SDA) and input/output clock line (SCL), which carry information between the devices connected to the bus. A third signal (I2CSEL) is used for slave address selection. Although the I²C system can be multimastered, the TVP5150 device functions as a slave device only.

Both SDA and SCL must be connected to a positive supply voltage via a pullup resistor. When the bus is free, both lines are high. The slave address select terminal (I2CSEL) enables the use of two TVP5150 devices tied to the same I²C bus. At power up, the status of the I2CSEL is polled. Depending on the write and read addresses to be used for the TVP5150 device, it can either pulled low or high through a resistor. This terminal is multiplexed with YOUT7 and hence must not be tied directly to ground or V_{DD}. Table 3−6 summarizes the terminal functions of the I²C-mode host interface.

Table 3−5. Write Address Selection

I2CSEL	WRITE ADDRESS
0	B8h
1	BAh

Table 3−6. I²C Terminal Description

SIGNAL	TYPE	DESCRIPTION
I2CSEL (YOUT7)	I	Slave address selection
SCL	I/O (open drain)	Input/output clock line
SDA	I/O (open drain)	Input/output data line

Data transfer rate on the bus is up to 400 kbits/s. The number of interfaces connected to the bus is dependent on the bus capacitance limit of 400 pF. The data on the SDA line must be stable during the high period of the SCL except for start and stop conditions. The high or low state of the data line can only change with the clock signal on the SCL line being low. A high-to-low transition on the SDA line while the SCL is high indicates an I²C start condition. A low-to-high transition on the SDA line while the SCL is high indicates an I²C stop condition.

Every byte placed on the SDA must be 8 bits long. The number of bytes which can be transferred is unrestricted. Each byte must be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the I²C master.

3.18.1 I²C Write Operation

Data transfers occur utilizing the following illustrated formats.

An I²C master initiates a write operation to the TVP5150 device by generating a start condition (S) followed by the TVP5150 I²C address (as shown below), in MSB first bit order, followed by a 0 to indicate a write cycle. After receiving an acknowledge from the TVP5150 device, the master presents the subaddress of the register, or the first of a block of registers it wants to write, followed by one or more bytes of data, MSB first. The TVP5150 device acknowledges each byte after completion of each transfer. The I²C master terminates the write operation by generating a stop condition (P).

Step 1	**0**
I²C Start (master)	S

Step 2	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C General address (master)	1	0	1	1	1	0	X	0

Step 3	**9**
I²C Acknowledge (slave)	A

Step 4	7	6	5	4	3	2	1	0
I2C Write register address (master)	addr	addr	addr	addr	addr	addr	addr	addr

Step 5	9
I2C Acknowledge (slave)	A

Step 6	7	6	5	4	3	2	1	0
I2C Write data (master)	Data	Data	Data	Data	Data	Data	Data	Data

Step 7†	9
I2C Acknowledge (slave)	A

Step 8	0
I2C Stop (master)	P

† Repeat steps 6 and 7 until all data have been written.

3.18.2 I2C Read Operation

The read operation consists of two phases. The first phase is the address phase. In this phase, an I2C master initiates a write operation to the TVP5150 device by generating a start condition (S) followed by the TVP5150 I2C address, in MSB first bit order, followed by a 0 to indicate a write cycle. After receiving acknowledges from the TVP5150 device, the master presents the subaddress of the register or the first of a block of registers it wants to read. After the cycle is acknowledged, the master terminates the cycle immediately by generating a stop condition (P).

Table 3−7. Read Address Selection

I2CSEL	READ ADDRESS
0	B9h
1	BBh

The second phase is the data phase. In this phase, an I2C master initiates a read operation to the TVP5150 device by generating a start condition followed by the TVP5150 I2C address (as shown below for a read operation), in MSB first bit order, followed by a 1 to indicate a read cycle. After an acknowledge from the TVP5150 device, the I2C master receives one or more bytes of data from the TVP5150 device. The I2C master acknowledges the transfer at the end of each byte. After the last data byte desired has been transferred from the TVP5150 device to the master, the master generates a not acknowledge followed by a stop.

3.18.2.1 Read Phase 1

Step 1	0
I2C Start (master)	S

Step 2	7	6	5	4	3	2	1	0
I2C General address (master)	1	0	1	1	1	0	X	0

Step 3	9
I2C Acknowledge (slave)	A

Step 4	7	6	5	4	3	2	1	0
I2C Read register address (master)	addr	addr	addr	addr	addr	addr	addr	addr

Step 5	9
I2C Acknowledge (slave)	A

Step 6	0
I2C Stop (master)	P

3.18.2.2 Read Phase 2

Step 7	0
I2C Start (master)	S

Step 8	7	6	5	4	3	2	1	0
I2C General address (master)	1	0	1	1	1	0	X	1

Step 9	9
I2C Acknowledge (slave)	A

Step 10	7	6	5	4	3	2	1	0
I2C Read data (slave)	Data	Data	Data	Data	Data	Data	Data	Data

Step 11†	9
I2C Not Acknowledge (master)	$\overline{A}$

Step 12	0
I2C Stop (master)	P

† Repeat steps 10 and 11 for all bytes read. Master does not acknowledge the last read data received.

3.18.2.3 I2C Timing Requirements

The TVP5150 device requires delays in the I2C accesses to accommodate its internal processor's timing. In accordance with I2C specifications, the TVP5150 device holds the I2C clock line (SCL) low to indicate the wait period to the I2C master. If the I2C master is not designed to check for the I2C clock line held-low condition, then the maximum delays must always be inserted where required. These delays are of variable length; maximum delays are indicated in the following diagram:

Normal register writing address 00h−8Fh (addresses 90h−FFh do not require delays)

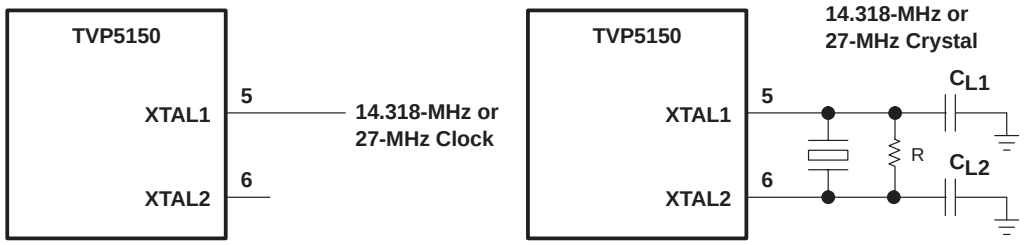
Start	Slave address (B8h)	Ack	Subaddress	Ack	Data (XXh)	Ack	Wait 64 µs	Stop

3.19 Clock Circuits

An internal line-locked phase-locked loop (PLL) generates the system and pixel clocks. The PLL minimizes jitter and process and environmental variability. It is capable of operating off a single crystal frequency with a high supply rejection ratio. A 14.318-MHz clock is required to drive the PLL. This may be input to the TVP5150 device on terminal 5 (XTAL1), or a crystal of 14.318-MHz fundamental resonant frequency may be connected across terminals 5 and 6 (XTAL2). Figure 3−12 shows the reference clock configurations. For the example crystal circuit shown (a parallel-resonant crystal with 14.318-MHz fundamental frequency), the external capacitors must have the following relationship:

$C_{L1} = C_{L2} = 2C_L - C_{STRAY}$,

where C_{STRAY} is the terminal capacitance with respect to ground. Please note that with the crystal oscillator, an external 100-kΩ resistor can be optionally put across XTAL1 and XTAL2 terminals. Figure 3−12 shows the reference clock configurations.



NOTE: 100-kΩ resistor R is optional

Figure 3−12. Reference Clock Configurations

3.20 Genlock Control (GLCO) and Real-Time Control (RTC)

A Genlock control function is provided to support a standard video encoder to synchronize its internal color phase DCO for a clean video line and color lock.

The frequency control word of the internal color subcarrier digital control oscillator (DCO) and the subcarrier phase reset bit are transmitted via terminal 23 (GLCO). The frequency control word is a 23-bit binary number. The frequency of the DCO can be calculated from the following equation:

$$F_{dco} = \frac{F_{ctrl}}{2^{23}} \times F_{sclk}$$

where F_{dco} is the frequency of the DCO, F_{ctrl} is the 23-bit DCO frequency control, and F_{sclk} is the frequency of the SCLK.

3.20.1 TVP5150 Genlock Control Interface

A write of 1 to bit 4 of the chrominance control register at I^2C subaddress 1Ah causes the subcarrier DTO phase reset bit to be sent on the next scan line on GLCO. The active low reset bit occurs 7 SCLKs after the transmission of the last bit of DCO frequency control. Upon the transmission of the reset bit, the phase of the TVP5150 internal subcarrier DCO is reset to zero.

A Genlock slave device can be connected to the GLCO terminal and use the information on GLCO to synchronize its internal color phase DCO to achieve clean line and color lock.

Figure 3−13 shows the timing diagram of the GLCO mode.

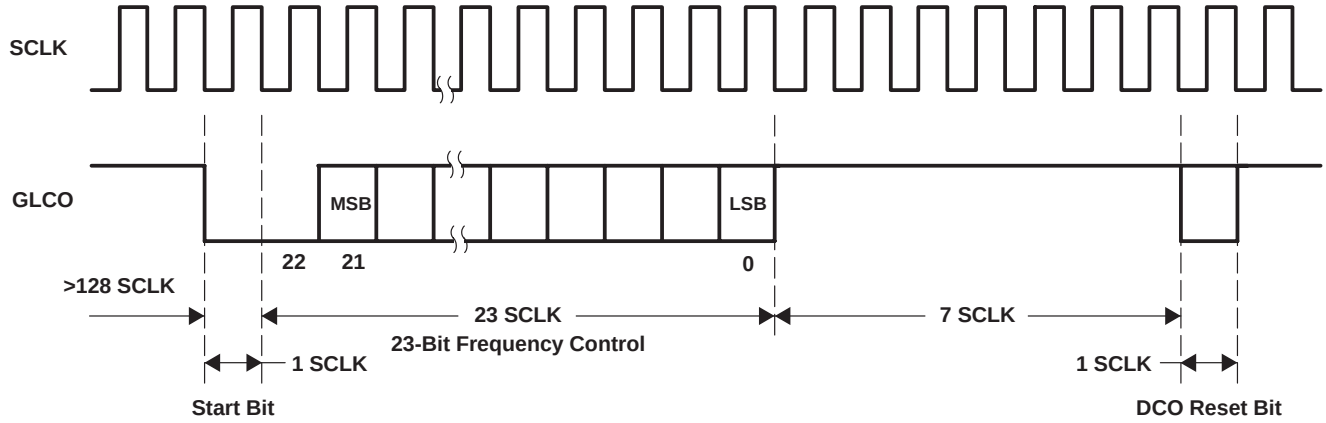


Figure 3−13. GLCO Timing

3.20.2 RTC Mode

Figure 3−14 shows the timing diagram of the RTC mode. Clock rate for the RTC mode is 4 times slower than the GLCO clock rate. For PLL frequency control, the upper 22 bits are used. Each frequency control bit is 2 clock cycles long. The active low reset bit occurs 6 CLKs after the transmission of the last bit of PLL frequency control.

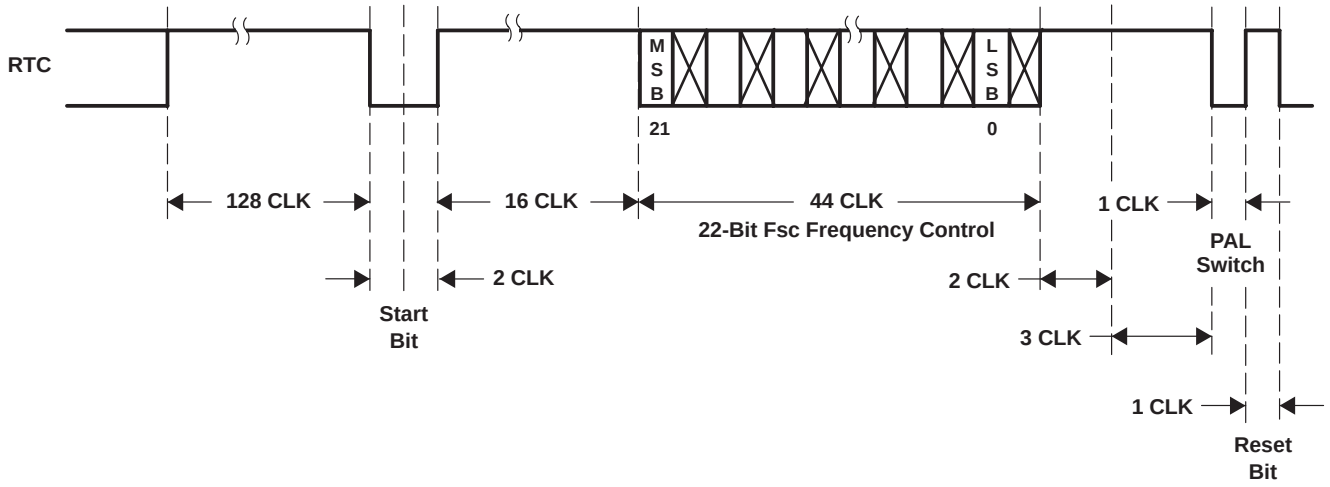


Figure 3−14. RTC Timing

3.21 Internal Control Registers

The TVP5150 device is initialized and controlled by a set of internal registers which set all device operating parameters. Communication between the external controller and the TVP5150 device is through I^2C. Table 3−8 shows the summary of these registers. The reserved registers must not be written. However, reserved bits in the defined registers must be written with 0s. The detailed programming information of each register is described in the following sections.

Table 3−8. Registers Summary

REGISTER FUNCTION	ADDRESS	DEFAULT	R/W
Video input source selection #1	00h	00h	R/W
Analog channel controls	01h	15h	R/W
Operation mode controls	02h	00h	R/W
Miscellaneous controls	03h	01h	R/W
Autoswitch mask	04h	00h	R/W
Software reset	05h	00h	R/W
Color killer threshold control	06h	10h	R/W
Luminance processing control #1	07h	20h	R/W
Luminance processing control #2	08h	00h	R/W
Brightness control	09h	80h	R/W
Color saturation control	0Ah	80h	R/W
Hue control	0Bh	00h	R/W
Contrast control	0Ch	80h	R/W
Outputs and data rates select	0Dh	47h	R/W

R = Read only
W = Write only
R/W = Read and write

Table 3−8. Registers Summary (Continued)

REGISTER FUNCTION	ADDRESS	DEFAULT	R/W
Luminance processing control #3	0Eh	00h	R/W
Configuration shared pins	0Fh	08h	R/W
Reserved	10h		
Active video cropping start MSB	11h	00h	R/W
Active video cropping start LSB	12h	00h	R/W
Active video cropping stop MSB	13h	00h	R/W
Active video cropping stop LSB	14h	00h	R/W
Genlock/RTC	15h	01h	R/W
Horizontal sync start	16h	80h	R/W
Reserved	17h		
Vertical blanking start	18h	00h	R/W
Vertical blanking stop	19h	00h	R/W
Chrominance processing control #1	1Ah	0Ch	R/W
Chrominance processing control #2	1Bh	14h	R/W
Interrupt reset register B	1Ch	00h	R/W
Interrupt enable register B	1Dh	00h	R/W
Interrupt configuration register B	1Eh	00h	R/W
Reserved	1Fh−27h		
Video standard	28h	00h	R/W
Reserved	29h–7Fh		
MSB of device ID	80h	51h	R
LSB of device ID	81h	50h	R
ROM version	82h	02h	R
RAM patch-code version	83h	10h	R
Vertical line count MSB	84h		R
Vertical line count LSB	85h		R
Interrupt status register B	86h		R
Interrupt active register B	87h	00h	R
Status register #1	88h		R
Status register #2	89h		R
Status register #3	8Ah		R
Status register #4	8Bh		R
Status register #5	8Ch		R
Reserved	8Dh−8Fh		
Closed caption data registers	90h−93h		R
WSS data registers	94h−99h		R
VPS data registers	9Ah−A6h		R
VITC data registers	A7h−AFh		R
VBI FIFO read data	B0h		R
Teletext filter 1	B1h−B5h	00h	R/W
Teletext filter 2	B6h−BAh	00h	R/W

R = Read only
W = Write only
R/W = Read and write

Table 3−8. Registers Summary (Continued)

REGISTER FUNCTION	ADDRESS	DEFAULT	R/W
Teletext filter enable	BBh	00h	R/W
Reserved	BCh−BFh		
Interrupt status register A	C0h	00h	R/W
Interrupt enable register A	C1h	00h	R/W
Interrupt configuration	C2h	04h	R/W
VDP configuration RAM data	C3h	DCh	R/W
Configuration RAM address low byte	C4h	0Fh	R/W
Configuration RAM address high byte	C5h	00h	R/W
VDP status register	C6h		R/W
FIFO word count	C7h		R
FIFO interrupt threshold	C8h	80h	R/W
FIFO reset	C9h	00h	W
Line number interrupt	CAh	00h	R/W
Pixel alignment register low byte	CBh	59h	R/W
Pixel alignment register high byte	CCh	03h	R/W
FIFO output control	CDh	01h	R/W
Automatic initialization	CEh	00h	R/W
Full field enable	CFh	00h	R/W
Line mode registers	D0h−FBh	FFh	R/W
Full field mode register	FCh	7Fh	R/W
Reserved	FDh−FFh		

R = Read only
W = Write only
R/W = Read and write

3.22 Register Definitions

3.22.1 Video Input Source Selection #1 Register

Address	00h

7	6	5	4	3	2	1	0
Reserved						Channel 1 source selection	S-video selection

Channel 1 source selection:

0 = AIP1A selected (default)
1 = AIP1B selected

Table 3−9. Analog Channel and Video Mode Selection

	INPUT(S) SELECTED	ADDRESS 00	
		BIT 1	BIT 0
Composite	AIP1A (default)	0	0
	AIP1B	1	0
S-Video	1A luma, 2A chroma	x	1

3.22.2 Analog Channel Controls Register

Address	01h

7	6	5	4	3	2	1	0
Reserved			1	Automatic offset control		Automatic gain control	

Automatic offset control:

00 = Disabled
01 = Automatic offset enabled (default)
10 = Reserved
11 = Clamping level frozen to the previously set value

Automatic gain control (AGC):

00 = Disabled (fixed gain value)
01 = AGC enabled (default)
10 = Reserved
11 = AGC frozen to the previously set value

3.22.3 Operation Mode Controls Register

Address	02h

7	6	5	4	3	2	1	0
Reserved					Color subcarrier PLL frozen	Reserved	Power down mode

Color subcarrier PLL frozen:

0 = Color subcarrier PLL increments by the internally generated phase increment. (default)
GLCO pin outputs the frequency increment.
1 = Color subcarrier PLL stops operating.
GLCO pin outputs the frozen frequency increment.

Power down mode:

0 = Normal operation (default)
1 = Power down mode. A/Ds are turned off and internal clocks are reduced to minimum.

3.22.4 Miscellaneous Control Register

Address	03h

7	6	5	4	3	2	1	0
VBKO	GPCL pin	GPCL I/O mode select	Lock status (HVLK)	YUV output enable (TVPOE)	HSYNC, VSYNC/PALI, AVID, FID/GLCO output enable	Vertical blanking on/off	Clock output enable

VBKO (pin 27) function select:

0 = GPCL (default)
1 = VBLK

GPCL (data is output based on state of bit 5):

0 = GPCL outputs 0 (default)
1 = GPCL outputs 1

GPCL I/O mode select:

0 = GPCL is input (default)
1 = GPCL is output

Lock status (HVLK) (configured along with register 0Fh):

0 = Terminal VSYNC/PALI outputs. PAL indicator (PALI) signal and terminal FID/GLCO outputs field ID (FID) signal (default) (if terminals are configured to output PALI and FID in register 0Fh)
1 = Terminal VSYNC/PALI outputs horizontal lock indicator (HLK) and terminal FID outputs vertical lock indicator (VLK) (if terminals are configured to output PALI and FID in register 0Fh)

These are additional functionalities that are provided for ease of use.

YUV output enable:

0 = Y(OUT7:0) high impedance (default)
1 = Y(OUT7:0) active

HSYNC, VSYNC/PALI, active video indicator (AVID), and FID/GLCO output enables:

0 = HSYNC, VSYNC/PALI, AVID, and FID/GLCO are high-impedance (default).
1 = HSYNC, VSYNC/PALI, AVID, and FID/GLCO are active.

Vertical blanking on/off:

0 = Vertical blanking (VBLK) off (default)
1 = Vertical blanking (VBLK) on

Clock output enable:

0 = SCLK output is high impedance.
1 = SCLK output is enabled (default).

Table 3−10. Digital Output Control

Terminal 28 (AVID)	Register 03h, Bit 3 (TVPOE)	Register C2h, Bit 2 (VDPOE)	YUV Output	Notes
1 during reset	X	X	Active after reset	After reset and before YUV output enable bits are programmed. TVPOE defaults to 1 and VDPOE is 1.
0 during reset	X	X	High impedance after reset	After reset and before YUV output enable bits are programmed. TVPOE defaults to 0 and VDPOE is 1.
X	0	X	High impedance	After both YUV output enable bits are programmed.
X	X	0	High impedance	After both YUV output enable bits are programmed.
X	1	1	Active	After both YUV output enable bits are programmed.

3.22.5 Autoswitch Mask Register

Address	04h

7	6	5	4	3	2	1	0
Reserved			N443_OFF	PALN_OFF	PALM_OFF	Reserved	

N443_OFF:

0 = NTSC443 is masked from the autoswitch process. Autoswitch does not switch to NTSC443.
1 = Normal operation (default)

PALN_OFF:

0 = PAL-N is masked from the autoswitch process. Autoswitch does not switch to PAL-N.
1 = Normal operation (default)

PALM_OFF:

0 = PAL-M is masked from the autoswitch process. Autoswitch does not switch to PAL-M.
1 = Normal operation (default)

3.22.6 Software Reset Register

Address	05h

7	6	5	4	3	2	1	0
Reserved							Reset

Reset:

0 = Normal operation (default)
1 = Reset device

3.22.7 Color Killer Threshold Control Register

Address	06h

7	6	5	4	3	2	1	0
Reserved	Automatic color killer		Color killer threshold				

Automatic color killer:

00 = Automatic mode (default)
01 = Reserved
10 = Color killer enabled, the UV terminals are forced to a zero color state.
11 = Color killer disabled

Color killer threshold:

11111 = −30 dB (minimum)
10000 = −24 dB (default)
00000 = −18 dB (maximum)

3.22.8 Luminance Processing Control #1 Register

Address	07h

7	6	5	4	3	2	1	0
Luma bypass mode	Pedestal not present	Disable raw header	Luma bypass during vertical blank	Luminance signal delay with respect to chrominance signal			

Luma bypass mode:

0 = Input video bypasses the chroma trap and comb filters. Chroma outputs are forced to zero (default).
1 = Input video bypasses the whole luma processing. Raw A/D data is output alternatively as UV data and Y data at SCLK rate. The output data is properly clipped to comply to ITU−R BT.601 coding range. Only valid for 8-bit YUV output format (YUV output format = 100 or 111 at register 0Dh).

Pedestal not present:

0 = 7.5 IRE pedestal is present on the analog video input signal (default).
1 = Pedestal is not present on the analog video input signal.

Disable raw header:

0 = Insert 656 ancillary headers for raw data.
1 = Disable 656 ancillary headers and instead force dummy ones (0x40) (default).

Luminance bypass enabled during vertical blanking:

0 = Disabled (default)
1 = Enabled

Luminance bypass occurs for the duration of the vertical blanking as defined by registers 18h and 19h. This feature may be used to prevent distortion of test and data signals present during the vertical blanking interval.

Luma signal delay with respect to chroma signal in pixel clock increments (range −8 to +7 pixel clocks):

1111 = −8 pixel clocks delay
1011 = −4 pixel clocks delay
1000 = −1 pixel clocks delay
0000 = 0 pixel clocks delay (default)
0011 = 3 pixel clocks delay
0111 = 7 pixel clocks delay

3.22.9 Luminance Processing Control #2 Register

Address	08h

7	6	5	4	3	2	1	0
Reserved	Luminance filter select	Reserved		Peaking gain		Reserved	

Luminance filter select:

0 = Luminance comb filter enabled (default)
1 = Luminance chroma trap filter enabled

Peaking gain:

00 = 0 (default)
01 = 0.5
10 = 1
11 = 2

Information on peaking frequency: ITU−R BT.601 sampling rate: all standards—2.6 MHz

3.22.10 Brightness Control Register

Address	09h

7	6	5	4	3	2	1	0
Brightness control							

Brightness control:

1111 1111 = 255 (bright)
1000 1011 = 139 (ITU−R BT.601 level)
1000 0000 = 128 (default)
0000 0000 = 0 (dark)

3.22.11 Color Saturation Control Register

Address	0Ah

7	6	5	4	3	2	1	0
Saturation control							

Saturation control:

1111 1111 = 255 (maximum)
1000 0000 = 128 (default)
0000 0000 = 0 (no color)

3.22.12 Hue Control Register

Address	0Bh

7	6	5	4	3	2	1	0
Hue control							

Hue control:

0111 1111 = +180 degrees
0000 0000 = 0 degrees (default)
1000 0000 = −180 degrees

3.22.13 Contrast Control Register

Address	0Ch

7	6	5	4	3	2	1	0
Contrast control							

Contrast control:

1111 1111 = 255 (maximum contrast)
1000 0000 = 128 (default)
0000 0000 = 0 (minimum contrast)

3.22.14 Outputs and Data Rates Select Register

Address	0Dh

7	6	5	4	3	2	1	0
Reserved	YUV output code range	UV code format	YUV data path bypass		YUV output format		

YUV output code range:

0 = ITU−R BT.601 coding range (Y ranges from 16 to 235. U and V range from 16 to 240)
1 = Extended coding range (Y, U, and V range from 1 to 254) (default)

UV code format:

0 = Offset binary code (2s complement + 128) (default)
1 = Straight binary code (2s complement)

YUV data path bypass:

00 = Normal operation (default)
01 = Digital composite output pins connected to decimation filter output, decoder function bypassed, data output alternately as Y and UV buses at the SCLK rate.
10 = YUV output pins connected to A/D output, decoder function bypassed, data output at SCLK rate.
11 = Reserved

YUV output format:

000 = 8-bit 4:2:2 YUV with discrete sync output
001 = Reserved
010 = Reserved
011 = Reserved
100 = Reserved
101 = Reserved
110 = Reserved
111 = 8-bit ITU−R BT.656 interface with embedded sync output (default)

3.22.15 Luminance Processing Control #3 Register

Address	0Eh

7	6	5	4	3	2	1	0
Reserved						Luminance trap filter select	

Luminance filter stop band bandwidth (MHz):

00 = No notch (default)
01 = Notch 1
10 = Notch 2
11 = Notch 3

Luminance filter select [1:0] selects one of the four chroma trap filters to produce luminance signal by removing the chrominance signal from the composite video signal. The stopband of the chroma trap filter is centered at the chroma subcarrier frequency with stopband bandwidth controlled by the two control bits. Please refer to Figure 3−5, for the frequency responses of the filters.

3.22.16 Configuration Shared Pins

Address	0Fh

7	6	5	4	3	2	1	0
Reserved	LOCK23	LOCK24A	LOCK24B	FID/GLCO	VSYNC/PALI	INTREQ/GPCL/VBLK	SCLK/PCLK

LOCK23 (pin 23) function select:

0 = FID (default, if bit 3 is selected to output FID)
1 = Lock indicator (Indicates whether device is locked both horizontally and vertically)

LOCK24A (pin 24) function select:

0 = VSYNC (default, if bit 2 is selected to output VSYNC)
1 = Lock indicator (Indicates whether device is locked both horizontally and vertically)

LOCK24B (pin 24) function select:

0 = PALI (default, if bit 2 is selected to output PALI)
1 = Lock indicator (Indicates whether device is locked both horizontally and vertically)

FID/GLCO (pin 23) function select (also refer to register 03h for enhanced functionality):

0 = FID
1 = GLCO (default)

VSYNC/PALI (pin 24) function select (also refer to register 03h for enhanced functionality):

0 = VSYNC (default)
1 = PALI

INTREQ/GPCL/VBLK (pin 27) function select:

0 = INTREQ (default)
1 = GPCL or VBLK depending on bit 7 of register 03h

SCLK/PCLK (pin 9) function select:

0 = SCLK (default)
1 = PCLK (1x pixel clock frequency)

3.22.17 Active Video Cropping Start Pixel MSB

Address	11h

7	6	5	4	3	2	1	0
AVIDST_MSB [9:2]							

Active video cropping start pixel MSB [9:2], set this register first before setting register 12h. The TVP5150 device updates the AVID start values only when register 12h is written to.

3.22.18 Active Video Cropping Start Pixel LSB

Address	12h

7	6	5	4	3	2	1	0
Reserved					AVID active	AVIDST_LSB [1:0]	

AVID active:

0 = AVID out active in VBLK (default)
1 = AVID out inactive in VBLK

Active video cropping start pixel LSB [1:0]: The TVP5150 device updates the AVID start values only when this register is written to.

AVID start [9:0] (combined registers 11h and 12h):

01 1111 1111 = 511
00 0000 0001 = 1
00 0000 0000 = 0 (default)
11 1111 1111 = −1
10 0000 0000 = −512

3.22.19 Active Video Cropping Stop Pixel MSB

Address	13h

7	6	5	4	3	2	1	0
AVID stop pixel MSB							

Active video cropping stop pixel MSB [9:2], set this register first before setting the register 14h. The TVP5150 device updates the AVID stop values only when register 14h is written to.

3.22.20 Active Video Cropping Stop Pixel LSB

Address	14h

7	6	5	4	3	2	1	0
Reserved						AVID stop pixel LSB	

Active video cropping stop pixel LSB [1:0]: The number of pixels of active video must be an even number. The TVP5150 device updates the AVID stop values only when this register is written to.

AVID stop [9:0] (combined registers 13h and 14h):

01 1111 1111 = 511
00 0000 0001 = 1
00 0000 0000 = 0 (default) (see Figure 3−10)
11 1111 1111 = −1
10 0000 0000 = −512

3.22.21 Genlock and RTC Register

Address	15h

7	6	5	4	3	2	1	0
Reserved					CDTO_SW	Reserved	GLCO/ RTC

CDTO_LSB_Switch (CDTO_SW):

0 = CDTO_LSB is forced to 0
1 = CDTO_LSB is forced to 1 (default)

GLCO/RTC:

0 = GLCO output
1 = RTC output (default)

Figure 3−13 shows the timing of GLCO and Figure 3−14 shows the timing of RTC.

3.22.22 Horizontal Sync (HSYNC) Start Register

Address	16h

7	6	5	4	3	2	1	0
HSYNC start							

HSYNC start:

1111 1111 = −127 x 4 pixel clocks
1111 1110 = −126 x 4 pixel clocks
1111 1101 = −125 x 4 pixel clocks
1000 0000 = 0 pixel clocks (default)
0111 1111 = 1 x 4 pixel clocks
0111 1110 = 2 x 4 pixel clocks
0000 0000 = 128 x 4 pixel clocks

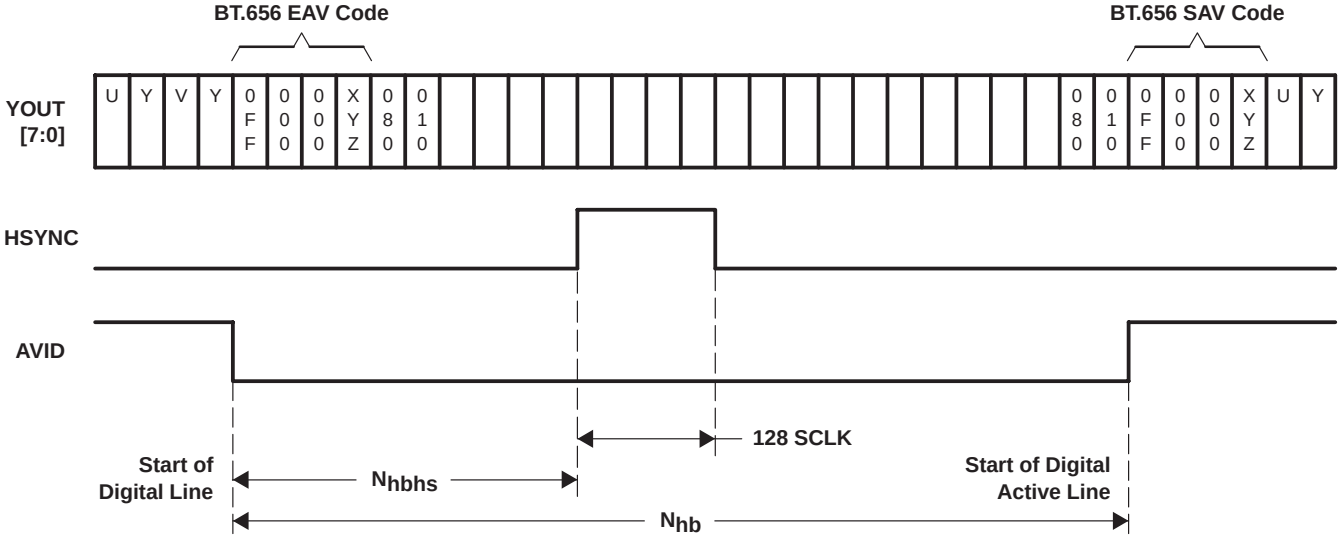


Figure 3−15. Horizontal Sync

Table 3−11. Clock Delays (SCLKs)

STANDARD	N_{hbhs}	N_{hb}
NTSC 601	32	272
PAL 601	24	284

Detailed timing information is also available in Section 3.15, *Synchronization Signals*.

3.22.23 Vertical Blanking Start Register

Address	18h

7	6	5	4	3	2	1	0
Vertical blanking start							

Vertical blanking (VBLK) start:

0111 1111 = 127 lines after start of vertical blanking interval
0000 0001 = 1 line after start of vertical blanking interval
0000 0000 = Same time as start of vertical blanking interval (default) (see Figure 3−9)
1000 0001 = 1 line before start of vertical blanking interval
1111 1111 = 128 lines before start of vertical blanking interval

Vertical blanking is adjustable with respect to the standard vertical blanking intervals. The setting in this register determines the timing of the GPCL/VBLK signal when it is configured to output vertical blank (see register 03h). The setting in this register also determines the duration of the luma bypass function (see register 07h).

3.22.24 Vertical Blanking Stop Register

Address	19h

7	6	5	4	3	2	1	0
Vertical blanking stop							

Vertical blanking (VBLK) stop:

0111 1111 = 127 lines after stop of vertical blanking interval
0000 0001 = 1 line after stop of vertical blanking interval
0000 0000 = Same time as stop of vertical blanking interval (default) (see Figure 3−9)
1000 0001 = 1 line before stop of vertical blanking interval
1111 1111 = 128 lines before stop of vertical blanking interval

Vertical blanking is adjustable with respect to the standard vertical blanking intervals. The setting in this register determines the timing of the GPCL/VBLK signal when it is configured to output vertical blank (see register 03h). The setting in this register also determines the duration of the luma bypass function (see register 07h).

3.22.25 Chrominance Control #1 Register

Address	1Ah

7	6	5	4	3	2	1	0
Reserved			Color PLL reset	Chrominance adaptive comb filter enable (ACE)	Chrominance comb filter enable (CE)	Automatic color gain control	

Color PLL reset:

0 = Color PLL not reset (default)
1 = Color PLL reset

Color PLL phase is reset to zero and the color PLL reset bit then immediately returns to zero. When this bit is set, the subcarrier PLL phase reset bit is transmitted on terminal 23 (GLCO) on the next line (NTSC or PAL).

Chrominance adaptive comb filter enable (ACE):

0 = Disable
1 = Enable (default)

Chrominance comb filter enable (CE):

0 = Disable
1 = Enable (default)

Automatic color gain control (ACGC):

00 = ACGC enabled (default)
01 = Reserved
10 = ACGC disabled
11 = ACGC frozen to the previously set value

3.22.26 Chrominance Control #2 Register

Address	1Bh

7	6	5	4	3	2	1	0
Chrominance comb filter mode [3:0]				Reserved	WCF	Chrominance filter select	

Chrominance comb filter mode [3:0] (CM[3:0]): Chrominance control #2 register 1Bh, bits 7−4

ACE	CE	CM[3]	CM[2]	CM[1]	CM[0]	COMB FILTER SELECTION
0	0	X	X	X	X	Comb filter disabled
0	1	0	0	0	X	Fixed 3-line comb filter with (1, 2, 1)/4 coefficients
0	1	0	0	1	X	Fixed 3-line comb filter with (1, 0, 1)/2 coefficients
0	1	1	0	X	X	Fixed 2-line comb filter
0	1	0	1	0	X	Fixed 4-line (1, 1, 1, 1)/4 comb filter
0	1	0	1	1	X	Fixed 4-line (1, 3, 3, 1)/8 comb filter
0	1	1	1	X	X	Fixed 2-line comb filter
1	X	X	0	0	0	Adaptive between 3-line (1, 2, 1)/4 and 2-line comb filter
1†	X	X	0†	0†	1†	Adaptive between 3-line (1, 2, 1)/4 comb filter and no comb filter
1	X	X	0	1	0	Adaptive between 3-line (1, 0, 1)/2 comb filter and 2-line comb filter
1	X	X	0	1	1	Adaptive between 3-line (1, 0, 1)/2 comb filter and no comb filter
1	X	X	1	0	0	Adaptive between 4-line (1, 1, 1, 1)/4 and 2-line comb filter
1‡	X	X	1‡	0‡	1‡	Adaptive between 4-line (1, 1, 1, 1)/4 comb filter and no comb filter
1	X	X	1	1	0	Adaptive between 4-line (1, 3, 3, 1)/8 comb filter and 2-line comb filter
1	X	X	1	1	1	Adaptive between 4-line (1, 3, 3, 1)/8 comb filter and no comb filter

† Indicates default settings for NTSC
‡ Indicates default settings for PAL mode

Wideband chroma filter (WCF):

0 = Disable
1 = Enable (default)

Chrominance filter select:

00 = No notch (default)
01 = Notch 1
10 = Notch 2
11 = Notch 3

Chrominance output bandwidth (MHz):

WCF	FILTER SELECT	NTSC ITU−R BT.601	PAL ITU−R BT.601
0	00	1.2214	1.2214
	01	0.8782	0.8782
	10	0.7297	0.7297
	11	0.4986	0.4986
1	00	1.4170	1.4170
	01	1.0303	1.0303
	10	0.8438	0.8438
	11	0.5537	0.5537

3.22.27 Interrupt Reset Register B

Address	1Ch

7	6	5	4	3	2	1	0
Software initialization reset	Macrovision detect changed reset	Command ready reset	Field rate changed reset	Line alternation changed reset	Color lock changed reset	H/V lock changed reset	TV/VCR changed reset

Software initialization reset:

0 = No effect (default)
1 = Reset software initialization bit

Macrovision detect changed reset:

0 = No effect (default)
1 = Reset macrovision detect changed bit

Command ready reset:

0 = No effect (default)
1 = Reset command ready bit

Field rate changed reset:

0 = No effect (default)
1 = Reset field rate changed bit

Line alternation changed reset:

0 = No effect (default)
1 = Reset line alternation changed bit

Color lock changed reset:

0 = No effect (default)
1 = Reset color lock changed bit

H/V lock changed reset:

0 = No effect (default)
1 = Reset H/V lock changed bit

TV/VCR changed reset [TV/VCR mode is determined by counting the total number of lines/frame. The mode switches to VCR for nonstandard number of lines]:

0 = No effect (default)
1 = Reset TV/VCR changed bit

Interrupt reset register B is used by the external processor to reset the interrupt status bits in interrupt status register B. Bits loaded with a 1 allow the corresponding interrupt status bit to reset to 0. Bits loaded with a 0 have no effect on the interrupt status bits.

3.22.28 Interrupt Enable Register B

Address	1Dh

7	6	5	4	3	2	1	0
Software initialization occurred enable	Macrovision detect changed	Command ready enable	Field rate changed	Line alternation changed	Color lock changed	H/V lock changed	TV/VCR changed

Software initialization occurred enable:

0 = Disabled (default)
1 = Enabled

Macrovision detect changed:

0 = Disabled (default)
1 = Enabled

Command ready enable:

0 = Disabled (default)
1 = Enabled

Field rate changed:

0 = Disabled (default)
1 = Enabled

Line alternation changed:

0 = Disabled (default)
1 = Enabled

Color lock changed:

0 = Disabled (default)
1 = Enabled

H/V lock changed:

0 = Disabled (default)
1 = Enabled

TV/VCR changed:

0 = Disabled (default)
1 = Enabled

Interrupt enable register B is used by the external processor to mask unnecessary interrupt sources for interrupt B. Bits loaded with a 1 allow the corresponding interrupt condition to generate an interrupt on the external pin. Conversely, bits loaded with a 0 mask the corresponding interrupt condition from generating an interrupt on the external pin. This register only affects the external pin, it does not affect the bits in the interrupt status register. A given condition can set the appropriate bit in the status register and not cause an interrupt on the external pin. To determine if this device is driving the interrupt pin either AND interrupt status register B with interrupt enable register B or check the state of interrupt B in the interrupt B active register.

3.22.29 Interrupt Configuration Register B

Address	1Eh

7	6	5	4	3	2	1	0
Reserved							Interrupt polarity B

Interrupt polarity B:

0 = Interrupt B is active low (default).
1 = Interrupt B is active high.

Interrupt polarity B must be same as interrupt polarity A bit at bit 0 of the interrupt configuration register A at address C2h.

Interrupt configuration register B is used to configure the polarity of interrupt B on the external interrupt pin. When the interrupt B is configured for active low, the pin is driven low when active and high-impedance when inactive (open-collector). Conversely, when the interrupt B is configured for active high, it is driven high-impedance for active and driven low for inactive.

3.22.30 Video Standard Register

Address	28h

7	6	5	4	3	2	1	0
Reserved				Video standard			

Video standard:

0000 = Autoswitch mode (default)
0001 = Reserved
0010 = (M) NTSC ITU−R BT.601
0011 = Reserved
0100 = (B, G, H, I, N) PAL ITU−R BT.601
0101 = Reserved
0110 = (M) PAL ITU−R BT.601
0111 = Reserved
1000 = (Combination-N) ITU−R BT.601
1001 = Reserved
1010 = NTSC 4.43 ITU−R BT.601
1011 = Reserved
1100 = Reserved

With the autoswitch code running, the user can force the device to operate in a particular video standard mode and sample rate by writing the appropriate value into this register.

3.22.31 MSB of Device ID Register

Address	80h

7	6	5	4	3	2	1	0
MSB of device ID							

This register identifies the MSB of the device ID. Value = 0x51.

3.22.32 LSB of Device ID Register

Address	81h

7	6	5	4	3	2	1	0
LSB of device ID							

This register identifies the LSB of the device ID. Value = 0x50.

3.22.33 ROM Version Register

Address	82h

7	6	5	4	3	2	1	0
ROM version: 0x01 for 1.0, 0x20 for 2.00							

Value = 0x02

3.22.34 RAM Patch Code Version Register

Address	83h

7	6	5	4	3	2	1	0
RAM patch code version: 0x10 for combined version 2-1, 0x20 for combined version 2-2							

Value = 0x10

3.22.35 Vertical Line Count MSB Register

Address	84h

7	6	5	4	3	2	1	0
Reserved						Vertical line count MSB	

Vertical line count bits [9:8]

3.22.36 Vertical Line Count LSB Register

Address	85h

7	6	5	4	3	2	1	0
Vertical line count LSB							

Vertical line count bits [7:0]

Registers 84h and 85h can be read and combined to extract the current vertical line count. This can be used with nonstandard video signals such as a VCR in fast-forward or rewind modes to synchronize the downstream video circuitry.

3.22.37 Interrupt Status Register B

Address	86h

7	6	5	4	3	2	1	0
Software initialization	Macrovision detect changed	Reserved	Field rate changed	Line alternation changed	Color lock changed	H/V lock changed	TV/VCR changed

Software initialization:

0 = Software initialization is not ready (default).
1 = Software initialization is ready.

Macrovision detect changed:

0 = Macrovision detect status has not changed (default).
1 = Macrovision detect status has changed.

Field rate changed:

0 = Field rate has not changed (default).
1 = Field rate has changed.

Line alternation changed:

0 = Line alteration has not changed (default).
1 = Line alternation has changed.

Color lock changed:

0 = Color lock status has not changed (default).
1 = Color lock status has changed.

H/V lock changed:

0 = H/V lock status has not changed (default).
1 = H/V lock status has changed.

TV/VCR changed:

0 = TV/VCR status has not changed (default).
1 = TV/VCR status has changed.

Interrupt status register B is polled by the external processor to determine the interrupt source for interrupt B. After an interrupt condition is set, it can be reset by writing to the interrupt reset register B at subaddress 1Ch with a 1 in the appropriate bit.

3.22.38 Interrupt Active Register B

Address	87h

7	6	5	4	3	2	1	0
Reserved							Interrupt B

Interrupt B:

0 = Interrupt B is not active on the external terminal (default).
1 = Interrupt B is active on the external terminal.

The interrupt active register B is polled by the external processor to determine if interrupt B is active.

3.22.39 Status Register #1

Address	88h

7	6	5	4	3	2	1	0
Peak white detect status	Line-alternating status	Field rate status	Lost lock detect	Color subcarrier lock status	Vertical sync lock status	Horizontal sync lock status	TV/VCR status

Peak white detect status:

0 = Peak white is not detected.
1 = Peak white is detected.

Line-alternating status:

0 = Nonline alternating
1 = Line alternating

Field rate status:

0 = 60 Hz
1 = 50 Hz

Lost lock detect:

0 = No lost lock since status register #1 was last read.
1 = Lost lock since status register #1 was last read.

Color subcarrier lock status:

0 = Color subcarrier is not locked.
1 = Color subcarrier is locked.

Vertical sync lock status:

0 = Vertical sync is not locked.
1 = Vertical sync is locked.

Horizontal sync lock status:

0 = Horizontal sync is not locked.
1 = Horizontal sync is locked.

TV/VCR status [TV/VCR mode is determined by counting the total number of lines/frame. The mode switches to VCR for nonstandard number of lines]:

0 = TV
1 = VCR

3.22.40 Status Register #2

Address	89h

7	6	5	4	3	2	1	0
Reserved	Weak signal detection	PAL switch polarity	Field sequence status	AGC and offset frozen status	Reserved	Macrovision detection	

Weak signal detection:

0 = No weak signal
1 = Weak signal mode

PAL switch polarity of first line of odd field:

0 = PAL switch is 0
1 = PAL switch is 1

Field sequence status:

0 = Even field
1 = Odd field

AGC and offset frozen status:

0 = AGC and offset are not frozen.
1 = AGC and offset are frozen.

Macrovision detection:

00 = No copy protection
01 = AGC pulses/pseudo-syncs present
10 = AGC pulses/pseudo-syncs and 2-line color striping present
11 = AGC pulses/pseudo-syncs and 4-line color striping present

3.22.41 Status Register #3

Address	8Ah

7	6	5	4	3	2	1	0
AGC gain							

AGC gain:

0000 0000 = −6 dB
0100 0000 = −3 dB
1000 0000 = 0 dB
1100 0000 = 3 dB
1111 1111 = 6 dB

3.22.42 Status Register #4

Address	8Bh

7	6	5	4	3	2	1	0
Subcarrier to horizontal (SCH) phase							

SCH (color PLL subcarrier phase at 50% of the falling edge of horizontal sync of line one of odd field; step size 360°/256):

0000 0000 = 0.00°
0000 0001 = 1.41°
0000 0010 = 2.81°
1111 1110 = 357.2°
1111 1111 = 358.6°

3.22.43 Status Register #5

Address	8Ch

7	6	5	4	3	2	1	0
Autoswitch mode	Reserved			Video standard			Sampling rate

This register contains information about the detected video standard and the sampling rate at which the device is currently operating. When autoswitch code is running, this register must be tested to determine which video standard has been detected.

Autoswitch mode:

0 = Stand-alone (forced video standard) mode
1 = Autoswitch mode

Video standard:

VIDEO STANDARD [3:1]			SR	VIDEO STANDARD
BIT 3	BIT2	BIT1	BIT 0	
0	0	0	0	Reserved
0	0	0	1	(M) NTSC ITU−R BT.601
0	0	1	0	Reserved
0	0	1	1	(B, G, H, I, N) PAL ITU−R BT.601
0	1	0	0	Reserved
0	1	0	1	(M) PAL ITU−R BT.601
0	1	1	0	Reserved
0	1	1	1	(Combination-N) ITU−R BT.601
1	0	0	0	Reserved
1	0	0	1	NTSC 4.43 ITU−R BT.601
1	0	1	0	Reserved
1	0	1	1	Reserved

Sampling rate (SR):

0 = Reserved
1 = ITU−R BT.601

3.22.44 Closed Caption Data Registers

Address	90h−93h

Address	7	6	5	4	3	2	1	0
90h	Closed caption field 1 byte 1							
91h	Closed caption field 1 byte 2							
92h	Closed caption field 2 byte 1							
93h	Closed caption field 2 byte 2							

These registers contain the closed caption data arranged in bytes per field.

3.22.45 WSS Data Registers

Address	94h−99h

NTSC

ADDRESS	7	6	5	4	3	2	1	0	BYTE
94h			b5	b4	b3	b2	b1	b0	WSS field 1 byte 1
95h	b13	b12	b11	b10	b9	b8	b7	b6	WSS field 1 byte 2
96h			b19	b18	b17	b16	b15	b14	WSS field 1 byte 3
97h			b5	b4	b3	b2	b1	b0	WSS field 2 byte 1
98h	b13	b12	b11	b10	b9	b8	b7	b6	WSS field 2 byte 2
99h			b19	b18	b17	b16	b15	b14	WSS field 2 byte 3

These registers contain the wide screen signaling (WSS) data for NTSC.

Bits 0−1 represent word 0, aspect ratio
Bits 2−5 represent word 1, header code for word 2
Bits 6−13 represent word 2, copy control
Bits 14−19 represent word 3, CRC

PAL

ADDRESS	7	6	5	4	3	2	1	0	BYTE
94h	b7	b6	b5	b4	b3	b2	b1	b0	WSS field 1 byte 1
95h			b13	b12	b11	b10	b9	b8	WSS field 1 byte 2
96h	b7	b6	b5	b4	b3	b2	b1	b0	WSS field 2 byte 1
97h			b13	b12	b11	b10	b9	b8	WSS field 2 byte 2
98h	Reserved								
99h	Reserved								

PAL:

Bits 0−3 represent group 1, aspect ratio
Bits 4−7 represent group 2, enhanced services
Bits 8−10 represent group 3, subtitles
Bits 11−13 represent group 4, others

3.22.46 VPS Data Registers

Address	9Ah–A6h

ADDRESS	7	6	5	4	3	2	1	0
9Ah	VPS byte 1							
9Bh	VPS byte 2							
9Ch	VPS byte 3							
9Dh	VPS byte 4							
9Eh	VPS byte 5							
9Fh	VPS byte 6							
A0h	VPS byte 7							
A1h	VPS byte 8							
A2h	VPS byte 9							
A3h	VPS byte 10							
A4h	VPS byte 11							
A5h	VPS byte 12							
A6h	VPS byte 13							

These registers contain the entire VPS data line except the clock run-in code or the start code.

3.22.47 VITC Data Registers

Address	A7h–AFh

ADDRESS	7	6	5	4	3	2	1	0
A7h	VITC byte 1, frame byte 1							
A8h	VITC byte 2, frame byte 2							
A9h	VITC byte 3, seconds byte 1							
AAh	VITC byte 4, seconds byte 2							
ABh	VITC byte 5, minutes byte 1							
ACh	VITC byte 6, minutes byte 2							
ADh	VITC byte 7, hour byte 1							
AEh	VITC byte 8, hour byte 2							
AFh	VITC byte 9, CRC							

These registers contain the VITC data.

3.22.48 VBI FIFO Read Data Register

Address	B0h

7	6	5	4	3	2	1	0
FIFO read data							

This address is provided to access VBI data in the FIFO through the host port. All forms of teletext data come directly from the FIFO, while all other forms of VBI data can be programmed to come from the registers or from the FIFO. Current status of the FIFO can be found at address C6h and the number of bytes in the FIFO is located at address C7h. If the host port is to be used to read data from the FIFO, then the output formatter must be disabled at address CDh bit 0. The format used for the VBI FIFO is shown in Section 3.12.

3.22.49 Teletext Filter and Mask Registers

Address	B1h–BAh

ADDRESS	7	6	5	4	3	2	1	0
B1h	Filter 1 Mask 1				Filter 1 Pattern 1			
B2h	Filter 1 Mask 2				Filter 1 Pattern 2			
B3h	Filter 1 Mask 3				Filter 1 Pattern 3			
B4h	Filter 1 Mask 4				Filter 1 Pattern 4			
B5h	Filter 1 Mask 5				Filter 1 Pattern 5			
B6h	Filter 2 Mask 1				Filter 2 Pattern 1			
B7h	Filter 2 Mask 2				Filter 2 Pattern 2			
B8h	Filter 2 Mask 3				Filter 2 Pattern 3			
B9h	Filter 2 Mask 4				Filter 2 Pattern 4			
BAh	Filter 2 Mask 5				Filter 2 Pattern 5			

For an NABTS system, the packet prefix consists of five bytes. Each byte contains four data bits (D[3:0]) interlaced with four Hamming protection bits (H[3:0]):

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D[3]	H[3]	D[2]	H[2]	D[1]	H[1]	D[0]	H[0]

Only the data portion D[3:0] from each byte is applied to a teletext filter function with corresponding pattern bits P[3:0] and mask bits M[3:0]. Hamming protection bits are ignored by the filter.

For a WST system (PAL or NTSC), the packet prefix consists of two bytes so that two patterns are used. Patterns 3, 4, and 5 are ignored.

The mask bits enable filtering using the corresponding bit in the pattern register. For example, a 1 in the LSB of mask 1 means that the filter module must compare the LSB of nibble 1 in the pattern register to the first data bit on the transaction. If these match, then a true result is returned. A 0 in a bit of mask 1 means that the filter module must ignore that data bit of the transaction. If all 0s are programmed in the mask bits, then the filter matches all patterns returning a true result (default 00h).

Pattern and mask for each byte and filter are referred as <1,2><P,M><1,2,3,4,5> where:

<1,2> identifies the filter 1 or 2
<P,M> identifies the pattern or mask
<1,2,3,4,5> identifies the byte number

3.22.50 Teletext Filter Control Register

Address	BBh

7	6	5	4	3	2	1	0
Reserved			Filter logic		Mode	TTX filter 2 enable	TTX filter 1 enable

Filter logic: allows different logic to be applied when combining the decision of filter 1 and filter 2 as follows:

00 = NOR (Default)
01 = NAND
10 = OR
11 = AND

Mode:

0 = Teletext WST PAL mode B (2 header bytes) (default)
1 = Teletext NABTS NTSC mode C (5 header bytes)

TTX filter 2 enable:

0 = Disabled (default)
1 = Enabled

TTX filter 1 enable:

0 = Disabled (default)
1 = Enabled

If the filter matches or if the filter mask is all 0s, then a true result is returned.

3.22.51 Interrupt Status Register A

Address	C0h

7	6	5	4	3	2	1	0
Lock state interrupt	Lock interrupt	Cycle complete interrupt	Bus error interrupt	Reserved	FIFO threshold interrupt	Line interrupt	Data interrupt

The interrupt status register A can be polled by the host processor to determine the source of an interrupt. After an interrupt condition is set it can be reset by writing to this register with a 1 in the appropriate bit(s).

Lock state interrupt:

0 = TVP5150 is not locked to the video signal.
1 = TVP5150 is locked to the video signal.

Lock interrupt:

0 = A transition has not occurred on the lock signal.
1 = A transition has occurred on the lock signal.

Cycle complete interrupt:

0 = Read or write cycle in progress
1 = Read or write cycle complete

Bus error interrupt:

0 = No bus error
1 = PHI interface detected an illegal access

FIFO threshold interrupt:

0 = The amount of data in the FIFO has not yet crossed the threshold programmed at address C8h.
1 = The amount of data in the FIFO has crossed the threshold programmed at address C8h.

Line interrupt:

0 = The video line number has not yet been reached.
1 = The video line number programmed in address CAh has occurred.

Data interrupt:

0 = No data is available.
1 = VBI data is available either in the FIFO or in the VBI data registers.

3.22.52 Interrupt Enable Register A

Address	C1h

7	6	5	4	3	2	1	0
Reserved	Lock interrupt enable	Cycle complete interrupt enable	Bus error interrupt enable	Reserved	FIFO threshold interrupt enable	Line interrupt enable	Data interrupt enable

The interrupt enable register A is used by the host processor to mask unnecessary interrupt sources. Bits loaded with a 1 allow the corresponding interrupt condition to generate an interrupt on the external pin. Conversely, bits loaded with a 0 mask the corresponding interrupt condition from generating an interrupt on the external pin. This register only affects the interrupt on the external terminal, it does not affect the bits in interrupt status register A. A given condition can set the appropriate bit in the status register and not cause an interrupt on the external terminal. To determine if this device is driving the interrupt terminal either perform a logical AND of interrupt status register A with interrupt enable register A, or check the state of the interrupt A bit in the interrupt configuration register at address C2h.

Lock interrupt enable:

0 = Disabled (default)
1 = Enabled

Cycle complete interrupt enable:

0 = Disabled (default)
1 = Enabled

Bus error interrupt enable:

0 = Disabled (default)
1 = Enabled

FIFO threshold interrupt enable:

0 = Disabled (default)
1 = Enabled

Line interrupt enable:

0 = Disabled (default)
1 = Enabled

Data interrupt enable:

0 = Disabled (default)
1 = Enabled

3.22.53 Interrupt Configuration Register A

Address	C2h

7	6	5	4	3	2	1	0
Reserved					YUV enable (VDPOE)	Interrupt A	Interrupt polarity A

YUV enable (VDPOE):

0 = YUV pins are high impedance.
1 = YUV pins are active if other conditions are met (default).

Interrupt A (read-only):

0 = Interrupt A is not active on the external pin (default).
1 = Interrupt A is active on the external pin.

Interrupt polarity A:

0 = Interrupt A is active low (default).
1 = Interrupt A is active high.

Interrupt configuration register A is used to configure the polarity of the external interrupt terminal. When interrupt A is configured as active low, the terminal is driven low when active and high-impedance when inactive (open collector). Conversely, when the terminal is configured as active high, it is driven high when active and driven low when inactive.

3.22.54 VDP Configuration RAM Register

Address	C3h−C5h

Address	7	6	5	4	3	2	1	0
C3h	Configuration data							
C4h	RAM address (7:0)							
C5h	Reserved							RAM address 8

The configuration RAM data is provided to initialize the VDP with initial constants. The configuration RAM is 512 bytes organized as 32 different configurations of 16 bytes each. The first 12 configurations are defined for the current VBI standards. An additional 2 configurations can be used as a custom programmed mode for unique standards like Gemstar.

Address C3h is used to read or write to the RAM. The RAM internal address counter is automatically incremented with each transaction. Addresses C5h and C4h make up a 9-bit address to load the internal address counter with a specific start address. This can be used to write a subset of the RAM for only those standards of interest. Registers D0h−FBh must all be programmed with FFh, before writing or reading the configuration RAM. Full field mode (CFh) must be disabled as well.

The suggested RAM contents are shown below. All values are hexadecimal.

Table 3−12. VBI Configuration RAM

Index	Address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Reserved	000	Reserved															
Reserved	010	Reserved															
Reserved	020	Reserved															
WST PAL B 6	030	AA	AA	FF	FF	27	2E	20	2B	A6	72	10	0	0	0	10	0
Reserved	040	Reserved															
WST PAL C 6	050	AA	AA	FF	FF	E7	2E	20	22	A6	98	0D	0	0	0	10	0
Reserved	060	Reserved															
WST NTSC 6	070	AA	AA	FF	FF	27	2E	20	23	69	93	0D	0	0	0	10	0
Reserved	080	Reserved															
NABTS, NTSC 6	090	AA	AA	FF	FF	E7	2E	20	22	69	93	0D	0	0	0	15	0
Reserved	0A0	Reserved															
NABTS, NTSC-J 6	0B0	AA	AA	FF	FF	A7	2E	20	23	69	93	0D	0	0	0	10	0
Reserved	0C0	Reserved															
CC, PAL 6	0D0	AA	2A	FF	3F	04	51	6E	02	A6	7B	09	0	0	0	27	0
Reserved	0E0	Reserved															
CC, NTSC 6	0F0	AA	2A	FF	3F	04	51	6E	02	69	8C	09	0	0	0	27	0
Reserved	100	Reserved															
WSS, PAL 6	110	5B	55	C5	FF	0	71	6E	42	A6	CD	0F	0	0	0	3A	0
Reserved	120	Reserved															
WSS, NTSC C	130	38	00	3F	00	0	71	6E	43	69	7C	08	0	0	0	39	0
Reserved	140	Reserved															
VITC, PAL 6	150	0	0	0	0	0	8F	6D	49	A6	85	08	0	0	0	4C	0
Reserved	160	Reserved															
VITC, NTSC 6	170	0	0	0	0	0	8F	6D	49	69	94	08	0	0	0	4C	0
Reserved	180	Reserved															
VPS, PAL 6	190	AA	AA	FF	FF	BA	CE	2B	0D	A6	DA	0B	0	0	0	60	0
Custom	1A0	Programmable															
Custom	1B0	Programmable															

3.22.55 VDP Status Register

Address	C6h

7	6	5	4	3	2	1	0
FIFO full error	FIFO empty	TTX available	CC field 1 available	CC field 2 available	WSS available	VPS available	VITC available

The VDP status register indicates whether data is available in either the FIFO or data registers, and status information about the FIFO. Reading data from the corresponding register does not clear the status flags automatically. These flags are only reset by writing a 1 to the respective bit. However, bit 6 is updated automatically.

FIFO full error:

0 = No FIFO full error
1 = FIFO was full during a write to FIFO.

The FIFO full error flag is set when the current line of VBI data can not enter the FIFO. For example, if the FIFO has only 10 bytes left and teletext is the current VBI line, the FIFO full error flag is set, but no data is written because the entire teletext line will not fit. However, if the next VBI line is closed caption requiring only 2 bytes of data plus the header, this goes into the FIFO. Even if the full error flag is set.

FIFO empty:

0 = FIFO is not empty.
1 = FIFO is empty.

TTX available:

0 = Teletext data is not available.
1 = Teletext data is available.

CC field 1 available:

0 = Closed caption data from field 1 is not available.
1 = Closed caption data from field 1 is available.

CC field 2 available:

0 = Closed caption data from field 2 is not available.
1 = Closed caption data from field 2 is available.

WSS available:

0 = WSS data is not available.
1 = WSS data is available.

VPS available:

0 = VPS data is not available.
1 = VPS data is available.

VITC available:

0 = VITC data is not available.
1 = VITC data is available.

3.22.56 FIFO Word Count Register

Address	C7h

7	6	5	4	3	2	1	0
Number of words							

This register provides the number of words in the FIFO. 1 word equals 2 bytes.

3.22.57 FIFO Interrupt Threshold Register

Address	C8h

7	6	5	4	3	2	1	0
Number of words							

This register is programmed to trigger an interrupt when the number of words in the FIFO exceeds this value (default 80h). This interrupt must be enabled at address C1h. 1 word equals 2 bytes.

3.22.58 FIFO Reset Register

Address	C9h

7	6	5	4	3	2	1	0
Any data							

Writing any data to this register resets the FIFO and clears any data present.

3.22.59 Line Number Interrupt Register

Address	CAh

7	6	5	4	3	2	1	0
Field 1 enable	Field 2 enable	Line number					

This register is programmed to trigger an interrupt when the video line number matches this value in bits 5:0. This interrupt must be enabled at address C1h. The value of 0 or 1 does not generate an interrupt.

Field 1 enable:

0 = Disabled (default)
1 = Enabled

Field 2 enable:

0 = Disabled (default)
1 = Enabled

Line number: (default 00h)

3.22.60 Pixel Alignment Registers

Address	CBh−CCh

Address	7	6	5	4	3	2	1	0
CBh	Switch pixel [7:0]							
CCh	Reserved						Switch pixel [9:8]	

These registers form a 10-bit horizontal pixel position from the falling edge of sync, where the VDP controller initiates the program from one line standard to the next line standard. For example, the previous line of teletext to the next line of closed caption. This value must be set so that the switch occurs after the previous transaction has cleared the delay in the VDP, but early enough to allow the new values to be programmed before the current settings are required.

The default value is 0x1E and has been tested with every standard supported here. A new value is needed only if a custom standard is in use.

3.22.61 FIFO Output Control Register

Address	CDh

7	6	5	4	3	2	1	0
Reserved							Host access enable

This register is programmed to allow I^2C access to the FIFO or allowing all VDP data to go out the video port.

Host access enable:

0 = Output FIFO data to the video output Y[9:2] (default)
1 = Allow I^2C access to the FIFO data

3.22.62 Automatic Initialization Register

Address	CEh

7	6	5	4	3	2	1	0
Reserved					Auto initialize	Auto clock	Reserved

This register enables the VDP to preprogram the line mode registers for the most common standards based on the video standard, that is, PAL, NTSC.

Auto initialize:

0 = Disable initialization of teletext and closed caption standards (default)
1 = Enable initialization of teletext and closed caption standards

Auto clock:

0 = Do not update bit 0 (default)
1 = Enable VDP to update bit 0

3.22.63 Full Field Enable Register

Address	CFh

7	6	5	4	3	2	1	0
Reserved							Full field enable

This register enables the full field mode. In this mode, all lines outside the vertical blank area and all lines in the line mode registers programmed with FFh are sliced with the definition of register FCh. Values other than FFh in the line mode registers allow a different slice mode for that particular line.

Full field enable:

0 = Disable full field mode (default)
1 = Enable full field mode

3.22.64 Line Mode Registers

Address	D0h−FBh

ADDRESS	7	6	5	4	3	2	1	0
D0h	Line 6 Field 1							
D1h	Line 6 Field 2							
D2h	Line 7 Field 1							
D3h	Line 7 Field 2							
D4h	Line 8 Field 1							
D5h	Line 8 Field 2							
D6h	Line 9 Field 1							
D7h	Line 9 Field 2							
D8h	Line 10 Field 1							
D9h	Line 10 Field 2							
DAh	Line 11 Field 1							
DBh	Line 11 Field 2							
DCh	Line 12 Field 1							
DDh	Line 12 Field 2							
DEh	Line 13 Field 1							
DFh	Line 13 Field 2							
E0h	Line 14 Field 1							
E1h	Line 14 Field 2							
E2h	Line 15 Field 1							
E3h	Line 15 Field 2							
E4h	Line 16 Field 1							
E5h	Line 16 Field 2							
E6h	Line 17 Field 1							
E7h	Line 17 Field 2							
E8h	Line 18 Field 1							
E9h	Line 18 Field 2							
EAh	Line 19 Field 1							
EBh	Line 19 Field 2							
ECh	Line 20 Field 1							
EDh	Line 20 Field 2							
EEh	Line 21 Field 1							
EFh	Line 21 Field 2							
F0h	Line 22 Field 1							
F1h	Line 22 Field 2							
F2h	Line 23 Field 1							
F3h	Line 23 Field 2							
F4h	Line 24 Field 1							
F5h	Line 24 Field 2							
F6h	Line 25 Field 1							
F7h	Line 25 Field 2							
F8h	Line 26 Field 1							
F9h	Line 26 Field 2							
FAh	Line 27 Field 1							
FBh	Line 27 Field 2							

These registers program the specific VBI standard at a specific line in the video field.

Bit 7:

0 = Disable filtering of null bytes in closed caption modes
1 = Enable filtering of null bytes in closed caption modes (default)

In teletext modes, bit 7 enables the data filter function for that particular line. If it is set to 0, then the data filter passes all data on that line.

Bit 6:

0 = Send VBI data to registers only.
1 = Send VBI data to FIFO and the registers. Teletext data only goes to FIFO. (default)

Bit 5:

0 = Allow VBI data with errors in the FIFO
1 = Do not allow VBI data with errors in the FIFO (default)

Bit 4:

0 = Do not enable error detection and correction
1 = Enable error detection and correction (when bits [3:0] = 1 2, 3, and 4 only) (default)

Bits [3:0]:

0000 = Reserved
0001 = WST PAL B
0010 = WST PAL C
0011 = WST NTSC
0100 = NABTS NTSC
0101 = TTX NTSC
0110 = CC PAL
0111 = CC NTSC
1000 = WSS PAL
1001 = WSS NTSC
1010 = VITC PAL
1011 = VITC NTSC
1100 = VPS PAL
1101 = Custom 1
1110 = Custom 2
1111 = Active video (VDP off) (default)

A value of FFh in the line mode registers is required for any line to be sliced as part of the full field mode.

3.22.65 Full Field Mode Register

Address	FCh

7	6	5	4	3	2	1	0
Full field mode							

This register programs the specific VBI standard for full field mode. It can be any VBI standard. Individual line settings take priority over the full field register. This allows each VBI line to be programmed independently but have the remaining lines in full field mode. The full field mode register has the same definitions as the line mode registers (default 7Fh).

4 Electrical Characteristics

4.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)†

Supply voltage range: IOV_{DD} to DGND . . . . . −0.5 V to 4.5 V
DV_{DD} to DGND . . . . . −0.5 V to 2.3 V
PLL_AV_{DD} to PLL_AGND . . . . . −0.5 V to 2.3 V
$CH1\_AV_{DD}$ to CH1_AGND . . . . . −0.5 V to 2.3 V
Digital input voltage range, V_I to DGND . . . . . −0.5 V to 4.5 V
Input voltage range, XTAL1 to PLL_GND . . . . . −0.5 V to 2.3 V
Analog input voltage range A_I to CH1_AGND . . . . . −0.2 V to 2.0 V
Digital output voltage range, V_O to DGND . . . . . −0.5 V to 4.5 V
Operating free-air temperature, T_A . . . . . 0°C to 70°C
Storage temperature, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
$IODV_{DD}$	Digital I/O supply voltage	3.0	3.3	3.6	V
DV_{DD}	Digital supply voltage	1.65	1.8	1.95	V
PLL_AV_{DD}	Analog PLL supply voltage	1.65	1.8	1.95	V
$CH1\_AV_{DD}$	Analog core supply voltage	1.65	1.8	1.95	V
$V_{I(P-P)}$	Analog input voltage (ac-coupling necessary)	0		0.75	V
V_{IH}	Digital input voltage high	0.7 IOV_{DD}			V
V_{IL}	Digital input voltage low			0.3 IOV_{DD}	V
V_{IH_XTAL}	XTAL input voltage high	0.7 PLL_AV_{DD}			V
V_{IL_XTAL}	XTAL input voltage low			0.3 PLL_AV_{DD}	V
I_{OH}	High-level output current			2	mA
I_{OL}	Low-level output current			−2	mA
I_{OH_SCLK}	SCLK high-level output current			4	mA
I_{OL_SCLK}	SCLK low-level output current			−4	mA
T_A	Operating free-air temperature	0		70	°C

4.2.1 Crystal Specifications

CRYSTAL SPECIFICATIONS	MIN	NOM	MAX	UNIT
Frequency		14.31818		MHz
Frequency tolerance		±50		ppm

4.3 Electrical Characteristics

DV_{DD} = 1.8 V, PLL_AV_{DD} = 1.8 V, $CH1\_AV_{DD}$ = 1.8 V, IOV_{DD} = 3.3 V

For minimum/maximum values: T_A = 0°C to 70°C, and for typical values: T_A = 25°C unless otherwise noted

4.3.1 DC Electrical Characteristics

PARAMETER		TEST CONDITIONS (see Note 1)	MIN	TYP	MAX	UNIT
$I_{DD(IO\_D)}$	Digital I/O supply current	Color bar input		6		mA
$I_{DD(D)}$	Digital core supply current	Color bar input		21		mA
$I_{DD(PLL\_A)}$	Analog PLL supply current	Color bar input		6		mA
$I_{DD(CH1\_A)}$	Analog PLL supply current	Color bar input		25		mA
P_{TOT}	Total power dissipation, normal mode	Color bar input		113	150	mW
P_{DOWN}	Total power dissipation, power-down mode	Color bar input		0.9		mW
C_i	Input capacitance	By design		8		pF
V_{OH}	Output voltage high	I_{OH} = 2 mA	0.8 IOV_{DD}			V
V_{OL}	Output voltage low	I_{OL} = −2 mA			0.22 IOV_{DD}	V
V_{OH_SCLK}	SCLK output voltage high	I_{OH} = 2 mA	0.8 IOV_{DD}			V
V_{OL_SCLK}	SCLK output voltage low	I_{OL} = −4 mA			0.22 IOV_{DD}	V
I_{IH}	High-level input current (see Note 2)	$V_I = V_{IH}$			±20	µA
I_{IL}	Low-level input current (see Note 2)	$V_I = V_{IL}$			±20	µA

NOTES: 1. Measured with a load of 15 pF.
2. YOUT7 is a bidirectional terminal with an internal pulldown resistor. This terminal may sink more than the specified current when in the RESET mode.

4.3.2 Analog Processing and A/D Converters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Zi	Input impedance, analog video inputs	By design		500		kΩ
C_i	Input capacitance, analog video inputs	By design		10		pF
Vi(pp)	Input voltage range	$C_{coupling}$ = 0.1 µF	0		0.75	V
ΔG	Gain control range		0		12	dB
DNL	DC differential nonlinearity	A/D only		±0.5		LSB
INL	DC integral nonlinearity	A/D only		±1		LSB
Fr	Frequency response	6 MHz		−0.9	−3	dB
SNR	Signal-to-noise ratio	6 MHz, 1.0 V_{P-P}		50		dB
NS	Noise spectrum	50% flat field		50		dB
DP	Differential phase			1.5		°
DG	Differential gain			0.5%		

4.3.3 Timing

4.3.3.1 Clocks, Video Data, Sync Timing

PARAMETER		TEST CONDITIONS (see NOTE 2)	MIN	TYP	MAX	UNIT
	Duty cycle PCLK, SCLK			50%		
t_1	Delay time, SCLK falling edge to digital outputs	See Note 3 (by design)		2.8	8	ns

NOTES: 3. C_L = 15 pF
4. All outputs are 3.3 V.

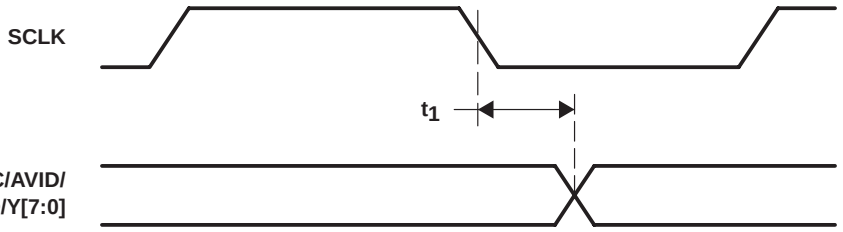


Figure 4−1. Clocks, Video Data, and Sync Timing

4.3.3.2 I2C Host Port Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Bus free time between STOP and START		1.3			µs
t_2	Setup time for a (repeated) START condition		0.6			µs
t_3	Hold time (repeated) START condition		0.6			µs
t_4	Setup time for a STOP condition		0.6			ns
t_5	Data setup time		100			ns
t_6	Data hold time		0		0.9	µs
t_7	Rise time VC1(SDA) and VC0(SCL) signal		250			ns
t_8	Fall time VC1(SDA) and VC0(SCL) signal			250		ns
C_b	Capacitive load for each bus line				400	pF
f_{I2C}	I2C clock frequency				400	kHz

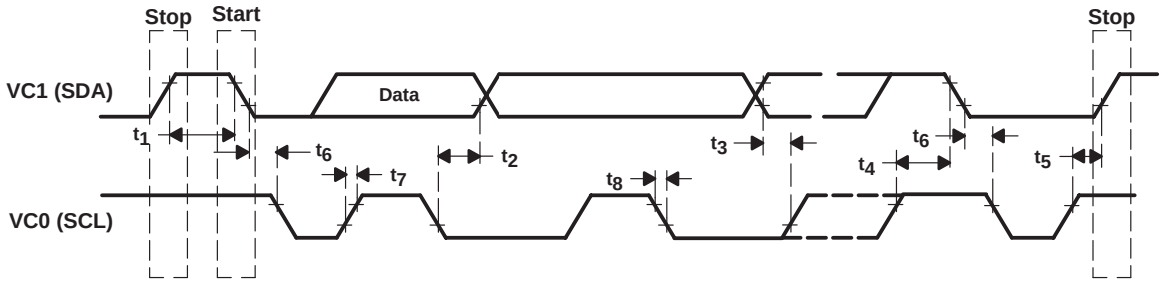
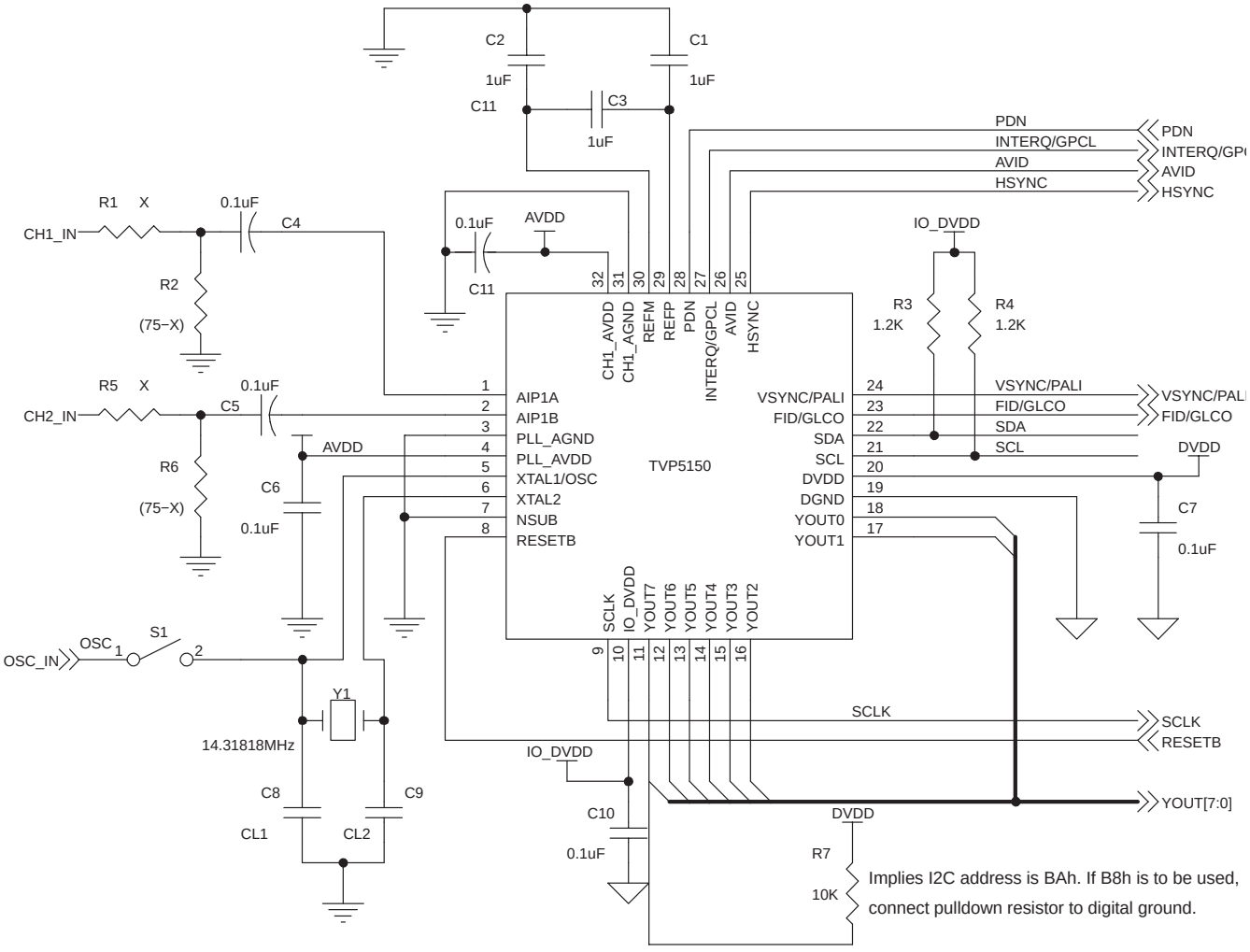


Figure 4−2. I2C Host Port Timing

5 Application Information

5.1 Application Example

NOTE: X and (75 − X) is used since the maximum P−P signal allowed is 0.75V. Hence for a 140IRE signal, the signal must be divided by approximately half. Change X depending on the input signal range.



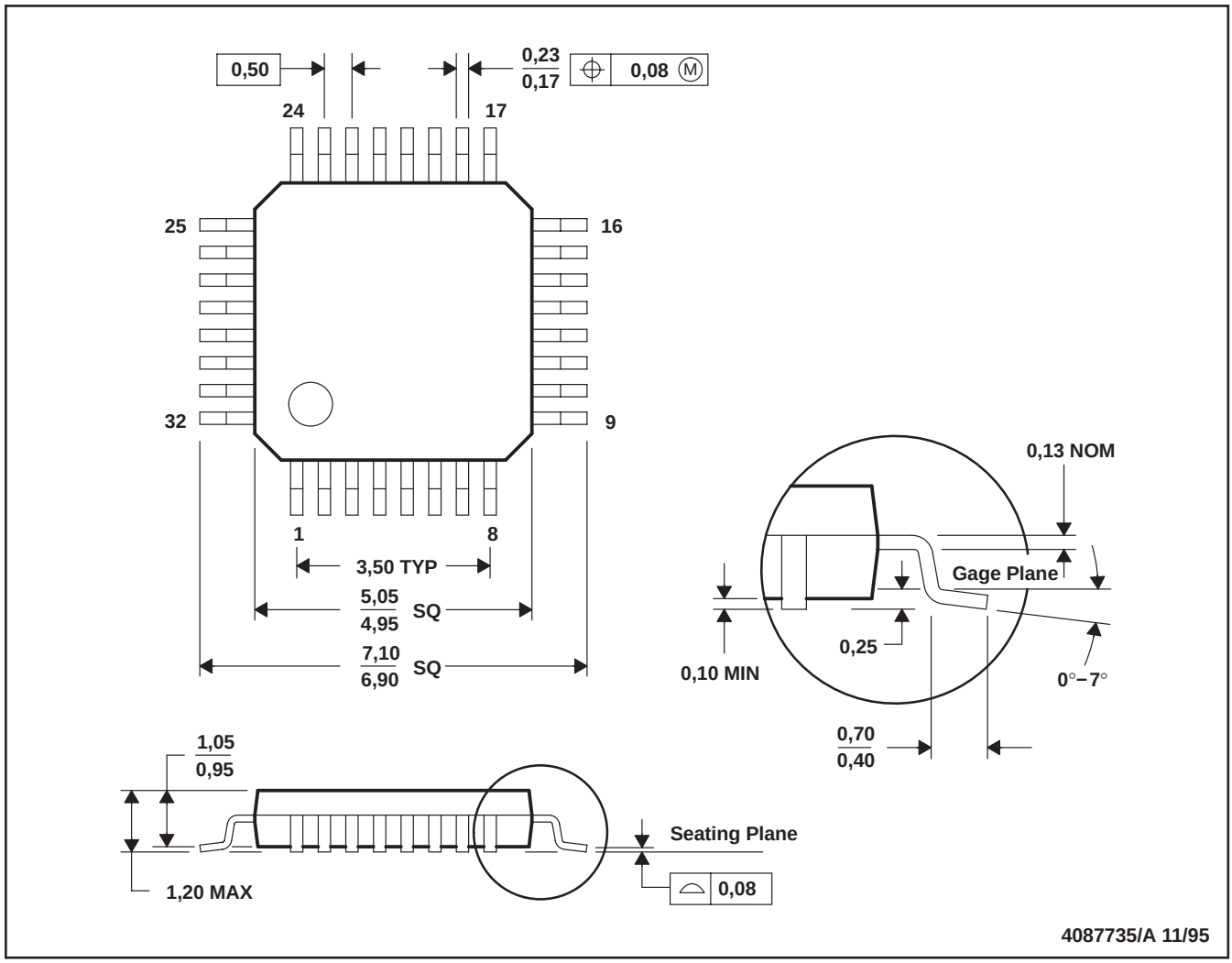
NOTE: The use of INTERQ/GPCL/AVID/HSYNC and VSYNC is optional. These are outputs and can be left floating.
When OSC is connected through S1, remove the caps for the crystal.
PDN needs to be high, if device has to be always operational.
RESETB is operational only when PDN is high. This allows an active low reset to the device.
CL1 and CL2 typical values used are 27 pF.

Figure 5−1. Application Example

6 Mechanical Data

The TVP5150 device is available in the 32-terminal PQFP package (PBS). The following figure shows the mechanical dimensions for the PBS package.

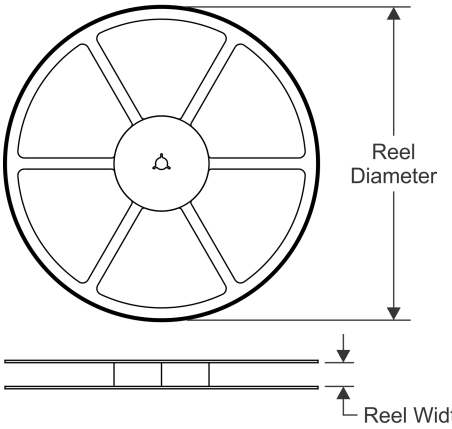
PBS (S-PQFP-G32) **PLASTIC QUAD FLATPACK**



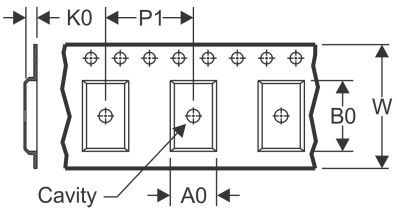
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

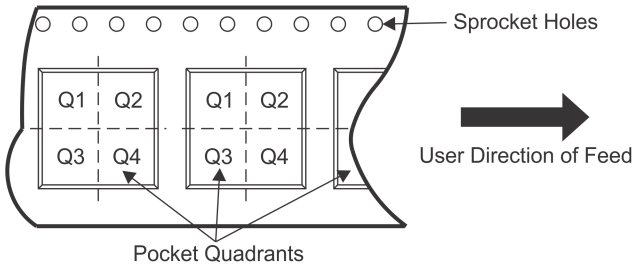


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

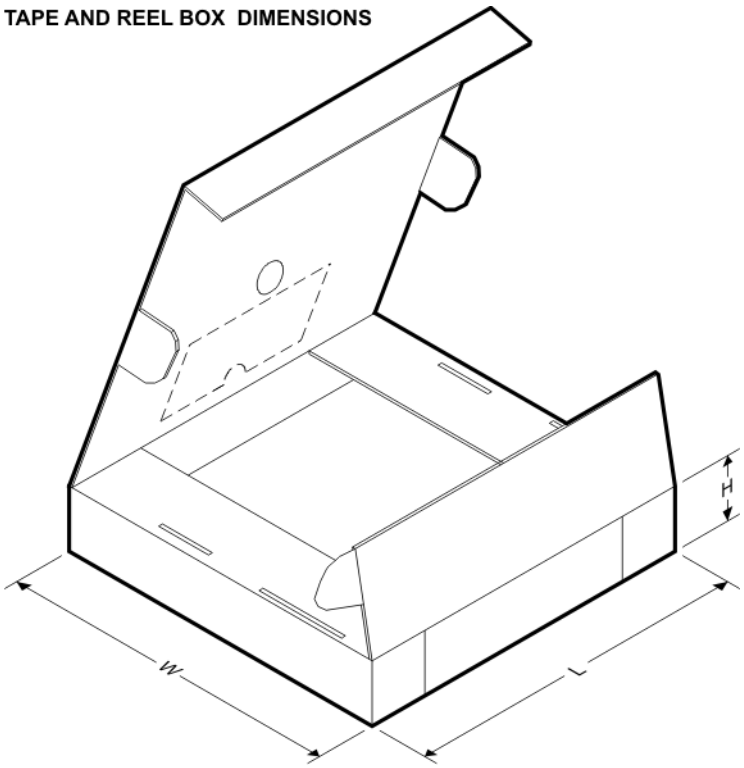
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TVP5150PBSR	TQFP	PBS	32	1000	330.0	16.4	7.2	7.2	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TVP5150PBSR	TQFP	PBS	32	1000	367.0	367.0	38.0

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