

4M-BIT CMOS FAST STATIC RAM
512K-WORD BY 8 BITS**Description**

The μ PD434008 is a high speed, low power, 4 194 304 bits (524 288 words by 8 bits) CMOS static RAM.

The μ PD434008 is packed in 36-pin plastic SOJ.

Features

- 524 288 words by 8 bits organization
- Fast access time 20 ns (MAX.)
- \overline{OE} input for easy application

Ordering Information

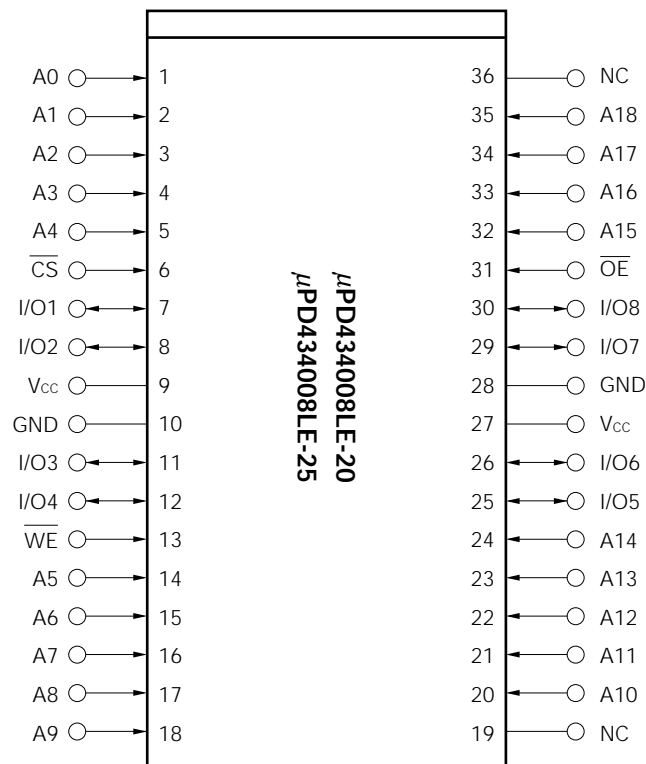
Part number	Package	Access time ns (MAX.)	Operating supply current mA (MAX.)	Standby supply current mA (MAX.)	Quality grade
μ PD434008LE-20	36-pin plastic SOJ (400 mil)	20	190	10	Standard
μ PD434008LE-25		25	170		

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

The information in this document is subject to change without notice.

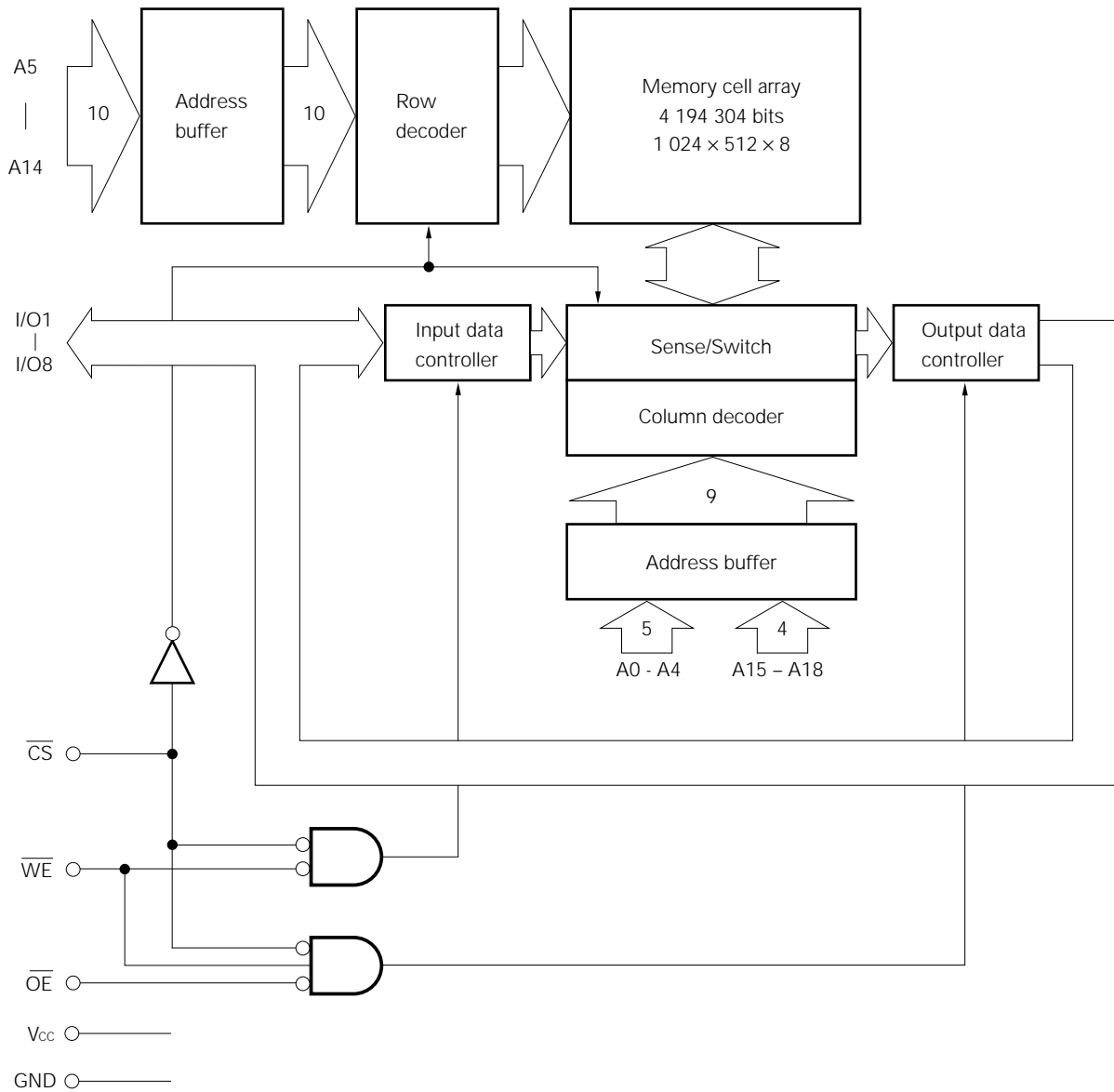
Pin Configuration (Marking Side)

36-pin plastic SOJ (400 mil)



- A0 – A18 : Address inputs
- I/O1 – I/O8 : Data inputs/outputs
- $\overline{\text{CS}}$: Chip Select
- $\overline{\text{WE}}$: Write Enable
- $\overline{\text{OE}}$: Output Enable
- Vcc : Power supply
- GND : Ground
- NC : No connection

Block Diagram



Truth Table

\overline{CS}	\overline{OE}	\overline{WE}	Mode	I/O	Supply current
H	X	X	Not selected	Hi-Z	I_{cc}
L	H	H	Output disable		
L	L	H	Read	D _{OUT}	I_{cc}
L	X	L	Write	D _{IN}	

Remark X : Don't care

Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 ^{Note} to +7.0	V
Input/Output voltage	V _T	-0.5 ^{Note} to V _{CC} +0.3	V
Operating temperature	T _{opt}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +125	°C

Note -2.0 V (MIN.) (Pulse width: 10 ns)

Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
High level input voltage	V _{IH}	2.2		V _{CC} +0.3	V
Low level input voltage	V _{IL}	-0.5 ^{Note}		+0.8	V
Ambient temperature	T _a	0		+70	°C

Note -2.0 V (MIN.) (Pulse width: 10 ns)

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input leakage current	I _{LI}	V _{IN} = 0 V to V _{CC}	-2		+2	μA
Output leakage current	I _{LO}	V _{I/O} = 0 V to V _{CC} , $\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$	-2		+2	μA
Operating supply current	I _{CC}	$\overline{CS} = V_{IL}$, I _{I/O} = 0 mA, Minimum cycle time	μPD434008-20		190	mA
			μPD434008-25		170	
Standby supply current	I _{SB}	$\overline{CS} = V_{IH}$, Minimum cycle time	μPD434008-20		60	mA
			μPD434008-25		50	
	I _{SB1}	V _{CC} - 0.2 V $\leq \overline{CS}$, V _{IN} \leq 0.2 V or V _{CC} - 0.2 V \leq V _{IN}			10	
High level output voltage	V _{OH}	I _{OH} = -4.0 mA	2.4			V
Low level output voltage	V _{OL}	I _{OL} = 8 mA			0.4	V

Remark V_{IN}: Input voltage

Capacitance (T_a = +25 °C, f = 1 MHz)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C _{IN}	V _{IN} = 0 V			6	pF
Input/Output capacitance	C _{I/O}	V _{I/O} = 0 V			10	pF

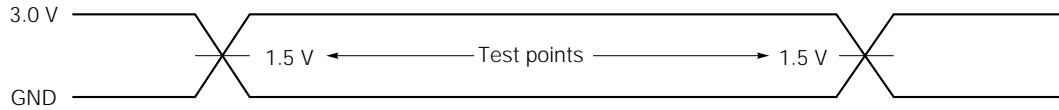
Remark 1. V_{IN}: Input voltage

2. These parameters are periodically sampled and not 100 % tested.

AC Characteristics (Recommended operating conditions unless otherwise noted)

AC Test Conditions

Input waveform (Rise/fall time ≤ 3 ns)

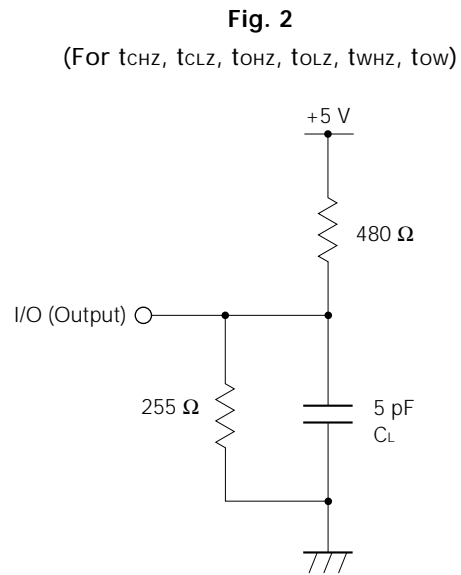
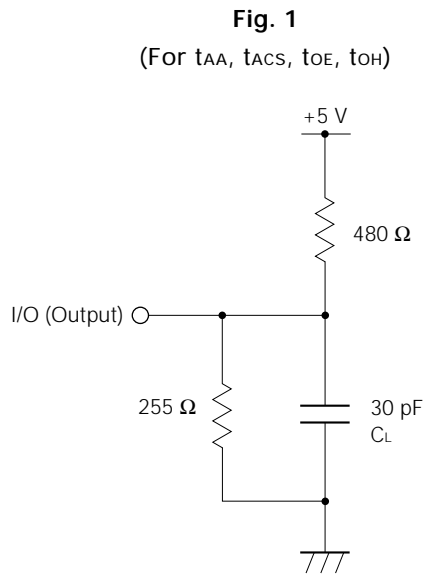


Output waveform



Output load

AC Characteristics directed with the note should be measured with the output load shown in Fig. 1 or Fig. 2.



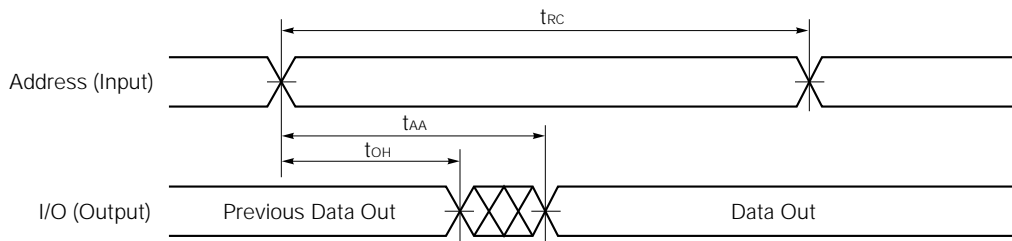
Remark C_L includes capacitances of the probe and jig, and stray capacitances.

Read Cycle

Parameter	Symbol	μPD434008LE-20		μPD434008LE-25		Unit	Condition
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	20		25		ns	
Address access time	t_{AA}		20		25	ns	Note 1.
\overline{CS} access time	t_{ACS}		20		25	ns	
\overline{OE} access time	t_{OE}		10		12	ns	
Output hold from address change	t_{OH}	3		3		ns	
\overline{CS} to output in low impedance	t_{CLZ}	3		3		ns	Note 2.
\overline{OE} to output in low impedance	t_{OLZ}	0		0		ns	
\overline{CS} to output in high impedance	t_{CHZ}		8		10	ns	
\overline{OE} to output in high impedance	t_{OHZ}		8		10	ns	

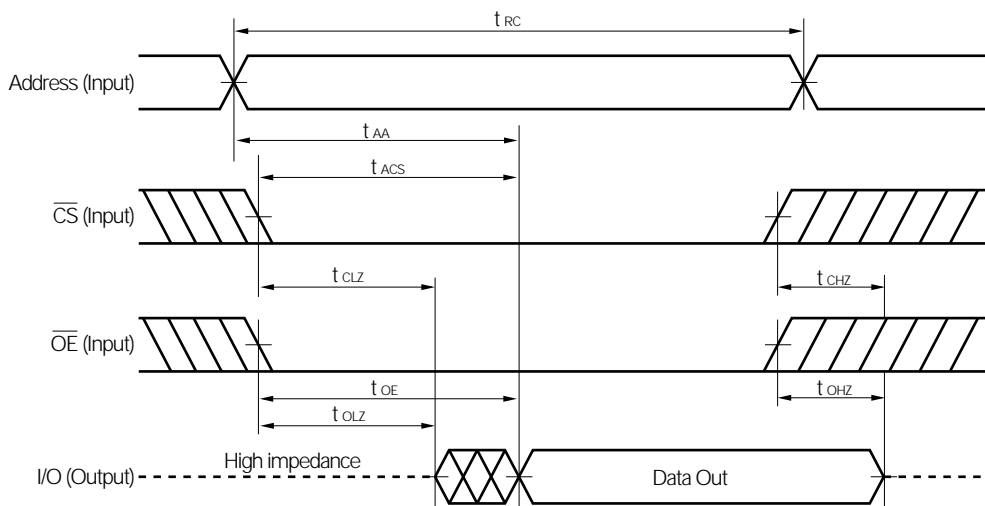
- Note 1.** See the output load shown in Fig. 1.
Note 2. See the output load shown in Fig. 2.

Read Cycle Timing Chart 1 (Address Access)



- Remark 1.** In read cycle, \overline{WE} should be fixed to high level.
2. $\overline{CS} = \overline{OE} = V_{IL}$

Read Cycle Timing Chart 2 (\overline{CS} Access)



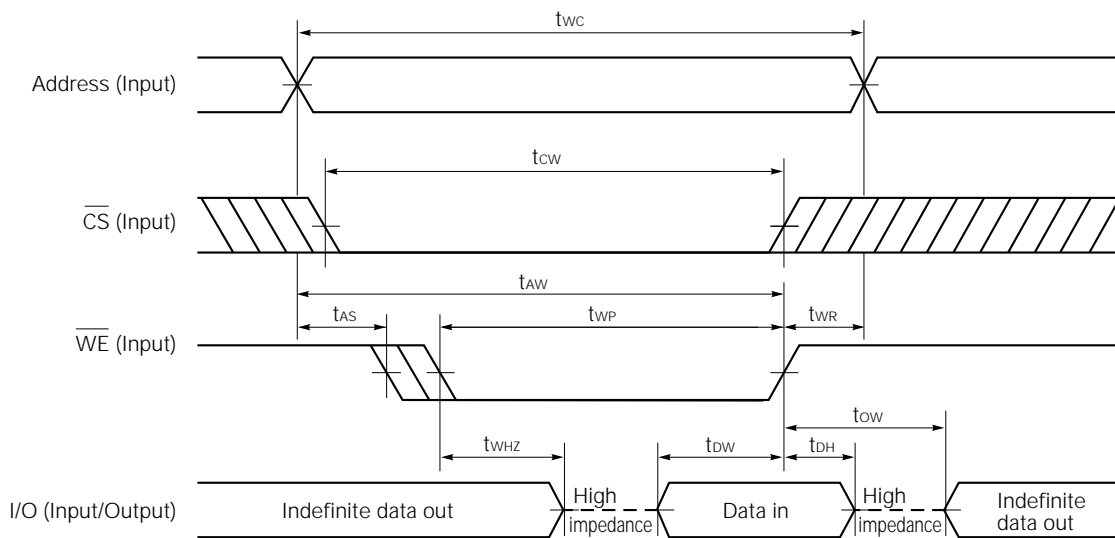
- Caution** Address valid prior to or coincident with \overline{CS} low level input.
Remark In read cycle, \overline{WE} should be fixed to high level.

Write Cycle

Parameter	Symbol	μPD434008LE-20		μPD434008LE-25		Unit	Condition
		MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{wc}	20		25		ns	
\overline{CS} to end of write	t_{cw}	14		17		ns	
Address valid to end of write	t_{aw}	14		17		ns	
Write pulse width	t_{wp}	12		15		ns	
Data valid to end of write	t_{dw}	10		12		ns	
Data hold time	t_{dh}	0		0		ns	
Address setup time	t_{as}	0		0		ns	
Write recovery time	t_{wr}	3		3		ns	
\overline{WE} to output in high impedance	t_{whz}		8		10	ns	Note
Output active from end of write	t_{ow}	0		0		ns	

Note See the output load shown in Fig. 2.

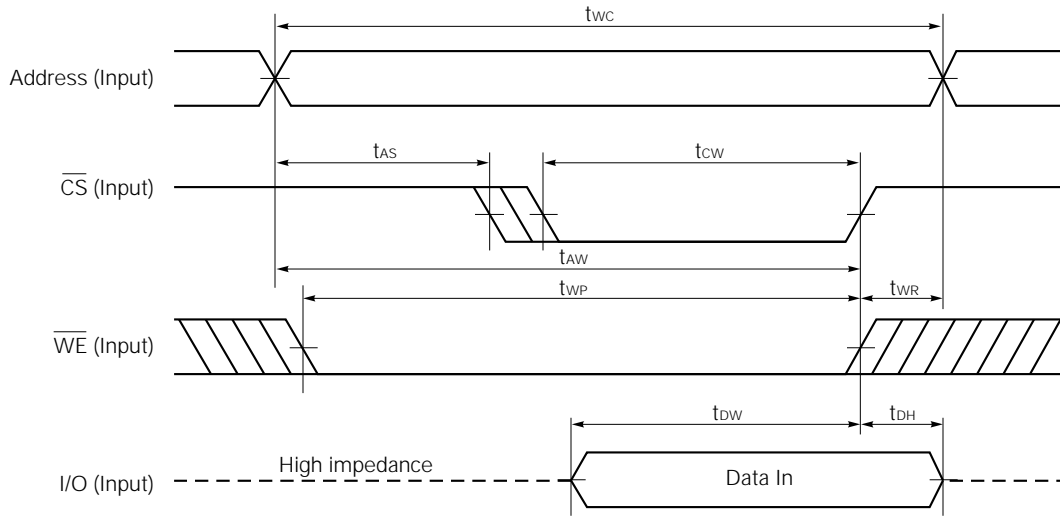
Write Cycle Timing Chart 1 (\overline{WE} Controlled)



Caution \overline{WE} should be fixed to high level during address transition.

- Remark 1. Write operation is done during the overlap time of a low level \overline{CS} and a low level \overline{WE} .
- When \overline{WE} is at low level, I/O pins are always high impedance. When \overline{WE} is at high level, read operation is executed. Therefore \overline{OE} should be high level to make I/O pins high impedance.
 - t_{wr} is measured between rising edge of \overline{CS} or \overline{WE} , whichever occurs first, and end of t_{wc} .
 - t_{whz} is measured at $V_{OL} + 200$ mV and $V_{OH} - 200$ mV with the output load shown in Fig. 2.
 - t_{ow} is measured at ± 200 mV from steady state voltage with the output load shown in Fig. 2.

★ Write Cycle Timing Chart 2 (\overline{CS} Controlled)

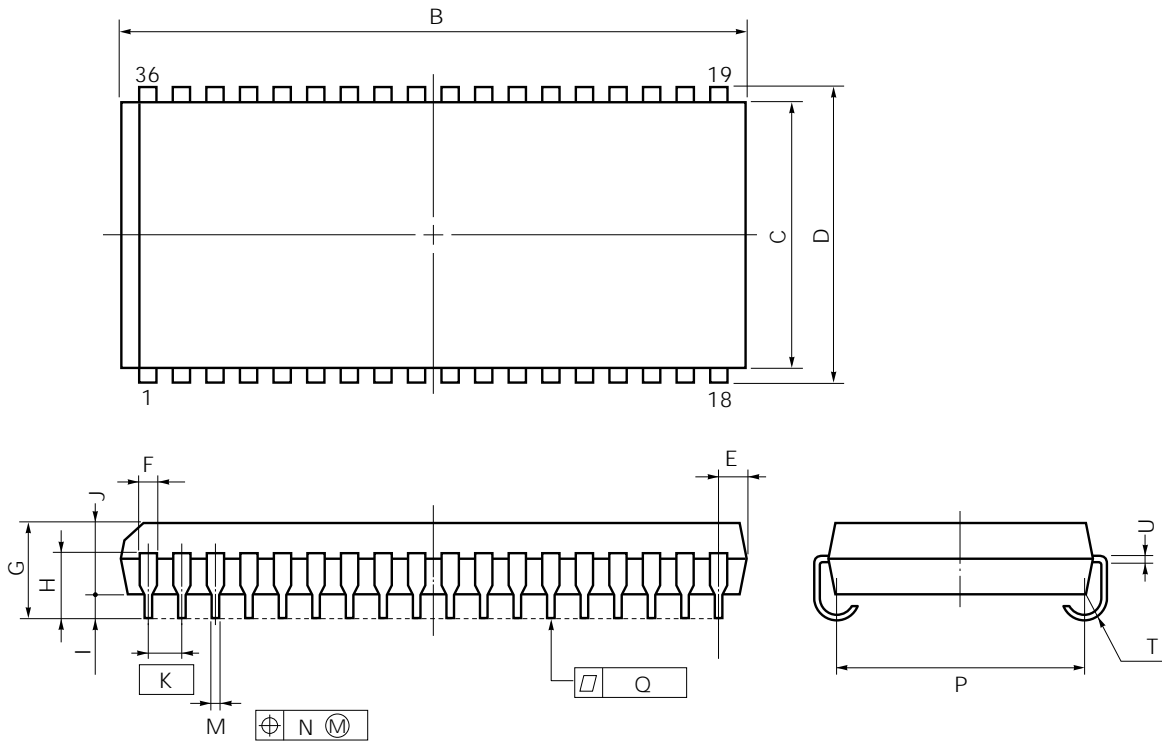


Caution \overline{CS} should be fixed to high level during address transition.

- Remark**
1. Write operation is done during the overlap time of a low level \overline{CS} and a low level \overline{WE} .
 2. t_{WR} is measured between rising edge of \overline{CS} or \overline{WE} , whichever occurs first, and end of t_{wc} .
 3. t_{WHZ} is measured at $V_{OL} + 200\text{ mV}$ and $V_{OH} - 200\text{ mV}$ with the output load shown in Fig. 2.

Package Drawing

36 PIN PLASTIC SOJ (400 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P36LE-400A

ITEM	MILLIMETERS	INCHES
B	23.6±0.2	0.929±0.008
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.005±0.1	0.040 ^{+0.004} _{-0.005}
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.1	0.004
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

★ RECOMMENDED SOLDERING CONDITIONS

Please consult with our sales offices for soldering conditions of the μ PD434008.

TYPE OF SURFACE MOUNT DEVICE

μ PD434008LE: 36-pin plastic SOJ (400 mil)

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Corporation. NEC Corporation assumes no responsibility for any errors which may appear in this document.

NEC Corporation does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from use of a device described herein or any other liability arising from use of such device. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Corporation or others.

The devices listed in this document are not suitable for use in aerospace equipment, submarine cables, nuclear reactor control systems and life support systems. If customers intend to use NEC devices for above applications or they intend to use "Standard" quality grade NEC devices for applications not intended by NEC, please contact our sales people in advance.

Application examples recommended by NEC Corporation

Standard: Computer, Office equipment, Communication equipment, Test and Measurement equipment, Machine tools, Industrial robots, Audio and Visual equipment, Other consumer products, etc.

Special: Automotive and Transportation equipment, Traffic control systems, Antidisaster systems, Anticrime systems, etc.