NEC

MOS INTEGRATED CIRCUIT

μPD442002-X

2M-BIT CMOS STATIC RAM
128K-WORD BY 16-BIT
EXTENDED TEMPERATURE OPERATION

Description

The μPD442002-X is a high speed, low power, 2,097,152 bits (131,072 words by 16 bits) CMOS static RAM.

The μPD442002-X is packed in 48-pin TAPE FBGA.

Features

- 131,072 words by 16 bits organization
- ★ • Fast access time : 50, 55, 70, 85, 100, 120 ns (MAX.)
- Byte data control : /LB (I/O1 - I/O8), /UB (I/O9 - I/O16)
- Low voltage operation

  (BB version : V_{CC} = 2.7 to 3.6 V, BC version : V_{CC} = 2.2 to 3.6 V, DD version : V_{CC} = 1.8 to 2.2 V)
- Low V_{CC} data retention : 1.0 V (MIN.)
- Operating ambient temperature : T_A = –25 to +85 °C
- Output Enable input for easy application

	Part number	Access time ns (MAX.)	Operating supply voltage V	Operating ambient temperature °C	Supply current		
					At operating mA (MAX.)	At standby μA (MAX.)	At data retention μA (MAX.)
★	μPD442002-BBxxX	50 Note 1, 55, 70, 85	2.7 to 3.6	–25 to +85	30 Note 2 35 Note 3 40 Note 4	4	2
	μPD442002-BCxxX	70, 85, 100	2.2 to 3.6		30		
★	μPD442002-DDxxX	85, 100, 120	1.8 to 2.2		15	3	

★ **Notes 1.** $V_{CC} \geq$ 3.0 V

★ **2.** Cycle time ≥ 70 ns

★ **3.** Cycle time = 55 ns

★ **4.** Cycle time = 50 ns

Document No. M14670EJ6V0DS00 (6th edition)
Date Published July 2001 NS CP (K)
Printed in Japan

The mark ★ shows major revised points.

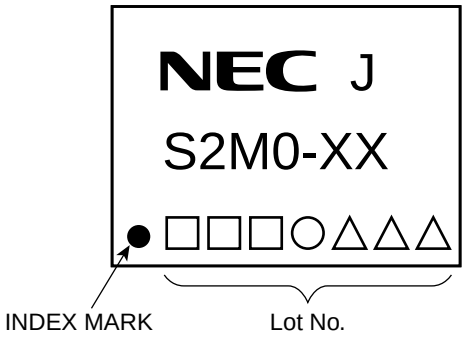
Ordering Information

Part number	Package	Access time ns (MAX.)	Operating supply voltage V	Operating temperature °C	Remark
★ μPD442002F9-BB55X-BC1	48-pin TAPE FBGA (6×8)	55, 50 Note	2.7 to 3.6	–25 to +85	BB version
μPD442002F9-BB70X-BC1		70			
μPD442002F9-BB85X-BC1		85			
μPD442002F9-BC70X-BC1		70	2.2 to 3.6		BC version
μPD442002F9-BC85X-BC1		85			
μPD442002F9-BC10X-BC1		100			
μPD442002F9-DD85X-BC1		85	1.8 to 2.2		DD version
μPD442002F9-DD10X-BC1		100			
μPD442002F9-DD12X-BC1		120			

★ **Note** $V_{CC} \geq 3.0$ V

Marking Image

Part number	Marking (XX)
μPD442002F9-BB55X-BC1	B1
μPD442002F9-BB70X-BC1	B2
μPD442002F9-BB85X-BC1	B3
μPD442002F9-BC70X-BC1	C2
μPD442002F9-BC85X-BC1	C3
μPD442002F9-BC10X-BC1	C4
μPD442002F9-DD85X-BC1	D3
μPD442002F9-DD10X-BC1	D4
μPD442002F9-DD12X-BC1	D5



Pin Configuration

/xxx indicates active low signal.

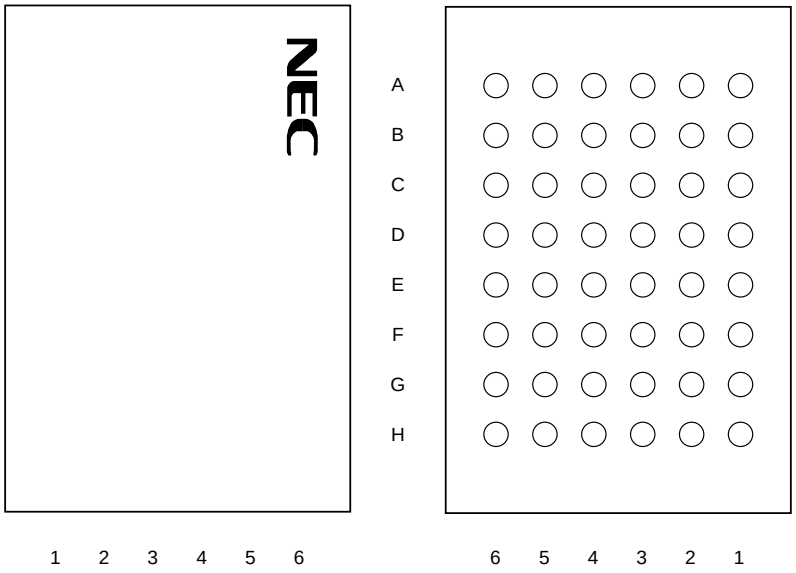
48-pin TAPE FBGA (6×8)

[μPD442002F9-BBxxX-BC1]

[μPD442002F9-BCxxX-BC1]

[μPD442002F9-DDxxX-BC1]

Top View **Bottom View**



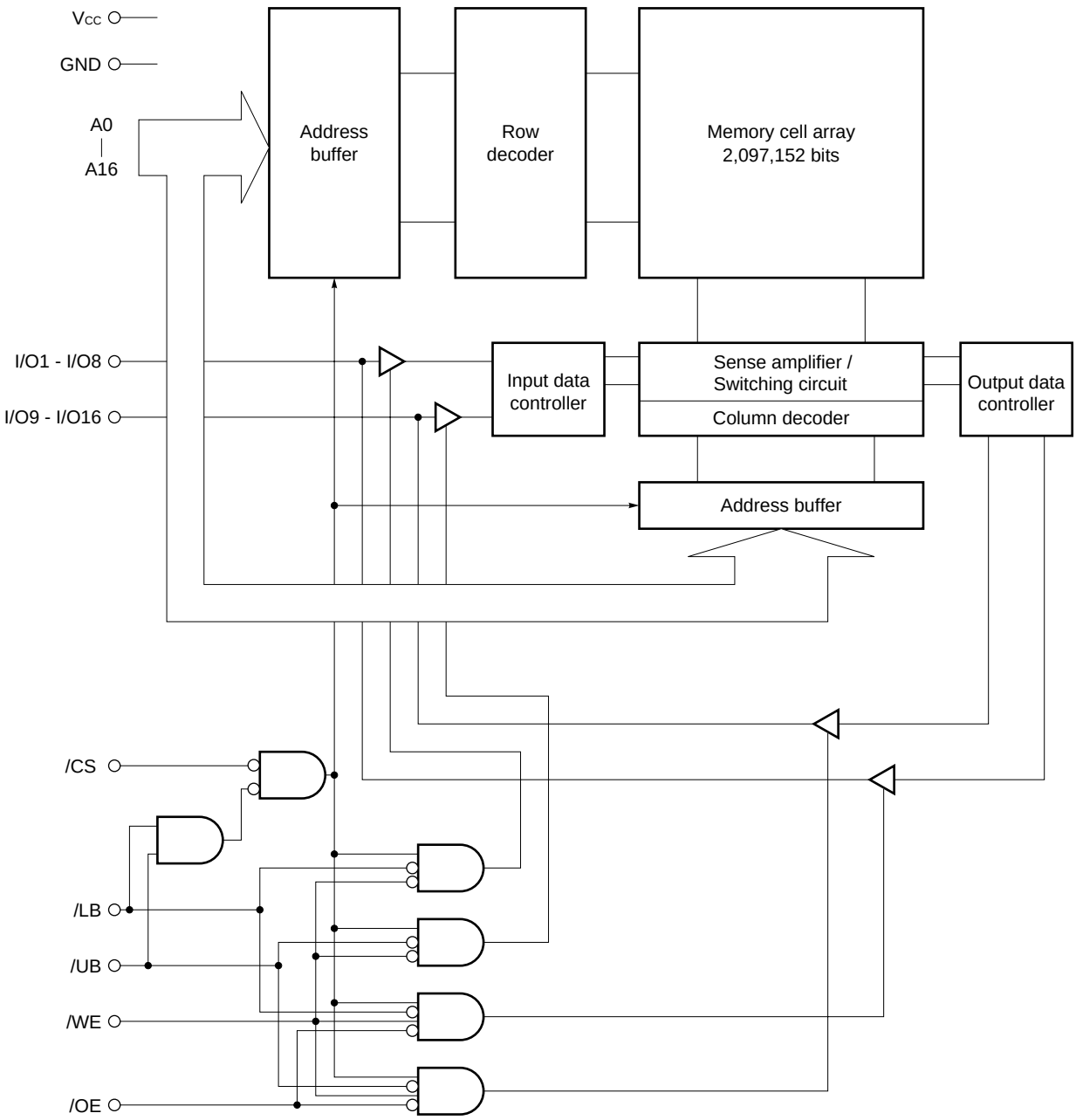
	1	2	3	4	5	6
A	/LB	/OE	A0	A1	A2	NC
B	I/O9	/UB	A3	A4	/CS	I/O1
C	I/O10	I/O11	A5	A6	I/O2	I/O3
D	GND	I/O12	NC	A7	I/O4	V_{CC}
E	V_{CC}	I/O13	NC	A16	I/O5	GND
F	I/O15	I/O14	A14	A15	I/O6	I/O7
G	I/O16	NC	A12	A13	/WE	I/O8
H	NC	A8	A9	A10	A11	NC

	6	5	4	3	2	1
A	NC	A2	A1	A0	/OE	/LB
B	I/O1	/CS	A4	A3	/UB	I/O9
C	I/O3	I/O2	A6	A5	I/O11	I/O10
D	V_{CC}	I/O4	A7	NC	I/O12	GND
E	GND	I/O5	A16	NC	I/O13	V_{CC}
F	I/O7	I/O6	A15	A14	I/O14	I/O15
G	I/O8	/WE	A13	A12	NC	I/O16
H	NC	A11	A10	A9	A8	NC

A0 - A16 : Address inputs
I/O1 - I/O16 : Data inputs / outputs
/CS : Chip Select
/WE : Write Enable
/OE : Output Enable
/LB, /UB : Byte data select
V_{CC} : Power supply
GND : Ground
NC : No Connection

Remark Refer to **Package Drawing** for the index mark.

Block Diagram



Truth Table

/CS	/OE	/WE	/LB	/UB	Mode	I/O		Supply current
						I/O1 - I/O8	I/O9 - I/O16	
H	×	×	×	×	Not selected	High impedance	High impedance	I_{SB}
×	×	×	H	H	Not selected	High impedance	High impedance	
L	H	H	L	×	Output disable	High impedance	High impedance	I_{CCA}
			×	L	Output disable	High impedance	High impedance	
	L	H	L	L	Word read	D_{OUT}	D_{OUT}	
			L	H	Lower byte read	D_{OUT}	High impedance	
			H	L	Upper byte read	High impedance	D_{OUT}	
	×	L	L	L	Word write	D_{IN}	D_{IN}	
			L	H	Lower byte write	D_{IN}	High impedance	
			H	L	Upper byte write	High impedance	D_{IN}	

Remark × : V_{IH} or V_{IL}

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Product	Rating	Unit
Supply voltage	V_{CC}	μPD442002-BBxxX, μPD442002-BCxxX	–0.5 Note to +4.0	V
		μPD442002-DDxxX	–0.5 Note to +2.7	
Input / Output voltage	V_T	μPD442002-BBxxX, μPD442002-BCxxX	–0.5 Note to V_{CC}+0.4 (4.0 V MAX.)	V
		μPD442002-DDxxX	–0.5 Note to V_{CC}+0.4 (2.7 V MAX.)	
Operating ambient temperature	T_A		–25 to +85	°C
Storage temperature	T_{stg}		–55 to +125	°C

Note –3.0 V (MIN.) (Pulse width : 30 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	μPD442002-BBxxX		μPD442002-BCxxX		μPD442002-DDxxX		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Supply voltage	V_{CC}		2.7	3.6	2.2	3.6	1.8	2.2	V
High level input voltage	V_{IH}	2.7 V ≤ V_{CC} ≤ 3.6 V	2.4	V_{CC}+0.4	2.4	V_{CC}+0.4	–	–	V
		2.2 V ≤ V_{CC} < 2.7 V	–	–	2.0	V_{CC}+0.3	–	–	
		1.8 V ≤ V_{CC} < 2.2 V	–	–	–	–	1.6	V_{CC}+0.2	
Low level input voltage	V_{IL}		–0.3 Note	+0.5	–0.3 Note	+0.4	–0.2 Note	+0.2	V
Operating ambient temperature	T_A		–25	+85	–25	+85	–25	+85	°C

Note –1.0 V (MIN.) (Pulse width : 20 ns)

Capacitance (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			8	pF
Input / Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

Remarks 1. V_{IN} : Input voltage

$V_{I/O}$: Input / Output voltage

2. These parameters are not 100% tested.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted) (1/2)

	Parameter	Symbol	Test condition		μPD442002-BBxxX			Unit
					MIN.	TYP.	MAX.	
	Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}		–1.0		+1.0	μA
	I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}, /CS = V_{IH} or /WE = V_{IL} or /OE = V_{IH}		–1.0		+1.0	μA
★	Operating supply current	I_{CCA1}	/CS = V_{IL},	Cycle time = 50 ns		–	40	mA
			$I_{I/O}$ = 0 mA,	Cycle time = 55 ns		–	35	
			Minimum cycle time	Cycle time ≥ 70 ns		–	30	
★		I_{CCA2}	/CS = V_{IL}, $I_{I/O}$ = 0 mA, Cycle time = ∞			–	4	
★		I_{CCA3}	/CS ≤ 0.2 V, Cycle time = 1 μs, $I_{I/O}$ = 0 mA, V_{IL} ≤ 0.2 V, V_{IH} ≥ V_{CC} – 0.2 V			–	4	
	Standby supply current	I_{SB}	/CS = V_{IH} or /LB = /UB = V_{IH}			–	0.6	mA
		I_{SB1}	/CS ≥ V_{CC} – 0.2 V			0.3	4	μA
		I_{SB2}	/LB = /UB ≥ V_{CC} – 0.2 V, /CS ≤ 0.2 V			0.3	4	
	High level output voltage	V_{OH}	I_{OH} = –0.5 mA		2.4			V
	Low level output voltage	V_{OL}	I_{OL} = 1.0 mA				0.4	V

Remarks 1. V_{IN} : Input voltage

$V_{I/O}$: Input / Output voltage

2. These DC characteristics are in common regardless of product classification.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted) (2/2)

Parameter	Symbol	Test condition		μPD442002-BCxxX			μPD442002-DDxxX			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}		–1.0		+1.0	–1.0		+1.0	μA
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}, /CS = V_{IH} or /WE = V_{IL} or /OE = V_{IH}		–1.0		+1.0	–1.0		+1.0	μA
Operating supply current	I_{CCA1}	/CS = V_{IL}, $I_{I/O}$ = 0 mA,			–	30		–	–	mA
★		Minimum cycle time	V_{CC} ≤ 2.7 V		–	25		–	–	
★			V_{CC} ≤ 2.2 V		–	–		–	15	
★	I_{CCA2}	/CS = V_{IL}, $I_{I/O}$ = 0 mA,			–	4		–	–	
★		Cycle time = ∞	V_{CC} ≤ 2.7 V		–	2		–	–	
★			V_{CC} ≤ 2.2 V		–	–		–	1	
★	I_{CCA3}	/CS ≤ 0.2 V, Cycle time = 1 μs,			–	4		–	–	
★		$I_{I/O}$ = 0 mA, V_{IL} ≤ 0.2 V,	V_{CC} ≤ 2.7 V		–	3		–	–	
★		V_{IH} ≥ V_{CC} – 0.2 V	V_{CC} ≤ 2.2 V		–	–		–	3	
Standby supply current	I_{SB}	/CS = V_{IH} or /LB = /UB = V_{IH}			–	0.6		–	–	mA
			V_{CC} ≤ 2.7 V		–	0.6		–	–	
			V_{CC} ≤ 2.2 V		–	–		–	0.6	
	I_{SB1}	/CS ≥ V_{CC} – 0.2 V			0.3	4		–	–	μA
			V_{CC} ≤ 2.7 V		0.25	3.5		–	–	
			V_{CC} ≤ 2.2 V		–	–		0.2	3	
	I_{SB2}	/LB = /UB ≥ V_{CC} – 0.2 V,			0.3	4		–	–	
		/CS ≤ 0.2 V	V_{CC} ≤ 2.7 V		0.25	3.5		–	–	
			V_{CC} ≤ 2.2 V		–	–		0.2	3	
High level output voltage	V_{OH}	I_{OH} = –0.5 mA		2.4			–			V
			V_{CC} ≤ 2.7 V	1.8			–			
			V_{CC} ≤ 2.2 V	–			1.5			
Low level output voltage	V_{OL}	I_{OL} = 1.0 mA				0.4			–	V
			V_{CC} ≤ 2.7 V			0.4			–	
			V_{CC} ≤ 2.2 V			–			0.4	

Remarks 1. V_{IN} : Input voltage

$V_{I/O}$: Input / Output voltage

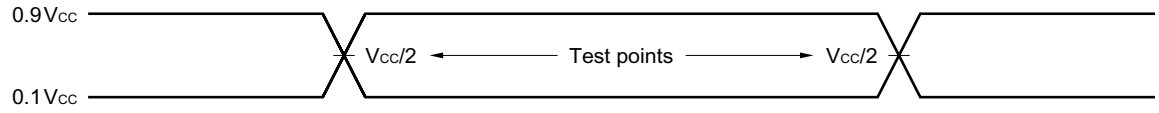
2. These DC characteristics are in common regardless of product classification.

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

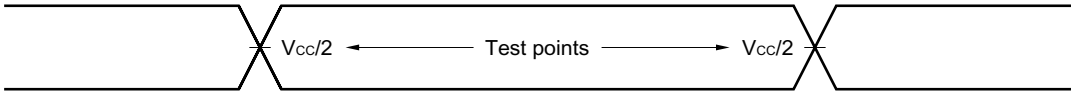
AC Test Conditions

[μPD442002-BB55X, μPD442002-BB70X, μPD442002-BB85X]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform

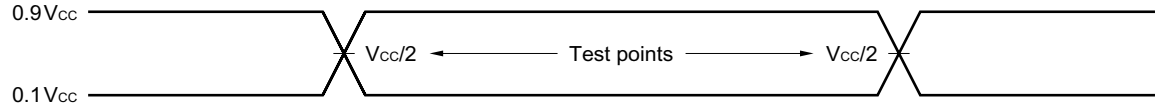


Output Load

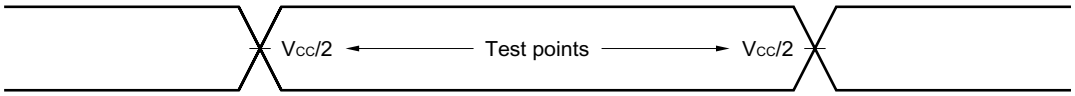
1TTL + 50 pF

[μPD442002-BC70X, μPD442002-BC85X, μPD442002-BC10X]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform

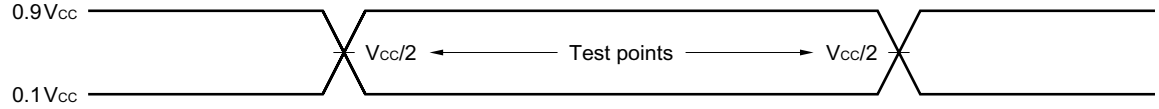


Output Load

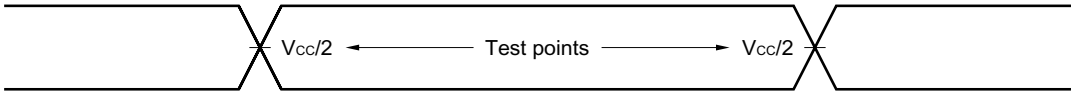
1TTL + 30 pF

[μPD442002-DD85X, μPD442002-DD10X, μPD442002-DD12X]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform



Output Load

1TTL + 30 pF

★ **Read Cycle (1/3) (BB version)**

Parameter	Symbol	μPD442002-BB55X				μPD442002 -BB70X		μPD442002 -BB85X		Unit	Condition
		$V_{CC} \geq 3.0$ V									
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	50		55		70		85		ns	
Address access time	t_{AA}		50		55		70		85	ns	**Note 1**
/CS access time	t_{ACS}		50		55		70		85	ns	
/OE to output valid	t_{OE}		30		30		35		40	ns	
/LB, /UB to output valid	t_{BA}		50		55		70		85	ns	
Output hold from address change	t_{OH}	10		10		10		10		ns	
/CS to output in low impedance	t_{LZ}	10		10		10		10		ns	**Note 2**
/OE to output in low impedance	t_{OLZ}	5		5		5		5		ns	
/LB, /UB to output in low impedance	t_{BLZ}	10		10		10		10		ns	
/CS to output in high impedance	t_{HZ}		20		20		25		30	ns	
/OE to output in high impedance	t_{OHZ}		20		20		25		30	ns	
/LB, /UB to output in high impedance	t_{BHZ}		20		20		25		30	ns	

Notes 1. The output load is 1TTL + 50 pF.

2. The output load is 1TTL + 5 pF.

Read Cycle (2/3) (BC version)

Parameter	Symbol	μPD442002 -BC70X		μPD442002 -BC85X		μPD442002 -BC10X		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	70		85		100		ns	
Address access time	t_{AA}		70		85		100	ns	**Note 1**
/CS access time	t_{ACS}		70		85		100	ns	
/OE to output valid	t_{OE}		35		40		50	ns	
/LB, /UB to output valid	t_{BA}		70		85		100	ns	
Output hold from address change	t_{OH}	10		10		10		ns	
/CS to output in low impedance	t_{LZ}	10		10		10		ns	**Note 2**
/OE to output in low impedance	t_{OLZ}	5		5		5		ns	
/LB, /UB to output in low impedance	t_{BLZ}	10		10		10		ns	
/CS to output in high impedance	t_{HZ}		25		30		35	ns	
/OE to output in high impedance	t_{OHZ}		25		30		35	ns	
/LB, /UB to output in high impedance	t_{BHZ}		25		30		35	ns	

Notes 1. The output load is 1TTL + 30 pF.

2. The output load is 1TTL + 5 pF.

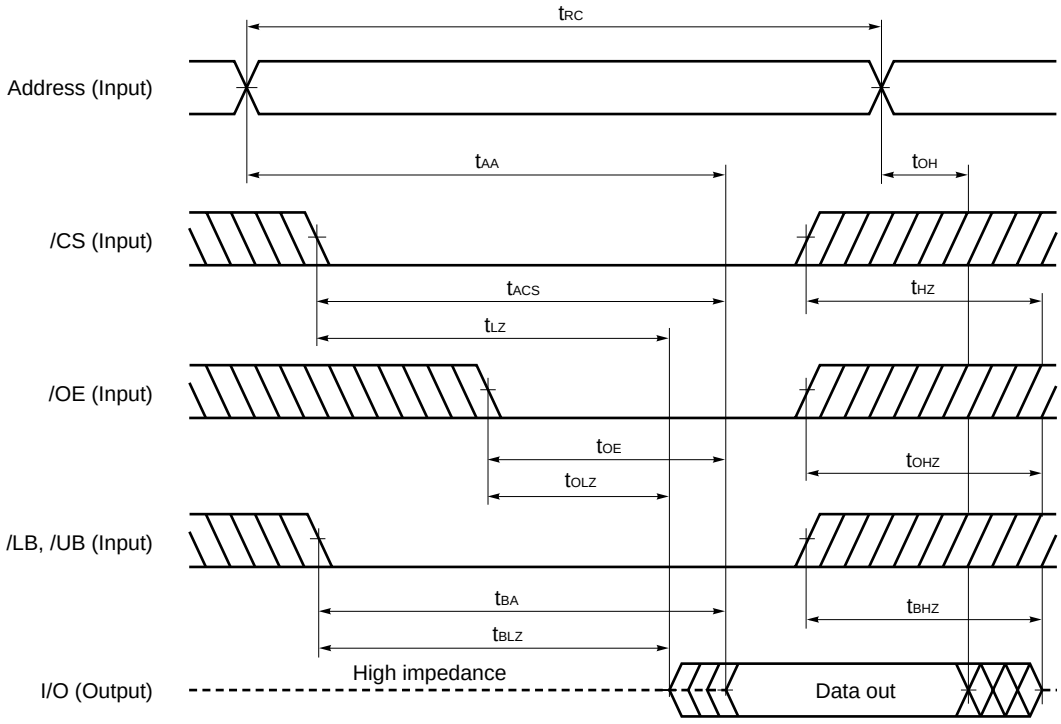
Read Cycle (3/3) (DD version)

Parameter	Symbol	μPD442002 -DD85X		μPD442002 -DD10X		μPD442002 -DD12X		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	85		100		120		ns	
Address access time	t_{AA}		85		100		120	ns	**Note 1**
/CS access time	t_{ACS}		85		100		120	ns	
/OE to output valid	t_{OE}		40		50		60	ns	
/LB, /UB to output valid	t_{BA}		85		100		120	ns	
Output hold from address change	t_{OH}	10		10		10		ns	
/CS to output in low impedance	t_{LZ}	10		10		10		ns	**Note 2**
/OE to output in low impedance	t_{OLZ}	5		5		5		ns	
/LB, /UB to output in low impedance	t_{BLZ}	10		10		10		ns	
/CS to output in high impedance	t_{HZ}		30		35		40	ns	
/OE to output in high impedance	t_{OHZ}		30		35		40	ns	
/LB, /UB to output in high impedance	t_{BHZ}		30		35		40	ns	

Notes 1. The output load is 1TTL + 30 pF.

2. The output load is 1TTL + 5 pF.

Read Cycle Timing Chart



Remark In read cycle, /WE should be fixed to high level.

★ **Write Cycle (1/3) (BB version)**

Parameter	Symbol	μPD442002-BB55X				μPD442002 -BB70X		μPD442002 -BB85X		Unit	Condition
		$V_{CC} \geq 3.0$ V									
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	50		55		70		85		ns	
/CS to end of write	t_{CW}	45		50		55		70		ns	
/LB, /UB to end of write	t_{BW}	45		50		55		70		ns	
Address valid to end of write	t_{AW}	45		50		55		70		ns	
Address setup time	t_{AS}	0		0		0		0		ns	
Write pulse width	t_{WP}	40		45		50		55		ns	
Write recovery time	t_{WR}	0		0		0		0		ns	
Data valid to end of write	t_{DW}	25		25		30		35		ns	
Data hold time	t_{DH}	0		0		0		0		ns	
/WE to output in high impedance	t_{WHZ}		20		20		25		30	ns	**Note**
Output active from end of write	t_{OW}	5		5		5		5		ns	

Note The output load is 1TTL + 5 pF.

Write Cycle (2/3) (BC version)

Parameter	Symbol	μPD442002 -BC70X		μPD442002 -BC85X		μPD442002 -BC10X		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	70		85		100		ns	
/CS to end of write	t_{CW}	55		70		80		ns	
/LB, /UB to end of write	t_{BW}	55		70		80		ns	
Address valid to end of write	t_{AW}	55		70		80		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	50		55		60		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	30		35		40		ns	
Data hold time	t_{DH}	0		0		0		ns	
/WE to output in high impedance	t_{WHZ}		25		30		35	ns	**Note**
Output active from end of write	t_{OW}	5		5		5		ns	

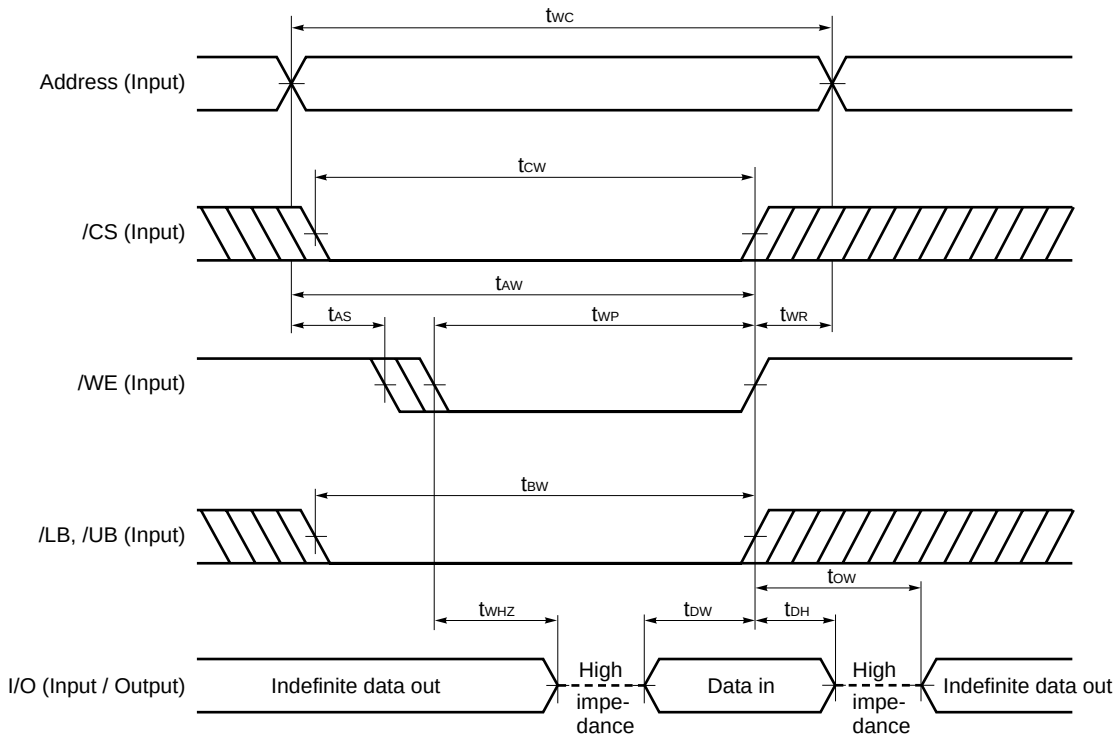
Note The output load is 1TTL + 5 pF.

Write Cycle (3/3) (DD version)

Parameter	Symbol	μPD442002 -DD85X		μPD442002 -DD10X		μPD442002 -DD12X		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	85		100		120		ns	
/CS to end of write	t_{CW}	70		80		100		ns	
/LB, /UB to end of write	t_{BW}	70		80		100		ns	
Address valid to end of write	t_{AW}	70		80		100		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	55		60		85		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	35		40		60		ns	
Data hold time	t_{DH}	0		0		0		ns	
/WE to output in high impedance	t_{WHZ}		30		35		40	ns	**Note**
Output active from end of write	t_{OW}	5		5		5		ns	

Note The output load is 1TTL + 5 pF.

Write Cycle Timing Chart 1 (/WE Controlled)



Cautions 1. During address transition, at least one of pins /CS, /WE should be inactivated.

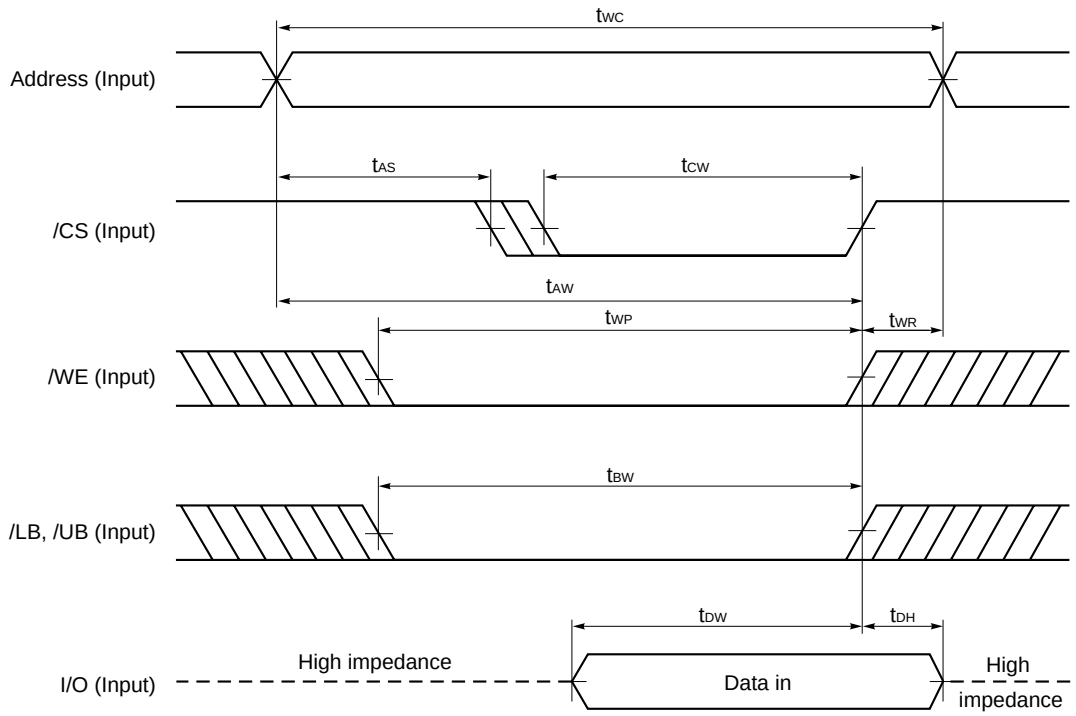
2. Do not input data to the I/O pins while they are in the output state.

Remarks 1. Write operation is done during the overlap time of a low level /CS, a low level /WE and a low level /LB (or low level /UB).

2. If /CS changes to low level at the same time or after the change of /WE to low level, the I/O pins will remain high impedance state.

3. When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

Write Cycle Timing Chart 2 (/CS Controlled)

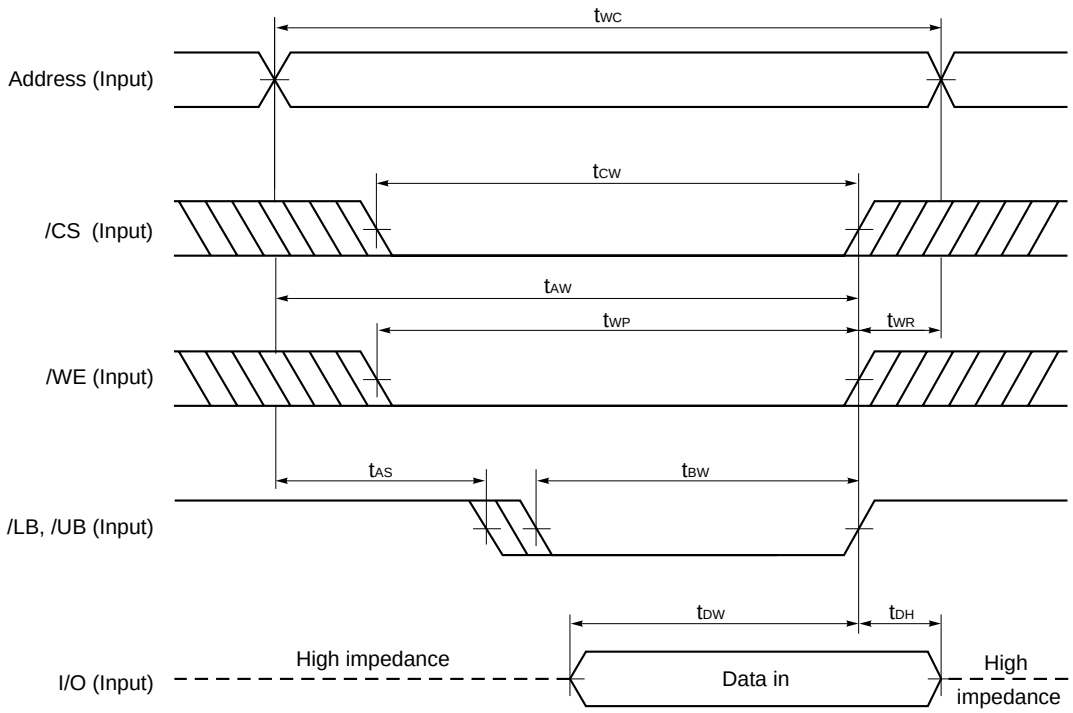


Cautions 1. During address transition, at least one of pins /CS, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

Remark Write operation is done during the overlap time of a low level /CS, a low level /WE and a low level /LB (or low level /UB).

Write Cycle Timing Chart 3 (/LB, /UB Controlled)



Cautions 1. During address transition, at least one of pins /CS, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

Remark Write operation is done during the overlap time of a low level /CS, a low level /WE and a low level /LB (or low level /UB).

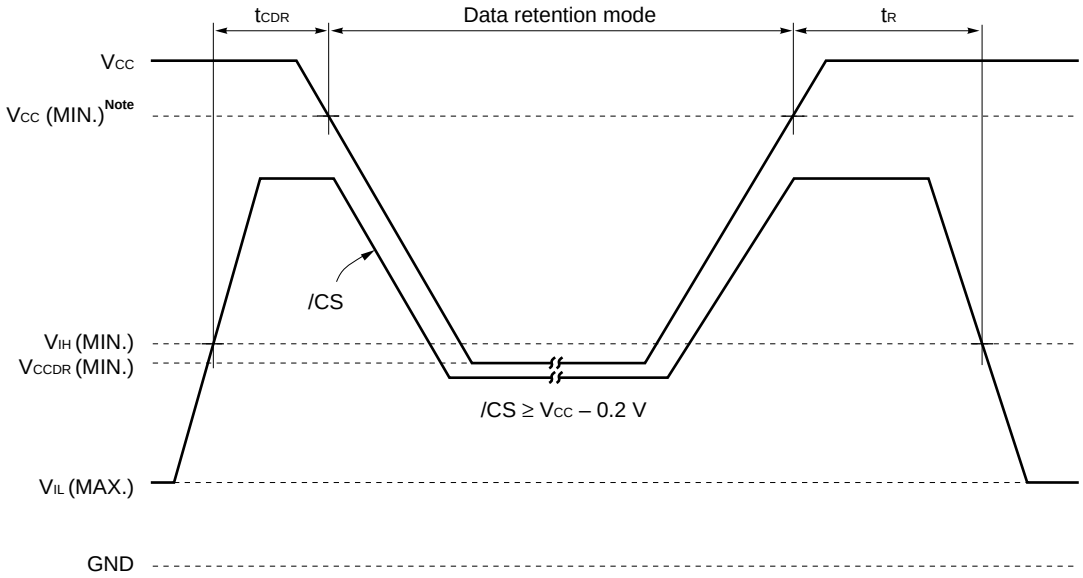
Low V_{CC} Data Retention Characteristics (T_A = –25 to +85°C)

Parameter	Symbol	Test Condition	μPD442002 -BBxxX			μPD442002 -BCxxX			μPD442002 -DDxxX			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Data retention supply voltage	V_{CCDR1}	/CS ≥ V_{CC} – 0.2 V	1.0		3.6	1.0		3.6	1.0		2.2	V
	V_{CCDR2}	/LB = /UB ≥ V_{CC} – 0.2 V, /CS ≤ 0.2 V	1.0		3.6	1.0		3.6	1.0		2.2	
Data retention supply current	I_{CCDR1}	V_{CC} = 1.2 V, /CS ≥ V_{CC} – 0.2 V		0.15	2		0.15	2		0.15	2	μA
	I_{CCDR2}	V_{CC} = 1.2 V, /LB = /UB ≥ V_{CC} – 0.2 V, /CS ≤ 0.2 V		0.15	2		0.15	2		0.15	2	
Chip deselection to data retention mode	t_{CDR}		0			0			0			ns
Operation recovery time	t_R		t_{RC} Note			t_{RC} Note			t_{RC} Note			ns

Note t_{RC} : Read cycle time

Data Retention Timing Chart

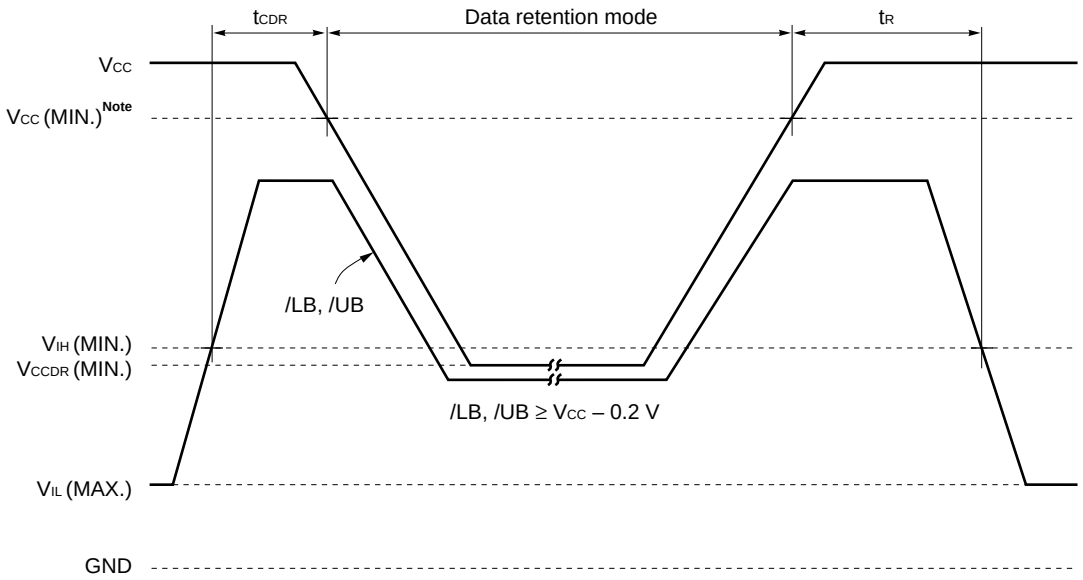
(1) /CS Controlled



Note BB version : 2.7 V, BC version : 2.2 V, DD version : 1.8 V

Remark On the data retention mode by controlling /CS, the other pins (Address, I/O, /WE, /OE, /LB, /UB) can be in high impedance state.

(2) /LB, /UB Controlled

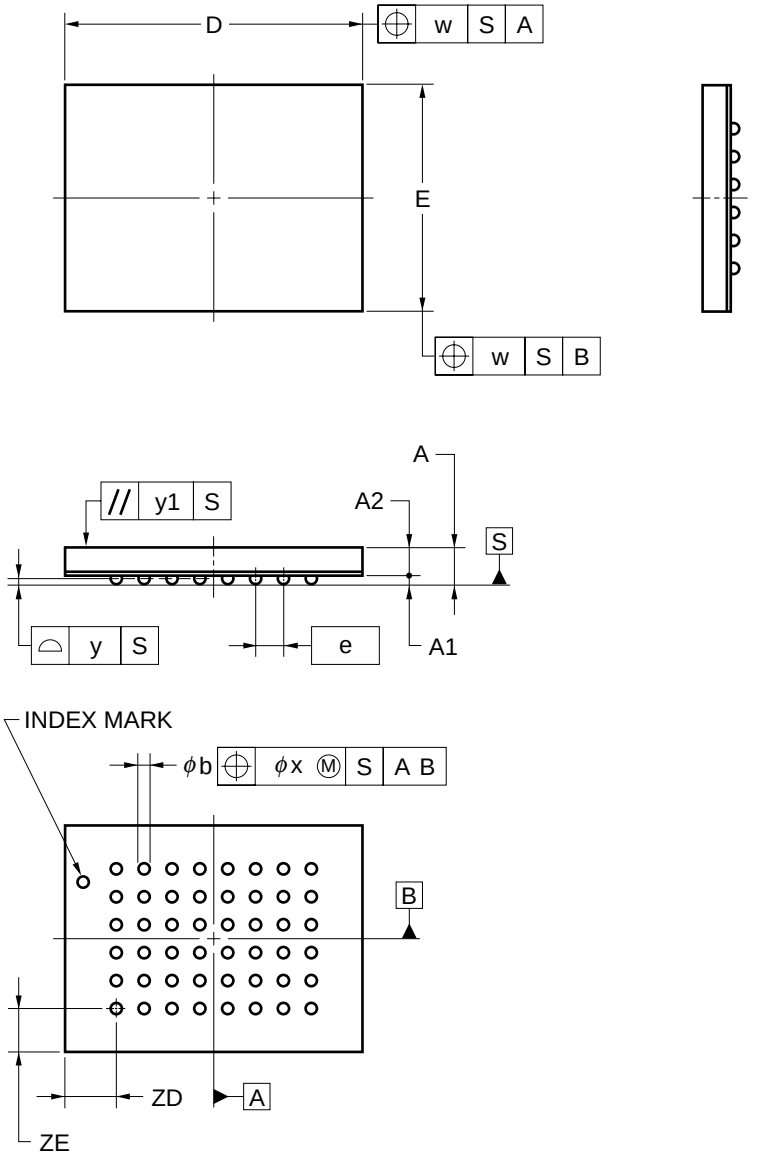


Note BB version : 2.7 V, BC version : 2.2 V, DD version : 1.8 V

Remark On the data retention mode by controlling /LB and /UB, the input level of /CS must be ≥ V_{CC} – 0.2 V or ≤ 0.2 V. The other pins (Address, I/O, /WE, /OE) can be in high impedance state.

Package Drawing

48-PIN TAPE FBGA (6x8)



ITEM	MILLIMETERS
D	8.0±0.1
E	6.0±0.1
w	0.2
e	0.75
A	0.96±0.10
A1	0.25±0.05
A2	0.71
b	0.35±0.05
x	0.08
y	0.1
y1	0.1
ZD	1.375
ZE	1.125

P48F9-75-BC1-1

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD442002-X.

Types of Surface Mount Device

μPD442002F9-BBxxX-BC1 : 48-pin TAPE FBGA (6x8)

μPD442002F9-BCxxX-BC1 : 48-pin TAPE FBGA (6x8)

μPD442002F9-DDxxX-BC1 : 48-pin TAPE FBGA (6x8)

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

- **The information in this document is current as of July, 2001. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC's data sheets or data books, etc., for the most up-to-date specifications of NEC semiconductor products. Not all products and/or types are available in every country. Please check with an NEC sales representative for availability and additional information.**
- No part of this document may be copied or reproduced in any form or by any means without prior written consent of NEC. NEC assumes no responsibility for any errors that may appear in this document.
- NEC does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC semiconductor products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC or others.
- Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of customer's equipment shall be done under the full responsibility of customer. NEC assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
- While NEC endeavours to enhance the quality, reliability and safety of NEC semiconductor products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC semiconductor products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment, and anti-failure features.
- NEC semiconductor products are classified into the following three quality grades:
  "Standard", "Special" and "Specific". The "Specific" quality grade applies only to semiconductor products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of a semiconductor product depend on its quality grade, as indicated below. Customers must check the quality grade of each semiconductor product before using it in a particular application.
  "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.
  The quality grade of NEC semiconductor products is "Standard" unless otherwise expressly specified in NEC's data sheets or data books, etc. If customers wish to use NEC semiconductor products in applications not intended by NEC, they must contact an NEC sales representative in advance to determine NEC's willingness to support a given application.
  (Note)
  (1) "NEC" as used in this statement means NEC Corporation and also includes its majority-owned subsidiaries.
  (2) "NEC semiconductor products" means any semiconductor product developed or manufactured by or for NEC (as defined above).

M8E 00.4