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ADVANCED ANALOG

VDAC 1850/1852

8-BIT, 80 MHz VIDEO DAC

FEATURES

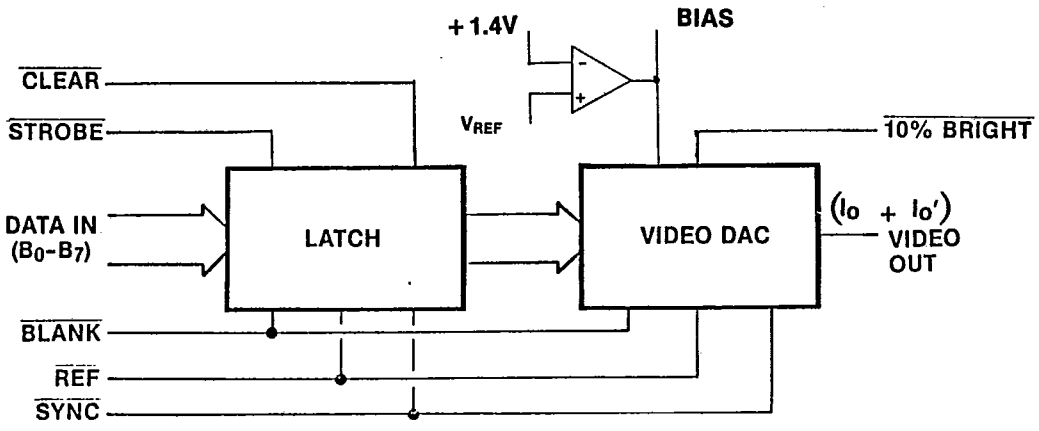
- CMOS CIRCUITRY
- UPDATE RATES TO 80MHz
- COMPOSITE SYNC and BLANKING OUTPUT SIGNALS
- INPUT DATA LATCHES
- CMOS/TTL COMPATIBLE INPUTS
- 20 or 24 PIN DIP PACKAGE
- SINGLE +5V SUPPLY
- ± 1 LSB NON-LINEARITY

DESCRIPTION

The VDAC-1850 and VDAC-1852 are monolithic, video speed digital-to-analog converters with 8-BITs of resolution. They contain latches for input data and produce a clean video output signal capable of driving 75Ω or 37.5Ω loads. Both models are also capable of producing composite sync and blanking signals plus reference black, reference white, and 10% bright. The VDAC-1850 is capable of accepting both binary or complementary binary coded data inputs while the VDAC-1852 operates on straight binary inputs. The VDAC-1850 has additional control pins to permit an adjustment of the composite sync, blanking and 10% bright output signal levels.

The DACs operate from a single positive 5V power supply and produces a standard 1V video output signal. The output circuitry may be connected to high voltage circuits to produce output voltage swings of up to 100V. The units are packaged in standard dual-in-line packages. The VDAC-1850 is a 24 pin DIP while the VDAC-1852 is in a 20 pin package.

BLOCK DIAGRAM



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SPECIFICATIONS

Typical @ +25°C, V_{DD} = +5V, R_L = 37.5[1]Ω I_O = 10 mA

ABSOLUTE MAXIMUM RATINGS	MIN	TYP	MAX	UNITS
Supply Voltage			6	V
Supply Current			60	mA
Full Scale Output Current (I_O)			40	mA
Drive Current (any pin)	−10		+10	mA
I_O, I_O', Voltage Range	−0.3		+2.5	V
Logic Input	V_{SS} − 0.3		V_{DD} + 0.3	V
I_O (VIDEO DAC OUTPUT)				
Max Current (@ V_O = 1.2V)		17.5	33	mA
Max Voltage (@ I_O = 10 mA			1.5	V
I_O'				
Blanking Current	0	1.4		mA
Sync Current	0	7.7		mA
10% Bright Current	0	1.9		mA
ACCURACY				
Absolute		± ½	±1	LSB
Linearity		± ½	±1	LSB
Offset Current			0.1	LSB
Voltage Reference	1.26	1.40	1.54	V
DYNAMIC CHARACTERISTICS				
Max Conversion Rate	75	80		MHz
Settling Time (to 0.5 LSB)		8		ns
Strobe Propogation Time		10		ns
Set-up Time	3			ns
Hold Time	0			ns
Glitch Energy		150		pV-s
Amplitude		60		mV
DIGITAL INPUTS				
Logic "0"	0		0.8	V
Logic "1"	2.0		V_{DD}	V
Compatibility	TTL/CMOS			
Coding	BINARY[2]			
POWER REQUIREMENTS				
Voltage	4.75	5	5.25	V
Current[3]		30	45	mA
TEMPERATURE RANGE				
Ambient	0		70	°C

NOTES: 1. 75Ω Resistor at I_O Pin and 75Ω load impedance in parallel.
2. VDAC-1850 operates on inverted binary with pin 16 at logic "1".
3. Includes 28 mA delivered to load.

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DEVICE OPERATION

The output of the VDAC-1850/1852 is a current source whose full scale value is set by an external resistor. This resistor is connected to an internal reference (1.4V nominal), and the current through the resistor represents 7 LSBs of output current. Thus, for a full scale current of 255 LSBs, $I_O = 1.4/R \times 255/7 = 51/R$, where I_O = full scale output current, R = current setting resistor (ohms). This resistor is connected from pin 21 to ground.

Example: $R_L = 37.5\Omega$, $I_O = .017$ ($V_O = 637.5$ mV from black to white level)

$$R = \frac{51}{I_O} = \frac{51}{0.017} = 3K$$

The value of R would be 6K nominal for $R_L = 75\Omega$, $I_O = .0085$

$$R = \frac{51}{.0085} = 6K$$

There is a separate pin (I_O') for the composite video signal. The output currents for composite sync, composite blank, and 10% bright are summed and appear at this pin (1). Normally I_O' is connected to pin 23, I_O. The three video signals have the following weighted values:

- Composite sync 112 LSB (40½ IRE)
- Composite blank 21 LSB (7½ IRE)
- 10% bright 28 LSB (10 IRE)

Note that these currents are ratioed to the 8-BIT DAC full scale current (255 LSBs).

PIN DESCRIPTIONS

DATA

These pins are the digital data inputs to the latch for the DAC. The inputs operate on normal TTL logic levels and the coding is binary. (The VDAC-1850 will accept inverted binary data if pin 16 is at logic "1".) The input data is transferred to the DAC when the strobe makes a HI to LO transition.

$\overline{\text{STROBE}}$

This input is used to clock the input data into the latch. Data is loaded into the latches at logic "1" and transferred from their outputs to the DAC inputs on a logic "1" to logic "0" transition.

$\overline{\text{SYNC}}$

A logic "0" clears the DAC (inputs all zeros) and turns off this current source (at I_O' pin) driving the output negative by 289 mV, with a normal configuration.

$\overline{\text{BLANK}}$

A logic "0" clears the DAC (inputs all zeros) and turns off this current source at I_O' pin) driving the output negative by 53 mV with a normal configuration.

I_O

This is the output of the 8-BIT Video DAC. It is a current output and has a full scale value of 92.5 IRE units or 17 mA (0.6375V) with a normal 37.5Ω load. The full scale output current value is programmable with an external resistor at the 1.4V pin. This output is normally tied to the I_O' pin to obtain video signals with composite sync, blanking and 10% bright output levels.

+1.4V

This pin is used to calibrate the gain of the 8-BIT VIDEO DAC. This is normally accomplished by connecting a resistor between it and ground. The value of the resistor is selected so that the current through it is equal to 7 LSBs of output current at I_O as described under DEVICE OPERATION.

I_O'

This pin contains the outputs for the current sources for the composite sync, composite blanking and 10% bright signals. It is normally summed with I_O pin to generate a video output which contains all these signals.

$\overline{\text{REF}}$

This input provides a convenient way to force the output of the DAC to go to "Ref-White" level. A logic "0" at this input will override the other inputs and cause the output to go to its full-scale level.

$\overline{\text{CLEAR}}$

This is a control pin that is synchronized with the clock. If CLEAR is pulled low, then the input latches will be set to zero when the clock goes high. When the clock then goes low, the zeros are transferred to the output latches and this sets the DAC output current to zero. This line must be kept low to override data, but REF will override it.

$\overline{\text{10\% BRIGHT}}$

A logic "0" turns on this current source at I_O' pin) boosting the output by 71 mV with a normal configuration. This input is normally used to generate extra brilliant pixels for a cursor, etc.

BIAS

Sets the current for the current sources. This line is driven by an internal amplifier. It can also be easily driven by an external source if desired. This line should be bypassed to V_{DD} with a .01μF capacitor.

INVERT (VDAC 1850 ONLY)

A logic "1" on this input complements the data inputs (B_0-B_7). It is used if the digital data inputs are inverted or complementary binary coded.

SADJ, CADJ, BADJ (VDAC 1850 ONLY)

These three lines may be used to adjust the output current levels of the 10% Bright, Composite Blanking and SYNC signals. For normal applications these circuits are not required and these pins may be left open. To adjust these current levels, connect a 10K potentiometer from V_{DD} to V_{SS}. Connect a 10K resistor from the center tap of the potentiometer to the adjustment pin desired.

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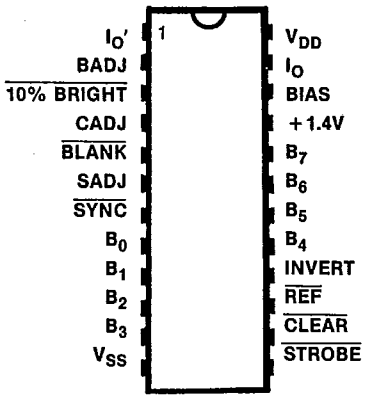
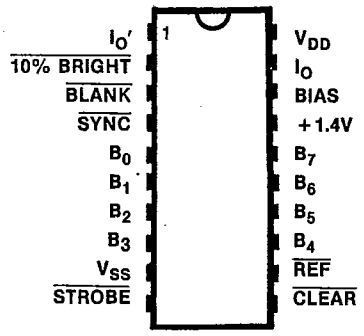
PIN DESIGNATION



VDAC-1850



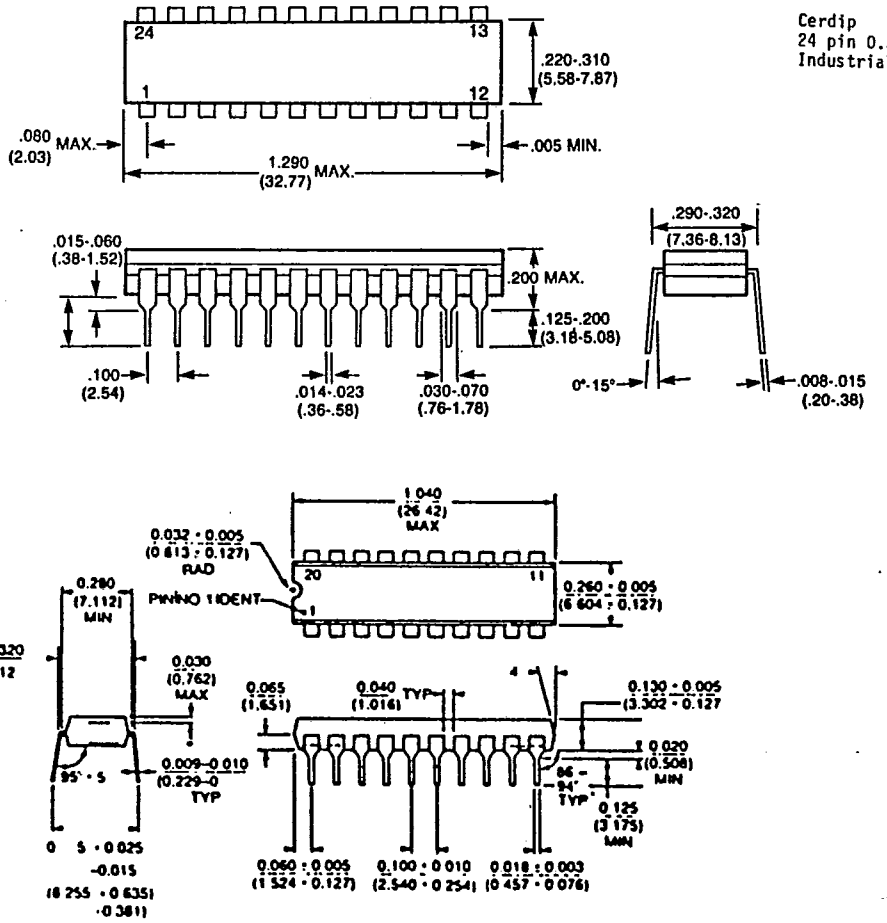
VDAC-1852

MECHANICAL OUTLINE

Ceramic VDAC-1850J

Plastic VDAC-1850N

Cerdip
24 pin 0.3" wide
Industrial



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The information in this data sheet has been carefully checked and is believed to be accurate, however, no responsibility is assumed for possible errors. The specifications are subject to change without notice.

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ADVANCED ANALOG
2270 MARTIN AVENUE, SANTA CLARA, CALIFORNIA 95050-2781
TELEPHONE (408) 988-4930
TWX 910-338-2218

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