Winbond Electronics Corp.

32K × 32 BURST PIPELINED HIGH-SPEED CMOS STATIC RAM

GENERAL DESCRIPTION

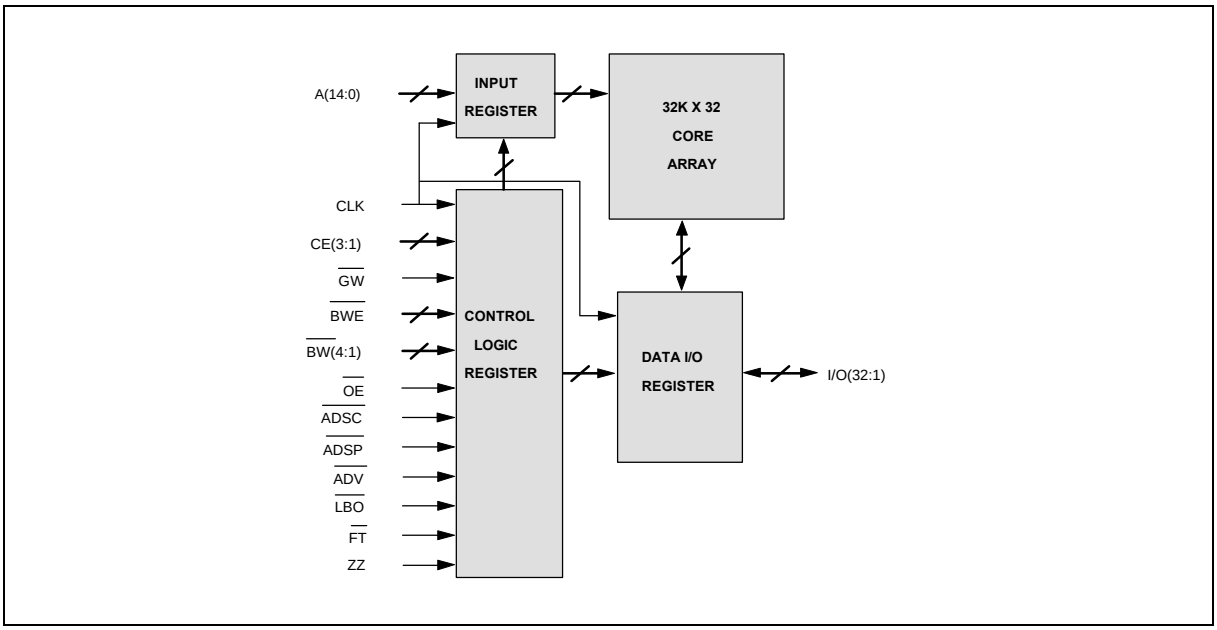
The W25P010A is a high-speed, low-power, synchronous-burst pipelined, CMOS static RAM organized as 32,768 × 32 bits that operates on a single 3.3-volt power supply. A built-in two-bit burst address counter supports both Pentium™ burst mode and linear burst mode. The mode to be executed is controlled by the ____ pin. Pipelining or non-pipelining of the data outputs is controlled by the ___

W25P010A support 2T/2T mode whcih will delay one cycle data output in a burst read cycle when the device is deselected by CE2 or $\overline{CE3}$. This mode supports 3-1-1-1-1-1-1-1 in a two-bank, back-to-back burst read cycle.

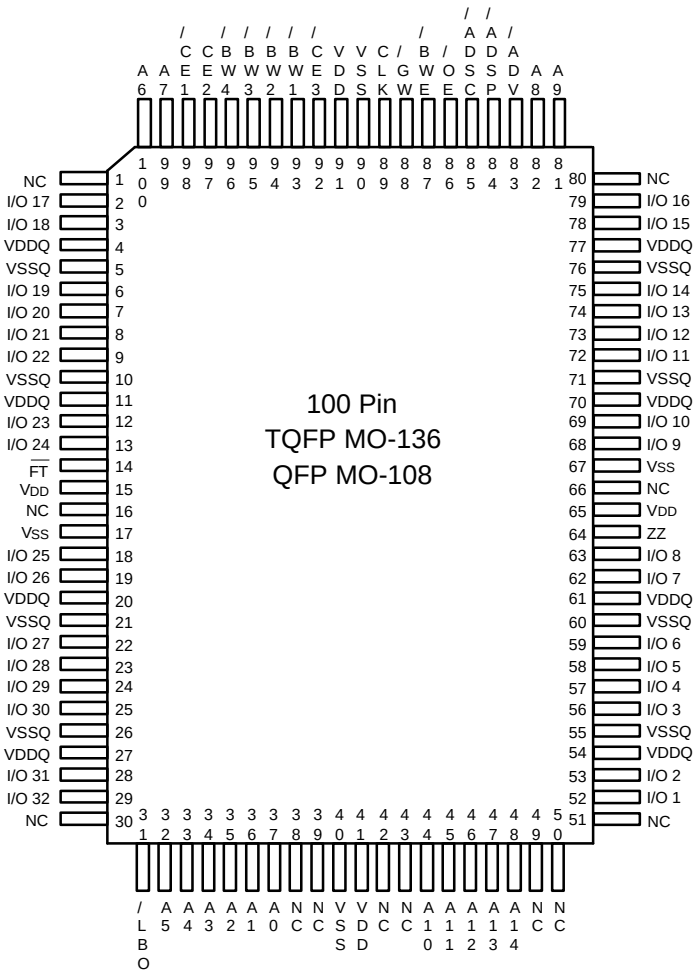
FEATURES

- Synchronous operation
- High-speed access time: 6/7/8 nS (max.)
- Single +3.3V power supply
- Individual byte write capability
- 3.3V LVTTL compatible I/O
- Clock-controlled and registered input
- Asynchronous output enable
- Pipelined/non-pipelined data output capability
- Supports snooze mode (low-power state)
- Internal burst counter supports Intel burst mode & linear burst mode
- Supports 2T/2T mode
- Packaged in 100-pin QFP and TQFP

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	TYPE	DESCRIPTION
A0–A14	Input, Synchronous	Host Address
I/O1–I/O32	I/O, Synchronous	Data Inputs/Outputs
CLK	Input, Clock	Processor Host Bus Clock
$\overline{CE1}$, CE2, $\overline{CE3}$	Input, Synchronous	Chip Enables
$\overline{GW}$	Input, Synchronous	Global Write
$\overline{BWE}$	Input, Synchronous	Byte Write Enable from Cache Controller
$\overline{BW1}$–$\overline{BW4}$	Input, Synchronous	Host Bus Byte Enables Used with $\overline{BWE}$
$\overline{OE}$	Input, Asynchronous	Output Enable Input
$\overline{ADV}$	Input, Synchronous	Internal Burst Address Counter Advance
$\overline{ADSC}$	Input, Synchronous	Address Status from Chip Set
$\overline{ADSP}$	Input, Synchronous	Address Status from CPU
ZZ	Input, Asynchronous	Snooze Pin for Low-power State, Internal Pull Low
$\overline{FT}$	Input, Static	Connected to V_{SSQ}: Device operates in flow-through (non-pipelined) mode. Connected to V_{DDQ} or unconnected: Device operates in pipelined mode.
$\overline{LBO}$	Input, Static	Lower Address Burst Order Connected to V_{SSQ}: Device is in linear mode. Connected to V_{DDQ} or unconnected: Device is in non-linear mode.
V_{DDQ}		I/O Power Supply
V_{SSQ}		I/O Ground
V_{DD}		Power Supply
V_{SS}		Ground
NC		No Connectiion

FUNCTIONAL DESCRIPTION

The W25P010A is a synchronous-burst pipelined, SRAM designed for use in high-end personal computers. It supports two burst address sequences for Intel™ systems and linear mode, which can be controlled by the $\overline{LBO}$ pin. The burst cycles are initiated by $\overline{ADSP}$ or $\overline{ADSC}$ and the burst counter is incremented whenever $\overline{ADV}$ is sampled low. The device can also be switched to non-pipelined mode if necessary.

BURST ADDRESS SEQUENCE

	INTEL SYSTEM ($\overline{LBO}$ = V_{DDQ})				LINEAR MODE ($\overline{LBO}$= V_{SSQ})			
	A[1:0]	A[1:0]	A[1:0]	A[1:0]	A[1:0]	A[1:0]	A[1:0]	A[1:0]
External Start Address	00	01	10	11	00	01	10	11
Second Address	01	00	11	10	01	10	11	00
Third Address	10	11	00	01	10	11	00	01
Fourth Address	11	10	01	00	11	00	01	10

The device supports several types of write mode operations. $\overline{BWE}$ and $\overline{BW}$[4:1] support individual byte writes. The $\overline{BE}$[7:0] signals can be directly connected to the SRAM $\overline{BW}$[4:1]. The $\overline{GW}$ signal is used to override the byte enable signals and allows the cache controller to write all bytes to the SRAM, no matter what the byte write enable signals are. The various write modes are indicated in the Write Table below. Note that in pipelined mode, the byte write enable signals are not latched by the SRAM with addresses but with data. In pipelined mode, the cache controller must ensure the SRAM latches both data and valid byte enable signals from the processor.

TRUTH TABLE

CYCLE	ADDRESS USED	$\overline{CE1}$	CE2	$\overline{CE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{OE}$	DATA	WRITE*
Unselected	No	1	X	X	X	0	X	X	Hi-Z	X
Unselected	No	0	X	1	0	X	X	X	Hi-Z	X
Unselected	No	0	0	X	0	X	X	X	Hi-Z	X
Unselected	No	0	X	1	1	0	X	X	Hi-Z	X
Unselected	No	0	0	X	1	0	X	X	Hi-Z	X
Begin Read	External	0	1	0	0	X	X	X	Hi-Z	X
Begin Read	External	0	1	0	1	0	X	X	Hi-Z	Read
Continue Read	Next	X	X	X	1	1	0	1	Hi-Z	Read
Continue Read	Next	X	X	X	1	1	0	0	D-Out	Read
Continue Read	Next	1	X	X	X	1	0	1	Hi-Z	Read
Continue Read	Next	1	X	X	X	1	0	0	D-Out	Read

Truth Table, continued

Suspend Read	Current	X	X	X	1	1	1	1	Hi-Z	Read
Suspend Read	Current	X	X	X	1	1	1	0	D-Out	Read
Suspend Read	Current	1	X	X	X	1	1	1	Hi-Z	Read
Suspend Read	Current	1	X	X	X	1	1	0	D-Out	Read
Begin Write	Current	X	X	X	1	1	1	X	Hi-Z	Write
Begin Write	Current	1	X	X	X	1	1	X	Hi-Z	Write
Begin Write	External	0	1	0	1	0	X	X	Hi-Z	Write
Continue Write	Next	X	X	X	1	1	0	X	Hi-Z	Write
Continue Write	Next	1	X	X	X	1	0	X	Hi-Z	Write
Suspend Write	Current	X	X	X	1	1	1	X	Hi-Z	Write
Suspend Write	Current	1	X	X	X	1	1	X	Hi-Z	Write

Notes:

1. For a detailed definition of read/write, see the Write Table below.

2. An "X" means don't care, "1" means logic high, and "0" means logic low.

3. The $\overline{OE}$ pin enables the data output but is not synchronous with the clock. All signals of the SRAM are sampled synchronous to the bus clock except for the $\overline{OE}$ pin.

4. On a write cycle that follows a read cycle, $\overline{OE}$ must be inactive prior to the start of write cycle to allow write data to setup he SRAM. $\overline{OE}$ must also disable the output buffer prior to the end of a write cycle to ensure the SRAM data hold timings are met.

WRITE TABLE

READ/WRITE FUNCTION	$\overline{GW}$	$\overline{BWE}$	$\overline{BW4}$	$\overline{BW3}$	$\overline{BW2}$	$\overline{BW1}$
Read	1	1	X	X	X	X
Read	1	0	1	1	1	1
Write byte 1 I/O1–I/O8	1	0	1	1	1	0
Write byte 2 I/O9–I/O16	1	0	1	1	0	1
Write byte 2, byte 1	1	0	1	1	0	0
Write byte 3 I/O17–I/O24	1	0	1	0	1	1
Write byte 3, byte 1	1	0	1	0	1	0
Write byte 3, byte 2	1	0	1	0	0	1
Write byte 3, byte 2, byte 1	1	0	1	0	0	0
Write byte 4 I/O25–I/O32	1	0	0	1	1	1
Write byte 4, byte 1	1	0	0	1	1	0

Write Table, continued

READ/WRITE FUNCTION	$\overline{GW}$	$\overline{BWE}$	$\overline{BW4}$	$\overline{BW3}$	$\overline{BW2}$	$\overline{BW1}$
Write byte 4, byte 2	1	0	0	1	0	1
Write byte 4, byte 2, byte 1	1	0	0	1	0	0
Write byte 4, byte 3	1	0	0	0	1	1
Write byte 4, byte 3, byte 1	1	0	0	0	1	0
Write byte 4, byte 3, byte 2	1	0	0	0	0	1
Write all bytes I/O–I/O32	1	0	0	0	0	0
Write all bytes I/O1–I/O32	0	X	X	X	X	X

The ZZ state is a low-power state in which the device consumes less power than in the Unselected mode. Enabling the ZZ pin for a fixed period of time will force the SRAM into the ZZ state. Pulling the ZZ pin low for a set period of time will wake up the SRAM again. While the SRAM is in ZZ mode, data retention is guaranteed, but the chip will not monitor any input signal except for the ZZ pin. In the Unselected mode, on the other hand, all the input signals are monitored.

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Core Supply Voltage to V_{SS}	-0.5 to 4.6	V
I/O Supply Voltage to V_{SS}	-0.5 to 4.6	V
Input/Output to V_{SSQ} Potential	V_{SSQ} -0.5 to V_{DDQ} +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to 150	°C
Operating Temperature	0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(V_{DD}/V_{DDQ} = 3.15V to 3.6V, V_{SS}/V_{SSQ} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Low Voltage	V_{IL}	-	-0.5	-	+0.8	V
Input High Voltage	V_{IH}	-	+2.0	-	V_{DD} +0.3	V
Input Leakage Current	I_{LI}	V_{IN} = V_{SSQ} to V_{DDQ}	-10	-	+10	µA
Output Leakage Current	I_{LO}	$V_{I/O}$ = V_{SSQ} to V_{DDQ}, and data I/O pins in high-Z state defined in truth table	-10	-	+ 10	µA
Output Low Voltage	V_{OL}	I_{OL} = +8.0 mA	-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0 mA	2.4	-	-	V
Operating Current	I_{DD}	$T_{CYC} \geq$ min., I/O = 0 mA	-	-	250	mA
Standby Current	I_{SBT}	Unselected mode defined in truth table, V_{IN}, V_{IO} = V_{IH} (min.) /V_{IL} (max.) $T_{CYC} \geq$ min.	-	-	80	mA
	I_{SBC}	Unselected mode defined in truth table,V_{IN} = V_{DD} - 0.2V/0.2V $T_{CYC} \geq$ min	-	-	10	mA
ZZ Mode Current	I_{ZZ}	ZZ mode, $T_{CYC} \geq$ min.	-	-	1	mA

Note: Typical characteristics are measured at V_{DD} = 3.3V, T_A = 25° C.

CAPACITANCE

(V_{DD} = 3.3V, T_A = 25° C, f = 1 MHz)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0V	8	pF

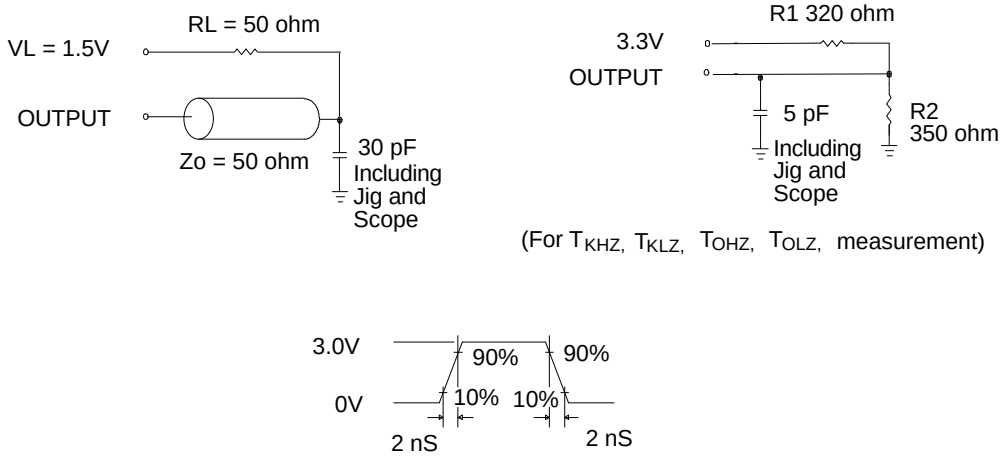
Note: These parameters are sampled but not 100% tested.

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	2 nS
Input and Output Timing Reference Level	1.5V
Output Load	C_L = 30 pF, I_{OH}/I_{OL} = -4 mA/8 mA

AC Test Loads and Waveform



AC Timing Characteristics

(V_{DD}/V_{DDQ} = 3.15V to 3.6V, V_{SS}/V_{SSQ} = 0V, T_A = 0 to 70° C, all timings measured in pipelined mode)

PARAMETER	SYM.	W25P010A-6		W25P010A-7		W25P010A-8		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Add. Setup Time	T_{AS}	2.5	-	2.5	-	2.5	-	nS	
Add. Hold Time	T_{AH}	0.5	-	0.5	-	0.5	-	nS	
Write Data Setup Time	T_{DS}	2.5	-	2.5	-	2.5	-	nS	
Write Data Hold Time	T_{DH}	0.5	-	0.5	-	0.5	-	nS	
$\overline{ADV}$ Setup Time	T_{ADVS}	2.5	-	2.5	-	2.5	-	nS	
$\overline{ADV}$ Hold Time	T_{ADVH}	0.5	-	0.5	-	0.5	-	nS	
$\overline{ADSP}$ Setup Time	T_{ADSS}	2.5	-	2.5	-	2.5	-	nS	
$\overline{ADSP}$ Hold Time	T_{ADSH}	0.5	-	0.5	-	0.5	-	nS	
$\overline{ADSC}$ Setup Time	T_{ADCS}	2.5	-	2.5	-	2.5	-	nS	
$\overline{ADSC}$ Hold Time	T_{ADCH}	0.5	-	0.5	-	0.5	-	nS	
$\overline{CE1}$, CE2, $\overline{CE3}$ Setup Time	T_{CES}	2.5	-	2.5	-	2.5	-	nS	
$\overline{CE1}$, CE2, $\overline{CE3}$ Hold Time	T_{CEH}	0.5	-	0.5	-	0.5	-	nS	
$\overline{GW}$, $\overline{BWE}$ X Setup Time	T_{WS}	2.5	-	2.5	-	2.5	-	nS	

AC Timing Characteristics, continued

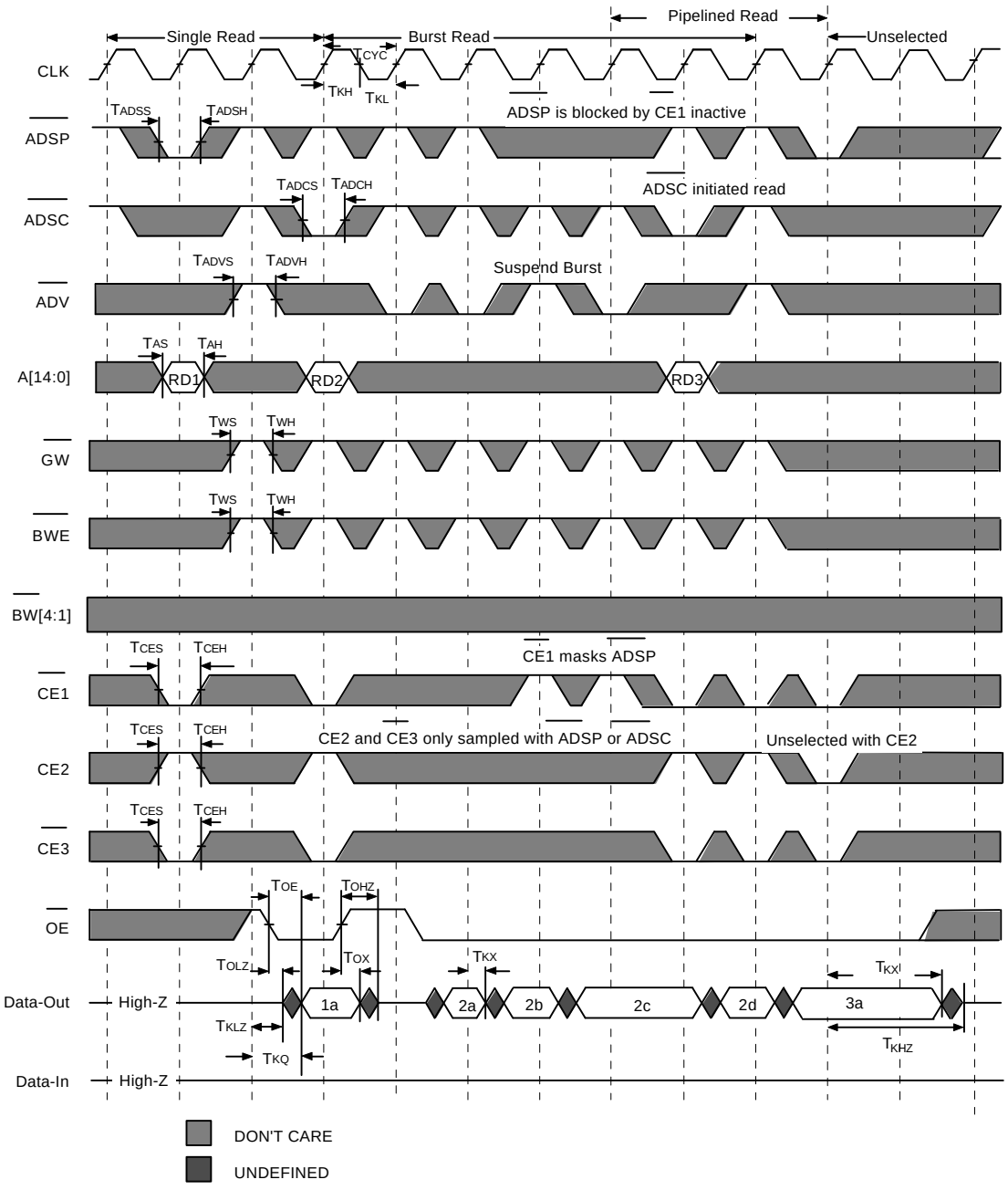
PARAMETER	SYM.	W25P010A-6		W25P010A-7		W25P010A-8		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{GW}$, $\overline{BWE}$ X Hold Time	TWH	0.5	-	0.5	-	0.5	-	nS	
Clock Cycle Time	TCYC	13.3	-	15	-	15	-	nS	
Clock High Pulse Width	TKH	5	-	6	-	6	-	nS	
Clock Low Pulse Width	TKL	5	-	6	-	6	-	nS	
Clock to Output Valid	TKQ	-	6	-	7	-	8	nS	
Clock to Output High-Z	TKHZ	2	13.3	2	15	2	15	nS	1, 5
		15.3	26.6	17	30	17	30	nS	1, 6
Clock to Output Low-Z	TKLZ	0	-	0	-	0	-	nS	1
Clock to Output Invalid	TKX	2	-	2	-	2	-	nS	1, 5
		15.3	-	17	-	17	-	nS	1, 6
Output Enable to Output Valid	TOE	-	6	-	7	-	8	nS	
Output Enable to Output High-Z	TOHZ	-	6	-	7	-	8	nS	1
Output Enable to Output Low-Z	TOLZ	0	-	0	-	0	-	nS	1
Output Enable to Output Invalid	TOX	0	-	0	-	0	-	nS	
ZZ Standby Time	TZZS	-	100	-	100	-	100	nS	2
ZZ Recover Time	TZZR	100	-	100	-	100	-	nS	3

Notes:

1. These parameters are sampled but not 100% tested
2. In the ZZ mode, the SRAM will enter a low-power state. In this mode, data retention is guaranteed and the clock is active.
3. $\overline{ADSC}$ and $\overline{ADSP}$ should not be accessed for at least 100 nS after chip leaves ZZ mode.
4. Configuring signals $\overline{LBO}$ and $\overline{FT}$ are static and should not be changed during operations.
5. Output datas are not controlled by CE2, $\overline{CE3}$.
6. Output datas are controlled by CE2, $\overline{CE3}$.

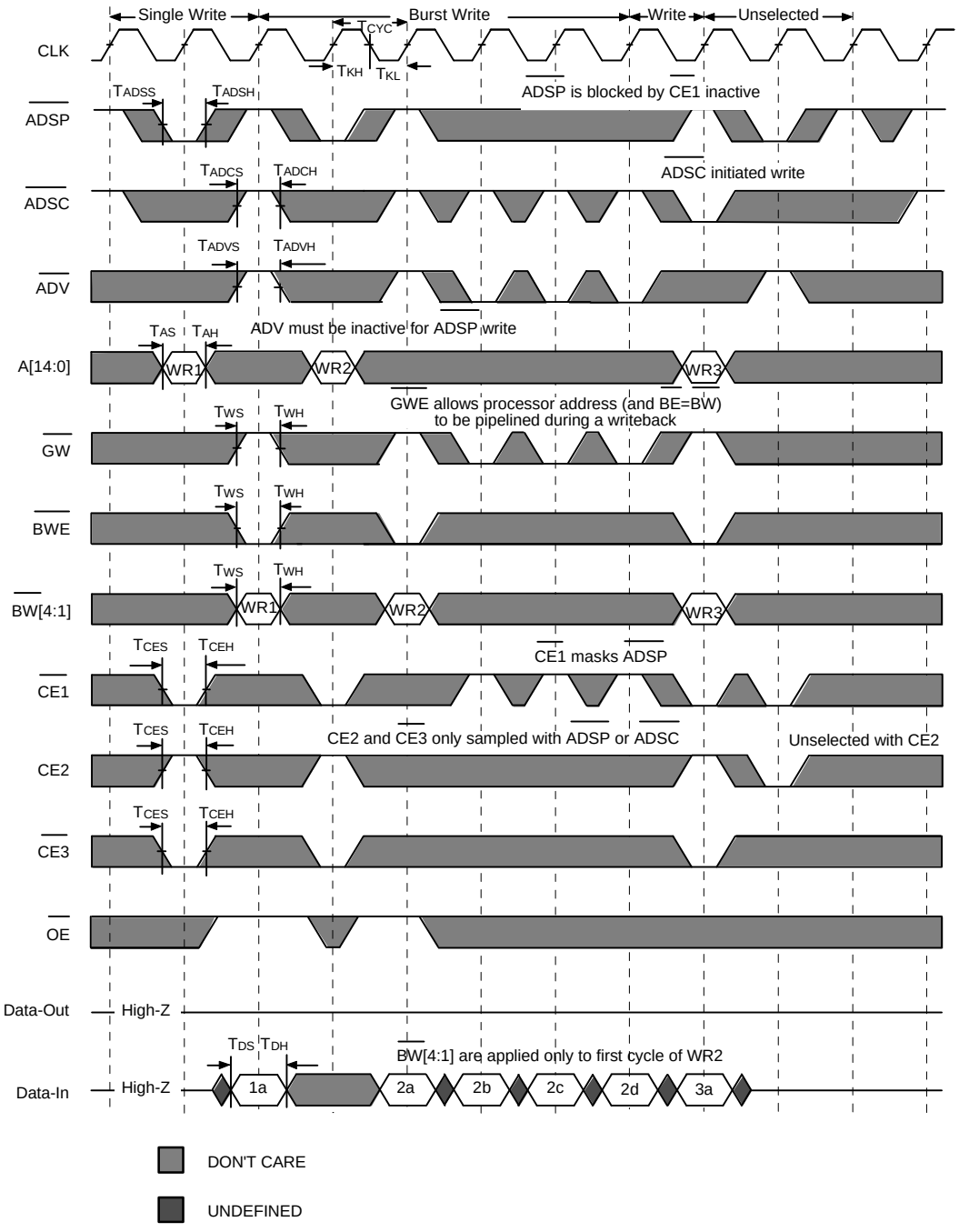
TIMING WAVEFORMS

Read Cycle Timing



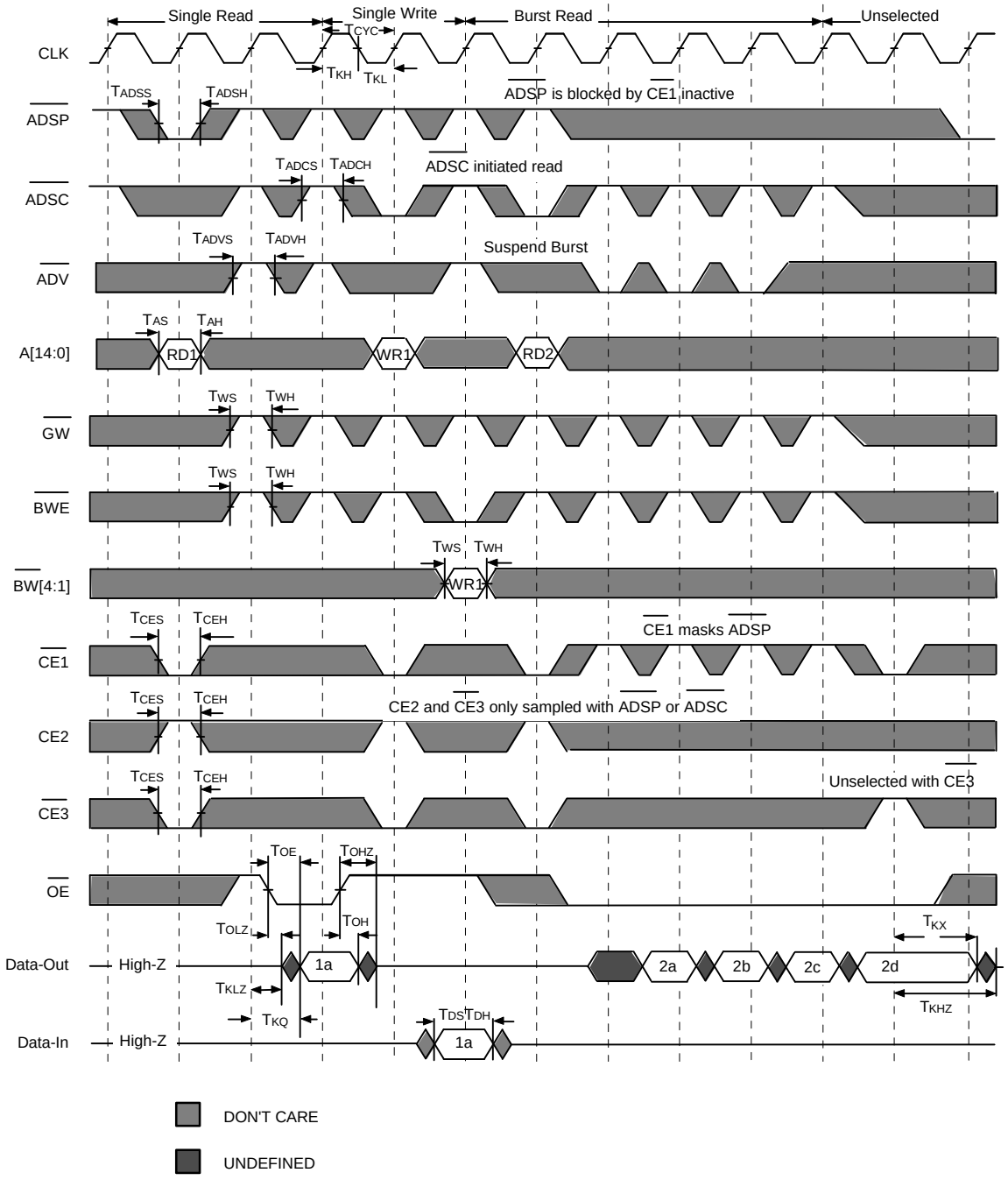
Timing Waveforms, continued

Write Cycle Timing



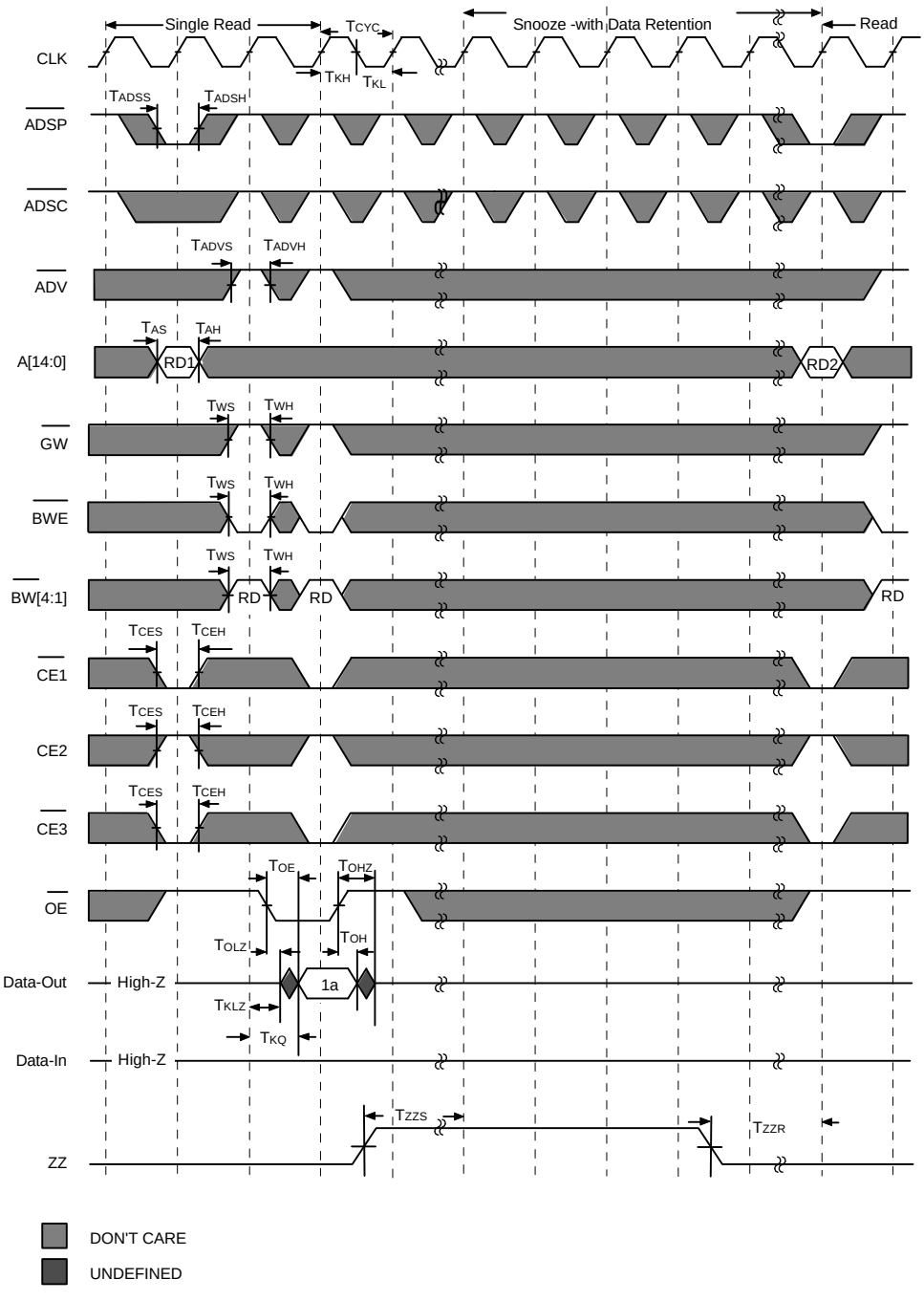
Timing Waveforms, continued

Read/Write Cycle Timing



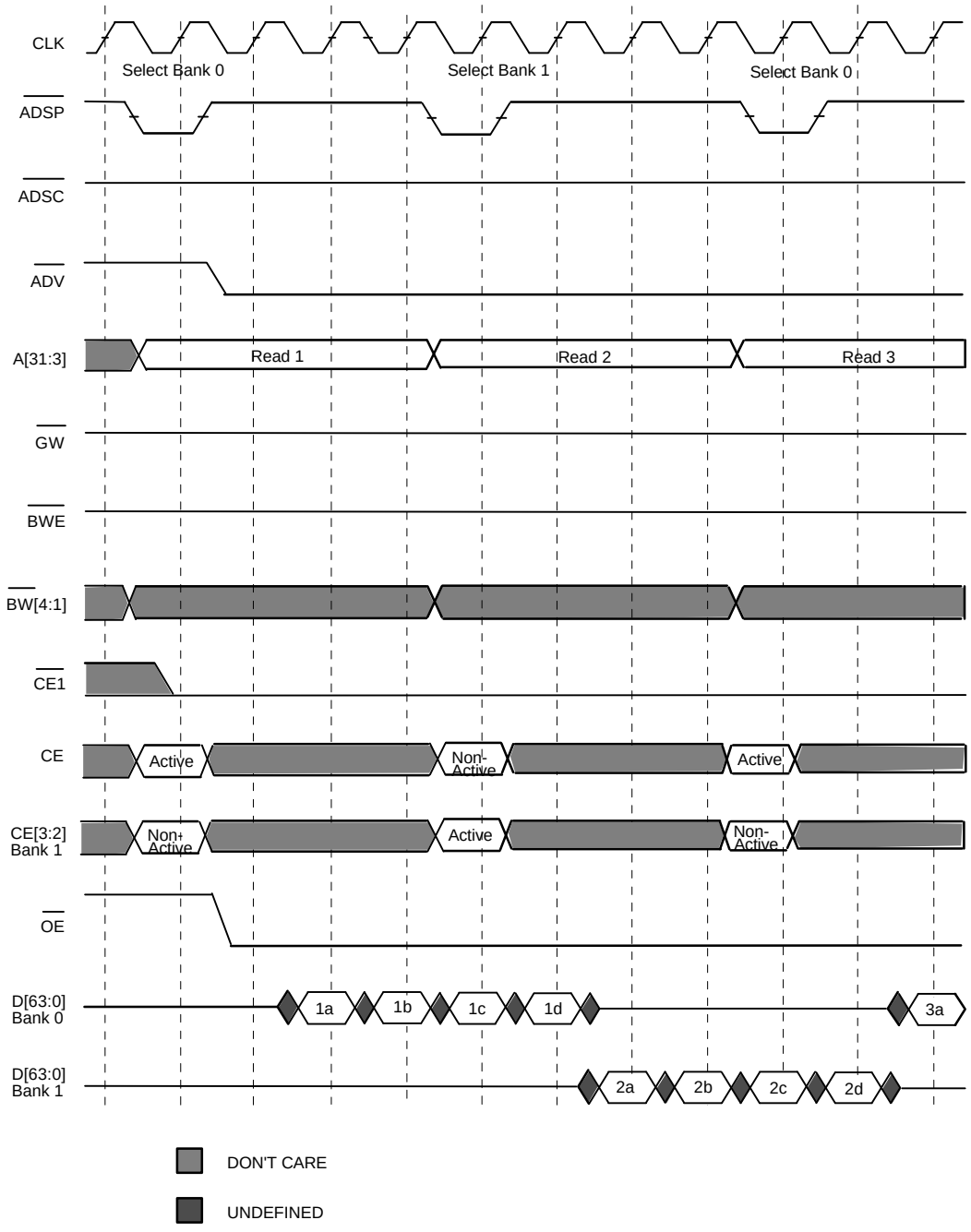
Timing Waveforms, continued

ZZ and RD Timing



Timing Waveforms, continued

Dual Bank Burst Read Cycle



ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (mA)	PACKAGE
W25P010AF-6	6	250	80	100-pin QFP
W25P010AF-7	7	250	80	100-pin QFP
W25P010AF-8	8	250	80	100-pin QFP
W25P010AD-6	6	250	80	100-pin TQFP
W25P010AD-7	7	250	80	100-pin TQFP
W25P010AD-8	8	250	80	100-pin TQFP

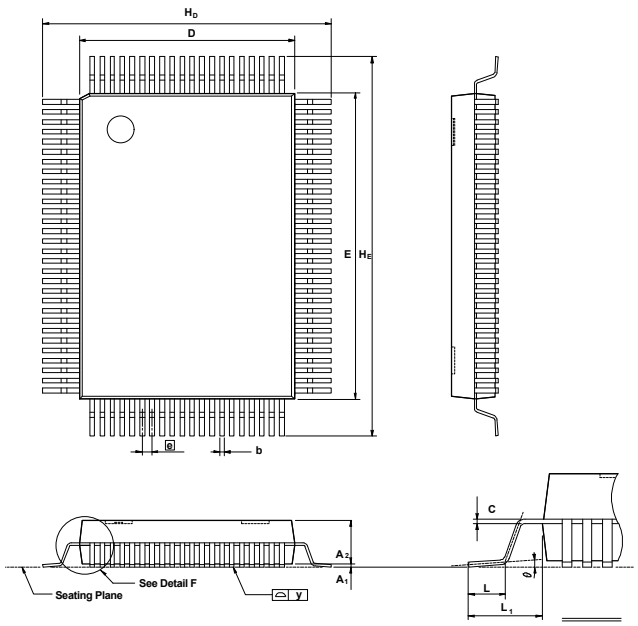
Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

Winbond Electronics Corp.

PACKAGE DIMENSIONS

100-pin QFP

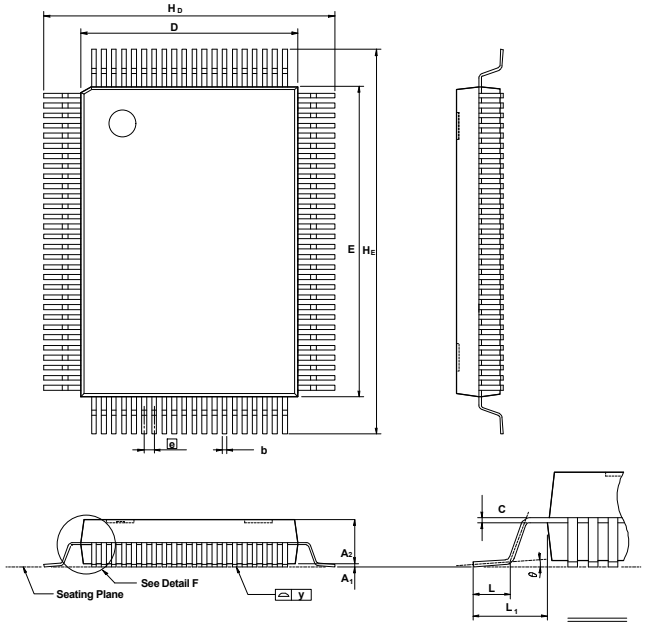


Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	—	—	—	—
A_1	0.01	0.014	0.018	0.25	0.35	0.45
A_2	0.101	0.107	0.113	2.57	2.72	2.87
b	0.008	0.012	0.016	0.20	0.30	0.40
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.783	0.787	0.791	19.90	20.00	20.10
e	0.020	0.026	0.032	0.498	0.65	0.802
H_D	0.669	0.677	0.685	17.00	17.20	17.40
H_E	0.905	0.913	0.921	23.00	23.20	23.40
L	0.025	0.031	0.037	0.65	0.80	0.95
L_1		0.063			1.60	
y	—	—	0.003	—	—	0.08
q	0°	—	7 °	0°	—	7 °

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

100-pin TQFP



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1035	1.40	1.45
b	0.009	0.013	0.015	0.22	0.32	0.38
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.783	0.787	0.791	19.90	20.00	20.10
e	0.020	0.026	0.032	0.498	0.65	0.802
H_D	0.626	0.630	0.634	15.90	16.00	16.10
H_E	0.862	0.866	0.870	21.90	22.00	22.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1		0.039			1.00	
y	—	—	0.003	—	—	0.08
q	0°	—	7 °	0°	—	7 °

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

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