XC4000
Logic Cell Array Family

Product Specifications

Features

- Third Generation Field-Programmable Gate Arrays
  - Abundant flip-flops
  - Flexible function generators
  - On-chip ultra-fast RAM
  - Dedicated high-speed carry-propagation circuit
  - Wide edge decoders (four per edge)
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - Eight global low-skew clock or signal distribution network
- Flexible Array Architecture
  - Programmable logic blocks and I/O blocks
  - Programmable interconnects and wide decoders
- Sub-micron CMOS Process
  - High-speed logic and Interconnect
  - Low power consumption
- Systems-Oriented Features
  - IEEE 1149.1-compatible boundary-scan logic support
  - Programmable output slew rate (2 modes)
  - Programmable input pull-up or pull-down resistors
  - 12-mA sink current per output
  - 24-mA sink current per output pair
- Configured by Loading Binary File
  - Unlimited reprogrammability
  - Six programming modes
- XACT Development System runs on ’386/’486-type PC, NEC PC, Apollo, Sun-4, and Hewlett-Packard 700 series
  - Interfaces to popular design environments like Viewlogic, Mentor Graphics and OrCAD
  - Fully automatic partitioning, placement and routing
  - Interactive design editor for design optimization
  - 288 macros, 34 hard macros, RAM/ROM compiler

Description

The XC4000 family of Field-Programmable Gate Arrays (FPGAs) provides the benefits of custom CMOS VLSI, while avoiding the initial cost, time delay, and inherent risk of a conventional masked gate array.

The XC4000 family provides a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile routing resources, and surrounded by a perimeter of programmable Input/Output Blocks (IOBs).

XC4000 devices have generous routing resources to accommodate the most complex interconnect patterns. They are customized by loading configuration data into the internal memory cells. The FPGA can either actively read its configuration data out of external serial or byte-parallel PROM (master modes), or the configuration data can be written into the FPGA (slave and peripheral modes).

The XC4000 family is supported by powerful and sophisticated software, covering every aspect of design: from schematic entry, to simulation, to automatic block placement and routing of interconnects, and finally the creation of the configuration bit stream.

Since Xilinx FPGAs can be reprogrammed an unlimited number of times, they can be used in innovative designs where hardware is changed dynamically, or where hardware must be adapted to different user applications. FPGAs are ideal for shortening the design and development cycle, but they also offer a cost-effective solution for production rates well beyond 1000 systems per month.

For a detailed description of the device features, architecture, configuration methods and pin descriptions, see pages 2-9 through 2-45.

Table 1. The XC4000 Family of Field-Programmable Gate Arrays

Device	XC4003	XC4005	XC4006	XC4008	XC4010/10D	XC4013	XC4020	XC4025
Appr. Gate Count	3,000	5,000	6,000	8,000	10,000	13,000	20,000	25,000
CLB Matrix	10 x 10	14 x 14	16 x 16	18 x 18	20 x 20	24 x 24	28 x 28	32 x 32
Number of CLBs	100	196	256	324	400	576	784	1,024
Number of Flip-Flops	360	616	768	936	1,120	1,536	2,016	2,560
Max Decode Inputs (per side)	30	42	48	54	60	72	84	96
Max RAM Bits	3,200	6,272	8,192	10,368	12,800*	18,432	25,088	32,768
Number of IOBs	80	112	128	144	160	192	224	256

*XC4010D has no RAM

Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to + 150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+ 260	°C
T_J	Junction temperature	+ 150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to 85°C junction	4.75	5.25	V
	Supply voltage relative to GND Industrial -40°C to 100°C junction	4.5	5.5	V
	Supply voltage relative to GND Military –55°C to 125°C case	4.5	5.5	V
V_{IH}	High-level input voltage (XC4000 has TTL-like input thresholds)	2.0	V_{CC}	V
V_{IL}	Low-level input voltage (XC4000 has TTL-like input thresholds)	0	0.8	V
T_{IN}	Input signal transition time		250	ns

At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.

DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = –4.0 mA, V_{CC} min	2.4		V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0 mA, V_{CC} min (Note 1)		0.4	V
I_{CCO}	Quiescent LCA supply current (Note 2)		10	mA
I_{IL}	Leakage current	–10	+10	µA
C_{IN}	Input capacitance (sample tested)		15	pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)	0.02	0.25	mA
I_{RLL}	Horizontal Long Line pull-up (when selected) @ logic Low	0.2	2.5	mA

Note: 1. With 50% of the outputs simultaneously sinking 12 mA.
2. With no output current loads, no active input or longline pull-up resistors, all package pins at V_{CC} or GND, and the LCA configured with a MakeBits tie option.

Wide Decoder Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

	Speed Grade		-6	-5	-4	
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	**Units**
Full length, both pull-ups, inputs from IOB I-pins	T_{WAF}	XC4003	9.0	8.0	5.0	ns
		XC4005	10.0	9.0	6.0	ns
		XC4006	11.0	10.0	7.0	ns
		XC4008	12.0	11.0	8.0	ns
		XC4010	13.0	12.0	9.0	ns
		XC4013	15.0	14.0	11.0	ns
		XC4025	21.0	19.0	17.0	ns
Full length, both pull-ups inputs from internal logic	T_{WAFL}	XC4003	12.0	11.0	7.0	ns
		XC4005	13.0	12.0	8.0	ns
		XC4006	14.0	13.0	9.0	ns
		XC4008	15.0	14.0	10.0	ns
		XC4010	16.0	15.0	11.0	ns
		XC4013	18.0	17.0	13.0	ns
		XC4025	24.0	23.0	20.0	ns
Half length, one pull-up inputs from IOB I-pins	T_{WAO}	XC4003	9.0	8.0	6.0	ns
		XC4005	10.0	9.0	7.0	ns
		XC4006	11.0	10.0	8.0	ns
		XC4008	12.0	11.0	9.0	ns
		XC4010	13.0	12.0	10.0	ns
		XC4013	15.0	14.0	12.0	ns
		XC4025	21.0	19.0	18.0	ns
Half length, one pull-up inputs from internal logic	T_{WAOL}	XC4003	12.0	11.0	8.0	ns
		XC4005	13.0	12.0	9.0	ns
		XC4006	14.0	13.0	10.0	ns
		XC4008	15.0	14.0	11.0	ns
		XC4010	16.0	15.0	12.0	ns
		XC4013	18.0	17.0	14.0	ns
		XC4025	24.0	23.0	21.0	ns

Note: These delays are specified from the decoder input to the decoder output. For pin-to-pin delays, add the input delay (T_{PID}) and output delay (T_{OPF} or T_{OPS}), as listed on page 2-52.

PRELIMINARY

Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

	Speed Grade		-6	-5	-4	
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	**Units**
Global Signal Distribution						
From pad through **primary** buffer, to any clock K	T_{PG}	XC4003	7.8	5.8	5.1	ns
		XC4005	8.0	6.0	5.5	ns
		XC4006	8.2	6.2	5.7	ns
		XC4008	8.6	6.6	6.1	ns
		XC4010	9.0	7.0	6.5	ns
		XC4013	10.0	8.0	7.5	ns
		XC4025	17.0	15.0	14.5	ns
From pad through **secondary** buffer, to any clock K	T_{SG}	XC4003	8.8	6.8	6.3	ns
		XC4005	9.0	7.0	6.7	ns
		XC4006	9.2	7.2	6.9	ns
		XC4008	9.6	7.6	7.3	ns
		XC4010	10.0	8.0	7.7	ns
		XC4013	11.0	9.0	8.7	ns
		XC4025	18.0	16.0	15.7	ns

Horizontal Longline Switching Characteristic Guidelines

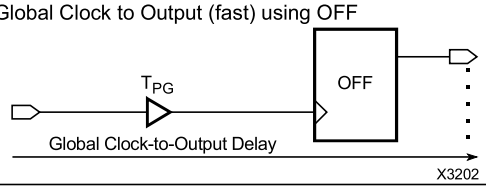
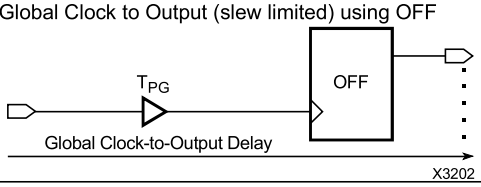
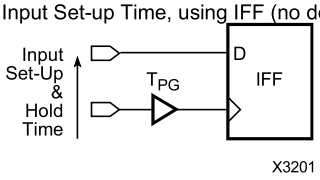
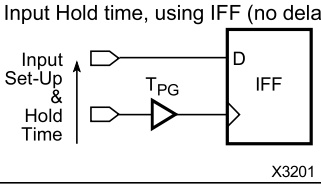
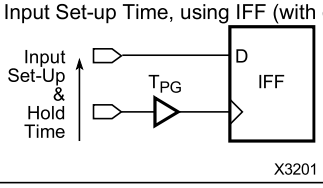
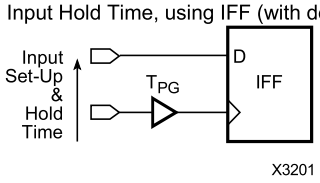
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

	Speed Grade		-6	-5	-4	
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	**Units**
TBUF driving a Horizontal Longline (L.L.) I going High or Low to L.L. going High or Low, while T is Low, i.e. buffer is constantly active	T_{IO1}	XC4003	8.8	6.2	4.4	ns
		XC4005	10.0	7.0	5.5	ns
		XC4006	10.6	7.5	6.0	ns
		XC4008	11.1	8.0	6.5	ns
		XC4010	11.7	8.5	7.0	ns
		XC4013	13.0	9.5	7.5	ns
		XC4025	20.0	16.5	14.5	ns
I going Low to L.L. going from resistive pull-up High to active Low, (TBUF configured as open drain)	T_{IO2}	XC4003	9.3	6.7	5.0	ns
		XC4005	10.5	7.5	6.0	ns
		XC4006	11.1	8.0	6.5	ns
		XC4008	11.6	8.5	7.0	ns
		XC4010	12.2	9.0	7.5	ns
		XC4013	13.5	10.0	8.0	ns
		XC4025	23.5	20.0	18.0	ns
T going Low to L.L. going from resistive pull-up or floating High to active Low, (TBUF configured as open drain or active buffer with I = Low)	T_{ON}	XC4003	10.7	9.0	7.2	ns
		XC4005	12.0	10.0	8.0	ns
		XC4006	12.6	10.5	8.5	ns
		XC4008	13.2	11.0	9.0	ns
		XC4010	13.8	11.5	9.5	ns
		XC4013	15.1	12.6	11.1	ns
		XC4025	23.0	20.5	19.0	ns
T going High to TBUF going inactive, not driving L.L.	T_{OFF}	All devices	3.0	2.0	1.8	ns
T going High to L.L. going from Low to High, pulled up by a single resistor	T_{PUS}	XC4003	24.0	20.0	14.0	ns
		XC4005	26.0	22.0	16.0	ns
		XC4006	28.0	24.0	18.0	ns
		XC4008	30.0	26.0	20.0	ns
		XC4010	32.0	28.0	22.0	ns
		XC4013	36.0	32.0	26.0	ns
		XC4025	52.0	48.0	42.0	ns
T going High to L.L. going from Low to High, pulled up by two resistors	T_{PUF}	XC4003	11.6	9.0	7.0	ns
		XC4005	12.0	10.0	8.0	ns
		XC4006	13.0	11.0	9.0	ns
		XC4008	14.0	12.0	10.0	ns
		XC4010	15.0	13.0	11.0	ns
		XC4013	17.0	15.0	13.0	ns
		XC4025	24.0	22.0	20.0	ns

PRELIMINARY

Guaranteed Input and Output Parameters (Pin-to-Pin)

All values listed below are tested directly, and guaranteed over the operating conditions. The same parameters can also be derived indirectly from the IOB and Global Buffer specifications. The XACT delay calculator uses this indirect method. When there is a discrepancy between these two methods, the values listed below should be used, and the derived values must be ignored.

Description	Symbol	Speed Grade / Device	-6	-5	-4	Units
Global Clock to Output (fast) using OFF 	T_{ICKOF} (Max)	XC4003	15.1	12.5	11.6	ns
		XC4005	15.5	13.0	12.0	ns
		XC4006	15.7	13.2	12.2	ns
		XC4008	16.1	13.6	12.6	ns
		XC4010	16.5	14.0	13.0	ns
		XC4013	17.5	15.0	14.0	ns
		XC4025	25.5	22.0	21.0	ns
Global Clock to Output (slew limited) using OFF 	T_{ICKO} (Max)	XC4003	19.9	15.2	14.4	ns
		XC4005	20.5	16.0	15.0	ns
		XC4006	20.7	16.2	15.2	ns
		XC4008	21.1	16.6	15.6	ns
		XC4010	21.5	17.0	16.0	ns
		XC4013	22.5	18.0	17.0	ns
		XC4025	29.5	25.0	24.0	ns
Input Set-up Time, using IFF (no delay) 	T_{PSUF} (Min)	XC4003	2.4	2.0	1.6	ns
		XC4005	2.0	1.5	1.2	ns
		XC4006	1.8	1.3	1.0	ns
		XC4008	1.4	0.9	0.6	ns
		XC4010	1.0	0.5	0.2	ns
		XC4013	0.5	0	0	ns
		XC4025	0	0	0	ns
Input Hold time, using IFF (no delay) 	T_{PHF} (Min)	XC4003	5.1	4.0	4.0	ns
		XC4005	5.5	4.5	4.5	ns
		XC4006	5.7	4.7	4.7	ns
		XC4008	6.1	5.1	5.1	ns
		XC4010	6.5	5.5	5.5	ns
		XC4013	7.5	6.5	6.5	ns
		XC4025	18.0	16.0	15.5	ns
Input Set-up Time, using IFF (with delay) 	T_{PSU} (Min)	XC4003	21.5	18.5	12.0	ns
		XC4005	21.0	18.0	12.0	ns
		XC4006	20.8	17.8	12.0	ns
		XC4008	20.4	17.4	12.0	ns
		XC4010	20.0	17.0	12.0	ns
		XC4013	19.0	16.0	12.0	ns
		XC4025	18.0	15.0	12.0	ns
Input Hold Time, using IFF (with delay) 	T_{PH} (Min)	XC4003	0	0	0	ns
		XC4005	0	0	0	ns
		XC4006	0	0	0	ns
		XC4008	0	0	0	ns
		XC4010	0	0	0	ns
		XC4013	0	0	0	ns
		XC4025	0	0	0	ns

Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). When testing fast outputs, only one output switches. When testing slew-rate limited outputs, half the number of outputs on one side of the device are switching. These parameter values are tested and guaranteed for worst-case conditions of supply voltage and temperature, and also with the most unfavorable clock polarity choice.

T_{PDLI} for -4 Speed Grade

Pad to I1, I2 via transparent latch, with delay	XC4003	17.6 ns
	XC4005	17.9 ns
	XC4006	18.0 ns
	XC4008	18.3 ns
	XC4010	18.6 ns
	XC4013	19.3 ns
	XC4025	23.5 ns

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See page 2-52

T_{PICKD} for -4 Speed Grade

Input set-up time pad to clock (IK) with delay	XC4003	15.6 ns
	XC4005	15.9 ns
	XC4006	16.0 ns
	XC4008	16.3 ns
	XC4010	16.6 ns
	XC4013	17.3 ns
	XC4025	22.5 ns

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IOB Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

Speed Grade		-6		-5		-4		
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Input								
Propagation Delays								
Pad to I1, I2	T_{PID}		4.0		3.0		2.8	ns
Pad to I1, I2, via transparent latch (no delay)	T_{PLI}		8.0		7.0		6.0	ns
Pad to I1, I2, via transparent latch (with delay)	T_{PDLI}		26.0		24.0		**	ns
Clock (IK) toI1, I2, (flip-flop)	T_{IKRI}		8.0		7.0		6.0	ns
Clock (IK) to I1, I2 (latch enable, active Low)	T_{IKLI}		8.0		7.0		6.0	ns
Set-up Time (Note 3)								
Pad to Clock (IK), no delay	T_{PICK}	7.0		6.0		4.0		ns
Pad to Clock (IK) with delay	T_{PICKD}	25.0		24.0		**		ns
Hold Time (Note 3)								
Pad to Clock (IK), no delay	T_{IKPI}	1.0		1.0		1.0		ns
Pad to Clock (IK) with delay	T_{IKPID}	neg		neg		neg		ns
Output								
Propagation Delays								
Clock (OK) to Pad (fast)	T_{OKPOF}		7.5		7.0		6.5	ns
same (slew rate limited)	T_{OKPOS}		11.5		10.0		9.5	ns
Output (O) to Pad (fast)	T_{OPF}		9.0		7.0		5.5	ns
same (slew-rate limited)	T_{OPS}		13.0		10.0		8.5	ns
3-state to Pad begin hi-Z (slew-rate independent)	T_{TSHZ}		9.0		7.0		6.5	ns
3-state to Pad active and valid (fast)	T_{TSONF}		13.0		10.0		9.5	ns
same (slew -rate limited)	T_{TSONS}		17.0		13.0		12.5	ns
Set-up and Hold Times								
Output (O) to clock (OK) set-up time	T_{OOK}	8.0		6.0		5.5		ns
Output (O) to clock (OK) hold time	T_{OKO}	0		0		0		ns
Clock								
Clock High or Low time	T_{CH}/T_{CL}	5.0		4.5		4.0		ns
Global Set/Reset								
Delay from GSR net through Q to I1, I2	T_{RRI}		14.5		13.5		13.5	ns
Delay from GSR net to Pad	T_{RPO}		18.0		17.0		14.0	ns
GSR width*	T_{MRW}	21.0		18.0		18.0		ns

* Timing is based on the XC4005. For other devices see XACT timing calculator.
** See preceding page

Notes: 1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). **Slew rate limited** output rise/fall times are approximately two times longer than **fast** output rise/fall times. For the effect of capacitive loads on ground bounce, see pages 8-8 through 8-10.

2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up or pull-down resistor or alternatively configured as a driven output or be driven from an external source.

3. Input pad setup times and hold times are specified with respect to the internal clock (IK). To calculate system setup time, subtract clock delay (clock pad to IK) from the specified input pad setup time value, but do not subtract below zero. Negative hold time means that the delay in the input data is adequate for the **external system hold time** to be zero, provided the input clock uses the Global signal distribution from pad to IK.

CLB Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

Speed Grade		-6		-5		-4		
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Combinatorial Delays								
F/G inputs to X/Y outputs	T_{ILO}		6.0		4.5		4.0	ns
F/G inputs via H' to X/Y outputs	T_{IHO}		8.0		7.0		6.0	ns
C inputs via H' to X/Y outputs	T_{HHO}		7.0		5.0		4.5	ns
CLB Fast Carry Logic								
Operand inputs (F1,F2,G1,G4) to COUT	T_{OPCY}		7.0		5.5		5.0	ns
Add/Subtract input (F3) to COUT	T_{ASCY}		8.0		6.0		5.5	ns
Initialization inputs (F1,F3) to COUT	T_{INCY}		6.0		4.0		3.5	ns
C_{IN} through function generators to X/Y outputs	T_{SUM}		8.0		6.0		5.5	ns
C_{IN} to C_{OUT}, bypass function generators.	T_{BYP}		2.0		1.5		1.5	ns
Sequential Delays								
Clock K to outputs Q	T_{CKO}		5.0		3.0		3.0	ns
Set-up Time before Clock K								
F/G inputs	T_{ICK}	6.0		4.5		4.5		ns
F/G inputs via H'	T_{IHCK}	8.0		6.0		6.0		ns
C inputs via H1	T_{HHCK}	7.0		5.0		5.0		ns
C inputs via DIN	T_{DICK}	4.0		3.0		3.0		ns
C inputs via EC	T_{ECCK}	7.0		4.0		3.0		ns
C inputs via S/R, going Low (inactive)	T_{RCK}	6.0		4.5		4.0		ns
C_{IN} input via F'/G'	T_{CCK}	8.0		6.0		5.5		ns
C_{IN} input via F'/G' and H'	T_{CHCK}	10.0		7.5		7.3		ns
Hold Time after Clock K								
F/G inputs	T_{CKI}	0		0		0		ns
F/G inputs via H'	T_{CKIH}	0		0		0		ns
C inputs via H1	T_{CKHH}	0		0		0		ns
C inputs via DIN	T_{CKDI}	0		0		0		ns
C inputs via EC	T_{CKEC}	0		0		0		ns
C inputs via S/R, going Low (inactive)	T_{CKR}	0		0		0		ns
Clock								
Clock High time	T_{CH}	5.0		4.5		4.0		ns
Clock Low time	T_{CL}	5.0		4.5		4.0		ns
Set/Reset Direct								
Width (High)	T_{RPW}	5.0		4.0		4.0		ns
Delay from C inputs via S/R, going High to Q	T_{RIO}		9.0		8.0		7.0	ns
Master Set/Reset*								
Width (High or Low)	T_{MRW}	21.0		18.0		18.0		ns
Delay from Global Set/Reset net to Q	T_{MRQ}		33.0		31.0		28.0	ns

* Timing is based on the XC4005. For other devices see XACT timing calculator.

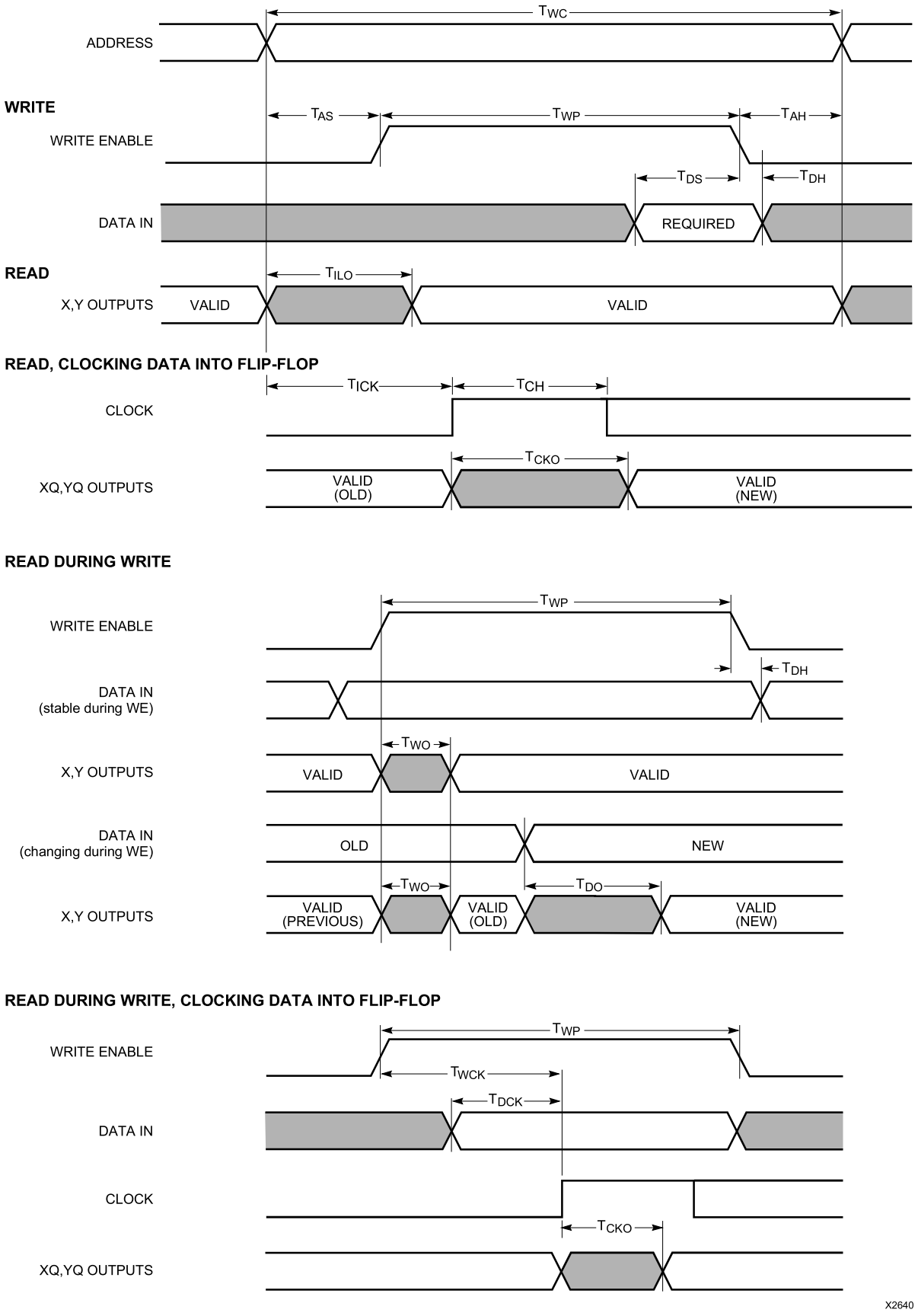
CLB Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

CLB RAM Option	**Speed Grade**		**-6**		**-5**		**-4**		
Description	**Symbol**		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Write Operation									
Address write cycle time	16 x 2	T_{WC}	9.0		8.0		8.0		ns
	32 x 1	T_{WCT}	9.0		8.0		8.0		ns
Write Enable pulse width (High)	16 x 2	T_{WP}	5.0		4.0		4.0		ns
	32 x 1	T_{WPT}	5.0		4.0		4.0		ns
Address set-up time before beginning of WE	16 x 2	T_{AS}	2.0		2.0		2.0		ns
	32 x 1	T_{AST}	2.0		2.0		2.0		ns
Address hold time after end of WE	16 x 2	T_{AH}	2.0		2.0		2.0		ns
	32 x 1	T_{AHT}	2.0		2.0		2.0		ns
DIN set-up time before end of WE	16 x 2	T_{DS}	4.0		4.0		4.0		ns
	32 x 1	T_{DST}	5.0		5.0		5.0		ns
DIN hold time after end of WE	both	T_{DHT}	2.0		2.0		2.0		ns
Read Operation									
Address read cycle time	16 x 2	T_{RC}	7.0		5.5		5.0		ns
	32 x 1	T_{RCT}	10.0		7.5		7.0		ns
Data valid after address change	16 x 2	T_{ILO}		6.0		4.5		4.0	ns
(no Write Enable)	32 x 1	T_{IHO}		8.0		7.0		6.0	ns
Read Operation, Clocking Data into Flip-Flop									
Address setup time before clock K	16 x 2	T_{ICK}	6.0		4.5		4.5		ns
	32 x 1	T_{IHCK}	8.0		6.0		6.0		ns
Read During Write									
Data valid after WE going active	16 x 2	T_{WO}		12.0		10.0		9.0	ns
(DIN stable before WE)	32 x 1	T_{WOT}		15.0		12.0		11.0	ns
Data valid after DIN	16 x 2	T_{DO}		11.0		9.0		8.5	ns
(DIN change during WE)	32 x 1	T_{DOT}		14.0		11.0		11.0	ns
Read During Write, Clocking Data into Flip-Flop									
WE setup time before clock K	16 x 2	T_{WCK}	12.0		10.0		9.5		ns
	32 x 1	T_{WCKT}	15.0		12.0		11.5		ns
Data setup time before clock K	16 x 2	T_{DCK}	11.0		9.0		9.0		ns
	32 x 1	T_{DCKT}	14.0		11.0		11.0		ns

Note: Timing for the 16 x 1 RAM option is identical to 16 x 2 RAM timing

CLB RAM Timing Characteristics



XC4003 Pinouts

Pin Description	PC84	PQ100	PG120	Bound Scan
VCC	2	92	G3	–
I/O (A8)	3	93	G1	32
I/O (A9)	4	94	F1	35
I/O	–	95	E1	38
I/O	–	96	F2	41
I/O (A10)	5	97	F3	44
I/O (A11)	6	98	D1	47
–	–	–	E2*	–
I/O (A12)	7	99	C1	50
I/O (A13)	8	100	D2	53
–	–	–	E3*	–
–	–	–	B1*	–
I/O (A14)	9	1	C2	56
SGCK1 (A15,I/O)	10	2	D3	59
VCC	11	3	C3	–
GND	12	4	C4	–
PGCK1 (A16, I/O)	13	5	B2	62
I/O (A17)	14	6	B3	65
–	–	–	A1*	–
–	–	–	A2*	–
I/O (TDI)	15	7	C5	68
I/O (TCK)	16	8	B4	71
–	–	–	A3*	–
I/O (TMS)	17	9	B5	74
I/O	18	10	A4	77
I/O	–	–	C6	80
I/O	–	11	A5	83
I/O	19	12	B6	86
I/O	20	13	A6	89
GND	21	14	B7	–
VCC	22	15	C7	–
I/O	23	16	A7	92
I/O	24	17	A8	95
I/O	–	18	A9	98
I/O	–	–	B8	101
I/O	25	19	C8	104
I/O	26	20	A10	107
I/O	27	21	B9	110
I/O	–	22	A11	113
–	–	–	B10*	–
I/O	28	23	C9	116
SGCK2 (I/O)	29	24	A12	119
O (M1)	30	25	B11	122
GND	31	26	C10	–
I (M0)	32	27	C11	125†
VCC	33	28	D11	–
I (M2)	34	29	B12	126†
PGCK2 (I/O)	35	30	C12	127
I/O (HDC)	36	31	A13	130
–	–	–	B13*	–
–	–	–	E11*	–
I/O	–	32	D12	133
I/O (LDC)	37	33	C13	136
I/O	38	34	E12	139
I/O	39	35	D13	142
I/O	–	36	F11	145
I/O	–	37	E13	148
I/O	40	38	F12	151
I/O (ERR, INIT)	41	39	F13	154
VCC	42	40	G12	–

Pin Description	PC84	PQ100	PG120	Bound Scan
GND	43	41	G11	–
I/O	44	42	G13	157
I/O	45	43	H13	160
I/O	–	44	J13	163
I/O	–	45	H12	166
I/O	46	46	H11	169
I/O	47	47	K13	172
I/O	48	48	J12	175
I/O	49	49	L13	178
–	–	–	K12*	–
–	–	–	J11*	–
I/O	50	50	M13	181
SGCK3 (I/O)	51	51	L12	184
GND	52	52	K11	–
DONE	53	53	L11	–
VCC	54	54	L10	–
PROG	55	55	M12	–
I/O (D7)	56	56	M11	187
PGCK3 (I/O)	57	57	N13	190
–	–	–	N12*	–
–	–	–	L9*	–
I/O (D6)	58	58	M10	193
I/O	–	59	N11	196
I/O (D5)	59	60	M9	199
I/O (CS0)	60	61	N10	202
I/O	–	62	L8	205
I/O	–	63	N9	208
I/O (D4)	61	64	M8	211
I/O	62	65	N8	214
VCC	63	66	M7	–
GND	64	67	L7	–
I/O (D3)	65	68	N7	217
I/O (RS)	66	69	N6	220
I/O	–	70	N5	223
I/O	–	–	M6	226
I/O (D2)	67	71	L6	229
I/O	68	72	N4	232
I/O (D1)	69	73	M5	235
I/O (RCLK-BUSY/RDY)	70	74	N3	238
–	–	–	M4*	–
–	–	–	L5*	–
I/O (D0, DIN)	71	75	N2	241
SGCK4 (DOUT, I/O)	72	76	M3	244
CCLK	73	77	L4	–
VCC	74	78	L3	–
O (TDO)	75	79	M2	–
GND	76	80	K3	–
I/O (A0, WS)	77	81	L2	2
PGCK4 (A1, I/O)	78	82	N1	5
–	–	–	M1*	–
–	–	–	J3*	–
I/O (CS1, A2)	79	83	K2	8
I/O (A3)	80	84	L1	11
I/O (A4)	81	85	J2	14
I/O (A5)	82	86	K1	17
I/O	–	87	H3	20
I/O	–	88	J1	23
I/O (A6)	83	89	H2	26
I/O (A7)	84	90	H1	29
GND	1	91	G2	–

* Indicates unconnected package pins.
† Contributes only one bit (.i) to the boundary scan register.
Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 247 = BSCANT.UPD

XC4005 Pinouts

Pin Description	PC84	PQ160	PQ208	PG156	Bound Scan
VCC	2	142	183	H3	–
I/O (A8)	3	143	184	H1	44
I/O (A9)	4	144	185	G1	47
I/O	–	145	186	G2	50
I/O	–	146	187	G3	53
–	–	–	188*	–	–
–	–	–	189*	–	–
I/O (A10)	5	147	190	F1	56
I/O (A11)	6	148	191	F2	59
I/O	–	149	192	E1	62
I/O	–	150	193	E2	65
GND	–	151	194	F3	–
–	–	–	195*	–	–
–	–	–	196*	–	–
–	–	152*	197*	D1*	–
–	–	153*	198*	D2*	–
I/O (A12)	7	154	199	E3	68
I/O (A13)	8	155	200	C1	71
–	–	–	–	–	–
I/O	–	156	201	C2	74
I/O	–	157	202	D3	77
I/O (A14)	9	158	203	B1	80
SGCK1 (A15, I/O)	10	159	204	B2	83
VCC	11	160	205	C3	–
–	–	–	206*	–	–
–	–	–	207*	–	–
–	–	–	208*	–	–
–	–	–	1*	–	–
GND	12	1	2	C4	–
–	–	–	3*	–	–
PGCK1 (A16, I/O)	13	2	4	B3	86
I/O (A17)	14	3	5	A1	89
I/O	–	4	6	A2	92
I/O	–	5	7	C5	95
–	–	–	–	–	–
I/O (TDI)	15	6	8	B4	98
I/O (TCK)	16	7	9	A3	101
–	–	8*	10*	A4*	–
–	–	9*	11*	–	–
–	–	–	12*	–	–
–	–	–	13*	–	–
GND	–	10	14	C6	–
I/O	–	11	15	B5	104
I/O	–	12	16	B6	107
I/O (TMS)	17	13	17	A5	110
I/O	18	14	18	C7	113
–	–	–	19*	–	–
–	–	–	20*	–	–
I/O	–	15	21	B7	116
I/O	–	16	22	A6	119
I/O	19	17	23	A7	122
I/O	20	18	24	A8	125
GND	21	19	25	C8	–
VCC	22	20	26	B8	–
I/O	23	21	27	C9	128
I/O	24	22	28	B9	131
I/O	–	23	29	A9	134
I/O	–	24	30	B10	137
–	–	–	31*	–	–
–	–	–	32*	–	–
I/O	25	25	33	C10	140
I/O	26	26	34	A10	143
I/O	–	27	35	A11	146
I/O	–	28	36	B11	149
GND	–	29	37	C11	–
–	–	–	38*	–	–
–	–	–	39*	–	–
–	–	30*	40*	A12*	–
–	–	31*	41*	–	–
I/O	27	32	42	B12	152
I/O	–	33	43	A13	155
I/O	–	34	44	A14	158

Pin Description	PC84	PQ160	PQ208	PG156	Bound Scan
I/O	–	35	45	C12	161
–	–	–	–	–	–
I/O	28	36	46	B13	164
SGCK2 (I/O)	29	37	47	B14	167
O (M1)	30	38	48	A15	170
GND	31	39	49	C13	–
I (M0)	32	40	50	A16	173†
–	–	–	51*	–	–
–	–	–	52*	–	–
–	–	–	53*	–	–
–	–	–	54*	–	–
VCC	33	41	55	C14	–
I (M2)	34	42	56	B15	174†
PGCK2 (I/O)	35	43	57	B16	175
I/O (HDC)	36	44	58	D14	178
I/O	–	45	59	C15	181
–	–	–	–	–	–
I/O	–	46	60	D15	184
I/O	–	47	61	E14	187
I/O (LDC)	37	48	62	C16	190
–	–	49*	63*	E15*	–
–	–	50*	64*	D16*	–
–	–	–	65*	–	–
–	–	–	66*	–	–
GND	–	51	67	F14	–
I/O	–	52	68	F15	193
I/O	–	53	69	E16	196
I/O	38	54	70	F16	199
I/O	39	55	71	G14	202
–	–	–	72*	–	–
–	–	–	73*	–	–
I/O	–	56	74	G15	205
I/O	–	57	75	G16	208
I/O	40	58	76	H16	211
I/O (ERR, INIT)	41	59	77	H15	214
VCC	42	60	78	H14	–
GND	43	61	79	J14	–
I/O	44	62	80	J15	217
I/O	45	63	81	J16	220
I/O	–	64	82	K16	223
I/O	–	65	83	K15	226
–	–	–	84*	–	–
–	–	–	85*	–	–
I/O	46	66	86	K14	229
I/O	47	67	87	L16	232
I/O	–	68	88	M16	235
I/O	–	69	89	L15	238
GND	–	70	90	L14	–
–	–	–	91*	–	–
–	–	–	92*	–	–
–	–	71*	93*	N16*	–
–	–	72*	94*	M15*	–
I/O	48	73	95	P16	241
I/O	49	74	96	M14	244
I/O	–	75	97	N15	247
I/O	–	76	98	P15	250
I/O	50	77	99	N14	253
SGCK3 (I/O)	51	78	100	R16	256
GND	52	79	101	P14	–
–	–	–	102*	–	–
DONE	53	80	103	R15	–
–	–	–	104*	–	–
–	–	–	105*	–	–
VCC	54	81	106	P13	–
–	–	–	107*	–	–
PROG	55	82	108	R14	–
I/O (D7)	56	83	109	T16	259
PGCK3 (I/O)	57	84	110	T15	262
I/O	–	85	111	R13	265
–	–	–	–	–	–
I/O	–	86	112	P12	268
I/O (D6)	58	87	113	T14	271

Pin Description	PC84	PQ160	PQ208	PG156	Bound Scan
I/O	–	88	114	T13	274
–	–	89*	115*	R12*	–
–	–	89*	115*	R12*	–
–	–	90	116*	T12*	–
–	–	–	117*	–	–
–	–	–	118*	–	–
GND	–	91	119	P11	–
I/O	–	92	120	R11	277
I/O	–	93	121	T11	280
I/O (D5)	59	94	122	T10	283
I/O (CS0)	60	95	123	P10	286
–	–	–	124*	–	–
–	–	–	125*	–	–
I/O	–	96	126	R10	289
I/O	–	97	127	T9	292
I/O (D4)	61	98	128	R9	295
I/O	62	99	129	P9	298
VCC	63	100	130	R8	–
GND	64	101	131	P8	–
I/O (D3)	65	102	132	T8	301
I/O (RS)	66	103	133	T7	304
I/O	–	104	134	T6	307
I/O	–	105	135	R7	310
–	–	–	136*	–	–
–	–	–	137*	–	–
I/O (D2)	67	106	138	P7	313
I/O	68	107	139	T5	316
I/O	–	108	140	R6	319
I/O	–	109	141	T4	322
GND	–	110	142	P6	–
–	–	–	143*	–	–
–	–	–	144*	–	–
–	–	111*	145*	R5*	–
–	–	112*	146*	–	–
I/O (D1)	69	113	147	T3	325
I/O (BCLK-BUSY/RDY)	70	114	148	P5	328
I/O	–	115	149	R4	331
–	–	–	–	–	–
I/O	–	116	150	R3	334
I/O (D0, DIN)	71	117	151	P4	337
SGCK4 (DOUT, I/O)	72	118	152	T2	340
CCLK	73	119	153	R2	–
VCC	74	120	154	P3	–
–	–	–	155*	–	–
–	–	–	156*	–	–
–	–	–	157*	–	–
–	–	–	158*	–	–
O (TDO)	75	121	159	T1	–
GND	76	122	160	N3	–
I/O (A0,WS)	77	123	161	R1	2
PGCK4 (A1,I/O)	78	124	162	P2	5
I/O	–	125	163	N2	8
–	–	–	–	–	–
I/O	–	126	164	M3	11
I/O (CS1,A2)	79	127	165	P1	14
I/O (A3)	80	128	166	N1	17
–	–	129*	167*	M2*	–
–	–	130*	168*	M1*	–
–	–	–	169*	–	–
–	–	–	170*	–	–
GND	–	131	171	L3	–
I/O	–	132	172	L2	20
I/O	–	133	173	L1	23
I/O (A4)	81	134	174	K3	26
I/O (A5)	82	135	175	K2	29
–	–	–	176*	–	–
–	–	136*	177*	–	–
I/O	–	137	178	K1	32
I/O	–	138	179	J1	35
I/O (A6)	83	139	180	J2	38
I/O (A7)	84	140	181	J3	41
GND	1	141	182	H2	–

* Indicates unconnected package pins.

† Contributes only one bit (.i) to the boundary scan register.

Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 343 = BSCANT.UPD

XC4006 Pinouts

Pin Description	PC 84	PG 156	PQ 160	PQ 208	Boundary Scan Order
VCC	2	H3	142	183	-
I/O (A8)	3	H1	143	184	50
I/O (A9)	4	G1	144	185	53
I/O	-	G2	145	186	56
I/O	-	G3	146	187	59
-	-	-	-	188*	-
-	-	-	-	189*	-
I/O (A10)	5	F1	147	190	62
I/O (A11)	6	F2	148	191	65
I/O	-	E1	149	192	68
I/O	-	E2	150	193	71
GND	-	F3	151	194	-
-	-	-	-	195*	-
-	-	-	-	196*	-
I/O	-	D1	152	197	74
I/O	-	D2	153	198	77
I/O (A12)	7	E3	154	199	80
I/O (A13)	8	C1	155	200	83
I/O	-	C2	156	201	86
I/O	-	D3	157	202	89
I/O (A14)	9	B1	158	203	92
SGCK1 (A15, I/O)	10	B2	159	204	95
VCC	11	C3	160	205	-
-	-	-	-	206*	-
-	-	-	-	207*	-
-	-	-	-	208*	-
-	-	-	-	1*	-
GND	12	C4	1	2	-
-	-	-	-	3*	-
PGCK1 (A16, I/O)	13	B3	2	4	98
I/O (A17)	14	A1	3	5	101
I/O	-	A2	4	6	104
I/O	-	C5	5	7	107
I/O (TDI)	15	B4	6	8	110
I/O (TCK)	16	A3	7	9	113
I/O	-	A4	8	10	116
I/O	-	-	9	11	119
-	-	-	-	12*	-
-	-	-	-	13*	-
GND	-	C6	10	14	-
I/O	-	B5	11	15	122
I/O	-	B6	12	16	125
I/O (TMS)	17	A5	13	17	128
I/O	18	C7	14	18	131
-	-	-	-	19*	-
-	-	-	-	20*	-
I/O	-	B7	15	21	134
I/O	-	A6	16	22	137
I/O	19	A7	17	23	140
I/O	20	A8	18	24	143
GND	21	C8	19	25	-
VCC	22	B8	20	26	-

Pin Description	PC 84	PG 156	PQ 160	PQ 208	Boundary Scan Order
I/O	23	C9	21	27	146
I/O	24	B9	22	28	149
I/O	-	A9	23	29	152
I/O	-	B10	24	30	155
-	-	-	-	31*	-
-	-	-	-	32*	-
I/O	25	C10	25	33	158
I/O	26	A10	26	34	161
I/O	-	A11	27	35	164
I/O	-	B11	28	36	167
GND	-	C11	29	37	-
-	-	-	-	38*	-
-	-	-	-	39*	-
I/O	-	A12	30	40	170
I/O	-	-	31	41	173
I/O	27	B12	32	42	176
I/O	-	A13	33	43	179
I/O	-	A14	34	44	182
I/O	-	C12	35	45	185
I/O	28	B13	36	46	188
SGCK2 (I/O)	29	B14	37	47	191
O (M1)	30	A15	38	48	194
GND	31	C13	39	49	-
I (M0)	32	A16	40	50	197†
-	-	-	-	51*	-
-	-	-	-	52*	-
-	-	-	-	53*	-
-	-	-	-	54*	-
VCC	33	C14	41	55	-
I (M2)	34	B15	42	56	198†
PGCK2 (I/O)	35	B16	43	57	199
I/O (HDC)	36	D14	44	58	202
I/O	-	C15	45	59	205
I/O	-	D15	46	60	208
I/O	-	E14	47	61	211
I/O ($\overline{\text{LDC}}$)	37	C16	48	62	214
I/O	-	E15	49	63	217
I/O	-	D16	50	64	220
-	-	-	-	65*	-
-	-	-	-	66*	-
GND	-	F14	51	67	-
I/O	-	F15	52	68	223
I/O	-	E16	53	69	226
I/O	38	F16	54	70	229
I/O	39	G14	55	71	232
-	-	-	-	72*	-
-	-	-	-	73*	-
I/O	-	G15	56	74	235
I/O	-	G16	57	75	238
I/O	40	H16	58	76	241
I/O ($\overline{\text{ERR}}$,$\overline{\text{INIT}}$)	41	H15	59	77	244
VCC	42	H14	60	78	-

* Indicates unconnected package pins.

† Contributes only one bit (.i) to the boundary scan register.

XC4006 Pinouts (continued)

Pin Description	PC 84	PG 156	PQ1 60	PQ 208	Boundary Scan Order
GND	43	J14	61	79	-
I/O	44	J15	62	80	247
I/O	45	J16	63	81	250
I/O	-	K16	64	82	253
I/O	-	K15	65	83	256
-	-	-	-	84*	-
-	-	-	-	85*	-
I/O	46	K14	66	86	259
I/O	47	L16	67	87	262
I/O	-	M16	68	88	265
I/O	-	L15	69	89	268
GND	-	L14	70	90	-
-	-	-	-	91*	-
-	-	-	-	92*	-
I/O	-	N16	71	93	271
I/O	-	M15	72	94	274
I/O	48	P16	73	95	277
I/O	49	M14	74	96	280
I/O	-	N15	75	97	283
I/O	-	P15	76	98	286
I/O	50	N14	77	99	289
SGCK3 (I/O)	51	R16	78	100	292
GND	52	P14	79	101	-
-	-	-	-	102*	-
DONE	53	R15	80	103	-
-	-	-	-	104*	-
-	-	-	-	105*	-
VCC	54	P13	81	106	-
-	-	-	-	107*	-
$\overline{\text{PROG}}$	55	R14	82	108	-
I/O (D7)	56	T16	83	109	295
PGCK3 (I/O)	57	T15	84	110	298
I/O	-	R13	85	111	301
I/O	-	P12	86	112	304
I/O (D6)	58	T14	87	113	307
I/O	-	T13	88	114	310
I/O	-	R12	89	115	313
I/O	-	T12	90	116	316
-	-	-	-	117*	-
-	-	-	-	118*	-
GND	-	P11	91	119	-
I/O	-	R11	92	120	319
I/O	-	T11	93	121	322
I/O (D5)	59	T10	94	122	325
I/O ($\overline{\text{CS0}}$)	60	P10	95	123	328
-	-	-	-	124*	-
-	-	-	-	125*	-
I/O	-	R10	96	126	331
I/O	-	T9	97	127	334
I/O (D4)	61	R9	98	128	337
I/O	62	P9	99	129	340
VCC	63	R8	100	130	-

* Indicates unconnected package pins.

Pin Description	PC 84	PG 156	PQ 160	PQ 208	Boundary Scan Order
GND	64	P8	101	131	-
I/O (D3)	65	T8	102	132	343
I/O ($\overline{\text{RS}}$)	66	T7	103	133	346
I/O	-	T6	104	134	349
I/O	-	R7	105	135	352
-	-	-	-	136*	-
-	-	-	-	137*	-
I/O (D2)	67	P7	106	138	355
I/O	68	T5	107	139	358
I/O	-	R6	108	140	361
I/O	-	T4	109	141	364
GND	-	P6	110	142	-
-	-	-	-	143*	-
-	-	-	-	144*	-
I/O	-	R5	111	145	367
I/O	-	-	112	146	370
I/O (D1)	69	T3	113	147	373
I/O (RCLK-BUSY/$\overline{\text{RDY}}$)	70	P5	114	148	376
I/O	-	R4	115	149	379
I/O	-	R3	116	150	382
I/O (D0, DIN)	71	P4	117	151	385
SGCK4 (DOUT, I/O)	72	T2	118	152	388
CCLK	73	R2	119	153	-
VCC	74	P3	120	154	-
-	-	-	-	155*	-
-	-	-	-	156*	-
-	-	-	-	157*	-
-	-	-	-	158*	-
TDO	75	T1	121	159	-
GND	76	N3	122	160	-
I/O (A0, $\overline{\text{WS}}$)	77	R1	123	161	2
PGCK4 (I/O, A1)	78	P2	124	162	5
I/O	-	N2	125	163	8
I/O	-	M3	126	164	11
I/O (CS1,A2)	79	P1	127	165	14
I/O (A3)	80	N1	128	166	17
I/O	-	M2	129	167	20
I/O	-	M1	130	168	23
-	-	-	-	169*	-
-	-	-	-	170*	-
GND	-	L3	131	171	-
I/O	-	L2	132	172	26
I/O	-	L1	133	173	29
I/O (A4)	81	K3	134	174	32
I/O (A5)	82	K2	135	175	35
-	-	-	-	176*	-
-	-	-	136*	177*	-
I/O	-	K1	137	178	38
I/O	-	J1	138	179	41
I/O (A6)	83	J2	139	180	44
I/O (A7)	84	J3	140	181	47
GND	1	H2	141	182	-

Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 391 = BSCAN.UPD

XC4008 Pinouts

Pin Description	PC 84	PQ 160	PG 191	PQ 208	Boundary Scan Order
VCC	2	142	J4	183	–
I/O (A8)	3	143	J3	184	56
I/O (A9)	4	144	J2	185	59
I/O	–	145	J1	186	62
I/O	–	146	H1	187	65
I/O	–	–	H2	188	68
I/O	–	–	H3	189	71
I/O (A10)	5	147	G1	190	74
I/O (A11)	6	148	G2	191	77
I/O	–	149	F1	192	80
I/O	–	150	E1	193	83
GND	–	151	G3	194	–
–	–	–	F2*	195*	–
–	–	–	D1*	196*	–
I/O	–	152	C1	197	86
I/O	–	153	E2	198	89
I/O (A12)	7	154	F3	199	92
I/O (A13)	8	155	D2	200	95
I/O	–	156	B1	201	98
–	–	–	–	–	–
I/O	–	157	E3	202	101
I/O (A14)	9	158	C2	203	104
SGCK1 (A15, I/O)	10	159	B2	204	107
VCC	11	160	D3	205	–
–	–	–	–	206*	–
–	–	–	–	207*	–
–	–	–	–	208*	–
–	–	–	–	1*	–
GND	12	1	D4	2	–
–	–	–	–	3*	–
PGCK1 (A16, I/O)	13	2	C3	4	110
I/O (A17)	14	3	C4	5	113
I/O	–	4	B3	6	116
–	–	–	–	–	–
I/O	–	5	C5	7	119
I/O (TDI)	15	6	A2	8	122
I/O (TCK)	16	7	B4	9	125
I/O	–	8	C6	10	128
I/O	–	9	A3	11	131
–	–	–	B5*	12*	–
–	–	–	B6*	13*	–
GND	–	10	C7	14	–
I/O	–	11	A4	15	134
I/O	–	12	A5	16	137
I/O (TMS)	17	13	B7	17	140
I/O	18	14	A6	18	143
I/O	–	–	C8	19	146
I/O	–	–	A7	20	149
I/O	–	15	B8	21	152
I/O	–	16	A8	22	155
I/O	19	17	B9	23	158
I/O	20	18	C9	24	161
GND	21	19	D9	25	–

Pin Description	PC 84	PQ 160	PG 191	PQ 208	Boundary Scan Order
VCC	22	20	D10	26	–
I/O	23	21	C10	27	164
I/O	24	22	B10	28	167
I/O	–	23	A9	29	170
I/O	–	24	A10	30	173
I/O	–	–	A11	31	176
I/O	–	–	C11	32	179
I/O	25	25	B11	33	182
I/O	26	26	A12	34	185
I/O	–	27	B12	35	188
I/O	–	28	A13	36	191
GND	–	29	C12	37	–
–	–	–	B13*	38*	–
–	–	–	A14*	39*	–
I/O	–	30	A15	40	194
I/O	–	31	C13	41	197
I/O	27	32	B14	42	200
I/O	–	33	A16	43	203
I/O	–	34	B15	44	206
I/O	–	35	C14	45	209
I/O	28	36	A17	46	212
SGCK2 (I/O)	29	37	B16	47	215
O (M1)	30	38	C15	48	218
GND	31	39	D15	49	–
I (M0)	32	40	A18	50	221†
–	–	–	–	51*	–
–	–	–	–	52*	–
–	–	–	–	53*	–
–	–	–	–	54*	–
VCC	33	41	D16	55	–
I (M2)	34	42	C16	56	222†
PGCK2 (I/O)	35	43	B17	57	223
I/O (HDC)	36	44	E16	58	226
–	–	–	–	–	–
I/O	–	45	C17	59	229
I/O	–	46	D17	60	232
I/O	–	47	B18	61	235
I/O (LDC)	37	48	E17	62	238
I/O	–	49	F16	63	241
I/O	–	50	C18	64	244
–	–	–	D18*	65*	–
–	–	–	F17*	66*	–
GND	–	51	G16	67	–
I/O	–	52	E18	68	247
I/O	–	53	F18	69	250
I/O	38	54	G17	70	253
I/O	39	55	G18	71	256
I/O	–	–	H16	72	259
I/O	–	–	H17	73	262
I/O	–	56	H18	74	265
I/O	–	57	J18	75	268
I/O	40	58	J17	76	271
I/O ($\overline{\text{ERR}}$, $\overline{\text{INIT}}$)	41	59	J16	77	274
VCC	42	60	J15	78	–

* Indicates unconnected package pins.

† Contributes only one bit (.i) to the boundary scan register.

XC4008 Pinouts (continued)

Pin Description	PC 84	PQ 160	PG 191	PQ 208	Boundary Scan Order
GND	43	61	K15	79	–
I/O	44	62	K16	80	277
I/O	45	63	K17	81	280
I/O	–	64	K18	82	283
I/O	–	65	L18	83	286
I/O	–	–	L17	84	289
I/O	–	–	L16	85	292
I/O	46	66	M18	86	295
I/O	47	67	M17	87	298
I/O	–	68	N18	88	301
I/O	–	69	P18	89	304
GND	–	70	M16	90	–
–	–	–	N17*	91*	–
–	–	–	R18*	92*	–
I/O	–	71	T18	93	307
I/O	–	72	P17	94	310
I/O	48	73	N16	95	313
I/O	49	74	T17	96	316
I/O	–	75	R17	97	319
I/O	–	76	P16	98	322
I/O	50	77	U18	99	325
SGCK3 (I/O)	51	78	T16	100	328
GND	52	79	R16	101	–
–	–	–	–	102*	–
DONE	53	80	U17	103	–
–	–	–	–	104*	–
–	–	–	–	105*	–
VCC	54	81	R15	106	–
–	–	–	–	107*	–
$\overline{\text{PROG}}$	55	82	V18	108	–
I/O (D7)	56	83	T15	109	331
PGCK3 (I/O)	57	84	U16	110	334
–	–	–	–	–	–
I/O	–	85	T14	111	337
I/O	–	86	U15	112	340
I/O (D6)	58	87	V17	113	343
I/O	–	88	V16	114	346
I/O	–	89	T13	115	349
I/O	–	90	U14	116	352
–	–	–	V15*	117*	–
–	–	–	V14*	118*	–
GND	–	91	T12	119	–
I/O	–	92	U13	120	355
I/O	–	93	V13	121	358
I/O (D5)	59	94	U12	122	361
I/O ($\overline{\text{CSO}}$)	60	95	V12	123	364
I/O	–	–	T11	124	367
I/O	–	–	U11	125	370
I/O	–	96	V11	126	373
I/O	–	97	V10	127	376
I/O (D4)	61	98	U10	128	379
I/O	62	99	T10	129	382
VCC	63	100	R10	130	
GND	64	101	R9	131	

Pin Description	PC 84	PQ 160	PG 191	PQ 208	Boundary Scan Order
I/O (D3)	65	102	T9	132	385
I/O ($\overline{\text{RS}}$)	66	103	U9	133	388
I/O	–	104	V9	134	391
I/O	–	105	V8	135	394
I/O	–	–	U8	136	397
I/O	–	–	T8	137	400
I/O (D2)	67	106	V7	138	403
I/O	68	107	U7	139	406
I/O	–	108	V6	140	409
I/O	–	109	U6	141	412
GND	–	110	T7	142	–
–	–	–	V5*	143*	–
–	–	–	V4*	144*	–
I/O	–	111	U5	145	415
I/O	–	112	T6	146	418
I/O (D1)	69	113	V3	147	421
I/O ($\overline{\text{RCLK}}$-BUSY/RDY)	70	114	V2	148	424
I/O	–	115	U4	149	427
I/O	–	116	T5	150	430
I/O (D0, DIN)	71	117	U3	151	433
SGCK4 (DOUT, I/O)	72	118	T4	152	436
CCLK	73	119	V1	153	–
VCC	74	120	R4	154	–
–	–	–	–	155*	–
–	–	–	–	156*	–
–	–	–	–	157*	–
–	–	–	–	158*	–
TD0	75	121	U2	159	–
GND	76	122	R3	160	–
I/O (A0, $\overline{\text{WS}}$)	77	123	T3	161	2
PGCK4 (I/O,A1)	78	124	U1	162	5
–	–	–	–	–	–
I/O	–	125	P3	163	8
I/O	–	126	R2	164	11
I/O (CS1, A2)	79	127	T2	165	14
I/O (A3)	80	128	N3	166	17
I/O	–	129	P2	167	20
I/O	–	130	T1	168	23
–	–	–	R1*	169*	–
–	–	–	N2*	170*	–
GND	–	131	M3	171	–
I/O	–	132	P1	172	26
I/O	–	133	N1	173	29
I/O (A4)	81	134	M2	174	32
I/O (A5)	82	135	M1	175	35
I/O	–	–	L3	176	38
I/O	–	136	L2	177	41
I/O	–	137	L1	178	44
I/O	–	138	K1	179	47
I/O (A6)	83	139	K2	180	50
I/O (A7)	84	140	K3	181	53
GND	1	141	K4	182	–

* Indicates unconnected package pins.
Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 439 = BSCAN.UPD

XC4010/XC4010D Pinouts

Pin Description	PC84	PQ160	†† PG191	PQ208	*** BG225	Boundary Scan Order
VCC	2	142	J4	183	D8	-
I/O (A8)	3	143	J3	184	E8	62
I/O (A9)	4	144	J2	185	B7	65
I/O	-	145	J1	186	A7	68
I/O	-	146	H1	187	C7	71
I/O	-	-	H2	188	D7	74
I/O	-	-	H3	189	E7	77
I/O (A10)	5	147	G1	190	A6	80
I/O (A11)	6	148	G2	191	B6	83
I/O	-	149	F1	192	A5	86
I/O	-	150	E1	193	B5	89
GND	-	151	G3	194	**	-
I/O	-	-	F2	195	D6	92
I/O	-	-	D1	196	C5	96
I/O	-	152	C1	197	A4	98
I/O	-	153	E2	198	E6	101
I/O (A12)	7	154	F3	199	B4	104
I/O (A13)	8	155	D2	200	D5	107
I/O	-	156	B1	201	B3	110
I/O	-	157	E3	202	F6	113
I/O (A14)	9	158	C2	203	A2	116
SGCK1 (A15, I/O)	10	159	B2	204	C3	119
VCC	11	160	D3	205	B2	-
-	-	-	-	206*	-	-
-	-	-	-	207*	-	-
-	-	-	-	208*	-	-
-	-	-	-	1*	-	-
GND	12	1	D4	2	A1	-
-	-	-	-	3*	-	-
PGCK1 (A16, I/O)	13	2	C3	4	D4	122
I/O (A17)	14	3	C4	5	B1	125
I/O	-	4	B3	6	C2	128
I/O	-	5	C5	7	E5	131
I/O (TDI)	15	6	A2	8	D3	134
I/O (TCK)	16	7	B4	9	C1	137
I/O	-	8	C6	10	D2	140
I/O	-	9	A3	11	G6	143
I/O	-	-	B5	12	E4	146
I/O	-	-	B6	13	D1	149
GND	-	10	C7	14	**	-
I/O	-	11	A4	15	F5	152
I/O	-	12	A5	16	E1	155
I/O (TMS)	17	13	B7	17	F4	158
I/O	18	14	A6	18	F3	161
I/O	-	-	C8	19	G4	164
I/O	-	-	A7	20	G3	167
I/O	-	15	B8	21	G2	170
I/O	-	16	A8	22	G1	173
I/O	19	17	B9	23	G5	176
I/O	20	18	C9	24	H3	179
GND	21	19	D9	25	H2	-
VCC	22	20	D10	26	H1	-
I/O	23	21	C10	27	H4	182
I/O	24	22	B10	28	H5	185
I/O	-	23	A9	29	J2	188

Pin Description	PC84	PQ160	PG191	PQ208	*** BG225	Boundary Scan Order
I/O	-	24	A10	30	J1	191
I/O	-	-	A11	31	J3	194
I/O	-	-	C11	32	J4	197
I/O	25	25	B11	33	K2	200
I/O	26	26	A12	34	K3	203
I/O	-	27	B12	35	J6	206
I/O	-	28	A13	36	L1	209
GND	-	29	C12	37	**	-
I/O	-	-	B13	38	L3	212
I/O	-	-	A14	39	M1	215
I/O	-	30	A15	40	K5	218
I/O	-	31	C13	41	M2	221
I/O	27	32	B14	42	L4	224
I/O	-	33	A16	43	N1	227
I/O	-	34	B15	44	M3	230
I/O	-	35	C14	45	N2	233
I/O	28	36	A17	46	K6	236
SGCK2 (I/O)	29	37	B16	47	P1	239
O (M1)	30	38	C15	48	N3	242
GND	31	39	D15	49	**	-
I (M0)	32	40	A18	50	P2	245†
-	-	-	-	51*	-	-
-	-	-	-	52*	-	-
-	-	-	-	53*	-	-
-	-	-	-	54*	-	-
VCC	33	41	D16	55	R1	-
I (M2)	34	42	C16	56	M4	246†
PGCK2 (I/O)	35	43	B17	57	R2	247
I/O (HDC)	36	44	E16	58	P3	250
I/O	-	45	C17	59	L5	253
I/O	-	46	D17	60	N4	256
I/O	-	47	B18	61	R3	259
I/O (LDC)	37	48	E17	62	P4	262
I/O	-	49	F16	63	K7	265
I/O	-	50	C18	64	M5	268
I/O	-	-	D18	65	R4	271
I/O	-	-	F17	66	N5	274
GND	-	51	G16	67	**	-
I/O	-	52	E18	68	R5	277
I/O	-	53	F18	69	M6	280
I/O	38	54	G17	70	N6	283
I/O	39	55	G18	71	P6	286
I/O	-	-	H16	72	R6	289
I/O	-	-	H17	73	M7	291
I/O	-	56	H18	74	R7	295
I/O	-	57	J18	75	L7	298
I/O	40	58	J17	76	N8	301
I/O ($\overline{ERR}$, $\overline{INIT}$)	41	59	J16	77	P8	304
VCC	42	60	J15	78	R8	-
GND	43	61	K15	79	M8	-
I/O	44	62	K16	80	L8	307
I/O	45	63	K17	81	P9	310
I/O	-	64	K18	82	R9	313
I/O	-	65	L18	83	N9	316
I/O	-	-	L17	84	M9	319
I/O	-	-	L16	85	L9	322
I/O	46	66	M18	86	N10	325

* Indicates unconnected package pins.

** The following BGA225 balls are connected to ground:
F8, G7, G8, G9, H6, H7, H8, H9, H10, J7, J8, J9, K8

*** The following BG225 balls are unconnected:
E3, E2, F1, F2, J5, K1, L2, K4, P5, L6, N7, P7, R10, P10, M10, N11, N15, M14, L15, K12, G10, E15, E14, F12, F9, D11, C10, B10, C6, F7, A3, C4

† Contributes only one bit (.i) to the boundary scan register.
†† XC4010 only. PG191 package not available for XC4010D

XC4010/XC4010D Pinouts (continued)

Pin Description	PC84	†† PQ160	PG191	PQ208	*** BG225	Boundary Scan Order
I/O	47	67	M17	87	K9	328
I/O	-	68	N18	88	R11	331
I/O	-	69	P18	89	P11	334
GND	-	70	M16	90	**	-
I/O	-	-	N17	91	R12	337
I/O	-	-	R18	92	L10	340
I/O	-	71	T18	93	P12	343
I/O	-	72	P17	94	M11	346
I/O	48	73	N16	95	R13	349
I/O	49	74	T17	96	N12	352
I/O	-	75	R17	97	P13	355
I/O	-	76	P16	98	K10	358
I/O	50	77	U18	99	R14	361
SGCK3 (I/O)	51	78	T16	100	N13	364
GND	52	79	R16	101	**	-
-	-	-	-	102*	-	-
DONE	53	80	U17	103	P14	-
-	-	-	-	104*	-	-
-	-	-	-	105*	-	-
VCC	54	81	R15	106	R15	-
-	-	-	-	107*	-	-
$\overline{\text{PROG}}$	55	82	V18	108	M12	-
I/O (D7)	56	83	T15	109	P15	367
PGCK3 (I/O)	57	84	U16	110	N14	370
I/O	-	85	T14	111	L11	373
I/O	-	86	U15	112	M13	376
I/O (D6)	58	87	V17	113	J10	379
I/O	-	88	V16	114	L12	382
I/O	-	89	T13	115	M15	385
I/O	-	90	U14	116	L13	388
I/O	-	-	V15	117	L14	391
I/O	-	-	V14	118	K11	394
GND	-	91	T12	119	**	-
I/O	-	92	U13	120	K13	397
I/O	-	93	V13	121	K14	400
I/O ($\overline{\text{D5}}$)	59	94	U12	122	K15	403
I/O ($\overline{\text{CSO}}$)	60	95	V12	123	J12	406
I/O	-	-	T11	124	J13	409
I/O	-	-	U11	125	J14	412
I/O	-	96	V11	126	J15	415
I/O	-	97	V10	127	J11	418
I/O (D4)	61	98	U10	128	H13	421
I/O	62	99	T10	129	H14	424
VCC	63	100	R10	130	H15	-
GND	64	101	R9	131	**	-
I/O (D3)	65	102	T9	132	H12	427
I/O ($\overline{\text{RS}}$)	66	103	U9	133	H11	430
I/O	-	104	V9	134	G14	433
I/O	-	105	V8	135	G15	436
I/O	-	-	U8	136	G13	439
I/O	-	-	T8	137	G12	442
I/O (D2)	67	106	V7	138	G11	445
I/O	68	107	U7	139	F15	448
I/O	-	108	V6	140	F14	451
I/O	-	109	U6	141	F13	454
GND	-	110	T7	142	**	-
I/O	-	-	V5	143	E13	457

Pin Description	PC84	PQ160	PG191	PQ208	*** BG225	Boundary Scam Order
I/O	-	-	V4	144	D15	460
I/O	-	111	U5	145	F11	463
I/O	-	112	T6	146	D14	466
I/O (D1)	69	113	V3	147	E12	469
I/O ($\overline{\text{RCLK-BUSY}}$/RDY	70	114	V2	148	C15	472
I/O	-	115	U4	149	D13	475
I/O	-	116	T5	150	C14	478
I/O (D0, DIN)	71	117	U3	151	F10	481
SGCK4 (DOUT, I/O)	72	118	T4	152	B15	484
CCLK	73	119	V1	153	C13	-
VCC	74	120	R4	154	B14	-
-	-	-	-	155*	-	-
-	-	-	-	156*	-	-
-	-	-	-	157*	-	-
-	-	-	-	158*	-	-
TD0	75	121	U2	159	A15	-
GND	76	122	R3	160	D12	-
I/O (A0, $\overline{\text{WS}}$)	77	123	T3	161	A14	2
PGCK4 (I/O, A1)	78	124	U1	162	B13	5
I/O	-	125	P3	163	E11	8
I/O	-	126	R2	164	C12	11
I/O (CS1, A2)	79	127	T2	165	A13	14
I/O (A3)	80	128	N3	166	B12	17
I/O	-	129	P2	167	A12	20
I/O	-	130	T1	168	C11	23
I/O	-	-	R1	169	B11	26
I/O	-	-	N2	170	E10	29
GND	-	131	M3	171	**	-
I/O	-	132	P1	172	A11	32
I/O	-	133	N1	173	D10	35
I/O (A4)	81	134	M2	174	A10	38
I/O (A5)	82	135	M1	175	D9	41
I/O	-	-	L3	176	C9	44
I/O	-	136	L2	177	B9	47
I/O	-	137	L1	178	A9	50
I/O	-	138	K1	179	E9	53
I/O (A6)	83	139	K2	180	C8	56
I/O (A7)	84	140	K3	181	B8	59
GND	1	141	K4	182	A8	-

Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 487 = BSCAN.UPD

* Indicates unconnected package pins.

** The following BGA225 balls are connected to ground:
F8, G7, G8, G9, H6, H7, H8, H9, H10, J7, J8, J9, K8

*** The following BG225 balls are unconnected:
E3, E2, F1, F2, J5, K1, L2, K4, P5, L6, N7, P7, R10, P10, M10, N11, N15, M14, L15, K12, G10, E15, E14, F12, F9, D11, C10, B10, C6, F7, A3, C4

†† XC4010 only. PG 191 package not available for XC4010D

XC4013/XC4013D Pinouts

Pin Description	PQ160	MQ208	PG223	BG225	PQ240	Boundary Scan Order
VCC	142	183	J4	A10	212	-
I/O (A8)	143	184	J3	E8	213	74
I/O (A9)	144	185	J2	F8	214	77
I/O	145	186	J1	B7	215	80
I/O	146	187	H1	A7	216	83
I/O	-	188	H2	G7	217	86
I/O	-	189	H3	E7	218	89
-	-	-	-	-	219*	-
I/O (A10)	147	190	G1	F7	220	92
I/O (A11)	148	191	G2	C7	221	95
VCC	-	-	-	-	222	-
I/O	-	-	H4	B6	223	98
I/O	-	-	G4	E6	224	101
I/O	149	192	F1	D7	225	104
I/O	150	193	E1	F6	226	107
GND	151	194	G3	A5	227	-
I/O	-	195	F2	B5	228	110
I/O	-	196	D1	D5	229	113
I/O	152	197	C1	C5	230	116
I/O	153	198	E2	C6	231	119
I/O (A12)	154	199	F3	A4	232	122
I/O (A13)	155	200	D2	D4	233	125
I/O	-	-	F4	B4	234	128
I/O	-	-	E4	C3	235	131
I/O	156	201	B1	A3	236	134
I/O	157	202	E3	C2	237	137
I/O (A14)	158	203	C2	D6	238	140
SGCK1 (A15, I/O)	159	204	B2	A2	239	143
VCC	160	205	D3	A6	240	-
-	-	206*	-	-	-	-
-	-	207*	-	-	-	-
-	-	208*	-	-	-	-
-	-	1*	-	-	-	-
GND	1	2	D4	A1	1	-
-	-	3*	-	-	-	-
PGCK1 (A16,I/O)	2	4	C3	B1	2	146
I/O (A17)	3	5	C4	B3	3	149
I/O	4	6	B3	C4	4	152
I/O	5	7	C5	B2	5	155
I/O (TDI)	6	8	A2	C1	6	158
I/O (TCK)	7	9	B4	E3	7	161
I/O	8	10	C6	D2	8	164
I/O	9	11	A3	D3	9	167
I/O	-	12	B5	D1	10	170
I/O	-	13	B6	E5	11	173
I/O	-	-	D5	F4	12	176
I/O	-	-	D6	E2	13	179
GND	10	14	C7	E1	14	-
I/O	11	15	A4	E4	15	182
I/O	12	16	A5	F3	16	185
I/O (TMS)	13	17	B7	F2	17	188
I/O	14	18	A6	F5	18	191
VCC	-	-	-	F1	19	-
I/O	-	-	D7	G4	20	194
I/O	-	-	D8	G2	21	197
-	-	-	-	-	22*	-
I/O	-	19	C8	G3	23	200
I/O	-	20	A7	G6	24	203
I/O	15	21	B8	G5	25	206
I/O	16	22	A8	G1	26	209
I/O	17	23	B9	H5	27	212
I/O	18	24	C9	H7	28	215
GND	19	25	D9	H1	29	-
VCC	20	26	D10	H2	30	-

Pin Description	PQ160	MQ208	PG223	BG225	PQ240	Boundary Scan Order
I/O	21	27	C10	H6	31	218
I/O	22	28	B10	H3	32	221
I/O	23	29	A9	J6	33	224
I/O	24	30	A10	H4	34	227
I/O	-	31	A11	J1	35	230
I/O	-	32	C11	J5	36	233
-	-	-	-	-	37*	-
I/O	-	-	D11	J2	38	236
I/O	-	-	D12	J7	39	239
VCC	-	-	-	K1	40	-
I/O	25	33	B11	J3	41	242
I/O	26	34	A12	K2	42	245
I/O	27	35	B12	K5	43	248
I/O	28	36	A13	K3	44	251
GND	29	37	C12	L1	45	-
I/O	-	-	D13	K6	46	254
I/O	-	-	D14	L2	47	257
I/O	-	38	B13	J4	48	260
I/O	-	39	A14	M2	49	263
I/O	30	40	A15	L5	50	266
I/O	31	41	C13	M1	51	269
I/O	32	42	B14	H3	52	272
I/O	33	43	A16	L3	53	275
I/O	34	44	B15	M4	54	278
I/O	35	45	C14	N1	55	281
I/O	36	46	A17	N2	56	284
SGCK2 (I/O)	37	47	B16	K4	57	287
O (M1)	38	48	C15	L4	58	290
GND	39	49	D15	41	59	-
I (M0)	40	50	A18	P1	60	293†
-	-	51*	-	-	-	-
-	-	52*	-	-	-	-
-	-	53*	-	-	-	-
-	-	54*	-	-	-	-
VCC	41	55	D16	R6	61	-
I (M2)	42	56	C16	R2	62	294†
PGCK2 (I/O)	43	57	B17	P3	63	295
I/O (HDC)	44	58	E16	M6	64	298
I/O	45	59	C17	P2	65	301
I/O	46	60	D17	R3	66	304
I/O	47	61	B18	N3	67	307
I/O (LDC)	48	62	E17	N5	68	310
I/O	49	63	F16	N4	69	313
I/O	50	64	C18	R4	70	316
I/O	-	65	D18	P4	71	319
I/O	-	66	F17	N6	72	322
I/O	-	-	E15	P5	73	325
I/O	-	-	F15	M5	74	328
GND	51	67	G16	R5	75	-
I/O	52	68	E18	M7	76	331
I/O	53	69	F18	P6	77	334
I/O	54	70	G17	L6	78	337
I/O	55	71	G18	N7	79	340
VCC	-	-	-	-	80	-
I/O	-	72	H16	P7	81	343
I/O	-	73	H17	M8	82	346
-	-	-	-	-	83*	-
I/O	-	-	G15	K7	84	349
I/O	-	-	H15	L7	85	352
I/O	56	74	H18	R7	86	355
I/O	57	75	J18	N8	87	358
I/O	58	76	J17	J8	88	361
I/O (ERR, INIT)	59	77	J16	P8	89	364
VCC	60	78	J15	R10	90	-

* Indicates unconnected package pins.
† Contributes only one bit (.i) to the boundary scan register.

XC4013/XC4013D Pinouts (continued)

Pin Description	PQ160	MQ208	PG223	BG225	PQ240	Boundary Scan Order
GND	61	79	K15	R8	91	-
I/O	62	80	K16	L8	92	367
I/O	63	81	K17	M9	93	370
I/O	64	82	K18	P9	94	373
I/O	65	83	L18	R9	95	376
I/O	-	84	L17	K8	96	379
I/O	-	85	L16	L9	97	382
-	-	-	-	-	98*	-
I/O	-	-	L15	K9	99	385
I/O	-	-	M15	N9	100	388
VCC	-	-	-	-	101	-
I/O	66	86	M18	P10	102	391
I/O	67	87	M17	L10	103	394
I/O	68	88	N18	N10	104	397
I/O	69	89	P18	K10	105	400
GND	70	90	M16	R11	106	-
I/O	-	-	N15	N11	107	403
I/O	-	-	P15	P11	108	406
I/O	-	91	N17	M10	109	409
I/O	-	92	R18	P12	110	412
I/O	71	93	T18	R12	111	415
I/O	72	94	P17	N12	112	418
I/O	73	95	N16	K12	113	421
I/O	74	96	T17	P13	114	424
I/O	75	97	R17	R13	115	427
I/O	76	98	P16	P14	116	430
I/O	77	99	U18	K13	117	433
SGCK3 (I/O)	78	100	T16	M13	118	0
GND	79	101	R16	R15	119	-
-	-	102*	-	-	-	-
DONE	80	103	U17	R14	120	-
-	-	104*	-	-	-	-
-	-	105*	-	-	-	-
VCC	81	106	R15	K15	121	-
-	-	107*	-	-	-	-
PROG	82	108	V18	P15	122	-
I/O (D7)	83	109	T15	N14	123	439
PGCK3 (I/O)	84	110	U16	L13	124	442
I/O	85	111	T14	N13	125	445
I/O	86	112	U15	N15	126	448
I/O	-	-	R14	M11	127	451
I/O	-	-	R13	M14	128	454
I/O (D6)	87	113	V17	M12	129	457
I/O	88	114	V16	M15	130	460
I/O	89	115	T13	L11	131	463
I/O	90	116	U14	J12	132	466
I/O	-	117	V15	L14	133	469
I/O	-	118	V14	L12	134	472
GND	**91**	119	T12	L15	135	-
I/O	-	-	R12	J13	136	475
I/O	-	-	R11	K14	137	478
I/O	92	120	U13	K11	138	481
I/O	93	121	V13	H11	139	484
VCC	**-**	-	-	-	140	-
I/O (D5)	94	122	U12	J14	141	487
I/O (CSO)	95	123	V12	H12	142	490
-	-	-	-	-	143*	-
I/O	-	124	T11	J10	144	493
I/O	-	125	U11	J11	145	496
I/O	96	126	V11	J15	146	499
I/O	97	127	V10	H13	147	502
I/O (D4)	98	128	U10	J9	148	505
I/O	99	129	T10	H9	149	508
VCC	100	130	R10	H14	150	-

Pin Description	PQ160	MQ208	PG223	BG225	PQ240	Boundary Scan Order
GND	101	131	R9	H15	151	-
I/O (D3)	102	132	T9	H10	152	511
I/O (RS)	103	133	U9	G12	153	514
I/O	104	134	V9	G14	154	517
I/O	105	135	V8	G15	155	520
I/O	-	136	U8	G9	156	523
I/O	-	137	T8	G11	157	526
-	-	-	-	-	158*	-
I/O (D2)	106	138	V7	G10	159	529
I/O	107	139	U7	G13	160	532
VCC	**-**	-	-	-	161	-
I/O	108	140	V6	F14	162	535
I/O	109	141	U6	F11	163	538
I/O	-	-	R8	F13	164	541
I/O	-	-	R7	F10	165	544
GND	110	142	T7	E15	166	-
I/O	-	-	R6	E14	167	547
I/O	-	-	R5	F12	168	550
I/O	-	143	V5	D14	169	553
I/O	-	144	V4	E12	170	556
I/O	111	145	U5	D15	171	559
I/O	112	146	T6	D13	172	562
I/O (D1)	113	147	V3	E13	173	565
I/O (RCLK-BUSY/RDY)	114	148	V2	C13	174	568
I/O	115	149	U4	C15	175	571
I/O	116	150	T5	C14	176	574
I/O (D0, DIN)	117	151	U3	D10	177	577
SGCK4 (DOUT, I/O)	118	152	T4	C11	178	580
CCLK	119	153	V1	B15	179	-
VCC	120	154	R4	F15	180	-
-	-	155*	-	-	-	-
-	**-**	156*	-	-	-	-
-	**-**	157*	-	-	-	-
-	**-**	158*	-	-	-	-
TD0	121	159	U2	A14	181	-
GND	122	160	R3	A15	182	-
I/O (A0, WS)	123	161	T3	C12	183	2
PGCK4 (I/O, A1)	124	162	U1	C10	184	5
I/O	125	163	P3	B14	185	8
I/O	126	164	R2	A13	186	11
I/O (CS1, A2)	127	165	T2	B13	187	14
I/O (A3)	128	166	N3	B12	188	17
I/O	-	-	P4	D12	189	20
I/O	-	-	N4	A12	190	23
I/O	129	167	P2	E11	191	26
I/O	130	168	T1	D9	192	29
I/O	-	169	R1	B11	193	32
I/O	-	170	N2	D11	194	35
-	-	-	-	-	195*	-
GND	131	171	M3	A11	196	-
I/O	132	172	P1	C9	197	38
I/O	133	173	N1	B10	198	41
I/O	-	-	M4	E10	199	44
I/O	-	-	L4	D8	200	47
VCC	**-**	-	-	-	201	-
I/O (A4)	134	174	M2	B9	202	50
I/O (A5)	135	175	M1	C8	203	53
-	-	-	-	-	204*	-
I/O	-	176	L3	F9	205	56
I/O	136	177	L2	E9	206	59
I/O	137	178	L1	A9	207	62
I/O	138	179	K1	B8	208	65
I/O (A6)	139	180	K2	H8	209	68
I/O (A7)	140	181	K3	G8	210	71
GND	141	182	K4	A8	211	-

* Indicates unconnected package pins.

Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 583 = BSCAN.UPD

XC4020 Pinouts

Pin Description	HQ208	HQ240	PG233	PG299	Bound Scan
VCC	183	212	J4	K1	-
I/O (A8)	184	213	J3	K2	86
I/O (A9)	185	214	J2	K3	89
I/O	186	215	J1	K5	92
I/O	187	216	H1	K4	95
I/O	188	217	H2	J1	98
I/O	189	218	H3	J2	101
I/O (A10)	190	220	G1	H1	104
I/O (A11)	191	221	G2	J3	107
I/O	-	-	-	H2	110
I/O	-	-	-	G1	113
VCC	-	222	-	E1	-
I/O	-	223	H4	H3	116
I/O	-	224	G4	G2	119
I/O	192	225	F1	H4	122
I/O	193	226	E1	F2	125
GND	194	227	G3	F1	-
I/O	195	228	F2	D1	128
I/O	196	229	D1	G4	131
I/O	197	230	C1	E2	134
I/O	198	231	E2	F3	137
I/O (A12)	199	232	F3	G5	140
I/O (A13)	200	233	D2	C1	143
I/O	-	-	-	F4	146
I/O	-	-	-	E3	149
I/O	-	234	F4	D2	152
I/O	-	235	E4	C2	155
I/O	201	236	B1	F5	158
I/O	202	237	E3	E4	161
I/O (A14)	203	238	C2	D3	164
SGCK1(A15,I/O)	204	239	B2	C3	167
VCC	205	240	D3	A2	-
GND	2	1	D4	B1	-
PGCK1 (A16,I/O)	4	2	C3	D4	170
I/O (A17)	5	3	C4	B2	173
I/O	6	4	B3	B3	176
I/O	7	5	C5	E6	179
I/O (TDI)	8	6	A2	D5	182
I/O (TCK)	9	7	B4	C4	185
I/O	-	-	-	A3	188
I/O	-	-	-	D6	191
I/O	10	8	C6	E7	194
I/O	11	9	A3	B4	197
I/O	12	10	B5	C5	200
I/O	13	11	B6	A4	203
I/O	-	12	D5	D7	206
I/O	-	13	D6	C6	209
GND	14	14	C7	A5	-
I/O	15	15	A4	B6	212
I/O	16	16	A5	D8	215
I/O (TMS)	17	17	B7	C7	218
I/O	18	18	A6	B7	221
VCC	-	19	-	A6	-
I/O	-	20	D7	C8	224
I/O	-	21	D8	E9	227
I/O	-	-	-	B8	230
I/O	-	-	-	A8	233
I/O	19	23	C8	C9	236
I/O	20	24	A7	B9	239
I/O	21	25	B8	E10	242
I/O	22	26	A8	A9	245
I/O	23	27	B9	D10	248
I/O	24	28	C9	C10	251
GND	25	29	D9	A10	-
VCC	26	30	D10	A11	-
I/O	27	31	C10	B10	254
I/O	28	32	B10	B11	257
I/O	29	33	A9	C11	260
I/O	30	34	A10	E11	263
I/O	31	35	A11	D11	266
I/O	32	36	C11	A12	269
I/O	-	-	-	B12	272
I/O	-	-	-	A13	275
I/O	-	38	D11	E12	278
I/O	-	39	D12	B13	281
VCC	-	40	-	A16	-
I/O	33	41	B11	A14	284

Pin Description	HQ208	HQ240	PG233	PG299	Bound Scan
I/O	34	42	A12	C13	287
I/O	35	43	B12	B14	290
I/O	36	44	A13	D13	293
GND	37	45	C12	A15	-
I/O	-	46	D13	C14	296
I/O	-	47	D14	A17	299
I/O	38	48	B13	D14	302
I/O	39	49	A14	B16	305
I/O	40	50	A15	C15	308
I/O	41	51	C13	E14	311
I/O	-	-	-	A18	314
I/O	-	-	-	D15	317
I/O	42	52	B14	C16	320
I/O	43	53	A16	B17	323
I/O	44	54	B15	B18	326
I/O	45	55	C14	E15	329
I/O	46	56	A17	D16	332
SCGK2 (I/O)	47	57	B16	C17	335
O (M1)	48	58	C15	A20	338
GND	49	59	D15	A19	-
I (M0)	50	60	A18	C18	341
VCC	55	61	D16	B20	-
I (M2)	56	62	C16	D17	342
PGCK2 (I/O)	57	63	B17	B19	343
I/O (HDC)	58	64	E16	C19	346
I/O	59	65	C17	F16	349
I/O	60	66	D17	E17	352
I/O	61	67	B18	D18	355
I/O (LDC)	62	68	E17	C20	358
I/O	-	-	-	F17	361
I/O	-	-	-	G16	364
I/O	63	69	F16	D19	367
I/O	64	70	C18	E18	370
I/O	65	71	D18	D20	373
I/O	66	72	F17	G17	376
I/O	-	73	E15	F18	379
I/O	-	74	F15	H16	382
GND	67	75	G16	E20	-
I/O	68	76	E18	H17	385
I/O	69	77	F18	G18	388
I/O	70	78	G17	G19	391
I/O	71	79	G18	H18	394
VCC	-	80	-	F20	-
I/O	72	81	H16	J16	397
I/O	73	82	H17	G20	400
I/O	-	-	-	H20	403
I/O	-	-	-	J18	406
I/O	-	84	G15	J19	409
I/O	-	85	H15	K16	412
I/O	74	86	H18	J20	415
I/O	75	87	J18	K17	418
I/O	76	88	J17	K18	421
I/O (ERR, INIT)	77	89	J16	K19	424
VCC	78	90	J15	L20	-
GND	79	91	K15	K20	-
I/O	80	92	K16	L19	427
I/O	81	93	K17	L18	430
I/O	82	94	K18	L16	433
I/O	83	95	L18	L17	436
I/O	84	96	L17	M20	439
I/O	85	97	L16	M19	442
I/O	-	-	-	N20	445
I/O	-	-	-	M18	448
I/O	-	99	L15	N19	451
I/O	-	100	M15	P20	454
VCC	-	101	-	T20	-
I/O	86	102	M18	N18	457
I/O	87	103	M17	P19	460
I/O	88	104	N18	N17	463
I/O	89	105	P18	R19	466
GND	90	106	M16	R20	-
I/O	-	107	N15	U20	469
I/O	-	108	P15	P17	472
I/O	91	109	N17	T19	475
I/O	92	110	R18	R18	478
I/O	93	111	T18	P16	481
I/O	94	112	P17	V20	484

Pin Description	HQ208	HQ240	PG233	PG299	Bound Scan
I/O	-	-	-	R17	487
I/O	-	-	-	T18	490
I/O	95	113	N16	U19	493
I/O	96	114	T17	V19	496
I/O	97	115	R17	R16	499
I/O	98	116	P16	T17	502
I/O	99	117	U18	U18	505
SGCK3 (I/O)	100	118	T16	X20	508
GND	101	119	R16	W20	-
DONE	103	120	U17	V18	-
VCC	106	121	R15	X19	-
PROG	108	122	V18	U17	-
I/O (D7)	109	123	T15	W19	511
PGCK3 (I/O)	110	124	U16	W18	514
I/O	111	125	T14	T15	517
I/O	112	126	U15	U16	520
I/O	-	127	R14	V17	523
I/O	-	128	R13	X18	526
I/O	-	-	-	U15	529
I/O	-	-	-	T14	532
I/O (D6)	113	129	V17	W17	535
I/O	114	130	V16	V16	538
I/O	115	131	T13	X17	541
I/O	116	132	U14	U14	544
I/O	117	133	V15	V15	547
I/O	118	134	V14	T13	550
GND	119	135	T12	X16	-
I/O	-	136	R12	U13	553
I/O	-	137	R11	V14	556
I/O	120	138	U13	W14	559
I/O	121	139	V13	V13	562
VCC	-	140	-	X15	-
I/O (D5)	122	141	U12	T12	565
I/O (CS0)	123	142	V12	X14	568
I/O	-	-	-	X13	571
I/O	-	-	-	V12	574
I/O	124	144	T11	W12	577
I/O	125	145	U11	T11	580
I/O	126	146	V11	X12	583
I/O	127	147	V10	U11	586
I/O (D4)	128	148	U10	V11	589
I/O	129	149	T10	W11	592
VCC	130	150	R10	X10	-
GND	131	151	R9	X11	-
I/O (D3)	132	152	T9	W10	595
I/O (RS)	133	153	U9	V10	598
I/O	134	154	V9	T10	601
I/O	135	155	V8	U10	604
I/O	136	156	U8	X9	607
I/O	137	157	T8	W9	610
I/O	-	-	-	X8	613
I/O	-	-	-	V9	616
I/O (D2)	138	159	V7	W8	619
I/O	139	160	U7	X7	622
VCC	-	161	-	X5	-
I/O	140	162	V6	V8	625
I/O	141	163	U6	W7	628
I/O	-	164	R8	U8	631
I/O	-	165	R7	W6	634
GND	142	166	T7	X6	-
I/O	-	167	R6	X4	637
I/O	-	168	R5	U7	640
I/O	143	169	V5	W5	643
I/O	144	170	V4	V6	646
I/O	145	171	U5	T7	-
I/O	146	172	T6	X3	649
I/O (D1)	147	173	V3	U6	652
I/O (RCLK-BUSY/RDY)	148	174	V2	V5	655
I/O	-	-	-	W4	658
I/O	-	-	-	W3	661
I/O	149	175	U4	T6	664
I/O	150	176	T5	U5	667
I/O (D0, DIN)	151	177	U3	V4	670
SGCK4 (DOUT, I/O)	152	178	T4	X1	673
CCLK	153	179	V1	V3	-
VCC	154	180	R4	W1	-
TDO	159	181	U2	U4	-

† Contributes only one bit (.i) to the boundary scan register.

XC4020 Pinouts (continued)

Pin Description	HQ208	HQ240	PG233	PG299	Bound Scan
GND	160	182	R3	X2	-
I/O (A0, WS)	161	183	T3	W2	2
PGCK4 (I/O, A1)	162	184	U1	V2	5
I/O	163	185	P3	R5	8
I/O	164	186	R2	T4	11
I/O (CS1, A2)	165	187	T2	U3	14
I/O (A3)	166	188	N3	V1	17
I/O	-	-	-	R4	20
I/O	-	-	-	P5	23
I/O	-	189	P4	U2	26
I/O	-	190	N4	T3	29

Pin Description	HQ208	HQ240	PG233	PG299	Bound Scan
I/O	167	191	P2	U1	32
I/O	168	192	T1	P4	35
I/O	169	193	R1	R3	38
I/O	170	194	N2	N5	41
GND	171	196	M3	T1	-
I/O	172	197	P1	N4	44
I/O	173	198	N1	P3	47
I/O	-	199	M4	P2	50
I/O	-	200	L4	N3	53
VCC	-	201	-	R1	-
I/O	-	-	-	M5	56

Pin Description	HQ208	HQ240	PG233	PG299	Bound Scan
I/O	-	-	-	P1	59
I/O (A4)	174	202	M2	N1	62
I/O (A5)	175	203	M1	M3	65
I/O	176	205	L3	M2	68
I/O	177	206	L2	L5	71
I/O	178	207	L1	M1	74
I/O	179	208	K1	L4	77
I/O (A6)	180	209	K2	L3	80
I/O (A7)	181	210	K3	L2	83
GND	182	211	K4	L1	-

XC4025 Pinouts

Pin Description	PG 223	MQ 240	PG 299	HQ 304	Bound Scan
VCC	J4	212	K1	38	-
I/O (A8)	J3	213	K2	37	98
I/O (A9)	J2	214	K3	36	101
I/O	J1	215	K5	35	104
I/O	H1	216	K4	34	107
I/O	H2	217	J1	33	110
I/O	H3	218	J2	32	113
GND	-	219	-	-	-
I/O (A10)	G1	220	H1	31	116
I/O (A11)	G2	221	J3	30	119
I/O	-	-	J4	29	122
I/O	-	-	J5	28	125
I/O	-	-	H2	27	128
I/O	-	-	G1	26	131
VCC	-	222	E1	25	-
I/O	H4	223	H3	23	134
I/O	G4	224	G2	22	137
I/O	F1	225	H4	21	140
I/O	E1	226	F2	20	143
GND	G3	227	F1	19	-
I/O	-	-	H5	18	146
I/O	-	-	G3	17	149
I/O	F2	228	D1	16	152
I/O	D1	229	G4	15	155
I/O	C1	230	E2	14	158
I/O	E2	231	F3	13	161
I/O (A12)	F3	232	G5	12	164
I/O (A13)	D2	233	C1	10	167
I/O	-	-	F4	9	170
I/O	-	-	E3	8	173
I/O	F4	234	D2	7	176
I/O	E4	235	C2	6	179
I/O	B1	236	F5	5	182
I/O	E3	237	E4	4	185
I/O (A14)	C2	238	D3	3	188
SGCK1 (A15, I/O)	B2	239	C3	2	191
VCC	D3	240	A2	1	-
GND	D4	1	B1	304	-
PGCK1 (A16, I/O)	C3	2	D4	303	194
VCC	-	-	E5	-	-
I/O (A17)	C4	3	B2	302	197
I/O	B3	4	B3	301	200
I/O	C5	5	E6	300	203
I/O (TDI)	A2	6	D5	299	206
I/O (TCK)	B4	7	C4	298	209
I/O	-	-	A3	297	212
I/O	-	-	D6	296	215
I/O	C6	8	E7	295	218
I/O	A3	9	B4	294	221
I/O	B5	10	C5	293	224
I/O	B6	11	A4	292	227
I/O	D5	12	D7	291	230
I/O	D6	13	C6	290	233
I/O	-	-	E8	289	236
I/O	-	-	B5	288	239
GND	C7	14	A5	287	-
I/O	A4	15	B6	286	242
I/O	A5	16	D8	285	245
I/O (TMS)	B7	17	C7	284	248
I/O	A6	18	B7	283	251

Pin Description	PG 223	MQ 240	PG 299	HQ 304	Bound Scan
VCC	-	19	A6	-	-
I/O	D7	20	C8	280	254
I/O	D8	21	E9	279	257
GND	-	22	-	-	-
I/O	-	-	A7	278	260
I/O	-	-	D9	277	263
I/O	-	-	B8	276	266
I/O	-	-	A8	275	269
I/O	C8	23	C9	274	272
I/O	A7	24	B9	273	275
I/O	B8	25	E10	272	278
I/O	A8	26	A9	271	281
I/O	B9	27	D10	270	284
I/O	C9	28	C10	269	287
GND	D9	29	A10	268	-
VCC	D10	30	A11	267	-
I/O	C10	31	B10	266	290
I/O	B10	32	B11	265	293
I/O	A9	33	C11	264	296
I/O	A10	34	E11	263	299
I/O	A11	35	D11	262	302
I/O	C11	36	A12	261	305
I/O	-	-	B12	260	308
I/O	-	-	A13	259	311
I/O	-	-	C12	258	314
I/O	-	-	D12	257	317
GND	-	37	-	-	-
I/O	D11	38	E12	256	320
I/O	D12	39	B13	255	323
VCC	-	40	A16	-	-
I/O	B11	41	A14	252	326
I/O	A12	42	C13	251	329
I/O	B12	43	B14	250	332
I/O	A13	44	D13	249	335
GND	C12	45	A15	248	-
I/O	-	-	B15	247	338
I/O	-	-	E13	246	341
I/O	D13	46	C14	245	344
I/O	D14	47	A17	244	347
I/O	B13	48	D14	243	350
I/O	A14	49	B16	242	353
I/O	A15	50	C15	241	356
I/O	C13	51	E14	240	359
I/O	-	-	A18	239	362
GND	C15	58	A20	231	386
GND	D15	59	A19	230	-
I/O	A18	60	C18	229	389†
VCC	D16	61	B20	228	-
I/O	C16	62	D17	227	390†
I/O	B17	63	B19	226	391
I/O	E16	64	C19	225	394
GND	-	-	E16	-	-
I/O	C17	65	F16	224	397

Pin Description	PG 223	MQ 240	PG 299	HQ 304	Bound Scan
I/O	D17	66	E17	223	400
I/O	B18	67	D18	222	403
I/O (LDC)	E17	68	C20	221	406
I/O	-	-	F17	220	409
I/O	-	-	G16	219	412
I/O	F16	69	D19	218	415
I/O	C18	70	E18	217	418
I/O	D18	71	D20	216	421
I/O	F17	72	G17	215	424
I/O	E15	73	F18	214	427
I/O	F15	74	H16	213	430
I/O	-	-	E19	212	433
I/O	-	-	F19	211	436
GND	G16	75	E20	210	-
I/O	E18	76	H17	209	439
I/O	F18	77	G18	208	442
I/O	G17	78	G19	207	445
I/O	G18	79	H18	206	448
VCC	-	80	F20	204	-
I/O	H16	81	J16	203	451
I/O	H17	82	G20	202	454
GND	-	83	-	-	-
I/O	-	-	J17	201	457
I/O	-	-	H19	200	460
I/O	-	-	H20	199	463
I/O	-	-	J18	198	466
I/O	G15	84	J19	197	469
I/O	H15	85	K16	196	472
I/O	H18	86	J20	195	475
I/O	J18	87	K17	194	478
I/O (ERR, INIT)	J16	89	K19	192	484
VCC	J15	90	L20	191	-
GND	K15	91	K20	190	-
I/O	K16	92	L19	189	487
I/O	K17	93	L18	188	490
I/O	K18	94	L16	188	493
I/O	L18	95	L17	187	496
I/O	L17	96	M20	185	499
I/O	L16	97	M19	184	502
I/O	-	-	N20	183	505
I/O	-	-	M18	182	508
I/O	-	-	M17	181	511
I/O	-	-	M16	180	514
GND	L15	98	-	179	-
I/O	M15	99	N19	178	517
I/O	-	100	-	-	520
VCC	-	101	T20	177	-
I/O	M18	102	N18	175	523
I/O	M17	103	P19	174	526
I/O	N18	104	N17	173	529
I/O	P18	105	R19	172	532
GND	M16	106	R20	171	-
I/O	-	-	N16	170	535
I/O	-	-	P18	169	538
I/O	N15	107	U20	168	541
I/O	P15	108	P17	167	544
I/O	N17	109	T19	166	547
I/O	R18	110	R18	165	550
I/O	T18	111	P16	164	553

Pin Description	PG 223	MQ 240	PG 299	HQ 304	Bound Scan
I/O	P17	112	V20	163	556
I/O	-	-	R17	162	559
I/O	-	-	T18	161	562
I/O	N16	113	U19	160	565
I/O	T17	114	V19	159	568
I/O	R17	115	R16	158	571
I/O	P16	116	T17	157	574
I/O	U18	117	U18	156	577
SGCK3 (I/O)	T16	118	X20	155	580
VCC	R16	-	T16	154	-
GND	-	119	W20	-	-
DONE	U17	120	V18	153	-
VCC	R15	121	X19	152	-
PROG	V18	122	U17	151	-
I/O (D7)	T15	123	W19	150	583
PGCK3 (I/O)	U16	124	W18	149	586
I/O	T14	125	T15	148	589
I/O	U15	126	U16	147	592
I/O	R14	127	V17	146	595
I/O	R13	128	X18	145	598
I/O	-	-	U15	144	601
I/O	-	-	T14	143	604
I/O (D6)	V17	129	W17	142	607
I/O	V16	130	V16	141	610
I/O	T13	131	X17	140	613
I/O	U14	132	U14	139	616
I/O	V15	133	V15	138	619
I/O	V14	134	T13	137	622
I/O	-	-	W16	136	625
I/O	-	-	W15	135	628
GND	T12	135	X16	134	-
I/O	R12	136	U13	133	631
I/O	R11	137	V14	132	634
I/O	U13	138	W14	131	637
I/O	V13	139	V13	130	640
VCC	-	140	X15	-	-
I/O (D5)	U12	141	T12	127	643
I/O (CS0)	V12	142	X14	126	646
GND	-	143	-	-	-
I/O	-	-	U12	125	649
I/O	-	-	W13	124	652
I/O	-	-	X13	123	655
I/O	-	-	V12	122	658
I/O	T11	144	W12	121	661
I/O	U11	145	T11	120	664
I/O	V11	146	X12	119	667
I/O	V10	147	U11	118	670
I/O (D4)	U10	148	V11	117	673
I/O	T10	149	W11	116	676
VCC	R10	150	X10	115	-
GND	R9	151	X11	114	-
I/O (D3)	T9	152	W10	113	679
I/O (RS)	U9	153	V10	112	682
I/O	V9	154	T10	111	685
I/O	V8	155	U10	110	688
I/O	U8	156	X9	109	691
I/O	T8	157	W9	108	694
I/O	-	-	X8	107	697
I/O	V9	106	700		
I/O	U9	105	703		

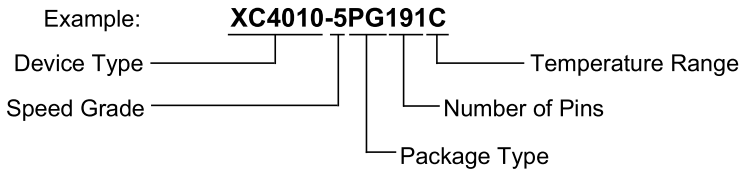
Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 775 = BSCAN.UPD

XC4025 Pinouts (continued)

Pin Description	PG 223	MQ 240	PG 299	HQ 304	Bound Scan	Pin Description	PG 223	MQ 240	PG 299	HQ 304	Bound Scan	Pin Description	PG 223	MQ 240	PG 299	HQ 304	Bound Scan	Pin Description	PG 223	MQ 240	PG 299	HQ 304	Bound Scan
I/O	-	-	T9	104	706	I/O	T6	172	X3	87	745	I/O	R2	186	T4	71	11	I/O	L4	200	N3	54	59
GND	-	158	-	-	-	I/O (D1)	V3	173	U6	86	748	I/O (CS1, A2)	T2	187	U3	70	14	**VCC**	-	201	R1	52	-
I/O (D2)	V7	159	W8	103	709	I/O (RCLK-BUSY/RDY)	V2	174	V5	85	751	I/O (A3)	N3	188	V1	69	17	I/O	-	-	M5	51	62
I/O	U7	160	X7	102	712	I/O	-	-	W4	84	754	I/O	-	-	R4	68	20	I/O	-	-	P1	50	65
VCC	-	161	X5	-	-	I/O	-	-	W3	83	757	I/O	-	-	P5	67	23	I/O	-	-	M4	49	68
I/O	V6	162	V8	99	715	I/O	U4	175	T6	82	760	I/O	P4	189	U2	66	26	I/O	-	-	N2	48	71
I/O	U6	163	W7	98	718	I/O	T5	176	U5	81	763	I/O	N4	190	T3	65	29	I/O (A4)	M2	202	N1	47	74
I/O	R8	164	U8	97	721	I/O (D0, DIN)	U3	177	V4	80	766	I/O	P2	191	U1	64	32	I/O (A5)	M3	203	M3	46	77
I/O	R7	165	W6	96	724	SGCK4 (DOUT, I/O)	T4	178	X1	79	769	I/O	T1	192	P4	63	35	**GND**	-	204	-	-	-
GND	T7	166	X6	95	-	CCLK	V1	179	V3	78	-	I/O	R1	193	R3	62	38	I/O	L3	205	M2	45	80
I/O	-	-	T8	94	727	**GND**	-	-	T5	-	-	I/O	N2	194	N5	61	41	I/O	L2	206	L5	44	83
I/O	-	-	V7	93	730	**VCC**	R4	180	W1	77	-	I/O	-	195	T2	60	44	I/O	L1	207	M1	43	86
I/O	R6	167	X4	92	733	TDO	U2	181	U4	76		I/O	-	-	R2	59	47	I/O	K1	208	L4	42	89
I/O	R5	168	U7	91	736	**GND**	R3	182	X2	75	-	**GND**	M3	196	T1	58	-	I/O (A6)	K2	209	L3	41	92
I/O	V5	169	W5	90	739	I/O (A0, WS)	T3	183	W2	74	2	I/O	P1	197	N4	57	50	I/O (A7)	K3	210	L2	40	95
I/O	V4	170	V6	89	742	PGCK4 (I/O, A1)	U1	184	V2	73	5	I/O	N1	198	P3	56	53	**GND**	K4	211	L1	39	-
I/O	U5	171	T7	88	-	I/O	P3	185	R5	72	8	I/O	M4	199	P2	55	56						

For a detailed description of the device architecture, see pages 2-9 through 2-31.
For a detailed description of the configuration modes and their timing, see pages 2-32 through 2-55.
For detailed lists of package pinouts, see pages 2-57 through 2-67.
For package physical dimensions and thermal data, see Section 4.

Ordering Information



Component Availability

PINS		84	100			120	144	156	160	164	191	196	208		223	225	240		299	304
TYPE		PLAST. PLCC	PLAST. PQFP	PLAST. VQFP	TOP BRAZED CQFP	CERAM. PGA	PLAST. TQFP	CERAM PGA	PLAST. PQFP	TOP BRAZED CQFP	CERAM. PGA	TOP BRAZED CQFP	PLAST. PQFP	METAL PQFP	CERAM. PGA	PLAST. BGA	PLAST. PQFP	METAL PQFP	CERAM. PGA	CERAM. PGA
CODE		PC84	PQ100	VQ100	CB100	PG120	TQ144	PG156	PQ160	CB164	PG191	CB196	PQ208	MQ208	PG223	BG225	PQ240	MQ240	PG299	HQ304
XC4003	-6	C I	C I			C I														
	-5	C	C			C														
	-4	C	C			C														
XC4005	-10							M B		M B										
	-6	C I	C I					C I M B	C I	M B			C I							
	-5	C I	C I					C I	C I				C I							
	-4	C	C					C	C				C							
XC4006	-6	C I						C I	C I				C I							
	-5	C I						C I	C I				C I							
	-4	C						C	C				C							
XC4008	-6	C I							C I		C I		C I	C I						
	-5	C I							C I		C		C I	C I						
	-4	C							C		C		C	C						
XC4010	-10										M B	M B								
	-6	C I							C I		C I M B	M B	C I	C I		C I				
	-5	C I							C I		C I		C I	C I		C I				
	-4	C							C		C		C	C		C				
XC4010D	-6	C I							C I				C I			C I				
	-5	C I							C I				C I			C I				
	-4	C							C				C			C				
XC4013	-6								C I				C I	C I	C I (M B)	C I	C I	C I		
	-5								C I				C I	C I	C I	C I	C I	C I		
	-4								C				C	C	C	C	C	C		
XC4013D	-6								C I				C I			C I	C I			
	-5								C I				C I			C I	C I			
	-4								C				C			C	C			
XC4020	-6												(C I)		(C I)		(C I)		(C I)	
	-5												(C I)		(C I)		(C I)		(C I)	
	-4												(C)		(C)		(C)		(C)	
XC4025	-6														C I			C I	C I	C
	-5														C I			C I	C I	C
	-4																			

C = Commercial = 0° to +85° C I = Industrial = -40° to +100° C M = Mil Temp = -55° to +125° C
B = MIL-STD-883C Class B Parentheses indicates future product plans