XR-2211

FSK Demodulator/Tone Decoder

The XR-2211 is a monolithic phase-locked loop (PLL) system especially designed for data communications. It is particularly well suited for FSK modem applications. It operates over a wide supply voltage range of 4.5 to 20V and a wide frequency range of 0.01 Hz to 300 kHz. It can accommodate analog signals between 2 mV and 3V, and can interface with conventional DTL, TTL and ECL logic families. The circuit consists of a basic PLL for tracking an input signal within the pass band, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set center frequency, bandwidth, and output delay.

FEATURES

Wide Frequency Range	0.01 Hz to 300 kHz
Wide Supply Voltage Range	4.5V to 20V
DTL/TTL/ECL Logic Compatibility	
FSK Demodulation, with Carrier-Detection	
Wide Dynamic Range	2 mV to 3 Vrms
Adjustable Tracking Range (±1% to ±80%)	
Excellent Temp. Stability	20 ppm/°C, typ.

APPLICATIONS

FSK Demodulation
Data Synchronization
Tone Decoding
FM Detection
Carrier Detection

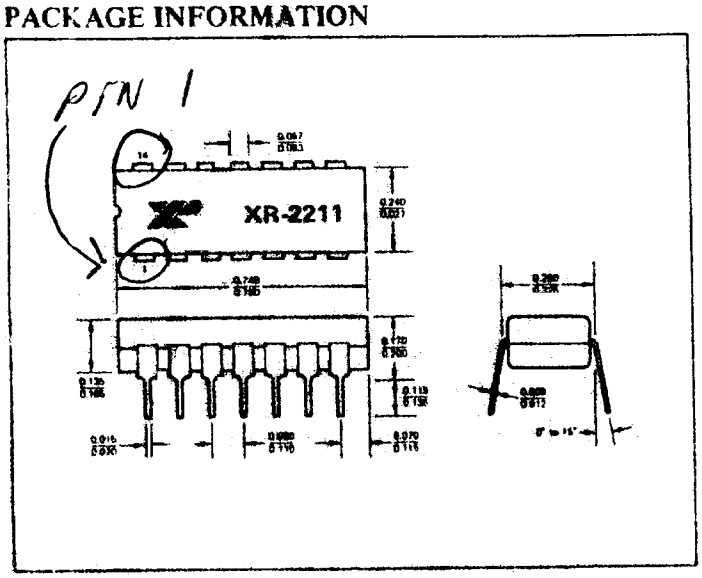
ABSOLUTE MAXIMUM RATINGS

Power Supply	20V
Input Signal Level	3V rms
Power Dissipation	
Ceramic Package:	750 mW
Derate above $T_A = +25°C$	6 mW/°C
Plastic Package:	625 mW
Derate above $T_A = +25°C$	5.0 mW/°C

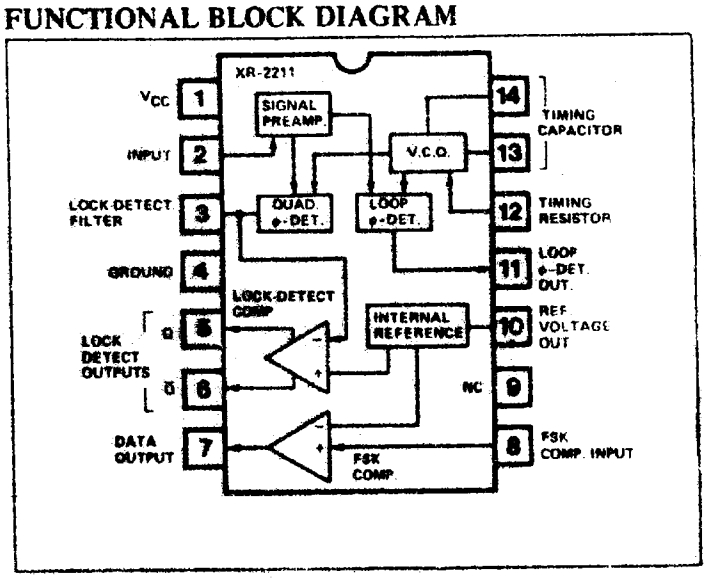
AVAILABLE TYPES

Part Number	Package	Operating Temperature
XR-2211M	Ceramic	-55°C to +125°C
XR-2211CN	Ceramic	0°C to +75°C
XR-2211CP	Plastic	0°C to +75°C
XR-2211N	Ceramic	-40°C to +85°C
XR-2211P	Plastic	-40°C to +85°C

PACKAGE INFORMATION



FUNCTIONAL BLOCK DIAGRAM



CHARACTERISTICS

Conditions: $V^+ = +12V$, $T_A = +25°C$, $R_0 = 30\ K\Omega$, $C_0 = 0.033\ \mu F$. See Fig. 2 for component designation

CHARACTERISTICS	XR-2211/2211M			XR-2211C			UNITS	CONDITIONS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
GENERAL								
Supply Voltage	4.5		20	4.5		20	V	
Supply Current		4	7		5	9	mA	$R_0 \geq 10\ K\Omega$. See Fig. 4
OSCILLATOR SECTION								
Frequency Accuracy		±1	±3		±1		%	Deviation from $f_0 = 1/R_0C_0$
Frequency Stability								$R_1 = \infty$
Temperature		±20	±50		±20		ppm/°C	See Fig. 8.
Power Supply		0.05	0.5		0.05		%/V	$V^+ = 12 \pm 1V$. See Fig. 7.
		0.2			0.2		%/V	$V^+ = 5 \pm 0.5V$. See Fig. 7.
Upper Frequency Limit	100	300			300		kHz	$R_0 = 8.2\ K\Omega$, $C_0 = 400\ pF$
Lowest Practical								
Operating Frequency			0.01		0.01		Hz	$R_0 = 2\ M\Omega$, $C_0 = 50\ \mu F$
Timing Resistor, R_0								See Fig. 5.
Operating Range	5		2000	5		2000	KΩ	
Recommended Range	15		100	15		100	KΩ	See Fig. 7 and 8.
LOOP PHASE DETECTOR SECTION								
Peak Output Current	±150	±200	±300	±100	±200	±300	μA	Measured at Pin 11.
Output Offset Current		±1			±2		μA	
Output Impedance		1			1		MΩ	
Maximum Swing	±4	±5		±4	±5		V	Referenced to Pin 10.
QUADRATURE PHASE DETECTOR								
Peak Output Current	100	150			150		μA	Measured at Pin 3.
Output Impedance		1			1		MΩ	
Maximum Swing		11			11		Vpp	
INPUT PREAMP SECTION								
Input Impedance		20			20		KΩ	Measured at Pin 2.
Input Signal								
Voltage Required to Cause Limiting		2	10		2		mV rms	
VOLTAGE COMPARATOR SECTIONS								
Input Impedance		2			2		MΩ	
Input Bias Current		100			100		nA	Measured at Pins 3 and 8.
Voltage Gain	55	70		55	70		dB	$R_L = 5.1\ K\Omega$
Output Voltage Low		300			300		mV	$I_C = 3\ mA$
Output Leakage Current		.01			.01		μA	$V_O = 12V$
INTERNAL REFERENCE								
Voltage Level	4.9	5.3	5.7	4.75	5.3	5.85	V	Measured at Pin 10.
Output Impedance		100			100		Ω	

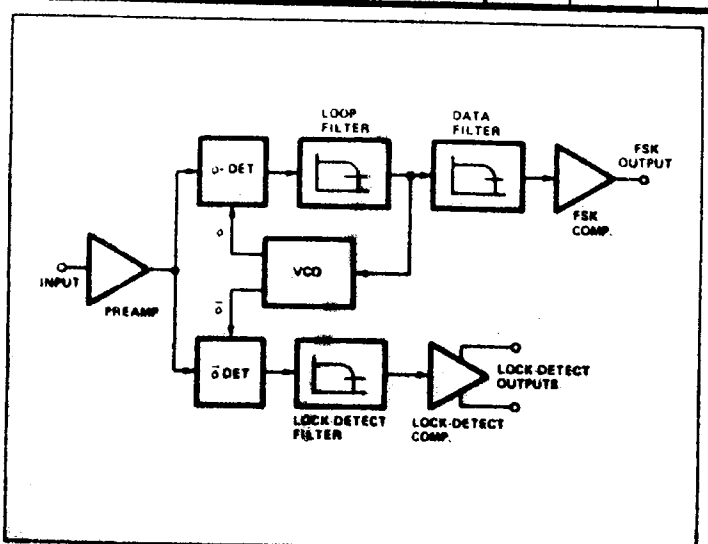


Figure 1. Functional Block Diagram of a Tone and FSK Decoding System Using XR-2211.

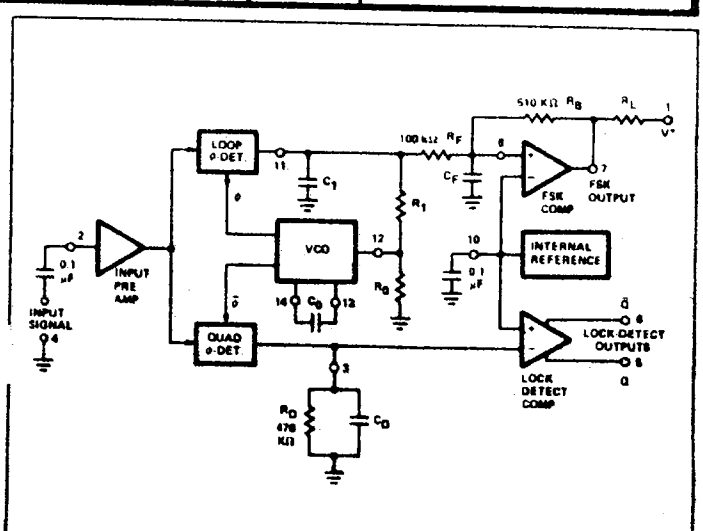


Figure 2. Generalized Circuit Connection for FSK and Tone Detection.

XR-2211 FSK Demodulator/Tone Decoder

Description

The XR-2211 is a monolithic phase-locked loop (PLL) system especially designed for data communications. It is particularly well suited for FSK modem applications. It operates over a wide supply voltage range of 4.5 to 20 V and a wide frequency range of 0.01 Hz to 300 kHz. It can accommodate analog signals between 2 mV and 3 V, and can interface with conventional DTL, TTL, and ECL logic families. The circuit consists of a basic PLL for tracking an input signal within the pass band, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set center frequency, bandwidth, and output delay.

Features

• Wide Frequency Range	0.01 Hz to 300 kHz
• Wide Supply Voltage Range	4.5 V to 20 V
• DTL/TTL/ECL Logic Compatibility	
• FSK Demodulation, with Carrier Detection	
• Wide Dynamic Range	2 mV to 3 V rms
• Adjustable Tracking Range (±1% to ±80%)	
• Excellent Temp. Stability	20 ppm/°C, typ.

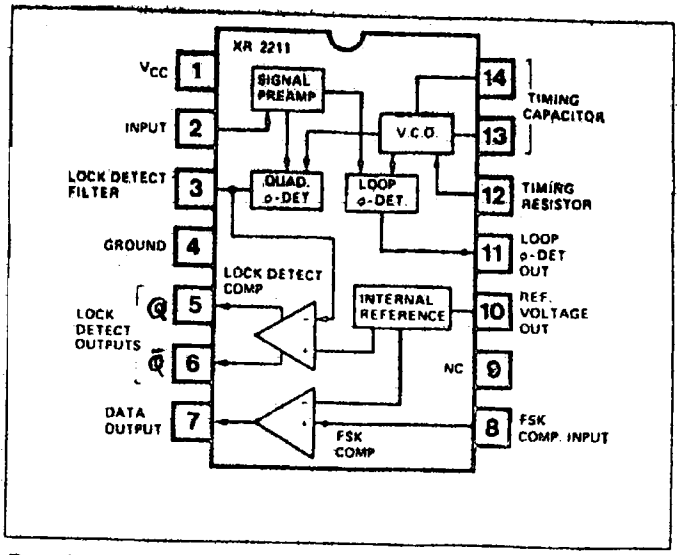
Applications

- FSK Demodulation
- Data Synchronization
- Tone Decoding
- FM Detection
- Carrier Detection

Absolute Maximum Ratings

Power Supply	20 V
Input Signal Level	3 V rms
Power Dissipation	625 mW
• Derate above T_A = +25°C	5.0 mW/°C
Operating Temperature	0°C to + 75°C

Functional Block Diagram



Description Of Circuit Controls

Signal Input (Pin 2): Signal is ac coupled to this terminal. The internal impedance at Pin 2 is 20 KΩ. Recommended input signal level is in the range of 10 mV rms to 3 V rms.

Quadrature Phase Detector Output (Pin 3): This is the pedance output of quadrature phase detector and is internally connected to the input of lock detect voltage comparator. In tone detection applications, Pin 3 is connected to ground through a parallel combination of R_D and C_D (see Figure 2) to eliminate the chatter at lock detect outputs. If the tone detect section is not used, Pin 3 can be left open circuited.

Lock Detect Output, Q (Pin 5): The output at Pin 5 is at "high" state when the PLL is out of lock and goes to "low" or conducting state when the PLL is locked. It is an open collector type output and requires a pull-up resistor, R_L, to V+ for proper operation. At "low" state, it can sink up to 5 mA of load current.

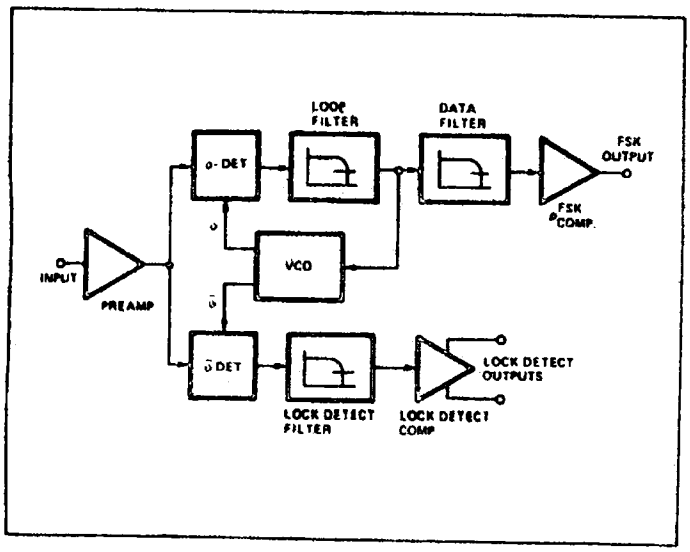


Figure 1: Functional Block Diagram of a Tone and FSK Decoding System Using XR-2211.

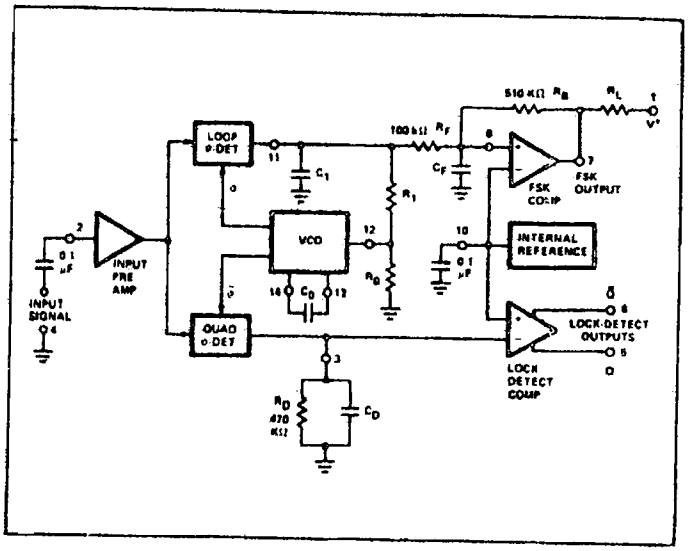


Figure 2: Generalized Circuit Connection for FSK and Tone Detection.

logic complement of the lock detect output at Pin 5. This output is also an open collector type stage which can sink 5 mA of load current at low or "on" state.

FSK Data Output (Pin 7): This output is an open collector logic stage which requires a pull-up resistor, R_L, to V+ for proper operation. It can sink 5 mA of load current. When decoding FSK signals, FSK data output is at "high" or "off" state for low input frequency, and at "low" or "on" state for high input frequency. If no input signal is present, the logic state at Pin 7 is indeterminate.

FSK Comparator Input (Pin 8): This is the high impedance input to the FSK voltage comparator. Normally, an FSK post-detection or data filter is connected between this terminal and the PLL phase detector output (Pin 11). This data filter is formed by R_F and C_F Figure 2. The threshold voltage of the comparator is set by the internal reference voltage, V_R, available at Pin 10.

Reference Voltage, V_R (Pin 10): This pin is internally biased at the reference voltage level, V_R: V_R = V+/2 – 650 mV. The dc voltage level at this pin forms an internal reference for the voltage levels at Pins 5, 8, 11 and 12. Pin 10 *must* be bypassed to ground with a 0.1 μF capacitor for proper operation of the circuit.

Loop Phase Detector Output (Pin 11): This terminal provides a high impedance output for the loop phase detector. The PLL loop filter is formed by R_1 and C_1 connected to Pin 11 (see Figure 2). With no input signal, or with no phase error within the PLL, the dc level at Pin 11 is very nearly equal to V_R. The peak voltage swing available at the phase detector output is equal to $\pm V_R$.

VCO Control Input (Pin 12): VCO free-running frequency is determined by external timing resistor, R_0, connected from this terminal to ground. The VCO free-running frequency, f_0, is:

$$f_0 = \frac{1}{R_0 C_0} \quad \text{Hz}$$

where C_0 is the timing capacitor across Pins 13 and 14. For optimum temperature stability, R_0 must be in the range of 10 KΩ to 100 KΩ.

This terminal is a low impedance point, and is internally biased at a dc level equal to V_R. The maximum timing current drawn from Pin 12 must be limited to $\leq$ 3 mA for proper operation of the circuit.

VCO Timing Capacitor (Pins 13 and 14): VCO frequency is inversely proportional to the external timing capacitor, C_0, connected across these terminals (see Figure 4). C_0 must be nonpolar, and in the range of 200 pF to 10 μF.

VCO Frequency Adjustment: VCO can be fine-tuned by connecting a potentiometer, R_X, in series with R_0 at Pin 12 (see Figure 6).

VCO Free-Running Frequency, f_0: XR-2211 does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase detector sections of the circuit. However, for set-up or adjustment purposes, VCO free-running frequency can be measured at Pin 3 (with C_0 disconnected), with no input and with Pin 2 shorted to Pin 10.

APPLICATIONS INFORMATION

FSK Decoding:

Figure 6 shows the basic circuit connection for FSK decoding. With reference to Figures 2 and 6, the functions of external components are defined as follows: R_0 and C_0 set the PLL center frequency R_1 sets the system band width, and C_1 sets the loop filter time constant and the loop damping factor. C_F and R_F form a one-pole post-detection filter for the FSK data output. The resistor R_B (= 510 KΩ) from Pin 7 to Pin 8 introduces positive feedback across FSK comparator to facilitate rapid transition between output logic states.

Recommended component values for some of the most commonly used FSK bands are given in Table I.

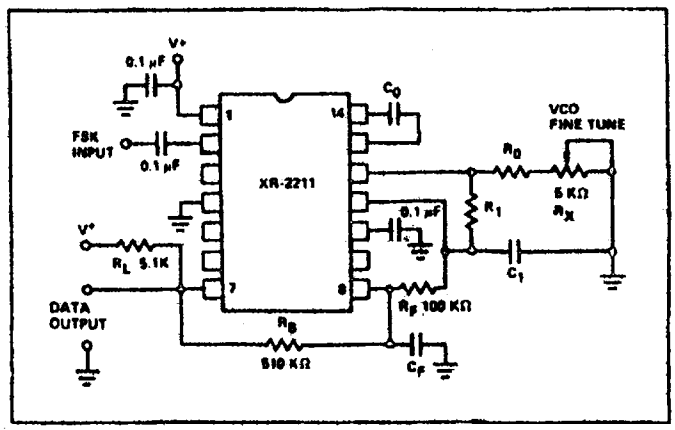


Figure 6: Circuit Connection for FSK Decoding.

Design Example:

75 Baud FSK demodulator with mark space frequencies of 1110/1170 Hz:

Step 1: Calculate f_0: f_0 = (1110 + 1170) (1/2) - 1140 Hz
Step 2: Choose R_0 = 20 KΩ (18 KΩ fixed resistor in series with 5 KΩ potentiometer)
Step 3: Calculate C_0 from Figure 5: C_0 = 0.044 μF
Step 4: Calculate R_1: R_1 = R_0 (2240/60) = 380 KΩ
Step 5: Calculate C_1: C_1 = C_0/4 = 0.011 μF

Note: All values except R_0 can be rounded to *nearest* standard value.

FSK BAND	COMPONENT VALUES	
300 Baud f_1 = 1070 Hz f_2 = 1270 Hz	C_0 = 0.039 μF C_1 = 0.01 μF R_1 = 100 KΩ	C_F = 0.005 μF R_0 = 18 KΩ
300 Baud f_1 = 2025 Hz f_2 = 2225 Hz	C_0 = 0.022 μF C_1 = 0.0047 μF R_1 = 200 KΩ	C_F = 0.005 μF R_0 = 18 KΩ
1200 Baud f_1 = 1200 Hz f_2 = 2200 Hz	C_0 = 0.027 μF C_1 = 0.01 μF R_1 = 30 KΩ	C_F = 0.0022 μF R_0 = 18 KΩ

Table 1: Recommended Component Values for Commonly Used FSK Bands. (See Circuit of Figure 6.)

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = +12$ V, $T_A = +25°C$, $R_0 = 30$ KΩ, $C_0 = 0.033$ μF. See Figure 2 for component designation.

PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
GENERAL					
Supply Voltage	4.5		20	V	
Supply Current		5	9	mA	$R_0 \geq 10$ KΩ
OSCILLATOR SECTION					
Frequency Accuracy		±1		%	Deviation from $f_0 = 1/R_0C_0$
Frequency Stability					$R_1 = \infty$
Temperature		±20		ppm/°C	
Power Supply		0.05		%/V	$V^+ = 12 \pm 1$ V.
		0.2		%/V	$V^+ = 5 \pm 0.5$ V.
Upper Frequency Limit		300		kHz	$R_0 = 8.2$ KΩ, $C_0 = 400$ pF
Lowest Practical					
Operating Frequency		0.01		Hz	$R_0 = 2$ MΩ, $C_0 = 50$ μF
Timing Resistor, R_0					
Operating Range	5		2000	KΩ	
Recommended Range	15		100	KΩ	
LOOP PHASE DETECTOR SECTION					
Peak Output Current	±100	±200	±300	μA	Measured at Pin 11.
Output Offset Current		±2		μA	
Output Impedance		1		MΩ	
Maximum Swing	±4	±5		V	Referenced to Pin 10.
QUADRATURE PHASE DETECTOR					Measured at Pin 3.
Peak Output Current		150		μA	
Output Impedance		1		MΩ	
Maximum Swing		11		V pp	
INPUT PREAMP SECTION					Measured at Pin 2.
Input Impedance		20		KΩ	
Input Signal					
Voltage Required to Cause Limiting		2		mV rms	
VOLTAGE COMPARATOR SECTIONS					
Input Impedance		2		MΩ	Measured at Pins 3 and 8.
Input Bias Current		100		nA	
Voltage Gain		70		dB	$R_L = 5.1$ KΩ
Output Voltage Low		300		mV	$I_C = 3$ mA
Output Leakage Current		0.01		μA	$V_O = 12$ V
INTERNAL REFERENCE					
Voltage Level	4.75	5.3	5.85	V	Measured at Pin 10.
Output Impedance		100		Ω	

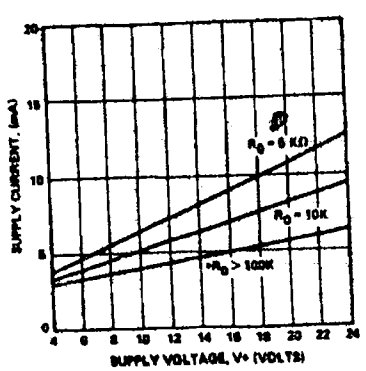


Figure 3: Typical Supply Current vs V^+ (Logic Outputs Open Circuited)

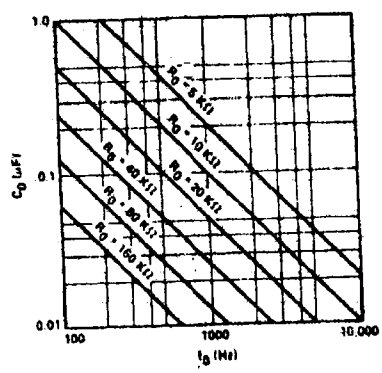


Figure 4: VCO Frequency vs Timing Resistor.

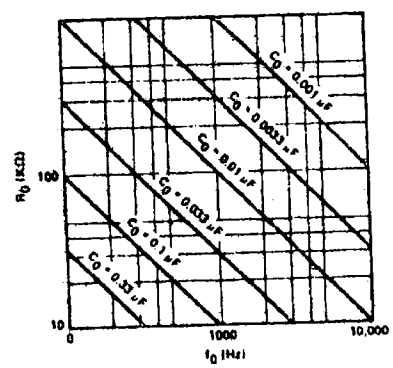


Figure 5: VCO Frequency vs Timing Capacitor.

TONE DETECTION:

Figure 7 shows the generalized circuit connection for tone detection. The logic outputs, Q and $\overline{Q}$ at Pins 5 and 6 are normally at "high" and "low" logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these outputs becomes reversed for the duration of the input tone. Each logic output can sink 5 mA of load current.

Both logic outputs at Pins 5 and 6 are open collector type stages, and require external pull-up resistors R_{L1} and R_{L2}, as shown in Figure 7.

With reference to Figures 2 and 7, the functions of the external circuit components can be explained as follows: R_0 and C_0 set VCO center frequency; R_1 sets the detection bandwidth; C_1 sets the low pass-loop filter time constant and the loop damping factor. R_{L1} and R_{L2} are the respective pull-up resistors for the Q and $\overline{Q}$ logic outputs.

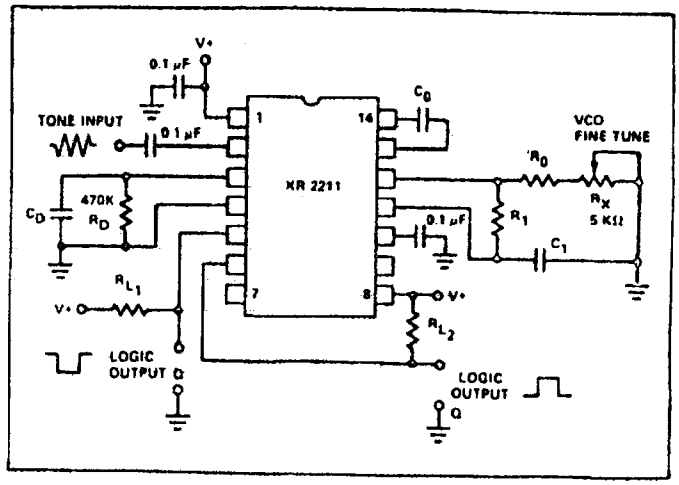


Figure 7: Circuit Connection for Tone Detection.

Typical values for detection band of 1 kHz ±20 Hz:

R_0 = 18K

C_0 = 0.05 µF

R_1 = 1 meg

C_1 = 0.013 µF

C_D = 0.42 µF

Fine-tune center frequency with R_X

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