

GENERAL DESCRIPTION

The XRT75R06 is a six channel fully integrated Line Interface Unit (LIU) featuring EXAR's R³ Technology (Reconfigurable, Relayless, Redundancy) for E3/DS3/STS-1 applications. The LIU incorporates 6 independent Receivers, Transmitters and Jitter Attenuators in a single 217 Lead BGA package.

Each channel of the XRT75R06 can be independently configured to operate in E3 (34.368 MHz), DS3 (44.736 MHz) or STS-1 (51.84 MHz). Each transmitter can be turned off and tri-stated for redundancy support or for conserving power.

The XRT75R06's differential receiver provides high noise interference margin and is able to receive data over 1000 feet of cable or with up to 12 dB of cable attenuation.

The XRT75R06 incorporates an advanced crystal-less jitter attenuator per channel that can be selected either in the transmit or receive path. The jitter

attenuator performance meets the ETSI TBR-24 and Bellcore GR-499 specifications.

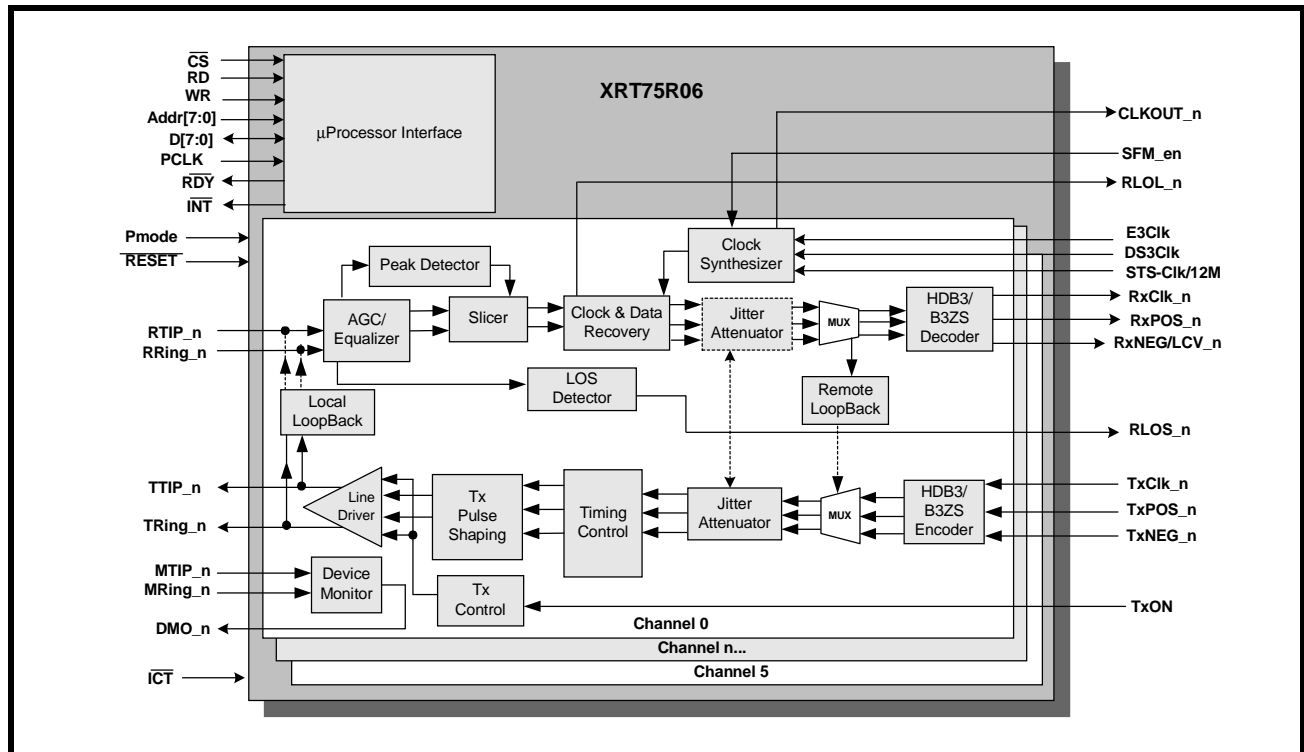
The XRT75R06 provides a Parallel Microprocessor Interface for programming and control.

The XRT75R06 supports analog, remote and digital loop-backs. The device also has a built-in Pseudo Random Binary Sequence (PRBS) generator and detector with the ability to insert and detect single bit error for diagnostic purposes.

APPLICATIONS

- E3/DS3 Access Equipment
- DSLAMs
- Digital Cross Connect Systems
- CSU/DSU Equipment
- Routers
- Fiber Optic Terminals

FIGURE 1. BLOCK DIAGRAM OF THE XRT 75R06



ORDERING INFORMATION

| PART NUMBER | PACKAGE | OPERATING TEMPERATURE RANGE |
|-------------|--------------|-----------------------------|
| XRT75R06IB | 217 Lead BGA | -40°C to +85°C |

FEATURES**RECEIVER**

- R³ Technology (Reconfigurable, Relayless, Redundancy)
- On chip Clock and Data Recovery circuit for high input jitter tolerance
- Meets E3/DS3/STS-1 Jitter Tolerance Requirement
- Detects and Clears LOS as per G.775
- Receiver Monitor mode handles up to 20 dB flat loss with 6 dB cable attenuation
- On chip B3ZS/HDB3 encoder and decoder that can be either enabled or disabled
- On-chip clock synthesizer provides the appropriate rate clock from a single 12.288 MHz Clock
- Provides low jitter output clock

TRANSMITTER

- R³ Technology (Reconfigurable, Relayless, Redundancy)
- Compliant with Bellcore GR-499, GR-253 and ANSI T1.102 Specification for transmit pulse
- Tri-state Transmit output capability for redundancy applications
- Each Transmitter can be independently turned on or off
- Transmitters provide Voltage Output Drive

JITTER ATTENUATOR

- On chip advanced crystal-less Jitter Attenuator for each channel
- Jitter Attenuator can be selected in Receive, Transmit path, or disabled
- Meets ETSI TBR 24 Jitter Transfer Requirements
- Compliant with jitter transfer template outlined in ITU G.751, G.752, G.755 and GR-499-CORE,1995 standards
- 16 or 32 bits selectable FIFO size

CONTROL AND DIAGNOSTICS

- Parallel Microprocessor Interface for control and configuration
- Supports optional internal Transmit driver monitoring

- Each channel supports Analog, Remote and Digital Loop-backs
- Single 3.3 V \pm 5% power supply
- 5 V Tolerant digital inputs
- Available in 217 pin BGA Package
- - 40°C to 85°C Industrial Temperature Range

TRANSMIT INTERFACE CHARACTERISTICS

- Accepts either Single-Rail or Dual-Rail data from Terminal Equipment and generates a bipolar signal to the line
- Integrated Pulse Shaping Circuit
- Built-in B3ZS/HDB3 Encoder (which can be disabled)
- Accepts Transmit Clock with duty cycle of 30%-70%
- Generates pulses that comply with the ITU-T G.703 pulse template for E3 applications
- Generates pulses that comply with the DSX-3 pulse template, as specified in Bellcore GR-499-CORE and ANSI T1.102_1993
- Generates pulses that comply with the STSX-1 pulse template, as specified in Bellcore GR-253-CORE
- Transmitter can be turned off in order to support redundancy designs

RECEIVE INTERFACE CHARACTERISTICS

- Integrated Adaptive Receive Equalization (optional) for optimal Clock and Data Recovery
 - Declares and Clears the LOS defect per ITU-T G.775 requirements for E3 and DS3 applications
 - Meets Jitter Tolerance Requirements, as specified in ITU-T G.823_1993 for E3 Applications
 - Meets Jitter Tolerance Requirements, as specified in Bellcore GR-499-CORE for DS3 Applications
 - Declares Loss of Lock (LOL) Alarm
 - Built-in B3ZS/HDB3 Decoder (which can be disabled)
 - Recovered Data can be muted while the LOS Condition is declared
 - Outputs either Single-Rail or Dual-Rail data to the Terminal Equipment
-

FIGURE 2. XRT75R06 IN BGA PACKAGE (BOTTOM VIEW)

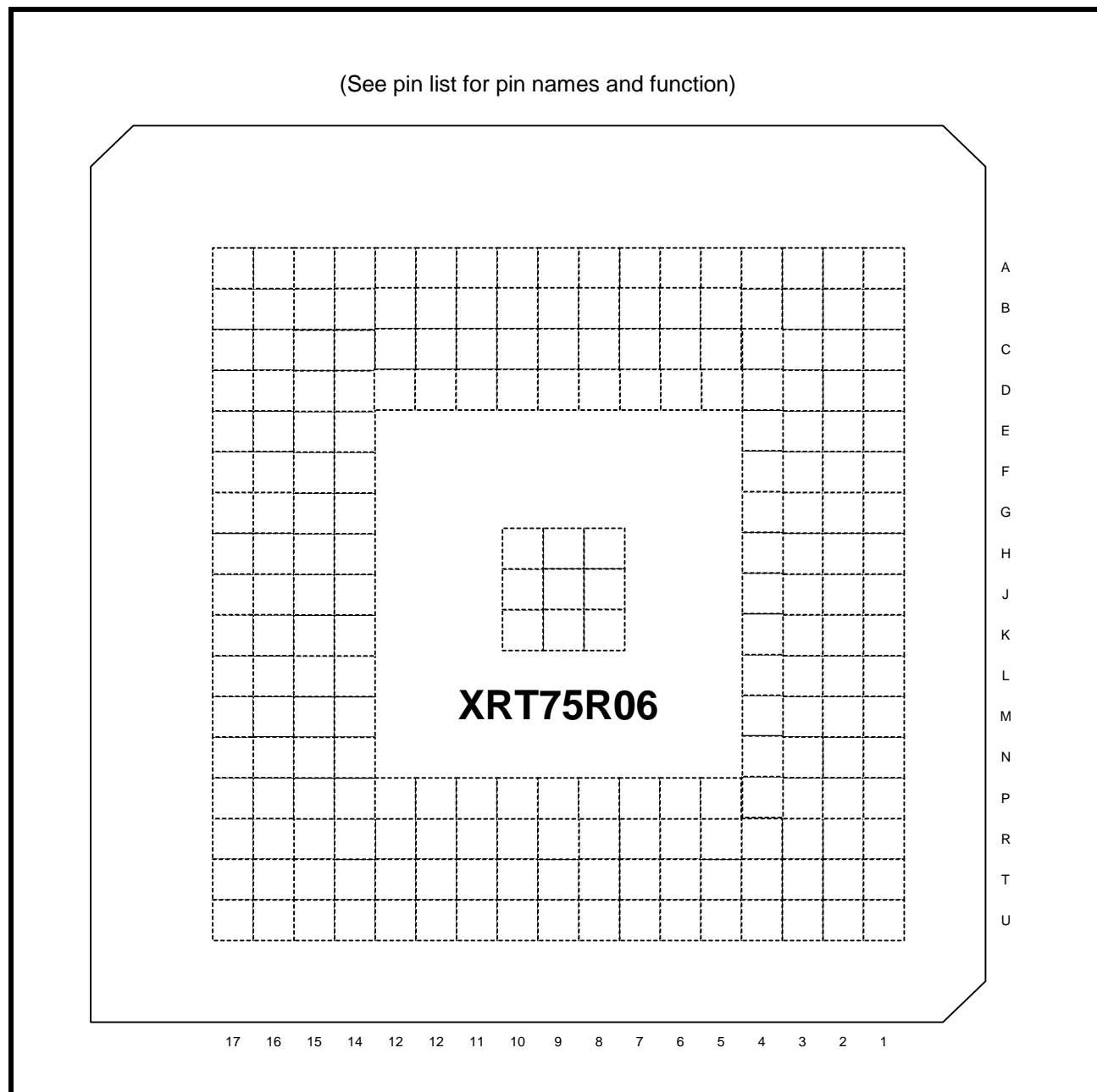


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PIN DESCRIPTIONS (BY FUNCTION)
TRANSMIT INTERFACE

| LEAD # | SIGNAL NAME | TYPE | DESCRIPTION | | | | | | | | | | | | | | | |
|--|--|--------------------|--|-----|-----|--------------------|---|---|-----|---|---|-----|---|---|-----|---|---|----|
| T15 R16 R15 N14 P14 P13 | TxON_0 TxON_1 TxON_2 TxON_3 TxON_4 TxON_5 | I | <p>Transmitter ON Input - Channel 0: Transmitter ON Input - Channel 1: Transmitter ON Input - Channel 2: Transmitter ON Input - Channel 3: Transmitter ON Input - Channel 4: Transmitter ON Input - Channel 5:</p> <p>These pins are active only when the corresponding TxON bits are set. Table below shows the status of the transmitter based on the TxON bit and TxON pin settings.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Bit</th> <th>Pin</th> <th>Transmitter Status</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>OFF</td> </tr> <tr> <td>0</td> <td>1</td> <td>OFF</td> </tr> <tr> <td>1</td> <td>0</td> <td>OFF</td> </tr> <tr> <td>1</td> <td>1</td> <td>ON</td> </tr> </tbody> </table> <p>NOTES:</p> <ol style="list-style-type: none"> 1. These pins will be active and can control the TTIP and TRING outputs only when the TxON_n bits in the channel register are set . 2. When Transmitters are turned off the TTIP and TRING outputs are Tri-stated. 3. These pins are internally pulled up. | Bit | Pin | Transmitter Status | 0 | 0 | OFF | 0 | 1 | OFF | 1 | 0 | OFF | 1 | 1 | ON |
| Bit | Pin | Transmitter Status | | | | | | | | | | | | | | | | |
| 0 | 0 | OFF | | | | | | | | | | | | | | | | |
| 0 | 1 | OFF | | | | | | | | | | | | | | | | |
| 1 | 0 | OFF | | | | | | | | | | | | | | | | |
| 1 | 1 | ON | | | | | | | | | | | | | | | | |
| E3 M3 F15 P16 G3 H15 | TxCLK_0 TxCLK_1 TxCLK_2 TxCLK_3 TxCLK_4 TxCLK_5 | I | <p>Transmit Clock Input for TPOS and TNEG - Channel 0: Transmit Clock Input for TPOS and TNEG - Channel 1: Transmit Clock Input for TPOS and TNEG - Channel 2: Transmit Clock Input for TPOS and TNEG - Channel 3: Transmit Clock Input for TPOS and TNEG - Channel 4: Transmit Clock Input for TPOS and TNEG - Channel 5:</p> <p>The frequency accuracy of this input clock must be of nominal bit rate ± 20 ppm. The duty cycle can be 30%-70%. By default, input data is sampled on the falling edge of TxCLK.</p> | | | | | | | | | | | | | | | |

TRANSMIT INTERFACE

| LEAD # | SIGNAL NAME | TYPE | DESCRIPTION |
|-------------------------------------|--|------|--|
| F2 P2 G15 R17 H3 K15 | TNEG_0 TNEG_1 TNEG_2 TNEG_3 TNEG_4 TNEG_5 | I | <p>Transmit Negative Data Input - Channel 0: Transmit Negative Data Input - Channel 1: Transmit Negative Data Input - Channel 2: Transmit Negative Data Input - Channel 3: Transmit Negative Data Input - Channel 4: Transmit Negative Data Input - Channel 5:</p> <p>In Dual-rail mode, these pins are sampled on the falling or rising edge of TxCLK_n.</p> <p>NOTES:</p> <ol style="list-style-type: none"> These input pins are ignored and must be grounded if the Transmitter Section is configured to accept Single-Rail data from the Terminal Equipment. |
| F3 N3 F16 P15 G2 J15 | TPOS_0 TPOS_1 TPOS_2 TPOS_3 TPOS_4 TPOS_5 | I | <p>Transmit Positive Data Input - Channel 0: Transmit Positive Data Input - Channel 1: Transmit Positive Data Input - Channel 2: Transmit Positive Data Input - Channel 3: Transmit Positive Data Input - Channel 4: Transmit Positive Data Input - Channel 5:</p> <p>By default sampled on the falling edge of TxCLK.</p> |
| D1 N1 D17 N17 H1 H17 | TTIP_0 TTIP_1 TTIP_2 TTIP_3 TTIP_4 TTIP_5 | O | <p>Transmit TTIP Output - Channel 0: Transmit TTIP Output - Channel 1: Transmit TTIP Output - Channel 2: Transmit TTIP Output - Channel 3: Transmit TTIP Output - Channel 4: Transmit TTIP Output - Channel 5:</p> <p>These pins along with TRING transmit bipolar signals to the line using a 1:1 transformer.</p> |
| E1 M1 E17 M17 J1 J17 | TRING_0 TRING_1 TRING_2 TRING_3 TRING_4 TRING_5 | O | <p>Transmit Ring Output - Channel 0: Transmit Ring Output - Channel 1: Transmit Ring Output - Channel 2: Transmit Ring Output - Channel 3: Transmit Ring Output - Channel 4: Transmit Ring Output - Channel 5:</p> <p>These pins along with TTIP transmit bipolar signals to the line using a 1:1 transformer.</p> |

RECEIVE INTERFACE

| LEAD # | SIGNAL NAME | TYPE | DESCRIPTION |
|--------------------------------------|--|------|--|
| A2 U2 A17 U17 D8 P8 | RxCLK_0 RXCLK_1 RxCLK_2 RxCLK_3 RxCLK_4 RxCLK_5 | O | Receive Clock Output - Channel 0: Receive Clock Output - Channel 1: Receive Clock Output - Channel 2: Receive Clock Output - Channel 3: Receive Clock Output - Channel 4: Receive Clock Output - Channel 5: By default, RPOS and RNEG data sampled on the rising edge RxCLK.. Set the RxCLKINV bit to sample RPOS/RNEG data on the falling edge of RxCLK |
| A1 U1 A16 U16 D9 P9 | RPOS_0 RPOS_1 RPOS_2 RPOS_3 RPOS_4 RPOS_5 | O | Receive Positive Data Output - Channel 0: Receive Positive Data Output - Channel 1: Receive Positive Data Output - Channel 2: Receive Positive Data Output - Channel 3: Receive Positive Data Output - Channel 4: Receive Positive Data Output - Channel 5: <i>NOTE: If the B3ZS/HDB3 Decoder is enabled in Single-rail mode, then the zero suppression patterns in the incoming line signal (such as: "00V", "000V", "B0V", "B00V") are removed and replaced with '0'.</i> |
| B2 T2 B16 T16 D10 P10 | RNEG_0/ LCV_0 RNEG_1/ LCV_1 RNEG_2/ LCV_2 RNEG_3/ LCV_3 RNEG_4/ LCV_4 RNEG_5/ LCV_5 | O | Receive Negative Data Output/Line Code Violation Indicator - Channel 0: Receive Negative Data Output/Line Code Violation Indicator - Channel 1: Receive Negative Data Output/Line Code Violation Indicator - Channel 2: Receive Negative Data Output/Line Code Violation Indicator - Channel 3: Receive Negative Data Output/Line Code Violation Indicator - Channel 4: Receive Negative Data Output/Line Code Violation Indicator - Channel 5: In Dual Rail mode, a negative pulse is output through RNEG. Line Code Violation Indicator - Channel n: If configured in Single Rail mode then Line Code Violation will be output. |

RECEIVE INTERFACE

| LEAD # | SIGNAL NAME | TYPE | DESCRIPTION |
|--------------------------------------|--|------|--|
| A5 U5 A14 U14 A9 U9 | RRING_0 RRING_1 RRING_2 RRING_3 RRING_4 RRING_5 | I | Receive Input - Channel 0: Receive Input - Channel 1: Receive Input - Channel 2: Receive Input - Channel 3: Receive Input - Channel 4: Receive Input - Channel 5: These pins along with RTIP receive the bipolar line signal from the remote DS3/E3/STS-1 Terminal. |
| A6 U6 A13 U13 A10 U10 | RTIP_0 RTIP_1 RTIP_2 RTIP_3 RTIP_4 RTIP_5 | I | Receive Input - Channel 0: Receive Input - Channel 1: Receive Input - Channel 2: Receive Input - Channel 3: Receive Input - Channel 4: Receive Input - Channel 5: These pins along with RRING receive the bipolar line signal from the Remote DS3/E3/STS-1 Terminal. |

CLOCK INTERFACE

| LEAD # | SIGNAL NAME | TYPE | DESCRIPTION |
|--------------------------------------|--|------|--|
| E15 | E3CLK | I | <p>E3 Clock Input (34.368 MHz ± 20 ppm): If any of the channels is configured in E3 mode, a reference clock 34.368 MHz is applied on this pin.</p> <p><i>NOTE: In single frequency mode, this reference clock is not required.</i></p> |
| G16 | DS3CLK | I | <p>DS3 Clock Input (44.736 MHz ± 20 ppm): If any of the channels is configured in DS3 mode, a reference clock 44.736 MHz. is applied on this pin.</p> <p><i>NOTE: In single frequency mode, this reference clock is not required.</i></p> |
| C16 | STS-1CLK/ 12M | I | <p>STS-1 Clock Input (51.84 MHz ± 20 ppm): If any of the channels is configured in STS-1 mode, a reference clock 51.84 MHz is applied on this pin..</p> <p>In Single Frequency Mode, a reference clock of 12.288 MHz ± 20 ppm is connected to this pin and the internal clock synthesizer generates the appropriate clock frequencies based on the configuration of the channels in E3, DS3 or STS-1 modes.</p> |
| L15 | SFM_EN | I | <p>Single Frequency Mode Enable: Tie this pin "High" to enable the Single Frequency Mode. A reference clock of 12.288 MHz ± 20 ppm is applied.</p> <p>In the Single Frequency Mode (SFM) a low jitter output clock is provided for each channel if the CLK_EN bit is set thus eliminating the need for a separate clock source for the framer.</p> <p>Tie this pin "Low" if single frequency mode is not selected. In this case, the appropriate reference clocks must be provided.</p> <p><i>NOTE: This pin is internally pulled down</i></p> |
| B1 T1 B17 T17 D11 P11 | CLKOUT_0 CLKOUT_1 CLKOUT_2 CLKOUT_3 CLKOUT_4 CLKOUT_5 | O | <p>Clock output for channel 0 Clock output for channel 1 Clock output for channel 2 Clock output for channel 3 Clock output for channel 4 Clock output for channel 5</p> <p>Low jitter clock output for each channel based on the mode selection (E3,DS3 or STS-1) if the CLKOUTEN_n bit is set in the control register.</p> <p>This eliminates the need for a separate clock source for the framer.</p> <p>NOTES:</p> <ol style="list-style-type: none"> The maximum drive capability for the clockouts is 16 mA. This clock out is available both in SFM and non-SFM modes. |

CONTROL AND ALARM INTERFACE

| LEAD # | SIGNAL NAME | TYPE | DESCRIPTION |
|-------------------------------------|--|------|---|
| B7 R6 C14 R14 C6 D14 | MRING_0 MRING_1 MRING_2 MRING_3 MRING_4 MRING_5 | I | <p>Monitor Ring Input - Channel 0: Monitor Ring Input - Channel 1: Monitor Ring Input - Channel 2: Monitor Ring Input - Channel 3: Monitor Ring Input - Channel 4: Monitor Ring Input - Channel 5:</p> <p>The bipolar line output signal from TRING_n is connected to this pin via a 270 Ω resistor to check for line driver failure.</p> <p><i>NOTE: This pin is internally pulled up.</i></p> |
| B8 R7 C13 R13 C7 D13 | MTIP_0 MTIP_1 MTIP_2 MTIP_3 MTIP_4 MTIP_5 | I | <p>Monitor Tip Input - Channel 0: Monitor Tip Input - Channel 1: Monitor Tip Input - Channel 2: Monitor Tip Input - Channel 3: Monitor Tip Input - Channel 4: Monitor Tip Input - Channel 5:</p> <p>The bipolar line output signal from TTIP_n is connected to this pin via a 270-ohm resistor to check for line driver failure.</p> <p><i>NOTE: This pin is internally pulled up.</i></p> |
| C5 T4 B12 T12 D5 B15 | DMO_0 DMO_1 DMO_2 DMO_3 DMO_4 DMO_5 | O | <p>Drive Monitor Output - Channel 0: Drive Monitor Output - Channel 1: Drive Monitor Output - Channel 2: Drive Monitor Output - Channel 3: Drive Monitor Output - Channel 4: Drive Monitor Output - Channel 5:</p> <p>If MTIP_n and MRING_n has no transition pulse for 128 ± 32 TxCLK_n cycles, DMO_n goes "High" to indicate the driver failure. DMO_n output stays "High" until the next AMI signal is detected.</p> |
| C8 T7 C12 T11 B11 R8 | RLOS_0 RLOS_1 RLOS_2 RLOS_3 RLOS_4 RLOS_5 | O | <p>Receive Loss of Signal - Channel 0: Receive Loss of Signal - Channel 1: Receive Loss of Signal - Channel 2: Receive Loss of Signal - Channel 3: Receive Loss of Signal - Channel 4: Receive Loss of Signal - Channel 5:</p> <p>This output pin toggles "High" if the receiver has detected a Loss of Signal Condition.</p> |

CONTROL AND ALARM INTERFACE

| | | | |
|-------------------------------------|--|------|--|
| C9 T8 D12 R11 C11 R9 | RLOL_0 RLOL_1 RLOL_2 RLOL_3 RLOL_4 RLOL_5 | O | Receive Loss of Lock - Channel 0: Receive Loss of Lock - Channel 1: Receive Loss of Lock - Channel 2: Receive Loss of Lock - Channel 3: Receive Loss of Lock - Channel 4: Receive Loss of Lock - Channel 5: This output pin toggles "High" if a Loss of Lock Condition is detected. LOL (Loss of Lock) condition occurs if the recovered clock frequency deviates from the Reference Clock frequency (available at either E3CLK or DS3CLK or STS-1CLK input pins) by more than 0.5%. |
| L16 | RXA | **** | External Resistor of 3.01K $\Omega \pm 1\%$. Should be connected between RxA and RxB for internal bias. |
| K16 | RXB | **** | External Resistor of 3.01K $\Omega \pm 1\%$. Should be connected between RxA and RxB for internal bias. |
| P12 | ICT | I | In-Circuit Test Input: Setting this pin "Low" causes all digital and analog outputs to go into a high-impedance state to allow for in-circuit testing. For normal operation, tie this pin "High". <i>NOTE: This pin is internally pulled up.</i> |
| R12 | TEST | **** | Factory Test Pin <i>NOTE: This pin must be connected to GND for normal operation.</i> |

MICROPROCESSOR INTERFACE

| LEAD # | SIGNAL NAME | TYPE | DESCRIPTION |
|--------|--------------------|------|--|
| K3 | \overline{CS} | I | Chip Select Tie this "Low" to enable the communication with the Microprocessor Interface. |
| R1 | PCLK | I | Processor Clock Input To operate the Microprocessor Interface, appropriate clock frequency is provided through this pin. Maximum frequency is 66 Mhz. |
| K2 | \overline{WR} | I | Write Data : To write data into the registers, this active low signal is asserted. |
| L2 | \overline{RD} | I | Read Data: To read data from the registers, this active low pin is asserted. |
| J3 | \overline{RESET} | I | Register Reset: Setting this input pin "Low" resets the contents of the Command Registers to their default settings and default operating configuration <i>NOTE: This pin is internally pulled up.</i> |
| L3 | PMODE | I | Processor Mode Select: When this pin is tied "High", the microprocessor is operating in synchronous mode which means that clock must be applied to the PCLK (pin 55). Tie this pin "Low" to select the Asynchronous mode. An internal clock is provided for the microprocessor interface. |

MICROPROCESSOR INTERFACE

| LEAD # | SIGNAL NAME | TYPE | DESCRIPTION |
|--|--|------|--|
| T3 | RDY | O | Ready Acknowledge: <i>NOTE: This pin must be connected to VDD via 3 kΩ ± 1% resistor.</i> |
| U3 | INT | O | INTERRUPT Output: A transition to "Low" indicates that an interrupt has been generated. The interrupt function can be disabled by clearing the interrupt enable bit in the Channel Control Register. NOTES: 1. This pin will remain asserted "Low" until the interrupt is serviced. 2. This pin must be connected to VDD via 3 kΩ ± 1% resistor. |
| B4 A3 B3 C4 C3 C2 D3 D4 | ADDR[0] ADDR[1] ADDR[2] ADDR[3] ADDR[4] ADDR[5] ADDR[6] ADDR[7] | I | ADDRESS BUS: 8 bit address bus for the microprocessor interface |
| N4 P3 P4 P5 R5 R4 R3 R2 | D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7] | I/O | DATA BUS: 8 bit Data Bus for the microprocessor interface |

ANALOG POWER AND GROUND

| LEAD # | SIGNAL NAME | TYPE | DESCRIPTION |
|--------|-------------|------|---|
| E2 | TxAVDD_0 | **** | Transmitter Analog 3.3 V \pm 5% VDD - Channel 0 |
| N2 | TxAVDD_1 | **** | Transmitter Analog 3.3 V \pm 5% VDD - Channel 1 |
| E16 | TxAVDD_2 | **** | Transmitter Analog 3.3 V \pm 5% VDD - Channel 2 |
| N16 | TxAVDD_3 | **** | Transmitter Analog 3.3 V \pm 5% VDD - Channel 3 |
| J2 | TxAVDD_4 | **** | Transmitter Analog 3.3 V \pm 5% VDD - Channel 4 |
| J16 | TxAVDD_5 | **** | Transmitter Analog 3.3 V \pm 5% VDD - Channel 5 |
| D2 | TxAGND_0 | **** | Transmitter Analog GND - Channel 0 |
| M2 | TxAGND_1 | **** | Transmitter Analog GND - Channel 1 |
| D16 | TxAGND_2 | **** | Transmitter Analog GND - Channel 2 |
| M16 | TxAGND_3 | **** | Transmitter Analog GND - Channel 3 |
| H2 | TxAGND_4 | **** | Transmitter Analog GND - Channel 4 |
| H16 | TxAGND_5 | **** | Transmitter Analog GND - Channel 5 |
| A4 | RxAVDD_0 | **** | Receiver Analog 3.3 V \pm 5% VDD - Channel 0 |
| U4 | RxAVDD_1 | **** | Receiver Analog 3.3 V \pm 5% VDD - Channel 1 |
| A15 | RxAVDD_2 | **** | Receiver Analog 3.3 V \pm 5% VDD - Channel 2 |
| U15 | RxAVDD_3 | **** | Receiver Analog 3.3 V \pm 5% VDD - Channel 3 |
| A8 | RxAVDD_4 | **** | Receiver Analog 3.3 V \pm 5% VDD - Channel 4 |
| U8 | RxAVDD_5 | **** | Receiver Analog 3.3 V \pm 5% VDD - Channel 5 |
| A7 | RxAGND_0 | **** | Receiver Analog GND - Channel_0 |
| U7 | RxAGND_1 | **** | Receive Analog GND - Channel 1 |
| A12 | RxAGND_2 | **** | Receive Analog GND - Channel 2 |
| U12 | RxAGND_3 | **** | Receive Analog GND - Channel 3 |
| A11 | RxAGND_4 | **** | Receive Analog GND - Channel 4 |
| U11 | RxAGND_5 | **** | Receive Analog GND - Channel 5 |
| E4 | JaAVDD_0 | **** | Analog 3.3 V \pm 5% VDD - Jitter Attenuator Channel 0 |
| K4 | JaAVDD_1 | **** | Analog 3.3 V \pm 5% VDD - Jitter Attenuator Channel 1 |
| E14 | JaAVDD_2 | **** | Analog 3.3 V \pm 5% VDD - Jitter Attenuator Channel 2 |
| K14 | JaAVDD_3 | **** | Analog 3.3 V \pm 5% VDD - Jitter Attenuator Channel 3 |
| G4 | JaAVDD_4 | **** | Analog 3.3 V \pm 5% VDD - Jitter Attenuator Channel 4 |
| G14 | JaAVDD_5 | **** | Analog 3.3 V \pm 5% VDD - Jitter attenuator Channel 5 |
| F4 | JaAGND_0 | **** | Analog GND - Jitter Attenuator Channel 0 |

ANALOG POWER AND GROUND

| LEAD # | SIGNAL NAME | TYPE | DESCRIPTION |
|--------|-------------|------|--|
| J4 | JaAGND_1 | **** | Analog GND - Jitter Attenuator Channel 1 |
| F14 | JaAGND_2 | **** | Analog GND - Jitter Attenuator Channel 2 |
| J14 | JaAGND_3 | **** | Analog GND - Jitter Attenuator Channel 3 |
| H4 | JaAGND_4 | **** | Analog GND - Jitter Attenuator Channel 4 |
| H14 | JaAGND_5 | **** | Analog GND - Jitter Attenuator Channel 5 |
| C10 | AGND | **** | Analog GND |
| R10 | AGND | **** | Analog GND |
| H9 | AGND | **** | Analog GND |
| J9 | AGND | **** | Analog GND |
| K9 | AGND | **** | Analog GND |
| N15 | REFAVDD | **** | Analog 3.3 V \pm 5% VDD - Reference |
| M15 | REFGND | **** | Reference GND |

DIGITAL POWER AND GROUND

| LEAD # | SIGNAL NAME | TYPE | DESCRIPTION |
|--------|-------------|------|--|
| F1 | TxVDD_0 | **** | Transmitter 3.3 V \pm 5% VDD Channel 0 |
| L1 | TxVDD_1 | **** | Transmitter 3.3 V \pm 5% VDD Channel 1 |
| F17 | TxVDD_2 | **** | Transmitter 3.3 V \pm 5% VDD Channel 2 |
| L17 | TxVDD_3 | **** | Transmitter 3.3 V \pm 5% VDD Channel 3 |
| K1 | TxVDD_4 | **** | Transmitter 3.3 V \pm 5% VDD Channel 4 |
| K17 | TxVDD_5 | **** | Transmitter 3.3 V \pm 5% VDD Channel 5 |
| C1 | TxGND_0 | **** | Transmitter GND - Channel 0 |
| P1 | TxGND_1 | **** | Transmitter GND - Channel 1 |
| C17 | TxGND_2 | **** | Transmitter GND - Channel 2 |
| P17 | TxGND_3 | **** | Transmitter GND - Channel 3 |
| G1 | TxGND_4 | **** | Transmitter GND - Channel 4 |
| G17 | TxGND_5 | **** | Transmitter GND - Channel 5 |
| B5 | RxDVDD_0 | **** | Receiver 3.3 V \pm 5% VDD - Channel 0 |
| T5 | RxDVDD_1 | **** | Receiver 3.3 V \pm 5% VDD - Channel 1 |
| B14 | RxDVDD_2 | **** | Receiver 3.3 V \pm 5% VDD - Channel 2 |
| T14 | RxDVDD_3 | **** | Receiver 3.3 V \pm 5% VDD - Channel 3 |
| B9 | RxDVDD_4 | **** | Receiver 3.3 V \pm 5% VDD - Channel 4 |
| T9 | RxDVDD_5 | **** | Receiver 3.3 V \pm 5% VDD - Channel 5 |
| B6 | RxDGND_0 | **** | Receiver Digital GND - Channel 0 |
| T6 | RxDGND_1 | **** | Receiver Digital GND - Channel 1 |
| B13 | RxDGND_2 | **** | Receiver Digital GND - Channel 2 |
| T13 | RxDGND_3 | **** | Receiver Digital GND - Channel 3 |
| B10 | RxDGND_4 | **** | Receiver Digital GND - Channel 4 |
| T10 | RxDGND_5 | **** | Receiver Digital GND - Channel 5 |
| P6 | DVDD_1 | **** | VDD 3.3 V \pm 5% |
| C15 | DVDD_2 | **** | VDD 3.3 V \pm 5% |
| L4 | JaDVDD_1 | **** | VDD 3.3 V \pm 5% |
| D6 | DVDD(uP) | **** | VDD 3.3 V \pm 5% |
| L14 | JaDVDD_2 | **** | VDD 3.3 V \pm 5% |
| D15 | DGND_1 | **** | Digital GND |
| D7 | DGND(uP) | **** | Digital GND |

DIGITAL POWER AND GROUND

| LEAD # | SIGNAL NAME | TYPE | DESCRIPTION |
|--------|-------------|------|-------------|
| M14 | JaDGND_2 | **** | Digital GND |
| M4 | JaDGND_1 | **** | Digital GND |
| P7 | DGND | **** | Digital GND |
| H8 | DGND | **** | Digital GND |
| J8 | DGND | **** | Digital GND |
| K8 | DGND | **** | Digital GND |
| H10 | DGND | **** | Digital GND |
| J10 | DGND | **** | Digital GND |
| K10 | DGND | **** | Digital GND |

FUNCTIONAL DESCRIPTION

The XRT75R06 is a six channel fully integrated Line Interface Unit featuring EXAR’s R³ Technology (Reconfigurable, Relayless Redundancy) for E3/DS3/STS-1 applications. The LIU incorporates 6 independent Receivers, Transmitters and Jitter Attenuators in a single 217 Lead BGA package. Each channel can be independently programmed to support E3, DS-3 or STS-1 line rates using one input clock reference of 12.288MHz in Single Frequency Mode (SFM). The LIU is responsible for providing the physical connection between a line interface and an aggregate mapper or framing device. Along with the analog-to-digital processing, the LIU offers monitoring and diagnostic features to help optimize network design implementation. A key characteristic within the network topology is Automatic Protection Switching (APS).

EXAR’s proven expertise in providing redundant solutions has paved the way for R³ Technology.

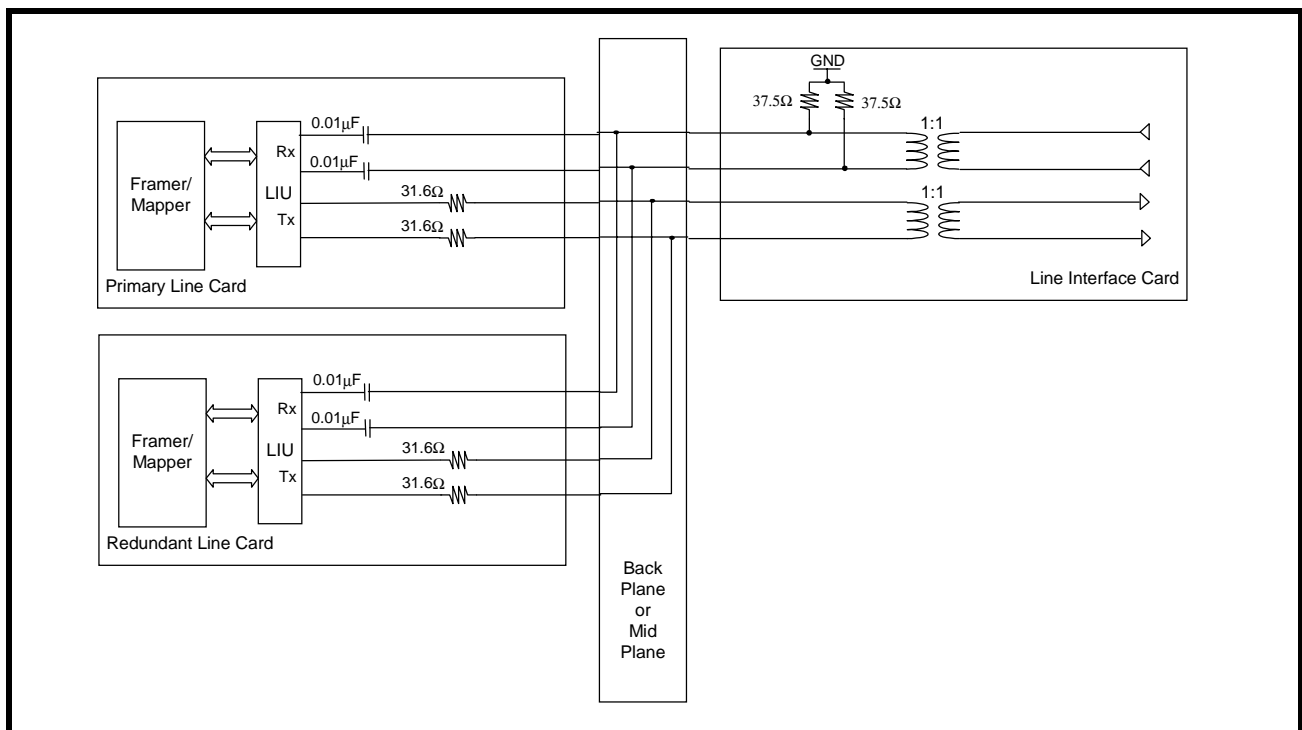
1.0 R³ TECHNOLOGY (RECONFIGURABLE, RELAYLESS REDUNDANCY)

Redundancy is used to introduce reliability and protection into network card design. The redundant card in many cases is an exact replicate of the primary card, such that when a failure occurs the network processor can automatically switch to the backup card. EXAR’s R³ technology has re-defined E3/DS-3/STS-1 LIU design for 1:1 and 1+1 redundancy applications. Without relays and one Bill of Materials, EXAR offers multi-port, integrated LIU solutions to assist high density aggregate applications and framing requirements with reliability. The following section can be used as a reference for implementing R³ Technology with EXAR’s world leading line interface units.

1.1 Network Architecture

A common network design that supports 1:1 or 1+1 redundancy consists of N primary cards along with N backup cards that connect into a mid-plane or back-plane architecture without transformers installed on the network cards. In addition to the network cards, the design has a line interface card with one source of transformers, connectors, and protection components that are common to both network cards. With this design, the bill of materials is reduced to the fewest amount of components. See Figure 3. for a simplified block diagram of a typical redundancy design.

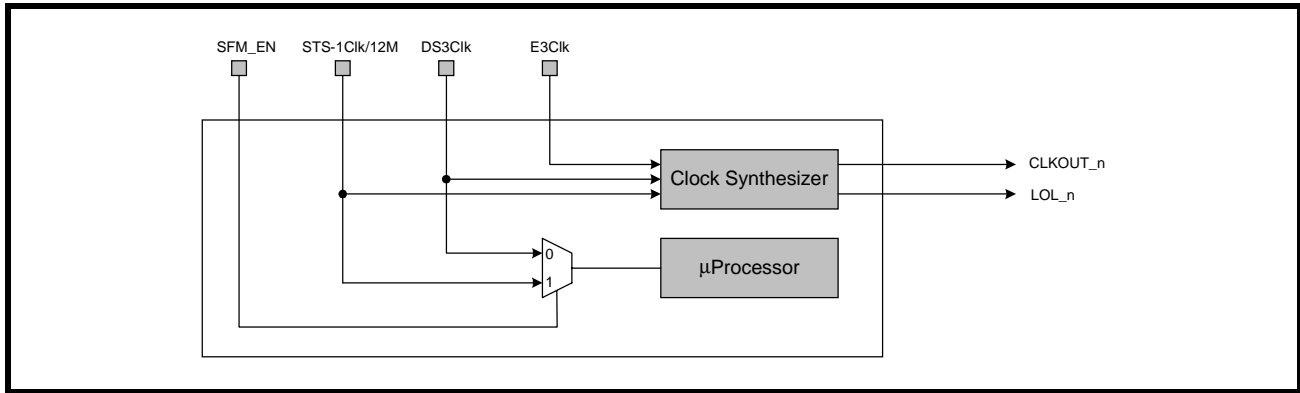
FIGURE 3. NETWORK REDUNDANCY ARCHITECTURE



2.0 CLOCK SYNTHESIZER

The LIU uses a flexible user interface for accepting clock references to generate the internal master clocks used to drive the LIU. The reference clock used to supply the microprocessor timing is generated from the DS-3 or SFM clock input. Therefore, if the chip is configured for STS-1 only or E3 only, then the DS-3 input pin must be connected to the STS-1 pin or E3 pin respectively. In DS-3 mode or when SFM is used, the STS-1 and E3 input pins can be left unconnected. If SFM is enabled by pulling the SFM_EN pin "High", 12.288MHz is the only clock reference necessary to generate DS-3, E3, or STS-1 line rates and the microprocessor timing. A simplified block diagram of the clock synthesizer is shown in Figure 4

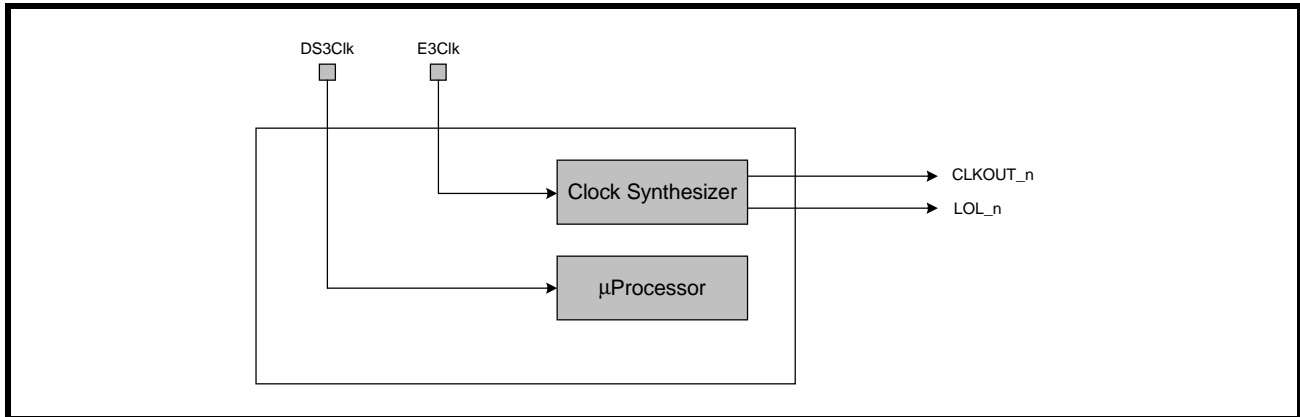
FIGURE 4. SIMPLIFIED BLOCK DIAGRAM OF THE INPUT CLOCK CIRCUITRY DRIVING THE MICROPROCESSOR



2.1 Clock Distribution

Network cards that are designed to support multiple line rates which are not configured for single frequency mode should ensure that a clock is applied to the DS3Clk input pin. For example: If the network card being supplied to an ISP requires E3 only, the DS-3 input clock reference is still necessary to provide read and write access to the internal microprocessor. Therefore, the E3 mode requires two input clock references. If however, multiple line rates will not be supported, i.e. E3 only, then the DS3Clk input pin may be hard wire connected to the E3Clk input pin.

FIGURE 5. CLOCK DISTRIBUTION CONFIGURED IN E3 MODE WITHOUT USING SFM

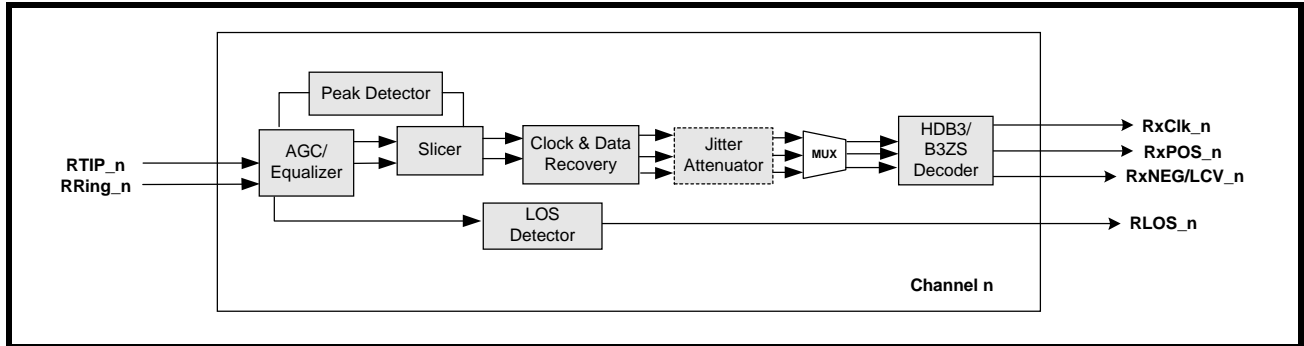


NOTE: For one input clock reference, the single frequency mode should be used.

3.0 THE RECEIVER SECTION

The receiver is designed so that the LIU can recover clock and data from an attenuated line signal caused by cable loss or flat loss according to industry specifications. Once data is recovered, it is processed and presented at the receiver outputs according to the format chosen to interface with a Framer/Mapper or ASIC. This section describes the detailed operation of various blocks within the receive path. A simplified block diagram of the receive path is shown in Figure 6.

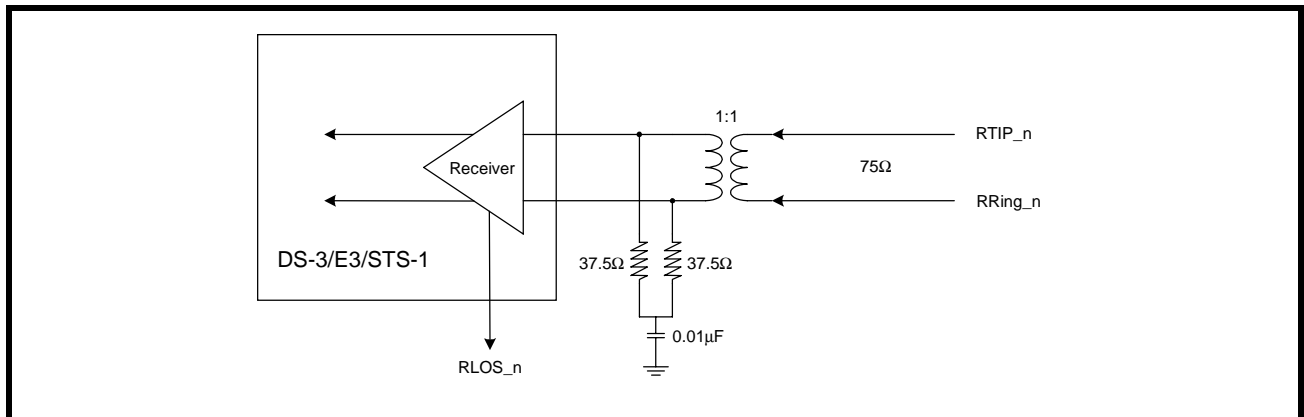
FIGURE 6. RECEIVE PATH BLOCK DIAGRAM



3.1 Receive Line Interface

Physical Layer devices are AC coupled to a line interface through a 1:1 transformer. The transformer provides isolation and a level shift by blocking the DC offset of the incoming data stream. The typical medium for the line interface is a 75Ω coaxial cable. Whether using E3, DS-3 or STS-1, the LIU requires the same bill of materials, see Figure 7.

FIGURE 7. RECEIVE LINE INTERFACE CONNECTION



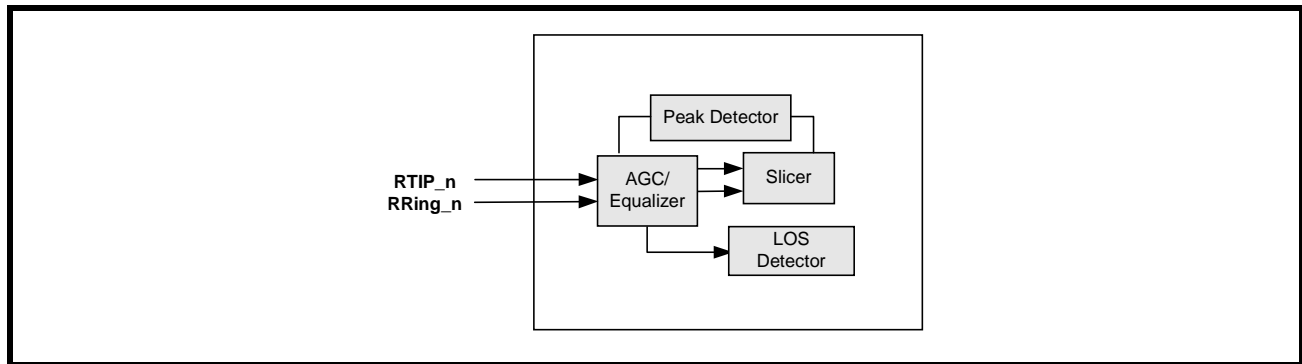
3.2 Adaptive Gain Control (AGC)

The Adaptive Gain Control circuit amplifies the incoming analog signal and compensates for the various flat losses and also for the loss at one-half symbol rate. The AGC has a dynamic range of 30 dB. The peak detector provides feedback to the equalizer before slicing occurs.

3.3 Receive Equalizer

The Equalizer restores the integrity of the signal and compensates for the frequency dependent attenuation of up to 900 feet of coaxial cable (1300 feet for E3). The Equalizer also boosts the high frequency content of the signal to reduce Inter-Symbol Interference (ISI) so that the slicer slices the signal at 50% of peak voltage to generate Positive and Negative data. The equalizer can be disabled by programming the appropriate register.

FIGURE 8. ACG/EQUALIZER BLOCK DIAGRAM



3.3.1 Recommendations for Equalizer Settings

The Equalizer has two gain settings to provide optimum equalization. In the case of normally shaped DS3/STS-1 pulses (pulses that meet the template requirements) that has been driven through 0 to 900 feet of cable, the Equalizer can be enabled. However, for square-shaped pulses such as E3 or for DS3/STS-1 high pulses (that does not meet the pulse template requirements), it is recommended that the Equalizer be disabled for cable length less than 300 feet. This would help to prevent over-equalization of the signal and thus optimize the performance in terms of better jitter transfer characteristics. The Equalizer also contains an additional 20 dB gain stage to provide the line monitoring capability of the resistively attenuated signals which may have 20dB flat loss. The equalizer gain mode can be enabled by programming the appropriate register.

NOTE: The results of extensive testing indicate that even when the Equalizer was enabled, regardless of the cable length, the integrity of the E3 signal was restored properly over 0 to 12 dB cable loss at Industrial Temperature.

3.4 Clock and Data Recovery

The Clock and Data Recovery Circuit extracts the embedded clock, RxClk_n from the sliced digital data stream and provides the retimed data to the B3ZS (HDB3) decoder. The Clock Recovery PLL can be in one of the following two modes:

3.4.1 Data/Clock Recovery Mode

In the presence of input line signals on the RTIP_n and RRing_n input pins and when the frequency difference between the recovered clock signal and the reference clock signal is less than 0.5%, the clock that is output on the RxClk_n out pins is the Recovered Clock signal.

3.4.2 Training Mode

In the absence of input signals at RTIP_n and RRing_n pins, or when the frequency difference between the recovered line clock signal and the reference clock applied on the ExClk_n input pins exceed 0.5%, a Loss of Lock condition is declared by toggling RLOL_n output pin “High” or setting the RLOL_n bit to “1” in the control register. Also, the clock output on the RxClk_n pins are the same as the reference channel clock.

3.5 LOS (Loss of Signal) Detector

3.5.1 DS3/STS-1 LOS Condition

A Digital Loss of Signal (DLOS) condition occurs when a string of 175 ± 75 consecutive zeros occur on the line. When the DLOS condition occurs, the DLOS_n bit is set to “1” in the status control register. DLOS condition is cleared when the detected average pulse density is greater than 33% for 175 ± 75 pulses. Analog Loss of Signal (ALOS) condition occurs when the amplitude of the incoming line signal is below the threshold as shown in the Table 1. The status of the ALOS condition is reflected in the ALOS_n status control register. RLOS is the logical OR of the DLOS and ALOS states. When the RLOS condition occurs the RLOS_n output pin is toggled “High” and the RLOS_n bit is set to “1” in the status control register.

TABLE 1: THE ALOS (ANALOG LOS) DECLARATION AND CLEARANCE THRESHOLDS FOR A GIVEN SETTING OF LOSTHR AND REQEN (DS3 AND STS-1 APPLICATIONS)

| APPLICATION | REQEN SETTING | LOSTHR SETTING | SIGNAL LEVEL TO DECLARE ALOS DEFECT | SIGNAL LEVEL TO CLEAR ALOS DEFECT |
|-------------|---------------|----------------|-------------------------------------|-----------------------------------|
| DS3 | 0 | 0 | < 75mVpk | > 130mVpk |
| | 1 | 0 | < 45mVpk | > 60mVpk |
| | 0 | 1 | < 120mVpk | > 45mVpk |
| | 1 | 1 | < 55mVpk | > 180mVpk |
| STS-1 | 0 | 0 | < 120mVpk | > 170mVpk |
| | 1 | 0 | < 50mVpk | > 75mVpk |
| | 0 | 1 | < 125mVpk | > 205mVpk |
| | 1 | 1 | < 55mVpk | > 90mVpk |

3.5.2 Disabling ALOS/DLOS Detection

For debugging purposes it is useful to disable the ALOS and/or DLOS detection. Writing a “1” to both ALOSDIS_n and DLOSDIS_n bits disables the LOS detection on a per channel basis.

3.5.3 E3 LOS Condition:

If the level of incoming line signal drops below the threshold as described in the ITU-T G.775 standard, the LOS condition is detected. Loss of signal is defined as no transitions for 10 to 255 consecutive zeros. No transitions is defined as a signal level between 15 and 35 dB below the normal. This is illustrated in Figure 9. The LOS condition is cleared within 10 to 255 UI after restoration of the incoming line signal. Figure 10 shows the LOS declaration and clearance conditions.

FIGURE 9. LOSS OF SIGNAL DEFINITION FOR E3 AS PER ITU-T G.775

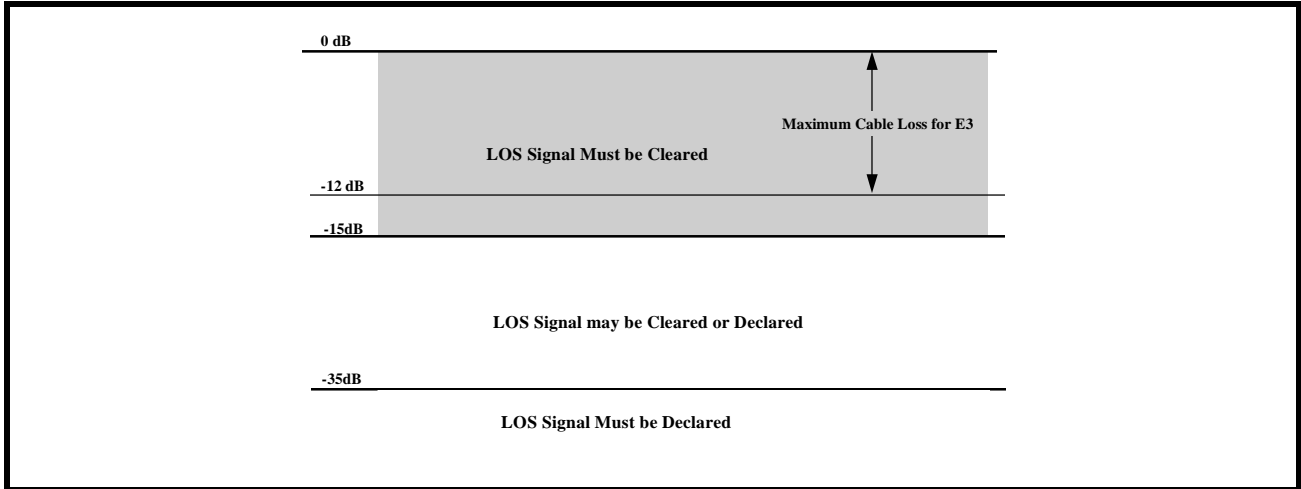
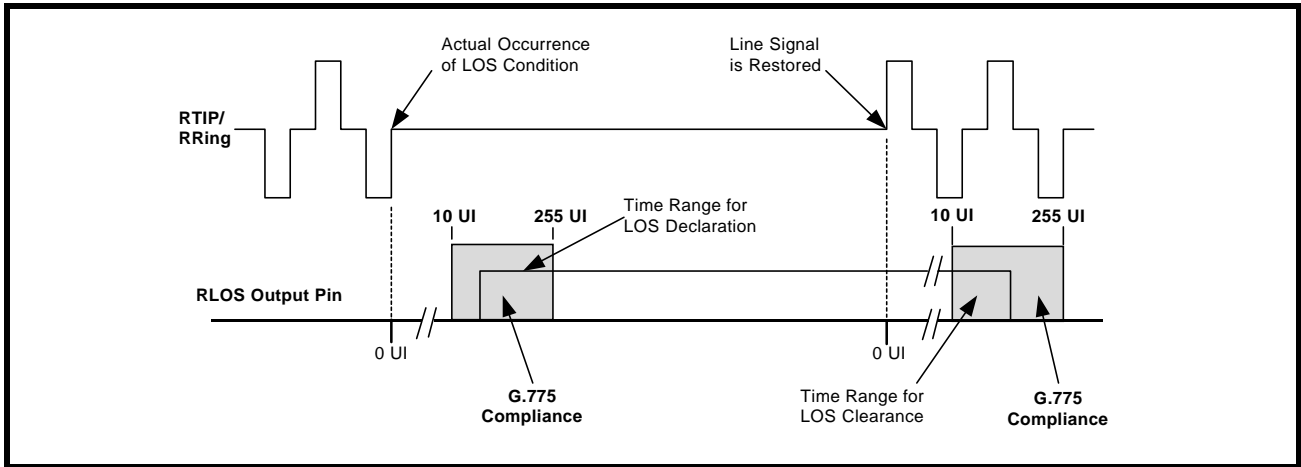


FIGURE 10. LOSS OF SIGNAL DEFINITION FOR E3 AS PER ITU-T G.775.



3.5.4 Interference Tolerance

For E3 mode, ITU-T G.703 Recommendation specifies that the receiver be able to recover error free clock and data in the presence of a sinusoidal interfering tone signal. For DS3 and STS-1 modes, the same recommendation is being used. Figure 11 shows the configuration to test the interference margin for DS3/STS1. Figure 12 shows the set up for E3.

FIGURE 11. INTERFERENCE MARGIN TEST SET UP FOR DS3/STS-1

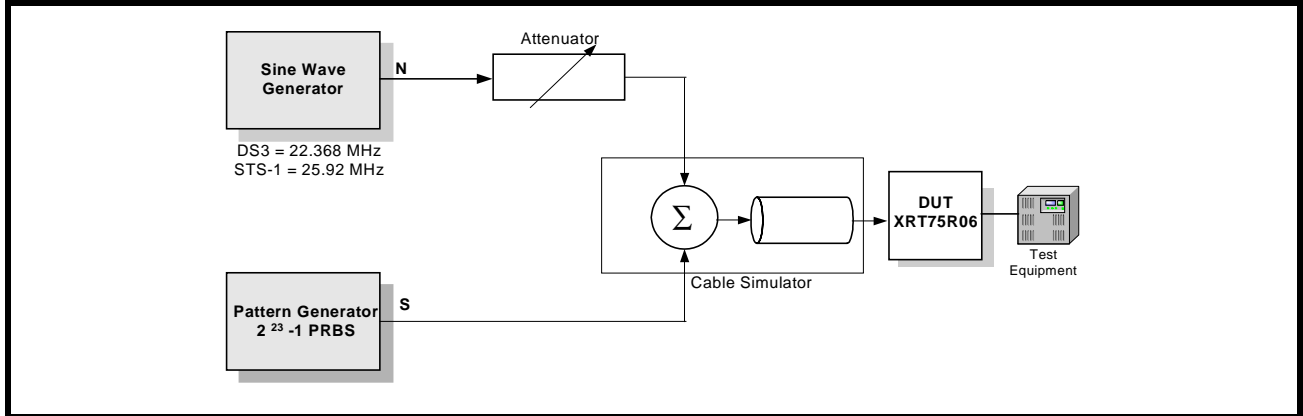


FIGURE 12. INTERFERENCE MARGIN TEST SET UP FOR E3.

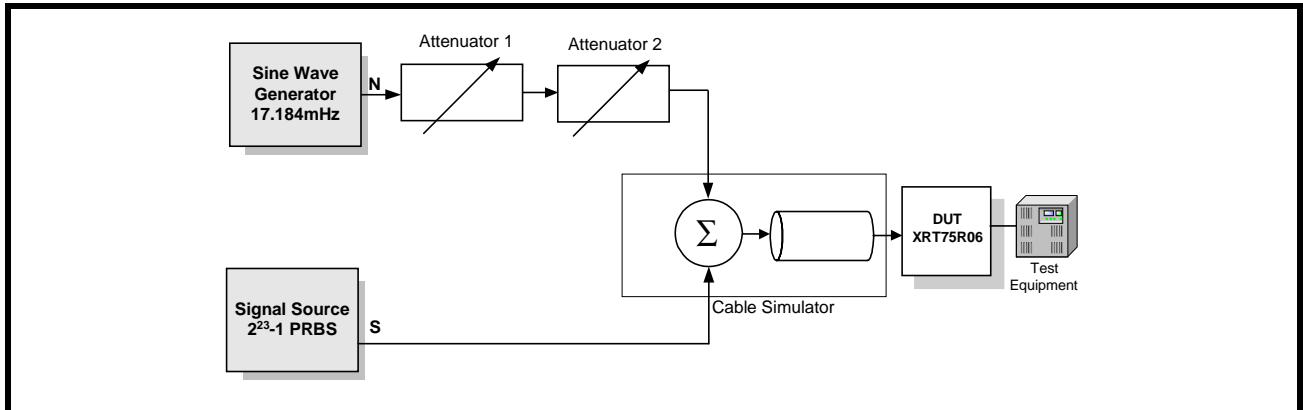


TABLE 2: INTERFERENCE MARGIN TEST RESULTS

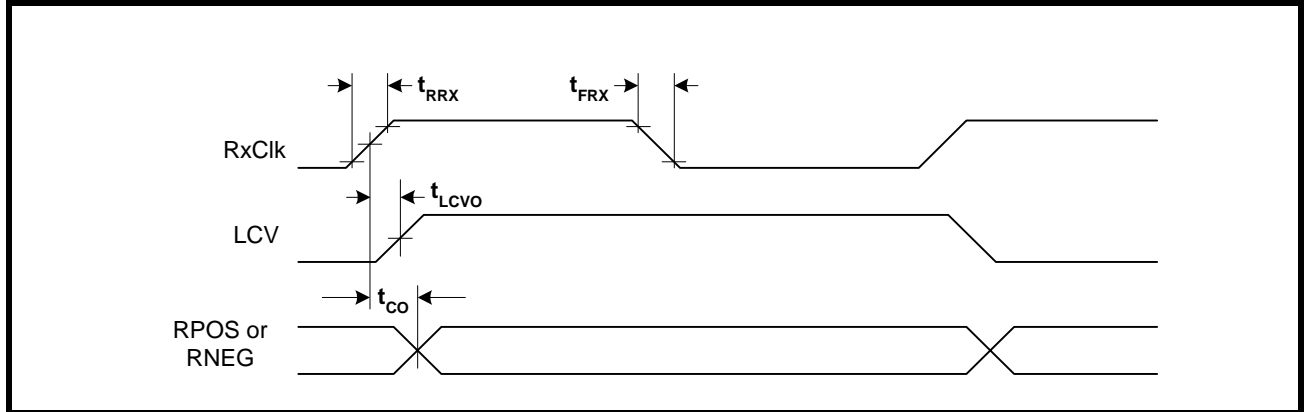
| MODE | CABLE LENGTH (ATTENUATION) | INTERFERENCE TOLERANCE |
|-------|----------------------------|------------------------|
| E3 | 0 dB | Equalizer "IN" |
| | | -17 dB |
| | | -14 dB |
| DS3 | 0 feet | -15 dB |
| | 225 feet | -15 dB |
| | 450 feet | -14 dB |
| STS-1 | 0 feet | -15 dB |
| | 225 feet | -14 dB |
| | 450 feet | -14 dB |

3.5.5 Muting the Recovered Data with LOS condition:

When the LOS condition is declared, the clock recovery circuit locks into the reference clock applied to the internal master clock outputs this clock onto the RxClk_n output pin. The data on the RxPOS_n and RxNEG_n pins can be forced to zero by setting the LOSMUT_n bits in the individual channel control register to “1”.

NOTE: When the LOS condition is cleared, the recovered data is output on RxPOS_n and RxNEG_n pins.

FIGURE 13. RECEIVER DATA OUTPUT AND CODE VIOLATION TIMING



| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS |
|-------------------|--|-----|--------|-----|-------|
| RxCIk | Duty Cycle | 45 | 50 | 55 | % |
| | RxCIk Frequency | | | | |
| | E3 | | 34.368 | | MHz |
| | DS-3 | | 44.736 | | MHz |
| | STS-1 | | 51.84 | | MHz |
| t _{RRX} | RxCIk rise time (10% o 90%) | | 2 | 4 | ns |
| t _{FRX} | RxCIk falling time (10% to 90%) | | 2 | 4 | ns |
| t _{CO} | RxCIk to RPOS/RNEG delay time | | | 4 | ns |
| t _{LCVO} | RxCIk to rising edge of LCV output delay | | 2.5 | | ns |

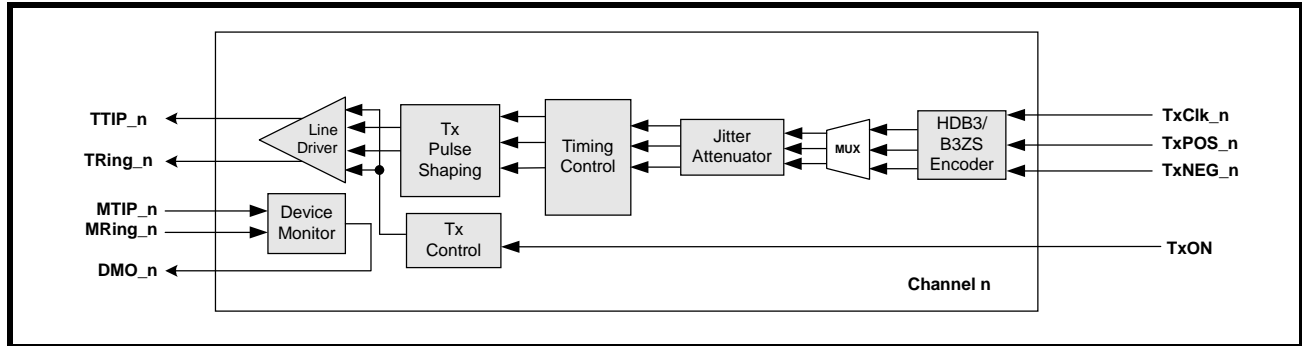
3.6 B3ZS/HDB3 Decoder

The decoder block takes the output from the clock and data recovery block and decodes the B3ZS (for DS3 or STS-1) or HDB3 (for E3) encoded line signal and detects any coding errors or excessive zeros in the data stream. Whenever the input signal violates the B3ZS or HDB3 coding sequence for bipolar violation or contains three (for B3ZS) or four (for HDB3) or more consecutive zeros, an active “High” pulse is generated on the RLCV_n output pins to indicate line code violation.

4.0 THE TRANSMITTER SECTION

The transmitter is designed so that the LIU can accept serial data from a local device, encode the data properly, and then output an analog pulse according to the pulse shape chosen in the appropriate registers. This section describes the detailed operation of various blocks within the transmit path. A simplified block diagram of the transmit path is shown in Figure 14.

FIGURE 14. TRANSMIT PATH BLOCK DIAGRAM



4.1 Transmit Digital Input Interface

The method for applying data to the transmit inputs of the LIU is a serial interface consisting of TxClk, TxPOS, and TxNEG. For single rail mode, only TxClk and TxPOS are necessary for providing the local data from a Framer device or ASIC. Data can be sampled on either edge of the input clock signal by programming the appropriate register. A typical interface is shown in Figure 15.

FIGURE 15. TYPICAL INTERFACE BETWEEN TERMINAL EQUIPMENT AND THE XRT75R06 (DUAL-RAIL DATA)

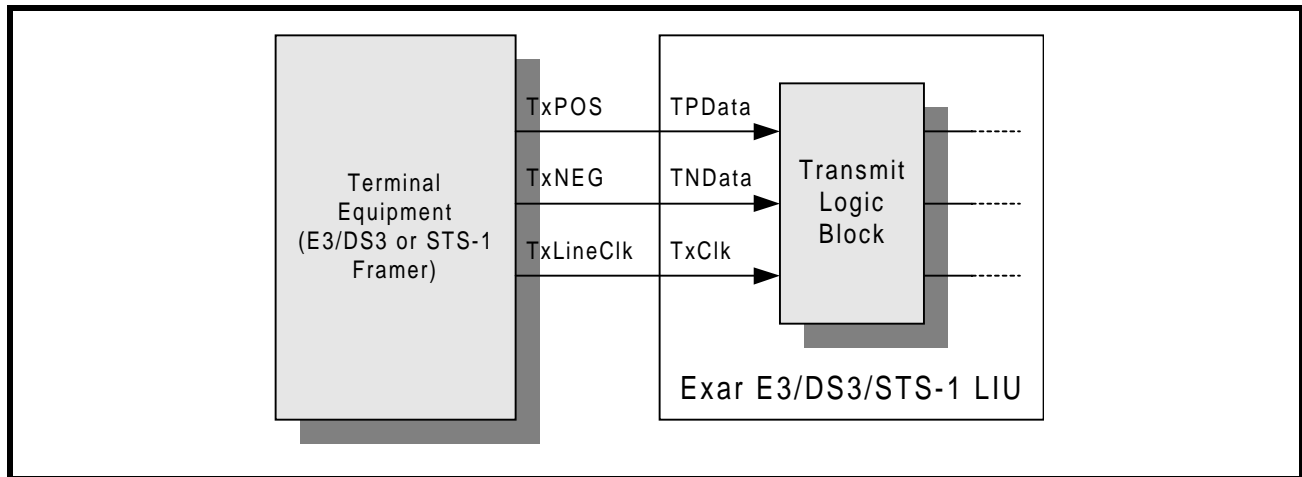
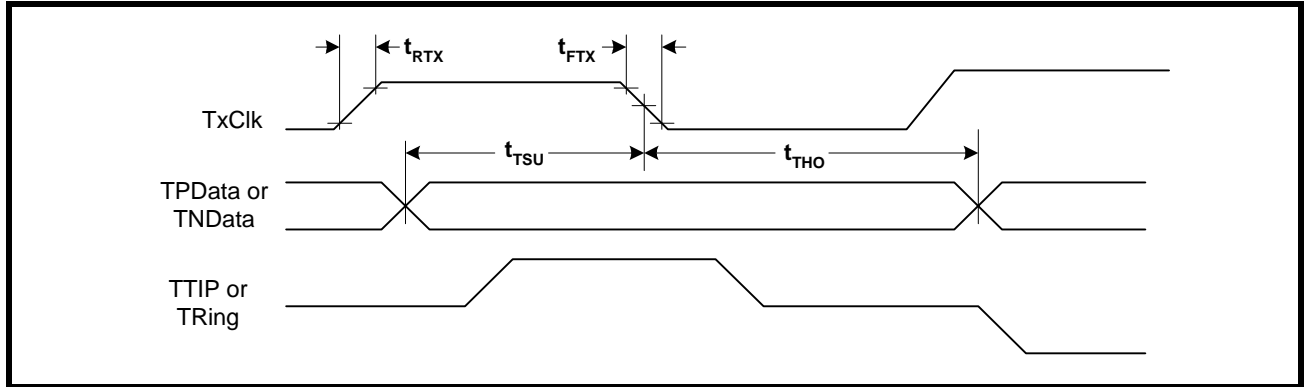


FIGURE 16. TRANSMITTER TERMINAL INPUT TIMING



| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS |
|-----------|---|-----|--------|-----|-------|
| TxCk | Duty Cycle | 30 | 50 | 70 | % |
| | TxCk Frequency | | | | |
| | E3 | | 34.368 | | MHz |
| | DS-3 | | 44.736 | | MHz |
| | STS-1 | | 51.84 | | MHz |
| t_{RTX} | TxCk Rise Time (10% to 90%) | | | 4 | ns |
| t_{FTX} | TxCk Fall Time (10% to 90%) | | | 4 | ns |
| t_{TSU} | TPData/TNData to TxCk falling set up time | 3 | | | ns |
| t_{THO} | TPData/TNData to TxCk falling hold time | 3 | | | ns |

FIGURE 17. SINGLE-RAIL OR NRZ DATA FORMAT (ENCODER AND DECODER ARE ENABLED)

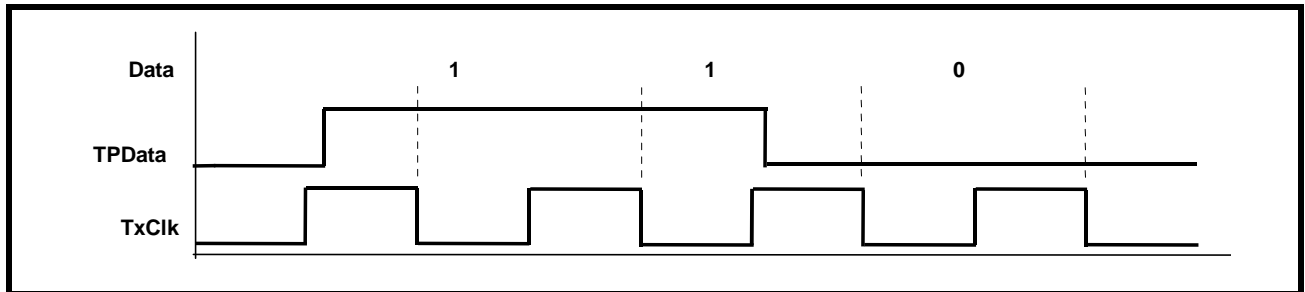
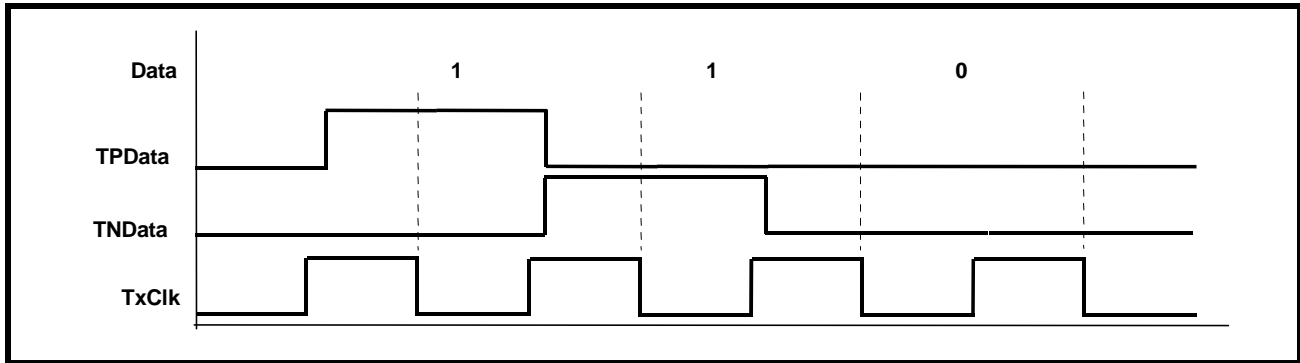


FIGURE 18. DUAL-RAIL DATA FORMAT (ENCODER AND DECODER ARE DISABLED)



4.2 Transmit Clock

The Transmit Clock applied via TxClk_n pins, for the selected data rate (for E3 = 34.368 MHz, DS3 = 44.736 MHz or STS-1 = 51.84 MHz), is duty cycle corrected by the internal PLL circuit to provide a 50% duty cycle clock to the pulse shaping circuit. This allows a 30% to 70% duty cycle Transmit Clock to be supplied.

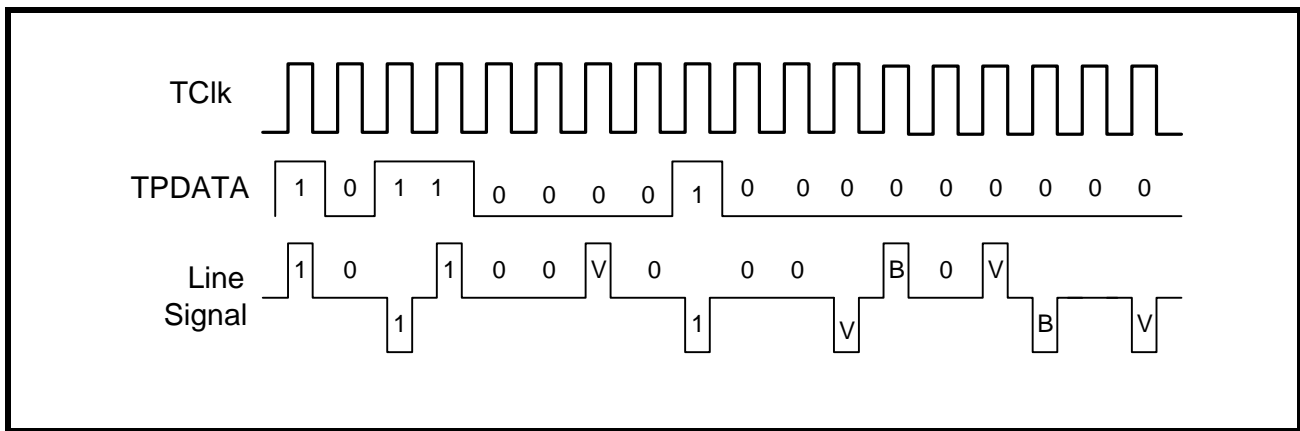
4.3 B3ZS/HDB3 ENCODER

When the Single-Rail (NRZ) data format is selected, the Encoder Block encodes the data into either B3ZS format (for either DS3 or STS-1) or HDB3 format (for E3).

4.3.1 B3ZS Encoding

An example of B3ZS encoding is shown in Figure 19. If the encoder detects an occurrence of three consecutive zeros in the data stream, it is replaced with either B0V or 00V, where 'B' refers to Bipolar pulse that is compliant with the Alternating polarity requirement of the AMI (Alternate Mark Inversion) line code and 'V' refers to a Bipolar Violation (e.g., a bipolar pulse that violates the AMI line code). The substitution of B0V or 00V is made so that an odd number of bipolar pulses exist between any two consecutive violation (V) pulses. This avoids the introduction of a DC component into the line signal.

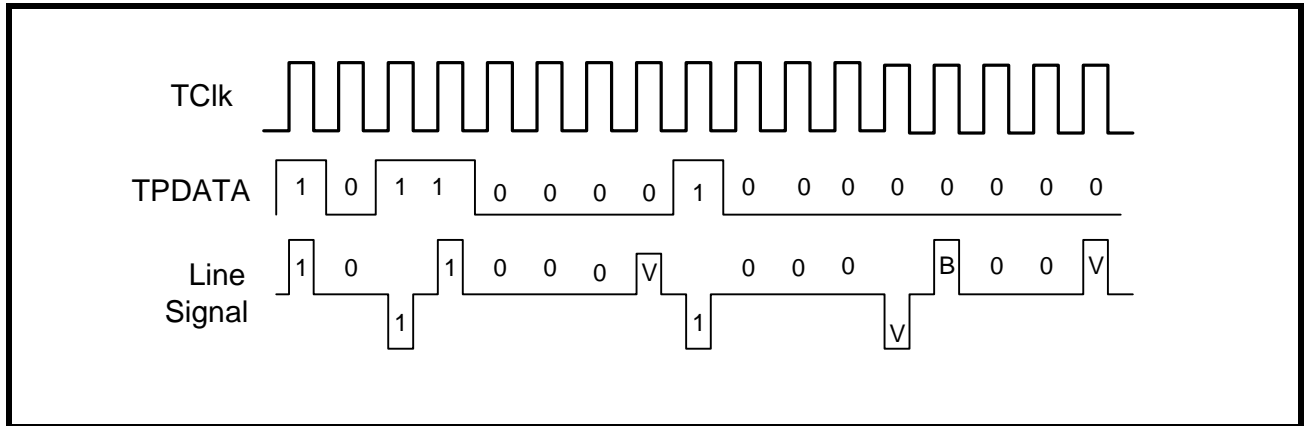
FIGURE 19. B3ZS ENCODING FORMAT



4.3.2 HDB3 Encoding

An example of the HDB3 encoding is shown in Figure 20. If the HDB3 encoder detects an occurrence of four consecutive zeros in the data stream, then the four zeros are substituted with either 000V or B00V pattern. The substitution code is made in such a way that an odd number of pulses exist between any consecutive V pulses. This avoids the introduction of DC component into the analog signal.

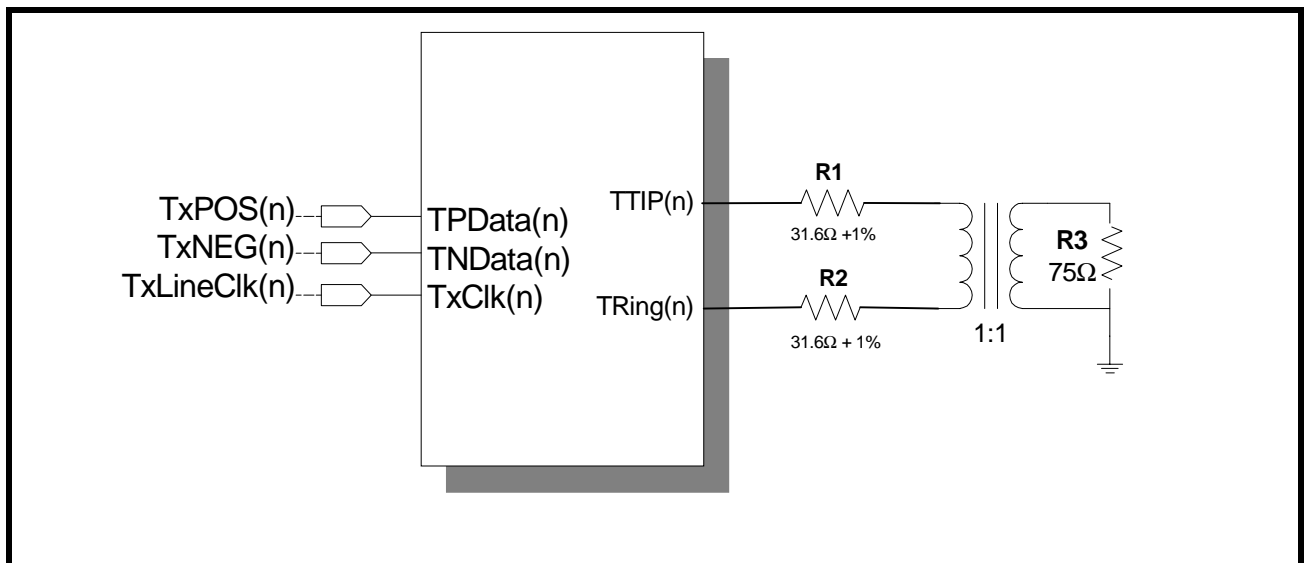
FIGURE 20. HDB3 ENCODING FORMAT



4.4 TRANSMIT PULSE SHAPER

The Transmit Pulse Shaper converts the B3ZS encoded digital pulses into a single analog Alternate Mark Inversion (AMI) pulse that meets the industry standard mask template requirements for STS-1 and DS3. For E3 mode, the pulse shaper converts the HDB3 encoded pulses into a single full amplitude square shaped pulse with very little slope. The Pulse Shaper Block also includes a Transmit Build Out Circuit, which can either be disabled or enabled by setting the TxLEV_n bit to "1" or "0" in the control register. For DS3/STS-1 rates, the Transmit Build Out Circuit is used to shape the transmit waveform that ensures that transmit pulse template requirements are met at the Cross-Connect system. The distance between the transmitter output and the Cross-Connect system can be between 0 to 450 feet. For E3 rate, since the output pulse template is measured at the secondary of the transformer and since there is no Cross-Connect system pulse template requirements, the Transmit Build Out Circuit is always disabled. The differential line driver increases the transmit waveform to appropriate level and drives into the 75Ω load as shown in Figure 21.

FIGURE 21. TRANSMIT PULSE SHAPE TEST CIRCUIT



4.4.1 Guidelines for using Transmit Build Out Circuit

If the distance between the transmitter and the DSX3 or STSX-1, Cross-Connect system, is less than 225 feet, enable the Transmit Build Out Circuit by setting the TxLEV_n control bit to "0". If the distance between the transmitter and the DSX3 or STSX-1 is greater than 225 feet, disable the Transmit Build Out Circuit.

4.5 E3 line side parameters

The XRT75R06 line output at the transformer output meets the pulse shape specified in ITU-T G.703 for 34.368 Mb/s operation. The pulse mask as specified in ITU-T G.703 for 34.368 Mb/s is shown in Figure 22.

FIGURE 22. PULSE MASK FOR E3 (34.368 MBITS/S) INTERFACE AS PER ITU-T G.703

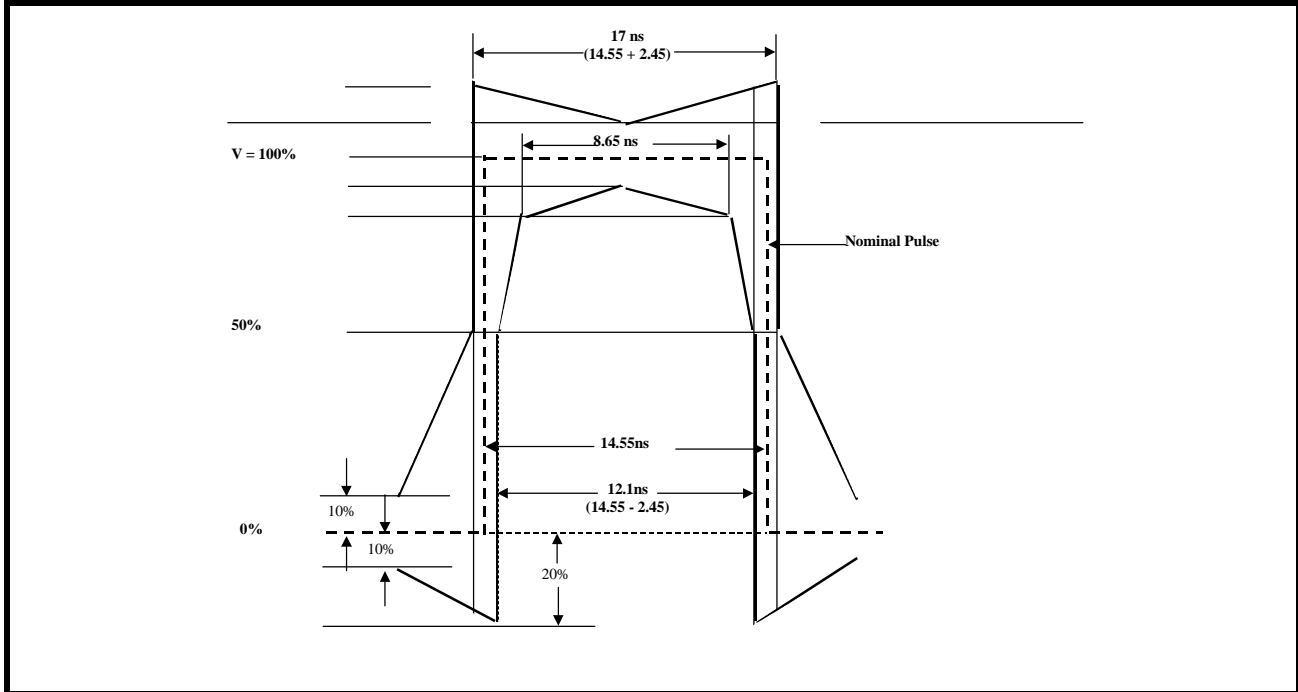


TABLE 3: E3 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS

| PARAMETER | MIN | TYP | MAX | UNITS |
|---|------|-------|------|------------------|
| TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS | | | | |
| Transmit Output Pulse Amplitude (Measured at secondary of the transformer) | 0.90 | 1.00 | 1.10 | V _{pk} |
| Transmit Output Pulse Amplitude Ratio | 0.95 | 1.00 | 1.05 | |
| Transmit Output Pulse Width | 12.5 | 14.55 | 16.5 | ns |
| Transmit Intrinsic Jitter | | 0.02 | 0.05 | UI _{pp} |
| RECEIVER LINE SIDE INPUT CHARACTERISTICS | | | | |
| Receiver Sensitivity (length of cable) | 900 | 1200 | | feet |
| Interference Margin | -20 | -14 | | dB |
| Jitter Tolerance @ Jitter Frequency 800KHz | 0.15 | 0.28 | | UI _{pp} |
| Signal level to Declare Loss of Signal | | | -35 | dB |
| Signal Level to Clear Loss of Signal | -15 | | | dB |
| Occurrence of LOS to LOS Declaration Time | 10 | | 255 | UI |
| Termination of LOS to LOS Clearance Time | 10 | | 255 | UI |

NOTE: The above values are at $T_A = 25^{\circ}C$ and $V_{DD} = 3.3 V \pm 5\%$.

FIGURE 23. BELLCORE GR-253 CORE TRANSMIT OUTPUT PULSE TEMPLATE FOR SONET STS-1 APPLICATIONS

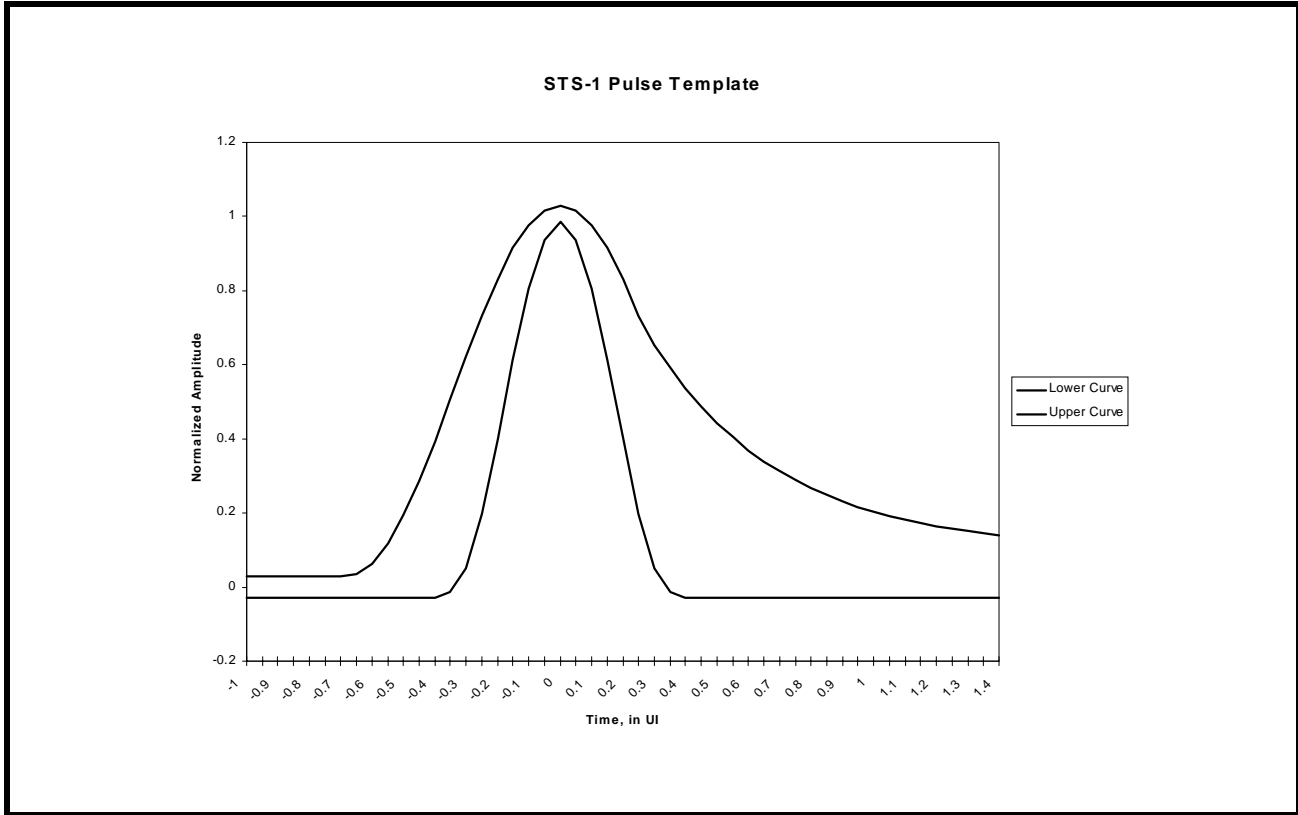


TABLE 4: STS-1 PULSE MASK EQUATIONS

| TIME IN UNIT INTERVALS | NORMALIZED AMPLITUDE |
|---------------------------|---|
| LOWER CURVE | |
| $-0.85 \leq T \leq -0.38$ | - 0.03 |
| $-0.38 \leq T \leq 0.36$ | $0.5 \left[1 + \sin \left\{ \frac{\pi}{2} \left(1 + \frac{T}{0.18} \right) \right\} \right] - 0.03$ |
| $0.36 \leq T \leq 1.4$ | - 0.03 |
| UPPER CURVE | |
| $-0.85 \leq T \leq -0.68$ | 0.03 |
| $-0.68 \leq T \leq 0.26$ | $0.5 \left[1 + \sin \left\{ \frac{\pi}{2} \left(1 + \frac{T}{0.34} \right) \right\} \right] + 0.03$ |
| $0.26 \leq T \leq 1.4$ | $0.1 + 0.61 \times e^{-2.4[T-0.26]}$ |

TABLE 5: STS-1 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS (GR-253)

| PARAMETER | MIN | TYP | MAX | UNITS |
|--|-------------------|------|------|------------------|
| TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS | | | | |
| Transmit Output Pulse Amplitude (measured with TxLEV = 0) | 0.65 | 0.75 | 0.90 | V _{pk} |
| Transmit Output Pulse Amplitude (measured with TxLEV = 1) | 0.90 | 1.00 | 1.10 | V _{pk} |
| Transmit Output Pulse Width | 8.6 | 9.65 | 10.6 | ns |
| Transmit Output Pulse Amplitude Ratio | 0.90 | 1.00 | 1.10 | |
| Transmit Intrinsic Jitter | | 0.02 | 0.05 | UI _{pp} |
| RECEIVER LINE SIDE INPUT CHARACTERISTICS | | | | |
| Receiver Sensitivity (length of cable) | 900 | 1100 | | feet |
| Jitter Tolerance @ Jitter Frequency 400 KHz | 0.15 | | | UI _{pp} |
| Signal Level to Declare Loss of Signal | Refer to Table 10 | | | |
| Signal Level to Clear Loss of Signal | Refer to Table 10 | | | |

NOTE: The above values are at TA = 25°C and V_{DD} = 3.3 V ± 5%.

FIGURE 24. TRANSMIT OUPUT PULSE TEMPLATE FOR DS3 AS PER BELLCORE GR-499

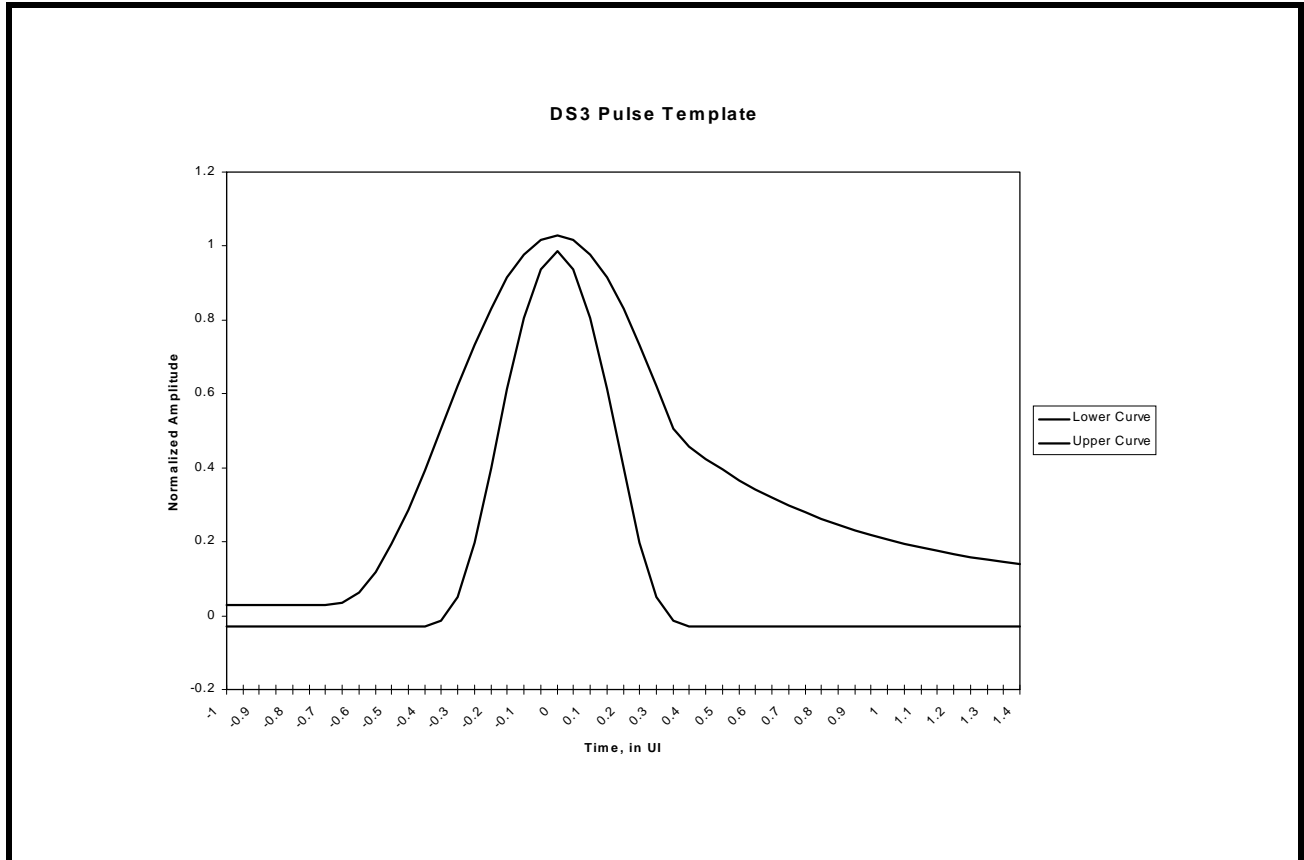


TABLE 6: DS3 PULSE MASK EQUATIONS

| TIME IN UNIT INTERVALS | NORMALIZED AMPLITUDE |
|---------------------------|---|
| LOWER CURVE | |
| $-0.85 \leq T \leq -0.36$ | - 0.03 |
| $-0.36 \leq T \leq 0.36$ | $0.5 \left[1 + \sin \left\{ \frac{\pi}{2} \left(1 + \frac{T}{0.18} \right) \right\} \right] - 0.03$ |
| $0.36 \leq T \leq 1.4$ | - 0.03 |
| UPPER CURVE | |
| $-0.85 \leq T \leq -0.68$ | 0.03 |
| $-0.68 \leq T \leq 0.36$ | $0.5 \left[1 + \sin \left\{ \frac{\pi}{2} \left(1 + \frac{T}{0.34} \right) \right\} \right] + 0.03$ |
| $0.36 \leq T \leq 1.4$ | $0.08 + 0.407 \times e^{-1.84[T-0.36]}$ |

TABLE 7: DS3 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS (GR-499)

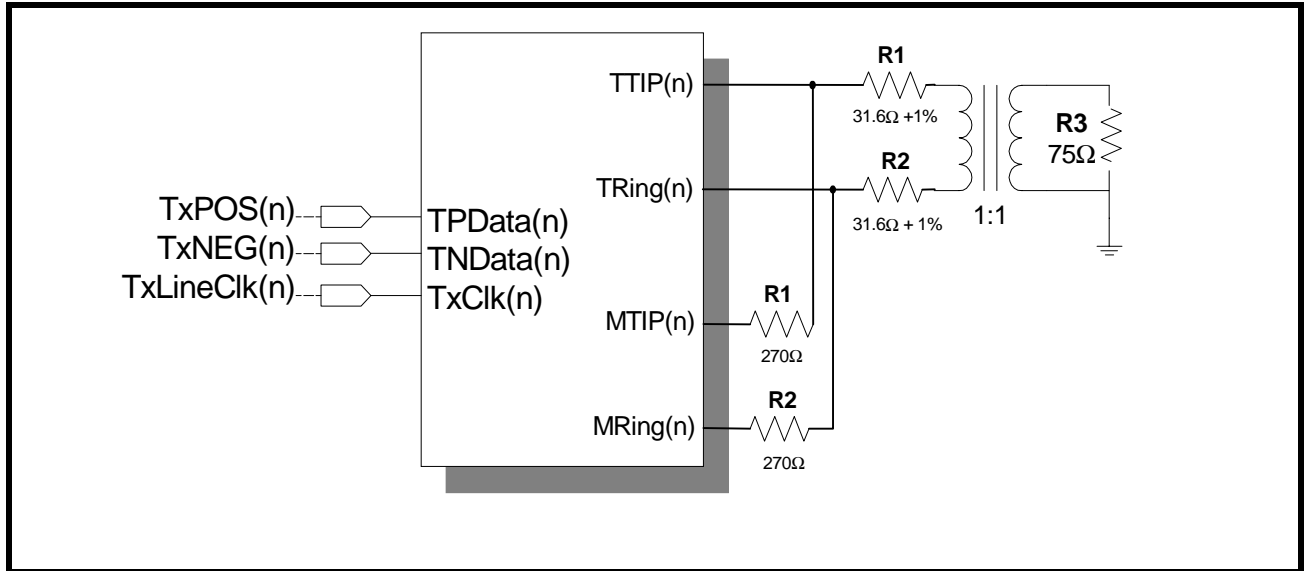
| PARAMETER | MIN | TP | MAX | UNITS |
|--|-------------------|-------|-------|------------------|
| TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS | | | | |
| Transmit Output Pulse Amplitude (measured with TxLEV = 0) | 0.65 | 0.75 | 0.85 | V _{pk} |
| Transmit Output Pulse Amplitude (measured with TxLEV = 1) | 0.90 | 1.00 | 1.10 | V _{pk} |
| Transmit Output Pulse Width | 10.10 | 11.18 | 12.28 | ns |
| Transmit Output Pulse Amplitude Ratio | 0.90 | 1.00 | 1.10 | |
| Transmit Intrinsic Jitter | | 0.02 | 0.05 | UI _{pp} |
| RECEIVER LINE SIDE INPUT CHARACTERISTICS | | | | |
| Receiver Sensitivity (length of cable) | 900 | 1100 | | feet |
| Jitter Tolerance @ 400 KHz (Cat II) | 0.15 | | | UI _{pp} |
| Signal Level to Declare Loss of Signal | Refer to Table 10 | | | |
| Signal Level to Clear Loss of Signal | Refer to Table 10 | | | |

NOTE: The above values are at TA = 25°C and V_{DD} = 3.3V ± 5%.

4.6 Transmit Drive Monitor

This feature is used for monitoring the transmit line for occurrence of fault conditions such as a short circuit on the line or a defective line driver. To activate this function, connect MTIP_n pins to the TTIP_n lines via a 270Ω resistor and MRing_n pins to TRing_n lines via 270Ω resistor as shown in Figure 25.

FIGURE 25. TRANSMIT DRIVER MONITOR SET-UP.



When the MTIP_n and MRing_n are connected to the TTIP_n and TRing_n lines, the drive monitor circuit monitors the line for transitions. The DMO_n (Drive Monitor Output) will be asserted “Low” as long as the transitions on the line are detected via MTIP_n and MRing_n. If no transitions on the line are detected for 128 ± 32 TxClk_n periods, the DMO_n output toggles “High” and when the transitions are detected again, DMO_n toggles “Low”.

NOTE: The Drive Monitor Circuit is only for diagnostic purpose and does not have to be used to operate the transmitter.

4.7 Transmitter Section On/Off

The transmitter section of each channel can either be turned on or off. To turn on the transmitter, set the input pin TxON to “High” and write a “1” to the TxON_n control bit. When the transmitter is turned off, TTIP_n and TRing_n are tri-stated.

NOTES:

1. This feature provides support for Redundancy.
2. To permit a system designed for redundancy to quickly shut-off the defective line card and turn on the back-up line card, writing a “1” to the TxON_n control bits transfers the control to TxON pin.

5.0 JITTER

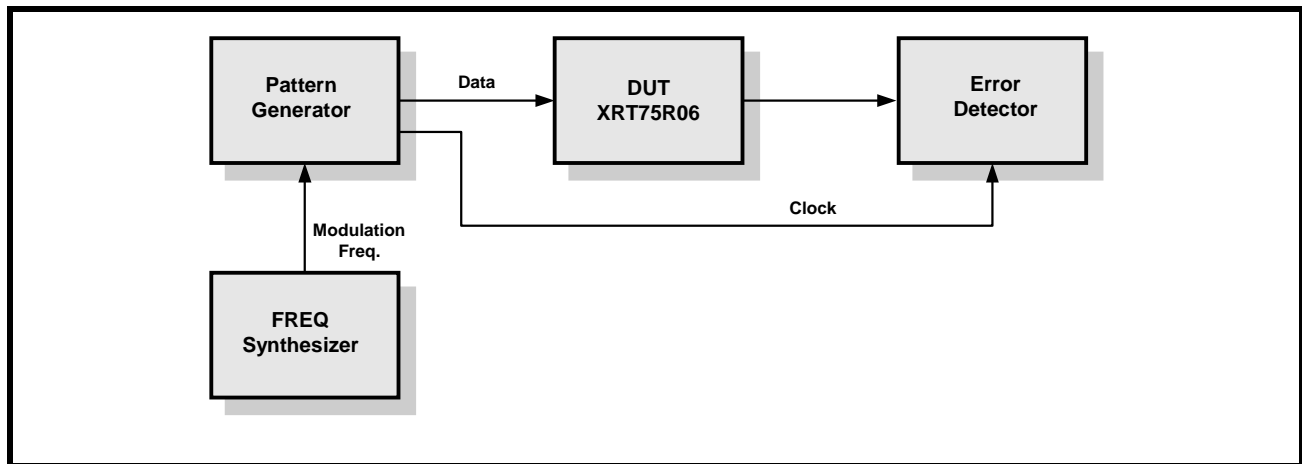
There are three fundamental parameters that describe circuit performance relative to jitter

- Jitter Tolerance
- Jitter Transfer
- Jitter Generation

5.1 JITTER TOLERANCE

Jitter tolerance is a measure of how well a Clock and Data Recovery unit can successfully recover data in the presence of various forms of jitter. It is characterized by the amount of jitter required to produce a specified bit error rate. The tolerance depends on the frequency content of the jitter. Jitter Tolerance is measured as the jitter amplitude over a jitter spectrum for which the clock and data recovery unit achieves a specified bit error rate (BER). To measure the jitter tolerance as shown in Figure 26, jitter is introduced by the sinusoidal modulation of the serial data bit sequence. Input jitter tolerance requirements are specified in terms of compliance with jitter mask which is represented as a combination of points. Each point corresponds to a minimum amplitude of sinusoidal jitter at a given jitter frequency.

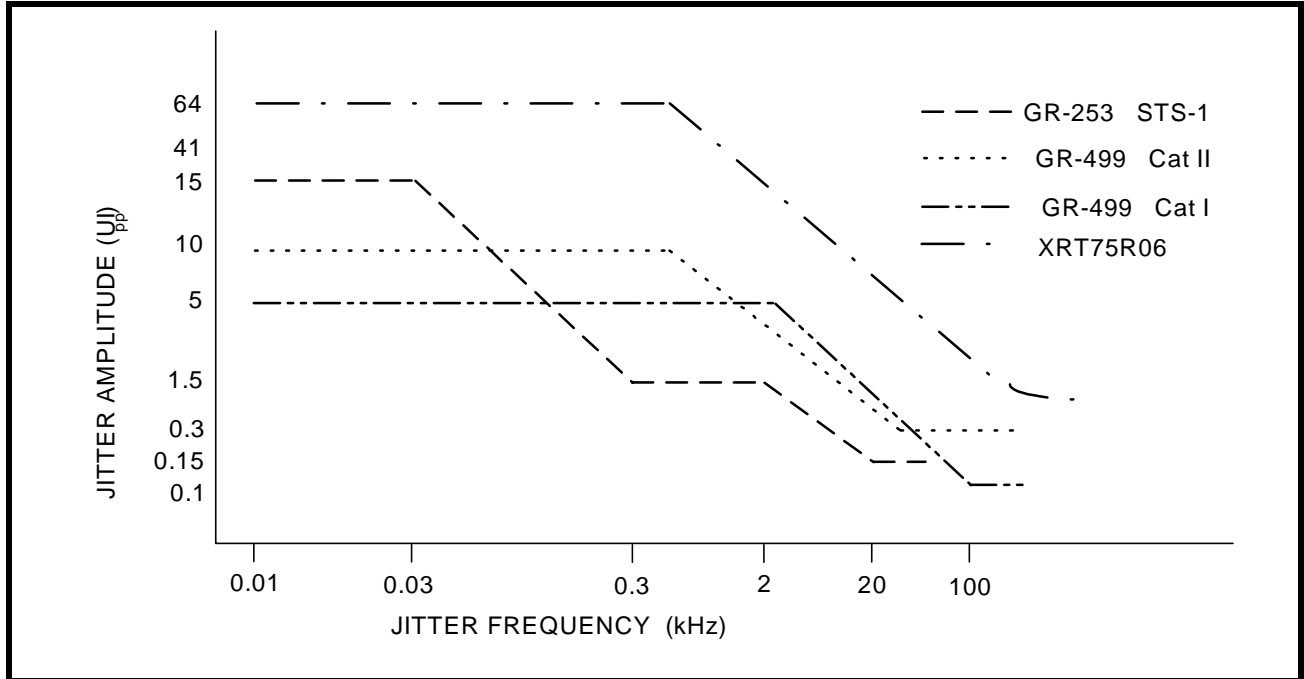
FIGURE 26. JITTER TOLERANCE MEASUREMENTS



5.1.1 DS3/STS-1 Jitter Tolerance Requirements

Bellcore GR-499 CORE specifies the minimum requirement of jitter tolerance for Category I and Category II. The jitter tolerance requirement for Category II is the most stringent. Figure 27 shows the jitter tolerance curve as per GR-499 specification.

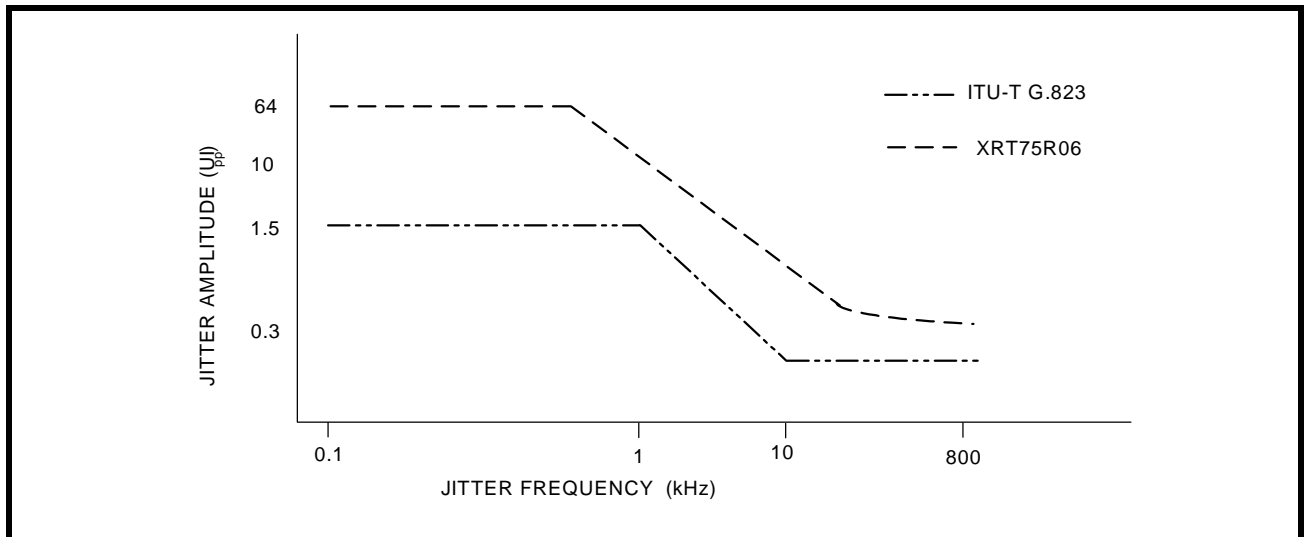
FIGURE 27. INPUT JITTER TOLERANCE FOR DS3/STS-1



5.1.2 E3 Jitter Tolerance Requirements

ITU-T G.823 standard specifies that the clock and data recovery unit must be able to tolerate jitter up to certain specified limits. Figure 28 shows the tolerance curve.

FIGURE 28. INPUT JITTER TOLERANCE FOR E3



As shown in the Figures above, in the jitter tolerance measurement, the dark line indicates the minimum level of jitter that the E3/DS3/STS-1 compliant component must tolerate. Table 8 below shows the jitter amplitude versus the modulation frequency for various standards.

TABLE 8: JITTER AMPLITUDE VERSUS MODULATION FREQUENCY (JITTER TOLERANCE)

| BIT RATE (KB/S) | STANDARD | INPUT JITTER AMPLITUDE (UI _{p-p}) | | | MODULATION FREQUENCY | | | | |
|-----------------|--------------------|---|------|------|----------------------|--------|---------|---------|---------|
| | | A1 | A2 | A3 | F1(Hz) | F2(Hz) | F3(kHz) | F4(kHz) | F5(kHz) |
| 34368 | ITU-T G.823 | 1.5 | 0.15 | - | 100 | 1000 | 10 | 800 | - |
| 44736 | GR-499 CORE Cat I | 5 | 0.1 | - | 10 | 2.3k | 60 | 300 | - |
| 44736 | GR-499 CORE Cat II | 10 | 0.3 | - | 10 | 669 | 22.3 | 300 | - |
| 51840 | GR-253 CORE Cat II | 15 | 1.5 | 0.15 | 10 | 30 | 300 | 2 | 20 |

5.2 JITTER TRANSFER

Jitter Transfer function is defined as the ratio of jitter on the output relative to the jitter applied on the input versus frequency. There are two distinct characteristics in jitter transfer, jitter gain (jitter peaking) defined as the highest ratio above 0dB and jitter transfer bandwidth. The overall jitter transfer bandwidth is controlled by a low bandwidth loop, typically using a voltage-controlled crystal oscillator (VCXO).

The jitter transfer function is a ratio between the jitter output and jitter input for a component, or system often expressed in dB. A negative dB jitter transfer indicates the element removed jitter. A positive dB jitter transfer indicates the element added jitter. A zero dB jitter transfer indicates the element had no effect on jitter. Table 9 shows the jitter transfer characteristics and/or jitter attenuation specifications for various data rates:

TABLE 9: JITTER TRANSFER SPECIFICATION/REFERENCES

| E3 | DS3 | STS-1 |
|-------------|--|-----------------------------|
| ETSI TBR-24 | GR-499 CORE section 7.3.2 Category I and Category II | GR-253 CORE section 5.6.2.1 |

NOTE: The above specifications can be met only with a jitter attenuator that supports E3/DS3/STS-1 rates.

5.3 Jitter Attenuator

An advanced crystal-less jitter attenuator per channel is included in the XRT75R06. The jitter attenuator requires no external crystal nor high-frequency reference clock. By clearing or setting the JATx/Rx_n bits in the channel control registers selects the jitter attenuator either in the Receive or Transmit path on per channel basis. The FIFO size can be either 16-bit or 32-bit. The bits JA0_n and JA1_n can be set to appropriate combination to select the different FIFO sizes or to disable the Jitter Attenuator on a per channel basis. Data is clocked into the FIFO with the associated clock signal (TxClk or RxClk) and clocked out of the FIFO with the dejittered clock. When the FIFO is within two bits of overflowing or underflowing, the FIFO limit status bit, FL_n is set to "1" in the Alarm status register. Reading this bit clears the FIFO and resets the bit into default state.

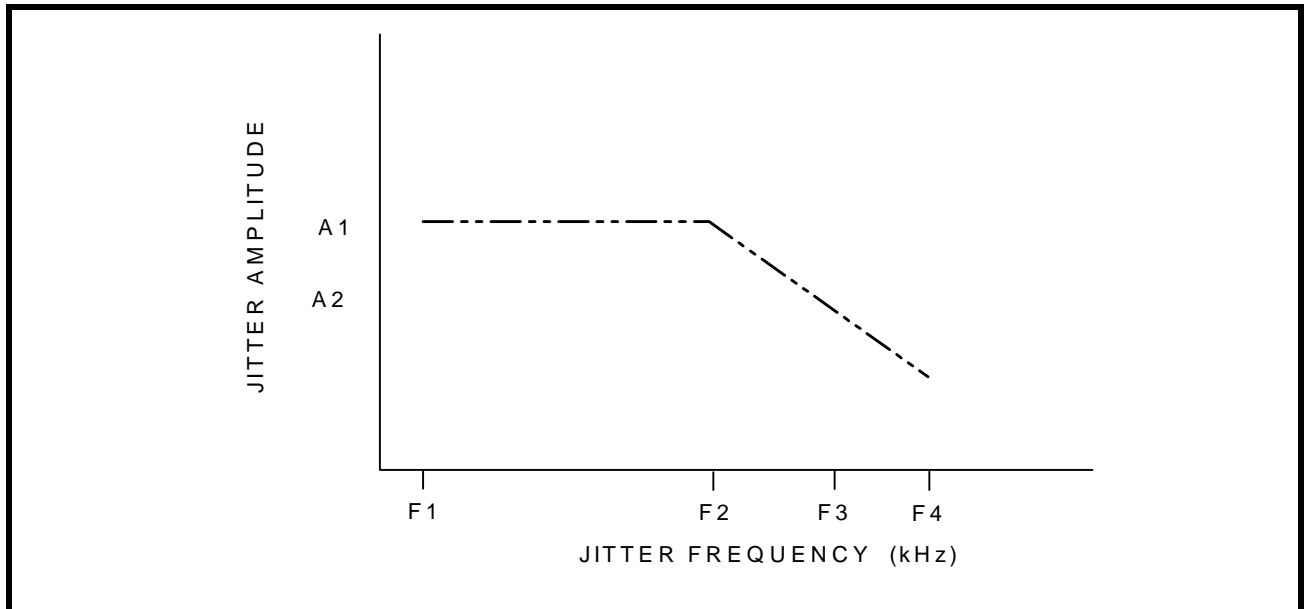
NOTE: It is recommended to select the 16-bit FIFO for delay-sensitive applications as well as for removing smaller amounts of jitter. Table 10 specifies the jitter transfer mask requirements for various data rates:

TABLE 10: JITTER TRANSFER PASS MASKS

| RATE (KBITS) | MASK | F1 (Hz) | F2 (Hz) | F3 (Hz) | F4 (kHz) | A1(dB) | A2(dB) |
|--------------|----------------------|---------|---------|---------|----------|--------|--------|
| 34368 | G.823 ETSI-TBR-24 | 100 | 300 | 3k | 800k | 0.5 | -19.5 |
| 44736 | GR-499, Cat I | 10 | 10k | - | 15k | 0.1 | - |
| | GR-499, Cat II | 10 | 56.6k | - | 300k | 0.1 | - |
| | GR-253 CORE | 10 | 40 | - | 15k | 0.1 | - |
| 51840 | GR-253 CORE | 10 | 40k | - | 400k | 0.1 | - |

The jitter attenuator within the XRT75R06 meets the latest jitter attenuation specifications and/or jitter transfer characteristics as shown in the Figure 29.

FIGURE 29. JITTER TRANSFER REQUIREMENTS AND JITTER ATTENUATOR PERFORMANCE



5.3.1 JITTER GENERATION

Jitter Generation is defined as the process whereby jitter appears at the output port of the digital equipment in the absence of applied input jitter. Jitter Generation is measured by sending jitter free data to the clock and data recovery circuit and measuring the amount of jitter on the output clock or the re-timed data. Since this is essentially a noise measurement, it requires a definition of bandwidth to be meaningful. The bandwidth is set according to the data rate. In general, the jitter is measured over a band of frequencies.

6.0 DIAGNOSTIC FEATURES

6.1 PRBS Generator and Detector

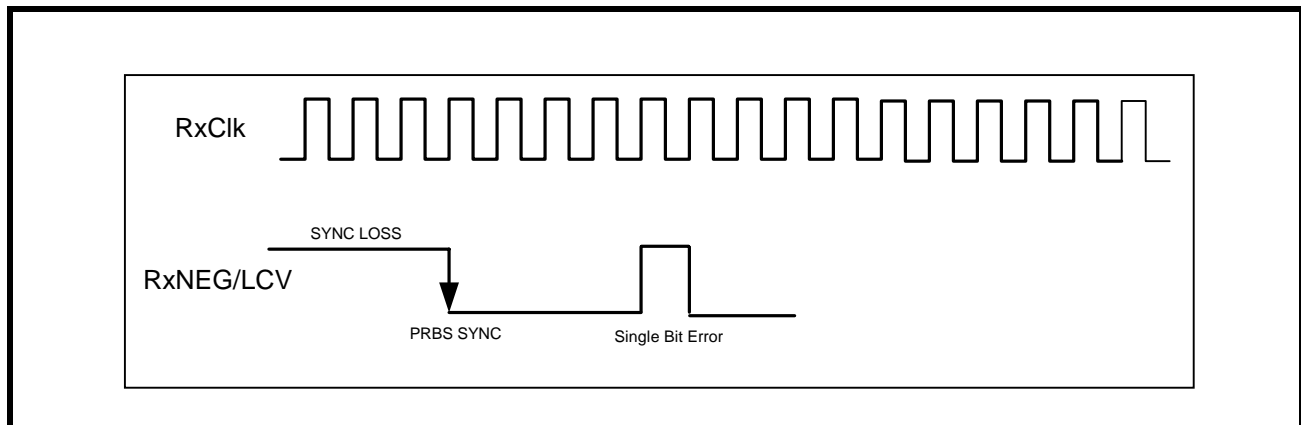
The XRT75R06 contains an on-chip Pseudo Random Binary Sequence (PRBS) generator and detector for diagnostic purpose. With the PRBSEN_n bit = "1", the transmitter will send out PRBS of $2^{23}-1$ in E3 rate or $2^{15}-1$ in STS-1/DS3 rate. At the same time, the receiver PRBS detector is also enabled. When the correct PRBS pattern is detected by the receiver, the RNEG/LCV pin will go "Low" to indicate PRBS synchronization has been achieved. When the PRBS detector is not in sync the PRBSLS bit will be set to "1" and RNEG/LCV pin will go "High".

With the PRBS mode enabled, the user can also insert a single bit error by toggling "INSPRBS" bit. This is done by writing a "1" to INSPRBS bit. The receiver at RNEG/LCV pin will pulse "High" for one RxClk cycle for every bit error detected. Any subsequent single bit error insertion must be done by first writing a "0" to INSPRBS bit and followed by a "1".

Figure 30 shows the status of RNEG/LCV pin when the XRT75R06 is configured in PRBS mode.

NOTE: In PRBS mode, the device is forced to operate in Single-Rail Mode.

FIGURE 30. PRBS MODE



6.2 LOOPBACKS

The XRT75R06 offers three loopback modes for diagnostic purposes. The loopback modes are selected via the RLB_n and LLB_n bits in the Channel control registers select the loopback modes.

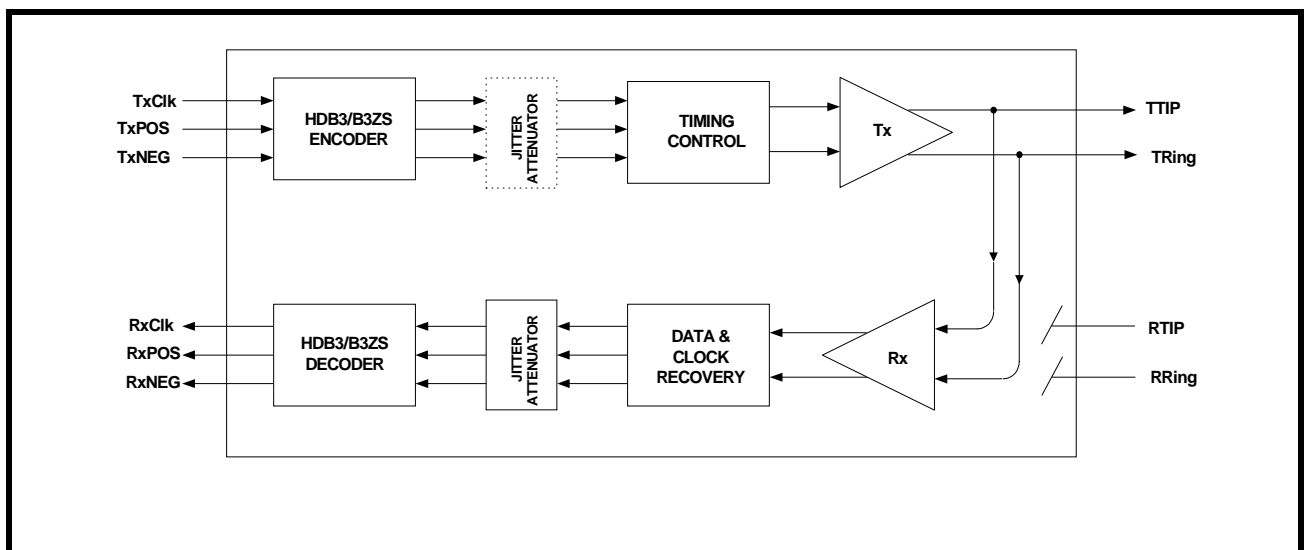
6.2.1 ANALOG LOOPBACK

In this mode, the transmitter outputs TTIP_n and TRing_n are internally connected to the receiver inputs RTIP_n and RRing_n as shown in Figure 31. Data and clock are output at RxClk_n, RxPOS_n and RxNEG_n pins for the corresponding transceiver. Analog loopback exercises most of the functional blocks of the device including the jitter attenuator which can be selected in either the transmit or receive path.

NOTES:

1. In the Analog loopback mode, data is also output via TTIP_n and TRing_n pins.
2. Signals on the RTIP_n and RRing_n pins are ignored during analog loopback.

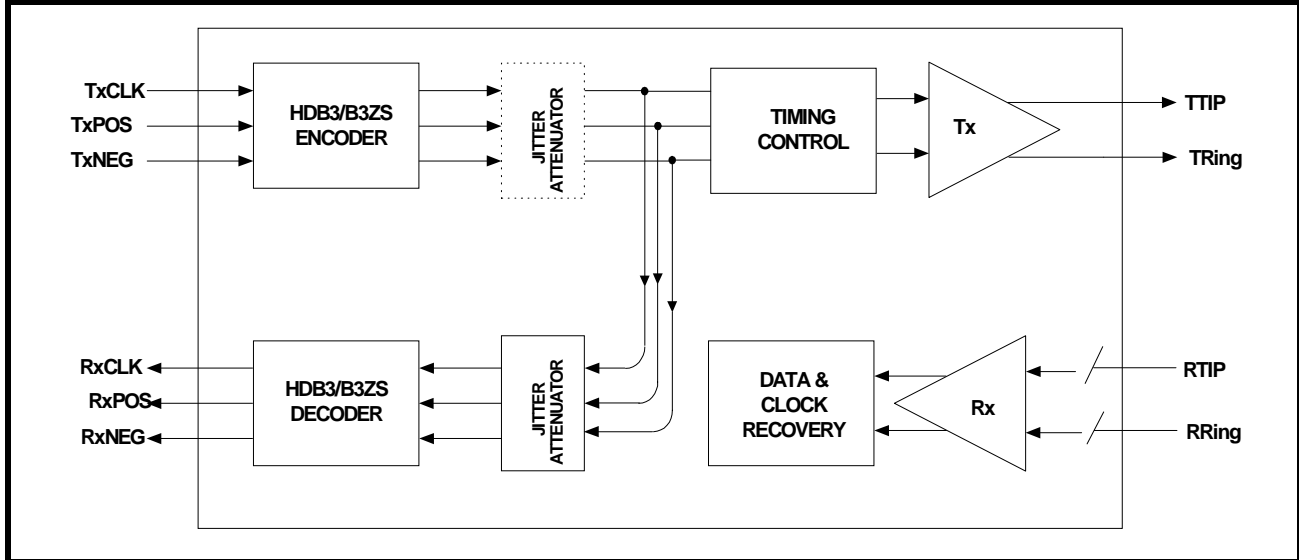
FIGURE 31. ANALOG LOOPBACK



6.2.2 DIGITAL LOOPBACK

When the Digital Loopback is selected, the transmit clock TxClk_n and transmit data inputs (TxPOS_n & TxNEG_n) are looped back and output onto the RxClk_n, RxPOS_n and RxNEG_n pins as shown in Figure 32.

FIGURE 32. DIGITAL LOOPBACK

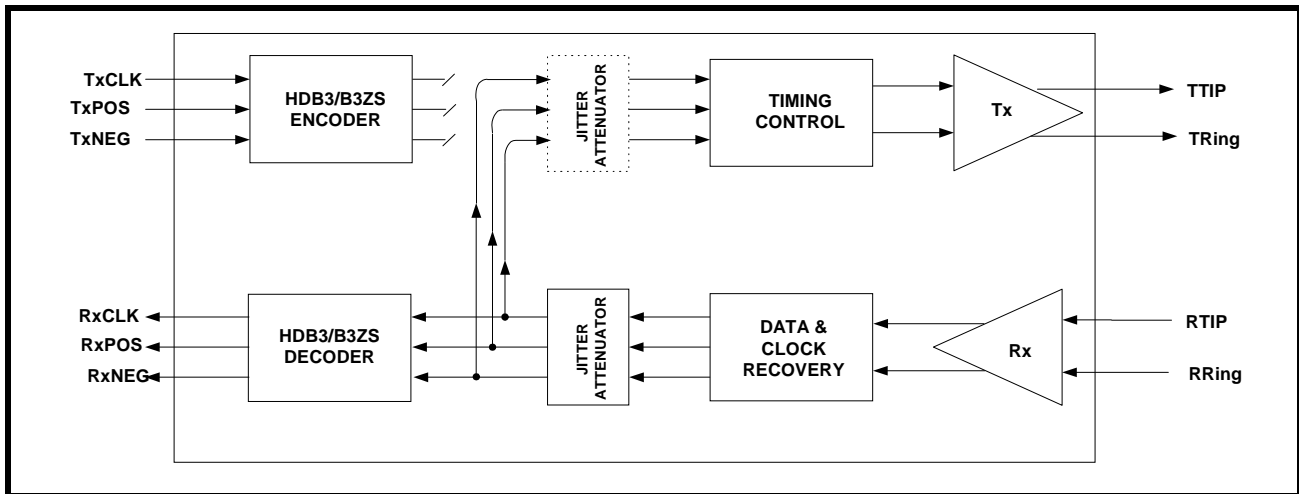


6.2.3 REMOTE LOOPBACK

With Remote loopback activated as shown in Figure 33, the receive data on RTIP and RRing is looped back after the jitter attenuator (if selected in receive or transmit path) to the transmit path using RxClk as transmit timing. The receive data is also output via the RxPOS and RxNEG pins.

NOTE: Input signals on TxClk, TxPOS and TxNEG are ignored during Remote loopback.

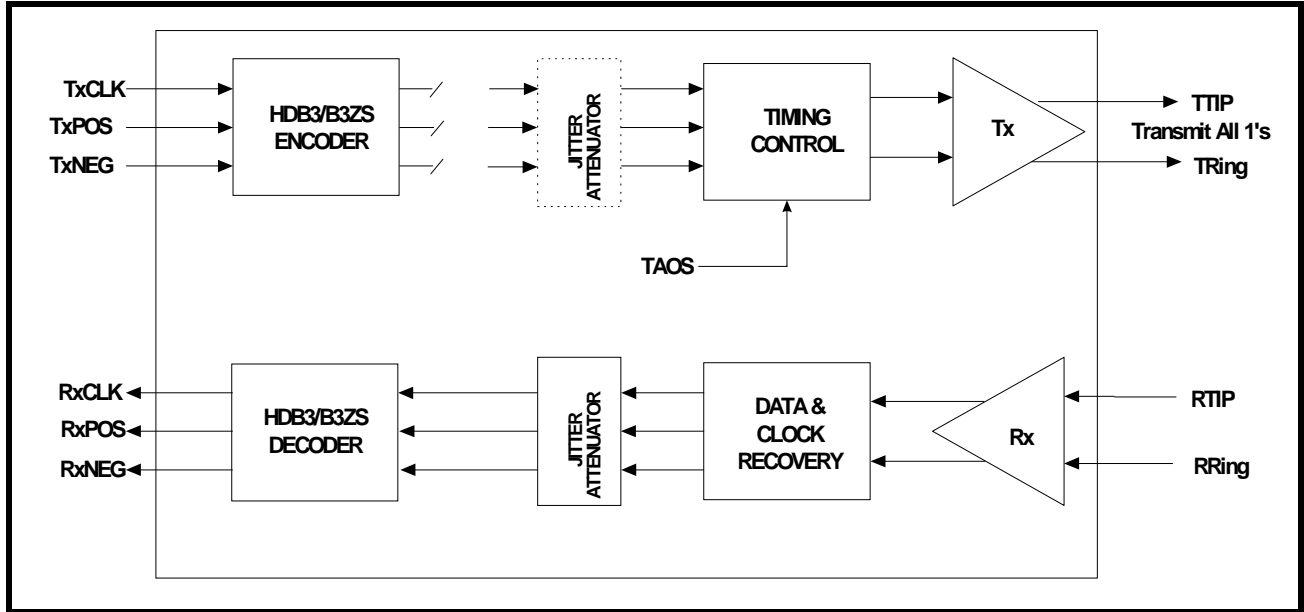
FIGURE 33. REMOTE LOOPBACK



6.3 TRANSMIT ALL ONES (TAOS)

Transmit All Ones (TAOS) can be set by setting the TAOS_n control bits to “1” in the Channel control registers. When the TAOS is set, the Transmit Section generates and transmits a continuous AMI all “1’s” pattern on TTIP_n and TRing_n pins. The frequency of this ones pattern is determined by TxClk_n. The TAOS data path is shown in Figure 34. TAOS does not operate in Analog loopback or Remote loopback modes, however will function in Digital loopback mode.

FIGURE 34. TRANSMIT ALL ONES (TAOS)



7.0 MICROPROCESSOR INTERFACE BLOCK

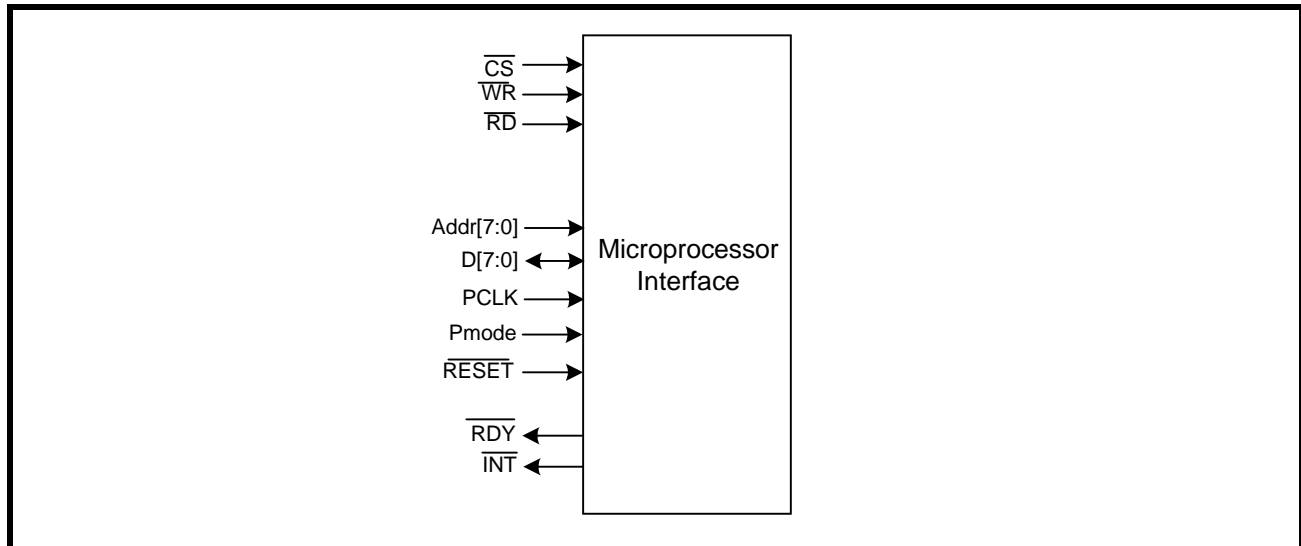
The Microprocessor Interface section supports communication between the local microprocessor (μP) and the LIU. The XRT75R06 supports a parallel interface asynchronously or synchronously timed to the LIU. The microprocessor interface is selected by the state of the Pmode input pin. Selecting the microprocessor interface mode is shown in Table 11.

TABLE 11: SELECTING THE MICROPROCESSOR INTERFACE MODE

| Pmode | Microprocessor Mode |
|--------|---------------------|
| "Low" | Asynchronous Mode |
| "High" | Synchronous Mode |

The local μP configures the LIU by writing data into specific addressable, on-chip Read/Write registers. The μP provides the signals which are required for a general purpose microprocessor to read or write data into these registers. The μP also supports polled and interrupt driven environments. A simplified block diagram of the microprocessor is shown in Figure 35.

FIGURE 35. SIMPLIFIED BLOCK DIAGRAM OF THE MICROPROCESSOR INTERFACE BLOCK



7.1 THE MICROPROCESSOR INTERFACE BLOCK SIGNALS

The LIU may be configured into different operating modes and have its performance monitored by software through a standard microprocessor using data, address and control signals. These interface signals are described below in Table 12. The microprocessor interface can be configured to operate in Asynchronous mode or Synchronous mode.

TABLE 12: XRT75R06 MICROPROCESSOR INTERFACE SIGNALS

| PIN NAME | TYPE | DESCRIPTION |
|--------------------|------|---|
| Pmode | I | Microprocessor Interface Mode Select Input pin This pin is used to specify the microprocessor interface mode. |
| D[7:0] | I/O | Bi-Directional Data Bus for register "Read" or "Write" Operations. |
| Addr[7:0] | I | Eight-Bit Address Bus Inputs The XRT75R06 LIU microprocessor interface uses a direct address bus. This address bus is provided to permit the user to select an on-chip register for Read/Write access. |
| \overline{CS} | I | Chip Select Input This active low signal selects the microprocessor interface of the XRT75R06 LIU and enables Read/Write operations with the on-chip register locations. |
| \overline{RD} | I | Read Signal This active low input functions as the read signal from the local μP . When this pin is pulled "Low" (if \overline{CS} is "Low") the LIU is informed that a read operation has been requested and begins the process of the read cycle. |
| \overline{WR} | I | Write Signal This active low input functions as the write signal from the local μP . When this pin is pulled "Low" (if \overline{CS} is "Low") the LIU is informed that a write operation has been requested and begins the process of the write cycle. |
| \overline{RDY} | O | Ready Output This active low signal is provided by the LIU device. It indicates that the current read or write cycle is complete, and the LIU is waiting for the next command. |
| \overline{INT} | O | Interrupt Output This active low signal is provided by the LIU to alert the local mP that a change in alarm status has occurred. This pin is Reset Upon Read (RUR) once the alarm status registers have been cleared. |
| \overline{RESET} | I | Reset Input This active low input pin is used to Reset the LIU. |

7.2 ASYNCHRONOUS AND SYNCHRONOUS DESCRIPTION

Whether the LIU is configured for Asynchronous or Synchronous mode, the following descriptions apply. The synchronous mode requires an input clock (PCLK) to be used as the microprocessor timing reference. Read and Write operations are described below.

Read Cycle (For Pmode = "0" or "1")

Whenever the local μP wishes to read the contents of a register, it should do the following.

1. Place the address of the target register on the address bus input pins Addr[7:0].
2. While the μP is placing this address value on the address bus, the address decoding circuitry should assert the $\overline{\text{CS}}$ pin of the LIU, by toggling it "Low". This action enables communication between the μP and the LIU microprocessor interface block.
3. Next, the μP should indicate that this current bus cycle is a Read operation by toggling the $\overline{\text{RD}}$ input pin "Low". This action enables the bi-directional data bus output drivers of the LIU.
4. After the μP toggles the Read signal "Low", the LIU will toggle the $\overline{\text{RDY}}$ output pin "Low". The LIU does this to inform the μP that the data is available to be read by the μP , and that it is ready for the next command.
5. After the μP detects the $\overline{\text{RDY}}$ signal and has read the data, it can terminate the Read Cycle by toggling the $\overline{\text{RD}}$ input pin "High".
6. The $\overline{\text{CS}}$ input pin must be pulled "High" before a new command can be issued.

Write Cycle (For Pmode = "0" or "1")

Whenever a local μP wishes to write a byte or word of data into a register within the LIU, it should do the following.

1. Place the address of the target register on the address bus input pins Addr[7:0].
2. While the μP is placing this address value on the address bus, the address decoding circuitry should assert the $\overline{\text{CS}}$ pin of the LIU, by toggling it "Low". This action enables communication between the μP and the LIU microprocessor interface block.
3. The μP should then place the byte or word that it intends to write into the target register, on the bi-directional data bus D[7:0].
4. Next, the μP should indicate that this current bus cycle is a Write operation by toggling the $\overline{\text{WR}}$ input pin "Low". This action enables the bi-directional data bus input drivers of the LIU.
5. After the μP toggles the Write signal "Low", the LIU will toggle the $\overline{\text{RDY}}$ output pin "Low". The LIU does this to inform the μP that the data has been written into the internal register location, and that it is ready for the next command.
6. The $\overline{\text{CS}}$ input pin must be pulled "High" before a new command can be issued.

FIGURE 36. ASYNCHRONOUS μ P INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

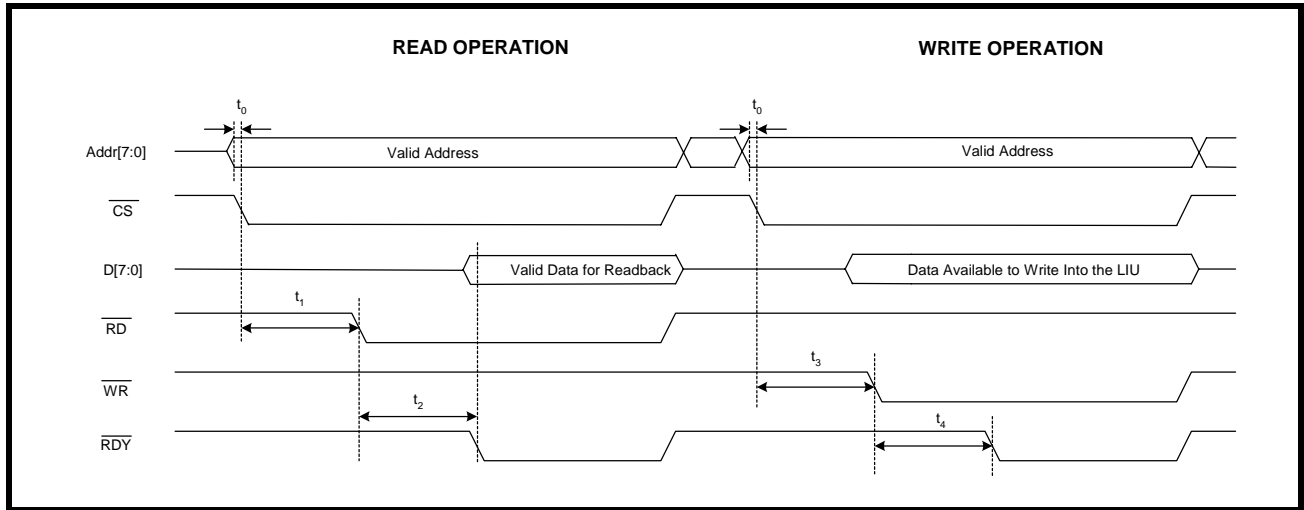


TABLE 13: ASYNCHRONOUS TIMING SPECIFICATIONS

| SYMBOL | PARAMETER | MIN | MAX | UNITS |
|--------|--|-----|-----|-------|
| t_0 | Valid Address to \overline{CS} Falling Edge | 0 | - | ns |
| t_1 | \overline{CS} Falling Edge to \overline{RD} Assert | 0 | - | ns |
| t_2 | \overline{RD} Assert to \overline{RDY} Assert | - | 65 | ns |
| NA | \overline{RD} Pulse Width (t_2) | 70 | - | ns |
| t_3 | \overline{CS} Falling Edge to \overline{WR} Assert | 0 | - | ns |
| t_4 | \overline{WR} Assert to \overline{RDY} Assert | - | 65 | ns |
| NA | \overline{WR} Pulse Width (t_4) | 70 | - | ns |

FIGURE 37. SYNCHRONOUS μ P INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

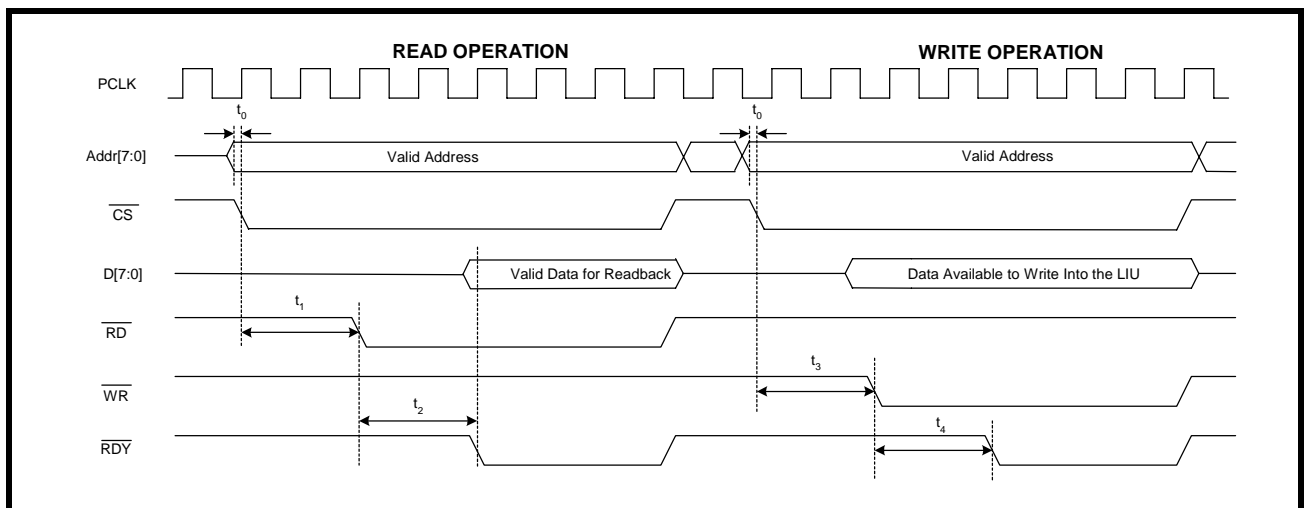
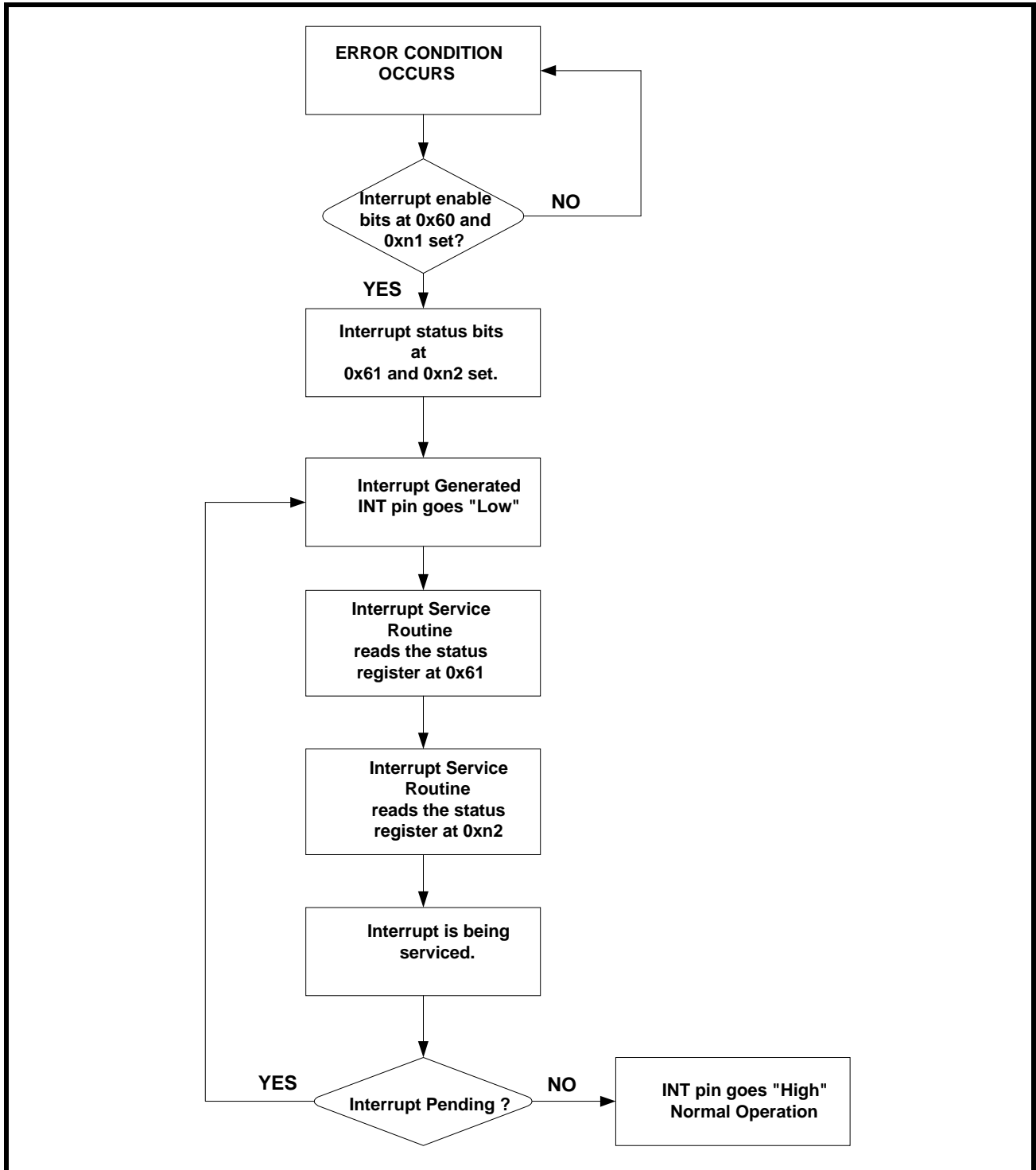


TABLE 14: SYNCHRONOUS TIMING SPECIFICATIONS

| SYMBOL | PARAMETER | MIN | MAX | UNITS |
|----------------|--|-----|-----|----------------|
| t ₀ | Valid Address to \overline{CS} Falling Edge | 0 | - | ns |
| t ₁ | \overline{CS} Falling Edge to \overline{RD} Assert | 0 | - | ns |
| t ₂ | \overline{RD} Assert to \overline{RDY} Assert | - | 35 | ns, see note 1 |
| NA | \overline{RD} Pulse Width (t ₂) | 40 | - | ns |
| t ₃ | \overline{CS} Falling Edge to \overline{WR} Assert | 0 | - | ns |
| t ₄ | \overline{WR} Assert to \overline{RDY} Assert | - | 35 | ns, see note 1 |
| NA | \overline{WR} Pulse Width (t ₄) | 40 | - | ns |
| | PCLK Period | 15 | | ns |
| | PCLK Duty Cycle | | | |
| | PCLK "High/Low" time | | | |

NOTE: 1. This timing parameter is based on the frequency of the synchronous clock (PCLK). To determine the access time, use the following formula: $(PCLK_{period} * 2) + 5ns$

FIGURE 38. INTERRUPT PROCESS



7.2.1 Hardware Reset:

The hardware reset is initiated by pulling the $\overline{\text{RESET}}$ pin “Low” for a minimum of 5 μs . After the $\overline{\text{RESET}}$ pin is released, the register values are put in default states.

TABLE 15: REGISTER MAP AND BIT NAMES

| ADDRESS (HEX) | PARAMETER NAME | DATA BITS | | | | | | | |
|---------------|-------------------------------|---------------------|---|---------|---------|---------|---------|---------|---------|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x00 | APS/Redundancy #1 | Reserved | | TxON_5 | TxON_4 | TxON_3 | TxON_2 | TxON_1 | TxON_0 |
| 0x08 | APS/ Redundancy #2 | Reserved | | RxON_5 | RxON_4 | RxON_3 | RxON_2 | RxON_1 | RxON_0 |
| 0x60 | Interrupt Enable (read/write) | Reserved | | INTEN_5 | INTEN_4 | INTEN_3 | INTEN_2 | INTEN_1 | INTEN_0 |
| 0x61 | Interrupt Status (read only) | Reserved | | INTST_5 | INTST_4 | INTST_3 | INTST_2 | INTST_1 | INTST_0 |
| 0x62 - 0x6D | | Reserved | | | | | | | |
| 0x6E | Chip_id (read only) | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 0x6F | Chip_revision_id (read only) | Chip version number | | | | | | | |

TABLE 16: REGISTER MAP DESCRIPTION - GLOBAL

| ADDRESS (HEX) | TYPE | REGISTER NAME | SYMBOL | DESCRIPTION | DEFAULT VALUE | | | | | | | | | | | | | | | |
|---------------|----------|--------------------|--------------|--|---------------|-----|--------------------|---|---|-----|---|---|-----|---|---|-----|---|---|----|---|
| 0x00 | R/W | APS # 1 | TxON_n | Table below shows the status of the transmitter based on the bit and pin setting. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Bit</th> <th>Pin</th> <th>Transmitter Status</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>OFF</td> </tr> <tr> <td>0</td> <td>1</td> <td>OFF</td> </tr> <tr> <td>1</td> <td>0</td> <td>OFF</td> </tr> <tr> <td>1</td> <td>1</td> <td>ON</td> </tr> </tbody> </table> | Bit | Pin | Transmitter Status | 0 | 0 | OFF | 0 | 1 | OFF | 1 | 0 | OFF | 1 | 1 | ON | 0 |
| Bit | Pin | Transmitter Status | | | | | | | | | | | | | | | | | | |
| 0 | 0 | OFF | | | | | | | | | | | | | | | | | | |
| 0 | 1 | OFF | | | | | | | | | | | | | | | | | | |
| 1 | 0 | OFF | | | | | | | | | | | | | | | | | | |
| 1 | 1 | ON | | | | | | | | | | | | | | | | | | |
| 0x08 | R/W | APS # 2 | RxON_n | Set this bit to turn on individual Receiver. | 0 | | | | | | | | | | | | | | | |
| 0x60 | R/W | Interrupt Enable | INTEN_n | Set this bit to enable the interrupts on per channel basis. | 0 | | | | | | | | | | | | | | | |
| 0x61 | ROR | Interrupt Status | INTST_n | Bits are set when an interrupt occurs.The respective source level interrupt status registers are read to determine the cause of interrupt. | 0 | | | | | | | | | | | | | | | |
| 0x62 - 0x6D | Reserved | | | | | | | | | | | | | | | | | | | |
| 0x6E | R | Device _ id | Chip_id | This read only register contains device id. | 01110101 | | | | | | | | | | | | | | | |
| 0x6F | R | Version Number | Chip_version | This read only register contains chip version number | | | | | | | | | | | | | | | | |

TABLE 17: REGISTER MAP AND BIT NAMES - CHANNEL N REGISTERS (N = 0,1,2,3,4,5)

| ADDRESS (HEX) | PARAMETER NAME | DATA BITS | | | | | | | |
|--|-------------------------------------|-----------|---|-------------------|----------------|--------|----------|--------------|---------|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x01 (ch 0) 0x11 (ch 1) 0x21 (ch 2) 0x31 (ch 3) 0x41 (ch 4) 0x51 (ch 5) | Interrupt Enable (read/write) | Reserved | | PRBSER CNTIE_n | PRBSERI E_n | FLIE_n | RLOLIE_n | RLOSIE_ n | DMOIE_n |
| 0x02 (ch 0) 0x12 (ch 1) 0x22 (ch 2) 0x32 (ch 3) 0x42 (ch 4) 0x52 (ch 5) | Interrupt Status (reset on read) | Reserved | | PRBSER CNTIS_n | PRBSERI S_n | FLIS_n | RLOLIS_n | RLOIS_ n | DMOIS_n |

TABLE 17: REGISTER MAP AND BIT NAMES - CHANNEL N REGISTERS (N = 0,1,2,3,4,5)

| ADDRESS (Hex) | PARAMETER NAME | DATA BITS | | | | | | | |
|--|---|-----------|-------------|-----------|-----------|-------------|----------|----------------|---------|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x03 (ch 0) 0x13 (ch 1) 0x23 (ch 2) 0x33 (ch 3) 0x43 (ch 4) 0x53 (ch 5) | Alarm Status (read only) | Reserved | PRBSLS_n | DLOS_n | ALOS_n | FL_n | RLOL_n | RLOS_n | DMO_n |
| 0x04 (ch 0) 0x14 (ch 1) 0x24 (ch 2) 0x34 (ch 3) 0x44 (ch 4) 0x54 (ch 5) | Transmit Control (read/write) | Reserved | | TxMON_n | INSPRBS_n | Reserved | TAOS_n | TxCLKINV_n | TxLEV_n |
| 0x05 (ch 0) 0x15 (ch 1) 0x25 (ch 2) 0x35 (ch 3) 0x45 (ch 4) 0x55 (ch 5) | Receive Control (read/write) | Reserved | | DLOSDIS_n | ALOSDIS_n | RxCLKIN_V_n | LOSMUT_n | RxMON_n | REQEN_n |
| 0x06 (ch 0) 0x16 (ch 1) 0x26 (ch 2) 0x36 (ch 3) 0x46 (ch 4) 0x56 (ch 5) | Block Control (read/write) | Reserved | CLKOUTE_N_n | PRBSEN_0 | RLB_n | LLB_n | E3_n | STS1/ DS3_n | SR/DR_n |
| 0x07 (ch 0) 0x17 (ch 1) 0x27 (ch 2) 0x37 (ch 3) 0x47 (ch 4) 0x57 (ch 5) | Jitter Attenuator Control (read/write) | Reserved | | | DFLCK_n | PNTRST_n | JA1_n | JATx/Rx_n | JA0_n |
| 0x0A (ch 0) 0x1A (ch 1) 0x2A (ch 2) 0x3A (ch 3) 0x4A (ch 4) 0x5A (ch 5) | PRBS Error Count Reg. MSB | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 |
| 0x0B (ch 0) 0x1B (ch 1) 0x2B (ch 2) 0x3B (ch 3) 0x4B (ch 4) 0x5B (ch 5) | PRBS Error Count Reg. LSB | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x0C (ch 0) 0x1C (ch 1) 0x2C (ch 2) 0x3C (ch 3) 0x4C (ch 4) 0x5C (ch 5) | PRBS Error Count Holding Register | | | | | | | | |

TABLE 18: REGISTER MAP DESCRIPTION - CHANNEL N

| ADDRESS (Hex) | TYPE | REGISTER NAME | BIT# | SYMBOL | DESCRIPTION | DEFAULT VALUE |
|--|---------------|---------------------------------|-------|---------------|---|---------------|
| 0x01 (ch 0) 0x11 (ch 1) 0x21 (ch 2) 0x31 (ch 3) 0x41 (ch 4) 0x51 (ch 5) | R/W | Interrupt Enable (source level) | D0 | DMOIE_n | If the Driver Monitor (connected to the output of the channel) detects the absence of pulses for 128 consecutive cycles, it will set the interrupt flag if this bit has been set. | 0 |
| | | | D1 | RLOSIE_n | This flag will allow a loss of receive signal(for that channel) to send an interrupt to the Host when this bit is set. | 0 |
| | | | D2 | RLOLIE_n | This flag will allow a loss of lock condition to send an interrupt to the Host when this bit is set. | 0 |
| | | | D3 | FLIE_n | Set this bit to enable the interrupt when the FIFO Limit of the Jitter Attenuator is within 2 bits of overflow/underflow condition. NOTE: This bit field is ignored when the Jitter Attenuator is disabled. | 0 |
| | | | D4 | PRBSERIE_n | Set this bit to enable the interrupt when the PRBS error is detected. | 0 |
| | | | D5 | PRBSERCNTIE_n | Set this bit to enable the interrupt when the PRBS error count register saturates. | 0 |
| | | | D6-D7 | Reserved | | |
| 0x02 (ch 0) 0x12 (ch 1) 0x22 (ch 2) 0x32 (ch 3) 0x42 (ch 4) 0x52 (ch 5) | Reset on Read | Interrupt Status (source level) | D0 | DMOIS_n | If the Drive monitor circuit detects the absence of pulses for 128 consecutive cycles, it will set this interrupt status flag (if enabled) This bit is set on a change of state of the DMO circuit. | 0 |
| | | | D1 | RLOISIS_n | This flag will indicate a change of "loss of Receive signal" to the Host when this bit is set. | 0 |
| | | | D2 | RLOLIS_n | This flag will allow a change in the loss of lock condition to send an interrupt to the Host when this bit is enabled.Loss of lock is defined as a difference of greater than 0.5% between the recovered clock and the channel's reference clock. Any change (return to lock) will trigger the interrupt status flag again. | 0 |
| | | | D3 | FLIS_n | This bit will generate an interrupt if the jitter attenuator FIFO reaches (or leaves) a limit condition. This limit condition is defined as the FIFO being within two counts of full or empty. | 0 |
| | | | D4 | PRBSERIS_n | This bit is set when the PRBS error occurs. | 0 |
| | | | D5 | PRBSERCNTIS_n | This bit is set when the PRBS error count register saturates. | 0 |
| | | | D7-D6 | Reserved | | |

TABLE 18: REGISTER MAP DESCRIPTION - CHANNEL N

| ADDRESS (HEX) | TYPE | REGISTER NAME | BIT# | SYMBOL | DESCRIPTION | DEFAULT VALUE |
|--|-----------|---------------|------|----------|---|---------------|
| 0x03 (ch 0) 0x13 (ch 1) 0x23 (ch 2) 0x33 (ch 3) 0x43 (ch 4) 0x53 (ch 5) | Read Only | Alarm Status | D0 | DMO_n | This bit is set when no transitions on the TTIP/TRING have been detected for 128 ± 32 TxCLK periods. It will be cleared when pulses resume. | 0 |
| | | | D1 | RLOS_n | This bit is set every time the receiver declares an LOS condition. It will be cleared when the signal is recognized again. | 0 |
| | | | D2 | RLOL_n | This bit is set when the detected clock is greater than 0.5% oof frequency from the reference clock. By definition, the two frequencies are "not in lock" with each other. It will be cleared when they are "in lock" again.. | 0 |
| | | | D3 | FL_n | This bit is set when the FIFO reaches its limit. The limit is defined to be within two bits of either underflow or overflow. | 0 |
| | | | D4 | ALOS_n | This bit is set when the receiver declares that the Analog signal has degraded to the point that the signal has been lost. | 0 |
| | | | D5 | DLOS_n | This bit is set when no input signals have been received for 10 to 255 bit times in E3 or 100 to 250 bit times in DS3 or STS-1 modes. This is a complete lack of incoming pulses rather than signal attenuation (ALOS). It should be noted that this time period is built into the Analog detector for E3 mode. Even though DS3/STS-1 mode does not require analog detection level, but it is provided and could help to determine the "quality of the line" for DS/STS-1 applications. | 0 |
| | | | D6 | PRBSLS_n | This bit is set when the PRBS detector has been enabled and it is not in sync with the incoming data pattern. Once the sync is achieved, it will be cleared. | 0 |
| | | | D7 | Reserved | | |

TABLE 18: REGISTER MAP DESCRIPTION - CHANNEL N

| ADDRESS (HEX) | TYPE | REGISTER NAME | BIT# | SYMBOL | DESCRIPTION | DEFAULT VALUE | | |
|--|------|------------------|-------|------------|--|---------------|--|--|
| 0x04 (ch 0) 0x14 (ch 1) 0x24 (ch 2) 0x34 (ch 3) 0x44 (ch 4) 0x54 (ch 5) | R/W | Transmit Control | D0 | TxLEV_n | This bit should be set when the transmitter is driving a line greater than 225 feet in the DS3 or STS-1 modes. It is not active in E3 mode. | 0 | | |
| | | | D1 | TxCLKINV_n | Set this bit to sample the data on TPOS/TNEG pins on the rising edge of TxCLK. Default is to sample on the falling edge of TxCLK. | 0 | | |
| | | | D2 | TAOS_n | This bit should be set to transmit a continuous "all ones" data pattern. Timing will come from TxCLK if available otherwise from channel reference clock. | 0 | | |
| | | | D3 | Reserved | | | | |
| | | | D4 | INSPRBS_n | This bit causes a single bit error to be inserted in the transmitted PRBS pattern if the PRBS generator/detector has been enabled. | 0 | | |
| | | | D5 | TxMON_n | When set, this bit enables the DMO circuit to monitor its own channel's transmit driver. Otherwise, it uses the MTIP/MRING pins to monitor another channel or device. | 0 | | |
| | | | D7-D6 | Reserved | | | | |
| 0x05 (ch 0) 0x15 (ch 1) 0x25 (ch 2) 0x35 (ch 3) 0x45 (ch 4) 0x55 (ch 5) | R/W | Receive Control | D0 | REQEN_n | This bit enables the Receiver Equalizer. When set, the equalizer boosts the high frequency components of the signal to make up for cable losses. NOTE: See section 5.01 for detailed description. | 0 | | |
| | | | D1 | RxMON_n | Set this bit to place the Receiver in the monitoring mode. In this mode, it can process signals (at RTIP/RRING) with 20dB of flat loss. This mode allows the channel to act as monitor of a line without loading the circuit. | 0 | | |
| | | | D2 | LOSMUT_n | When set, the data on RPOS/RNEG is forced to zero when LOS occurs. Thus any residual noise on the line is not output as spurious data. NOTE: If this bit has been set, it will remain set even after the LOS condition is cleared. | 0 | | |
| | | | D3 | RxCLKINV_n | When this bit is set, RPOS and RNEG will change on the falling edge of RCLK. Default is for the data to change on the rising edge of RCLK and be sampled by the terminal equipment on the falling edge of RCLK. | 0 | | |
| | | | D4 | ALOSDIS_n | This bit is set to disable the ALOS detector. This flag and the DLOSDIS are normally used in diagnostic mode. Normal operation of DS3 and STS-1 would have ALOS disabled. | 0 | | |
| | | | D5 | DLOSDIS_n | This bit disables the digital LOS detector. This would normally be disabled in E3 mode as E3 is a function of the level of the input. | 0 | | |
| | | | D7-D6 | Reserved | | | | |

TABLE 18: REGISTER MAP DESCRIPTION - CHANNEL N

| ADDRESS (HEX) | TYPE | REGISTER NAME | BIT# | SYMBOL | DESCRIPTION | DEFAULT VALUE | | | | | | | | | | | | | | | |
|--|-------------|--|-------|---------------------------|---|---------------|-------|---------------|---|---|------------------|---|---|--------------|---|---|--------|---|---|---------|---|
| 0x06 (ch 0) 0x16 (ch 1) 0x26 (ch 2) 0x36 (ch 3) 0x46 (ch 4) 0x56 (ch 5) | R/W | Block Control | D0 | SR/ \overline{DR}_n | Setting this bit configures the Receiver and Transmitter in Single-Rail (NRZ) mode. NOTE: See section 4.0 for detailed description. | 0 | | | | | | | | | | | | | | | |
| | | | D1 | STS-1/ $\overline{DS3}_n$ | Setting this bit configures the channel into STS-1 mode. NOTE: This bit field is ignored if the channel is configured to operate in E3 mode. | 0 | | | | | | | | | | | | | | | |
| | | | D2 | E3_n | Setting this bit configures the channel in E3 mode. | 0 | | | | | | | | | | | | | | | |
| | | | D3 | LLB_n | Setting this bit configures the channel in Local Loopback mode. | 0 | | | | | | | | | | | | | | | |
| | | | D4 | RLB_n | This bit along with LLB_n determine the diagnostic mode as shown in the table below. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>RLB_n</th> <th>LLB_n</th> <th>Loopback Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Normal Operation</td> </tr> <tr> <td>0</td> <td>1</td> <td>Analog Local</td> </tr> <tr> <td>1</td> <td>0</td> <td>Remote</td> </tr> <tr> <td>1</td> <td>1</td> <td>Digital</td> </tr> </tbody> </table> | RLB_n | LLB_n | Loopback Mode | 0 | 0 | Normal Operation | 0 | 1 | Analog Local | 1 | 0 | Remote | 1 | 1 | Digital | 0 |
| | | | RLB_n | LLB_n | Loopback Mode | | | | | | | | | | | | | | | | |
| | | | 0 | 0 | Normal Operation | | | | | | | | | | | | | | | | |
| | | | 0 | 1 | Analog Local | | | | | | | | | | | | | | | | |
| 1 | 0 | Remote | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | Digital | | | | | | | | | | | | | | | | | | | |
| D5 | PRBSEN_n | Setting this bit enables the PRBS generator/detector. When in E3 mode, an unframed $2^{23}-1$ pattern is used. For DS3 and STS-1, unframed $2^{15}-1$ pattern is used. This mode of operation will use TCLK for timing. One should insure that a stable frequency is provided. Looping this signal back to its own receive channel and using RCLK to generate TCLK will cause an unstable condition and should be avoided. | 0 | | | | | | | | | | | | | | | | | | |
| D6 | CLKOUTE_N_n | Set this bit to enable the CLKOUTs on a per channel basis. The frequency of the output clock is dependent on the configuration of the channels, either E3, DS3 or STS-1. | 0 | | | | | | | | | | | | | | | | | | |
| D7 | Reserved | | | | | | | | | | | | | | | | | | | | |

TABLE 18: REGISTER MAP DESCRIPTION - CHANNEL N

| ADDRESS (HEX) | TYPE | REGISTER NAME | BIT# | SYMBOL | DESCRIPTION | DEFAULT VALUE | | | | | | | | | | | | | | | |
|--|-----------|---|-------|--------|--|---------------|-------|------|---|---|-------------|---|---|-------------|---|---|---------------------------|---|---|---------------------------|---|
| 0x07 (ch 0) 0x17 (ch 1) 0x27 (ch 2) 0x37 (ch 3) 0x47 (ch 4) 0x57 (ch 5) | R/W | Jitter Attenuator | D0 | JA0_n | This bit along with JA1_n bit configures the Jitter Attenuator as shown in the table below. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>JA0_n</th> <th>JA1_n</th> <th>Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>16 bit FIFO</td> </tr> <tr> <td>0</td> <td>1</td> <td>32 bit FIFO</td> </tr> <tr> <td>1</td> <td>0</td> <td>Disable Jitter Attenuator</td> </tr> <tr> <td>1</td> <td>1</td> <td>Disable Jitter Attenuator</td> </tr> </tbody> </table> | JA0_n | JA1_n | Mode | 0 | 0 | 16 bit FIFO | 0 | 1 | 32 bit FIFO | 1 | 0 | Disable Jitter Attenuator | 1 | 1 | Disable Jitter Attenuator | 0 |
| | | | JA0_n | JA1_n | Mode | | | | | | | | | | | | | | | | |
| | | | 0 | 0 | 16 bit FIFO | | | | | | | | | | | | | | | | |
| | | | 0 | 1 | 32 bit FIFO | | | | | | | | | | | | | | | | |
| | | | 1 | 0 | Disable Jitter Attenuator | | | | | | | | | | | | | | | | |
| | | | 1 | 1 | Disable Jitter Attenuator | | | | | | | | | | | | | | | | |
| D1 | JATx/Rx_n | Setting this bit selects the Jitter Attenuator in the Transmit Path. A "0" selects in the Receive Path. | 0 | | | | | | | | | | | | | | | | | | |
| D2 | JA1_n | This bit along with the JA0_n configures the Jitter Attenuator as shown in the table. | 0 | | | | | | | | | | | | | | | | | | |
| D3 | PNTRST_n | Setting this bit resets the FIFO pointers to their initial state and flushes the FIFO. All existing FIFO data is lost. | 0 | | | | | | | | | | | | | | | | | | |
| D4 | DFLCK_n | Set this bit to "1" to disable fast locking of the PLL. This helps to reduce the time for the PLL to lock to incoming frequency when the Jitter Attenuator switches to narrow band. | 0 | | | | | | | | | | | | | | | | | | |
| D7-D5 | Reserved | | | | | | | | | | | | | | | | | | | | |

8.0 ELECTRICAL CHARACTERISTICS

TABLE 19: ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | MIN | MAX | UNITS | COMMENTS |
|-------------------|-------------------------------|------|-----|-------|---|
| V _{DD} | Supply Voltage | -0.5 | 6.0 | V | Note 1 |
| V _{IN} | Input Voltage at any Pin | -0.5 | 5.5 | V | Note 1 |
| I _{IN} | Input current at any pin | | 100 | mA | Note 1 |
| S _{TEMP} | Storage Temperature | -65 | 150 | °C | Note 1 |
| A _{TEMP} | Ambient Operating Temperature | -40 | 85 | °C | linear airflow 0 ft./min |
| Theta JA | Thermal Resistance | | 23 | °C/W | linear air flow 0ft/min (See Note 3 below) |
| M _{LEVL} | Exposure to Moisture | 4 | | level | EIA/JEDEC JESD22-A112-A |
| ESD | ESD Rating | 2000 | | V | Note 2 |

NOTES:

1. Exposure to or operating near the Min or Max values for extended period may cause permanent failure and impair reliability of the device.
2. ESD testing method is per MIL-STD-883D,M-3015.7
3. With Linear Air flow of 200 ft/min, reduce Theta JA by 20%, Theta JC is unchanged.

TABLE 20: DC ELECTRICAL CHARACTERISTICS:

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNITS |
|------------------|--|-------|------|-------|-------|
| DV _{DD} | Digital Supply Voltage | 3.135 | 3.3 | 3.465 | V |
| AV _{DD} | Analog Supply Voltage | 3.135 | 3.3 | 3.465 | V |
| I _{CC} | Supply current requirements | | 725 | 850 | mA |
| P _{DD} | Power Dissipation | | 2.64 | 2.93 | W |
| V _{IL} | Input Low Voltage | | | 0.8 | V |
| V _{IH} | Input High Voltage | 2.0 | | 5.5 | V |
| V _{OL} | Output Low Voltage, I _{OUT} = - 4mA | | | 0.4 | V |
| V _{OH} | Output High Voltage, I _{OUT} = 4 mA | 2.4 | | | V |
| I _L | Input Leakage Current ¹ | | | ±10 | µA |
| C _I | Input Capacitance | | | 10 | pF |
| C _L | Load Capacitance | | | 10 | pF |

NOTES:

1. Not applicable for pins with pull-up or pull-down resistors.
2. The Digital inputs are TTL 5V compliant.

APPENDIX - A**TABLE 21: TRANSFORMER RECOMMENDATIONS**

| PARAMETER | VALUE |
|--------------------|-------------|
| Turns Ratio | 1:1 |
| Primary Inductance | 40 μ H |
| Isolation Voltage | 1500 Vrms |
| Leakage Inductance | 0.6 μ H |

TABLE 22: TRANSFORMER DETAILS

| PART NUMBER | VENDOR | INSULATION | PACKAGE TYPE |
|-------------|------------|------------|-----------------|
| PE-68629 | PULSE | 3000 V | Large Thru-hole |
| PE-65966 | PULSE | 1500 V | Small Thru-hole |
| PE-65967 | PULSE | 1500 V | SMT |
| T 3001 | PULSE | 1500 V | SMT |
| TG01-0406NS | HALO | 1500 V | SMT |
| TTI 7601-SM | TransPower | 1500 V | SMT |

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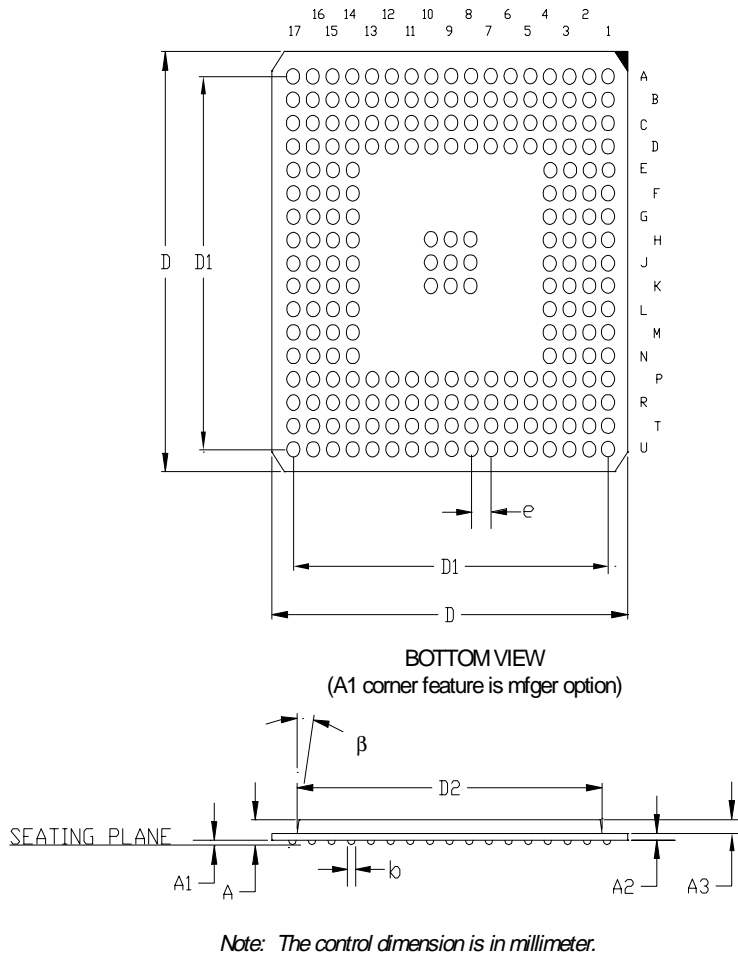
Email: info@trans-power.com

Website: <http://www.trans-power.com>

ORDERING INFORMATION

| PART NUMBER | PACKAGE | OPERATING TEMPERATURE RANGE |
|-------------|---------------------------|-----------------------------|
| XRT75R06IB | 217 Lead BGA (23 x 23 mm) | - 40°C to + 85°C |

PACKAGE DIMENSIONS - 23 X 23 MM 217 LEAD BGA PACKAGE



| SYMBOL | INCHES | | MILLIMETERS | |
|--------|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.067 | 0.098 | 1.70 | 2.50 |
| A1 | 0.016 | 0.028 | 0.40 | 0.70 |
| A2 | 0.012 | 0.024 | 0.30 | 0.60 |
| A3 | 0.039 | 0.047 | 1.00 | 1.20 |
| D | 0.898 | 0.913 | 22.80 | 23.20 |
| D1 | 0.800 BSC | | 20.32 BSC | |
| D2 | 0.780 | 0.795 | 19.80 | 20.20 |
| b | 0.024 | 0.035 | 0.60 | 0.90 |
| e | 0.050 BSC | | 1.27 BSC | |
| β | 10° | 20° | 10° | 20° |

REVISIONS

| REVISION | DATE | COMMENTS |
|-----------------|-------------|--|
| P1.0.0 | 06/11/04 | First release of the preliminary datasheet. |
| P1.0.1 | 07/15/04 | Second release of the preliminary datasheet. |
| 1.0.0 | 12/14/04 | Release to production. Entered power dissipation and power supply current in electrical. |

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