Z84C30

CMOS Z80® CTC COUNTER/TIMER CIRCUIT

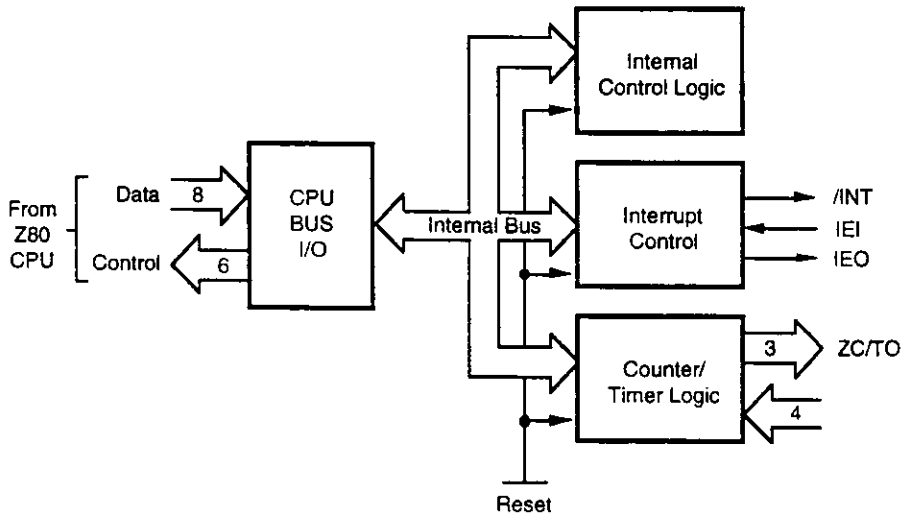
GENERAL DESCRIPTION

The Z84C30 CTC, hereinafter referred to as the CTC, is a four-channel counter/timer that can be programmed by system software for a broad range of counting and timing applications. The four independently programmable channels of the CTC satisfy common microprocessor system requirements for event counting, interrupt and interval timing, and general clock rate generation.

System design is simplified as the CTC connects directly to both the Z80 CPU and the Z80 SIO with no additional logic. In larger systems, address decoders and buffers may be required.

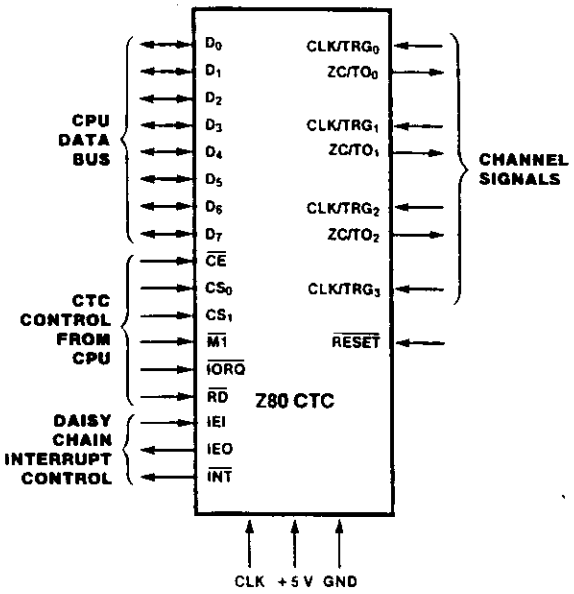
Programming the CTC is straightforward. Each channel is programmed with two bytes; a third is necessary when interrupts are enabled. Once started, the CTC counts down, automatically reloads its time-constant, and resumes counting. Software timing loops are completely eliminated. Interrupt processing is simplified as only one vector need be specified. The CTC internally generates a unique vector for each channel.

The CTC requires a single +5V power supply and the standard Z80 single-phase system clock. It is offered in 28-pin DIP, 44-pin PLCC, and 44-pin QFP packages. Note that the QFP package is only available for CMOS versions.

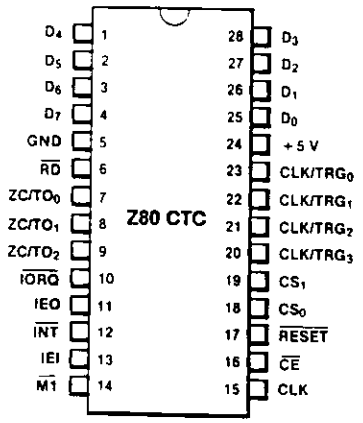


Functional Block Diagram

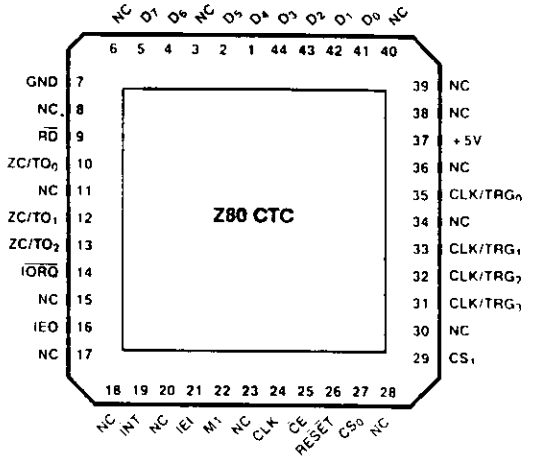
GENERAL DESCRIPTION (Continued)



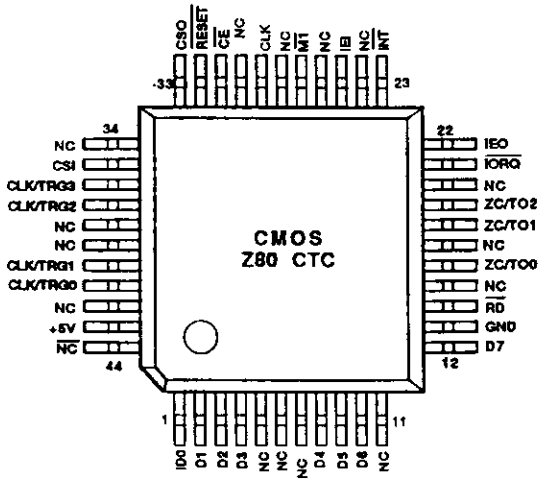
Pin Functions



28-Lead DIP Pin Assignments



44-Lead PLCC Pin Assignments



44-Lead QFP Pin Assignments (CMOS Device Only)

ABSOLUTE MAXIMUM RATINGS

Voltages on V_{CC} with respect to V_{SS} . . . . . – 0.3V to + 7.0V
Voltages on all inputs with respect to V_{SS} . . . . . – 0.3V to V_{CC} + 0.3V
Storage Temperature . . . . . – 65°C to + 150°C

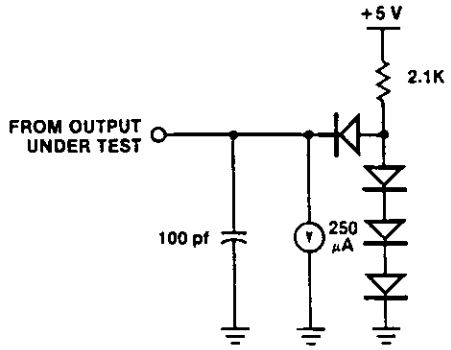
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above these indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics below apply for the following test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin. Available operating temperature range is:

- **S = 0°C to +70°C, V_{CC} Range**
  CMOS: +4.50V ≤ V_{CC} ≤ +5.50V
  *16 MHz +4.75V ≤ V_{CC} ≤ +5.25V
- E = –40°C to 100°C

The Ordering Information section lists package temperature ranges and product numbers. Refer to the Literature List for additional documentation. Package drawings are in the Package Information section.



DC CHARACTERISTICS (Z84C30/CMOS Z80 CTC)

V_{CC}=5.0V ± 10%, unless otherwise specified

Symbol	Parameter	Min	Max	Unit	Condition
V_{ILC}	Clock Input Low Voltage	-0.3	+0.45	V	
V_{IHC}	Clock Input High Voltage	V_{CC}-0.6	V_{CC}+0.3	V	
V_{IL}	Input High Voltage	2.2	V_{CC}	V	
V_{IH}	Input Low Voltage	-0.3	0.8	V	
V_{OL}	Output Low Voltage		0.4	V	I_{LO}=2.0mA
V_{OH1}	Output High Voltage	2.4		V	I_{OH}=-1.6mA
V_{OH2}	Output High Voltage	V_{CC}-0.8		V	I_{OH}=-250µA
I_{LI}	Input Leakage Current	-10	10	µA	V_{IN}=0.4V to V_{CC}
I_{LO}	3-state Output Leakage Current in Float	-10	10	µA	V_{OUT}=0.4V to V_{CC}
I_{CC1}	Power Supply Current - 4MHz		7 [1]	mA	V_{CC}=5V
	- 6MHz		8 [1]	mA	CLK=4,6,8,10,16 MHz
	- 8MHz		10 [1]	mA	V_{IH}=V_{CC}-0.2V
	- 10MHz		12 [1]	mA	V_{IL}=0.2V
	- 16 MHz*		TBD	mA	
I_{CC2}	Standby Supply Current		10	µA	V_{CC}=5V CLK=(0) V_{IH}=V_{CC}-0.2V V_{IL}=0.2V
I_{OHD}	Darlington Drive Current	-1.5	-5.0	mA	V_{OH}=1.5V REXT=1.1K ohm

Note: [1] Measurements made with outputs floating.

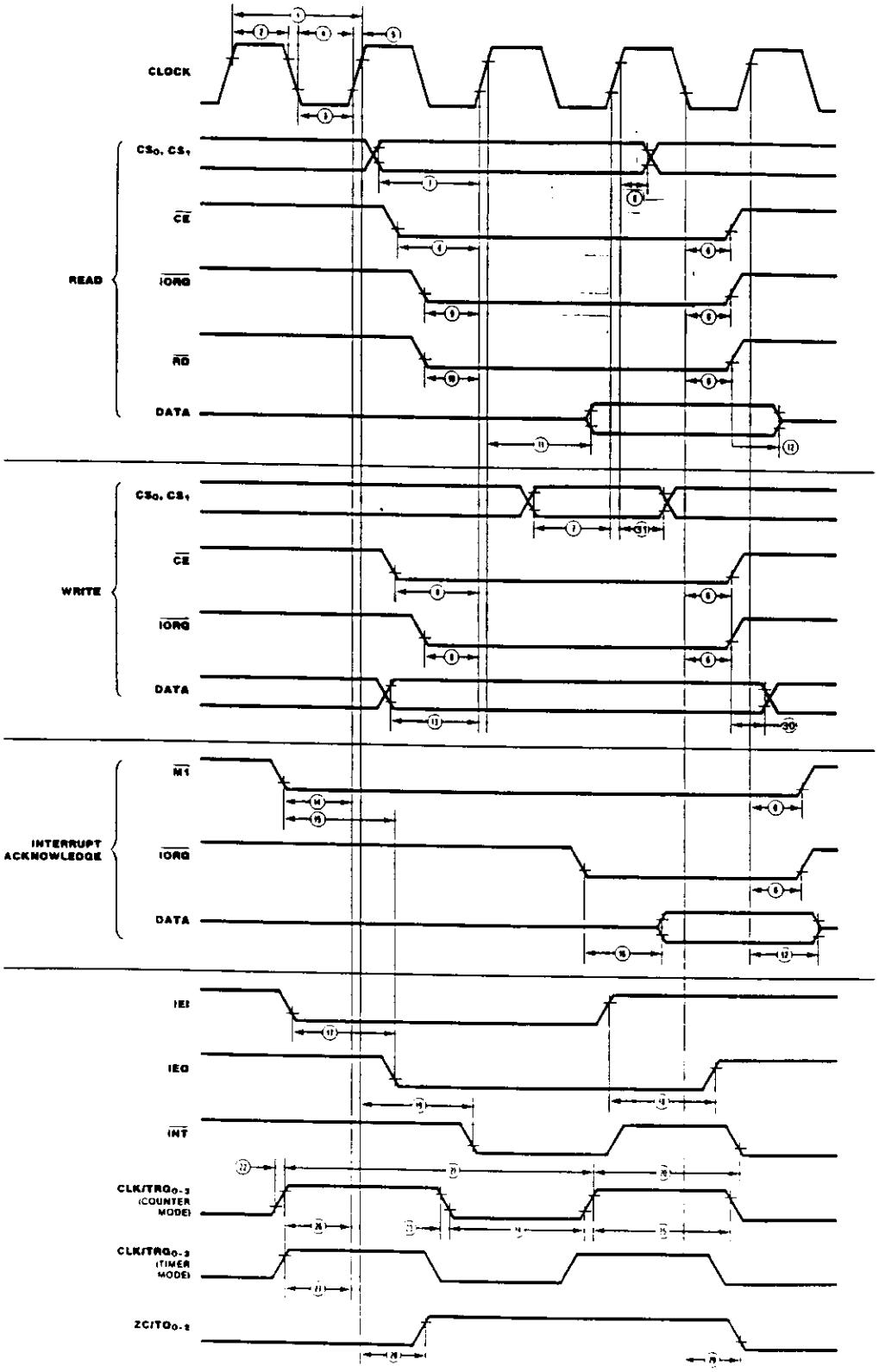
CAPACITANCE

Symbol	Parameter	Max	Unit
CLK	Clock Capacitance	10	pf
C_{IN}	Input Capacitance	10	pf
C_{OUT}	Output Capacitance	15	pf

T_A = 25°C, f = 1 MHz

Unmeasured pins returned to ground.

* V_{CC} limit is +, -5% for 16 MHz device.


CLOCK
READ
CS0, CS1
CE
IORQ
RD
DATA
WRITE
CS0, CS1
CE
IORQ
DATA
INTERRUPT ACKNOWLEDGE
M1
IORQ
DATA
IEI
IEO
INT
CLK/TRG0-3 (COUNTER MODE)
CLK/TRG0-3 (TIMER MODE)
ZC/TO0-2

No	Symbol	Parameter	Z84C3004 * Min	Z84C3004 * Max	Z84C3006 Min	Z84C3006 Max	Z84C3008 Min	Z84C3008 Max	Z84C3010 Min	Z84C3010 Max	Z84C3016* Min (ns)	Z84C3016* Max (ns)	Note
1	TcC	Clock Cycle Time	250	[1]	162	[1]	125	[1]	100	[1]	62	DC	
2	TwCh	Clock pulse Width (High)	110	DC	65	DC	55	DC	42	DC	26	DC	
3	TwCl	Clock pulse Width (Low)	110	DC	65	DC	55	DC	42	DC	26	DC	
4	TfC	Clock Fall Time		30		20		10		10		5	
5	TrC	Clock Rise Time		30		20		10		10		5	
6	Th	All Hold Times	0		0		0		0		0		
7	TsCS(C)	/CS to Clock Rise Setup Time	160		100		50		35		25		
8	TsCE(C)	/CE to Clock Rise Setup Time	150		100		50		35		25		
9	TsIO(C)	/IORQ to Clock Rise Setup Time	115		70		40		35		25		
10	TsRD(C)	/RD Fall to Clock Rise Setup Time	115		70		40		35		25		
11	TdC(DO)	Clock Rise to Data Out Float Delay		200		130		90		90		55	[2]
12	TdRIr (DOz)	/RD, /IORQ rising to Data Outime Float Delay		50		40		40		40		25	
13	TsDI (C)	Data In to Clock rising set-up	50		40		30		30		15		
14	TsM1(C)	/M1 to Clock Rise Setup Time	90		70		50		40		25		
15	TdM1(IEO)	/M1 Fall to IEO Fall Delay (Interrupt Immediately Preceding /M1 Fall)		190		130		90		70		45	[3]
16	TdIO(DIO)	/IORQ Fall to Data Out Delay (/INTACK Cycle)		160		110		80		80		80	[2,6]
17	TdIEI(IEOf)	IEI Fall to IEO Fall Delay		130		100		70		70		70	[3]
18	TdIEI(IEOr)	IEI Rise to IEO Rise Delay (After ED Decode)		160		110		70		70		70	[3]
19	TdC(INT)	Clock Rise to /INT Fall Delay	(TcC+140)		(TcC+120)		(TcC+100)		(TcC+80)			TcC+30	[4]
20	TdCLK(INT)	CLK/TRG Rise to /INT Fall Delay TsCTR(C) Satisfied	(19)+(26)		(19)+(26)		(19)+(26)		(19)+(26)			(19)+(26)	[5]
		TsCTR(C) Not Satisfied	(1)+(19)+(26)		(1)+(19)+(26)		(1)+(19)+(26)		(1)+(19)+(26)			(1)+(19)+(26)	[5]
21	TcCTR	CLK/TRG Cycle Time	(2TcC)		(2TcC)		(2TcC)		(2TcC)		(2TcC)		[5]
22	TrCTR	CLK/TRG Rise Time		50		40		30		30		15	
23	TfCTR	CLK/TRG Fall Time		50		40		30		30		15	
24	TwCTRh	CLK/TRG Width (Low)	200		120		90		90		25		
25	TwCTRl	CLK/TRG Width (High)	200		120		90		90		25		
26	TsCTR(Cs)	CLK/TRG Rise to Clock Rise Setup Time for Immediate Count	210		150		110		90		40		[5]
27	TsCTR(Ct)	CLK/TRG Rise to Clock Rise Setup Time for Enabling of Prescaler On Following Clock Rise	210		150		110		90		40		[4]

* 4 MHz Z84C30 is obsoleted and replaced by 6 MHz

* V_{cc} limit is +, -5% for 16 MHz device.

No	Symbol	Parameter	Z84C3004* Min	Z84C3004* Max	Z84C3006 Min	Z84C3006 Max	Z84C3008 Min	Z84C3008 Max	Z84C3010 Min	Z84C3010 Max	Z84C3016* Min (ns)	Z84C3016* Max (ns)	Note
28	TdC(ZC/TOr)	Clock Rise to ZC/TO Rise Delay		190		140		100		80		25	
29	TdC(ZC/TOf)	Clock Fall to ZC/TO Fall Delay		190		140		100		80		25	
30	ThRIr(D)	/CE, /IORQ Rise to Data Hold	20		20		10		10		10		
31	ThC(CS)	Clock Rise to /CS Hold	20		20		10		10		10		

* RESET must be active for a minimum of 3 clock cycles.
Units in Nanoseconds

Notes:
[1] TcC = TwCh + TwCl + TrC + TfC.
[2] Increasing delay by 10nS for each 50pF increase in loading, 200pF max for data lines, and 100pF for control lines.
[3] Increase delay by 2nS for each 10pF increase in loading, 100pF max.
[4] Timer mode.
[5] Counter mode.
[6] 2.5TcT > (N-2)TdIEI(IEOf) + TdM1(IEO) + TsIEI(IO) + TTL Buffer Delay, if any.

* 4 MHz Z84C30 is obsoleted and replaced by 6 MHz
* V_{cc} limit is +, -5% for 16 MHz device.

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