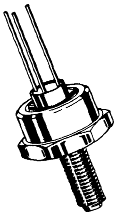
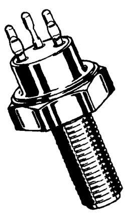
2N3924 (SILICON) thru 2N3927

NPN silicon annular RF power transistors, optimized for large-signal power-amplifier and driver applications to 300 MHz.



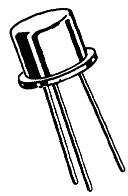
Collector electrically connected to case; stud electrically isolated from case

CASE 24
2N3925
(TO-102)



CASE 36
2N3926
2N3927
(TO-60)

Stud and case electrically connected to emitter



CASE 79
2N3924
(TO-39)

Collector connected to case

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

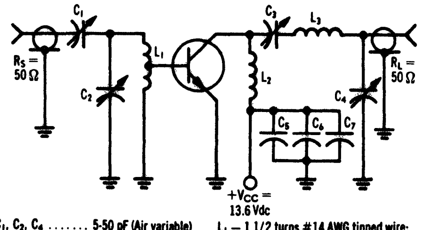
Rating	Symbol	2N3924	2N3925	2N3926	2N3927	Unit
Collector-Emitter Voltage	V_{CEO}	18	18	18	18	Vdc
Collector-Base Voltage	V_{CB}	36	36	36	36	Vdc
Emitter-Base Voltage	V_{EB}	4.0	4.0	4.0	4.0	Vdc
Collector Current	I_C	0.5	1.0	1.5	3.0	Adc
Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	7.0 40	10 57.1	11.6 66.3	23.2 132.5	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →				°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (1)	I_C = 200 mAdc	$BV_{CEO(sus)}$	18	-	-	Vdc
Collector-Base Breakdown Voltage	I_C = 0.25 mAdc, I_E = 0 — 2N3924 thru 2N3926	BV_{CBO}	36	-	-	Vdc
	I_C = 0.50 mAdc, I_E = 0 — 2N3927		36	-	-	
Emitter-Base Breakdown Voltage	I_E = 1.0 mAdc, I_C = 0 — 2N3924 thru 2N3926	BV_{EBO}	4.0	-	-	Vdc
	I_E = 2.0 mAdc, I_C = 0 — 2N3927		4.0	-	-	
Collector Cutoff Current	V_{CB} = 15 Vdc, I_E = 0 — 2N3924 thru 2N3926	I_{CBO}	-	-	0.1	mAdc
	2N3927				0.25	
	V_{CB} = 15 Vdc, I_E = 0, T_A = 150°C — 2N3924 thru 2N3926		-	-	5.0	
	2N3927		-	-	10	
DYNAMIC CHARACTERISTICS						
Current-Gain — Bandwidth Product	I_C = 100 mAdc, V_{CE} = 13.6 Vdc, f = 100 MHz — 2N3924 thru 2N3926	f_T	-	350	-	MHz
	I_C = 200 mAdc, V_{CE} = 13.6 Vdc, f = 100 MHz — 2N3927		-	350	-	
Output Capacitance	V_{CB} = 13.6 Vdc, I_E = 0, f = 100 kHz — 2N3924 thru 2N3926	C_{ob}	-	12.5	20	pF
	2N3927		-	25	45	
FUNCTIONAL TESTS 2N3924						
Power Input	Test Circuit Figure 1	P_{in}	-	-	1.0	Watt
Common-Emitter Amplifier Power Gain	V_{CE} = 13.6 Vdc, R_S = 50 ohms, R_L = 50 ohms, f = 175 MHz	G_{pe}	6.0	7.3	-	dB
Collector Efficiency	P_{out} = 4.0 Watts	η	70	-	-	%
2N3925						
Power Input	Test Circuit Figure 1	P_{in}	-	-	1.3	Watts
Common-Emitter Amplifier Power Gain	V_{CE} = 13.6 Vdc, R_S = 50 ohms, R_L = 50 ohms, f = 175 MHz	G_{pe}	5.84	6.5	-	dB
Collector Efficiency	P_{out} = 5.0 Watts	η	70	-	-	%
2N3926						
Power Input	Test Circuit Figure 1	P_{in}	-	-	2.0	Watts
Common-Emitter Amplifier Power Gain	V_{CE} = 13.6 Vdc, R_S = 50 ohms, R_L = 50 ohms, f = 175 MHz	G_{pe}	5.44	6.0	-	dB
Collector Efficiency	P_{out} = 7.0 Watts	η	70	-	-	%
2N3927						
Power Input	Test Circuit Figure 1	P_{in}	-	-	4.0	Watts
Common-Emitter Amplifier Power Gain	V_{CE} = 13.6 Vdc, R_S = 50 ohms, R_L = 50 ohms, f = 175 MHz	G_{pe}	4.77	5.0	-	dB
Collector Efficiency	P_{out} = 12 Watts	η	80	-	-	%

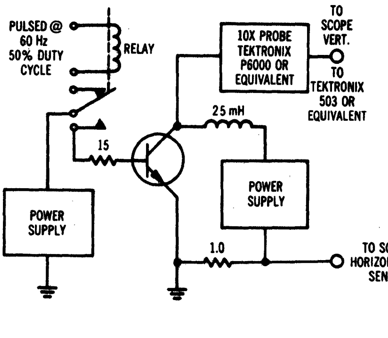
(1) Pulsed thru a 25-mH inductor (See Figure 2)

FIGURE 1 — 175 MHz TEST CIRCUIT



C_1, C_2, C_4 .... 5-50 pF (Air variable)
C_3 .... 7-100 pF (Air variable)
C_5 .... 470 pF (Disc ceramic)
C_6 .... 0.01 μF (Disc ceramic)
C_7 .... 0.001 μF (Disc ceramic)
L_1 — 1 1/2 turns #14 AWG tinned wire; 3/8" ID Air wound; winding length 3/16"; base tapped 1 turn from ground
L_2 — RFC
L_3 — 2 turns #14 AWG tinned wire; 1/4" ID Air wound; winding length 3/16"

FIGURE 2 — PULSE TEST CIRCUIT



CLASS C DESIGN DATA FOR V_{CE} = 13.6 Vdc, T_C = 25°C

(Emitter Grounded Directly to the Chassis — No Tuned-Emitter Techniques Used)

2N3924

FIGURE 3 — POWER OUTPUT vs FREQUENCY

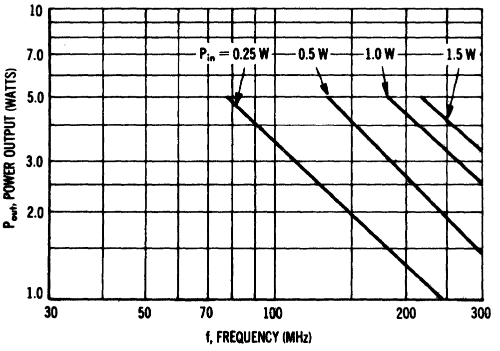


FIGURE 4 — POWER OUTPUT vs POWER INPUT

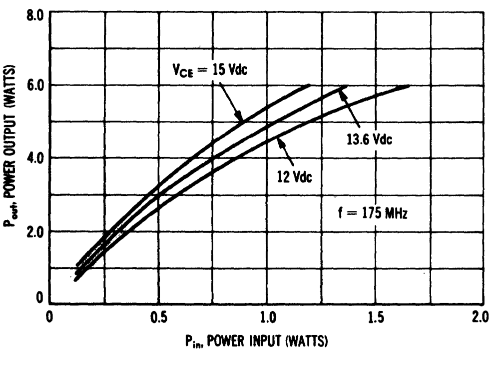


FIGURE 5 — PARALLEL EQUIVALENT INPUT RESISTANCE

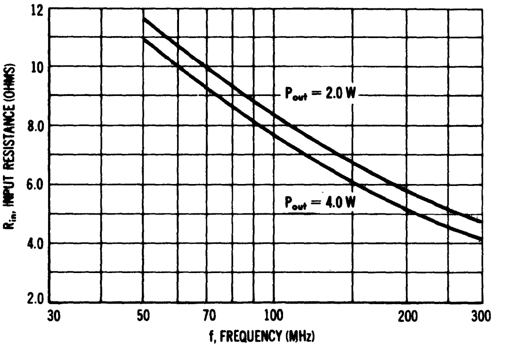


FIGURE 6 — PARALLEL EQUIVALENT INPUT CAPACITANCE

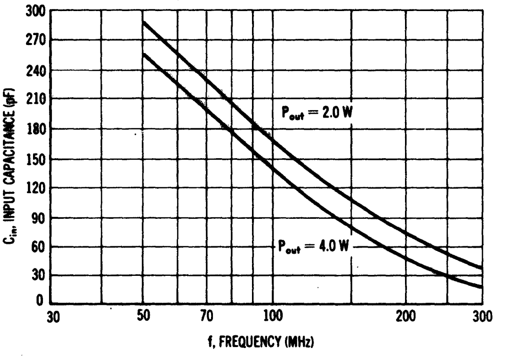


FIGURE 7 — PARALLEL EQUIVALENT OUTPUT CAPACITANCE

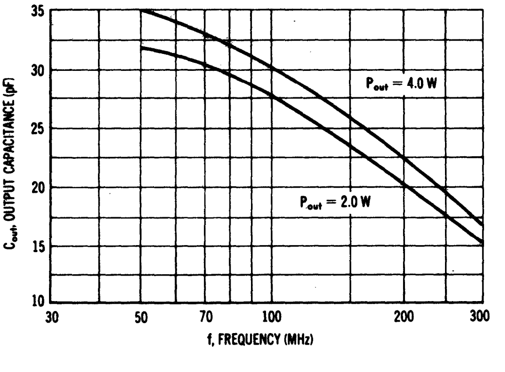


FIGURE 8 — POWER OUTPUT vs FREQUENCY

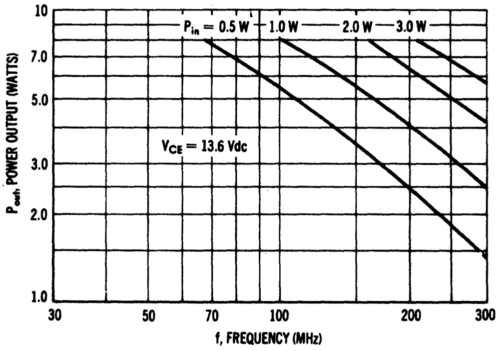
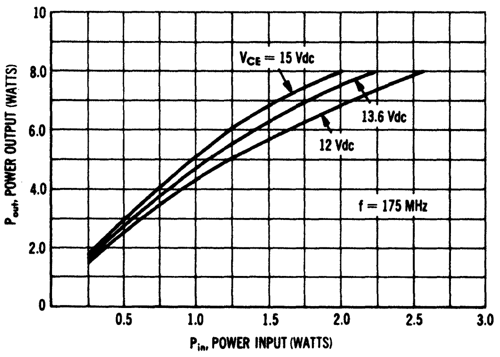


FIGURE 9 — POWER OUTPUT vs POWER INPUT



2N3925

FIGURE 10 — PARALLEL EQUIVALENT INPUT RESISTANCE

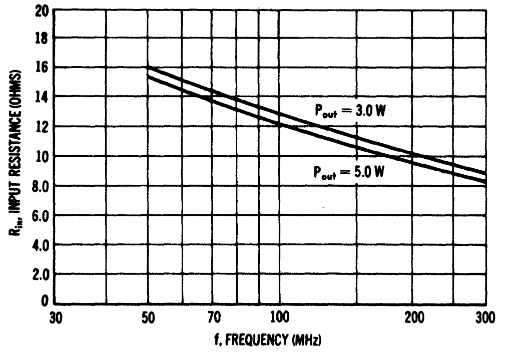


FIGURE 11 — PARALLEL EQUIVALENT INPUT CAPACITANCE

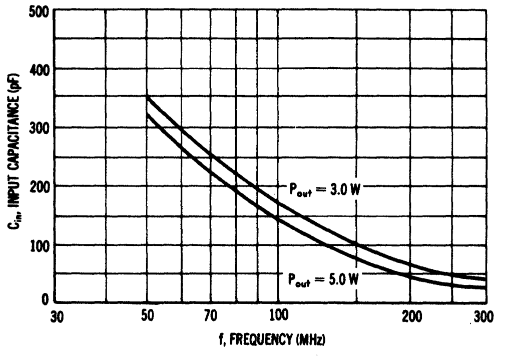
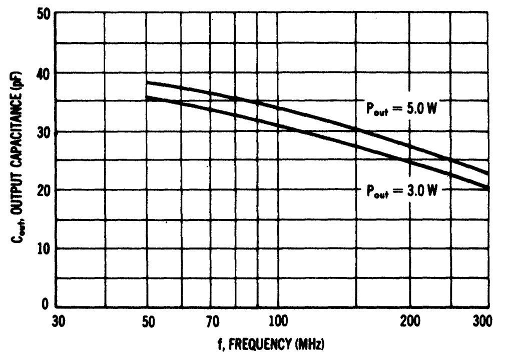


FIGURE 12 — PARALLEL EQUIVALENT OUTPUT CAPACITANCE



2N3926

FIGURE 13 — POWER OUTPUT vs FREQUENCY

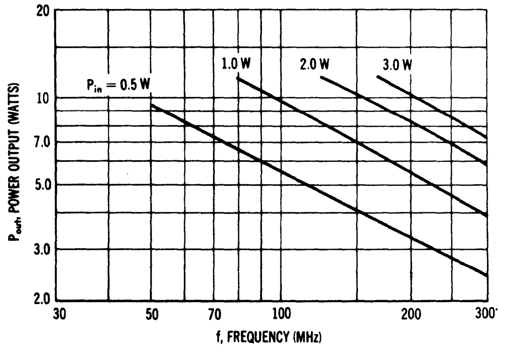


FIGURE 14 — POWER OUTPUT vs POWER INPUT

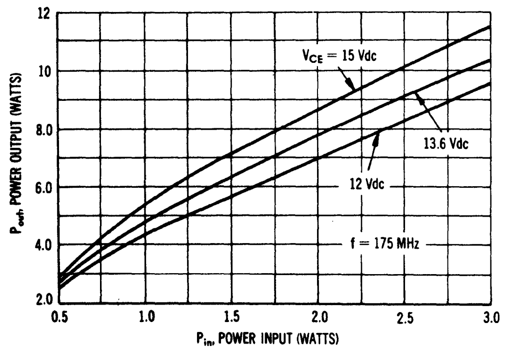


FIGURE 15 — PARALLEL EQUIVALENT INPUT RESISTANCE

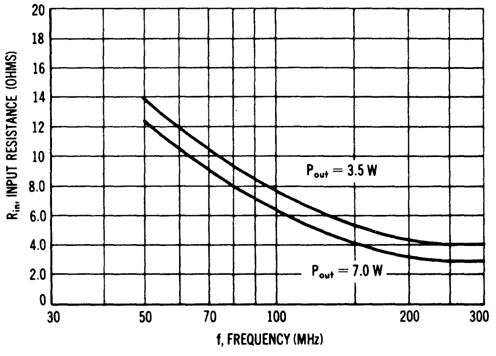


FIGURE 16 — PARALLEL EQUIVALENT INPUT CAPACITANCE

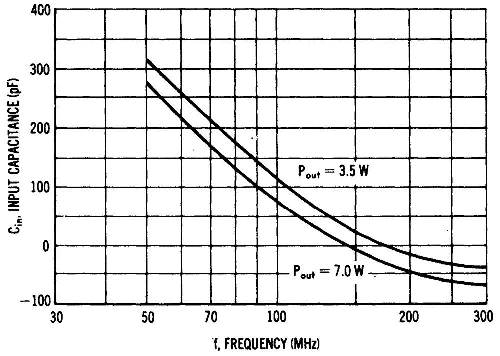
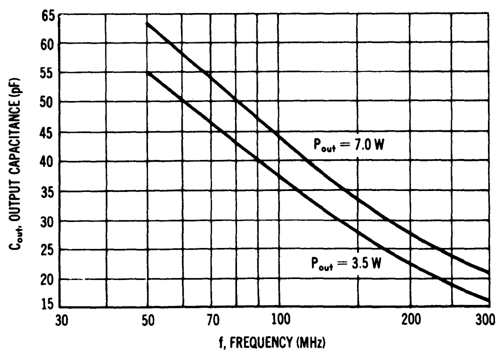


FIGURE 17 — PARALLEL EQUIVALENT OUTPUT CAPACITANCE



2N3927

FIGURE 18 — POWER INPUT vs FREQUENCY

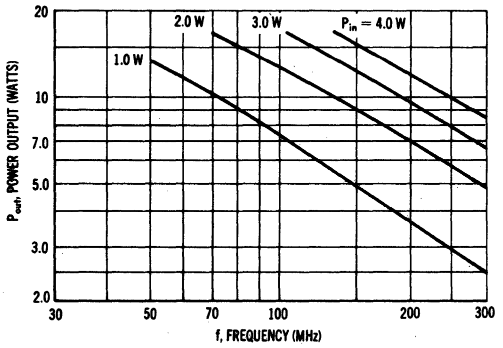


FIGURE 20 — PARALLEL EQUIVALENT INPUT RESISTANCE

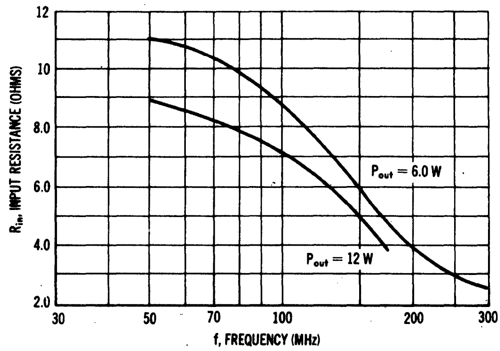


FIGURE 19 — POWER OUTPUT vs POWER INPUT

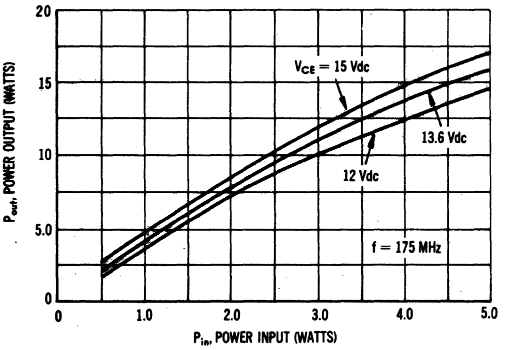


FIGURE 21 — PARALLEL EQUIVALENT INPUT CAPACITANCE

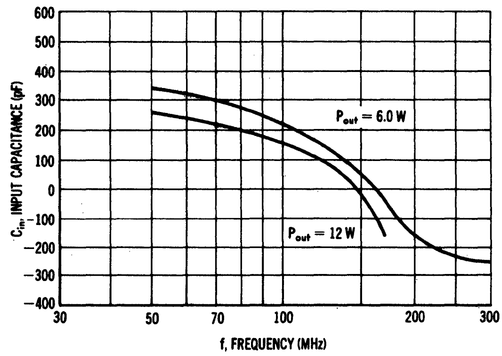
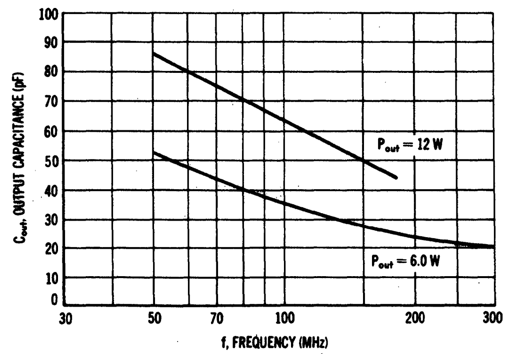


FIGURE 22 — PARALLEL EQUIVALENT OUTPUT CAPACITANCE



DESIGN NOTE

For Class C power-amplifier designs, small-signal parameters are not applicable. The parallel equivalent output capacitance and input resistance and capacitance for Class C power-amplifier design are used.

The parallel resistive portion of the collector load impedance for a power amplifier, R_L', may be computed by assuming a peak voltage swing equal to V_{CC}, and using the expression $R_L' = V_{CC}^2/2P$ where P = RF power output. The computed R_L' may then be combined with the data for Class C design to complete device impedance data.