

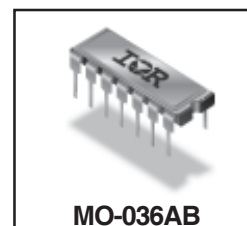
**POWER MOSFET
THRU-HOLE (MO-036AB)**

**IRFG6110
JANTX2N7336
JANTXV2N7336
REF:MIL-PRF-19500/598
100V, Combination 2N-2P-CHANNEL
HEXFET[®] MOSFET TECHNOLOGY**

Product Summary

Part Number	R _{DS(on)}	I _D	CHANNEL
IRFG6110	0.7Ω	1.0A	N
IRFG6110	1.4Ω	-0.75A	P

HEXFET[®] MOSFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry design achieves very low on-state resistance combined with high transconductance. HEXFET transistors also feature all of the well-established advantages of MOSFETs, such as voltage control, very fast switching, ease of paralleling and electrical parameter temperature stability. They are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, high energy pulse circuits, and virtually any application where high reliability is required. The HEXFET transistor's totally isolated package eliminates the need for additional isolating material between the device and the heatsink. This improves thermal efficiency and reduces drain capacitance.



Features:

- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Electrically Isolated
- Dynamic dv/dt Rating
- Light-weight

Absolute Maximum Ratings (Per Die)

	Parameter	N-Channel	P-Channel	Units
I _D @ V _{GS} = ± 10V, T _C = 25°C	Continuous Drain Current	1.0	-0.75	A
I _D @ V _{GS} = ± 10V, T _C = 100°C	Continuous Drain Current	0.6	-0.5	
I _{DM}	Pulsed Drain Current ①	4.0	-3.0	
P _D @ T _C = 25°C	Max. Power Dissipation	1.4	1.4	W
	Linear Derating Factor	0.011	0.011	W/°C
V _{GS}	Gate-to-Source Voltage	±20	±20	V
E _{AS}	Single Pulse Avalanche Energy	75 ②	75 ⑤	mJ
I _{AR}	Avalanche Current ①	1.0	-0.75	A
E _{AR}	Repetitive Avalanche Energy ①	0.14	0.14	mJ
dv/dt	Peak Diode Recovery dv/dt	5.5 ③	-5.5 ⑥	V/ns
T _J	Operating Junction	-55 to 150		°C
T _{STG}	Storage Temperature Range			
	Lead Temperature	300 (0.63 in./1.6 mm from case for 10s)		
	Weight	1.3 (Typical)		g

For footnotes, refer to the last page

Electrical Characteristics For Each N-Channel Device @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V _{GS} = 0V, I _D = 1.0mA
ΔBV _{DSS} /ΔT _J	Temperature Coefficient of Breakdown Voltage	—	0.13	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	0.7	Ω	V _{GS} = 10V, I _D = 0.6A ④
		—	—	0.8		V _{GS} = 10V, I _D = 1.0A
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	0.86	—	—	S	V _{DS} > 15V, I _{DS} = 0.6A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	25	μA	V _{DS} = 80V, V _{GS} = 0V
		—	—	250		V _{DS} = 80V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -20V
Q _g	Total Gate Charge	—	—	15	nC	V _{GS} = 10V, I _D = 1.0A, V _{DS} = 50V
Q _{gs}	Gate-to-Source Charge	—	—	7.5		
Q _{gd}	Gate-to-Drain ('Miller') Charge	—	—	7.5		
t _{d(on)}	Turn-On Delay Time	—	—	20	ns	V _{DD} = 50V, I _D = 1.0A, V _{GS} = 10V, R _G = 7.5Ω
t _r	Rise Time	—	—	25		
t _{d(off)}	Turn-Off Delay Time	—	—	40		
t _f	Fall Time	—	—	40		
L _S + L _D	Total Inductance	—	10	—	nH	Measured from drain lead (6mm/0.25in. from package) to source lead (6mm/0.25in. from package)
C _{iss}	Input Capacitance	—	180	—	pF	V _{GS} = 0V, V _{DS} = 25V f = 1.0MHz
C _{oss}	Output Capacitance	—	82	—		
C _{rss}	Reverse Transfer Capacitance	—	15	—		

Source-Drain Diode Ratings and Characteristics (Per Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	1.0	A	T _j = 25°C, I _S = 1.0A, V _{GS} = 0V ④
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	4.0		
V _{SD}	Diode Forward Voltage	—	—	1.5	V	T _j = 25°C, I _F = 1.0A, di/dt ≤ 100A/μs V _{DD} ≤ 50V ④
t _{rr}	Reverse Recovery Time	—	—	200	nS	
Q _{RR}	Reverse Recovery Charge	—	—	0.83	nC	
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

Thermal Resistance (Per Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJC}	Junction-to-Case	—	—	17	°C/W	Typical socket mount
R _{thJA}	Junction-to-Ambient	—	—	90		

Note: Corresponding Spice and Saber models are available on International Rectifier Website.

For footnotes, refer to the last page

Electrical Characteristics For Each P-Channel Device @ $T_J = 25^\circ\text{C}$ (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-100	—	—	V	$V_{GS} = 0V, I_D = -1.0mA$
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	-0.098	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = -1.0mA$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	1.4	Ω	$V_{GS} = -10V, I_D = -0.5A$ ④
		—	—	1.73		$V_{GS} = -10V, I_D = -0.75A$
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
g_{fs}	Forward Transconductance	0.67	—	—	S	$V_{DS} > -15V, I_{DS} = -0.5A$ ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-25	μA	$V_{DS} = -80V, V_{GS} = 0V$
		—	—	-250		$V_{DS} = -80V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	$V_{GS} = -20V$
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	100		$V_{GS} = 20V$
Q_g	Total Gate Charge	—	—	15	nC	$V_{GS} = -10V, I_D = -0.75A, V_{DS} = -50V$
Q_{gs}	Gate-to-Source Charge	—	—	7.0		
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	8.0		
$t_{d(on)}$	Turn-On Delay Time	—	—	30	ns	$V_{DD} = -50V, I_D = -0.75A, V_{GS} = -10V, R_G = 7.5\Omega$
t_r	Rise Time	—	—	60		
$t_{d(off)}$	Turn-Off Delay Time	—	—	70		
t_f	Fall Time	—	—	80		
$L_S + L_D$	Total Inductance	—	10	—	nH	Measured from drain lead (6mm/0.25in. from package) to source lead (6mm/0.25in. from package)
C_{iss}	Input Capacitance	—	200	—	pF	$V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz$
C_{oss}	Output Capacitance	—	85	—		
C_{rss}	Reverse Transfer Capacitance	—	30	—		

Source-Drain Diode Ratings and Characteristics (Per Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-0.75	A	T _j = 25°C, I _S = -0.75A, V _{GS} = 0V ④
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	-3.0		
V _{SD}	Diode Forward Voltage	—	—	-5.5	V	T _j = 25°C, I _F = -0.75A, di/dt ≤ -100A/μs V _{DD} ≤ -50V
t _{rr}	Reverse Recovery Time	—	—	200	nS	
Q _{RR}	Reverse Recovery Charge	—	—	9.0	nC	
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

Thermal Resistance (Per Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJC}	Junction-to-Case	—	—	17	$^\circ\text{C/W}$	Typical socket mount
R_{thJA}	Junction-to-Ambient	—	—	90		

For footnotes, refer to the last page

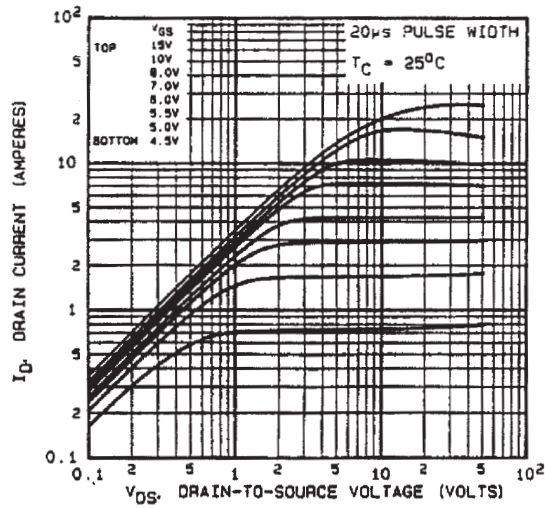
N-Channel
G1,G3

Fig 1. Typical Output Characteristics

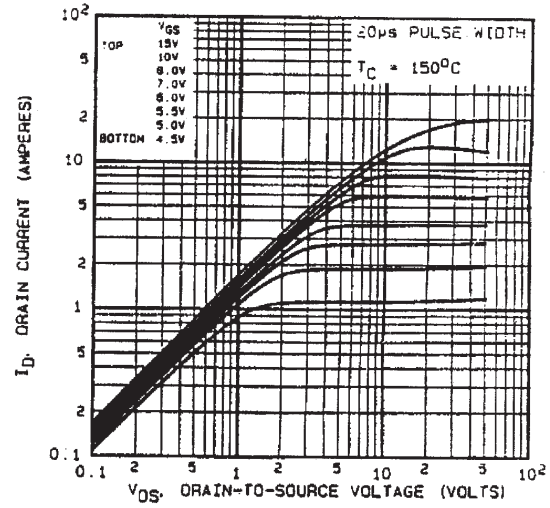


Fig 2. Typical Output Characteristics

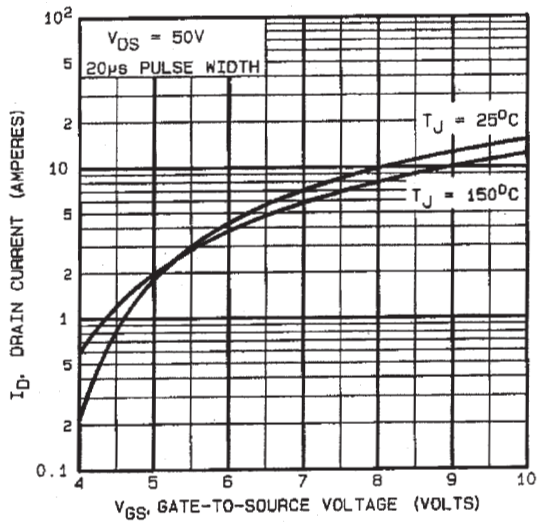
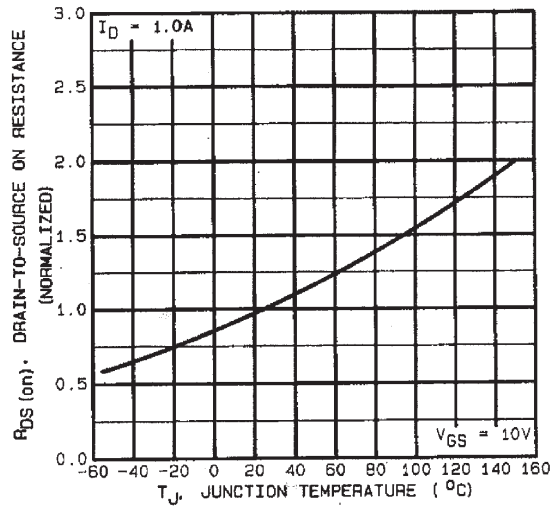


Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance
Vs. Temperature

N-Channel
G1,G3

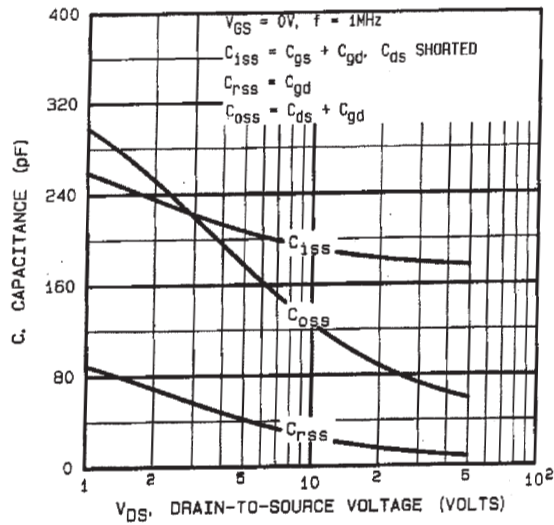


Fig 5. Typical Capacitance Vs.
Drain-to-Source Voltage

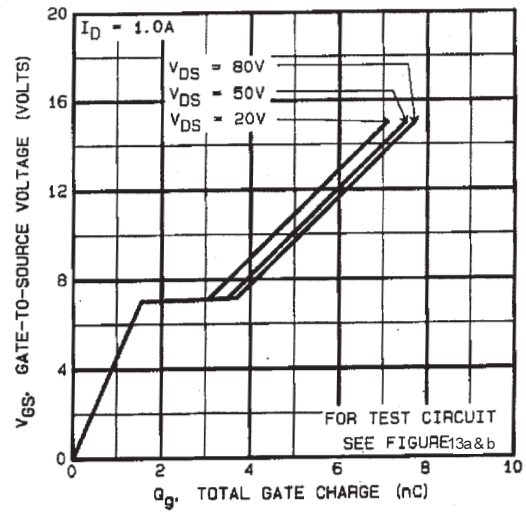


Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage

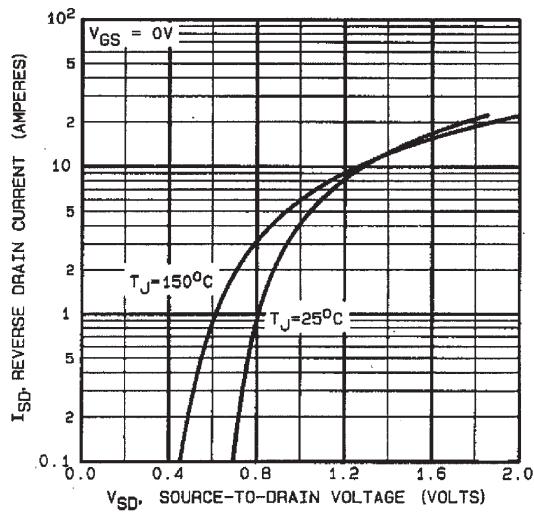


Fig 7. Typical Source-Drain Diode
Forward Voltage

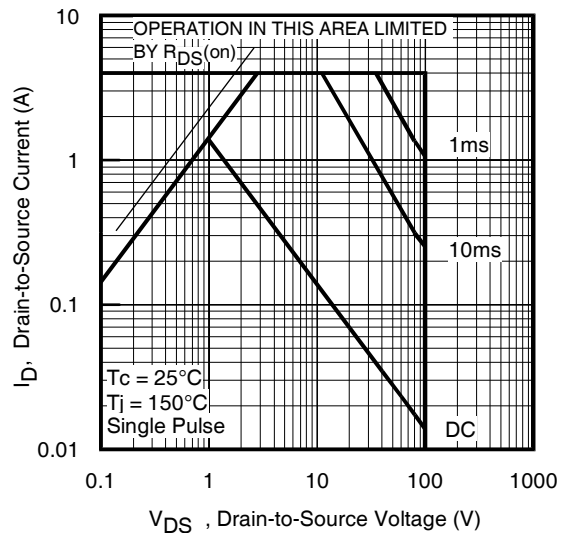


Fig 8. Maximum Safe Operating Area

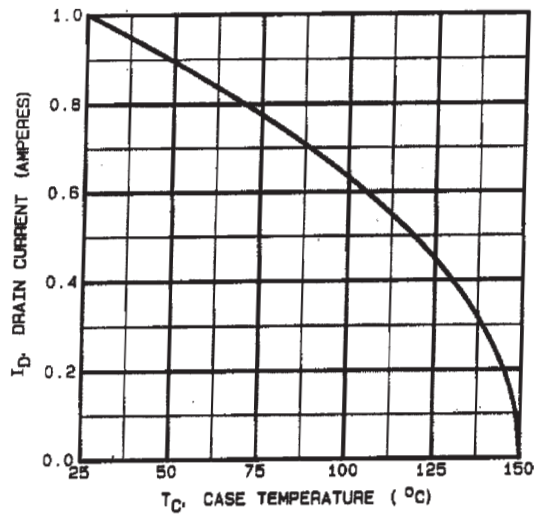
N-Channel
G1,G3

Fig 9. Maximum Drain Current Vs. Case Temperature

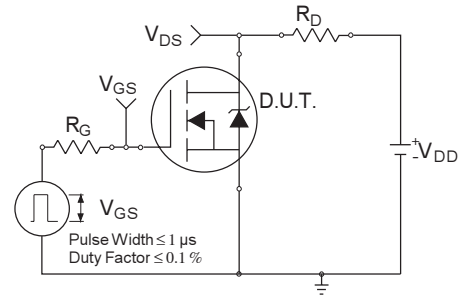


Fig 10a. Switching Time Test Circuit

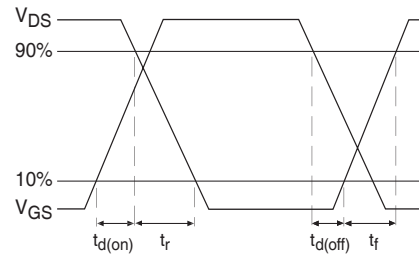


Fig 10b. Switching Time Waveforms

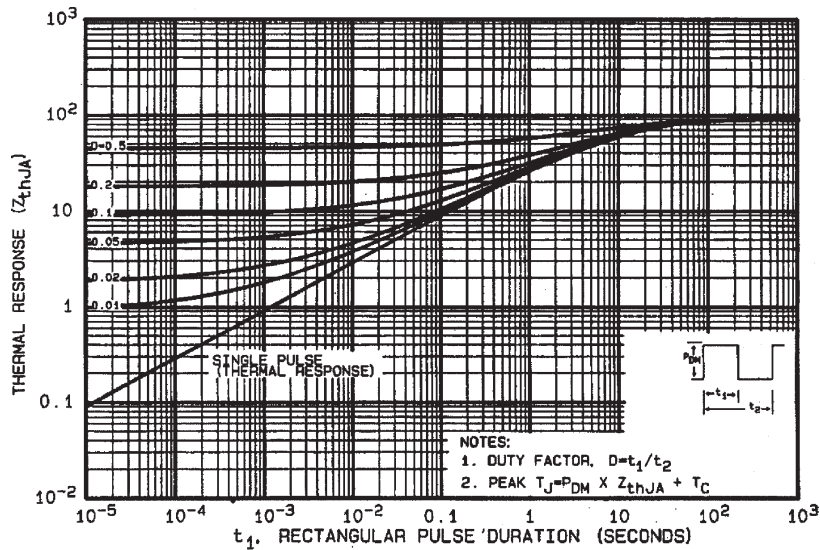


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

N-Channel
G1,G3

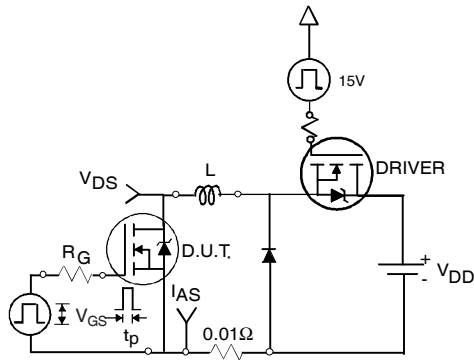


Fig 12a. Unclamped Inductive Test Circuit

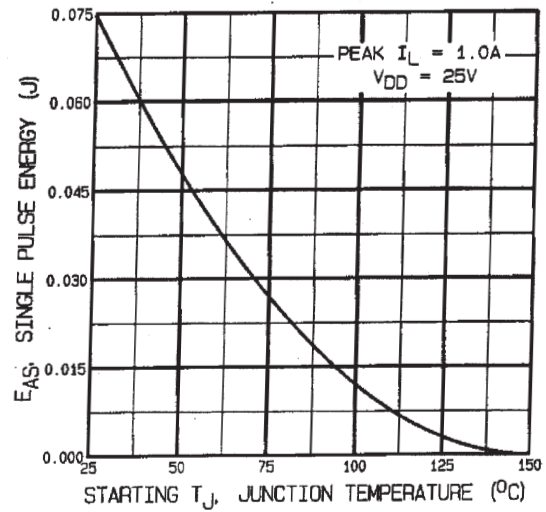


Fig 12c. Maximum Avalanche Energy
Vs. Drain Current

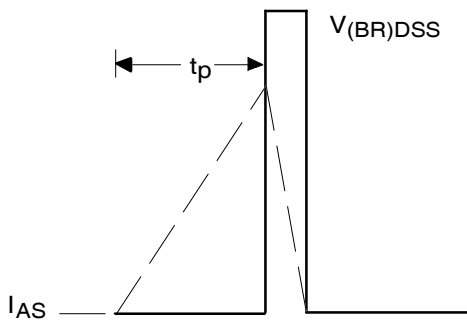


Fig 12b. Unclamped Inductive Waveforms

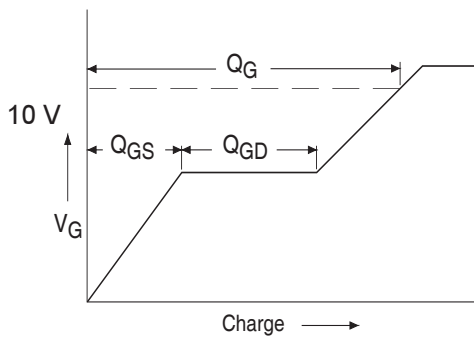


Fig 13a. Basic Gate Charge Waveform

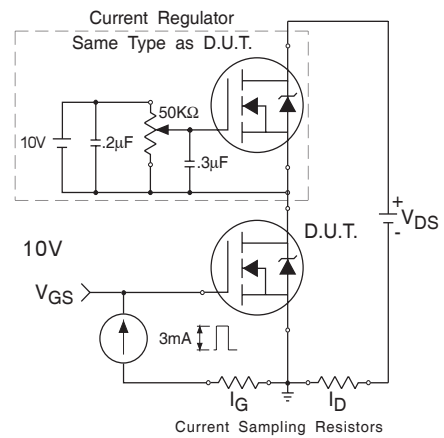


Fig 13b. Gate Charge Test Circuit

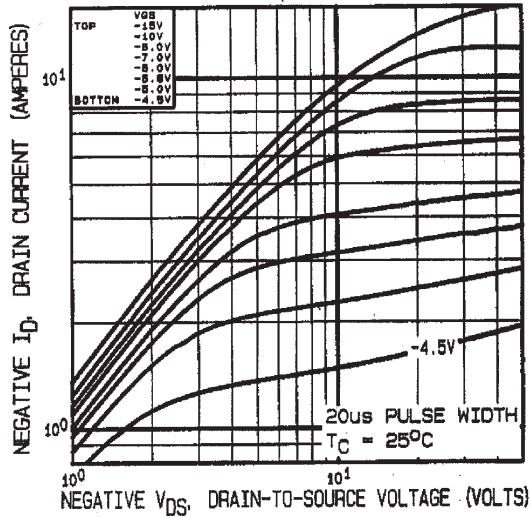
P-Channel
G2,G4

Fig 14. Typical Output Characteristics

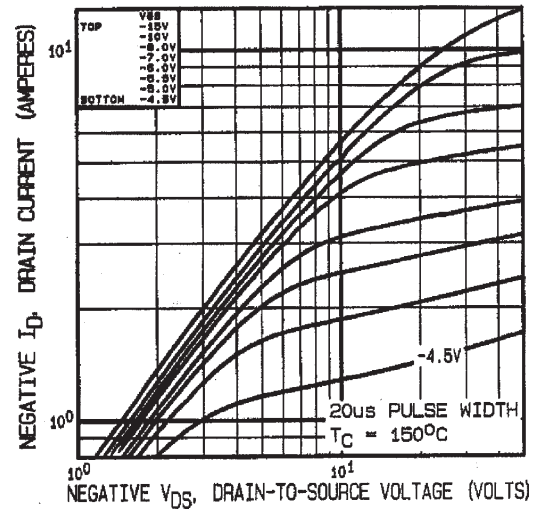


Fig 15. Typical Output Characteristics

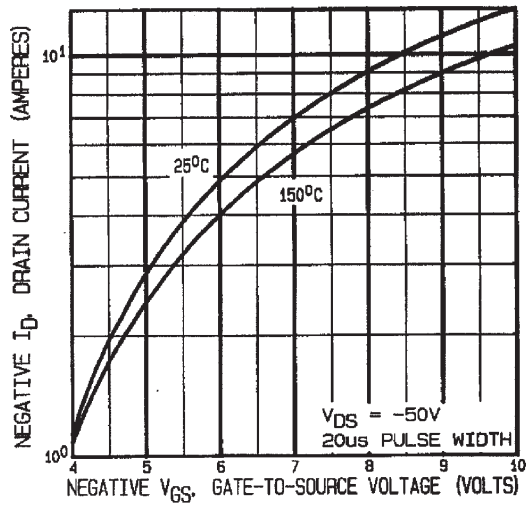
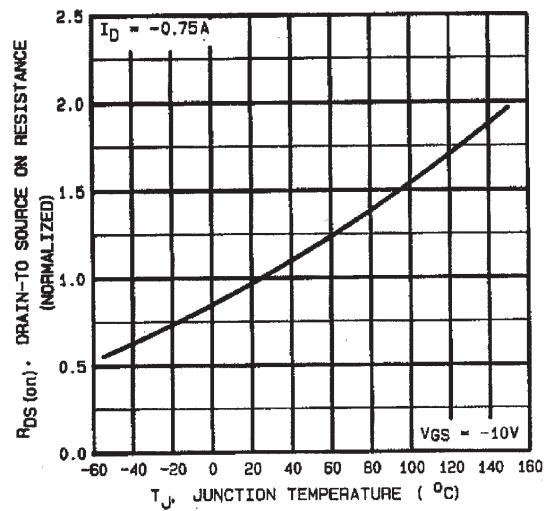


Fig 16. Typical Transfer Characteristics

Fig 17. Normalized On-Resistance
Vs. Temperature

P-Channel
G2,G4

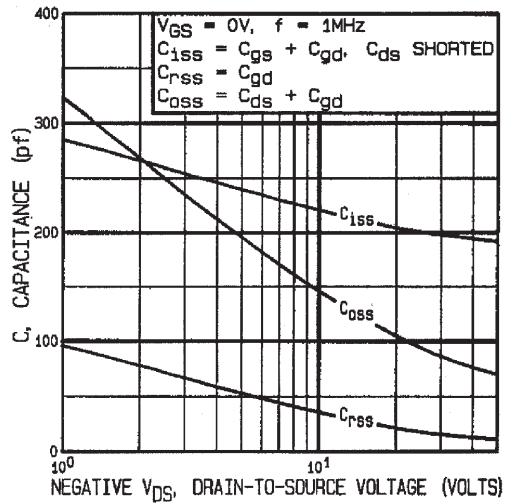


Fig 18. Typical Capacitance Vs.
Drain-to-Source Voltage

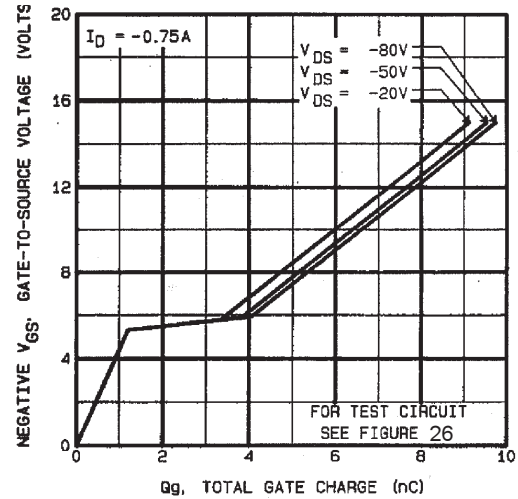


Fig 19. Typical Gate Charge Vs.
Gate-to-Source Voltage

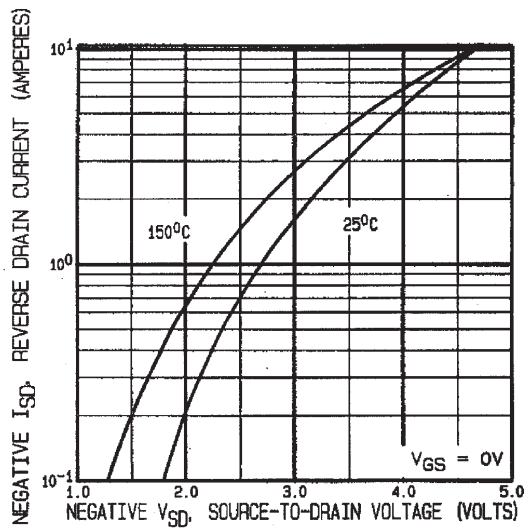


Fig 20. Typical Source-Drain Diode
Forward Voltage

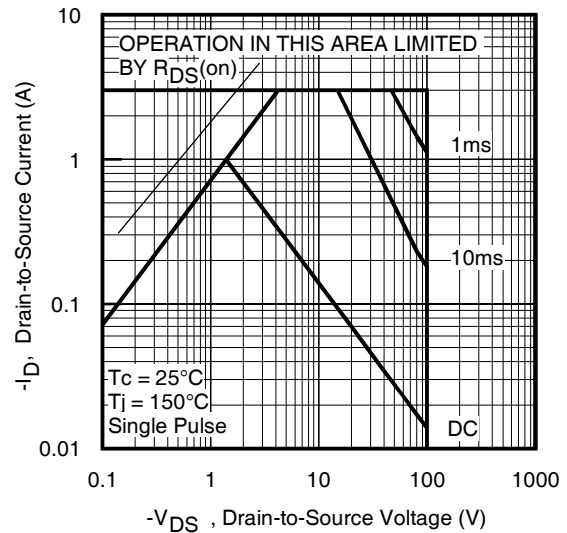


Fig 21. Maximum Safe Operating Area

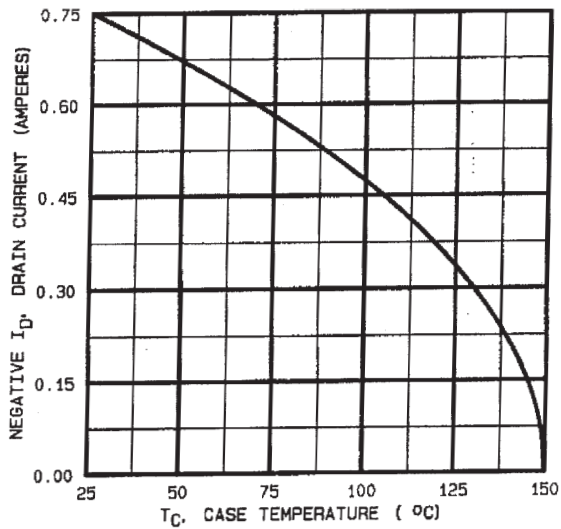
P-Channel
G2,G4

Fig22. Maximum Drain Current Vs. Case Temperature

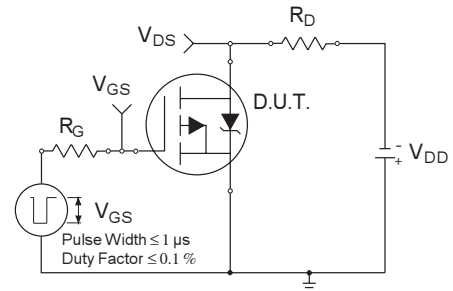


Fig 23a. Switching Time Test Circuit

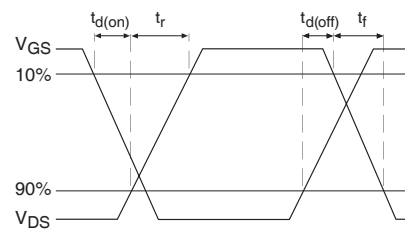


Fig 23b. Switching Time Waveforms

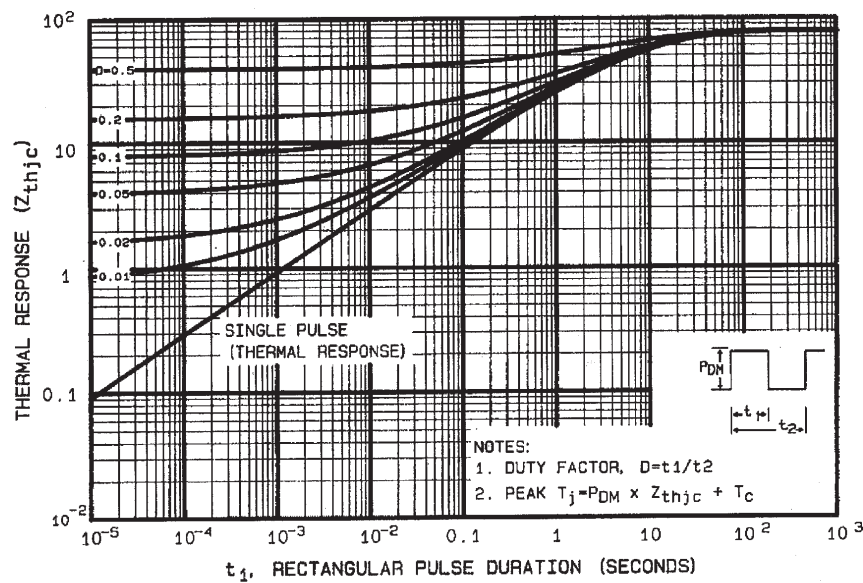


Fig 24. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

**P-Channel
G2,G4**

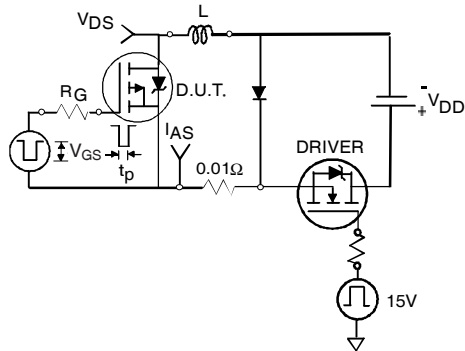


Fig 25a. Unclamped Inductive Test Circuit

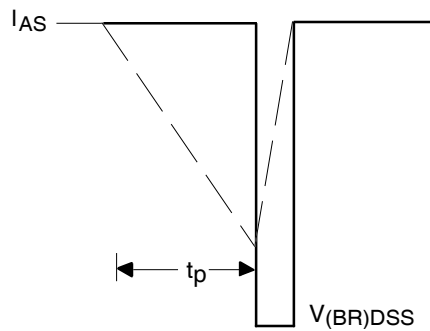


Fig 25b. Unclamped Inductive Waveforms

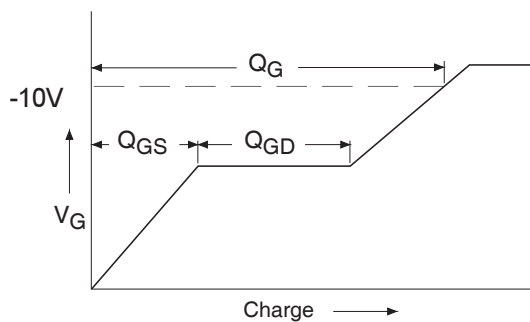


Fig 26a. Basic Gate Charge Waveform

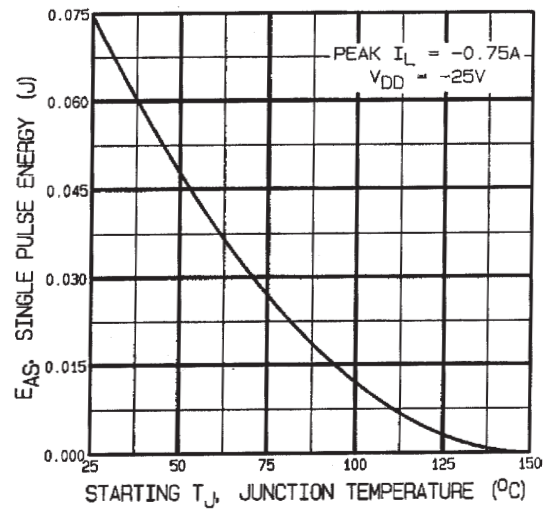


Fig 25c. Maximum Avalanche Energy
Vs. Drain Current

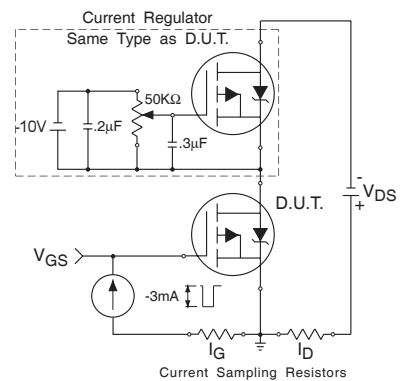


Fig 26b. Gate Charge Test Circuit

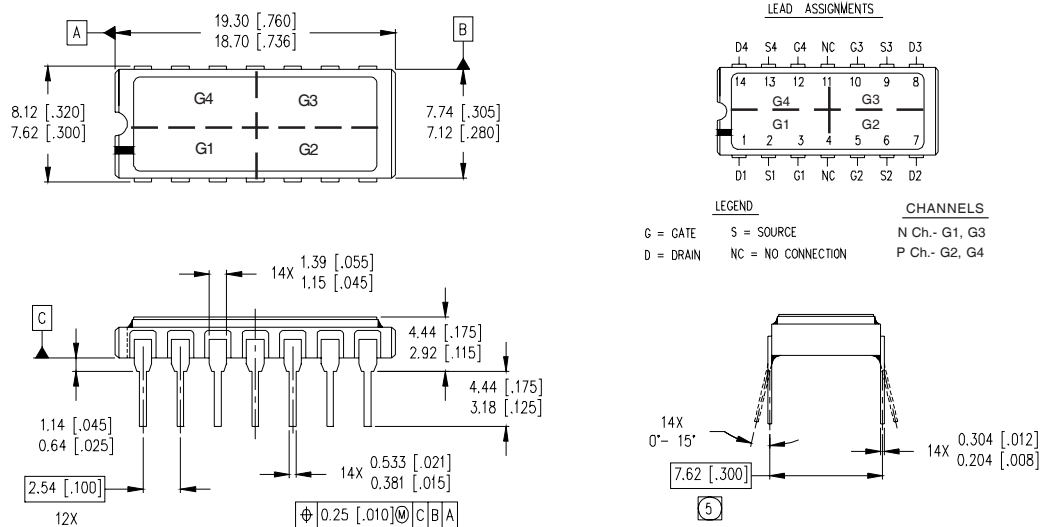
IRFG6110

International
IR Rectifier

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = 25V$, starting $T_J = 25^\circ C$, $L = 150mH$, Peak $I_L = 1.0A$, $V_{GS} = 10V$
- ③ $I_{SD} \leq 1.0A$, $di/dt \leq 75A/\mu s$, $V_{DD} \leq 100V$, $T_J \leq 150^\circ C$
- ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$
- ⑤ $V_{DD} = -25V$, starting $T_J = 25^\circ C$, $L = 266mH$, Peak $I_L = -0.75A$, $V_{GS} = -10V$
- ⑥ $I_{SD} \leq -0.75A$, $di/dt \leq -75A/\mu s$, $V_{DD} \leq -100V$, $T_J \leq 150^\circ C$

Case Outline and Dimensions — MO-036AB



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MO-036AB.
- ⑤ MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

International
IR Rectifier

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TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information.

Data and specifications subject to change without notice. 02/2010