

#### ◆ Features

- Up to 2.7 GHz frequency band
- Beyond +31 dBm output power
- Up to +48dBm Output IP3
- High Drain Efficiency
- 11dB Gain at 2.1GHz
- SOT-89 SMT Package
- Low Noise Figure



#### ◆ Applications

- Wireless communication system
- Cellular, PCS, PHS, W-CDMA, WLAN

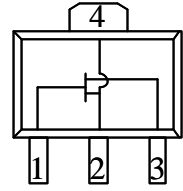
#### ◆ Description

P0120009P is a high performance GaAs MESFET housed in a low-cost SOT-89 package. Our originally developed "pulse-doped" channel structure has realized low distortion, which leads to high IP3. The channel structure also achieved an extremely low noise figure. The details about pulse-doped FET channel are described in our products catalog. Utilization of AuSn die attach has realized a low and stable thermal resistance. *The lead frame is plated with Sn-Bi to make the device Pb-free.*

Eudyna's long history of manufacturing has cultivated high device reliability. The estimated MTTF of the FET is longer than 15years at Tj of 150°C. You can see the details in *Reliability and Quality Assurance*.

#### ◆ Functional Diagram

Pin No.	Function
1	Input/Gate
2, 4	Ground
3	Output/Drain



#### ◆ Ordering Information

Part No	Description	Number of devices	Container
P0120009P	GaAs Power FET	1000	7" Reel
KP029J	2.11-2.17GHz Application Circuit	1	Anti-static Bag

#### ◆ Absolute Maximum Ratings (@Tc=25°C)

Parameter	Symbol	Value	Units
Drain-Source Voltage	Vds	10	V
Gate-Source Voltage	Vgs	- 4	V
Drain Current	Ids	Idss	---
RF Input Power (continuous)	Pin	23 (*)	dBm
Power Dissipation	Pt	5.43	W
Junction Temperature	Tj	150 (**)	°C
Storage Temperature	Tstg	- 40 to +150	°C

Tc: Case Temperature. Operating the device beyond any of these values may cause permanent damage.

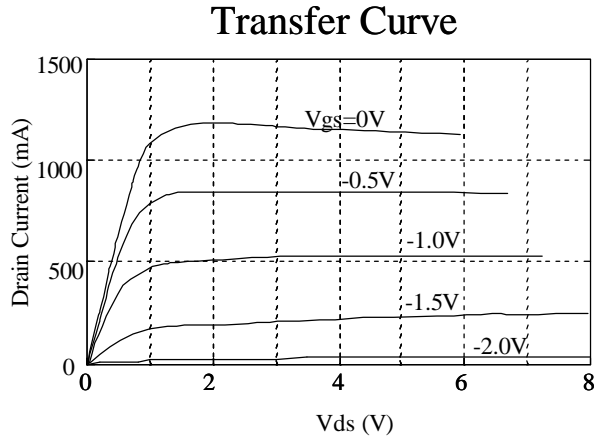
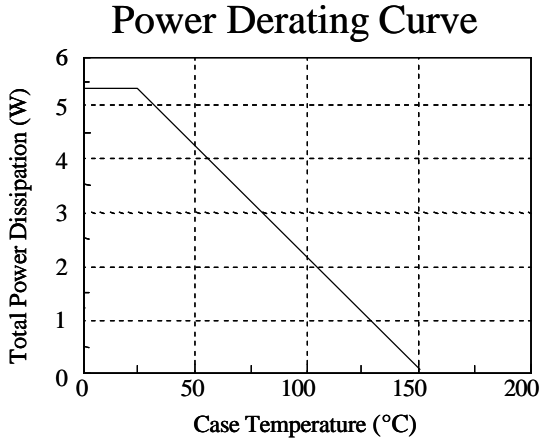
(\*) Measured at 2.1GHz with our test fixture matched to IP3.

(\*\*) Recommended Tj under operation is below 125°C.

#### ◆ Electrical Specifications (@Tc=25°C)

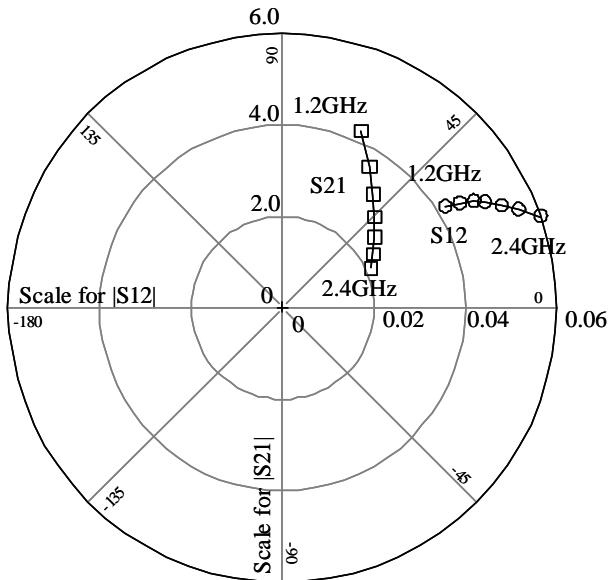
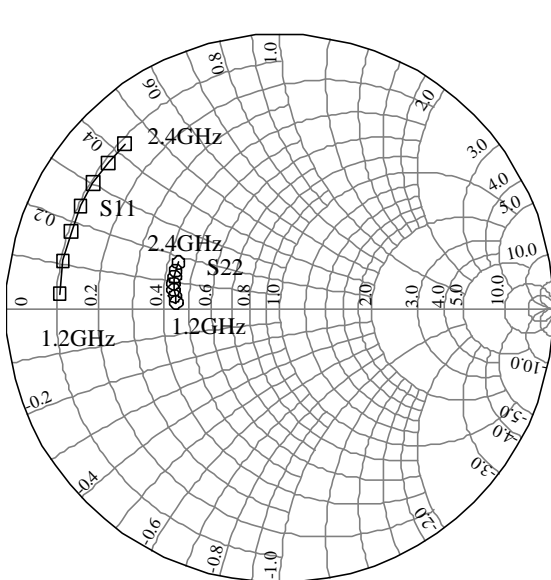
Parameter	Symbol	Test Conditions	Values			Units		
			Min.	Typ.	Max.			
DC	Saturated Drain Current	Idss	Vds=3V, Vg=0V	---	---	1400	mA	
	Transconductance	gm	Vds=3V, Ids=400mA	450	---	---	mS	
	Pinchoff Voltage	Vp	Vds=8V, Ids=50mA	- 3.0	---	- 1.5	V	
	Gate-Source Breakdown Voltage	Vgs0	Igso= - 50μA	3.0	---	---	V	
	Thermal Resistance	Rth	Channel-Case	---	---	22	°C/W	
RF	Frequency	f				2.7	GHz	
	Output Power @ 1dB Gain Compression	P1dB	Vds=8V Ids=400mA f=2.1GHz		33	---	dBm	
	Small Signal Gain	G			11	---	dB	
	Output IP3	IP3			---	48	---	dBm
	Power Added Efficiency	η <sub>add</sub>			---	57	---	%

◆ Typical Characteristics

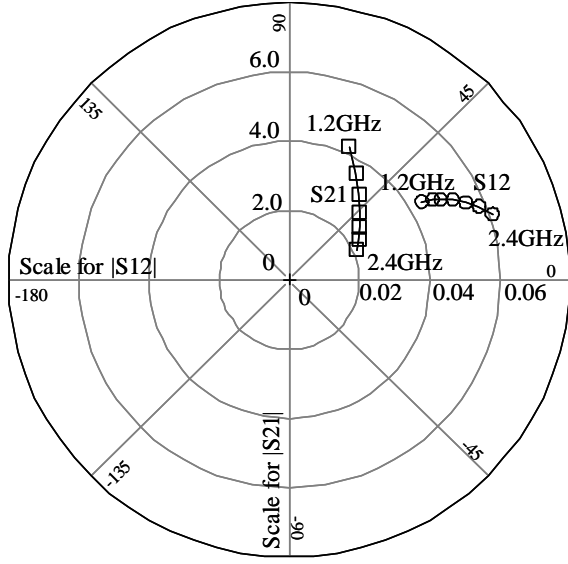
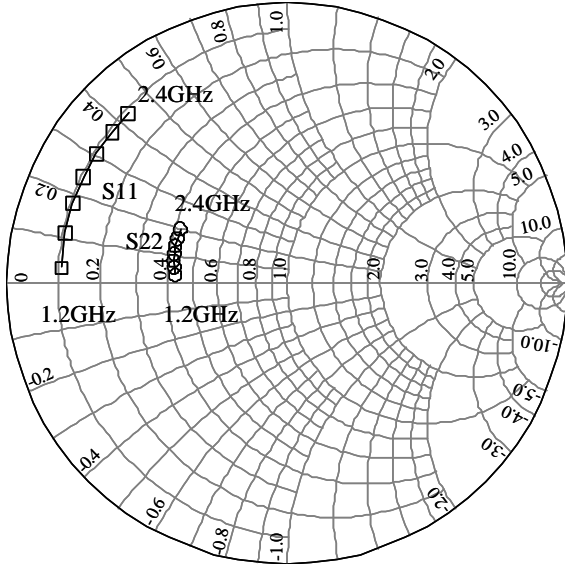


◆ Load-pull Characteristics (Typical Data)

T<sub>c</sub>=25°C, V<sub>ds</sub>=8V, I<sub>ds</sub>=400mA, Common Source, Z<sub>o</sub>=50Ω (Calibrated to device leads)



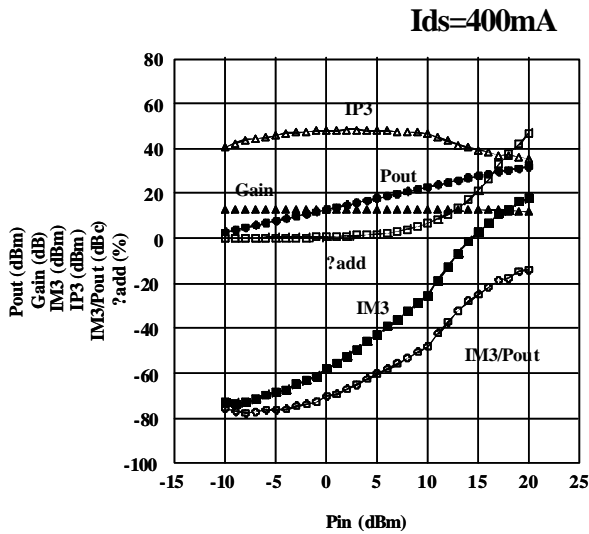
Tc=25°C, Vds=8V, **Ids=350mA**, Common Source, Zo=50Ω (Calibrated to device leads)



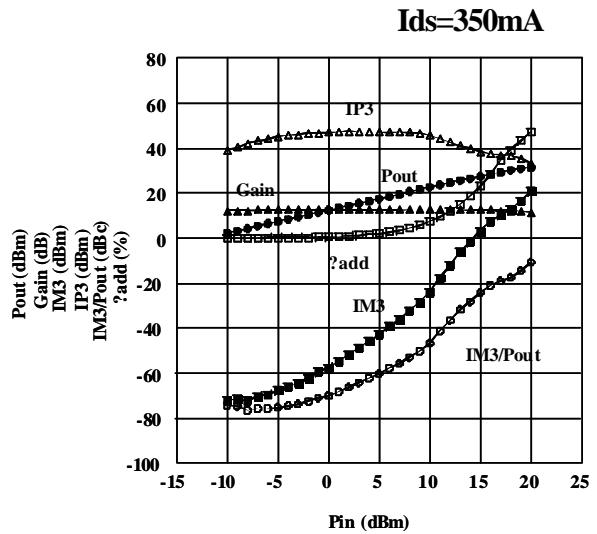
Ids=400mA	Freq(GHz)	S11 Mag	S11Ang	S21 Mag	S21 Ang	S12 Mag	S12 Ang	S22 Mag	S22 Ang
	1.2	0.807	176.1	4.225	66.1	0.042	31.9	0.380	176.7
	1.4	0.812	167.5	3.630	58.4	0.045	30.5	0.387	173.2
	1.6	0.815	159.8	3.179	51.2	0.048	29.2	0.394	170.0
	1.8	0.819	152.8	2.826	44.3	0.050	27.5	0.399	166.9
	2.0	0.822	146.1	2.545	37.4	0.053	25.1	0.403	163.4
	2.2	0.823	139.6	2.316	30.7	0.056	22.6	0.406	159.8
	2.4	0.827	133.4	2.124	24.0	0.060	19.5	0.408	155.7

Ids=350mA	Freq(GHz)	S11 Mag	S11Ang	S21 Mag	S21 Ang	S12 Mag	S12 Ang	S22 Mag	S22 Ang
	1.2	0.808	176.0	4.203	66.2	0.044	31.0	0.400	175.6
	1.4	0.812	167.2	3.612	58.5	0.047	29.6	0.407	171.8
	1.6	0.818	159.5	3.162	51.4	0.049	28.3	0.414	168.6
	1.8	0.821	152.5	2.811	44.4	0.052	26.5	0.417	165.3
	2.0	0.823	145.8	2.533	37.6	0.055	24.0	0.422	161.6
	2.2	0.824	139.2	2.303	30.9	0.058	21.4	0.423	157.9
	2.4	0.828	133.0	2.113	24.2	0.061	18.2	0.427	153.3

**[Note]** You can download the S-parameter list from our web site: [www.eudyna.com](http://www.eudyna.com)



Device: P0120009P  
 Frequency: f1=2.1GHz f2=2.101GHz  
 Bias: Vds=8V, Ids=400mA  
 Source Matching: Mag 0.74 Ang -156.6°  
 Load Matching: Mag 0.554 Ang -171.5°



Device: P0120009P  
 Frequency: f1=2.1GHz f2=2.101GHz  
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 Source Matching: Mag 0.74 Ang -156.6°  
 Load Matching: Mag 0.49 Ang -172.9°

[Note] P<sub>out</sub> and  $\eta_{add}$  are measured by one signal.

The data for the figures above were measured with the load impedance matched to IP3.

Id=400mA	Pin	Pout	Gain	IM3	IM3/Pout	IP3	Id	$\eta_{add}$
	(dBm)	(dBm)	(dB)	(dBm)	(dBc)	(dBm)	(mA)	(%)
	-10.0	2.8	12.8	-72.9	-75.7	40.6	401.3	0.1
	-5.0	7.8	12.8	-68.6	-76.3	45.7	397.0	0.2
	0.0	12.7	12.7	-57.7	-70.3	47.8	387.4	0.6
	5.0	17.7	12.7	-42.7	-60.3	47.8	370.0	1.9
	10.0	22.9	12.9	-25.1	-48.0	46.6	343.7	6.7
	15.0	27.7	12.7	2.7	-25.0	39.3	323.3	21.3
	20.0	31.7	11.7	17.7	-14.0	35.2	367.9	46.9

Id=350mA	Pin	Pout	Gain	IM3	IM3/Pout	IP3	Id	$\eta_{add}$
	(dBm)	(dBm)	(dB)	(dBm)	(dBc)	(dBm)	(mA)	(%)
	-10.0	2.2	12.2	-72.1	-74.3	39.4	346.7	0.1
	-5.0	7.5	12.5	-67.7	-75.2	45.2	342.5	0.2
	0.0	12.5	12.5	-57.6	-70.0	47.1	333.5	0.6
	5.0	17.5	12.5	-42.7	-60.2	47.3	317.3	2.1
	10.0	22.7	12.7	-23.9	-46.7	45.8	298.0	7.5
	15.0	27.5	12.5	3.4	-24.2	38.5	289.5	23.1
	20.0	31.6	11.6	20.9	-10.7	33.2	352.1	47.3



# P0120009P

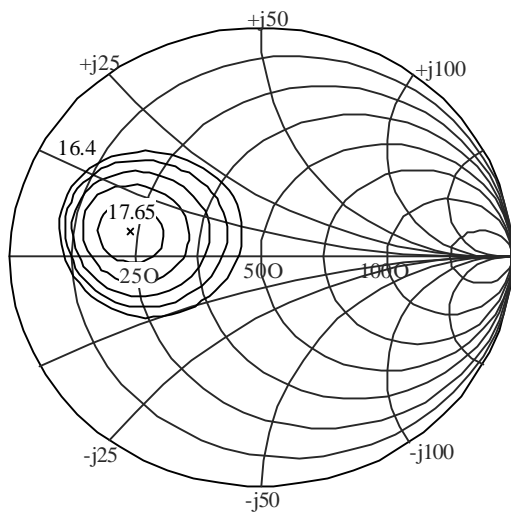
## 2W GaAs Power FET (Pb-Free Type)

### Technical Note

Tc= 25°C, Vds=8V, Ids=400mA, Pin=5dBm

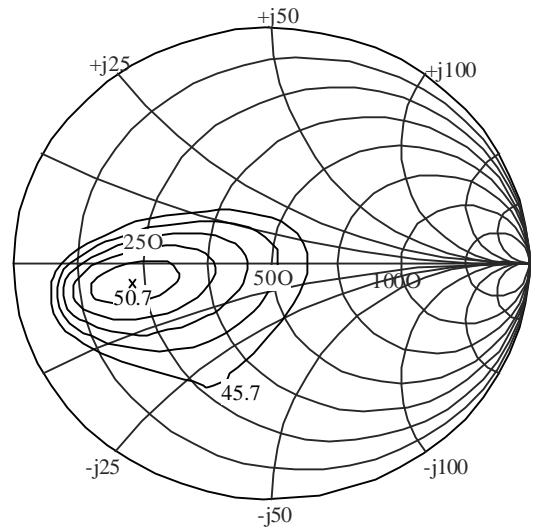
**[Pout-Lstate]**

f = 2.1GHz       $G_{pout} : 0.54 \angle 169.9$   
 Source :  $0.81 \angle -155.1$   
 Pout max : 17.65dBm



**[IP3-Lstate]**

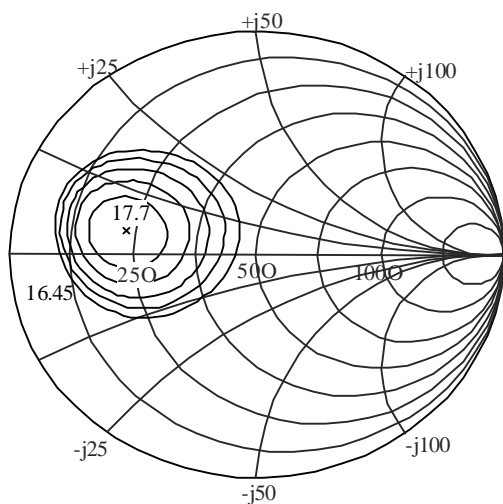
f1 = 2.1GHz       $G_{IP3} : 0.55 \angle -171.5$   
 f2 = 2.101GHz      Source :  $0.74 \angle -156.6$   
 IP3 max : 50.7dBm



Tc= 25°C, Vds=8V, Ids=350mA, Pin=5dBm

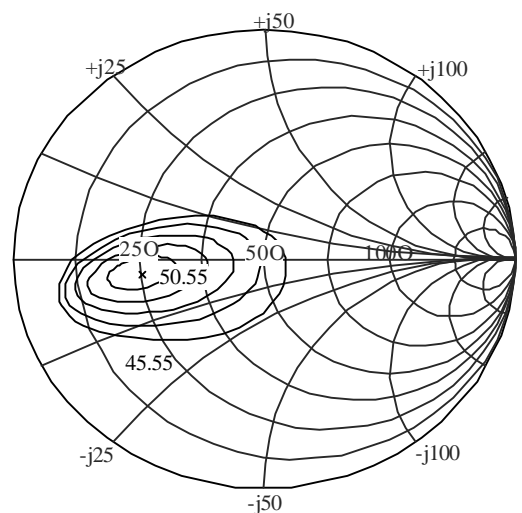
**[Pout-Lstate]**

f = 2.1GHz       $G_{pout} : 0.54 \angle 169.9$   
 Source :  $0.81 \angle -155.1$   
 Pout max : 17.7dBm



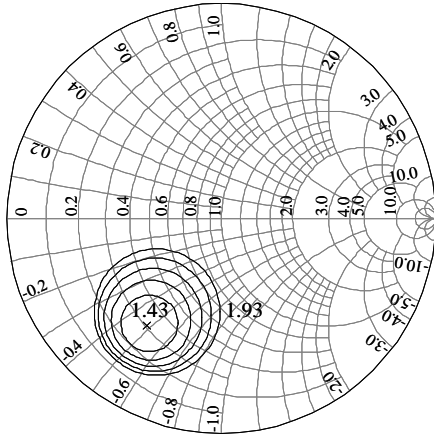
**[IP3-Lstate]**

f1 = 2.1GHz       $G_{IP3} : 0.49 \angle -172.9$   
 f2 = 2.101GHz      Source :  $0.74 \angle -156.6$   
 IP3 max : 50.55dBm

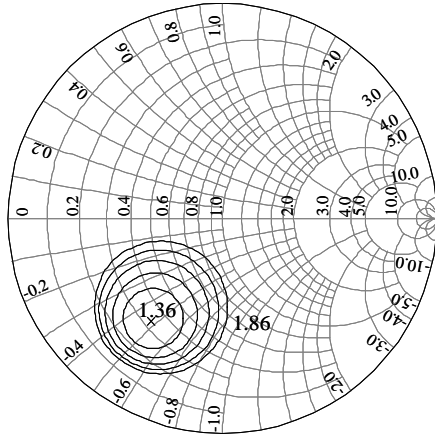


◆ **NF Characteristics**

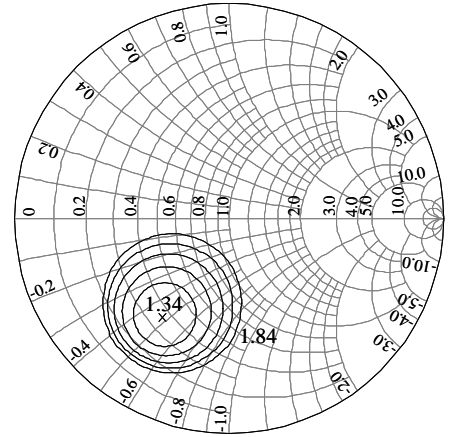
**Ids=400mA**



**Ids=350mA**



**Ids=300mA**



[Note] The data for Smith charts were measured at frequency of 2GHz and Tc of 25°C.

Vds=8V Ids=400mA

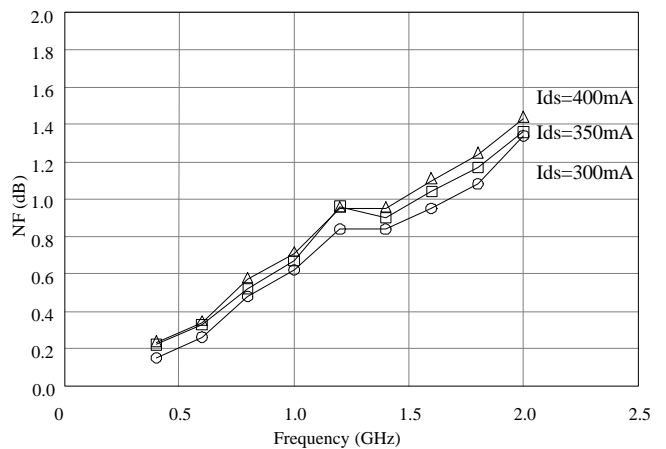
Freq. (GHz)	NFmin (dB)	Gopt Mag	Gopt Ang(deg)	Rn/50	Associated Gain(dB)
0.4	0.23	0.34	-64.4	0.08	21.8
0.6	0.34	0.28	-6.2	0.11	19.4
0.8	0.57	0.26	48.8	0.14	17.7
1.0	0.71	0.35	92.7	0.13	16.6
1.2	0.95	0.41	128.6	0.10	15.6
1.4	0.95	0.51	153.6	0.06	14.9
1.6	1.10	0.55	-178.1	0.04	14.1
1.8	1.24	0.58	-152.3	0.08	13.4
2.0	1.43	0.61	-124.6	0.20	12.9

Vds=8V Ids=300mA

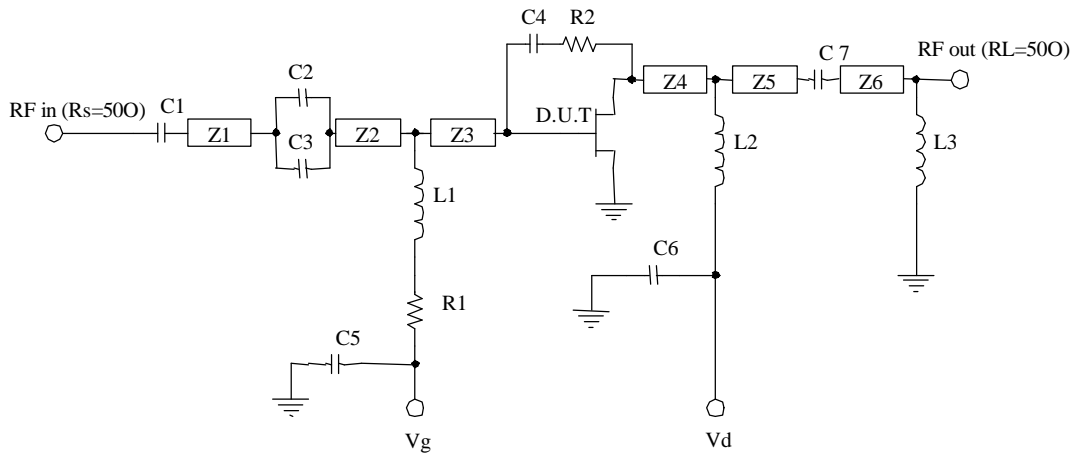
Freq. (GHz)	NFmin (dB)	Gopt Mag	Gopt Ang(deg)	Rn/50	Associated Gain(dB)
0.4	0.15	0.33	-77.9	0.06	21.1
0.6	0.26	0.26	-17.4	0.09	19.0
0.8	0.48	0.19	39.7	0.12	17.1
1.0	0.62	0.30	86.8	0.11	16.1
1.2	0.84	0.34	126.2	0.10	15.1
1.4	0.84	0.45	151.0	0.06	14.4
1.6	0.95	0.50	179.4	0.04	13.7
1.8	1.08	0.54	-154.0	0.06	13.1
2.0	1.34	0.55	-123.9	0.17	12.5

Vds=8V Ids=350mA

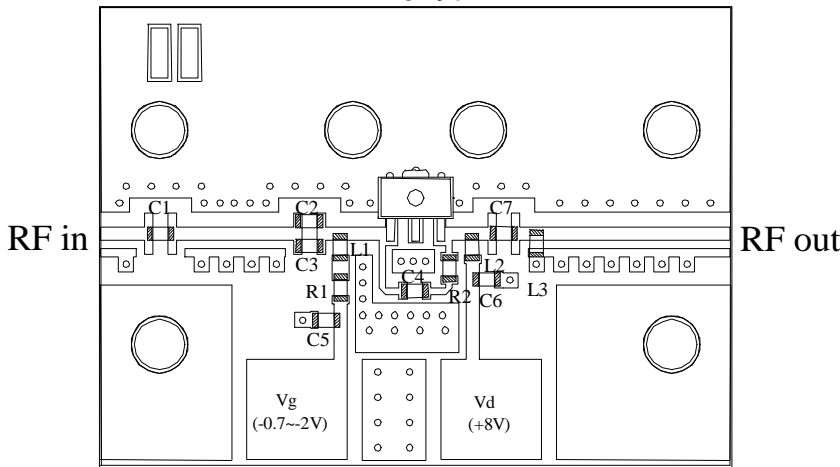
Freq. (GHz)	NFmin (dB)	Gopt Mag	Gopt Ang(deg)	Rn/50	Associated Gain(dB)
0.4	0.22	0.33	-73.8	0.06	21.3
0.6	0.33	0.25	-11.0	0.10	19.2
0.8	0.52	0.21	46.0	0.12	17.4
1.0	0.67	0.33	89.9	0.12	16.4
1.2	0.96	0.36	129.2	0.10	15.3
1.4	0.90	0.48	153.1	0.06	14.7
1.6	1.04	0.52	-179.2	0.04	13.9
1.8	1.17	0.57	-153.2	0.07	13.3
2.0	1.36	0.58	-124.8	0.18	12.7



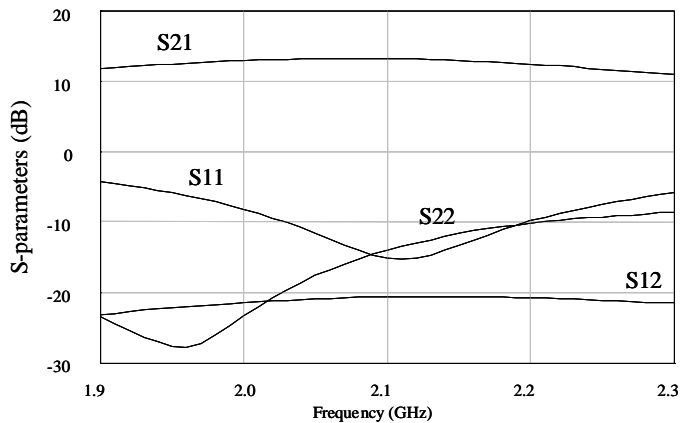
◆ Application Circuit : 2110-2170MHz



KP029J



Ref. Des.	Value	Part Number
R1	82Ω	SUSUMU
R2	820Ω	RR0816 series
C1	3pF	MURATA GRM18 series
C2	1pF	
C3	0.5pF	
C4	4pF	
C5	1μF	
C6	1μF	
C7	2pF	
L1	22nH	TOKO LL1608 series
L2	22nH	
L3	4.7nH	



Ref. Designator	Electrical length @ 2.1GHz (deg)
Z1	31.76
Z2	4.08
Z3	13.61
Z4	8.62
Z5	6.38
Z6	4.54

All microstrip lines have a line impedance of 50Ω.



# P0120009P

Technical Note

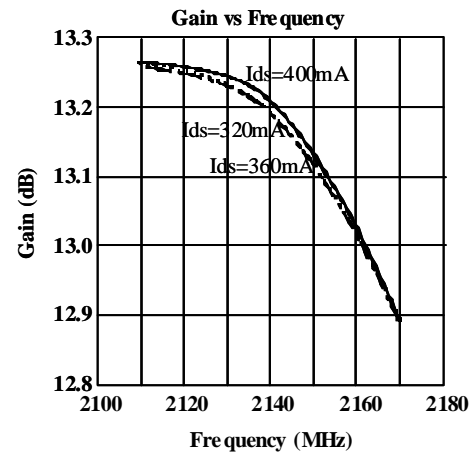
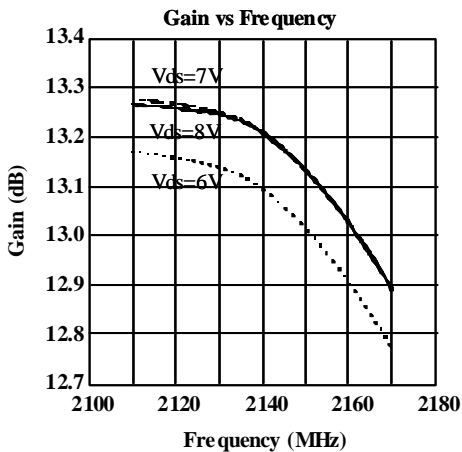
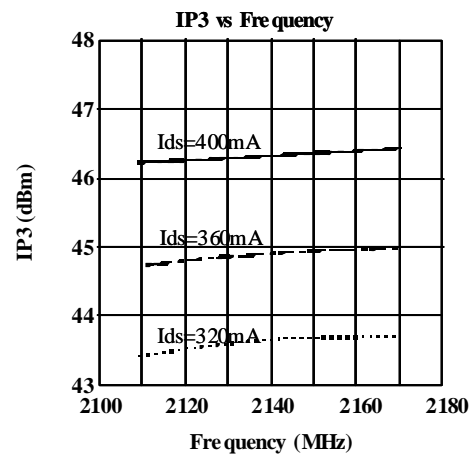
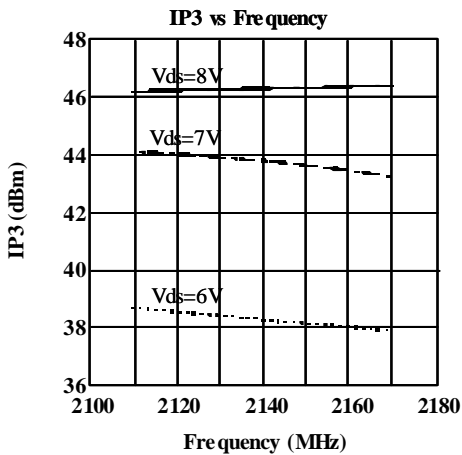
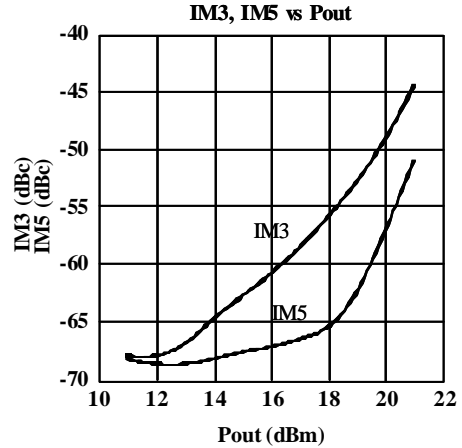
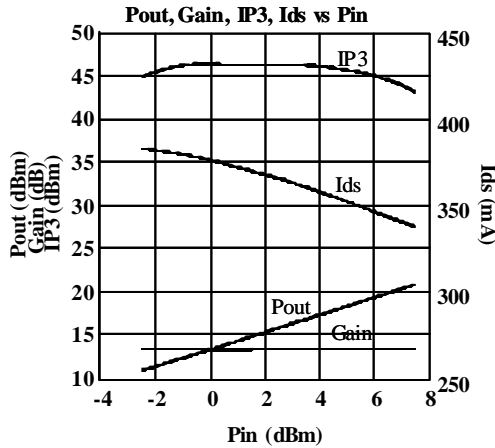
## 2W GaAs Power FET (Pb-Free Type)

### [Typical Performance]

KP029J Application Circuit

V<sub>ds</sub>=8V, I<sub>ds</sub>=400mA, T<sub>c</sub>=25°C

Frequency characteristics were measured with P<sub>out</sub> at 17dBm.

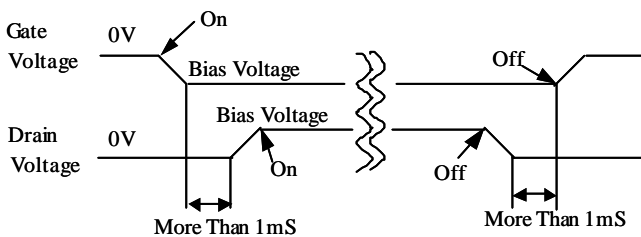




#### ◆ Caution: Power Supply Sequence

For safe operation, electric power should be supplied in following sequence. First, the negative voltage should be applied on the gate, and the voltage should be more negative than the pinch-off voltage when you turn on the power supply. Then, drain bias can be applied. Finally, you can turn on the RF signal.

When turning off the power supply, the sequence should be (1)RF signal (2)Drain (3)Gate.



#### ◆ Bias Circuit

##### [Passive Biasing]

If you use a fixed bias circuit, you sometimes need to control the gate bias to get the same  $I_{ds}$ , since the devices have some margin of pinch-off voltage ( $V_p$ ) variation depending on the wafer lots. If you employ a fixed  $V_{gs}$  biasing for your system, you should closely monitor the drain current, particularly when new wafer lots are introduced.

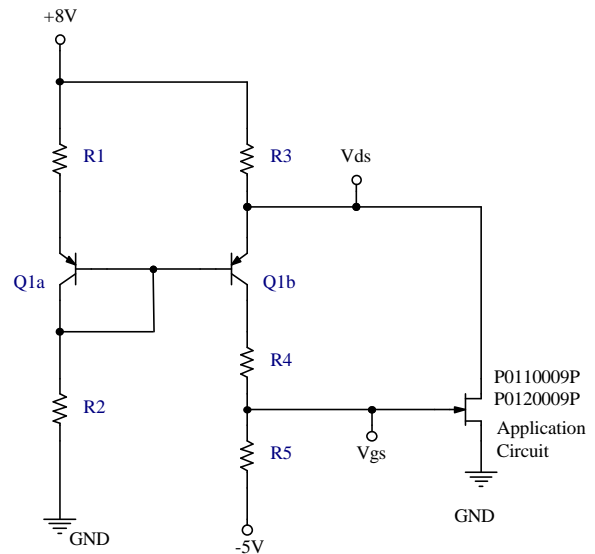
##### [Active Biasing]

We recommend using an active bias circuit, which can eliminate the influence of  $V_p$  variation. An example of an active bias circuit called "current mirror" is shown below. Here, two PNP transistors having the minimum variation of  $I_{be}$  characteristics are used. These transistors adjust  $V_{gs}$  by changing  $V_{ds}$  automatically. It will realize the constant current characteristics, regardless of the temperature.

The circuit should be connected directly in line with where the voltage supplies would be normally connected with the application circuit. Of course a matching circuit is required, but it is not shown in this figure.

##### [Note]

In the measurements of RF performance ( $P_{out}$  vs  $P_{in}$ , etc) using the application circuit described before, the active bias circuit herein was not utilized. The application circuits were biased directly from two power supplies.



$V_{ds}$	+7.9V
$I_{ds}$	400mA
Q1	UMT1N (Rohm)
R1	200 1/10W
R2	2.4kO 1/10W
R3	0.15O RL series (SUSUMU)
R4	1kO 1/10W
R5	1.3kO 1/10W

If you used  $I_{ds}$  other than 400mA, you can calculate the resistance values as follows:

R4 set to be 1kO

$I_1$ :  $I_c$  of Q1a     $I_2$ :  $I_c$  of Q1b

$V_{be1}$ :  $V_{be}$  of Q1a     $V_{be2}$ :  $V_{be}$  of Q1b

$$R1 = (+8V - V_{ds} + V_{be2} - V_{be1}) / I_1 = (+8V - V_{ds}) / I_1$$

$$R2 = (V_{ds} - V_{be2}) / I_1$$

$$R3 = (+8V - V_{ds}) / (I_{ds} + I_2)$$

$$R5 = |-5V - V_{gs}| / I_2$$

#### ◆ Attention to Heat Radiation

In the layout design of the printed circuit board (PCB) on which the power FETs are attached, the heat radiation to minimize the device junction temperature should be taken into account, since it significantly affects the MTTF and RF performance. In any environment, the junction temperature should be lower than the absolute maximum rating during the device operation and it is recommended that the thermal design has enough margin.

The junction temperature can be calculated by the following formula.

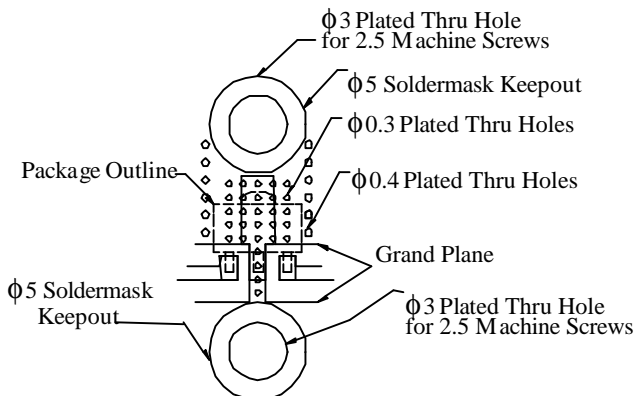
$$T_{jmax} = (V_{ds} \cdot I_{ds} - P_{out}) (R_{th} + R_{board} + R_{hs}) + T_a$$

- $P_{out}$ : Output power
- $R_{th}$ : Thermal resistance between channel and case
- $R_{board}$ : Thermal resistance of PCB
- $R_{hs}$ : Thermal resistance of heat sink
- $T_a$ : Ambient temperature
- $T_{jmax}$ : Maximum junction temperature

Generally, there are two ways of heat radiation. One is the plated thru hole and the other is the heat sink. Key points will be illustrated in each case below. Note that no measure against oscillation is adopted in the figures. In the design of circuit and layout, you should take stabilizing into account if necessary.

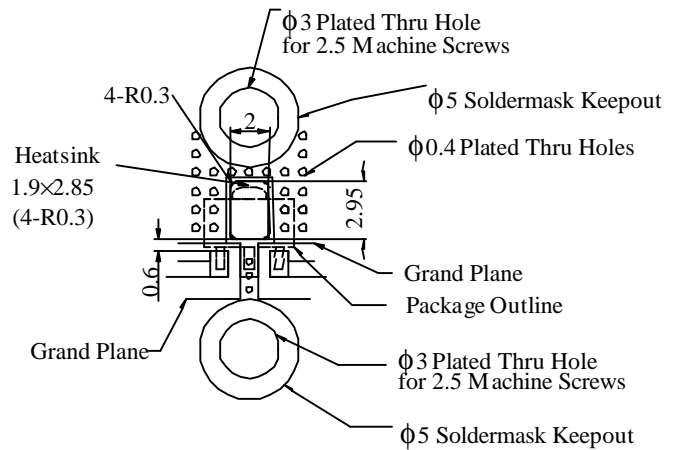
#### [Using Thru Hole]

- ? Multiple plated thru holes are required directly below the device.
- ? The PCB is screwed on the mounting plate or the heat sink to lower the thermal resistance of the PCB.
- ? Lay out a large ground pad area with multiple plated thru holes around pin 4 of the device.
- ? The required matching and feedback circuit described in the application circuit examples should be connected to the device, although it is not shown in the figure below.



#### [Using Heat Sink]

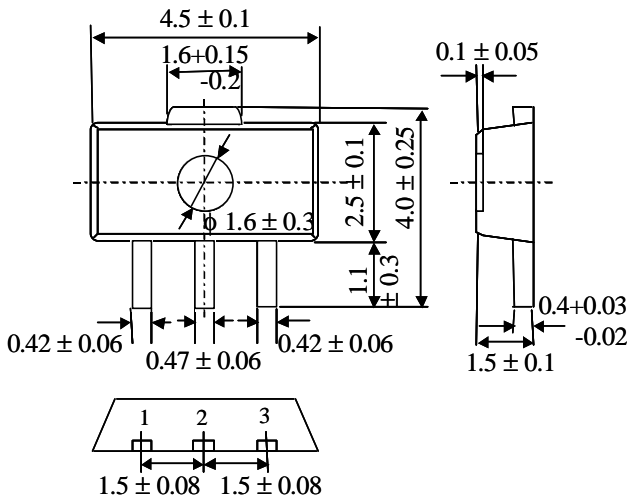
If you cannot get the junction temperature lower than the absolute maximum rating only with the plated thru holes, then you need to employ the heat sink. Attaching the heat sink directly under pin 4 of the device improves the thermal resistance between junction and ambient.



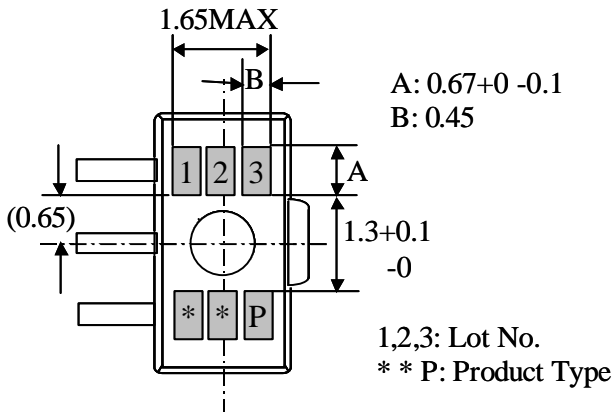
#### [Note]

- ? Ground/thermal vias are critical for the proper device performance. Drills of the recommended diameters should be used in the fabrication of vias.
- ? Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
- ? Mounting screws can be added near the part to fasten the board to heat sink. Ensure that the ground/thermal via region contacts the heat sink.
- ? Do not put solder mask on the backside of the PCB in the region where the board contacts the heat sink.
- ? RF trace width depends upon the PCB material and construction.
- ? Use 1 oz. Copper minimum.

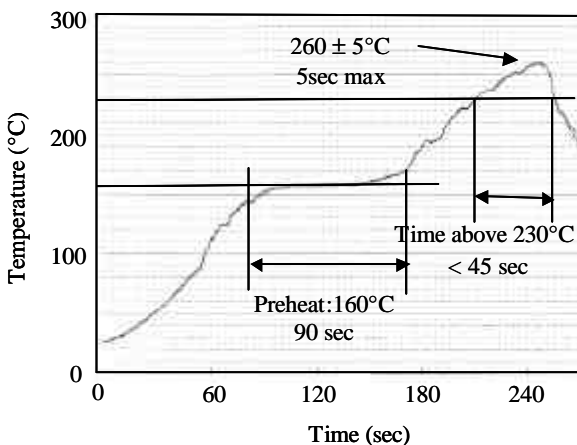
◆ **Package Drawing**



◆ **Laser Marking**



◆ **Convection Reflow Profile (Recommended)**



[Note]

*The reflow profile is different from the one for Sn-Pb plating.*

If you use a soldering iron to attach the devices, please beware of the followings.

- (1) The tip of the iron should be grounded. Or you should use an iron that is electrostatic discharge proof.
- (2) The temperature of the iron tip should be lower than  $240^\circ\text{C}$  and the soldering should be completed within 10 seconds.

◆ **Attention to ESD**

Generally, GaAs devices are very sensitive to electrostatic discharge (ESD). To reduce the ESD damage, please pay attention to the followings. The devices should be stored with the electrodes short-circuited by conductive materials. The workstation and tools should be grounded for safe dissipation of the static charges in the environment. The workpeople are to wear anti-static clothing and wrist straps. For safety reasons, resistance of  $10\text{M}\Omega$  or so should exist between workpeople and ground.

◆ **Attention to Moisture**

The moisture sensitivity level (MSL) of P0120009P is 3, which means that the “floor life” is 168 hours below  $30^\circ\text{C}$  with relative humidity (Rh) of 60%. The devices are usually shipped in moisture-resistant alumina-laminated packages. After breaking the packages, they are to be stored under normal temperature and humidity ( $5\text{-}35^\circ\text{C}$ ,  $45\text{-}75\%$ ), with no corrosive gases or dust in the environment. Assemble the devices within 168 hours after breaking the package, or you have to bake them at  $85^\circ\text{C}$  for 24 hours before assembling.

◆ **Reliability and Environmental Issues**

The detailed reliability information can be seen in *Reliability and Quality Assurance*, which you can download from our web site.

Eudyna’s Yokohama Works, where the devices are manufactured, has been accredited ISO-14001 since 1999. We control the toxic materials in our products in accordance with PRTR regulation.

◆ **Lead and Fluoride**

To realize Pb-free products, Sn-Bi is used for the lead frame plating. Any fluoride that has been determined by the Montreal agreement is not used in the products.

**◆ Caution**

GaAs FET chips are used in P0120009P. For safety reasons, you should attend to the following matters:

- (1) Do not put the products in your mouse.
- (2) Do not make the products into gases or powders, by

burning, breaking or chemical treatments.

- (3) In case you abandon the products, you should obey the related laws and regulations.

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