TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM6N17FU

High Speed Switching Applications

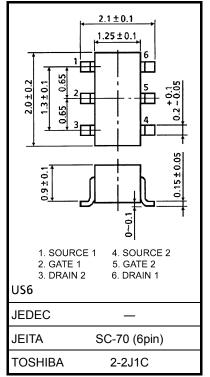
Analog Switch Applications

- Suitable for high-density mounting due to compact package
- High drain-source voltage
- High speed switching

Absolute Maximum Ratings (Ta = 25°C) (Q1, Q2 Common)

| Characteristics | | Symbol | Rating | Unit | |
|-------------------------------------|-------|-------------------------|---------|------|--|
| Drain-Source voltage | | V _{DS} | 50 | V | |
| Gate-Source voltage | | V _{GSS} | ±7 | V | |
| Drain current | DC | I _D | 100 | mA | |
| | Pulse | I _{DP} | 200 | | |
| Drain power dissipation (Ta = 25°C) | | P _D (Note 1) | 200 | mW | |
| Channel temperature | | T _{ch} | 150 | °C | |
| Storage temperature range | | T _{stg} | -55~150 | °C | |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

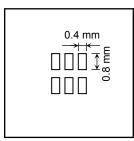


Weight: 6.8 mg (typ.)

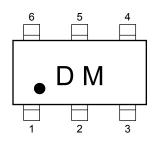
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling

Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

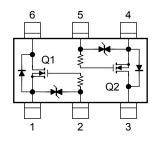
Note 1: Total rating,Mounted on FR4 board (25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 0.32 mm² × 6)



Marking



Equivalent Circuit



This transistor is a electrostatic sensitive device. Please handle with caution.

Unit: mm

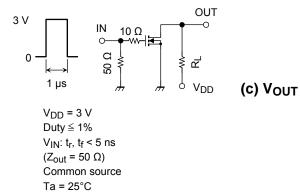
Electrical Characteristics (Ta = 25°C) (Q1, Q2 Common)

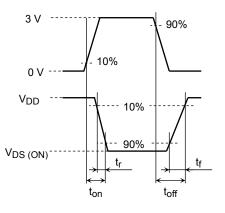
| Characteristics | | Symbol | Test Condition | Min | Тур. | Max | Unit |
|--------------------------------|---------------|----------------------|---|-----|------|-----|------|
| Gate leakage current | | I _{GSS} | $V_{GS} = \pm 7 V, V_{DS} = 0$ | _ | _ | ±5 | μA |
| Drain-Source breakdown voltage | | V (BR) DSS | I _D = 0.1 mA, V _{GS} = 0 | 50 | _ | _ | V |
| Drain cut-off curre | ent | I _{DSS} | V _{DS} = 50 V, V _{GS} = 0 | _ | _ | 1 | μA |
| Gate threshold vo | ltage | V _{th} | V _{DS} = 3 V, I _D = 1 μA | 0.9 | _ | 1.5 | V |
| Forward transfer | admittance | Y _{fs} | V _{DS} = 3 V, I _D = 10 mA | 20 | 40 | _ | mS |
| Drain-Source ON resistance | | R _{DS (ON)} | I _D = 10 mA, V _{GS} = 4 V | _ | 12 | 20 | Ω |
| | | | I _D = 10 mA, V _{GS} = 2.5 V | _ | 22 | 40 | |
| Input capacitance | | C _{iss} | V _{DS} = 3 V, V _{GS} = 0, f = 1 MHz | _ | 7 | _ | pF |
| Reverse transfer capacitance | | C _{rss} | | _ | 3 | _ | pF |
| Output capacitance | | C _{oss} |] | _ | 7 | _ | pF |
| Switching time | Turn-on time | t _{on} | V _{DD} = 3 V, I _D = 20 mA, V _{GS} = 0~3 V, R _G = 10 Ω, R _L = 150 Ω | - | 100 | _ | ns |
| | Turn-off time | t _{off} | | — | 40 | — | |

Switching Time Test Circuit

(a) Test circuit

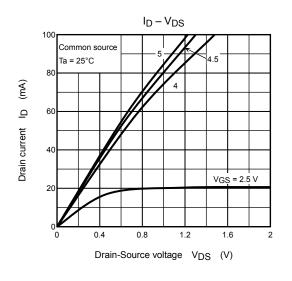
(b) V_{IN}

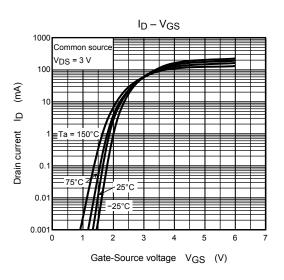


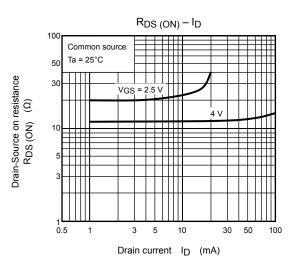


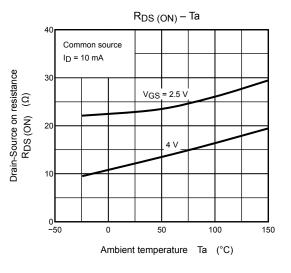
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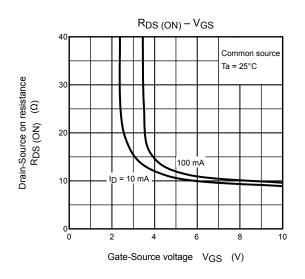
(Q1, Q2 Common)

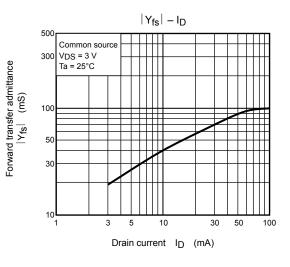






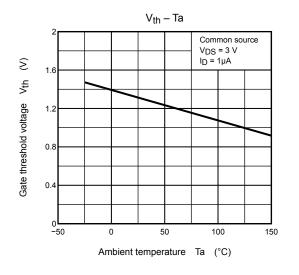


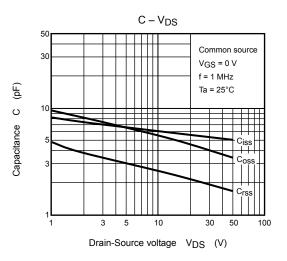


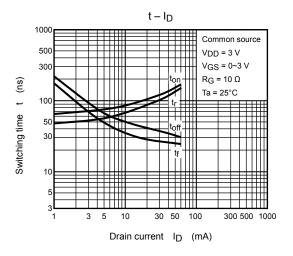


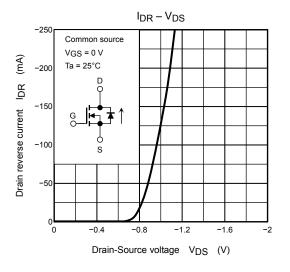
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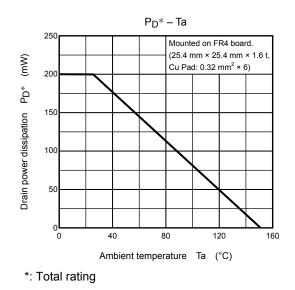
(Q1, Q2 Common)











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